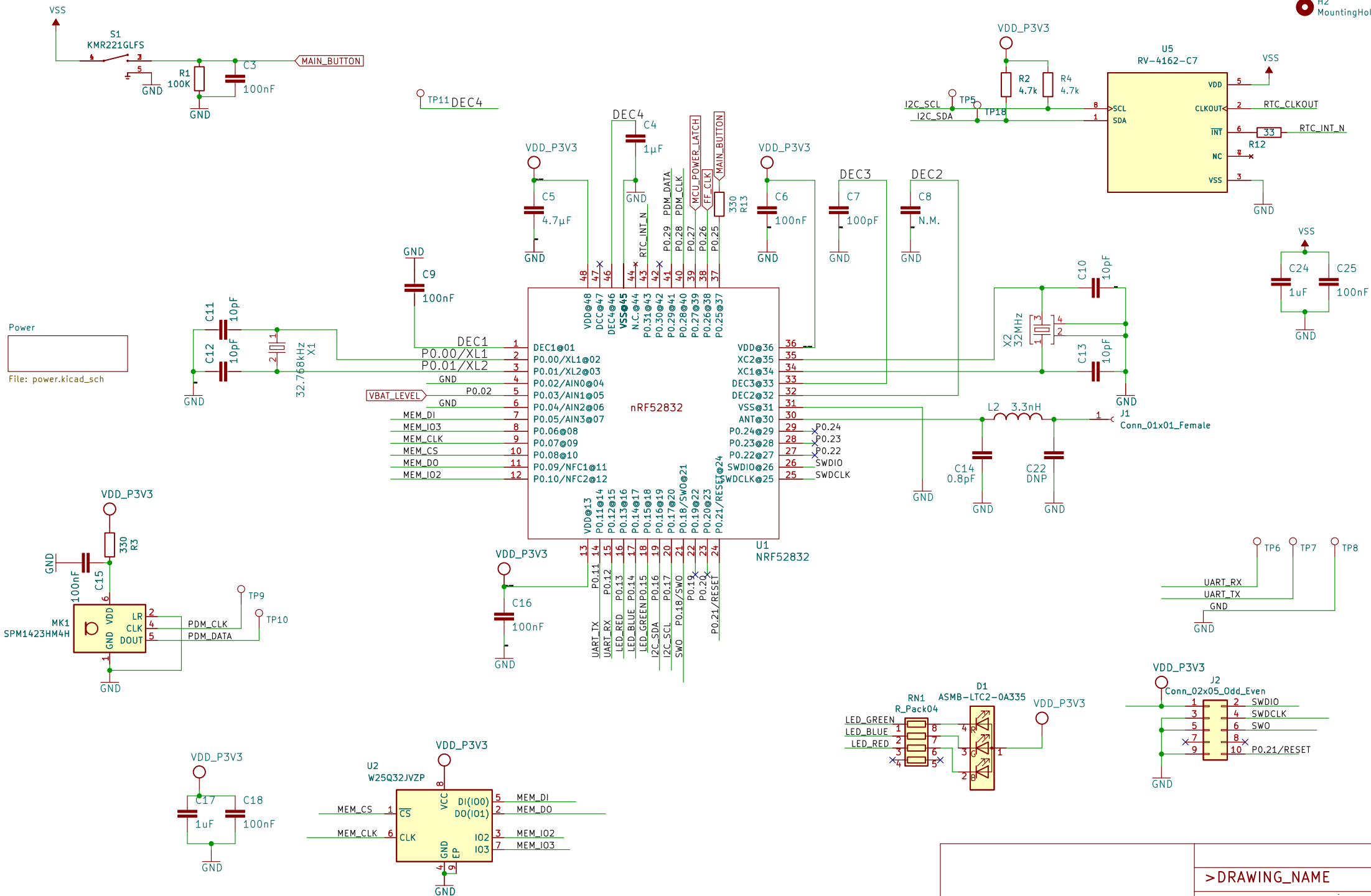


H1
MountingHole

H2
MountingHole



Reference schematic for the DC-DC.
 Calculated efficiency: 89%
 Calculated using
<https://webench.ti.com/wb5/PartDesigner/quickview.jsp>.
 Vin 3.4..4.2V, target I=0.1A or less

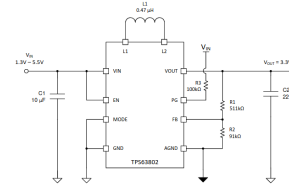
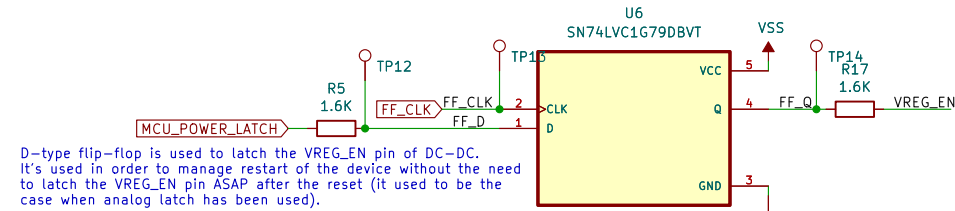
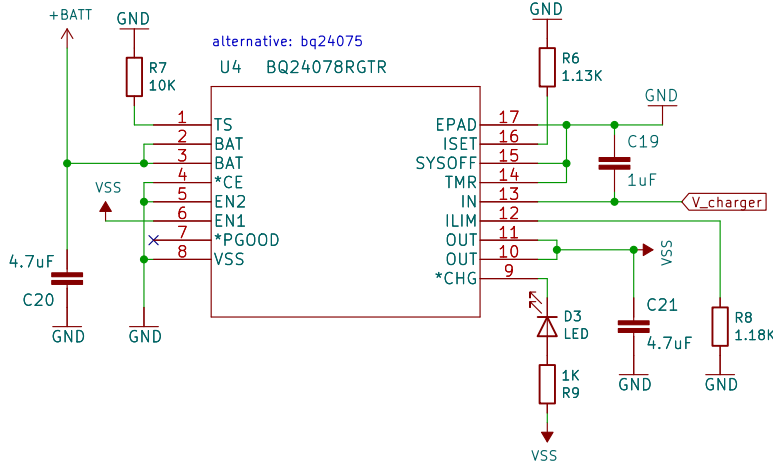
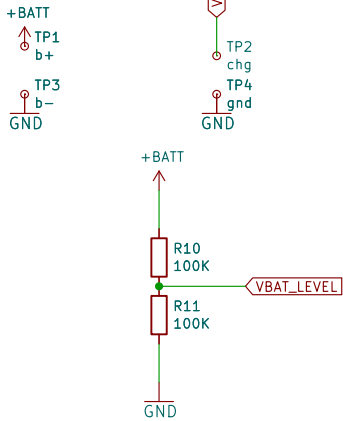
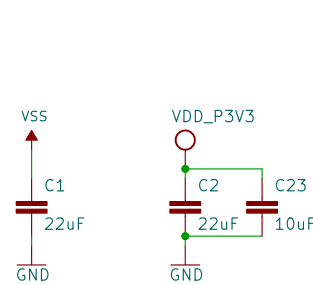
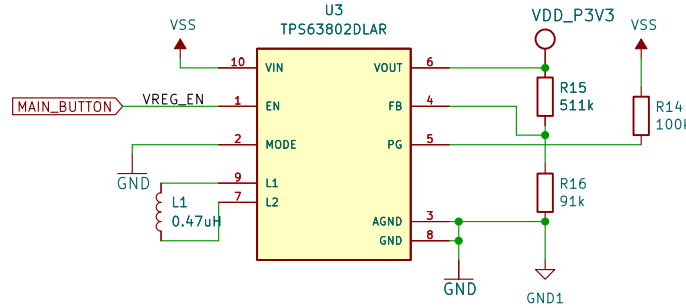


Figure 10-1. 3.3 V_{OUT} Typical Application



D-type flip-flop is used to latch the VREG_EN pin of DC-DC. It's used in order to manage restart of the device without the need to latch the VREG_EN pin ASAP after the reset (it used to be the case when analog latch has been used).

In order to latch power at startup, MCU should pull MCU_POWER_LATCH pin high and send 1 rising edge on FF_CLK. Pulse duration should be at least 2.5ns

Pull-down and filtering elements are added for latch inputs. Clock has only pull-down resistor, as there isn't enough space for an additional capacitor.

