H1
MountingHole
H2
MountingHole
VSS
S1
KMR221GLFS
BUTTON_INPUT
D5
D_Schottky
VREG_EN
VREG_EN
R1
100K
C3
100nF
GND
GND
VCC
L5
15nH
L3
10uH
U7A
NRF5340-QKAA-R7
C37
1u
C38
1u
C39(NPD)1
100pF
VDD1
DCC
DECR
DECRF
VDD2
DCCD
DECD
VDD3
DCCH
VDDH
VBUS
DECUSB
DECN
DECA
VSS_PAD
VSS
L6
15nH
L4
10uH
C39
1u
C40
1u
C41
2.2u
C45
100n
C43
4.7u
C42
4.7u
C44
1u
GND
VBUS
R20
4.7
C28
100n
C29
100n
C30
100n
C31
100n
C32
100n
C33
100n
C34
100n
C35
100n
C36
N.C
VCC
GND
BUTTON_INPUT
R13
1K
BUTTON_INPUT_MCU
R21
1.6K
C4
100n
GND
U7B
NRF5340-QKAA-R7
NC
XC2
XC1
ANT
RESET
SWDCLK
SWDIO
D-
D+
X2
32MHz
C10
10pF
C13
10pF
GND
L31
ANTENNA
AC31
N_RESET
W31
SWDCLK
AA31
SWDIO
B4
USB_N
B2
USB_P
U5
RV-4162-C7
VDD
CLKOUT
INT
NC
VSS
SCL
SDA
VCC
R2
4.7k
R4
4.7k
I2C_SCL
I2C_SDA
TP5
TP18
R12
330
RTC_INT_N
VSS
GND
R23
1M
R24
100K
R25
330
WAKEUP_RTC
PMOS
Q1
VSS
GND
TP32
RTC_INT_N
ANTENNA
L7
2.2nH
C47
0.7pF
C46
DNP
J1
Conn_01x01_Female
GND
GND
VSS
C24
1uF
C25
100nF
GND
Power
File: power.kicad_sch
FB1
FerriteBead
VBUS
V_charger
100n
C6
1u
C5
100n
C7
GND
J3
USB_B_Micro
VBUS
D+
D-
ID
Shield
GND
USB_P
USB_N
VBUS
R22
4.7k
FerriteBead
100n
C8
FB2
FB3
FerriteBead
GND
GND
VCC
I/O1
I/O2
D1
PRTR5V0U2X
GND
GND
C11
10pF
C12
10pF
32.768kHz
X1
GND
VBAT_LEVEL
RTC_INT_N
PDM_DATA
PDM_CLK
LED_BLUE
LED_RED
LED_GREEN
MEM_IO3
MEM_CLK
MEM_DI
MEM_DO
MEM_CS
BUTTON_INPUT_MCU
U7C
NRF5340-QKAA-R7
P0.00/XL1
P0.01/XL2
P0.02/NFC1
P0.03/NFC2
P0.04/AIN0
P0.05/AIN1
P0.06/AIN2
P0.07/AIN3
P0.08/TRACEDATA[3]/SCK
P0.09/TRACEDATA[2]/MOSI
P0.10/TRACEDATA[1]/MISO
P0.11/TRACEDATA[0]/CSN
P0.12/TRACECLK/DCX
P0.13/IO[0]
P0.14/IO[1]
P0.15/IO[2]
P0.16/IO[3]
P0.17/SCK
P0.18/CSN
P0.19
P0.20
P0.21
P0.22
P0.23
P0.24
P0.25/AIN4
P0.26/AIN5
P0.27/AIN6
P0.28/AIN7
P0.29
P0.30
P0.31
U7D
NRF5340-QKAA-R7
P1.00
P1.01
P1.02/TWI
P1.03/TWI
P1.04
P1.05
P1.06
P1.07
P1.08
P1.09
P1.10
P1.11
P1.12
P1.13
P1.14
P1.15
I2C_SCL
I2C_SDA
FF_CLK
MEM_IO2
MCU_POWER_LATCH
UART_RX
UART_TX
J5
Conn_01x03_Socket
DBG_RX
DBG_TX
UART_RX
UART_TX
GND
VCC
330
R15
MK1
CMM-4737DT
LR
CLK
DOUT
VDD
GND
PDM_CLK
PDM_DATA
C15
100nF
TP9
TP10
GND
VCC
C17
1uF
C18
100nF
GND
U2
W25Q128JWPIQ
CS
CLK
DI(IO0)
DO(IO1)
IO2
IO3
GND
EP
VCC
MEM_CS
MEM_CLK
MEM_DI
MEM_DO
MEM_IO2
MEM_IO3
GND
TP31
TP6
TP7
TP30
TP8
UART_RX
UART_TX
GND
GND
VCC
TP21
TP22
TP11
TP20
TP3
TP17
TP19
TP1
SWDIO
SWDCLK
TP28
TP29
N_RESET
GND
RN3
R_Pack04
D4
ASMB-LTC2-0A335
LED_GREEN
LED_BLUE
LED_RED
VCC
Sheet: /
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Title:
Size: A3
Date:
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1
Rev:
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Sheet: >SHEET

Reference schematic for the DC-DC.
Calculated efficiency: 92%
Calculated using
https://webench.ti.com/wb5/PartDesigner/quickview.jsp,
Vin 2.5..5.5V, target I=0.1A or less

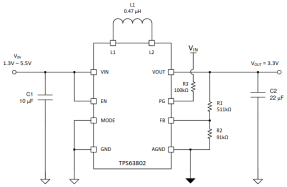

Figure 10-1. 3.3 V_{OUT} Typical Application

J4
Conn_01x02_Socket
+BATT
GND

WAKEUP_RTC
VREG_EN

U3
TPS63802DLAR
VIN
EN
MODE
L1
L2
VOUT
FB
PG
AGND
GND
L1
0.47uH
255k
R15
R16
91k
R14
100k
C1
22uF
C2
22uF
C23
10uF
VSS
VCC
GND1

TP24
TP25
TP27
TP28
TP26
V_charger
TP19

V_charger
TP2
chg
TP4
gnd

R10
1M
R11
1M
VBAT_LEVEL

alternative: bq24075
U4 BQ24078RGTR
TS
BAT
BAT
*CE
EN2
EN1
*PGOOD
VSS
EPAD
ISET
SYSOFF
TMR
IN
ILIM
OUT
OUT
*CHG
R7
10K
R6
1.13K
C19
1uF
C20
4.7uF
C21
4.7uF
R8
1.18K
D3
LED
1K
R9

U6
SN74LVC1G79DBVT
VCC
CLK
D
Q
GND
R5
1.6K
R17
1.6K
TP12
TP13
TP14
FF_CLK
FF_D
FF_Q
MCU_POWER_LATCH
VREG_EN

D-type flip-flop is used to latch the VREG_EN pin of DC-DC.
It's used in order to manage restart of the device without the need to latch the VREG_EN pin ASAP after the reset (it used to be the case when analog latch has been used).

In order to latch power at startup, MCU should pull MCU_POWER_LATCH pin high and send 1 rising edge on FF_CLK. Pulse duration should be at least 2.5ns

Pull-down and filtering elements are added for latch inputs.
Clock has only pull-down resistor, as there isn't enough space for an additional capacitor.

R19
100K
R18
100K
C27
100nF
TP16
C26
1uF

Sheet: /Power/
File: power.kicad_sch

Title:

Size: A4 | Date: | **Rev:**
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