Runyang Tian

San Diego, CA r3tian@ucsd.edu 858-405-7762 Homepage

Education

University of California San Diego *09/2024-06/2026*

- M.S. in Electrical Engineering, GPA: 3.5/4.0
- Courses: Computer Architecture, VLSI for ML, VLSI Physical Design, VLSI Testing, CMOS IC Lab

Xi'an Jiaotong University *09/2020-06/2024*

- B.E. in Microelectronic, GPA: 3.5/4.0
- Courses: Digital Integrated Circuits, Analog Integrated Circuits, C Programming, Computer Architecture

Skills

Languages: Verilog, System Verilog, Python, C/C++, MATLAB, SPICE, TCL

Tools: Cadence Virtuoso, Cadence Innovus, Synopsys DC, Altium, Xcelium, Vivado, HSpice, Linux

Publications

[1] Y. Chen*, R. Tian*, Y. Pan, Z. Li, W. Xu, T. Rosing, "CHIME: Chiplet-based Heterogeneous Near-Memory Acceleration for Edge Multimodal LLM Inference," 2026 Design, Automation & Test in Europe (DATE). (accepted)

[2] Y. Chen*, Z. Li*, K. Fan, R. Tian, J. Hsu, M. Zhou, T. Rosing, "RAPID-Graph: Recursive All-Pairs Shortest Paths Using Processing-in-Memory for Dynamic Programming on Graph," 2026 Design, Automation & Test in Europe (DATE). (accepted)

[3] Y. Chen, R. Tian, Z. Li, W. Xu, M. Afarin, W. Xu, T. Rosing, "GEN-Graph: A Heterogeneous PIM Architecture for Diverse Computational Patterns in Graph-based Dynamic Programming", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. (submitted)

[4] Q. Zhao, Y. Chen, S. Pinge, R. Tian, A. Vega, S. Gupta, S.Holmes, T. Rosing, "HDDB: Efficient In-Storage Database Search Using Hyperdimensional Computing on Ferroelectric NAND Flash", 2026 Design Automation Conference (DAC). (submitted)

[5] R. Tian*, Y. Chen*, R. Nafde, W. Xu, "SALUTE: Sparse-Aware LUT-Based Near-Memory Acceleration for Edge Multimodal LLM", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. (in progress)

Research Experience

At SEELab, UCSD, Advisor: Prof. Tajana Rosing

Sparse-Aware LUT-Based NMP Acceleration for Edge LLM Inference *09/2025-now*

- Simulated and analyzed performance of MAC-basd/LUT-basd NMP/PIM acceleration methods.
- Developed LUT-based Processing Engine (LUT-PE) in NMP accelerator that leverages mixed-precision lookup to avoid redundant operations.
- Designed Progressive Token Elimination Unit (PTEU) to dynamically prune tokens during inference.

Heterogeneous Near-Memory Acceleration for Edge LLM Inference *06/2025-09/2025*

- Proposed a compiler-supported near-memory accelerator that integrates monolithic 3D DRAM (low-latency, high-endurance) and 3D RRAM (high-density, low-refresh-energy) chiplets.
- Proposed a mapping and scheduling framework for heterogeneous near-memory kernels.
- Built a in-house cycle- and energy-accurate simulator to evaluate performance.

Recursive All-Pairs Shortest Paths Using PIM on Graph *05/2025-06/2025*

- Developed RTL modules and synthesized using 40nm CMOS technology, including a custom permutation unit, min-comparator tree, and controller.

- Contributed to a PIM-based system for all-pairs shortest paths with algorithm–architecture co-optimization.

In-Storage Database Search Using HDC on Ferroelectric NAND Flash *11/2025*

- Design peripherals to implement binding (XOR) and arithmetic operations (SUM, AVG, MIN, MAX).
- Modeled and optimized the energy efficiency of the peripherals.

At OEIC Lab, XJTU, Advisor: Prof. Dan Li

Design and Optimization of Optoelectronic Interface Driver *03/2024-06/2024*

- Designed a MZI-based optical DAC with binary-weighted phase control and LUT-based linearity optimization unit.
- Developed a linear driver array driving an 8-bit optical DAC to operate at 1GHz, while achieving electronic-optical speed matching with TSMC 28nm CMOS process.
- Reduced linearity from 10.8% to 1.8%, improved INL from 26 to 5 LSB, the power was 9.81mW.
- Outstanding Graduation Thesis Nomination.

Projects

9-bit SAR ADC Design and Tape-Out *03/2025-05/2025, 09/2025-11/2025*

- Designed the schematic and layout applying dummy devices, common centroid pattern, and power shielding to minimize mismatch and noise. Monte Carlo simulation showed 2mV offset and 0.01% capacitor mismatch.
- Developed the SAR controller in Verilog, synthesized using Genus and PnR with Innovus.
- Designed PCB for testing the chip, includes a Anti-Alias Filter, SE to DE converter.

TinyCPU: Single-Stage Single-Issue 9-bit Microprocessor *03/2025-06/2025*

- Developed an accumulator-based architecture to meet compact 9-bit instruction encoding constraint.
- Defined a custom ISA that supports arithmetic, logic, branch, jump and load-store operations in six instruction formats (SR, LS, SI, DR, RI, J).
- Designed control logic and datapath, implementing floating-point to fixed-point conversion program on TinyCPU.

Reconfigurable 2D Systolic-Array NPU Design *09/2024-12/2024*

- Implemented RTL design and functional verification for MAC core, input/output, FIFO, SRAM, and special function unit (SFU), supporting convolution, matrix multiplication, normalization, and ReLU operators.
- Designed a dual-core architecture with cross-clock-domain data transfer via FIFOs, and developed control logic to switch between weight-stationary and output-stationary modes.
- Designed a 1D version and completed synthesis, STA, and PnR in TSMC 65 nm technology, optimizing PPA through multi-cycle paths, pipelining, and clock gating.

FAST-9 Corner Detection Algorithm Accelerator *07/2023-08/2023*

- Developed RTL design for buffer, detection and non-maximum suppression modules to process image.
- Designed corner detection as a 4-stage pipeline (difference value, absolute value, threshold compare, result) to improve throughput.

Awards

Outstanding Graduate Award	*2024*
Outstanding Student Award	*2021-2023*
MCM/ICM Honorable Mentioned	*05/2022*
University Essay Writing Competition Second Prize	*11/2021*