Runyang Tian

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Education

University of California, San Diego 09/2024-06/2026
Master of Science in Electrical and Computer Engineering, GPA 3.5/4.0

Xi'an Jiaotong University 09/2020-06/2024
Bachelor of Engineering in Microelectronic, GPA 3.5/4.0

Skills

Languages: Python, Verilog, System Verilog, C, MATLAB, TCL

Tools: Cadence Virtuoso, Cadence Innovus, Synopsys DC, Xcelium, Vivado, HSpice, Linux

Research Experience

Heterogeneous Near-Memory Accelerator for Multimodal-LLM 06/2025-09/2025
Advisor: Prof. Tajana Rosing *UCSD*

- Designed and evaluated CHIME, a compiler-supported near-memory accelerator that integrates monolithic 3D DRAM (low-latency, high-endurance) and 3D RRAM (high-density, low-refresh-energy) chiplets to optimize MLLM inference on edge devices.
- Developed a simulator integrating device-level DRAM/RRAM models, compiler-based operator mapping and scheduling, and analytical performance models to accurately predict runtime, energy, and power.
- Achieved 54× speedup and 533× energy efficiency over NVIDIA Jetson Orin NX, sustaining 233–533 tps at 2W.
- Submitted to DATE '26.

Projects

9-bit SAR ADC Design and Tape-out 03/2025-06/2025

- Designed the schematic and layout applying dummy devices, common centroid pattern, and power shielding to minimize mismatch and noise. Monte Carlo simulation showed 2mV offset and 0.01% capacitor mismatch.
- Developed the SAR controller in Verilog, synthesized using Genus and PnR with Innovus.
- Designed pad ring with dummy fill and decoupling capacitors to meet density requirements.

TinyCPU: Single-stage single-issue 9-bit microprocessor 03/2025-06/2025

- Developed an accumulator-based architecture to meet compact 9-bit instruction encoding constraint.
- Defined a custom ISA that supports arithmetic, logic, branch, jump and load-store operations in six instruction formats (SR, LS, SI, DR, RI, J).
- Redesigned control logic and datapath, implementing floating-point to fixed-point conversion program on TinyCPU.

Reconfigurable 2D Systolic-Array NPU Design 01/2025-03/2025

- Implemented RTL design and functional verification for MAC core, input/output FIFO, SRAM, and special function unit (SFU), supporting convolution, matrix multiplication, normalization, and ReLU operators.
- Designed a dual-core architecture with cross-clock-domain data transfer via FIFOs, and developed control logic to switch between weight-stationary and output-stationary modes.
- Completed synthesis, STA, and place-and-route (PnR) in TSMC 65 nm technology, optimizing PPA through multi-cycle paths, pipelining, and clock gating.

FAST-9 Corner Detection Algorithm Accelerator 03/2023-06/2023

- Developed RTL design for buffer, detection and non-maximum suppression modules to process image.
- Designed corner detection as a 4-stage pipeline (difference value, absolute value, threshold compare, result) to improve throughput.