

# Runyang Tian

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## EDUCATION

<b>University of California, San Diego</b> <i>Master of Science in Electrical and Computer Engineering, GPA 3.5/4.0</i>	09/2024-06/2026
<b>Xi'an Jiaotong University</b> <i>Bachelor of Engineering in Microelectronic, GPA 3.5/4.0</i>	09/2020-06/2024

## SKILLS

**Languages:** Python, Verilog, System Verilog, C/C++, MATLAB, SPICE, TCL  
**Tools:** Cadence Virtuoso, Cadence Innovus, Synopsys DC, Xcelium, Vivado, HSpice, Linux

## RESEARCH EXPERIENCE

<b>Sparse-Aware LUT-based NMP Accelerator for Edge Multimodal-LLM</b> <i>Advisor: Prof. Tajana Rosing</i> <ul style="list-style-type: none"><li>Designed Progressive Token Elimination Unit (PTEU) to dynamically prune low-value tokens during inference.</li><li>Developed Sparse-Aware LUT-based Processing Engine (SAL-PE) that leverages mixed-precision lookup and activation sparsity to avoid redundant operations.</li><li>Will be submitted to TCAD, first author.</li></ul>	09/2025-Ongoing <i>SEELab, UCSD</i>
<b>Heterogeneous Near-Memory Accelerator for Multimodal-LLM</b> <i>Advisor: Prof. Tajana Rosing</i> <ul style="list-style-type: none"><li>Proposed a compiler-supported near-memory accelerator that integrates monolithic 3D DRAM (low-latency, high-endurance) and 3D RRAM (high-density, low-refresh-energy) chiplets.</li><li>Proposed a mapping and scheduling methods for heterogeneous near-memory kernels.</li><li>Built a in-house cycle- and energy-accurate simulator to evaluate performance.</li><li>Submitted to DATE '26, co-first author</li></ul>	06/2025-09/2025 <i>SEELab, UCSD</i>
<b>Recursive All-Pairs Shortest Paths Using Processing-in-Memory on Graph</b> <i>Advisor: Prof. Tajana Rosing</i> <ul style="list-style-type: none"><li>Developed RTL modules and synthesized using 40nm CMOS technology, including a custom permutation unit, min-comparator tree, and controller.</li><li>Contributed to a PIM-based system for all-pairs shortest paths (APSP) with algorithm-architecture co-optimization.</li><li>Submitted to DATE '26, collaborator</li></ul>	05/2025-06/2025 <i>SEELab, UCSD</i>

## PROJECTS

<b>9-bit SAR ADC Design and Tape-out</b> <ul style="list-style-type: none"><li>Designed the schematic and layout applying dummy devices, common centroid pattern, and power shielding to minimize mismatch and noise. Monte Carlo simulation showed 2mV offset and 0.01% capacitor mismatch.</li><li>Developed the SAR controller in Verilog, synthesized using Genus and PnR with Innovus.</li><li>Designed pad ring with dummy fill and decoupling capacitors to meet density requirements.</li></ul>	03/2025-06/2025
<b>TinyCPU: Single-stage single-issue 9-bit microprocessor</b> <ul style="list-style-type: none"><li>Developed an accumulator-based architecture to meet compact 9-bit instruction encoding constraint.</li><li>Defined a custom ISA that supports arithmetic, logic, branch, jump and load-store operations in six instruction formats (SR, LS, SI, DR, RI, J).</li><li>Redesigned control logic and datapath, implementing floating-point to fixed-point conversion program on TinyCPU.</li></ul>	03/2025-06/2025
<b>Reconfigurable 2D Systolic-Array NPU Design</b> <ul style="list-style-type: none"><li>Implemented RTL design and functional verification for MAC core, input/output FIFO, SRAM, and special function unit (SFU), supporting convolution, matrix multiplication, normalization, and ReLU operators.</li></ul>	01/2025-03/2025

- Designed a dual-core architecture with cross-clock-domain data transfer via FIFOs, and developed control logic to switch between weight-stationary and output-stationary modes.
- Completed synthesis, STA, and place-and-route (PnR) in TSMC 65 nm technology, optimizing PPA through multi-cycle paths, pipelining, and clock gating.

**Design and Optimization of Optoelectronic Interface Driver**
03/2024-06/2024

- Developed a linear driver array driving an 8-bit optical DAC to operate at 1GHz, while achieving electronic-optical speed matching with TSMC 28nm CMOS process.
- Revamped an optical DAC and created a Digital-digital Converter (DDC) to enhance linearity.
- Improved the power consumption of driver to 9.81mW. Reduced linearity from 10.8% to 1.8%, improved INL from 26 to 5 times the LSB.

**FAST-9 Corner Detection Algorithm Accelerator**
03/2023-06/2023

- Developed RTL design for buffer, detection and non-maximum suppression modules to process image.
- Designed corner detection as a 4-stage pipeline (difference value, absolute value, threshold compare, result) to improve throughput.

AWARDS

Outstanding Graduate Award	2024
Outstanding Student Award	2021-2023
MCM/ICM Honorable Mentioned	05/2022
University Essay Writing Competition Second Prize	11/2021