Runyang Tian

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Education

University of California, San Diego 09/2024-06/2026
Master of Science in Electrical and Computer Engineering, GPA 3.5/4.0

Xi'an Jiaotong University 09/2020-06/2024
Bachelor of Engineering in Microelectronic, GPA 3.5/4.0

Skills

Languages: Python, Verilog, System Verilog, C/C++, MATLAB, SPICE, TCL

Tools: Cadence Virtuoso, Cadence Innovus, Synopsys DC, Xcelium, Vivado, HSpice, Linux

Research Experience

Sparse-Aware NMP LUT-Based Accelerator for Edge Multimodal LLM 09/2025-Ongoing
Advisor: Prof. Tajana Rosing *SEELab, UCSD*

- Designed Progressive Token Elimination Unit (PTEU) to dynamically prune low-value tokens during inference.
- Developed Sparse-Aware LUT-based Processing Engine (SAL-PE) that leverages mixed-precision lookup and activation sparsity to avoid redundant operations.
- Will be submitted to TCAD, first author.

Heterogeneous Near-Memory Accelerator for Multimodal LLM 06/2025-09/2025
Advisor: Prof. Tajana Rosing *SEELab, UCSD*

- Proposed a compiler-supported near-memory accelerator that integrates monolithic 3D DRAM (low-latency, high-endurance) and 3D RRAM (high-density, low-refresh-energy) chiplets.
- Proposed a mapping and scheduling methods for heterogeneous near-memory kernels.
- Built a in-house cycle- and energy-accurate simulator to evaluate performance.
- Submitted to DATE '26, co-first author

Recursive All-Pairs Shortest Paths Using Processing-in-Memory on Graph 05/2025-06/2025
Advisor: Prof. Tajana Rosing *SEELab, UCSD*

- Developed RTL modules and synthesized using 40nm CMOS technology, including a custom permutation unit, min-comparator tree, and controller.
- Contributed to a PIM-based system for all-pairs shortest paths (APSP) with algorithm–architecture co-optimization.
- Submitted to DATE '26, collaborator

Projects

9-bit SAR ADC Design and Tape-Out 03/2025-06/2025

- Designed the schematic and layout applying dummy devices, common centroid pattern, and power shielding to minimize mismatch and noise. Monte Carlo simulation showed 2mV offset and 0.01% capacitor mismatch.
- Developed the SAR controller in Verilog, synthesized using Genus and PnR with Innovus.
- Designed pad ring with dummy fill and decoupling capacitors to meet density requirements.

TinyCPU: Single-Stage Single-Issue 9-bit Microprocessor 03/2025-06/2025

- Developed an accumulator-based architecture to meet compact 9-bit instruction encoding constraint.
- Defined a custom ISA that supports arithmetic, logic, branch, jump and load-store operations in six instruction formats (SR, LS, SI, DR, RI, J).
- Redesigned control logic and datapath, implementing floating-point to fixed-point conversion program on TinyCPU.

Reconfigurable 2D Systolic-Array NPU Design 01/2025-03/2025

- Implemented RTL design and functional verification for MAC core, input/output FIFO, SRAM, and special function unit (SFU), supporting convolution, matrix multiplication, normalization, and ReLU operators.

- Designed a dual-core architecture with cross-clock-domain data transfer via FIFOs, and developed control logic to switch between weight-stationary and output-stationary modes.
- Completed synthesis, STA, and place-and-route (PnR) in TSMC 65 nm technology, optimizing PPA through multi-cycle paths, pipelining, and clock gating.

Design and Optimization of Optoelectronic Interface Driver 03/2024-06/2024

- Developed a linear driver array driving an 8-bit optical DAC to operate at 1GHz, while achieving electronic-optical speed matching with TSMC 28nm CMOS process.
- Revamped an optical DAC and created a Digital-digital Converter (DDC) to enhance linearity.
- Improved the power consumption of driver to 9.81mW. Reduced linearity from 10.8% to 1.8%, improved INL from 26 to 5 times the LSB.

FAST-9 Corner Detection Algorithm Accelerator 03/2023-06/2023

- Developed RTL design for buffer, detection and non-maximum suppression modules to process image.
- Designed corner detection as a 4-stage pipeline (difference value, absolute value, threshold compare, result) to improve throughput.

Awards

Outstanding Graduate Award 2024
Outstanding Student Award 2021-2023
MCM/ICM Honorable Mentioned 05/2022
University Essay Writing Competition Second Prize 11/2021