This document is not indicative of your final exam, but will assist you in critically thinking about topics you learned about over the course of the semester. Please answer these questions briefly (1-2 sentences); however, if at any point you feel that you can't properly answer one of the questions or perhaps think I've ordered something backwards, I urge you to consider thinking past just course slides or perhaps review a little more on the topics presented.

Also, almost all the answers are based on use cases. There are certain situations where one will be better than the other whether this be in terms of time cost, energy cost, money cost, or complexity cost. Please consider all of these when answering each of the following.

I apologize for posting this late and without any answers, I simply don't have time. Instead, I put the location in the lecture slides where you can find more information. I stopped at question 16 though because of time.

1. Why might you want to implement a multi-cycle processor over a single-cycle processor?
    a. I don't know where to find this, but you should still generally know

2. Why might you want to implement a single-cycle processor over a pipelined processor? For this question, a single cycle for the single cycle processor is equivalent in time to five cycles in a 5-stage pipelined processor
    a. All of CSE341 Review Processor Design

3. Why might you want to implement a 15-stage pipelined processor over a 5-stage pipelined processor?
    a. CSE341 Review Processor Design Slides 129-131

4. Why might you want to implement a 1-bit branch predictor over a 3-bit branch predictor?
    a. CSE341 Review Processor Design Slides 84-87

5. Why might you want more levels of cache over less levels of cache before main memory?
    a. CSE341 Memory Slides 4&5

6. Why might you want to implement direct mapped cache over n-way set-associative cache?
    a. CSE341 Memory Slides 19-26, 60-66

7. Why might you want to have a smaller block size over a larger block size in cache?
    a. CSE341 Memory Slides 47&48

8. Why might you want to implement write-through cache over write-back cache?
    a. CSE341 Memory Slides 50&51

9. Why might you want to implement dual issue processing instead of very long instruction words?
    a. Chapter 3 Slides 41-43

10. When might you want to avoid loop unrolling instead of using loop unrolling?
    a. Chapter 3 Slides 11-13

11. Why might you want to implement less multiply and divide reservations stations instead of more multiply and divide reservation stations in Tomasulo's algorithm?
    a. Chapter 3 Slides 28-32
    b. Instruction Level Parallelism Slides 17-67 with edits on Piazza

12. Why might you want to implement consecutive memory storage of vectors over scatter gather vector protocols?
    a. Chapter 4 Slides 15&16

13. Why might you want to implement Snoopy Protocol for cache coherence over Directory Based Protocol for cache coherence?
    a. Chapter 5 Slides 11-13

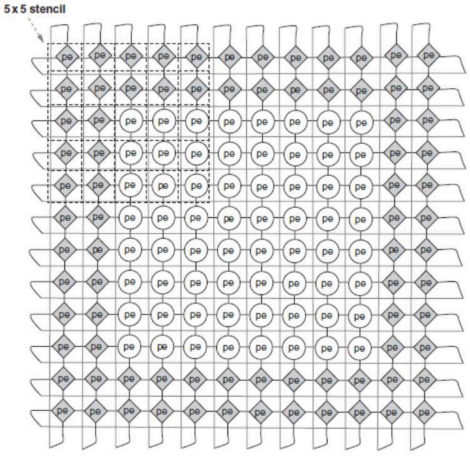
14. Why might you want to use a vector processor over a GPU(graphics processing unit)?
    a. Chapter 4 Slide 25

15. Why might you want to implement a GPU as a peripheral connected to a central processor over implementing the GPU as the central processor?
    a. Chapter 4 Slide 23

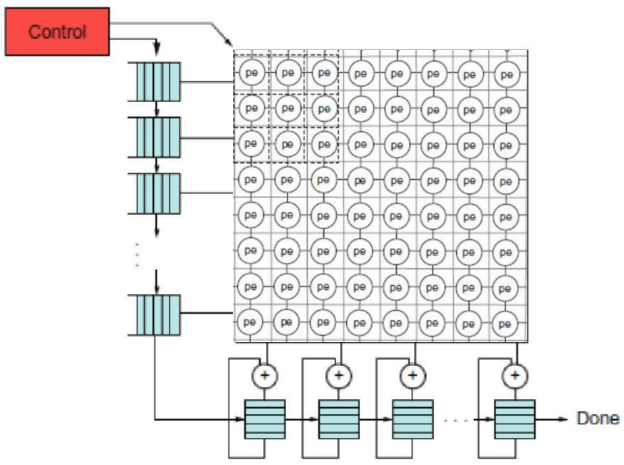
16. Why might you want to implement speculation with branch prediction over without branch prediction? What does without branch prediction even mean in this case?

17. Why might you want to use 1 over 2?

1. Crest (with gray diamonds around outside)



2. TPU (without gray diamonds around outside)



18. Why might you want to implement a centralized warehouse over scattered service-specific smaller computing centers?

19. Why might you want to download software over using cloud computing?

20. Why might you want to use SIMD processors with interconnection network and centralized thread scheduling while implementing a GPU over Tensor Processing Units with the same interconnection network and centralized thread scheduling to implement a GPU?