1

```
addi $v1, $0, #0x1000
add  $v0, $0, $0
addi $s0, $a0, #16      Assume $a0 is
addi $t0, $s0, #16      an arbitrary address
Loop: lw  $t1, -16($s0)
addi $s0, $s0, #4       Instruction Pipeline Format
add  $v0, $v0, $t1
sub  $v1, $v1, $t1
bne  $s0, $t0, Loop
add  $v0, $v0, $v1
```

	IF	ID	EX1	EX2	WB1	MEM1	MEM2	WB2	
lw	50	50	50	—	—	100	150 |	50	450 ps
add	50	50	50 |	—	100				250 ps
bne	50	50	50 ↑	100 |	100				350 ps

These bars represent when data is ready for data forwarding

1a. Using the Instruction Pipeline Format table, determine the single cycle cycle time and pipelined cycle time.

1b. How many ps longer does a single pipelined lw instruction take compared to single cycle? And compared to multi-cycle?

1c. Using data forwarding pipelined execution, identify all hazards in the code above including branch delay hazards.

1d. Use loop unrolling to get rid of the loop in the code above and use register renaming and/or out of order execution to remove or minimize hazards. What is the average CPI with data forwarding pipelined execution?

1e Using dual issue processing with one side only issuing ALU or Branch instructions and the other issuing any instruction, compute the new average CPI. Keep in mind potential hazards following the load and branch instructions

1f. Which locality of cache would make the above program get more hits?

1g. Without implementing locality, would set associative cache affect hit rate in the program above? Why or why not?

2
```
L.d   $f5, 8($f1)
L.d   $f2, 0($f1)
add.d $f8, $f2, $f2
daddui $f4, $0, #4.8
mul.d $f3, $f2, $f3
add.d $f2, $f5, $f8
```

	Busy?	Tag	Data
$f1			1004
$f2			-13
$f3			26
$f4			12.2
$f5			-3.8

Memory

1000	1.9
1004	2.6
1008	5.3
100C	0.6
1010	3.7

2a Identify all data dependencies, output dependencies, and anti-dependencies in this format _____ _____ _____ Ex. $f6 L9 L13
register first line number second line number

2b Fix the dependencies that are fixable using register renaming. Available registers are $f9 – $f15.

2c Using the original code, run Tomasulo's algorithm dual issue with 3 ADD/SUB stations and 2 MUL/DIV stations.
ADD/SUB Execution = 3 cycles
MUL/DIV Execution = 7 cycles
LW/SW Execution = 4 cycles
Assume instructions start execution as soon as data becomes available.
Keep track of reservation stations and the register file.

3 Assume you have a cache of size 1kB using direct mapped cache and byte addressing. Block size is 4 bytes long. Main memory has a size of 16kB. Calculate the number of tag bits, index bits, and offset bits and mark their position on the bitstring below. Remove any unused 0's in your address

00000000000000000000000000000000

4 Given an instruction breakdown of LW/SW = 25%, ALU = 70%, and Branch = 5% where a LW/sw takes 6 cycles, ALU takes 2 cycles, and Branch takes 3 cycles, calculate average CPI. What is the new average CPI if there is an instruction fetch miss rate of 5% with a penalty of 5 cycles, an L1 cache miss rate of 50% with penalty 10 cycles and L2 cache miss rate of 25% with a penalty of 40 cycles.

Ins type	CPI	%
LW/sw)	6	25%
ALU	2	70%
Branch	3	5%