**Table Of I2C Addresses**

Priority UID (1=High)	Board Des	Ref	Purpose	Speed (kHz)	Addr Mask (8 bit)	Address (7-bit / Hex)
1	Display_U301	LED0	I2C	1000	1aaaaaaW	1100111_77
2	Display_U301	LED1	I2C	1000	1aaaaaaW	1100111_78
3	Display_U701	LED2	I2C	1000	1aaaaaaW	1111010_7A
4	Display_U601	LED3	I2C	1000	1aaaaaaW	1111011_7B
5	Display_U701	LED4	I2C	1000	1aaaaaaW	1111100_7C
6	Display_U801	LED5	I2C	1000	1aaaaaaW	1111101_7D
7	Display_U201	LEDOP	I2C	1000	1aaaaaaW	1111110_7E
8	PhysI_U2	LEDPI	I2C	1000	1aaaaaaW	1111111_7F
9	Amb TBD	LUX	Light	400	0010100W	0101001_29
10	Amb SHT35	Humidity	Humidity	1000	000010w	1000101_45
11	Amb STS35	Ambient Temp	Temperature	1000	100101aW	1001011_4B
12	Amb ICP-10111	Pressure	Pressure	400	1100000W	1000001_63
13	Amb VCNL4000	Proximity	Proximity	400	1100000W	1000001_63
14	Main_U25	PCB Temperature	Temperature	3400	1000100W	1001100_4C
15	Main_U26	Power	Power	400	1101000W	1100000_68
16	Main_U28	Amplifier	Amplifier	400	110101aW	1001101_7A
17	Main_U301	V6P0 PI Vsns	VSense	2560	100aaaW	1000000_40
18	Main_U701	V6P0 Amb Vsns	VSense	2560	100aaaW	1000001_41
19	Main_U11	V6P0 Disp Vsns	VSense	2560	100aaaW	1000010_42
20	Main_U14	V12P0 Vsns	VSense	2560	100aaaW	1000100_44
21	Main_U17	V3P3 I2C Vsns	VSense	2560	100aaaW	1000110_46
22	Main_U19	V3P3 Amp Vsns	VSense	2560	100aaaW	1000100_48
23	Main_U21	VDD Amp Vsns	VSense	2560	100aaaW	1000101_49
24	Main_U23	V3P3 BT Vsns	VSense	2560	100aaaW	1000100_4A
25	Main_U24	IO Expander	IO	400	a11xxxxW	0111110_3E

Schematic Top

File: TOP.kicad_sch

2

Title: Clock-Radio Main

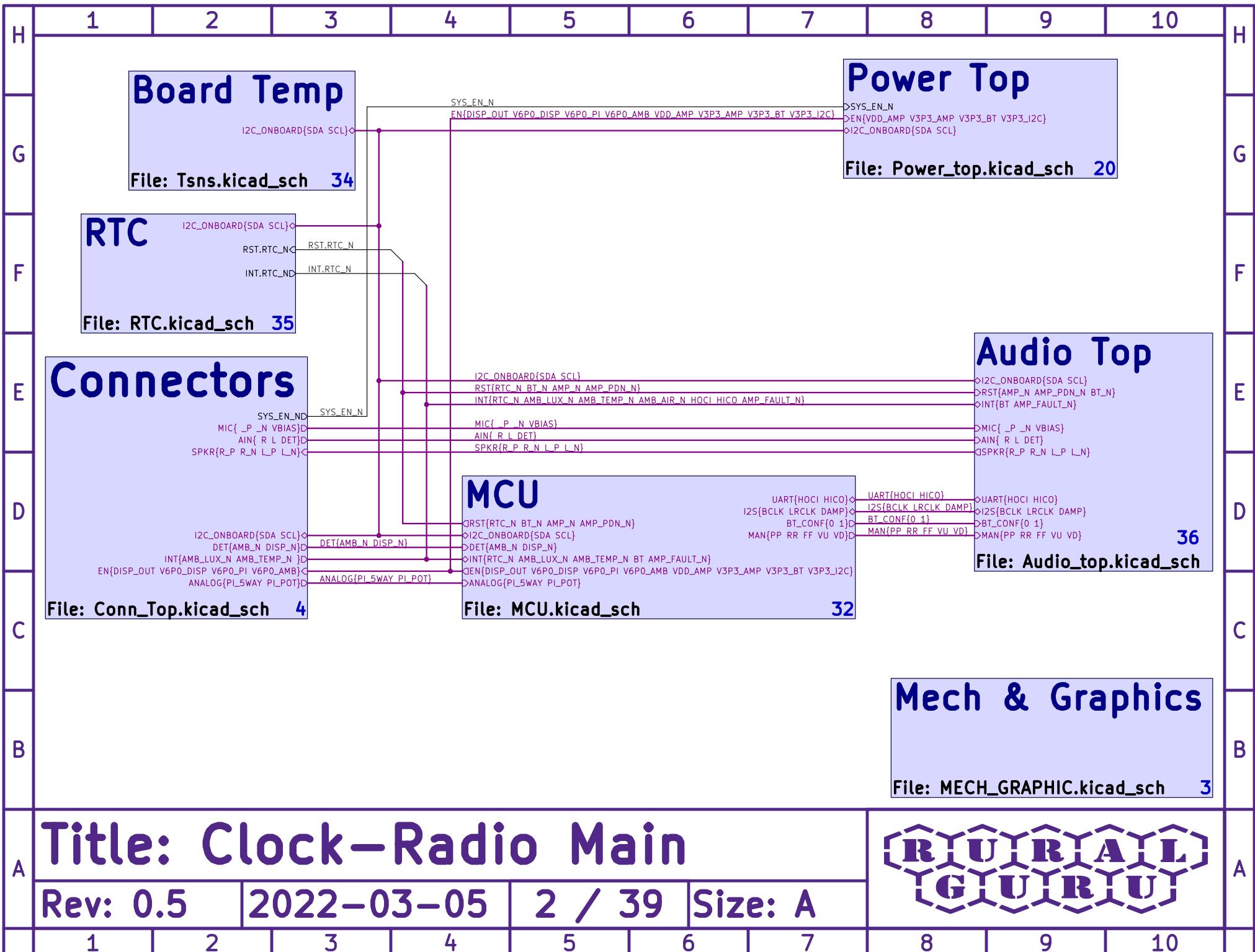
Rev: 0.5

2022-03-05

1 / 39

Size: A





1 2 3 4 5 6 7 8 9 10

H

H

Mech & Graphics

G

G

F

F

Logos



**SYSTEM: CLOCK RADIO
BOARD: MOTHERBOARD**



**SYSTEM: CLOCK RADIO
BOARD: MOTHERBOARD**

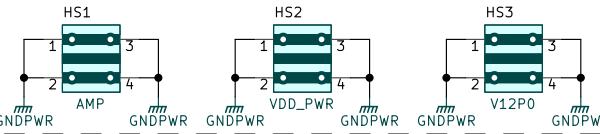
UCCS SP'22



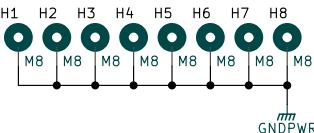
UCCS SP'22



Heatsinks



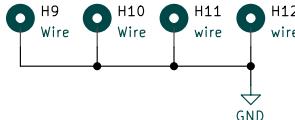
Mounting Holes



Fiducials



Wire Holes



A

A

Title: Clock-Radio Main

Rev: 0.5

2022-03-05

3 / 39

Size: A



1

2

3

4

5

6

7

8

9

10

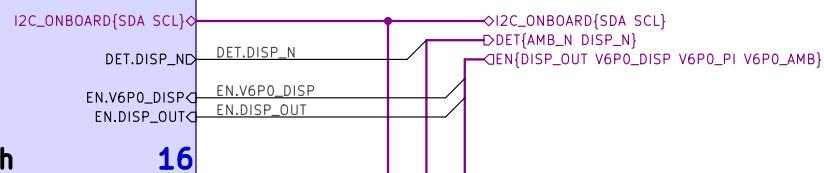
1 2 3 4 5 6 7 8 9 10

Connectors

Display Board

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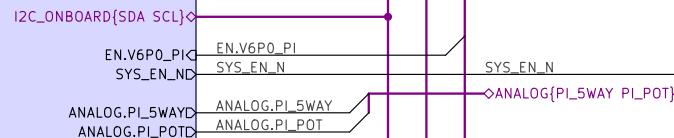
16



Phys Interface Board

File: Conn_phys-int_brd.kicad_sch

8



SYSTEM Power

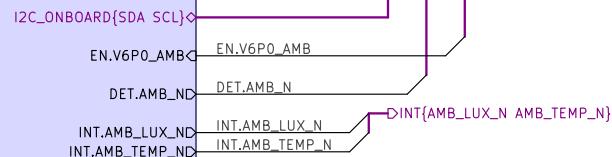
File: PWR_IN.kicad_sch

5

Ambient Board

File: Conn_amb_brd.kicad_sch

12



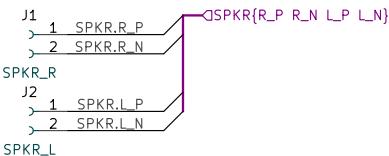
Line Input

AIN{ R L DET}—DAIN{ R L DET}

File: 3p5mm_jack.kicad_sch

6

SPEAKERS



Mic Conn

MIC{ _P _N BIAS}—DMIC{ _P _N VBIAS}

File: Mic_Conn.kicad_sch

7

Title: Clock-Radio Main

Rev: 0.5

2022-03-05

4 / 39 Size: A

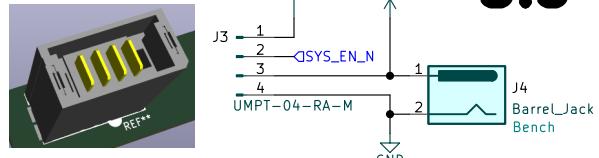


1 2 3 4 5 6 7 8 9 10

SYSTEM Power

Input Power Estimates				
	Min Input Voltage (V)	Input Current (A)	Input Power (W)	Input Resistance (Ω)
Min	30	0.12	3.60	249.82
Est	30	3.23	96.82	9.30
Max	30	7.37	220.99	4.07

30.0 V
3.5 A



Title: Clock-Radio Main

Rev: 0.5 | 2022-03-05 | 5 / 39 | Size: A



1 2 3 4 5 6 7 8 9 10

H

H

Line Input

G

G

F

F

E

E

D

D

C

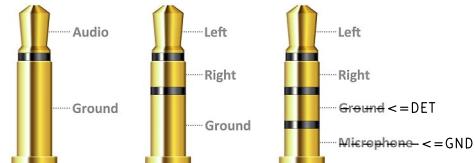
C

B

B

A

A



TS

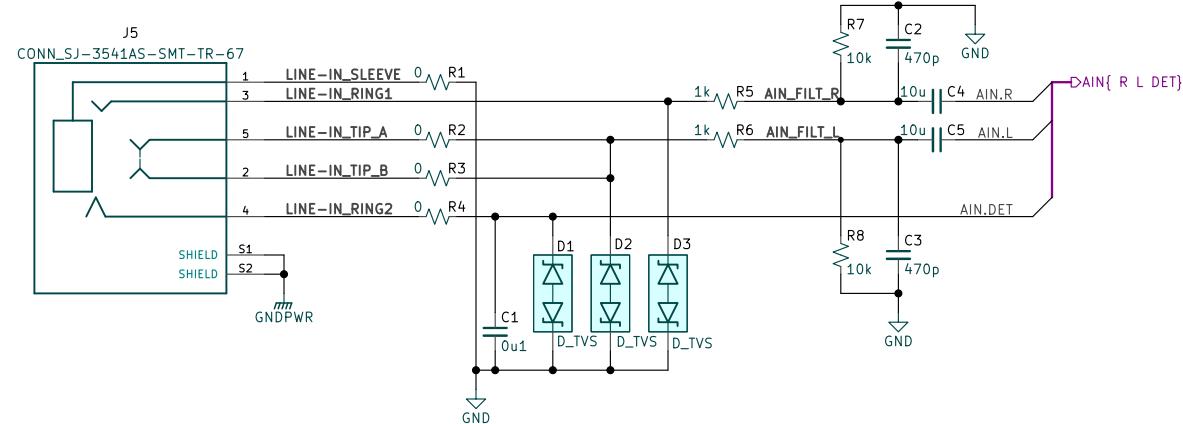
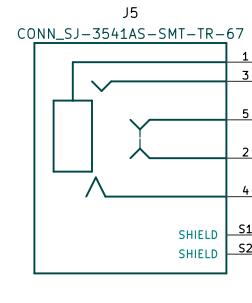
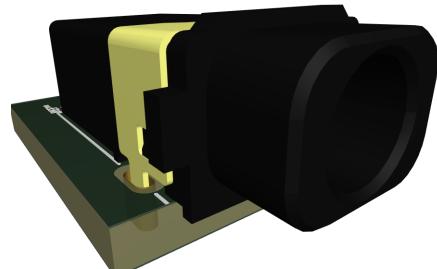
TRS

TRRS

Mono Audio
2 Pole

Stereo Audio
3 Pole

CTIA Standard
4 Pole



Title: Clock-Radio Main

Rev: 0.5

2022-03-05

6 / 39

Size: A



1 2 3 4 5 6 7 8 9 10

1 2 3 4 5 6 7 8 9 10

H

H

Mic Conn

G

G

F

F

E

E

D

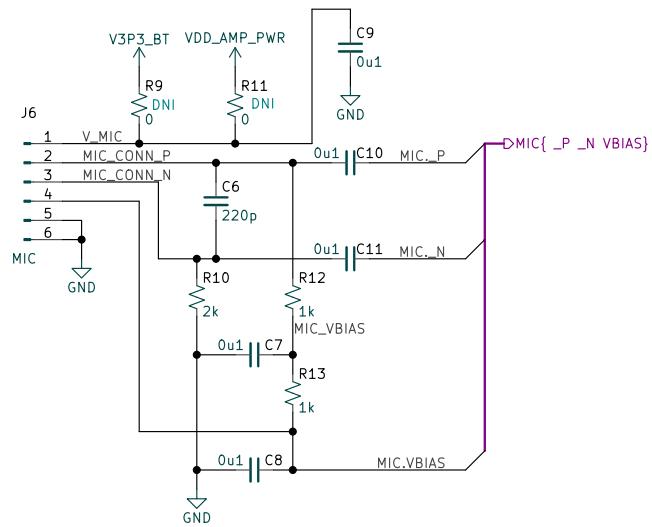
D

C

C

B

B



A

A

Title: Clock-Radio Main

Rev: 0.5

2022-03-05

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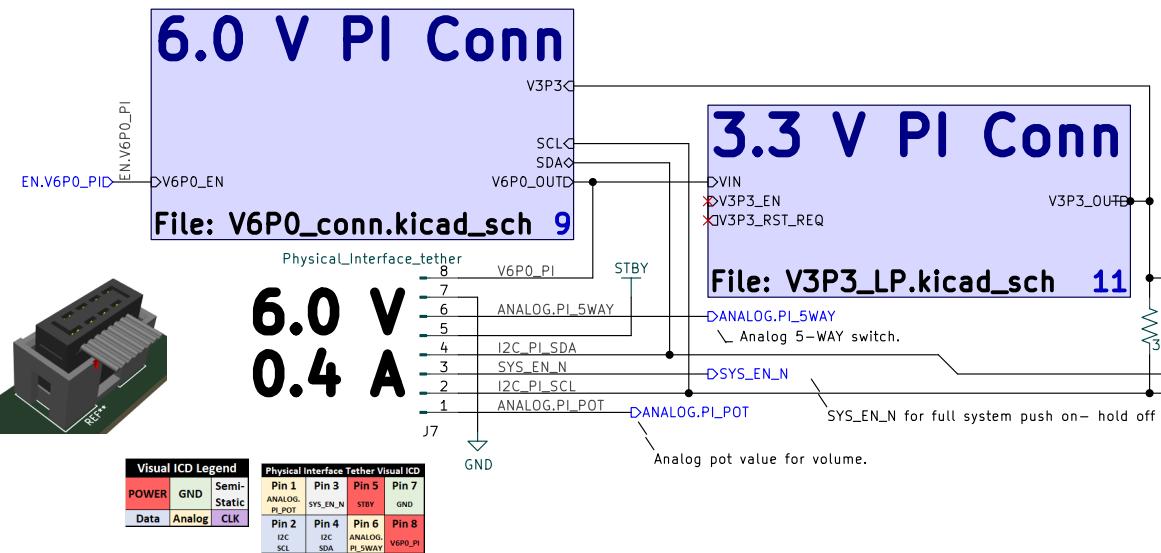
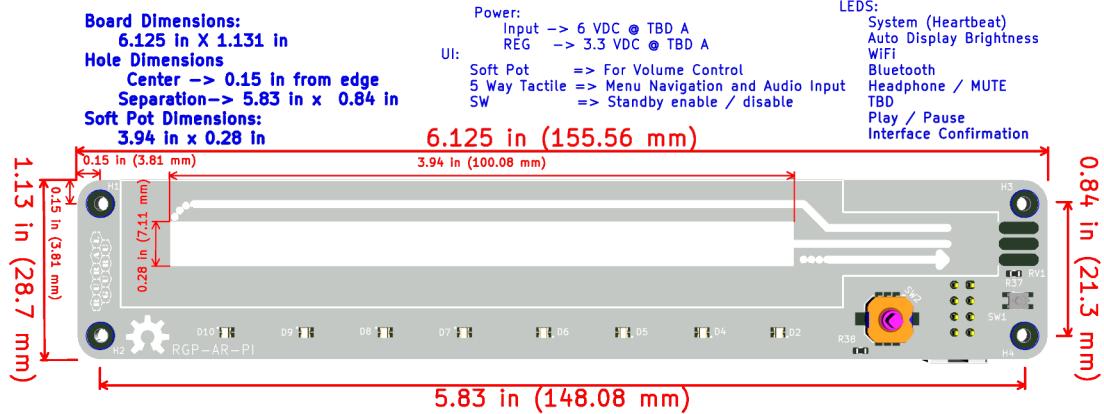
Size: A



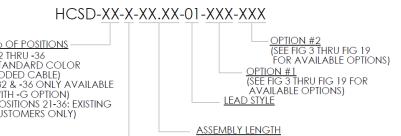
1 2 3 4 5 6 7 8 9 10

1 2 3 4 5 6 7 8 9 10

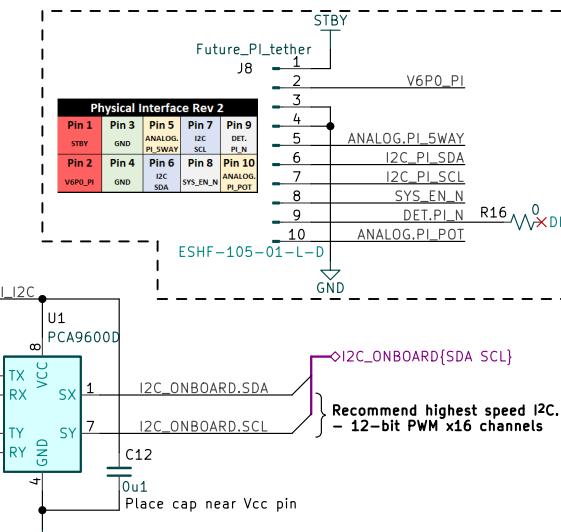
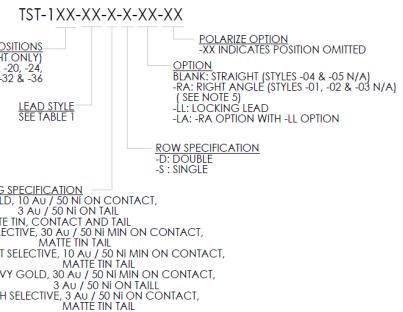
Phys Interface Board



Cable: Ribbon



PCB: Through Hole



A Title: Clock-Radio Main

Rev: 0.5 2022-03-05 8 / 39 Size: A



1 2 3 4 5 6 7 8 9 10

6.0 V PI Conn

TODO:

- Inductor Conf
 - Cin conf
 - Cout Conf
 - Diode Select

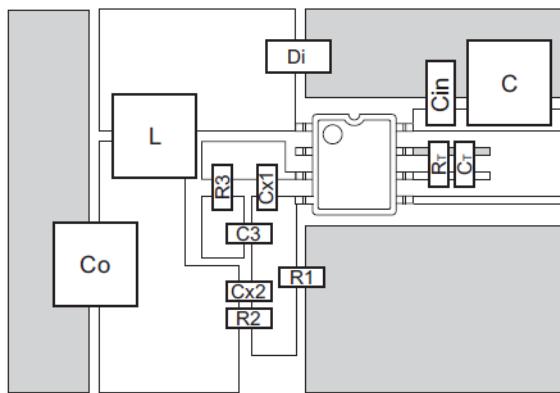


Fig.32 BD9001F reference layout pattern

5. Selection of input capacitor
 Two capacitors, ceramic capacitor C_{IN} and bypass capacitor C , should be inserted between the V_{IN} and GND. Be sure to insert a ceramic capacitor of 1 to $10 \mu F$ for the C . The capacitor C should have a low ESR and a significantly large ripple current. The ripple current I_{RMS} can be obtained by the following formula:

$$I_{RMS} = I_0 \sqrt{V_O \times (V_{in} - V_o) / V_{in}^2}$$

Select capacitors that can accept this ripple current. If the capacitance of CIN and C is not optimum, the IC may malfunction.

6.0 V Conn Sense

File: Vsns.kicad_sch

10

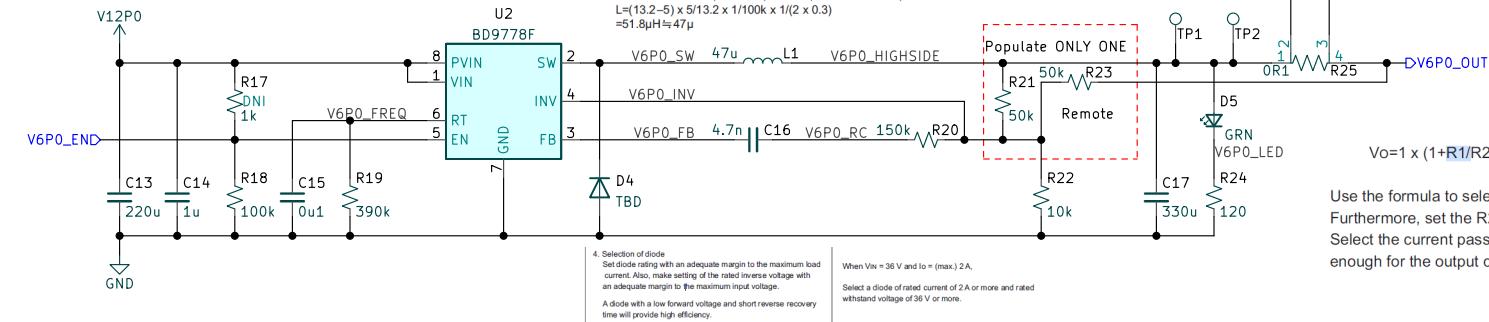
$$\Delta L = (13.2 - 5) \times 5 / (100 \times 10^{-6} \times 100 \times 10^3 \times 13.2) \approx 0.31$$

$$\Delta L = 0.31A$$

When $I_{\text{limit}} = 2 \text{ A}$, $I_0 (\text{Max}) = 1 \text{ A}$, and $V_0 = 5 \text{ V}$,

$$C_{Max} = 3.5m \times (2-1)/5 \\ = 700\mu$$

CMax=700



$$V_0=1 \times (1+B1/B2)$$

Use the formula to select the R₁ and R₂. Furthermore, set the R₂ to 30 kΩ or less. Select the current passing through the R₁ and R₂ to be small enough for the output current.

Title: Clock–Radio Main

Rev: 0.5

2022-03-05

9 / 39 | Size: A



1

10

T

10

6

10

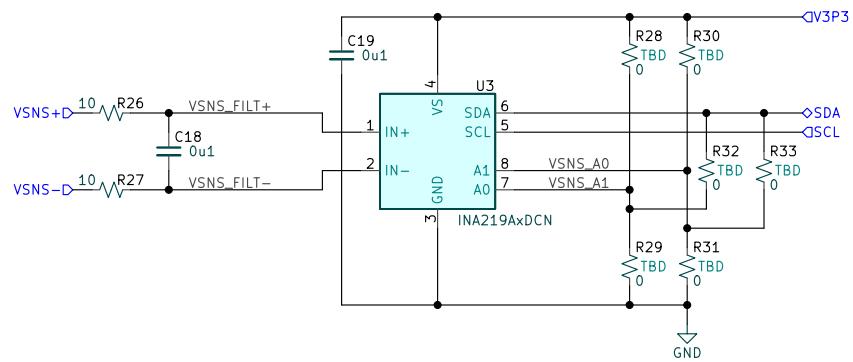
10

1

1

1 2 3 4 5 6 7 8 9 10

6.0 V Conn Sense

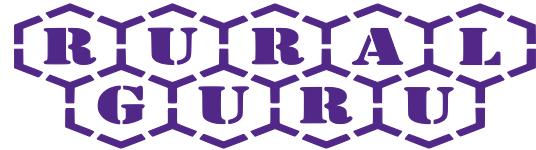


Title: Clock–Radio Main

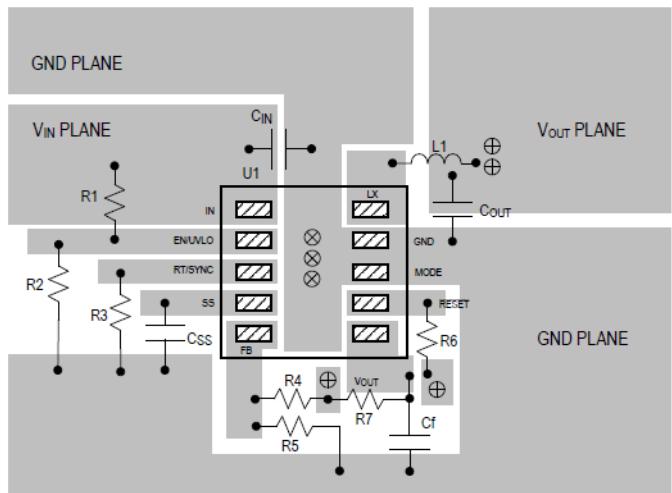
Rev: 0.5

2022-03-05

10 / 39 | Size: A



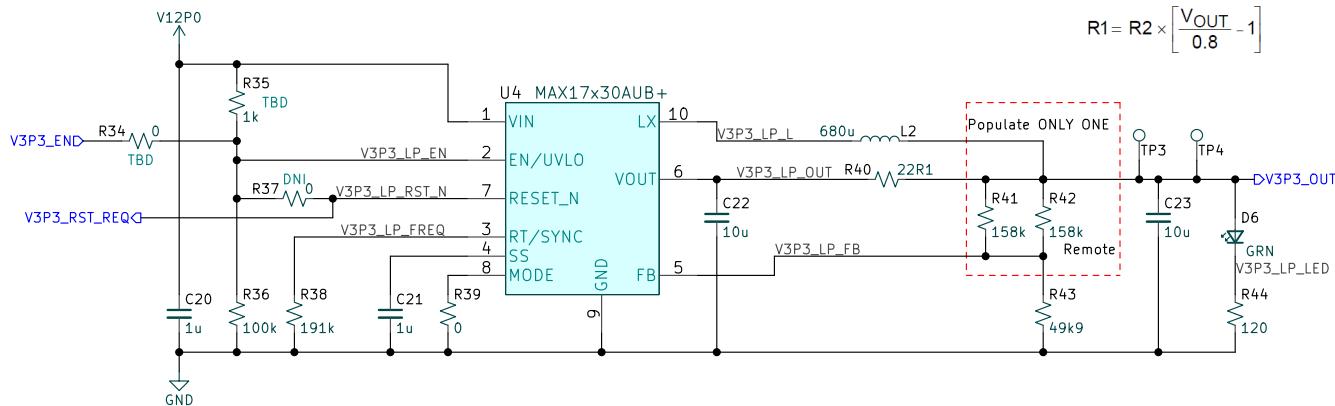
3.3 V PI Conn



- ⊗ Vias to Bottom Side Ground Plane
- ⊕ Vias to VOUT
- ◎ Vias to RESET

The output voltage can be programmed from 0.8V to $0.9 \times V_{IN}$. Set the output voltage by connecting a resistor-divider from output to FB to GND (see [Figure 3](#)). Choose R2 in the range of 25k Ω to 100k Ω and calculate R1 with the following equation:

$$R1 = R2 \times \left[\frac{V_{OUT}}{0.8} - 1 \right]$$



Title: Clock-Radio Main

Rev: 0.5

2022-03-05

11 / 39

Size: A



1 2 3 4 5 6 7 8 9 10

Ambient Board

Cable: Ribbon

FFSD-XX-X-XX.XX-01-X-X-XXX

No. OF POSITIONS
-02 THRU -25
(PER ROW)
END ASSEMBLY
-S: SINGLE END
-D: DOUBLE END

ASSEMBLY LENGTH
(INCLUDES ADDED OPTION LENGTHS)
ALL OPTIONS THAT USE D-02: 4.00 INCHES MINIMUM
ALL OTHER OPTIONS: 1.00 INCHES MINIMUM
LEAD STYLE

PLATING OPTIONS
- LEAVE BLANK FOR STANDARD,
USE C-67-L: 10µ GOLD IN CONTACT AREA
TIN IN IDC AREA
-S: USE C-67-S: 30µ GOLD IN CONTACT AREA
TIN IN IDC AREA
-F: USE C-67-F: 30µ GOLD IN CONTACT AREA
TIN IN IDC AREA

OPTION
-RW: REVERSE WIRING
(NOT AVAILABLE WITH -RN1 OR -RN2)
-D-XX: DATA LENGTH (MINIMUM 2.00[60.8])
1.00[25.4] INCREMENTS
-R: REVERSED (-D-XX) OPTIONAL
(NOT AVAILABLE WITH -M OR -O)
-RN1: REVERSE POLARIZATION NOTCH
(NOT AVAILABLE WITH -RW OR -RN2)
-RN2: REVERSE POLARIZATION NOTCH
(NOT AVAILABLE WITH -RW OR -RN1)
-M: MIDDLE REVERSE (REQUIRES -XX)
(NOT AVAILABLE WITH -R OR -O)
-O: OUTSIDE REVERSE (REQUIRES -D-XX)
(NOT AVAILABLE WITH -R OR -M)
-SR: STRAIN RELIEF
(NOT AVAILABLE WITH -O, -M,
-R, OR -D-XX)
(OLD ASSEMBLIES ONLY)

STANDARD POLARIZATION NOTCH
-N: POLARIZATION NOTCH
(NOT AVAILABLE IN -02 THRU -04)
(LEAVE BLANK FOR -02, -03, -04)

PCB: Through Hole

ESHF-1XX-01-X-D-XX-XX

No. OF POSITIONS
-02 THRU -25
LEAD STYLE
-01

PLATING SPECIFICATION

-L: LIGHT SELECTIVE
(USE T-157-1-XX-L)
-F: FLASH GOLD SELECTIVE
(USE T-157-1-XX-F)
-S: SELECTIVE GOLD
(USE T-157-1-XX-S)

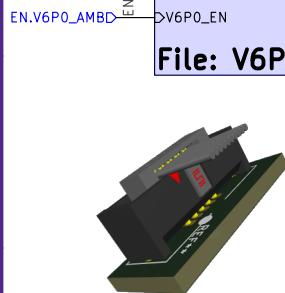
OPTION
-LC: LOCKING CLIP
(NOT AVAILABLE WITH -RA)
-K: POLYIMIDE FILM
(SM ONLY)
-T: THERMOPLASTIC
(SEE FIG. 5, SHT 4) [L]

BODY HEIGHT
-TH: THROUGH HOLE (SEE FIG. 1, SHT 1)
-RA: RIGHT ANGLE (SEE FIG. 2, SHT 2)
-SM: SURFACE MOUNT (SEE FIG. 3, SHT 3)

ROW SPECIFICATION
-D: DOUBLE

TODO:
- Ambient Board Quick Look when designed.

6.0 V Amb Conn



EN.V6P0_AMBD

EN.V6P0_EN

V6P0_AMB

V6P0_OUTD

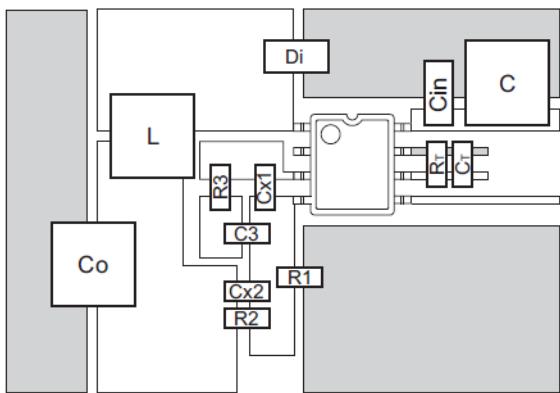
V3P3C

SCL

SDA

V6P0_AMBD

6.0 V Amb Conn TODO:



- Inductor Conf
- Cin conf
- Cout Conf
- Diode Select

Fig.32 BD9001F reference layout pattern

$V_{IN}=13.2V, V_o=5V, L=100\mu H, f=100kHz$
 $\Delta I_L=(13.2-5) \times 5/(100 \times 10^{-6} \times 100 \times 10^3 \times 13.2)$
 ≈ 0.31

$\Delta I_L=0.31A$

5. Selection of input capacitor
 Two capacitors, ceramic capacitor C_{IN} and bypass capacitor C , should be inserted between the V_{IN} and GND . Be sure to insert a ceramic capacitor of 1 to 10 μF for the C . The capacitor C should have a low ESR and a significantly large ripple current. The ripple current I_{rms} can be obtained by the following formula:

$$I_{rms}=I_0 \times \sqrt{V_O(V_{IN}-V_O)/V_{IN}}$$

Select capacitors that can accept this ripple current. If the capacitance of C_{IN} and C is not optimum, the IC may malfunction.

6.0 V Conn Sense

File: Vsns.kicad_sch

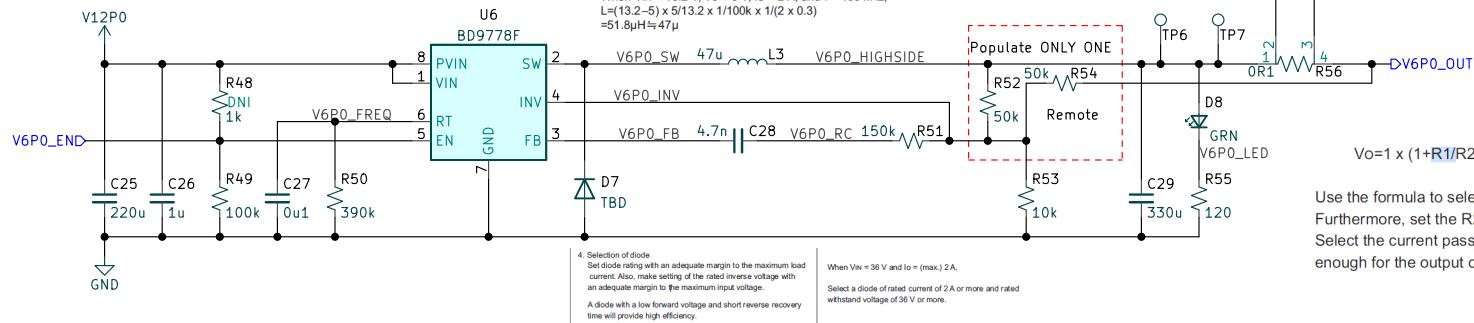
10

When $V_{IN} = 13.2V, V_o = 5V, I_o = 2A$, and $f = 100 kHz$,
 $L = (13.2-5) \times 5/13.2 \times 1/100k \times 1/(2 \times 0.3)$
 $= 51.8\mu H \approx 47\mu$

When $I_{Limit} = 2A$, $I_o (\text{Max}) = 1A$, and $V_o = 5V$,

$C_{Max} = 3.5m \times (2-1)/5$
 $= 700\mu$

$C_{Max}=700\mu F$



4. Selection of diode
 Set diode rating with an adequate margin to the maximum load current. Also, make setting of the rated inverse voltage with an adequate margin to the maximum input voltage.
 A diode with a low forward voltage and short reverse recovery time will provide high efficiency.

When $V_{IN} = 36V$ and $I_o = (\text{max}) 2A$,
 Select a diode of rated current of 2A or more and rated withstand voltage of 36V or more.

$V_o = 1 \times (1 + R_1/R_2)$

Use the formula to select the R_1 and R_2 . Furthermore, set the R_2 to 30 k Ω or less. Select the current passing through the R_1 and R_2 to be small enough for the output current.

Title: Clock-Radio Main

Rev: 0.5

2022-03-05

13 / 39 Size: A



1 2 3 4 5 6 7 8 9 10

6.0 V Conn Sense

G

F

E

D

C

B

A

H

G

F

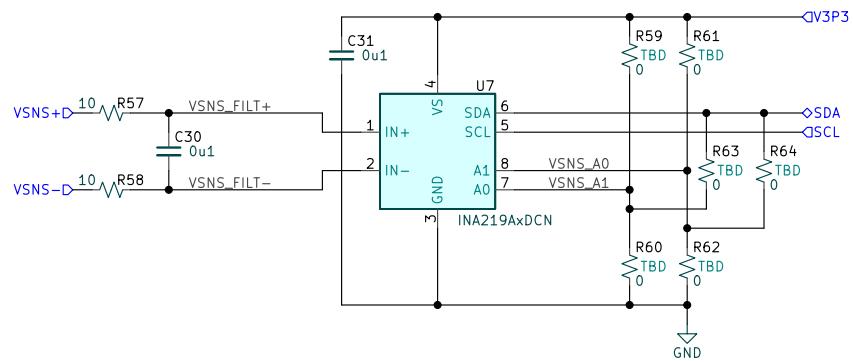
E

D

C

B

A



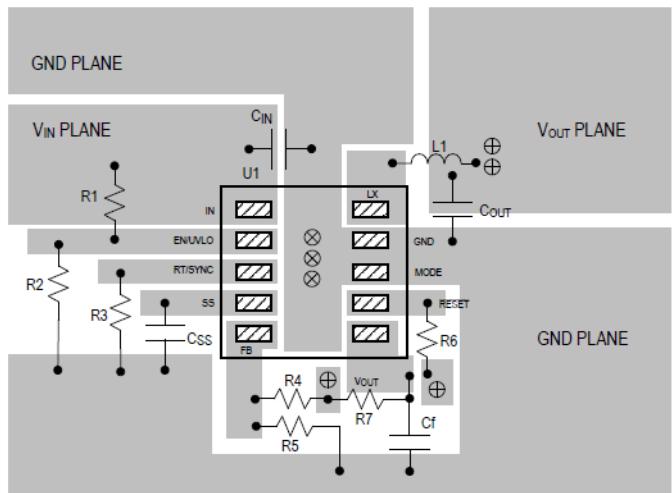
Title: Clock-Radio Main

Rev: 0.5 | 2022-03-05 | 14 / 39 | Size: A



1 2 3 4 5 6 7 8 9 10

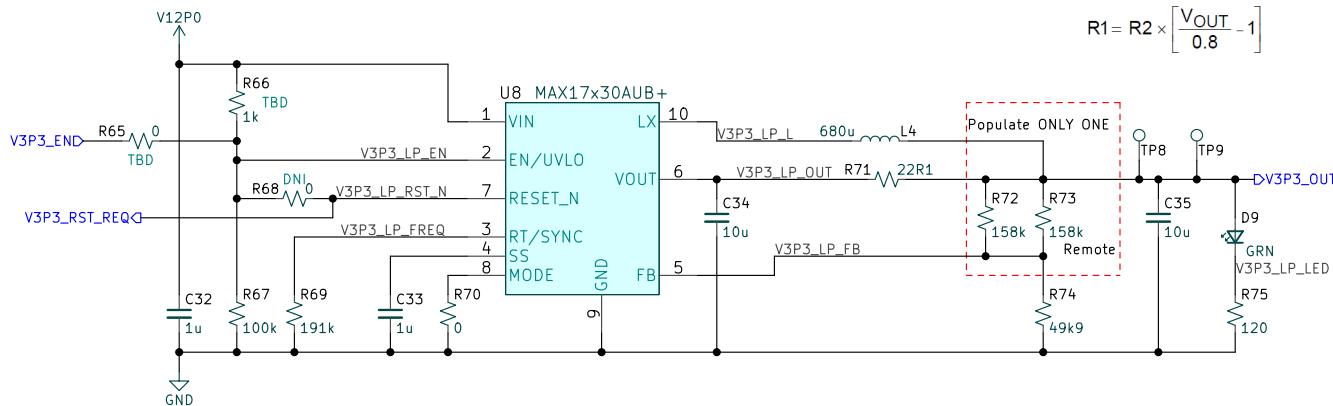
3.3 V Amb Conn



- ⊗ Vias to Bottom Side Ground Plane
- ⊕ Vias to VOUT
- ◎ Vias to RESET

The output voltage can be programmed from 0.8V to $0.9 \times V_{IN}$. Set the output voltage by connecting a resistor-divider from output to FB to GND (see [Figure 3](#)). Choose R2 in the range of 25k Ω to 100k Ω and calculate R1 with the following equation:

$$R1 = R2 \times \left[\frac{V_{OUT}}{0.8} - 1 \right]$$



Title: Clock-Radio Main

Rev: 0.5

2022-03-05

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Size: A



1 2 3 4 5 6 7 8 9 10

Display Board

Cable: Ribbon

FFSD-XX-X-XX,XX-01-X-X-XXX

OPTION
 -RW: REVERSE WIRING
 (NOT AVAILABLE WITH -RN1 OR -RN2)
 -D'XX: DAISY CHAIN (MINIMUM 2.00[50.8].
 1.00[25.4] INCREMENTS)
 -R: REVERSE POLARIZATION NOTCH
 (NOT AVAILABLE WITH -RN1 OR -RN2)
 -RN1: REVERSE POLARIZATION NOTCH
 (NOT AVAILABLE WITH -RW OR -RN2)
 -RN2: REVERSE POLARIZATION NOTCH
 (NOT AVAILABLE WITH -RW OR -RN1)
 -M: MIDDLE REVERSE (REQUIRES -D'XX)
 (NOT AVAILABLE WITH -R OR -RN1)
 -O: OUTSIDE REVERSE (REQUIRES -D'XX)
 (NOT AVAILABLE WITH -R OR -RN1)
 -SR: STRAIN RELIEF
 (NOT AVAILABLE WITH -O, -M,
 -R OR -RN1)
 (SOLD AS ASSEMBLIES ONLY)

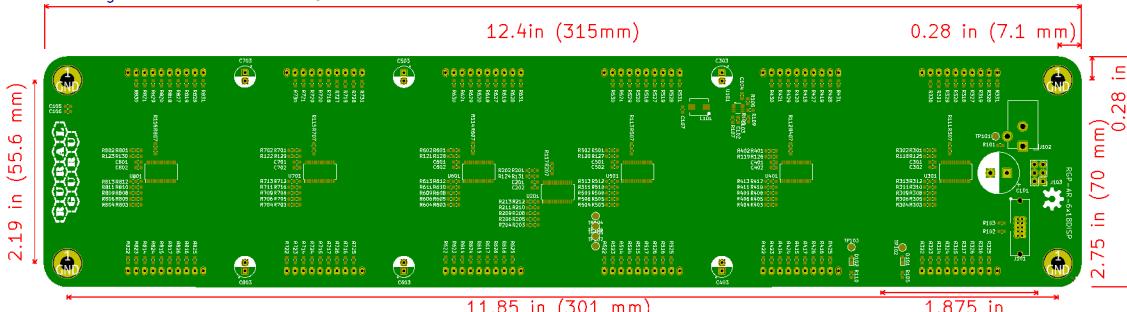
ASSEMBLY LENGTH
 (INCLUDES ADDED OPTION LENGTHS)
 ALL OPTIONS THAT USE -D'XX: 4.00 [101.6] MINIMUM
 ALL OTHER OPTIONS: 1.00 [25.4] MINIMUM
 LEAD STYLE

PLATING OPTIONS
 - LEAVE BLANK FOR STANDARD.
 USE C-67-L: 10µ GOLD IN CONTACT AREA
 TIN IN IDC AREA
 -S: USE C-67-S: 30µ GOLD IN CONTACT AREA
 TIN IN IDC AREA
 -F: USE C-67-F: 3µ GOLD IN CONTACT AREA
 TIN IN IDC AREA

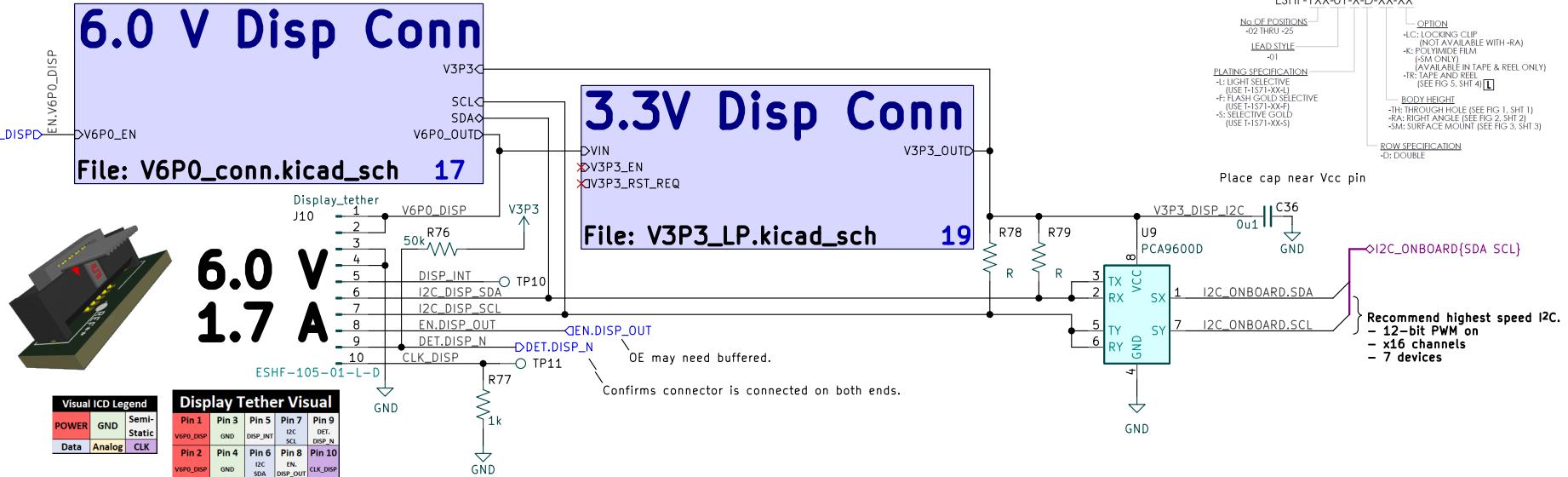
STANDARD POLARIZATION NOTCH
 -N: POLARIZATION NOTCH
 (NOT AVAILABLE IN -O2 THRU -O4)
 (LEAVE BLANK FOR -O2, -O3, -O4)

Board Dimensions:
 12 in x 2.75 in
Hole Dimensions
 Center → 0.28 in from edge. Drivers:
 Separation → 11.85 in x 2.19 (x6, Segments) 16 Drive, 6V tolerant, I2C controlled.
Display Dimensions:
 1.875 in x 2.75 in
Power:
 INPUT → 6 VDC @ TBD A.
 Regulated → 3.3 VDC @ TBD A.

Displays:
 (x6) 16+2DP Segment.
Misc.
 (x1) Lux sensor, I2C controlled
 (x1) Power FET for reverse Voltage Protection



PCB: Through Hole



Title: Clock-Radio Main

Rev: 0.5 2022-03-05 16 / 39 Size: A



1 2 3 4 5 6 7 8 9 10

6.0 V Disp Conn TODO:

- Inductor Conf
- Cin conf
- Cout Conf
- Diode Select

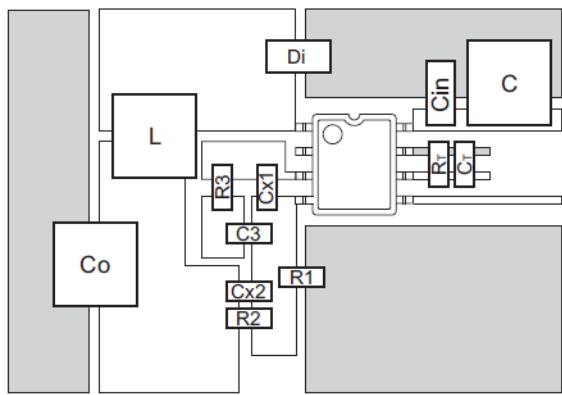


Fig.32 BD9001F reference layout pattern

5. Selection of input capacitor
Two capacitors, ceramic capacitor C_{IN} and bypass capacitor C , should be inserted between the V_{IN} and GND . Be sure to insert a ceramic capacitor of 1 to 10 μF for the C . The capacitor C should have a low ESR and a significantly large ripple current. The ripple current I_{rms} can be obtained by the following formula:

$$I_{rms} = I_o \times \sqrt{V_O(V_{IN}-V_O)/V_{IN}}$$

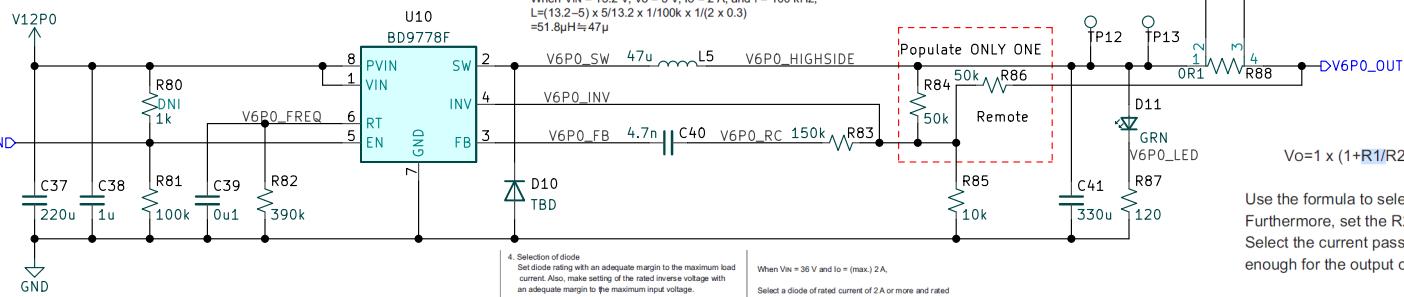
Select capacitors that can accept this ripple current. If the capacitance of C_{IN} and C is not optimum, the IC may malfunction.

6.0 V Conn Sense

File: Vsns.kicad_sch

10

When $V_{IN} = 13.2$ V, $V_O = 5$ V, $I_o = 2$ A, and $f = 100$ kHz,
 $L = (13.2-5) \times 5 / 13.2 \times 1 / 100k \times 1 / (2 \times 0.3)$
 $= 51.8\mu H \approx 47\mu$



$V_{IN}=13.2$ V, $V_O=5$ V, $L=100\mu H$, $f=100kHz$
 $\Delta IL=(13.2-5) \times 5 / (100 \times 10^6 \times 100 \times 10^3 \times 13.2)$
 ≈ 0.31

$\Delta IL=0.31A$

When I_{Limit} : 2 A, I_o (Max) = 1 A, and $V_O = 5$ V,

$C_{Max}=3.5m \times (2-1)/5$
 $=700\mu$

$C_{Max}=700\mu F$

$V_O=1 \times (1+R_1/R_2)$

Use the formula to select the R_1 and R_2 . Furthermore, set the R_2 to 30 k Ω or less. Select the current passing through the R_1 and R_2 to be small enough for the output current.

Title: Clock-Radio Main

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Size: A



1 2 3 4 5 6 7 8 9 10

6.0 V Conn Sense

G

F

E

D

C

B

A

H

G

F

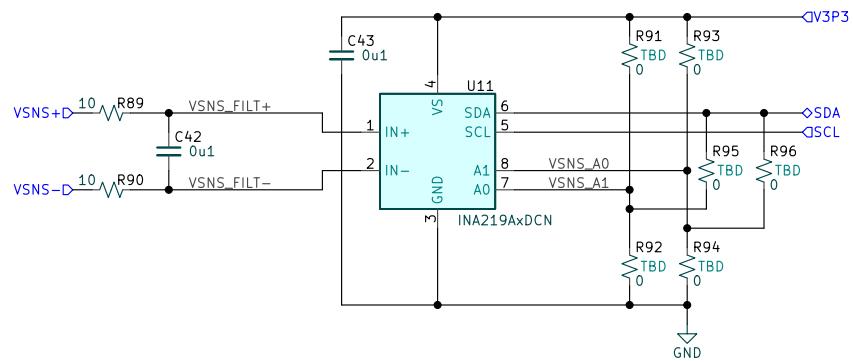
E

D

C

B

A



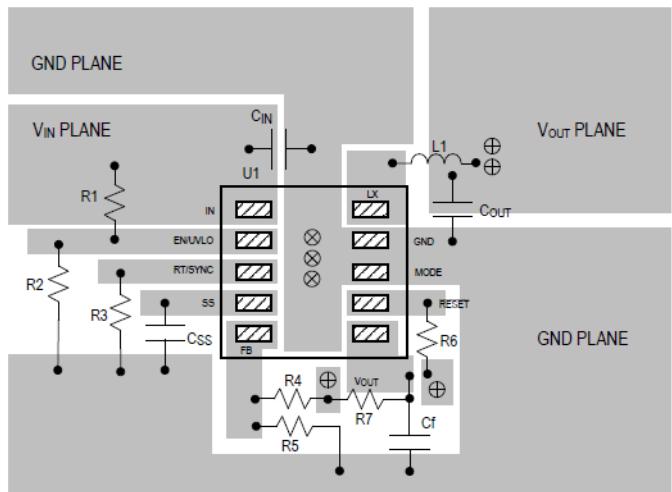
Title: Clock-Radio Main

Rev: 0.5 | 2022-03-05 | 18 / 39 | Size: A



1 2 3 4 5 6 7 8 9 10

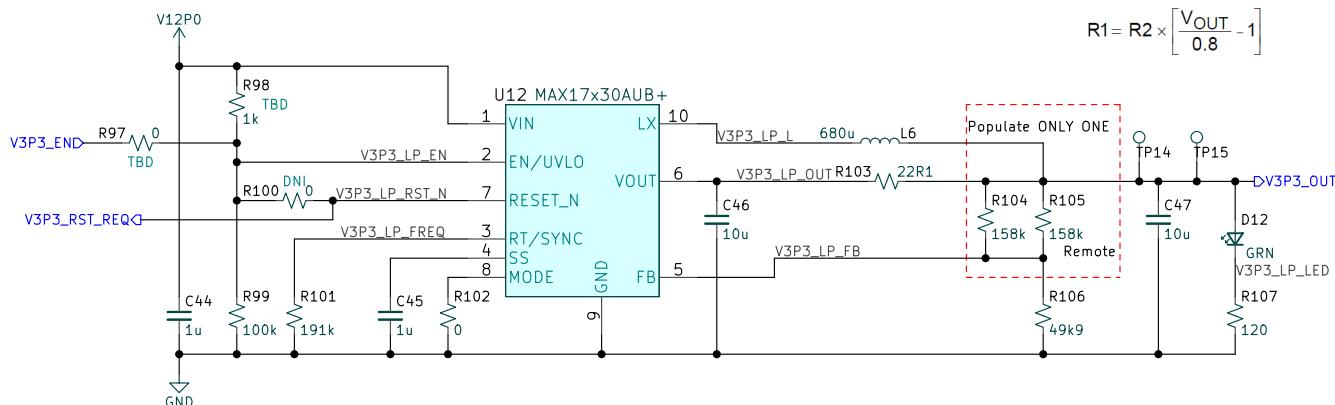
3.3V Disp Conn



- ⊗ Vias to Bottom Side Ground Plane
- ⊕ Vias to VOUT
- ◎ Vias to RESET

The output voltage can be programmed from 0.8V to $0.9 \times V_{IN}$. Set the output voltage by connecting a resistor-divider from output to FB to GND (see Figure 3). Choose R2 in the range of 25k Ω to 100k Ω and calculate R1 with the following equation:

$$R1 = R2 \times \left[\frac{V_{OUT}}{0.8} - 1 \right]$$



Title: Clock-Radio Main

Rev: 0.5

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Size: A



1 2 3 4 5 6 7 8 9 10

Power Top

V24PO AMP Power Sense Estimates									
Min	Input OR Voltage	Output Resistor	Input Current	Load	Supply	Sense Resistance	Input Power	Load Power	Power
Max	(V)	(V)	(A)	(A)	(V)	(Ω)	(W)	(W)	(W)
Min	24	0.00	0.020	0.01	40%	0.10	0.10	0.24	0.0000
Ext	30	24	0.25	2.173	2.50	93%	0.10	65.19	60.00
Max	30	24	0.54	4.80	5.40	92%	0.10	144.04	129.60
									2.92

V5P0 MCU Power Sense Estimates										
Min	Input OR Voltage	Output Resistor	Input Current	Load	Supply	Sense Resistance	Input Power	Load Power	Power	
Max	(V)	(V)	(A)	(A)	(V)	(Ω)	(W)	(W)	(W)	
Min	12	5	0.00	0.104	0.10	40%	0.00	1.25	0.50	0.000
Ext	12	5	0.00	0.231	0.50	90%	0.00	2.78	2.50	0.000
Max	12	5	0.00	0.49	1.00	85%	0.00	5.88	5.00	0.000

V12P0 SYS Power Sense Estimates									
Min	Input OR Voltage	Output Resistor	Input Current	Load	Supply	Sense Resistance	Input Power	Load Power	Power
Max	(V)	(V)	(A)	(A)	(V)	(Ω)	(W)	(W)	(W)
Min	30	24	0.01	0.300	0.01	40%	0.00	1.20	0.000
Ext	30	12	0.15	0.688	1.53	80%	0.10	20.63	18.34
Max	30	12	0.54	2.57	5.40	88%	0.10	76.95	65.80
									2.92

V6P0 SYS Power Sense Estimates									
Min	Input OR Voltage	Output Resistor	Input Current	Load	Supply	Sense Resistance	Input Power	Load Power	Power
Max	(V)	(V)	(A)	(A)	(V)	(Ω)	(W)	(W)	(W)
Min	30	24	0.01	0.300	0.01	40%	0.00	1.20	0.000
Ext	12	6	0.12	0.703	1.20	87%	0.10	8.44	7.20
Max	12	6	0.20	1.38	2.00	75%	0.10	16.53	12.00
									0.40

V6P0 Disp Tether Power Sense Estimates									
Min	Input OR Voltage	Output Resistor	Input Current	Load	Supply	Sense Resistance	Input Power	Load Power	Power
Max	(V)	(V)	(A)	(A)	(V)	(Ω)	(W)	(W)	(W)
Min	32	32	0.01	0.325	0.01	40%	0.00	1.50	0.000
Ext	12	6	0.04	0.229	0.40	88%	0.10	2.75	2.40
Max	32	6	0.08	0.47	0.75	80%	0.10	5.70	4.50
									0.09

V6P0 Ambient Tether Power Sense Estimates									
Min	Input OR Voltage	Output Resistor	Input Current	Load	Supply	Sense Resistance	Input Power	Load Power	Power
Max	(V)	(V)	(A)	(A)	(V)	(Ω)	(W)	(W)	(W)
Min	32	32	0.01	0.325	0.01	40%	0.00	1.50	0.000
Ext	12	6	0.05	0.286	0.50	88%	0.10	3.44	3.00
Max	12	6	0.08	0.47	0.75	80%	0.10	5.70	4.50
									0.09

V3P3 I2C Power Sense Estimates									
Min	Input OR Voltage	Output Resistor	Input Current	Load	Supply	Sense Resistance	Input Power	Load Power	Power
Max	(V)	(V)	(A)	(A)	(V)	(Ω)	(W)	(W)	(W)
Min	12	3.3	0.000	0.000	0.001	60%	0.10	0.31	0.000
Ext	12	3.3	0.008	0.026	0.08	85%	0.10	0.31	0.001
Max	12	3.3	0.010	0.03	0.10	90%	0.10	0.37	0.33
									0.00

V3P3 Bluetooth Power Sense Estimates									
Min	Input OR Voltage	Output Resistor	Input Current	Load	Supply	Sense Resistance	Input Power	Load Power	Power
Max	(V)	(V)	(A)	(A)	(V)	(Ω)	(W)	(W)	(W)
Min	12	3.3	0.008	0.026	0.08	85%	0.10	0.31	0.001
Ext	12	3.3	0.010	0.03	0.10	90%	0.10	0.37	0.33
Max	12	3.3	0.010	0.03	0.10	90%	0.10	0.37	0.33
									0.00

12.0 V System

I2C_ONBOARD{SDA SCL} ◊

File: V12P0_SYS.kicad_sch 21

VDD Amplifier

I2C_ONBOARD{SDA SCL} ◊

EN.VDD_AMP ◊

5.0 V MCU

EN{VDD_AMP V3P3_AMP V3P3_BT V3P3_I2C} ◊

EN.V3P3_I2C ◊

Title: Clock-Radio Main

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3.3 V Amplifier

V3P3_OUTD

I2C_ONBOARD{SDA SCL} ◊

EN.V3P3_AMP ◊

3.3 V Bluetooth

V3P3_OUTD

I2C_ONBOARD{SDA SCL} ◊

EN.V3P3_BT ◊

3.3 V I2C

V3P3_OUTD

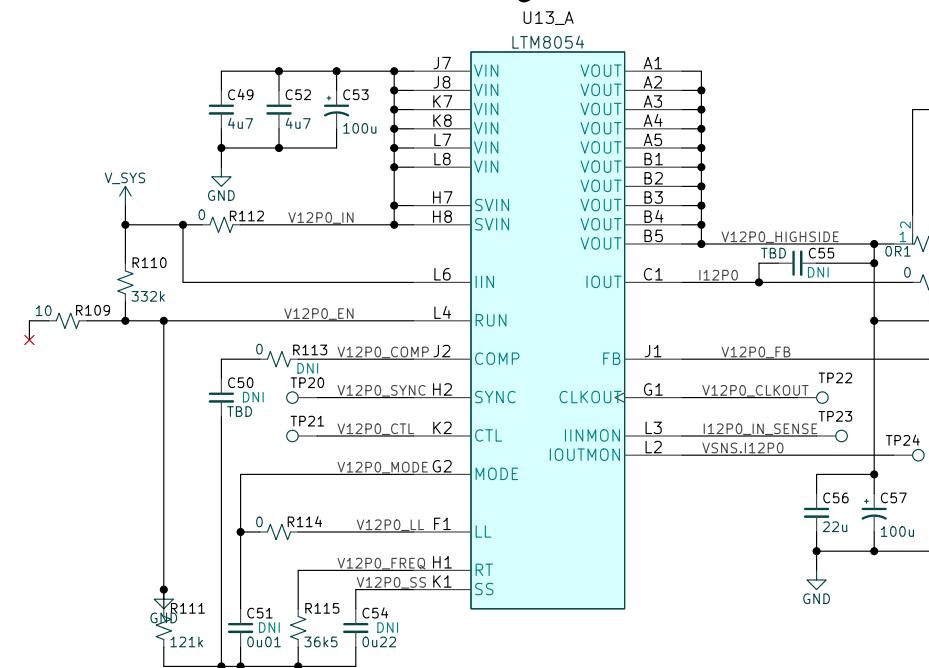
I2C_ONBOARD{SDA SCL} ◊

EN.V3P3_I2C ◊

GND TIE



12.0 V System



File: Vsns.kicad_sch

22

FB (Pin J1): Output Voltage Feedback. The LTM8054 regulates the FB pin to 1.2V. Connect the FB pin to a resistive divider between the output and GND to set the output voltage. The output voltage is determined by the equation

$$V_{\text{OUT}} = 1.2 \cdot \left(\frac{R_{\text{TOP}}}{R_{\text{BOT}}} \right)$$

Table 2. Electrolytic Caps Used in LTM8054 Testing

DESCRIPTION	MANUFACTURER	PART NUMBER
100µF, 6V, 75mΩ, Tantalum C Case	AVX	TPSC107M006R0075
100µF, 16V, 100mΩ, Tantalum Y Case	AVX	TPSY107M016R0100
68µF, 16V, 200mΩ, Tantalum C Case	AVX	TPSC686M016R0200
47µF, 25V, 900mΩ, Tantalum D Case	AVX	TADJ476M025R
33µF, 35V, 300mΩ, Tantalum D Case	AVX	TPSD336M035R0300
10µF, 50V, 120mΩ, Aluminum 6.3mm x 6mm case	SunCon	50HVP10M

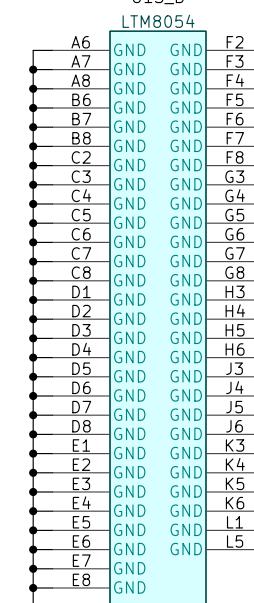
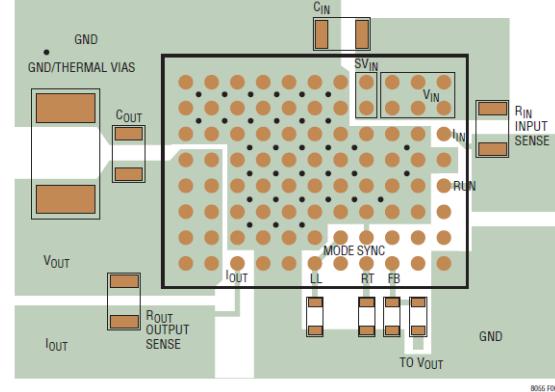


Table 1. Recommended Component Values and Configuration ($T_A = 25^\circ\text{C}$)

VIN Range	VOUT	CIN	COUT	R _{ADJ}	f _{OPTIMAL (kHz)}	R _{T (OPTIMAL)}	f _{m (kHz)}	f _{T (MIN)}
5V to 19V	3.3V	2 x 4.7μF, 50V, X5R, 0805	47μF, 4V, X5R, 1206 100μF, 6V, 75mΩ, Electrolytic C Case	100k/56.2k	600	36.5k	800	24.9k
5V to 25V	5V	2 x 4.7μF, 50V, X5R, 0805	22μF, 6.3V, X5R, 0805 100μF, 6V, 75mΩ, Electrolytic C Case	100k/31.6k	550	39.2k	800	24.9k
5V to 27V	8V	2 x 4.7μF, 50V, X5R, 0805	22μF, 10V, XTR, 1206 100μF, 16V, 100mΩ, Electrolytic D Case	100k/17.4k	500	45.3k	800	24.9k
5V to 35V	12V	2 x 4.7μF, 50V, X5R, 0805	22μF, 25V, X5R, 0805 68μF, 16V, 200mΩ, Electrolytic C Case	100k/11k	600	36.5k	800	24.9k
5.9V to 36V	18V	2 x 4.7μF, 50V, X5R, 0805	22μF, 25V, X5R, 0805 47μF, 25V, 900mΩ, Electrolytic D Case	100k/6.98k	500	45.3k	800	24.9k
7.5V to 36V	24V	2 x 4.7μF, 50V, X5R, 0805	22μF, 25V, X5R, 0805 33μF, 35V, 300mΩ, Electrolytic D Case	100k/5.23k	650	31.6k	800	24.9k
7.5V to 36V	36V	2 x 4.7μF, 50V, X5R, 0805	10μF, 50V, X5R, 1206 10μF, 50V, 120mΩ, Electrolytic 6.3mm × 6mm Case	100k/3.40k	650	31.6k	800	24.9k

Title: Clock–Radio Main

Rev: 0.5

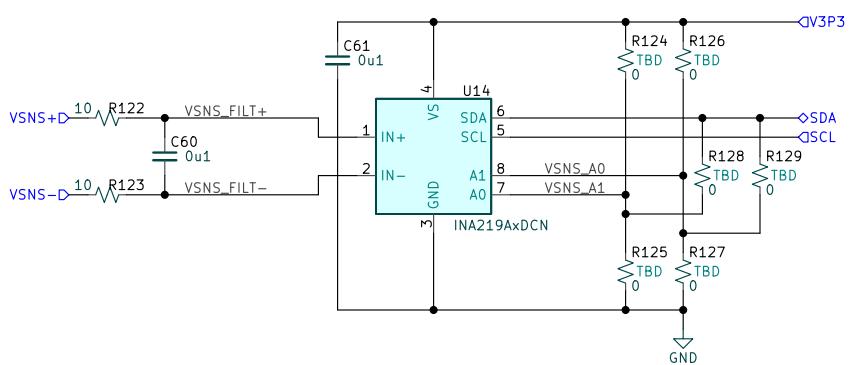
2022-03-05

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1 2 3 4 5 6 7 8 9 10

12.0V VSense



H 1 2 3 4 5 6 7 8 9 10 H

1 2 3 4 5 6 7 8 9 10

Title: Clock-Radio Main

Rev: 0.5 | 2022-03-05 | 22 / 39 | Size: A



1 2 3 4 5 6 7 8 9 10

5.0 V MCU

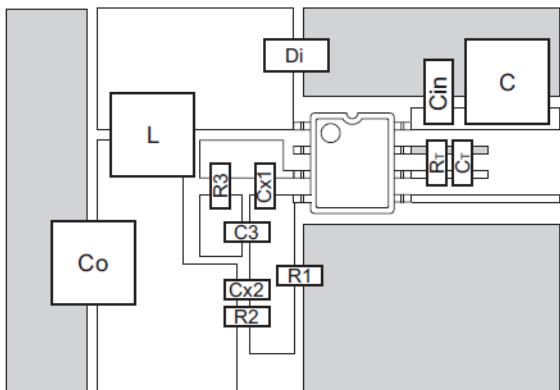
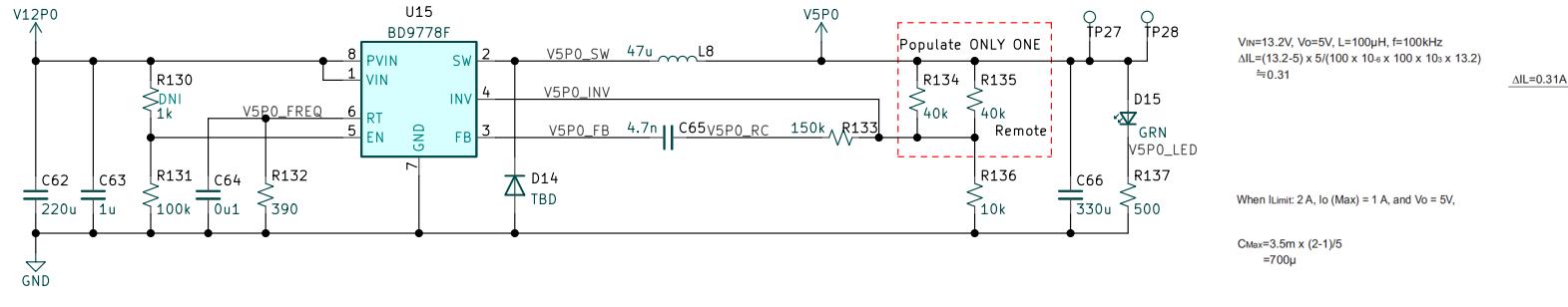


Fig.32 BD9001F reference layout pattern

- TODO:**

 - Inductor Conf
 - Cin conf
 - Cout Conf
 - Diode Select



5. Selection of input capacitor
 Two capacitors, ceramic capacitor C_{IN} and bypass capacitor C , should be inserted between the VIN and GND. Be sure to insert a ceramic capacitor of 1 to 10 μF for the C . The capacitor C should have a low ESR and a significantly large ripple current. The ripple current I_{RMS} can be obtained by the following formula:

$$I_{RMS} = I_0 \times \sqrt{V_O \times (V_{in} - V_o) / V_{in}}$$

Select capacitors that can accept this ripple current. If the capacitance of CIN and C is not optimum, the IC may malfunction.

4. Selection of diode
Set diode rating with an adequate margin to the maximum load current. Also, make setting of the rated inverse voltage with an adequate margin to the maximum input voltage.

A diode with a low forward voltage and short reverse recovery time is required.

When $V_{IN} = 36\text{ V}$ and $I_o = (\text{max.}) 2\text{ A}$,

Select a diode of rated current of 2A or more and rated withstand voltage of 20V or more.

$$V_o = 1 \times (1 + R_1/R_2)$$

Use the formula to select the R1 and R2. Furthermore, set the R2 to 30 k Ω or less.

Select the current passing through the R₁ and R₂ to be small enough for the output current.

Title: Clock–Radio Main

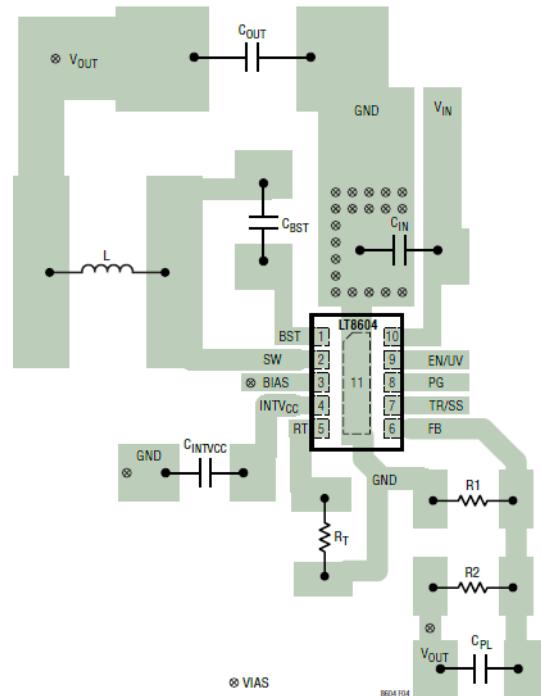
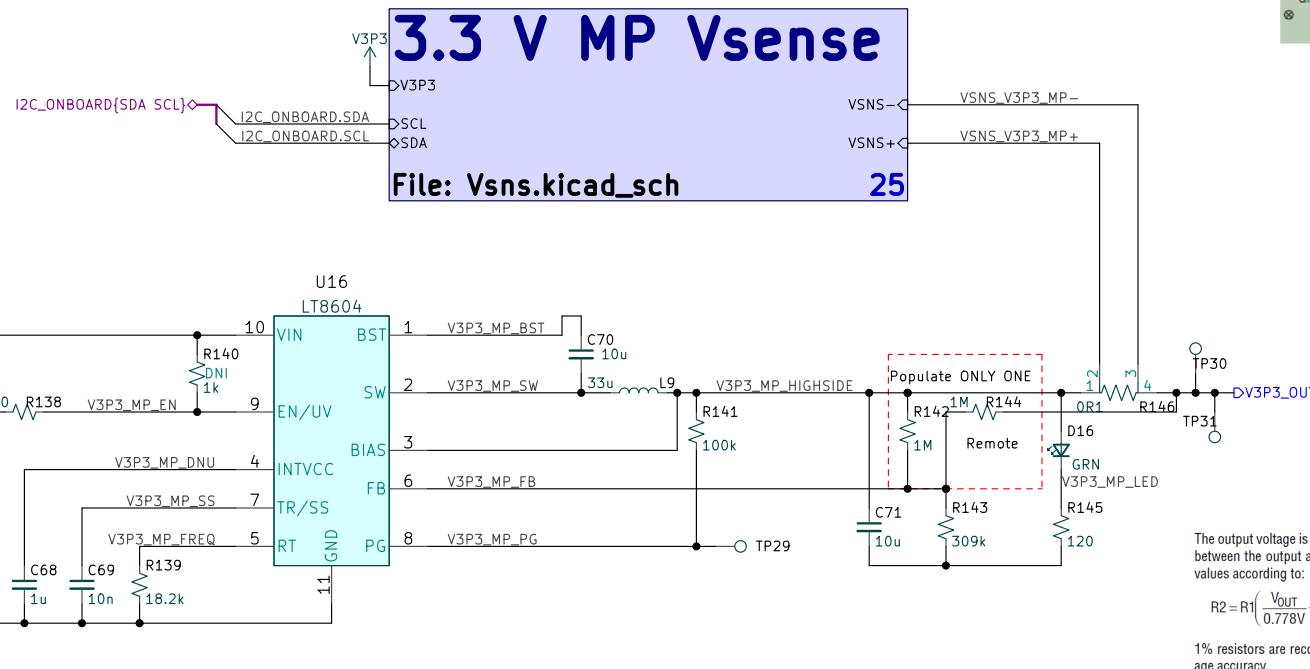
Rev: 0.5

2022-03-05

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3.3 V I2C



The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R_2 = R_1 \left(\frac{V_{OUT}}{0.778V} - 1 \right)$$

1% resistors are recommended to maintain output voltage accuracy.

Title: Clock–Radio Main

Rev: 0.5

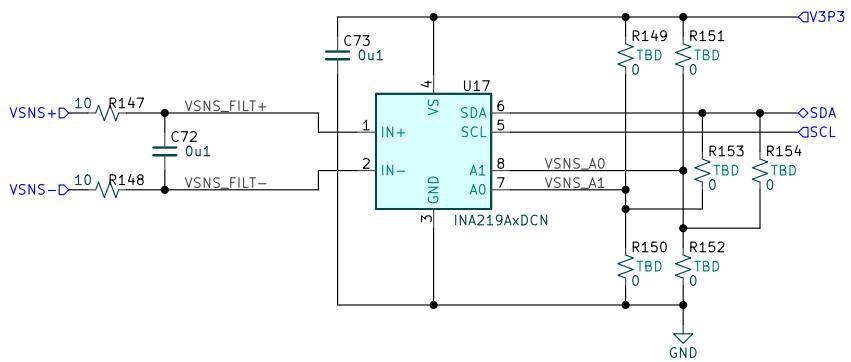
2022-03-05

24 / 39 | Size: A



1 2 3 4 5 6 7 8 9 10

3.3 V MP Vsense



A Title: Clock-Radio Main

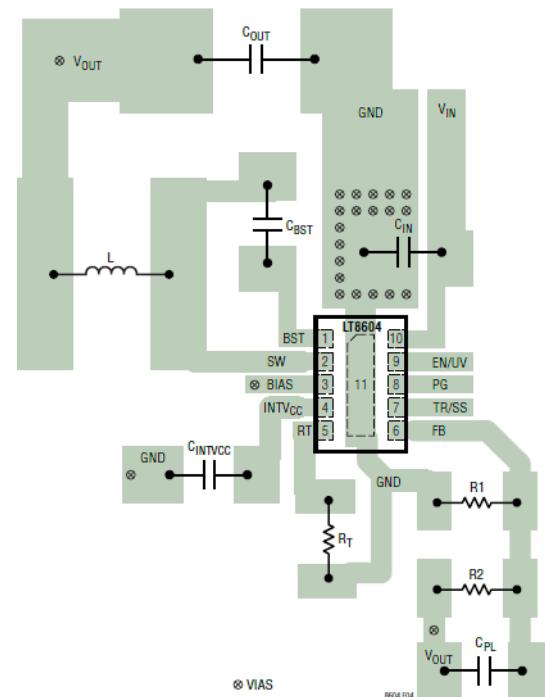
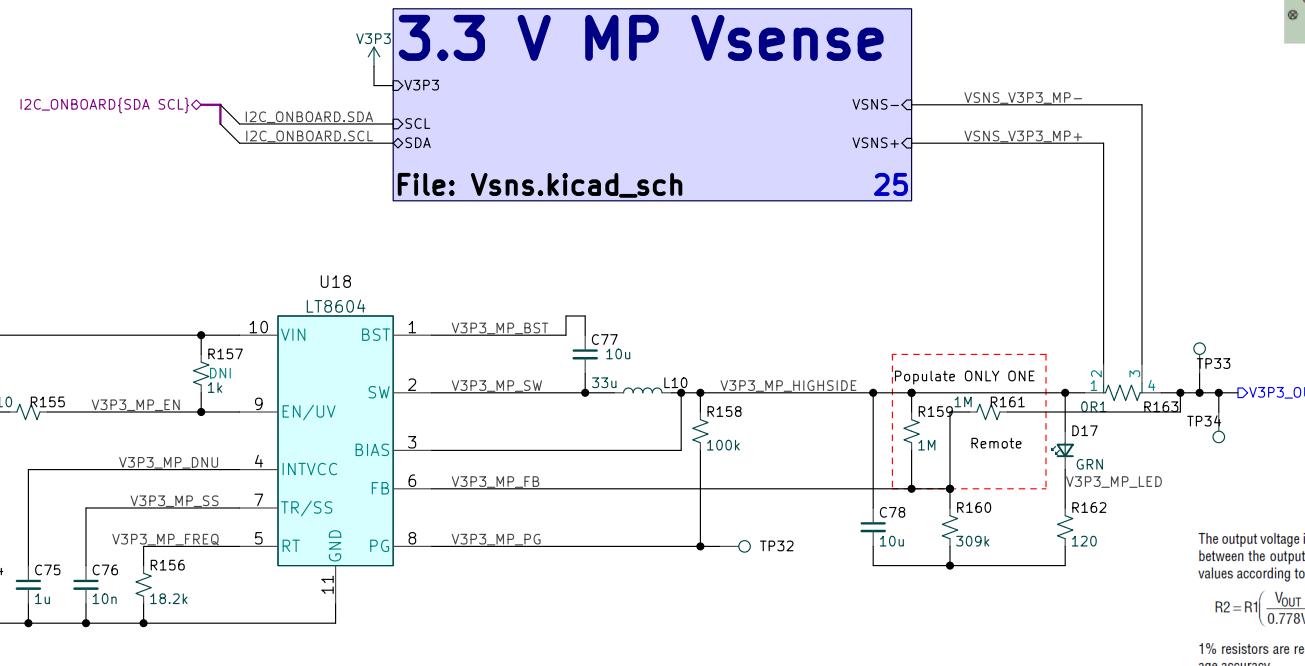
Rev: 0.5 | 2022-03-05 | 25 / 39 | Size: A



1 2 3 4 5 6 7 8 9 10

1 2 3 4 5 6 7 8 9 10

3.3 V Amplifier



The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R2 = R1 \left(\frac{V_{out}}{0.778V} - 1 \right)$$

1% resistors are recommended to maintain output voltage accuracy.

Title: Clock-Radio Main

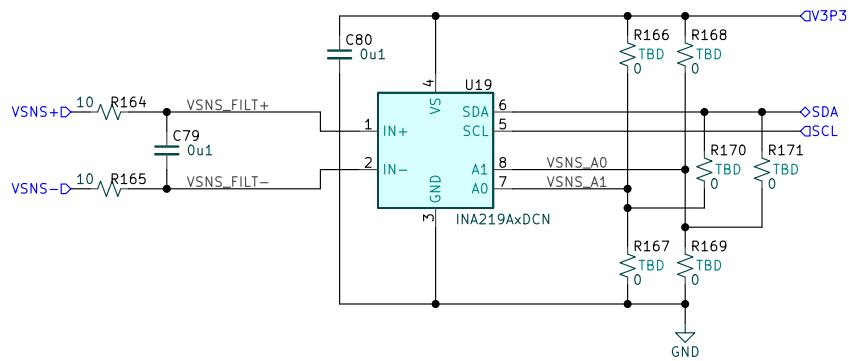
Rev: 0.5 | 2022-03-05 | 26 / 39 | Size: A



1 2 3 4 5 6 7 8 9 10

1 2 3 4 5 6 7 8 9 10

3.3 V MP Vsense

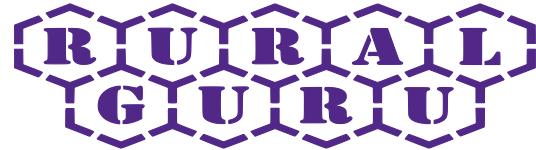


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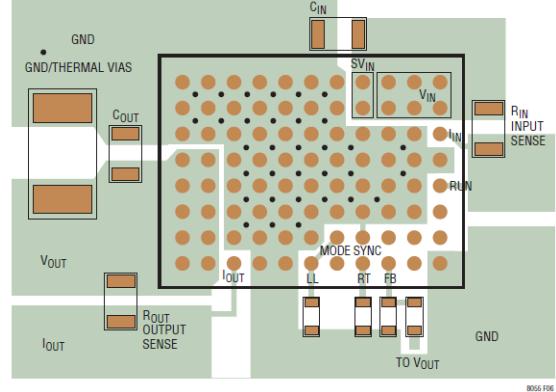
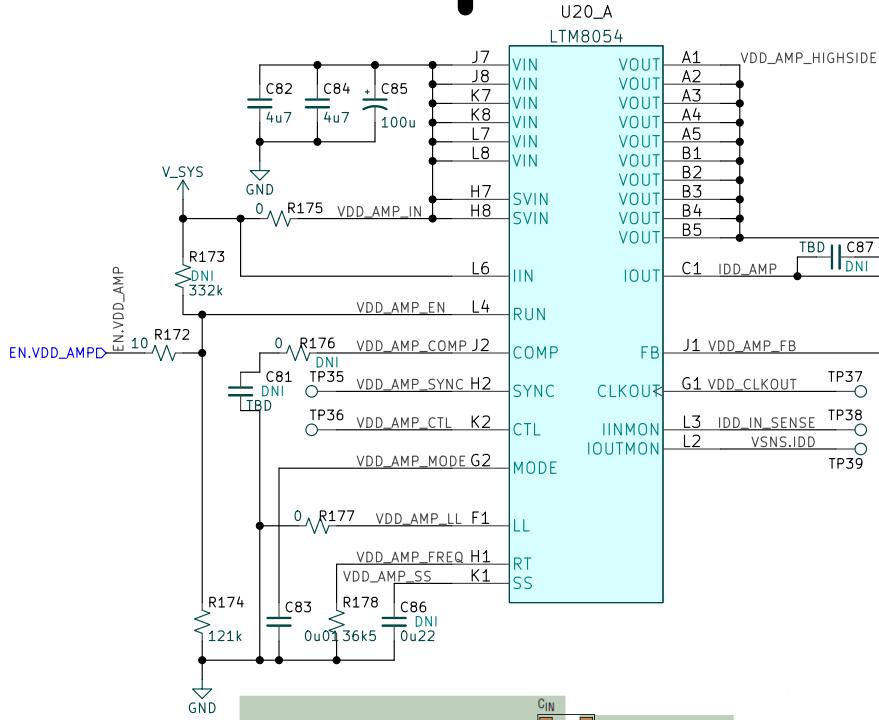
Rev: 0.5

2022-03-05

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VDD Amplifier



VDD AMP Vsense

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29

FB (Pin J1): Output Voltage Feedback. The LTM8054 regulates the FB pin to 1.2V. Connect the FB pin to a resistive divider between the output and GND to set the output voltage. The output voltage is determined by the equation

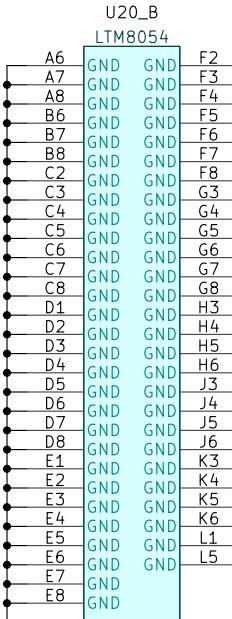
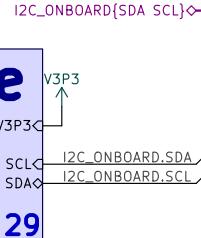
$$V_{\text{OUT}} = 1.2 \cdot \left(\frac{R_{\text{TOP}}}{R_{\text{BOT}}} + 1 \right)$$

Table 2. Electrolytic Caps Used in LTM8054 Testing

DESCRIPTION	MANUFACTURER	PART NUMBER
100µF, 6V, 75mΩ, Tantalum C Case	AVX	TPSC107M006R0075
100µF, 16V, 100mΩ, Tantalum Y Case	AVX	TPSY107M016R0100
68µF, 16V, 200mΩ, Tantalum C Case	AVX	TPSC686M016R0200
47µF, 25V, 900mΩ, Tantalum D Case	AVX	TJAD476M025R
33µF, 35V, 300mΩ, Tantalum D Case	AVX	TPSD336M035M0300
10µF, 50V, 120mΩ, Aluminum 6.3mm x 6mm case	SunCon	50HVP10M

Table 1. Recommended Component Values and Configuration ($T_A = 25^\circ C$)

V _{IN} Range	V _{OUT}	C _{IN}	C _{OUT}	R _{ADJ}	f _{OPTIMAL} (kHz)	R _{T(OPTIMAL)}	f _M (kHz)	I _Q (mA)
5V to 19V	3.3V	2 x 4.7μF, 50V, X5R, 0805	47μF, 4V, X5R, 1206 100μF, 6V, 75mΩ, Electrolytic C Case	100k/56.2k	600	36.5k	800	1.5
5V to 25V	5V	2 x 4.7μF, 50V, X5R, 0805	22μF, 6.3V, X5R, 0805 100μF, 6V, 75mΩ, Electrolytic C Case	100k/31.6k	550	39.2k	800	1.5
5V to 27V	8V	2 x 4.7μF, 50V, X5R, 0805	22μF, 10V, X7R, 1206 100μF, 16V, 100mΩ, Electrolytic D Case	100k/17.4k	500	45.3k	800	1.5
5V to 35V	12V	2 x 4.7μF, 50V, X5R, 0805	22μF, 25V, X5R, 0805 68μF, 16V, 200mΩ, Electrolytic C Case	100k/11k	600	36.5k	800	1.5
5.9V to 36V	18V	2 x 4.7μF, 50V, X5R, 0805	22μF, 25V, X5R, 0805 47μF, 25V, 900mΩ, Electrolytic D Case	100k/6.98k	500	45.3k	800	1.5
7.5V to 36V	24V	2 x 4.7μF, 50V, X5R, 0805	22μF, 25V, X5R, 0805 33μF, 25V, 300mΩ, Electrolytic D Case	100k/5.23k	650	31.6k	800	1.5
7.5V to 36V	36V	2 x 4.7μF, 50V, X5R, 0805	10μF, 50V, X5R, 1206 10μF, 50V, 120mΩ, Electrolytic 6.3mm x 6mm Case	100k/3.40k	650	31.6k	800	1.5



6

Title: Clock–Radio Main

Rev: 0.5

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1 2 3 4 5 6 7 8 9 10

H

H

VDD AMP Vsense

G

G

F

F

E

E

D

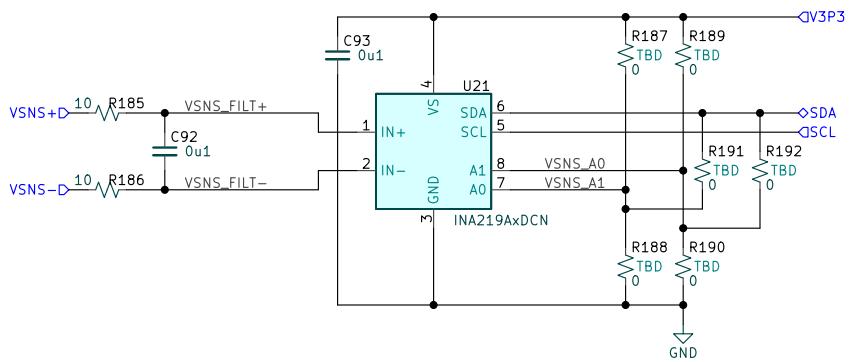
D

C

C

B

B



A Title: Clock-Radio Main

Rev: 0.5

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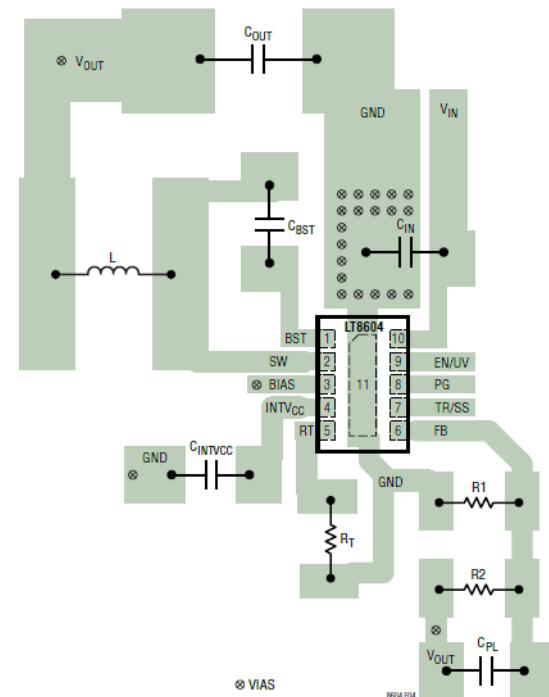


1 2 3 4 5 6 7 8 9 10

A

1 2 3 4 5 6 7 8 9 10

3.3 V Bluetooth



The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R2 = R1 \left(\frac{V_{out}}{0.778V} - 1 \right)$$

1% resistors are recommended to maintain output voltage accuracy.

Title: Clock-Radio Main

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1 2 3 4 5 6 7 8 9 10

1 2 3 4 5 6 7 8 9 10

H

H

3.3 V MP Vsense

G

G

F

F

E

E

D

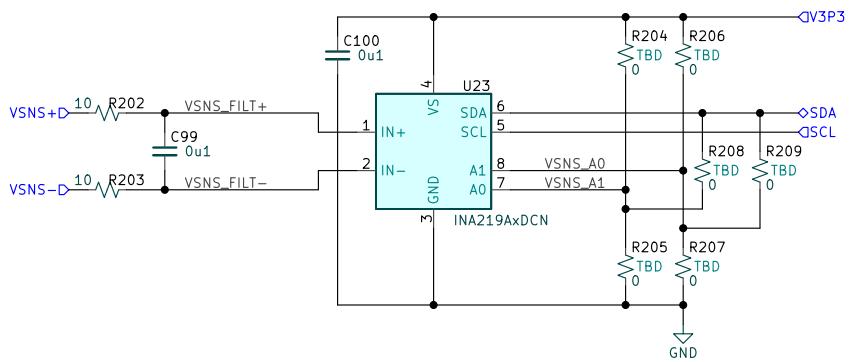
D

C

C

B

B



A Title: Clock-Radio Main

Rev: 0.5

2022-03-05

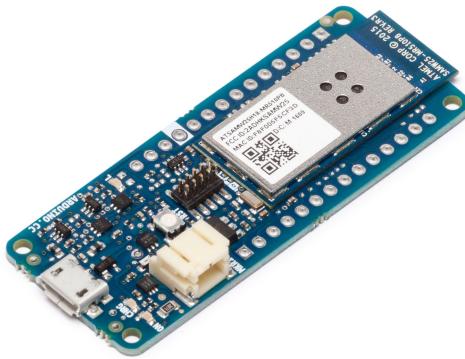
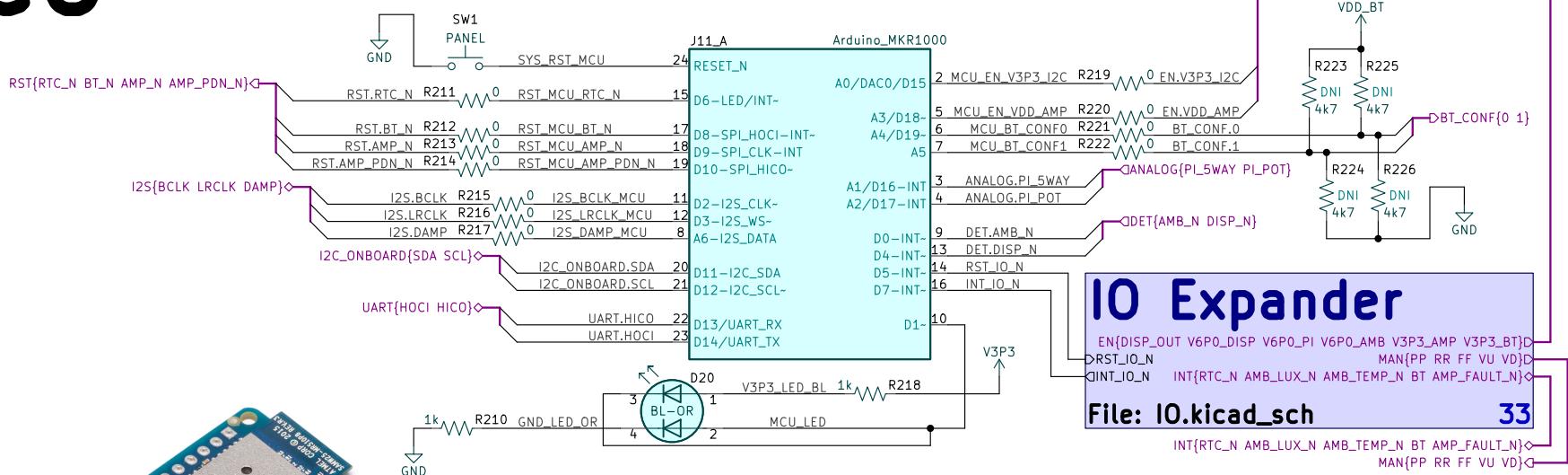
31 / 39 Size: A



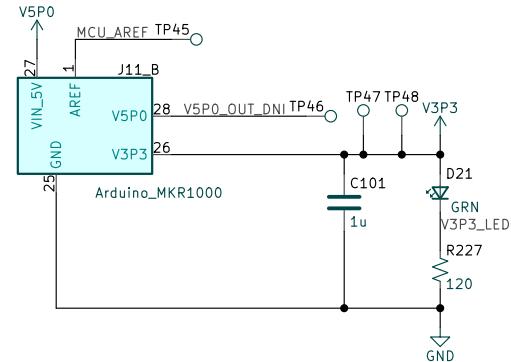
1 2 3 4 5 6 7 8 9 10

A

A



Offboard: ATSAMW25-Wifi Module



Title: Clock–Radio Main

Rev: 0.5

2022-03-05

32 / 39 Size: A



1 2 3 4 5 6 7 8 9 10

IO Expander

G

F

E

D

C

B

A

H

G

F

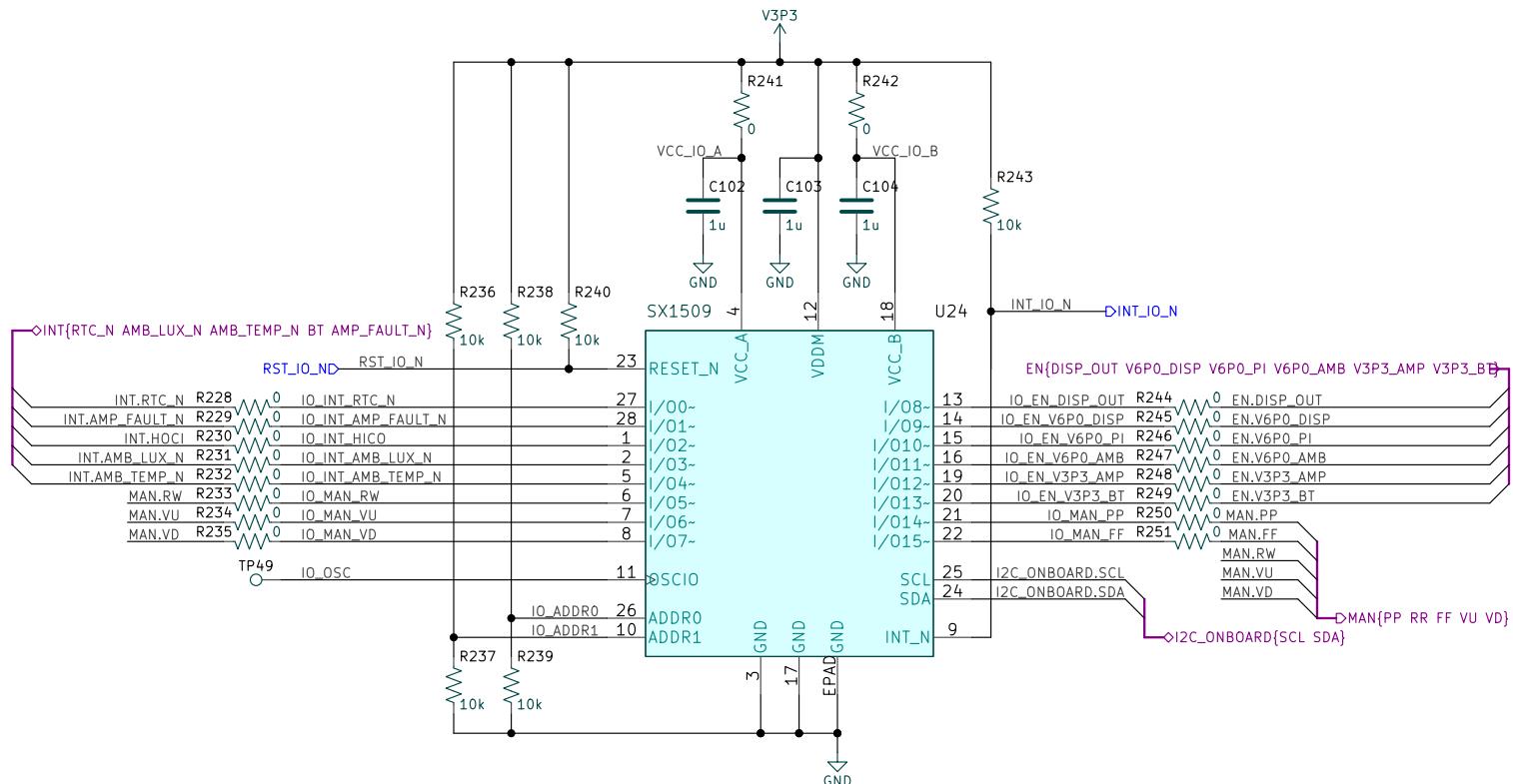
E

D

C

B

A



Title: Clock-Radio Main

Rev: 0.5

2022-03-05

33 / 39 Size: A



1 2 3 4 5 6 7 8 9 10

1 2 3 4 5 6 7 8 9 10

Board Temp

G

F

E

D

C

B

A

H

G

F

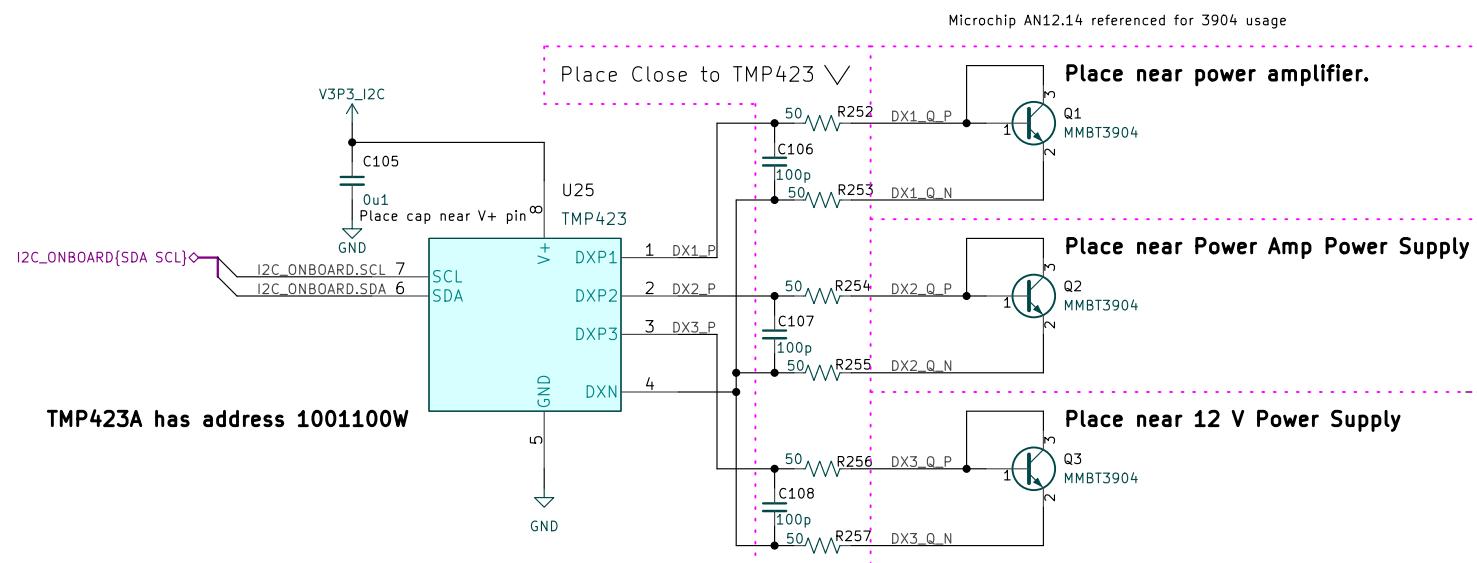
E

D

C

B

A



Title: Clock-Radio Main

Rev: 0.5

2022-03-05

34 / 39 Size: A



1 2 3 4 5 6 7 8 9 10

1 2 3 4 5 6 7 8 9 10

RTC

G

F

E

D

C

B

A

H

G

F

E

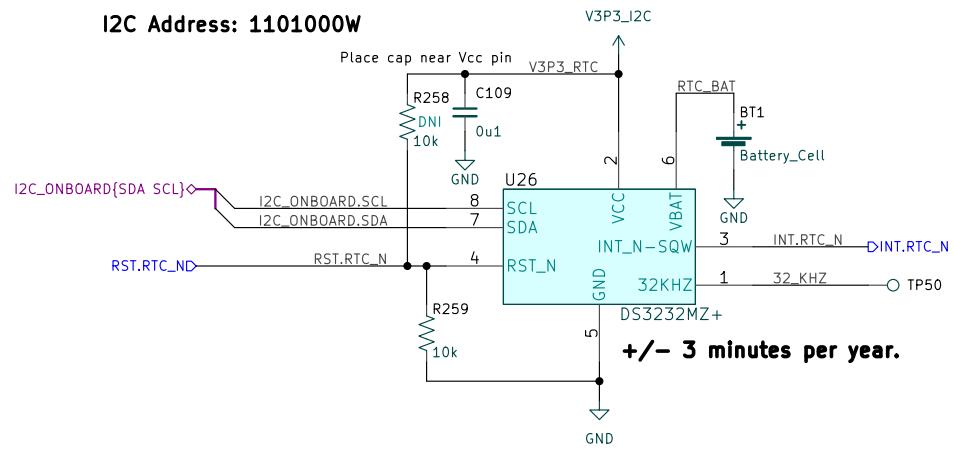
D

C

B

A

I2C Address: 1101000W



Title: Clock-Radio Main

Rev: 0.5

2022-03-05

35 / 39 Size: A



1 2 3 4 5 6 7 8 9 10

1 2 3 4 5 6 7 8 9 10

Audio Top

G

F

E

D

C

B

A

H

G

F

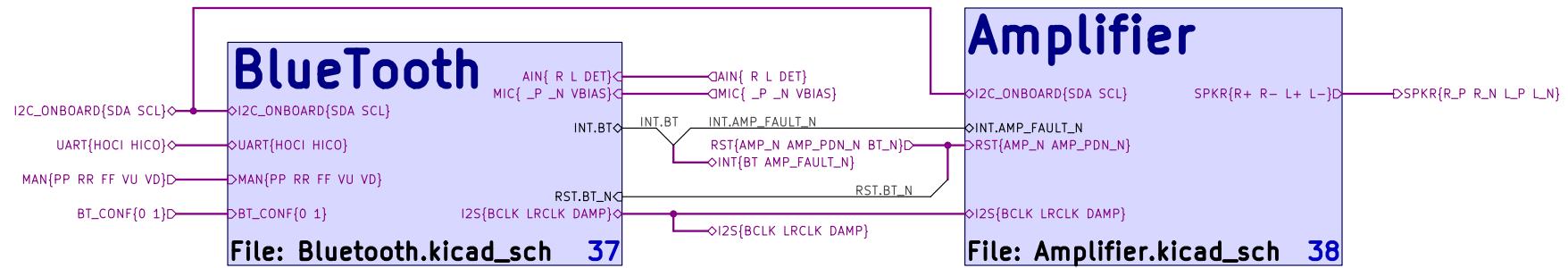
E

D

C

B

A



Title: Clock–Radio Main

Rev: 0.5

2022-03-05

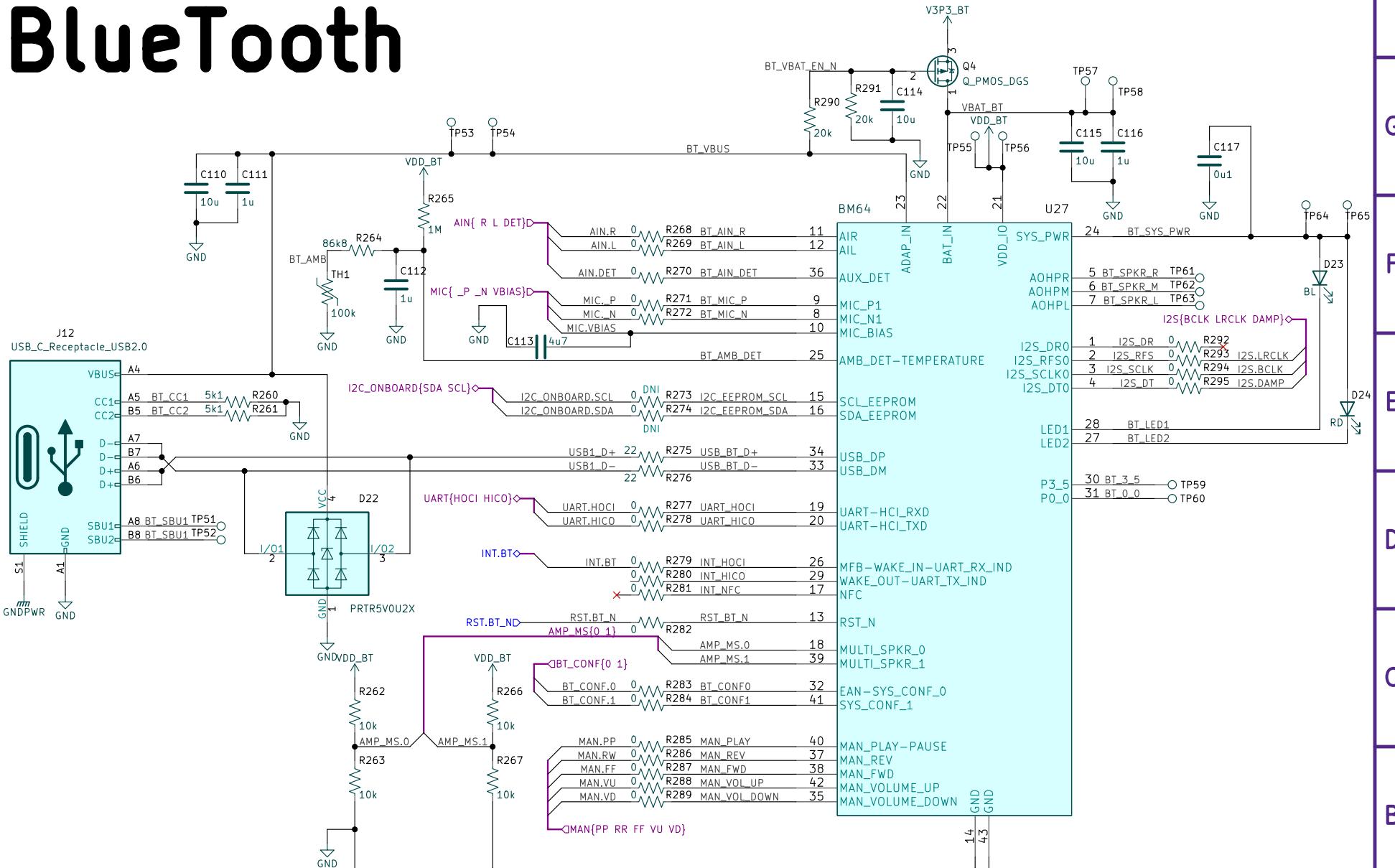
36 / 39 Size: A



1 2 3 4 5 6 7 8 9 10

1 2 3 4 5 6 7 8 9 10

BlueTooth



Title: Clock-Radio Main

Rev: 0.5

2022-03-05

37 / 39

Size: A



1 2 3 4 5 6 7 8 9 10

1	2	3	4	5	6	7	8	9	10
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Amplifier

G

F

E

D

C

B

A

H

G

F

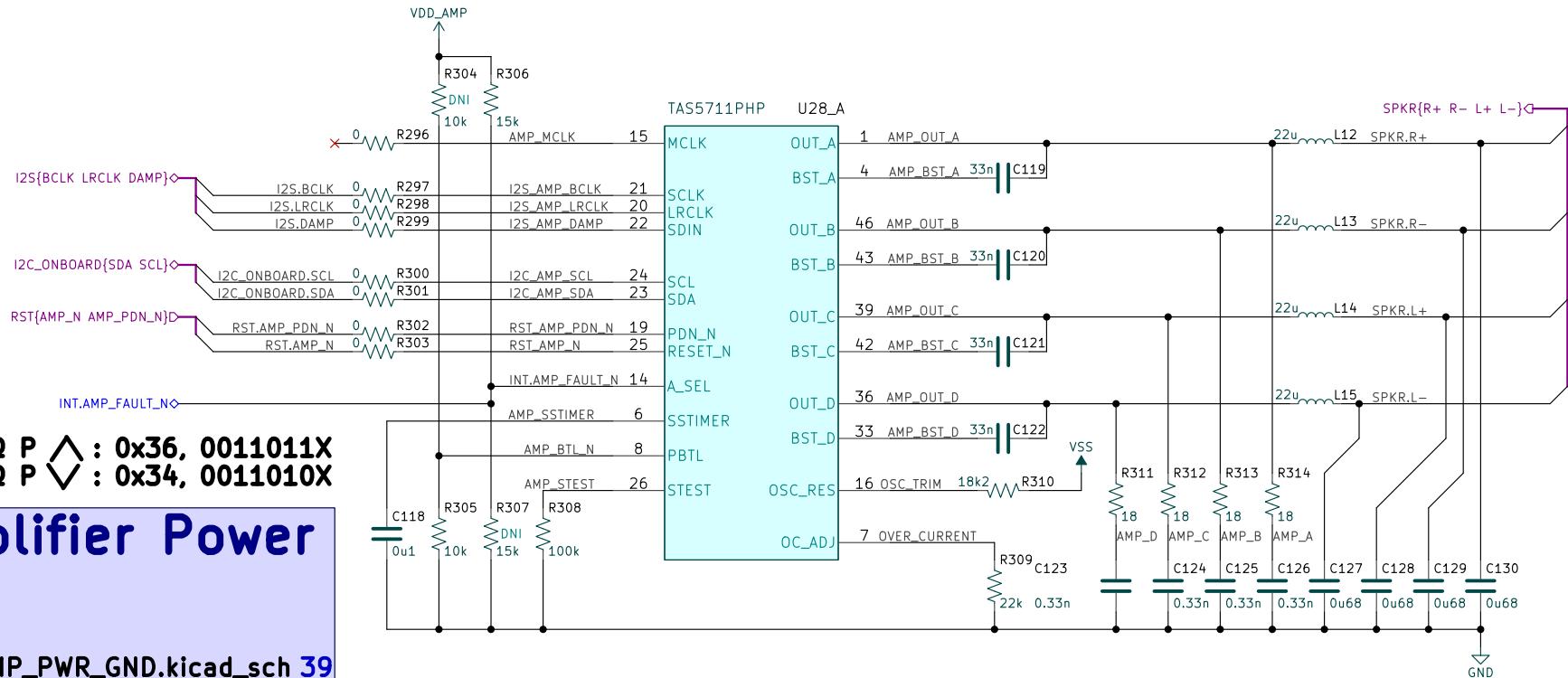
E

D

C

B

A



Title: Clock-Radio Main

Rev: 0.5 | 2022-03-05 | 38 / 39 | Size: A



1 2 3 4 5 6 7 8 9 10

Amplifier Power

G

F

E

D

C

B

A

H

G

F

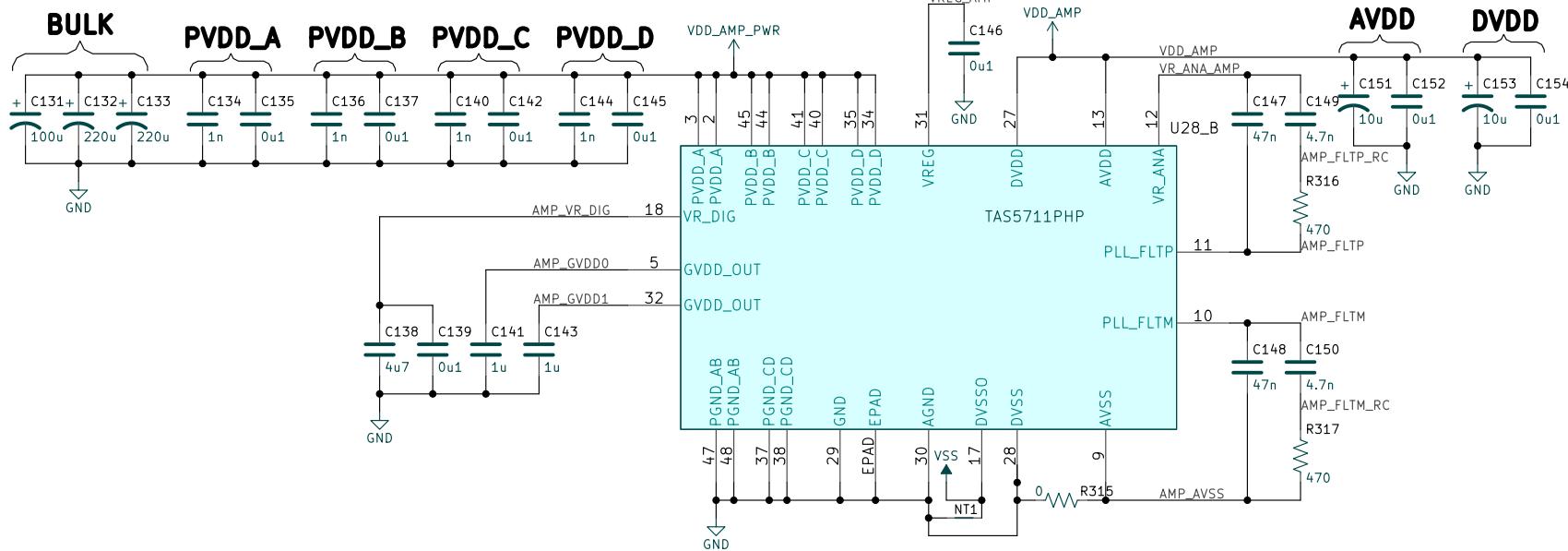
E

D

C

B

A



Title: Clock-Radio Main

Rev: 0.5

2022-03-05

39 / 39 Size: A



1 2 3 4 5 6 7 8 9 10