Computer Engineering Department, S V N I T, Surat
Mid-Semester Examinations, September 2018

B Tech II (CO) – 3rd semester
Course: Computer Organization (CO201)

Dated: 25th Sep 2018 | Time: 11:00 hrs to 12:30 hrs | Max Marks: 30

Instructions:
1. Write your B. Tech. Admission No. and other details clearly on the answer books and B. Tech. Admission No. on the question paper.
2. Assume any necessary data but give proper justifications.
3. Be precise and clear in answering the questions.
4. Calculator is allowed.

Q. 1 Answer the following [Any Five]: **[05]**

1) From the six levels of computer, identify two levels from which lower level is different for different computers but the higher level can be common for different computers.
2) Explain the drawback of von Neumann model and also explain the signifacance of non von Neumann model by listing some of the non von Neumann models.
3) Write the features which are known to the translator for the translation of the high level program to machine level program.
4) List the categories of different type of instruction without which instruction set is INCOMPLETE.
5) Justify the statement: If more operands in the instruction lead to more complex instuctions.
6) Explain the ISA design principle which can improve clock rate of the processor.

Q. 2 Answer the following [Any Two]: **[04]**

1) Store $183CFF_{16}$ in Intel 32-bit processor.
2) Explain with its pros and cons the GPR architecture utilized in VAX machines.
3) Show the branch instruction format component for MIPS-32 bit architecture and write the possible number of instructions to skip forward or backward direction for the target branch instruction, if condition is true.

Q. 3 Write MIPS instructions for given 'c' code given on address 40000_{10}. Also with explanation of addressing mode show the target address calculation and its offset, for branch instruction(s), if any. Consider i in $s1, j in $s2, k in $s3 and base address of A in $s4. **[06]**

```
i=1, j=2, k=3;
if ( i == j || i == k )
  A[i++]=i ;
else
  j-- ;
j = i + k ;
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Q. 4 Answer the following [Any Three]: **[06]**

1) A block-set-associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words.
   a. How many bits are there in a main memory address?
   b. How many bits are there in each of the TAG, SET and WORD fields?

2) The average seek time and rotational delay in a disk system are 6 ms and 3 ms, respectively. The rate of data transfer to or from the disk is 30 Mbytes/sec and all disk accesses are for 8 Kbytes of data. Disk DMA controllers, the processor, and the main memory are all attached to a single bus. The bus data width is 32 bits, and a bus transfer to or from the main memory takes 10 nanoseconds.
   What percentage of main memory cycles are stolen by a disk unit, on average, over a long period of time during which a sequence of independent 8K-byte transfers takes place?

3) Calculate $[(1.666015625 \times 10^0) \times (1.9760 \times 10^4 + (-1.9744 \times 10^4))]$ using half precision format.

4) A computer consists of RAM chips of 256×8 and ROM chips of 1024×8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers.
   a. How many RAM and ROM chips are needed?
   b. Draw a memory-address map for the system.

Q. 5 Answer the following [Any One]: **[04]**

1) Consider a 32-bit microprocessor that has an on-chip 16 Kbyte four-way set-associative cache. Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss. Where in the cache in the word four memory location ABCDE8F8 mapped?
2) Using booth's algorithm multiply two 8 bit numbers (-24 × 30).

Q. 6 Assume a computer has L1 and L2 caches. The cache block consists of 8 words. Assume that the hit rate is the same for both caches and that it is equal to 0.95 for instructions and 0.90 for data. Assume also that the times needed to access an 8-word block in these caches are C_1=1 cycle and C_2=10 cycles. **[05]**

   a. What is the average time experienced by the processor if the main memory uses interleaving?
   b. What is the average access time if the main memory is not interleaved?
   c. What is the improvement obtained with interleaving?

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