KIIT Deemed to be University
Online End Semester Examination (Spring Semester-2022)

Subject Name & Code: Computer Organization (CS 3042) **Applicable to Courses: B.Tech**

Full Marks=50 **Time:2 Hours**

SECTION-A(Answer All Questions. Each question carries 2 Marks)

Time:30 Minutes **(7×2=14 Marks)**

Scheme of Evaluation

<table>
<tr><th>Question No</th><th>Question</th><th>Scheme of Evaluation</th></tr>
<tr><td>Q.No:1</td><td>Define Computer architecture and computer organization.</td><td>Computer Architecture is concerned with the way hardware components are connected together to form a computer system. 1mark
Computer Organization is concerned with the structure and behaviour of a computer system as seen by the user. It acts as the interface between hardware and software. 1mark</td></tr>
<tr><td></td><td>Compare Van-Neumann architecture with Harvard architecture.</td><td>
<table>
<tr><th>BASIS OF COMPARISON</th><th>VON NEUMANN ARCHITECTURE</th><th>HARVARD ARCHITECTURE</th></tr>
<tr><td>Description</td><td>The Von Neumann architecture is a theoretical design based on the stored-program computer concept.</td><td>The Harvard architecture is a modern computer architecture based on the Harvard Mark I relay-based computer model.</td></tr>
<tr><td>Memory System</td><td>Has only one bus that is used for both instructions fetches and data transfers.</td><td>Has separate memory space for instructions and data which physically separates signals and storage code and data memory.</td></tr>
<tr><td>Instruction Processing</td><td>The processing unit would require two clock cycles to complete an instruction.</td><td>The processing unit can complete an instruction in one cycle if appropriate pipelining plans have been set.</td></tr>
<tr><td>Use</td><td>Von Neumann architecture is usually used literally in all machines from desktop computers,</td><td>Harvard architecture is a new concept used specifically in microcontrollers and digital signal processing (DSP).</td></tr>
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			notebooks, high performance computers to workstations.	
		Cost	Instructions and data use the same bus system therefore the design and development of control unit is simplified, hence the cost of production becomes minimum.	Complex kind of architecture because it employs two buses for instruction and data, a factor that makes development of the control unit comparatively more expensive.

Any two point-2mark

	Differentiate between the little endian and the big endian.	• **Little Endian** − In this scheme, low-order byte is stored on the starting address (A) and high-order byte is stored on the next address (A + 1)-**1Mark** • **Big Endian** − In this scheme, high-order byte is stored on the starting address (A) and low-order byte is stored on the next address (A + 1)-**1Mark** **Each-1mark**

	Differentiate between CISC vs RISC.	**RISC**	**CISC**
		It is a Reduced Instruction Set Computer.	It is a Complex Instruction Set Computer.
		It emphasizes on software to optimize the instruction set.	It emphasizes on hardware to optimize the instruction set.
		It is a hard wired unit of programming in the RISC Processor.	Microprogramming unit in CISC Processor.
		It requires multiple register sets to store the instruction.	It requires a single register set to store the instruction.
		RISC has simple decoding of instruction.	CISC has complex decoding of instruction.
		Uses of the pipeline are simple in RISC.	Uses of the pipeline are difficult in CISC.
		It uses a limited number of instruction that requires less time to execute the instructions.	It uses a large number of instruction that requires more time to execute the instructions.
		It uses LOAD and STORE	It uses LOAD and STORE

		that are independent instructions in the register-to-register a program's interaction.	instruction in the memory-to-memory interaction of a program.
		RISC has more transistors on memory registers.	CISC has transistors to store complex instructions.
		The execution time of RISC is very short.	The execution time of CISC is longer.
		RISC architecture can be used with high-end applications like telecommunication, image processing, video processing, etc.	CISC architecture can be used with low-end applications like home automation, security system, etc.
		It has fixed format instruction.	It has variable format instruction.
		The program written for RISC architecture needs to take more space in memory.	Program written for CISC architecture tends to take less space in memory.
		Example of RISC: ARM, PA-RISC, Power Architecture, Alpha, AVR, ARC and the SPARC.	Examples of CISC: VAX, Motorola 68000 family, System/360, AMD and the Intel x86 CPUs.
		Any four point-2mark	
Q.No:2	What is the role of MAR and MDR?	For MAR-**1mark** For MDR-**1Mark**	
	PC does the same function as MAR, and then justify your answer by keeping two registers instead of one.	The difference is that the program counter points to the next instruction to be fetched / executed, whereas the memory address register points to a memory location where the program being run will fetch some data (not an instruction).-**2mark**	
	What are the functions of external buses?	An external bus primarily enables connecting peripherals and all external devices to a computer. These devices can include storage, monitors, keyboard, mouse and more. Typically, an external bus is composed of electrical circuits that connect and transmit data between the computer and the external device-**2 mark**	
	At the end of a memory read operation, the MDR is loaded with a binary combination, how that combination is interpreted as an instruction or an operand to an instruction?	If the memory operation is initiated by sending the contents of PC to MAR, then the content of MDR will be interpreted as an instruction else as an operand.**(2 mark)**	
Q.No:3	What is the content of R_0 after executing the	Assume RshiftL means logical shift right. After execution, content of R0 is 00111110-**2Mark**	

	following instruction Rshift L #2, R_0 (Where R_0 is of 8 bit data and its content is 11111001.)		
	The content of register R1is 11010110. What will be the decimal value after execution RotateL #2,R1? [Assume the number is represented in 2's complement format]	After rotation R1's content will be 01011011.In Decimal the value will be 155-**2Mark**	
	Evaluate the arithmetic expression X=(P × Q) + R using a general register computer with its equivalent one address instruction format.	LOAD P MUL Q STORE Y LOAD R ADD Y ----------**2Mark**	
	How many memory references are required by the processor to execute the following instructions (i)ADD R1,R2,R3; (ii) PUSH X;	(i)ADD R1,R2,R3; → 1 memory reference---**1 Mark** (ii)PUSH X; → 3memory references-1 Mark	
Q.No:4	An instruction SUB 3000 a) Subtracts 3000 to the value in Accumulator and stores the result in the memory location 3030 b) Subtracts the value in memory location 3000 to the value in Accumulator and stores the result in Accumulator c) Subtracts 3000 to the value in Accumulator and stores the result in Accumulator d) None of the above		b
	An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. If a processor register R1 contains the number 200 then the effective address for immediate and index with R1 as the index register addressing mode of the instruction will be: a. 301 and 600 respectively b.400 and 702 respectively c.200 and 600 respectively d.702 and 400 respectively		a
	ADD takes 1 clock cycle and MULT takes 3 clock cycles. If a program consists of 20 ADD and 10 MULT instructions, and clock rate is 1GHz, what is the average CPI and the execution time? a. 1.66 and 50ns respectively b.1.66 and 40ns respectively c.2 and 50ns respectively d.2 and 40ns respectively		a
	How many times a subroutine should be called so that the stack becomes full,		c

	Assume that the stack address space ranges from 2040 to 1720 and each stack word consumes 4 bytes and machine is byte addressable.[Note: No parameter, return value, registers, local variables are stored in the stack due to subroutine call] a. 70 b.100 c.80 d.60		
Q.No:5	Hardwired control unit is relatively inflexible"-Justify the statement.	When one new instruction is added in a processor having Hardwired CU, all the circuits involving the control signal present in the control sequence for the newly added instruction has to be changed-**2Mark**	
	Explain the necessity of WMFC signal.	WMFC signal is needed for the write control signal / read control signal cause the memory bus interface hardware to issue write command / read command on the memory bus. The processor waits in this process unless the memory operation is completed and a WMFC response is received-**2Mark**	
	Specify the importance of RUN and END control signal in hardwired control unit.	After execution of each instruction End control signal is generated, this resets control step counter and makes it ready for generation of control step for next instruction-**1 Mark** when RUN set to 1, RUN causes the counter to be incremented by one at the end of every clock cycle. When RUN is equal to 0, the counter stops counting. This is needed to cause the processor to wait for the reply from the memory-**1 Mark**	
	Differentiate between Micro-routine and Micro-instruction.	**Micro-routine:** A sequence of control words corresponding to the control sequence of a machine instruction constitutes the micro-routine for that instruction-**1 Mark** **Micro-instruction:** Individual control words in this micro-routine are referred to as microinstructions-**1 Mark**	
Q.No:6	2K SRAM cells are there and if the memory is byte addressable than find the number of external connections.	No of external connections. -19-**2Mark** Address Bus-8 pins Data Bus-8 pins Control lines: 2pins Ground: 1pin	
	How many RAM chips of size 128K × 16 are required to provide a capacity of main memory eq ual to 4M × 32 ?	$128k \times 16 = 2^{17} \times 16$ Required is $4M \times 32 = 2^{22} \times 2 \times 16 = 2^{23} \times 16$ $2^{23} \times 16 = 2^{X} \times 2^{17} \times 16$ x=6, $2^6 = 64$--**2Mark**	
	How many address and data lines will be there for a 64 K x 8 memory system?	$64K = 2^6 \times 2^{10} = 2^{16}$, so there are 16 address lines-**1 Mark** There are 8 data lines-**1 Mark**	
	How much byte-addressable memory you can use with 12 bits address bus?	Total memory will be equal to size of each address * number of addresses = $8 * 2^n$ If n=12 Size of memory = $8 * 2^{12}$ bits = 2^{12} bytes = 2- Kilo	

		Bytes (2^{10} Bytes = 1 KB) = 4 KB--**2Mark**
Q.No:7	What is a Priority Interrupt?	A priority interrupt is a system which decides the priority at which various devices, which generates the interrupt signal at the same time, will be serviced by the CPU. The system has authority to decide which conditions are allowed to interrupt the CPU, while some other interrupt is being serviced. **-2Mark**
	Explain the meaning of Privileged Exception.	To protect the OS of a computer from being corrupted by user program certain instance can be executed only when the processor is in supervisor mode. These are called privileged exceptions. When the processor is in user mode, it will not execute instance (i.e.) when the processor is in supervisor mode , it will execute instance. **-2Mark**
	What do you mean by memory mapped I/O?	When I/O devices and the memory share the same address space, the arrangement is called memory-mapped I/O. Any machine instruction that can access memory can be used to transfer data to or from an I/O device. For example, if the input device in Figure is a keyboard and if DATAIN is its data register, the instruction-**2Mark**
	Define Bus Arbitration. What are the different approaches to bus arbitration	It is the process by which the next device to become the bus master is selected and the bus mastership is transferred to it-**1Mark** There are 2 approaches to bus arbitration. They are, _ Centralized arbitration (A single bus arbiter performs arbitration)-**0.5Mark** _ Distributed arbitration (all devices participate in the selection of next bus master)- **0.5Mark**

SECTION-B(Answer Any Three Questions. Each Question carries 12 Marks)

Time: 1 Hour and 30 Minutes **(3×12=36 Marks)**

Scheme of Evaluation

Question No	Question
Q.No:8	**Q.No:8-1st question** With a neat sketch explain about multiple bus CPU organization. write the control signals to execute following instruction using same organization (i) ADD R1,R2,(R3) (ii) SUB R1,R2,R3 **Scheme of Evaluation** Diagram-----**2Mark** Explanation about single bus CPU organization------**4Mark** **(i) ADD R1,R2,(R3)** 1. PC_{OUT}, R=B, MAR_{IN},Read,IncPC 2.WMFC 3.MDR_{OUTB}, R=B, IR_{IN} 4.R3out, MAR_{IN}, Read, WMFC . 5. R2out , MDRout, add , R1in,End. ----------**3Mark**

(ii) SUB R1,R2,R3

1. PCoutB , R=B , MARin, Read ,incPC
2. WMFC (wait for MFC)
3. MDRoutB, R=B , IRin
4. R1outA , select A , R2outB , SUB , R3in , End----------**3Mark**

Q.No:8-2nd question

With a neat sketch explain about single bus CPU organization. write the sequence of control steps for the following instructions for single bus CPU organization

(i)ADD 10(R3), R4 (ii) SUB R1,R2

Scheme of Evaluation

Diagram-----**2Mark**

Explanation about single bus CPU organization------**4Mark**

i)ADD 10(R3), R4

Ans:

1. PC_{out}, MAR_{in}, Read, Select 4, Add, Z_{in}
2. Z_{out}, PC_{in}, Y_{in}, WMFC
3. MDR_{out}, IR_{in}
4. Offset field of IR_{out}, Y_{in}
5. $R3_{out}$, Select Y, Add, Z_{in}
6. Z_{out}, MAR_{in}, Read
7. $R4_{out}$, Y_{in}, WMFC
8. MDR_{out}, Select Y, Add, Z_{in}
9. Z_{out}, $R4_{in}$, end----------**3Mark**

(ii) SUB R1,R2

Ans:

1. PC_{out}, MAR_{in}, Read, Select 4, Add, Z_{in}
2. Z_{out}, PC_{in}, Y_{in}, WMFC
3. MDR_{out}, IR_{in}
4. $R1_{out}$, Y_{in}
5. $R2_{out}$, Select Y, SUB, Z_{in}
6. Z_{out}, $R1_{in}$, end----------**3Mark**

Q.No:8-3rd question

Explain with neat diagram the working of each unit of Hardwired control organization. State its advantage over micro programmed controls. if a CPU has only three instructions I1, I2 and I3, which use the following signals in time steps T1-T5:

I1:	I2:	I3:
T1:A_{in},B_{out},Cin	T1:C_{in},B_{out},D_{in}	T1:D_{in},A_{out}
T2:PC_{out},B_{in}	T2:A_{out},B_{in}	T2:A_{in},B_{out}
T3:Z_{out},A_{in}	T3:Z_{out},A_{in}	T3:Z_{out},A_{in}
T4:B_{in},C_{out}	T4:B_{in},C_{out}	T4:D_{out},A_{in}
T5:End	T5:End	T5:End

Write the logic function and draw the circuit for generating A_{in}, C_{out} and End

Scheme of Evaluation

Explanation the working of each unit of Hardwired control organization----**3Mark**

	Diagram----**1Mark** Advantage Hardwired control organization-----**2Mark** A_{in}=T3+I1.T1+I3.T4----**1 Mark** Diagram of A_{in}----**1Mark** C_{out}= I1.T4+I2.T4----**1 Mark** Diagram of C_{out} ----**1Mark** End=T5---**1 Mark** Diagram of End ----**1Mark**
Q.No:9	**Q.No:9-1st question** a. Define parallel processing and explain the flynn's classification of computer with suitable diagram. [6]. b. Consider a pipeline having 4 phases with duration 60, 50, 100 and 80 ns. Given latch delay is 10 ns. [6]. Calculate- I. Pipeline cycle time II. Non-pipeline execution time III. Speed up ratio IV. Pipeline time for 1000 tasks V. Sequential time for 1000 tasks VI. Throughput **I.Cycle time** = Maximum delay due to any stage + Delay due to its register = Max { 60, 50, 100, 80 } + 10 ns = 100ns + 10 ns = 110 ns-------**1 Mark** **II.Non-Pipeline Execution Time-** Non-pipeline execution time for one instruction = 60 ns + 50 ns + 100 ns + 80 ns = 290 ns-------**1 Mark** III. **Speed Up Ratio-** Speed up = Non-pipeline execution time / Pipeline execution time = 290 ns / 110 ns = 2.67-------**1 Mark** **IV. Pipeline Time For 1000 Tasks-** Pipeline time for 1000 tasks = Time taken for 1st task + Time taken for remaining 999 tasks = 1 x 4 clock cycles + 999 x 1 clock cycle = 4 x cycle time + 999 x cycle time = 4 x 110 ns + 999 x 110 ns = 440 ns + 99900 ns = 110330 ns-------**1 Mark** V.**Sequential Time For 1000 Tasks-** Non-pipeline time for 1000 tasks = 1000 x Time taken for one task = 1000 x 290 ns = 290000 ns-------**1 Mark** V.Throughput- Throughput for pipelined execution = Number of instructions executed per unit time = 1000 tasks / 110330 ns-------**1 Mark**

Q.No:9-2nd question

a. Explain briefly about different type of hazards in pipelining. [6].

There are three types of hazards:

Structural hazards: Hardware cannot support certain combinations of instructions (two instructions in the pipeline require the same resource).

Data hazards: Instruction depends on result of prior instruction still in the pipeline

Control hazards or instruction hazard: Caused by delay between the fetching of instructions and decisions about changes in control flow (branches and jumps).

Explanation of each hazard (2 mark each)

b. Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of 5. The same processor is upgraded to a pipelined processor with five stages but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume there are no stalls in the pipeline. What is the speed up achieved in this pipelined processor ? [6].

Solution-

Cycle Time in Non-Pipelined Processor-

Frequency of the clock = 2.5 gigahertz

Cycle time

= 1 / frequency

= 1 / (2.5 gigahertz)

= 1 / (2.5 x 10^9 hertz)

= 0.4 ns-----**1 Mark**

Non-Pipeline Execution Time-

Non-pipeline execution time to process 1 instruction

= Number of clock cycles taken to execute one instruction

= 5 clock cycles

= 5 x 0.4 ns

= 2 ns-----**1 Mark**

Cycle Time in Pipelined Processor-

Frequency of the clock = 2 gigahertz

Cycle time

= 1 / frequency

= 1 / (2 gigahertz)

= 1 / (2 x 10^9 hertz)

= 0.5 ns-----1 Mark

Pipeline Execution Time-

Since there are no stalls in the pipeline, so ideally one instruction is executed per clock cycle. So,

Pipeline execution time

= 1 clock cycle

= 0.5 ns-----**1.5 Mark**

Speed Up-

Speed up

= Non-pipeline execution time / Pipeline execution time

= 2 ns / 0.5 ns

= 4-----**1.5 Mark**

Q.No:9-3rd question

a. Discuss the basic concepts of pipelining with necessary diagram and differentiate between Arithmetic Pipeline and Instruction Pipeline. [6].

Basic concepts of pipelining-**2Mark**

Diagram-**1Mark**

differentiate between Arithmetic Pipeline and Instruction Pipeline-**3Mark**

b. The stage delays in a 4 stage pipeline are 1000, 800, 500 and 400 picoseconds. The first stage is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. Calculate the % throughput increase in the pipeline.

Solution-

Execution Time in 4 Stage Pipeline-

Cycle time

= Maximum delay due to any stage + Delay due to its register

= Max { 1000,800, 500, 400} + 0

= 1000 picoseconds

Thus, Execution time in 4 stage pipeline = 1 clock cycle = 1000 picoseconds---**1Mark**

Throughput in 4 Stage Pipeline-

Throughput

= Number of instructions executed per unit time

= 1 instruction / 1000 picoseconds ---**1Mark**

Execution Time in 2 Stage Pipeline-

Cycle time

= Maximum delay due to any stage + Delay due to its register

= Max { 600, 350 } + 0

= 600 picoseconds

Thus, Execution time in 2 stage pipeline = 1 clock cycle = 600 picoseconds---**1Mark**

Throughput in 2 Stage Pipeline-

Throughput

= Number of instructions executed per unit time

= 1 instruction / 600 picoseconds---**1Mark**

Throughput Increase-

Throughput increase

= { (Final throughput – Initial throughput) / Initial throughput } x 100

= { (1 / 600 – 1 / 1000) / (1 / 1000) } x 100

=66.67%---**2Mark**

Q.No:10

Q.No:10-1st question

A.Discuss Memory Hierarchy and with a suitable diagram explain the working principle of SRAM chip. [6].

Explanation of memory Hierarchy--**2Mark**

Diagram-**1Mark**

Explanation of working principle of SRAM chip-**3 mark**

B.If a computer system uses 16 bit memory addresses. It has 2K-byte cache organized in a direct-mapped manner. With 64 bytes per cache block. Assume that the size of each memory word is 1 byte .[6].

I. Find the Size of ta g, block and word.

II. If 4 way set associative is used then find the size of tag and set

I. Block size = 64 bytes = 2^6 bytes = 2^6 words (since 1 word = 1 byte)
Therefore, **Number of bits in the *Word* field = 6---1 mark**
Cache size = 2K-byte = 2^{11} bytes
Number of cache blocks = Cache size / Block size = $2^{11}/2^6 = 2^5$
Therefore, **Number of bits in the *Block* field = 5---1 mark**
Total number of address bits = 16
Therefore, **Number of bits in the *Tag* field = 16 - 6 - 5 = 5---1 mark**

II,
Block size = 64 bytes = 2^6 bytes = 2^6 words
Therefore, **Number of bits in the *Word* field = 6**
Cache size = 2K-byte = 2^{11} bytes
Number of cache blocks per set = 4
Number of sets = Cache size / (Block size * Number of blocks per set) = $2^{11}/(2^6 * 4) = 2^3$
Therefore, **Number of bits in the *Set* field - 2 mark**
Total number of address bits = 16
Therefore, **Number of bits in the *Tag* field = 16 - 6 - 3 = 7-1 mark**

Q.No:10-2nd question

a. With a suitable diagram explain the working principle of DRAM chip and state the advantages of DRAM over SRAM. [6].
Digram-**1 mark**
working principle-**3 Mark**
advantages of DRAM over SRAM-**2 Mark**

b. If a cache consists of a total of 512 blocks. The main memory contains 16K blocks, each consisting of 32 words. [6].
I. What is the size of the main memory and cache memory?
II. How many bits are there in each of the TAG, INDEX, and BLOCK OFFSET field in case of direct mapping?
III. How many bits are there in each of the TAG, and BLOCK OFFSET field in case of associative mapping?

Total cache blocks = 512
Total words in cache =512 X 32 =16K.

Total main memory blocks = 16K Total words= 512K
Address bus size= 19 bits.

(i) Size of main memory=512 KB—**1.5 mark**
Size of cache memory=16KB
(ii) TAG= 5 bits, Index/ BLOCK=9 bits, WORD=5 bits--**1.5 mark**
(iii) TAG=14, WORD=5--**1.5 mark**
(iv) TAG=7 bits, SET=7 bits, WORD=5 bits.
4 blocks= 1 set
512 blocks=128 set
So bits in set block = $\log_2 128$ = 7 bits -**1.5 mark**

	Q.No:10-3rd question a. Write different mapping techniques in cache with their merits and demerits [6]. Mapping are of 3 types Direct Mapping Associative Mapping Set associative Mapping **Explanation of each mpping-2 Mark each** b. Consider a cache consisting of 128 blocks of 16 words each, for a total of 2048 (2K) words, and assume that the main memory is addressable by a 16-bit address. The main memory has 64K words, which we will view as 4K blocks of 16 words each. For simplicity, we have assumed that consecutive addresses refer to consecutive words. Find the size of Block, word and Tag for main memory and Cache [6]. **Main Memory :** Total no of words(row) = 64K = 2 ^ 6 X 2^10=2^16 words No of blocks = Total no of Words/ No of words of block = 2^16/ 2^4 =2^12- No of word-4-**1 Mark** No of Block-12-**1mark** **Tag-0--1mark** **Cache Memory :** No of Blocks :128 =2^7 i.e. 7--**1mark** Each Block contains 16 words = 2^4 No of word-4-**1 Mark** Tag bit=16-12=4--**1 Mark**
Q.No:11	**Q.No:11-1st question** Explain Direct Memory Access method with its requirement and explain the daisy chain method for handling simultaneous interrupt request?[12] **Explanation of Direct Memory Access method-6 Mark** **daisy chain method for handling simultaneous interrupt request-6 Mark**
	QNo:11-2nd question Explain the different modes of data transfer between the central unit and I/O devices.[12] Data transfer between the central unit and I/O devices can be handled in generally three types of modes which are given below: 1. Explanation of Programmed I/O-**4Mark** 2. Explanation of Interrupt Initiated I/O-**4Mark** 3. Explanation of Direct Memory Access-**4Mark**
	Q.No:11-3rd question Summarize the sequence of events involved in handling an interrupt request from a single device. How does the processor resolves among simultaneous interrupt requests? [12] Summarization-**6mark** Resolution of simultaneous interrupt requests-**6mark**