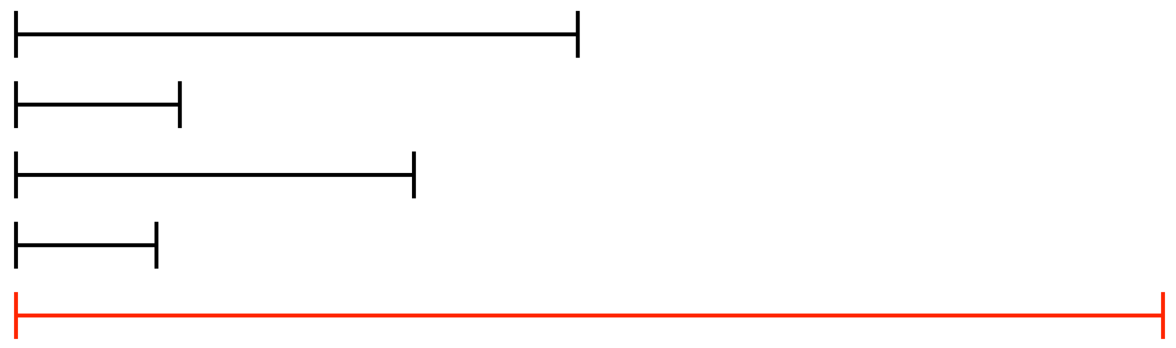
# Multi Cycle CPU

Jason Mars

## Why a Multiple Cycle CPU?



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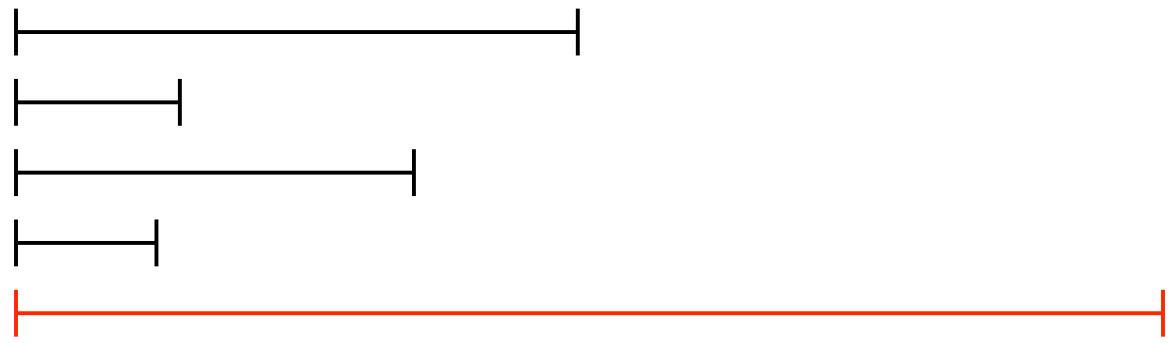

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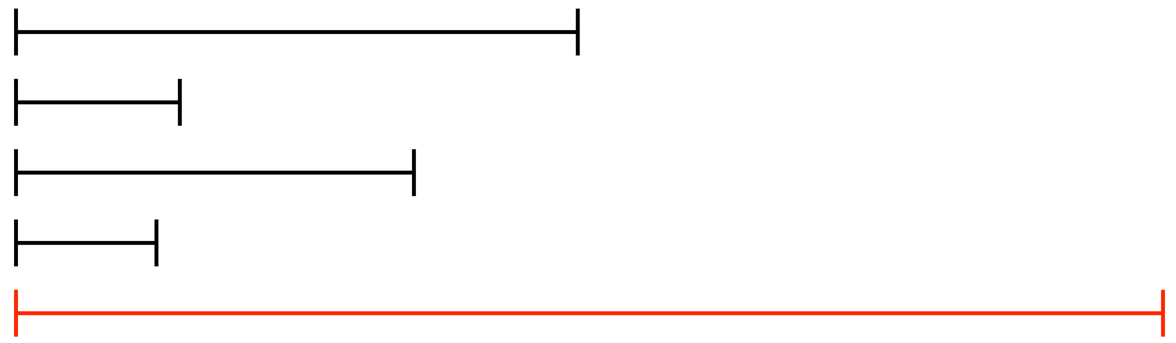

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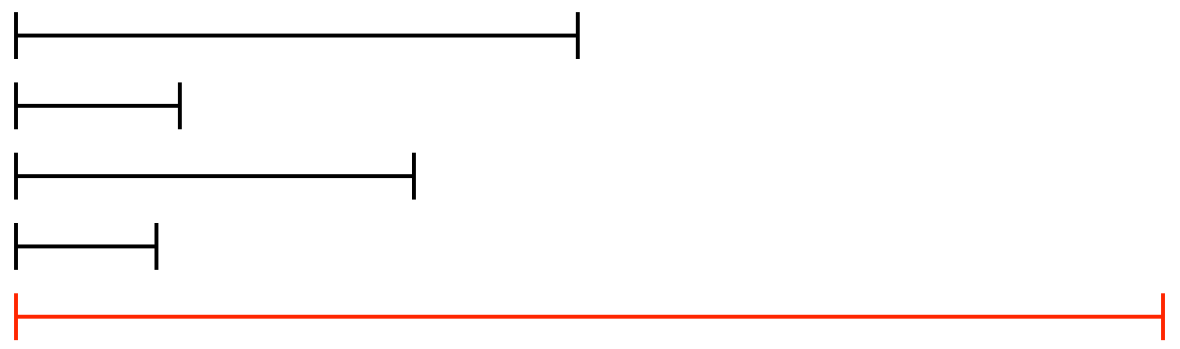

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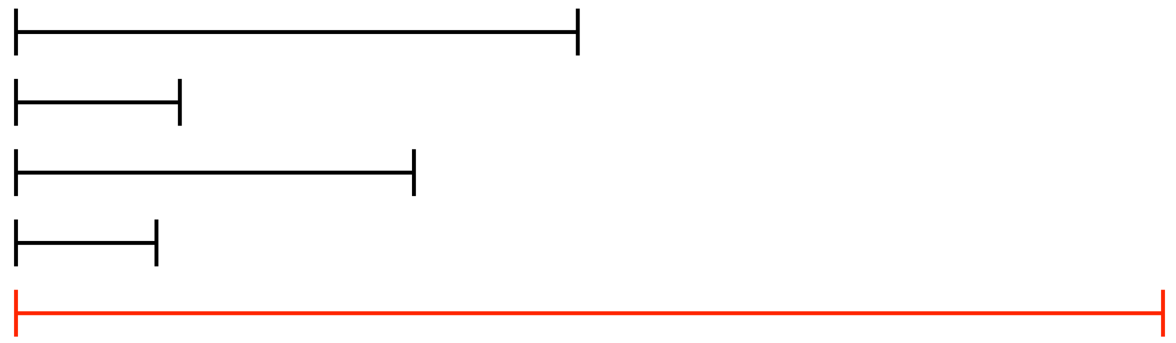

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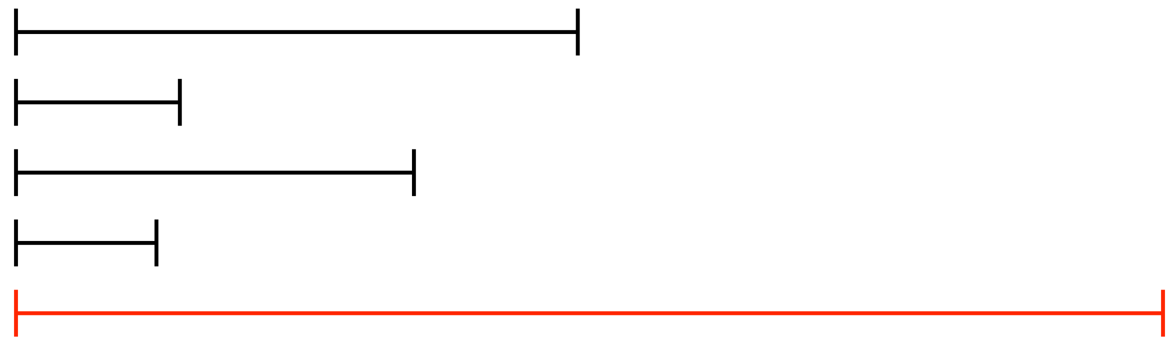
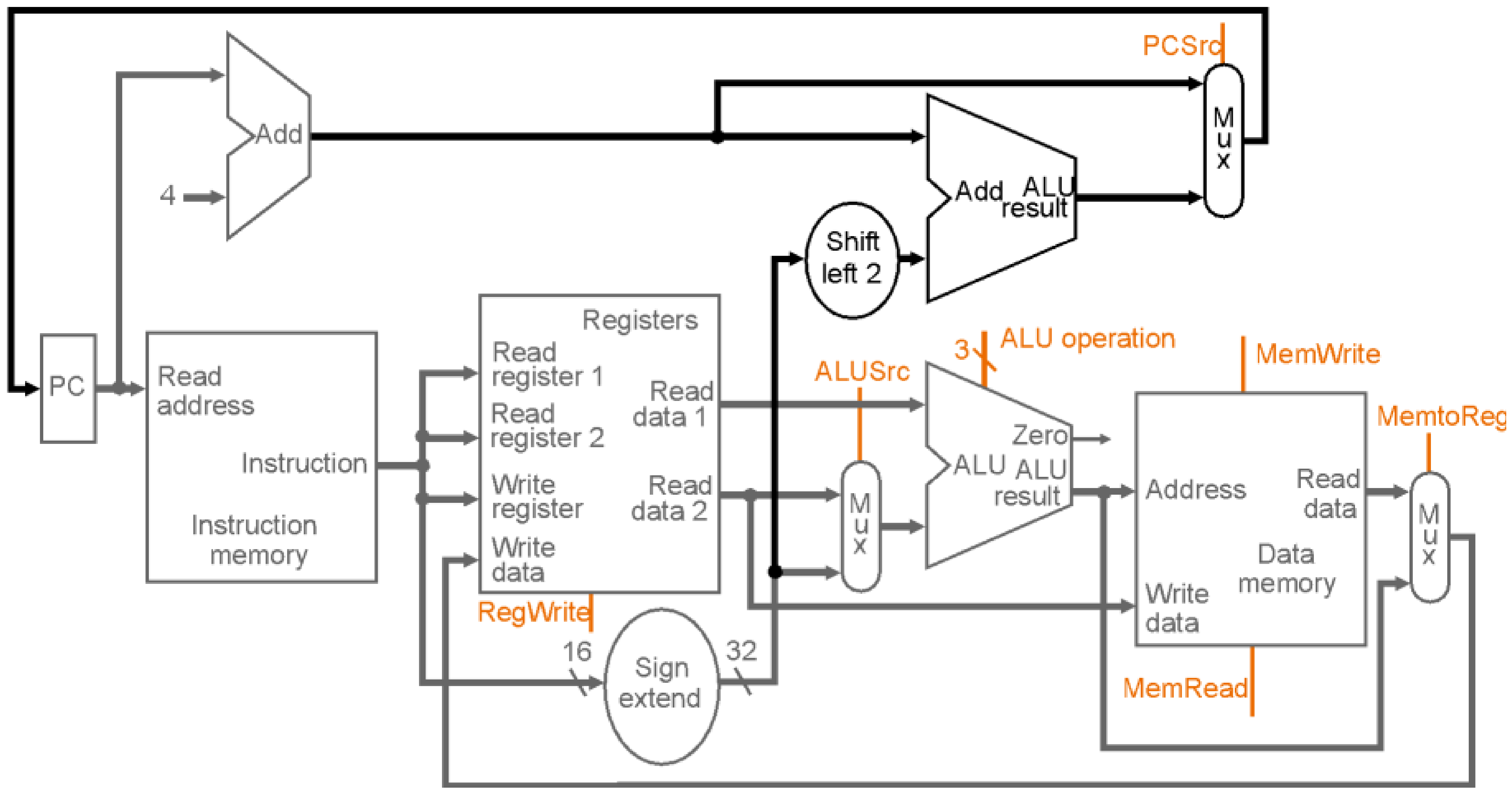
- ET = IC * CPI * CT



# High Level View



# Breaking Execution into Clock Cycles

- We will have five execution steps (not all instructions use all five)
  - fetch
  - decode & register fetch
  - execute
  - memory access
  - write-back
- We will use Register-Transfer-Language (RTL) to describe these steps

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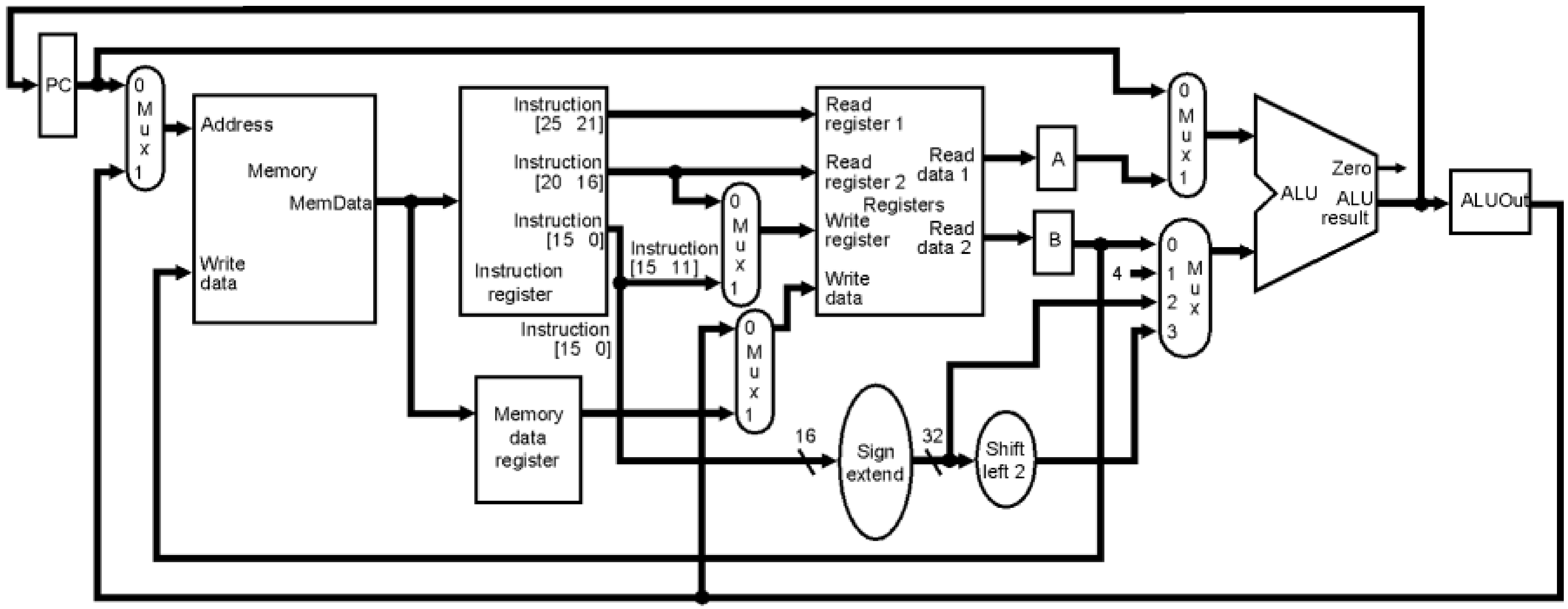
- Significantly complicates control. **Why?**
- The goal is to balance the amount of work done each cycle.

# Multi-Cycle Datapath



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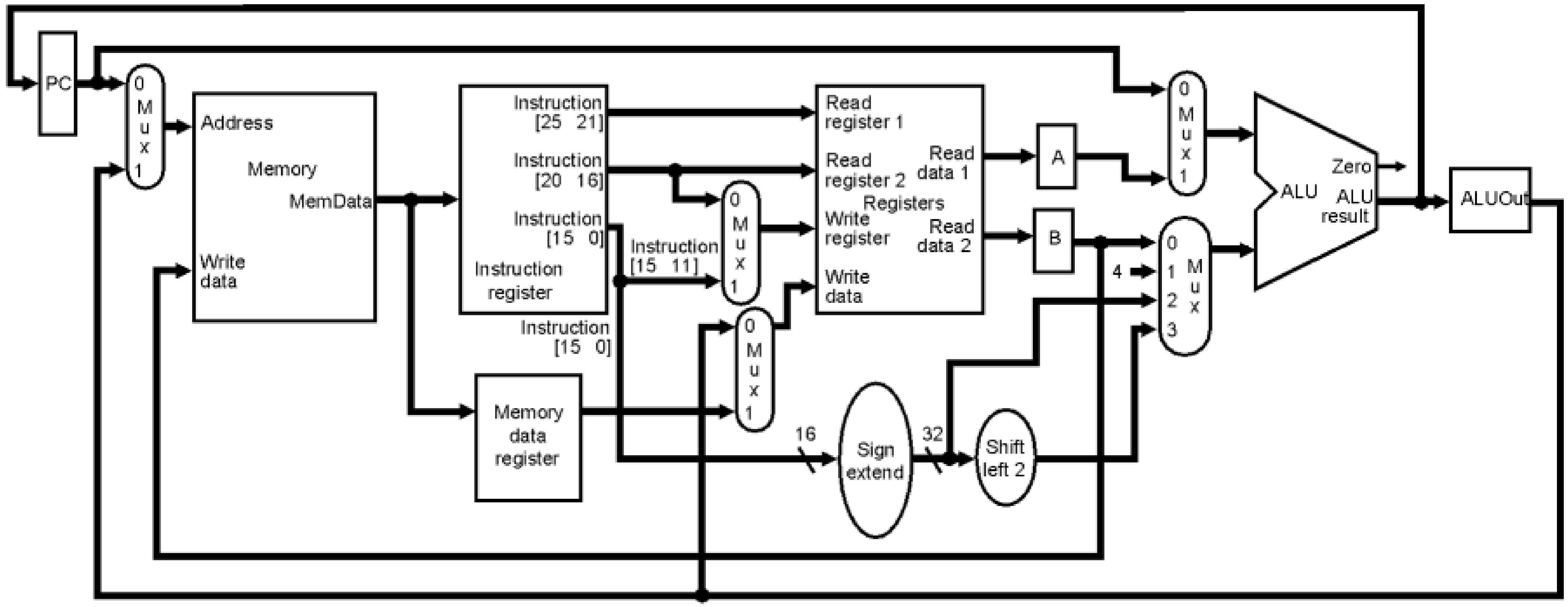

- **More Latches**

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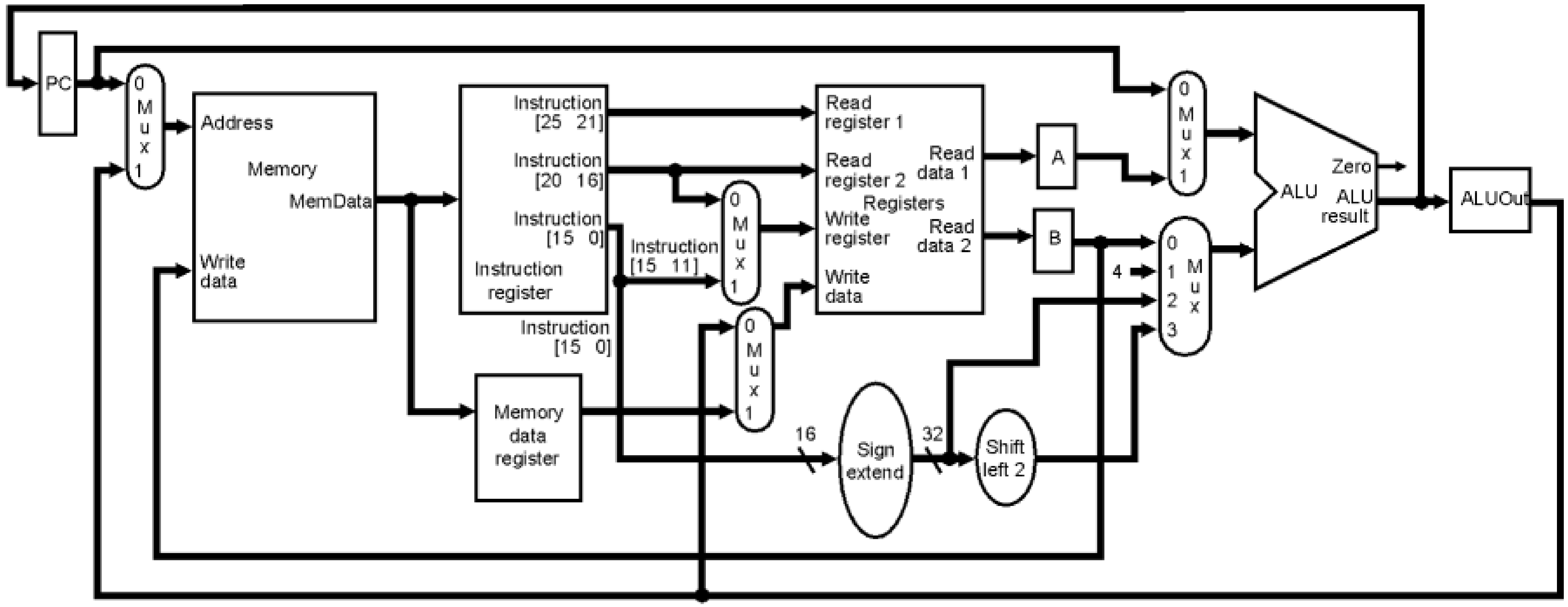

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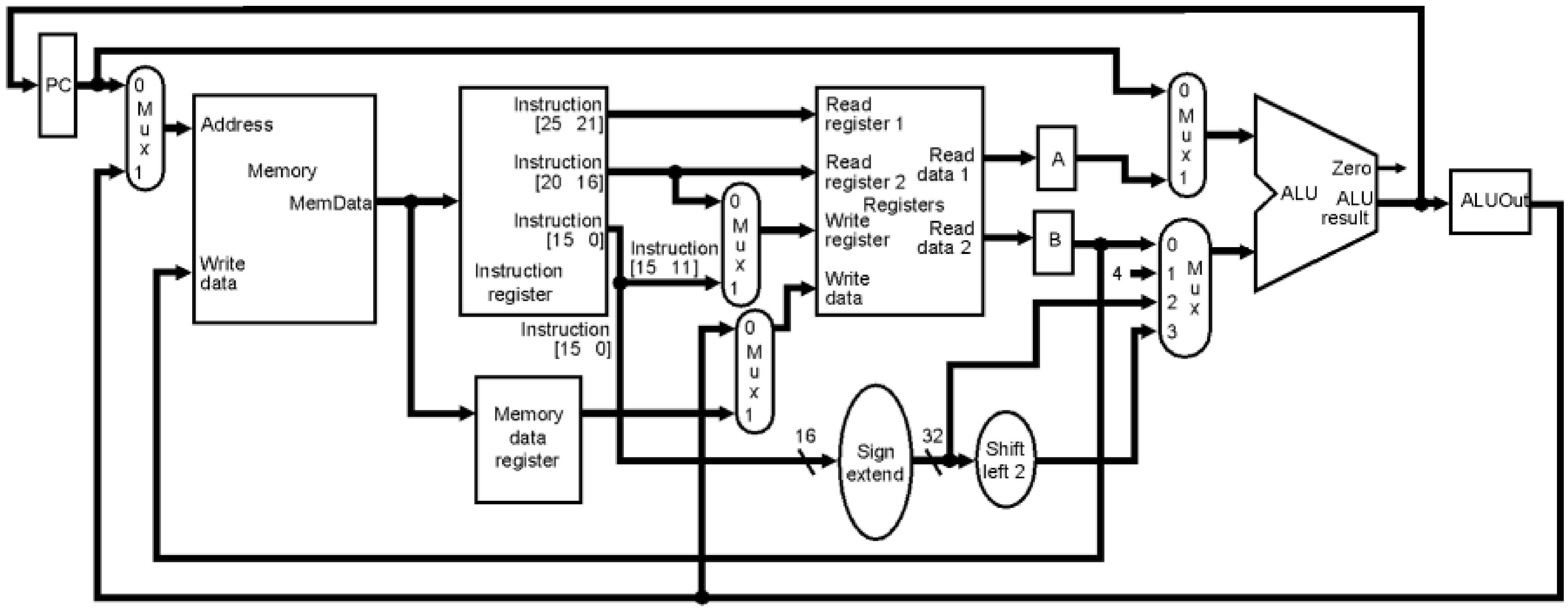

- **More Latches**
- **One ALU**
- **One Memory Unit**

## 1. Fetch

IR = Mem[PC]

PC = PC + 4

(*may not be final value of PC*)

## 2. Instruction Decode and Register Fetch

A = Reg[IR[25-21]]

B = Reg[IR[20-16]]

ALUOut = PC + (sign-extend (IR[15-0]) << 2)

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- *ALUOut is a new state element (temp register)*

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- *ALUOut is a new state element (temp register)*
- *everything up to this point must be Instruction-independent, because we still haven't decoded the instruction.*
- *everything instruction (opcode)-dependent from here on.*

## 3. Execution, Memory Address Computation, or Branch Completion

- Memory reference (load or store)
  - ALUOut = A + sign-extend(IR[15-0])
- R-type
  - ALUout = A op B
- Branch
  - if (A == B)  PC = ALUOut

*At this point, Branch is complete, and we start over; others require more cycles.*

## 4. Memory access or R-type completion

- Memory reference (load or store)
  - Load
    - MDR = Mem[ALUout]
  - Store
    - Mem[ALUout] = B
- R-type
  - Reg[IR[15-11]] = ALUout

*R-type is complete, store is complete.*

## 5. Memory Write-Back

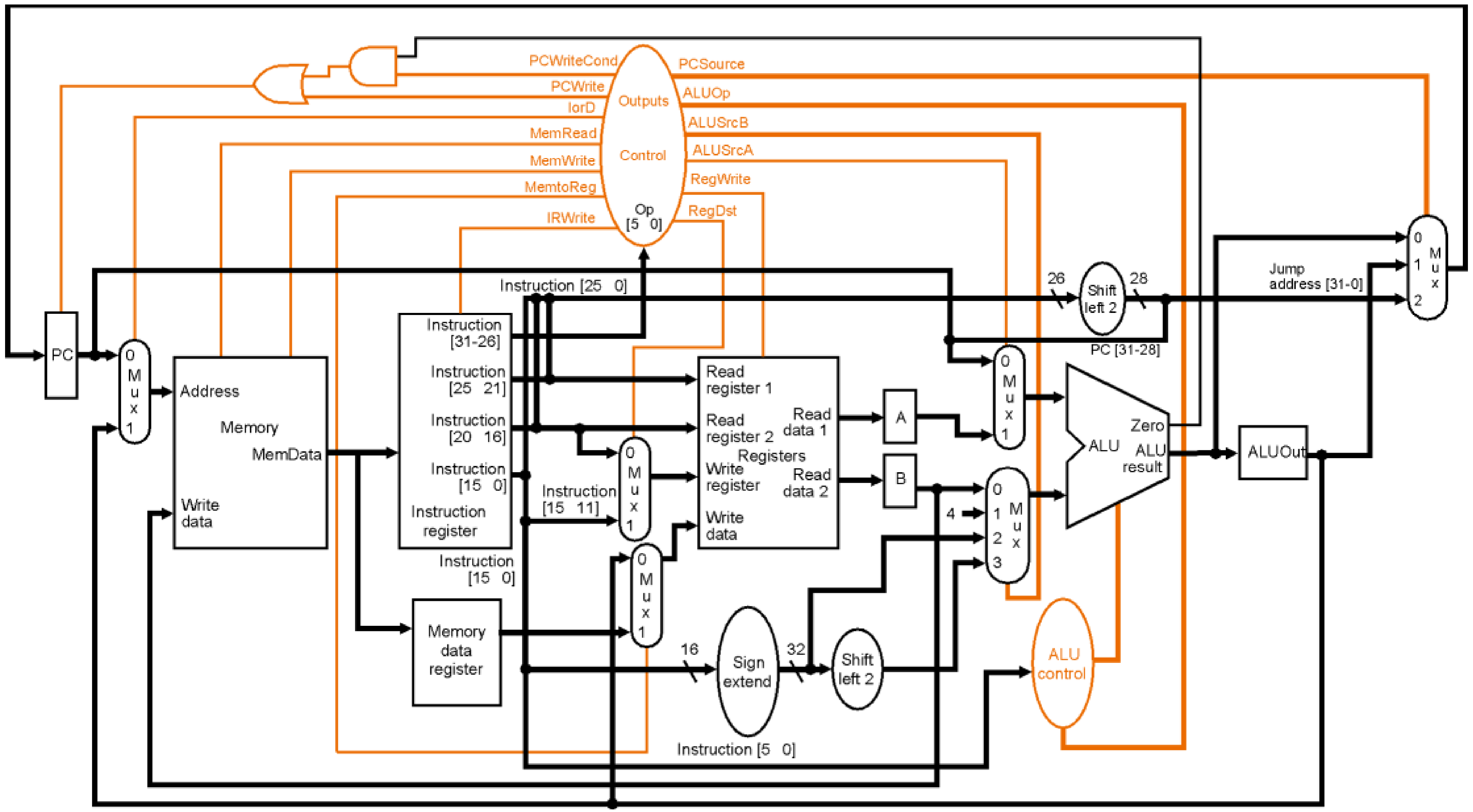
Reg[IR[20-16]] = MDR

*load is complete*

## Summary of Execution Steps

| Step | R-type | Memory | Branch |
|---|---|---|---|
| Instruction Fetch | IR = Mem[PC]<br>PC = PC + 4 | | |
| Instruction Decode/ register fetch | A = Reg[IR[25-21]]<br>B = Reg[IR[20-16]]<br>ALUout = PC + (sign-extend(IR[15-0]) << 2) | | |
| Execution, address computation, branch completion | ALUout = A op B | ALUout = A + sign-extend(IR[15-0]) | if (A==B) then PC=ALUout |
| Memory access or R-type completion | Reg[IR[15-11]] = ALUout | memory-data = Mem[ALUout]<br>*or*<br>Mem[ALUout]= B | |
| Write-back | | Reg[IR[20-16]] = memory-data | |

# Complete Multi-Cycle Datapath



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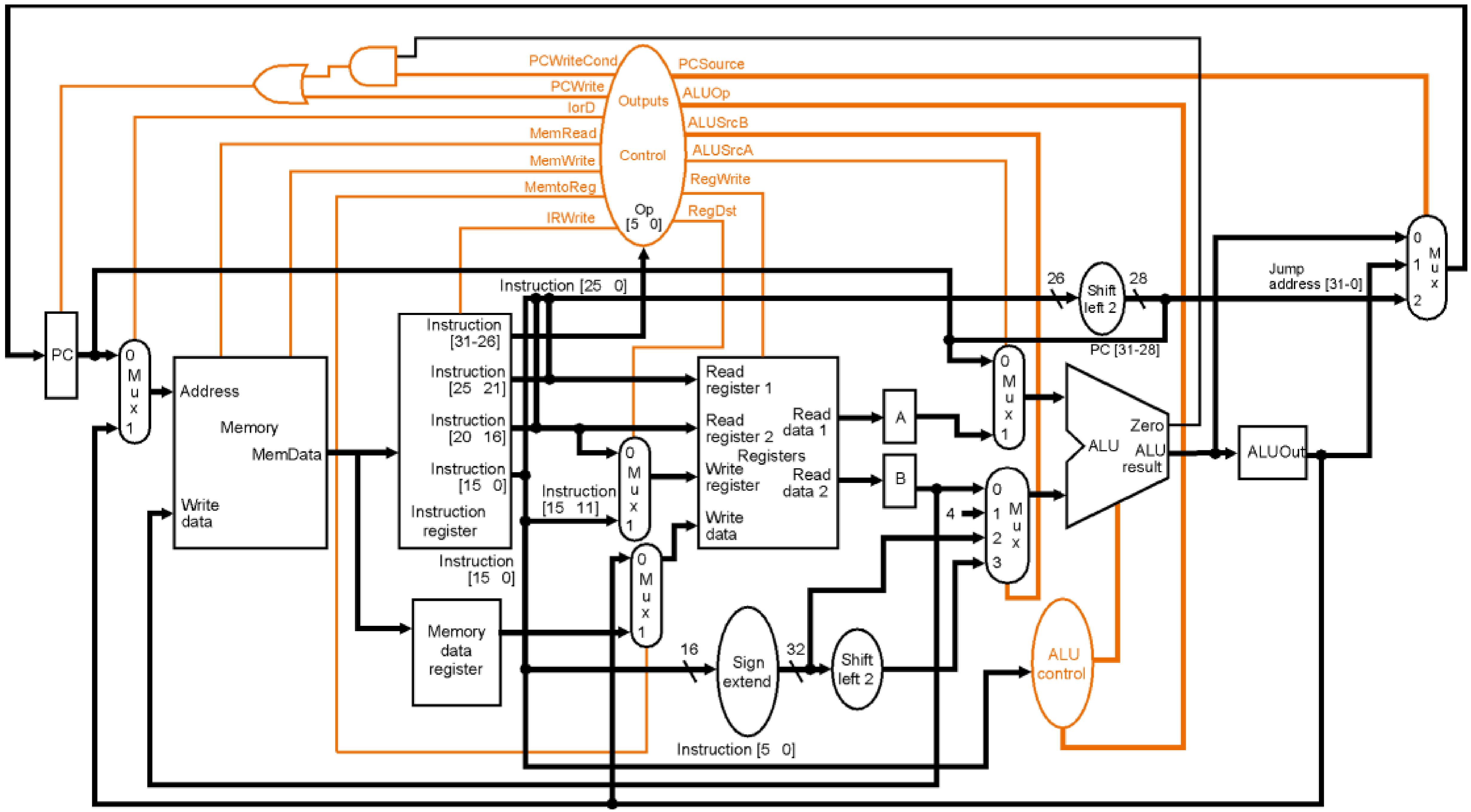

New Instruction Appears Out of Nowhere? Which One?

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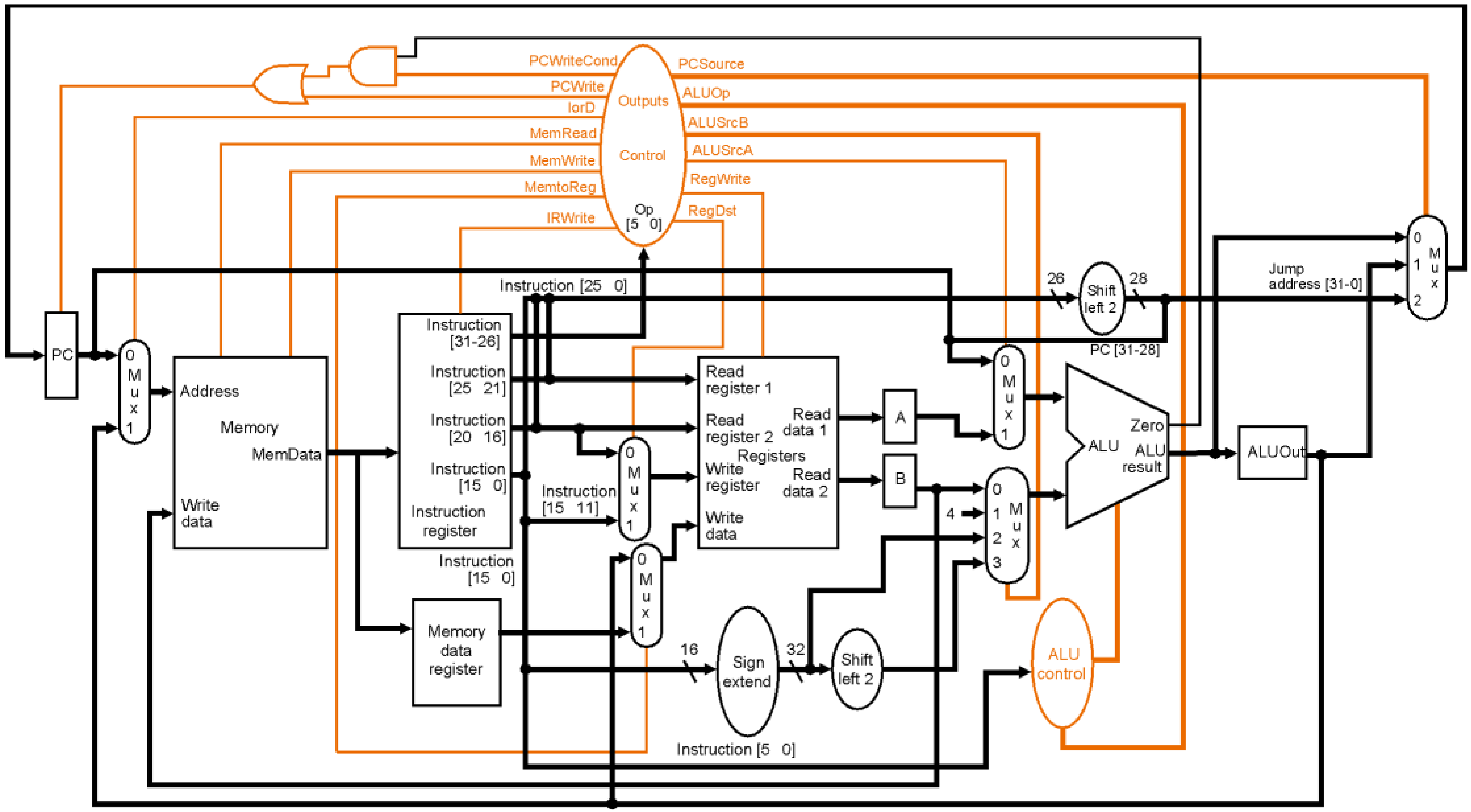

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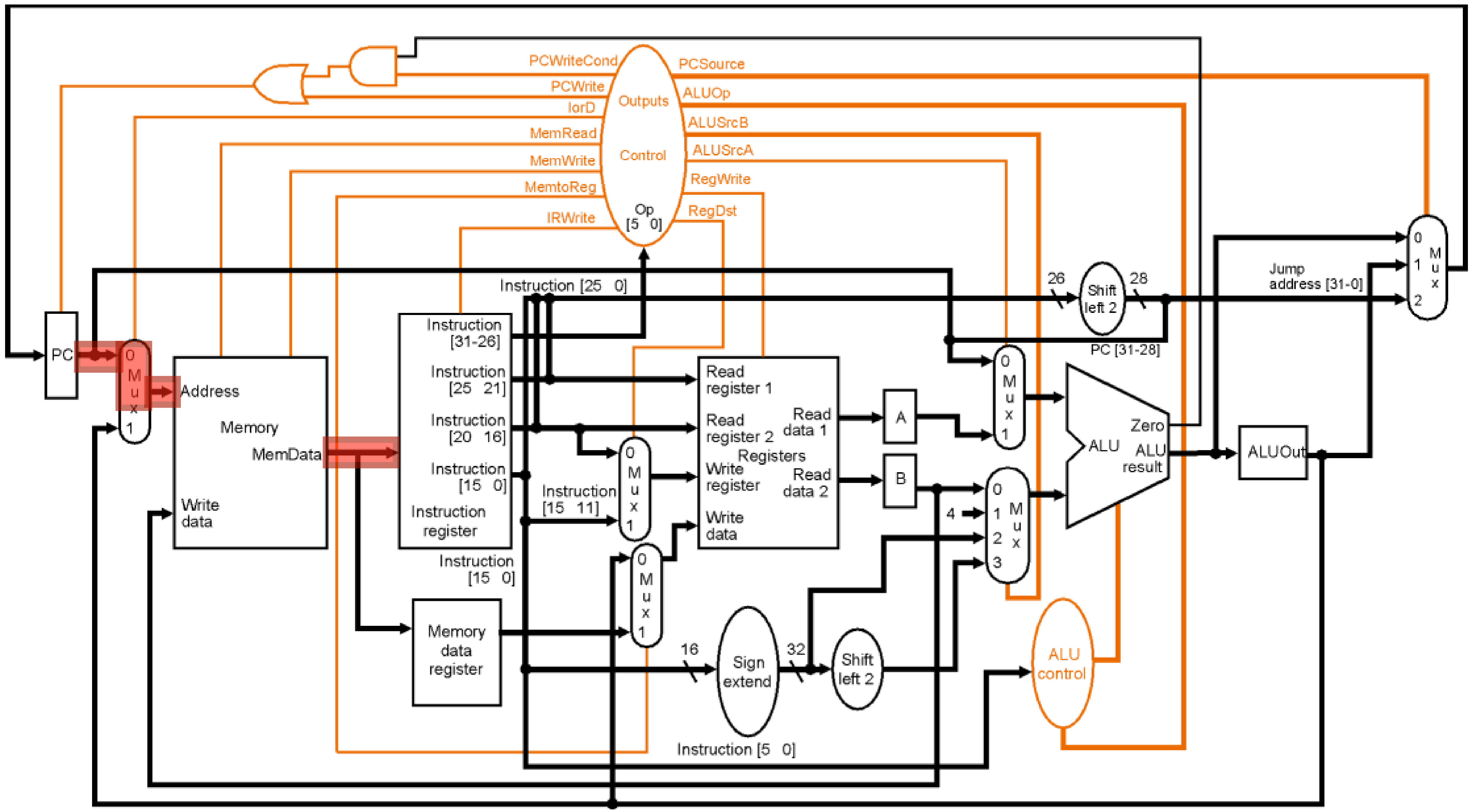

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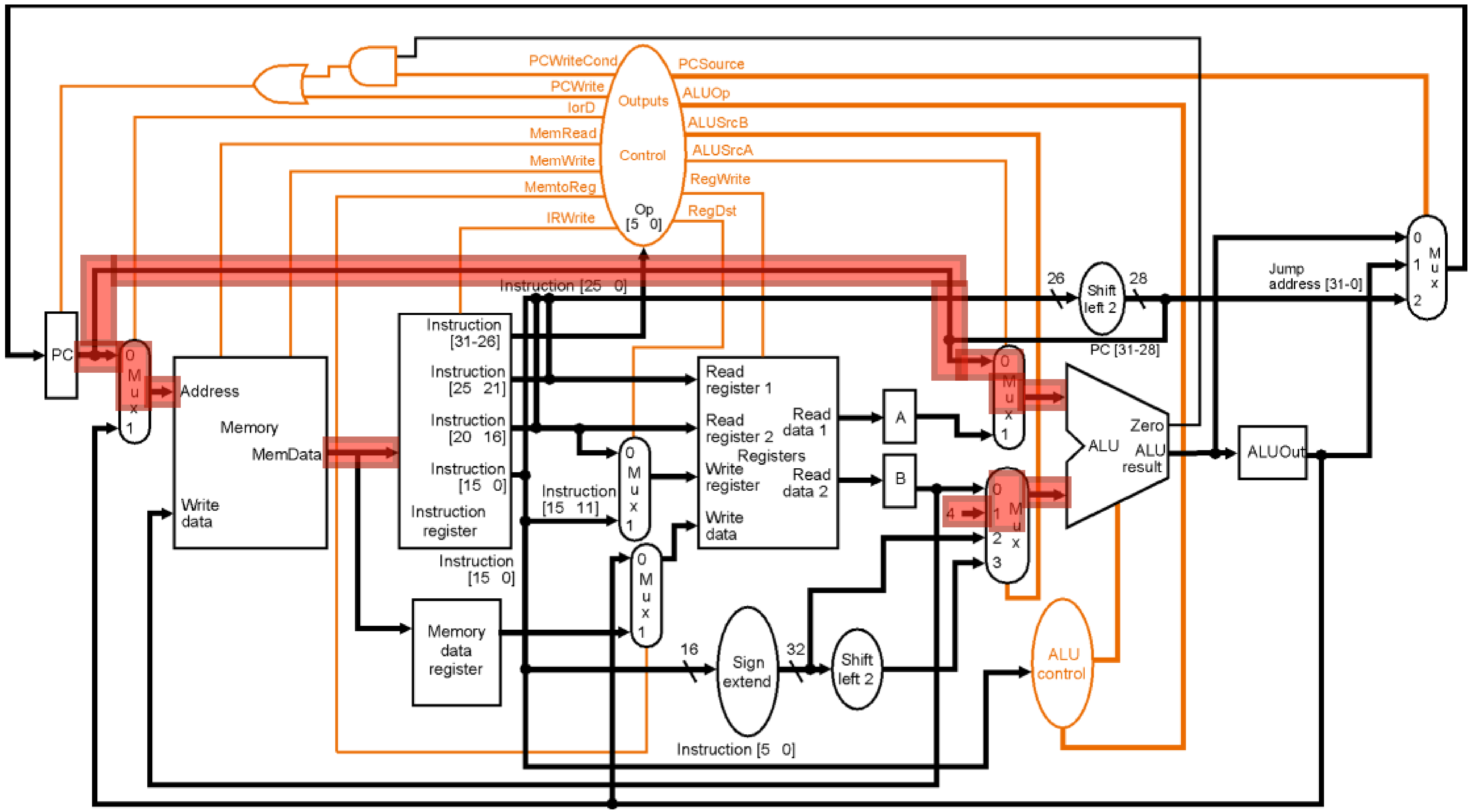

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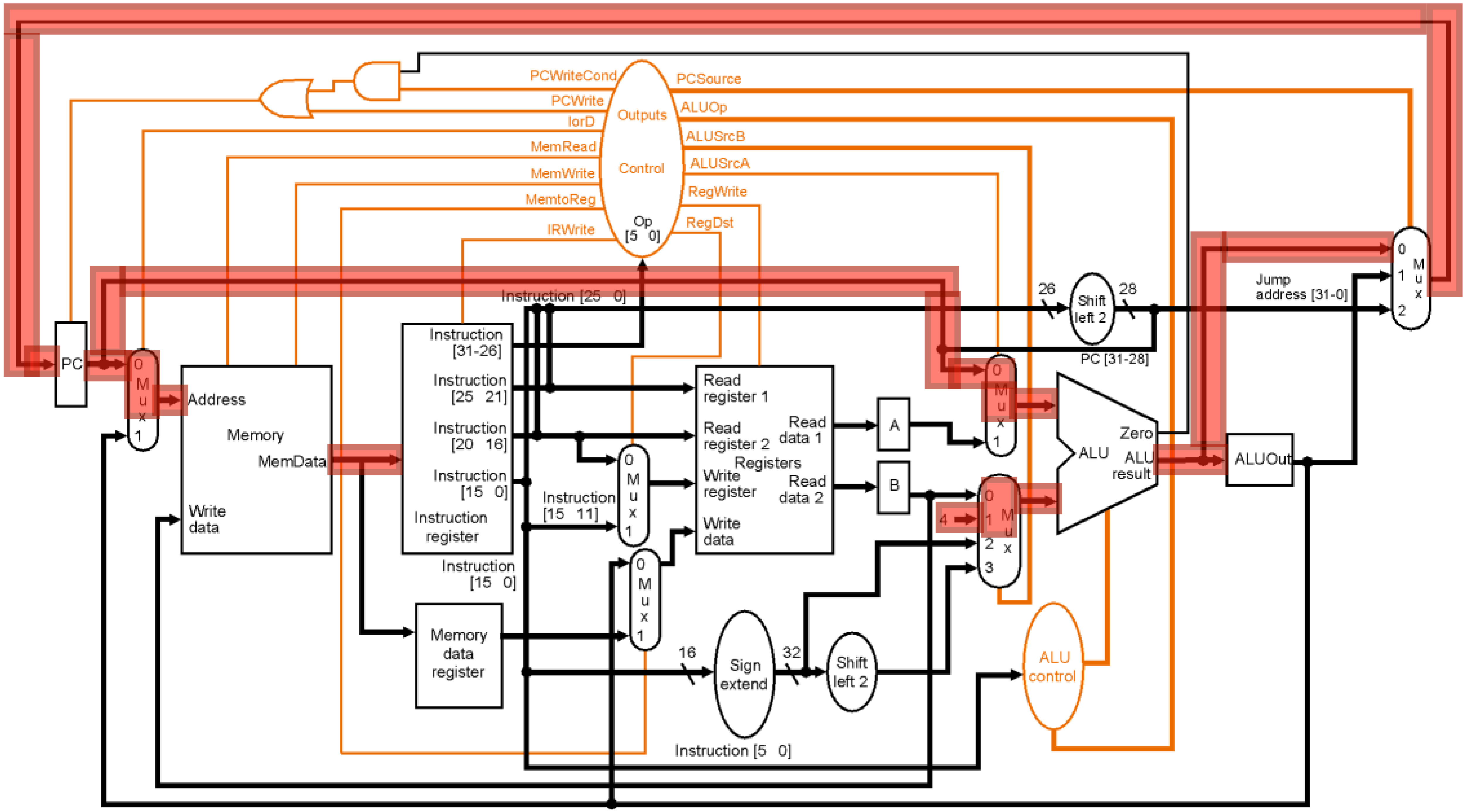

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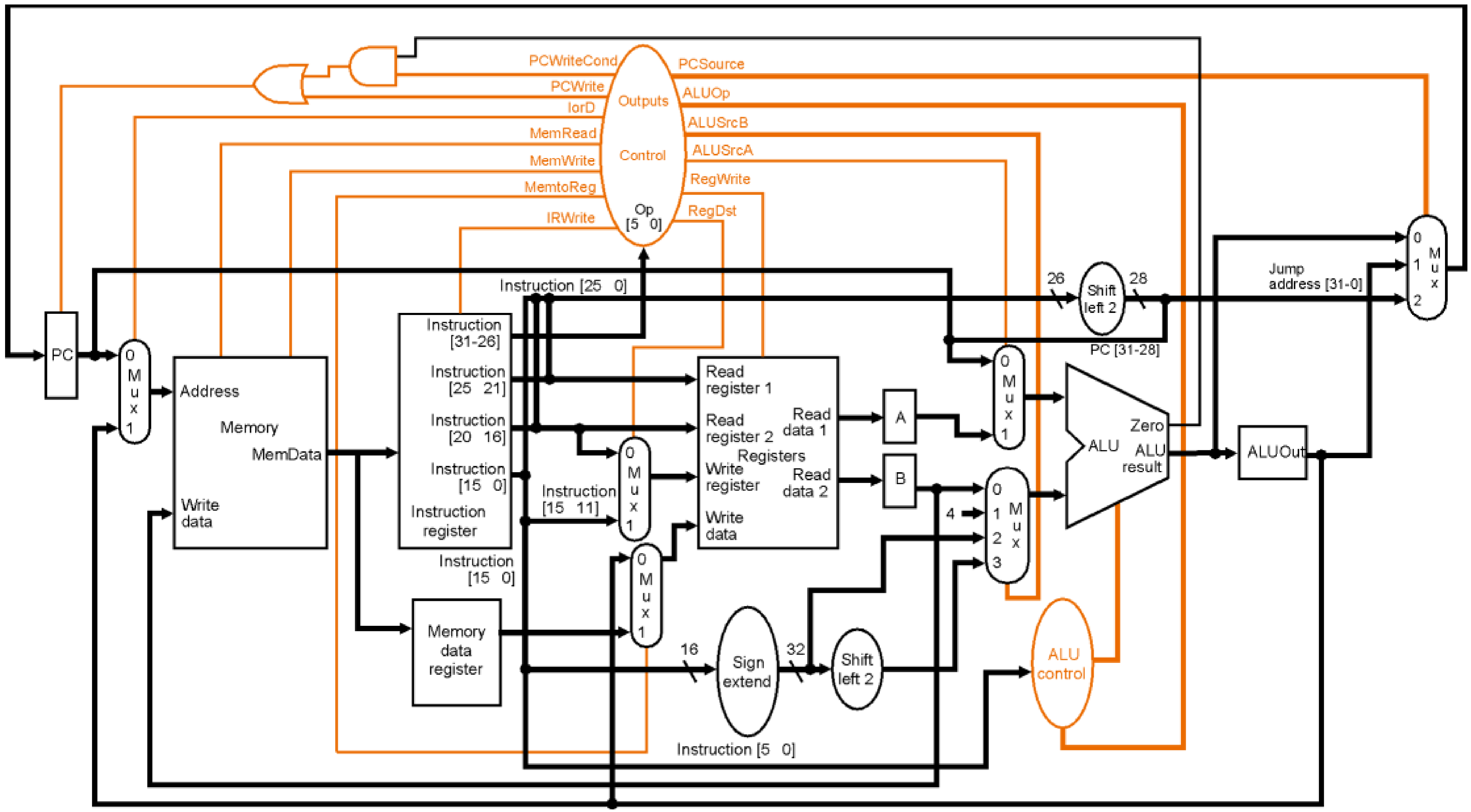

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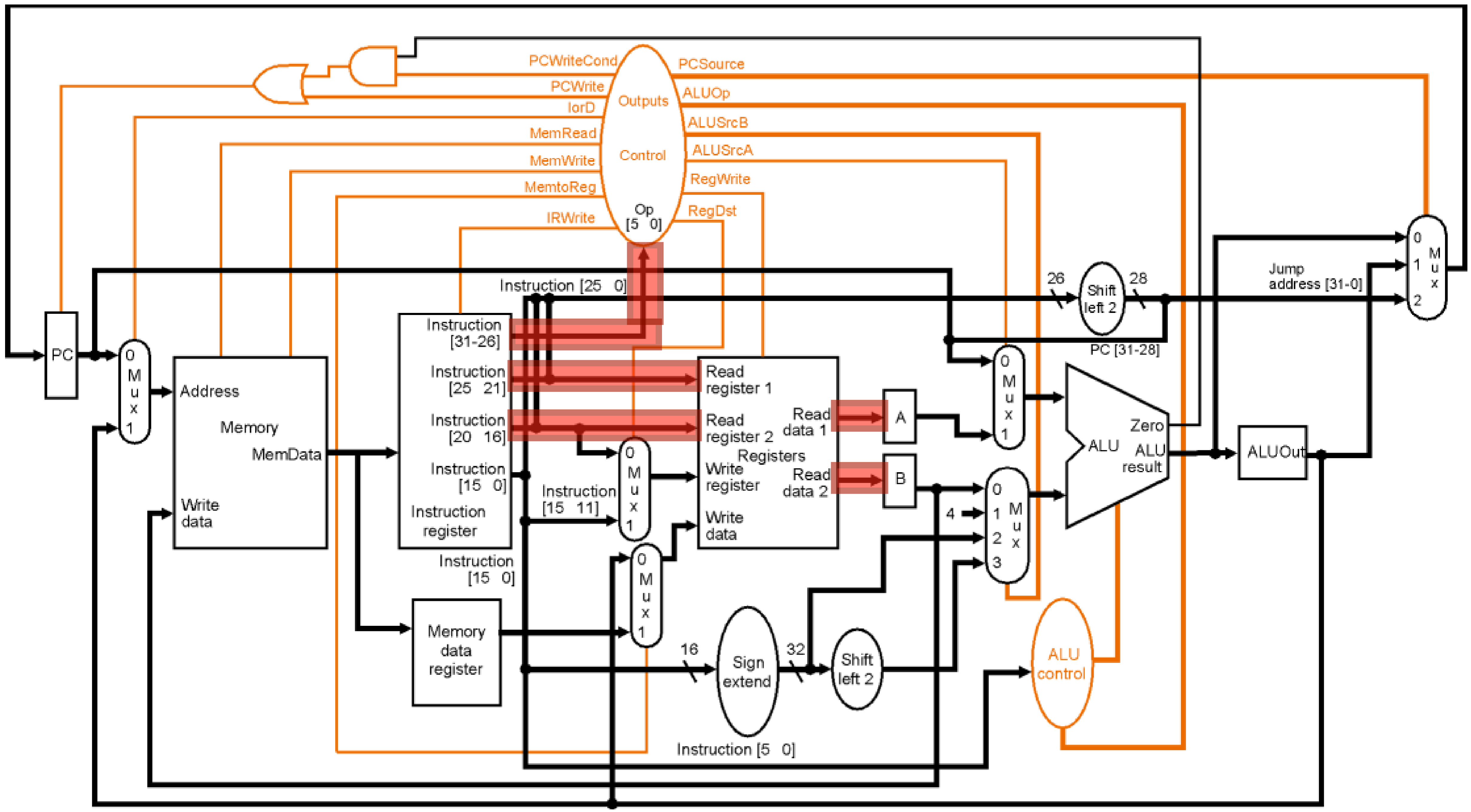

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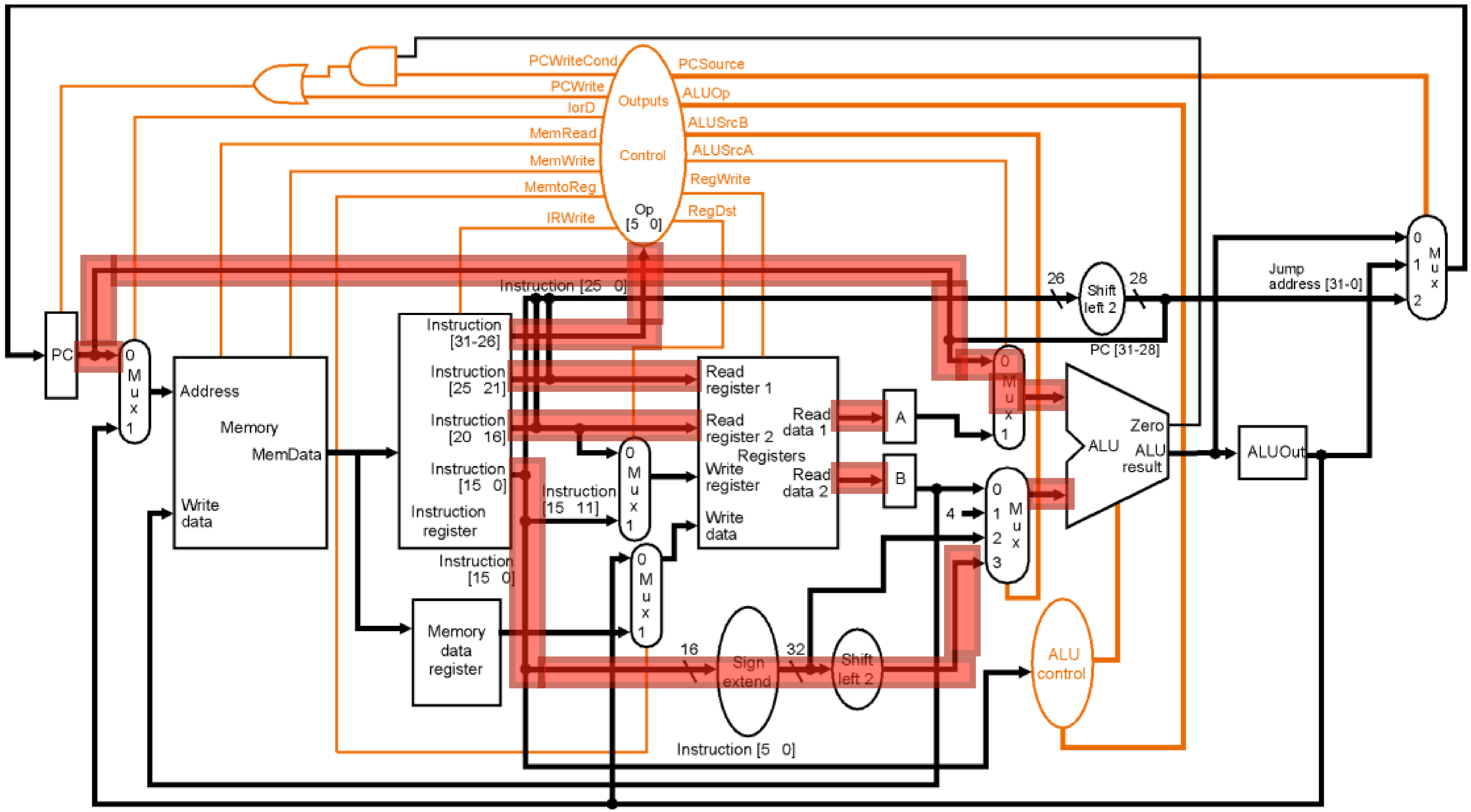

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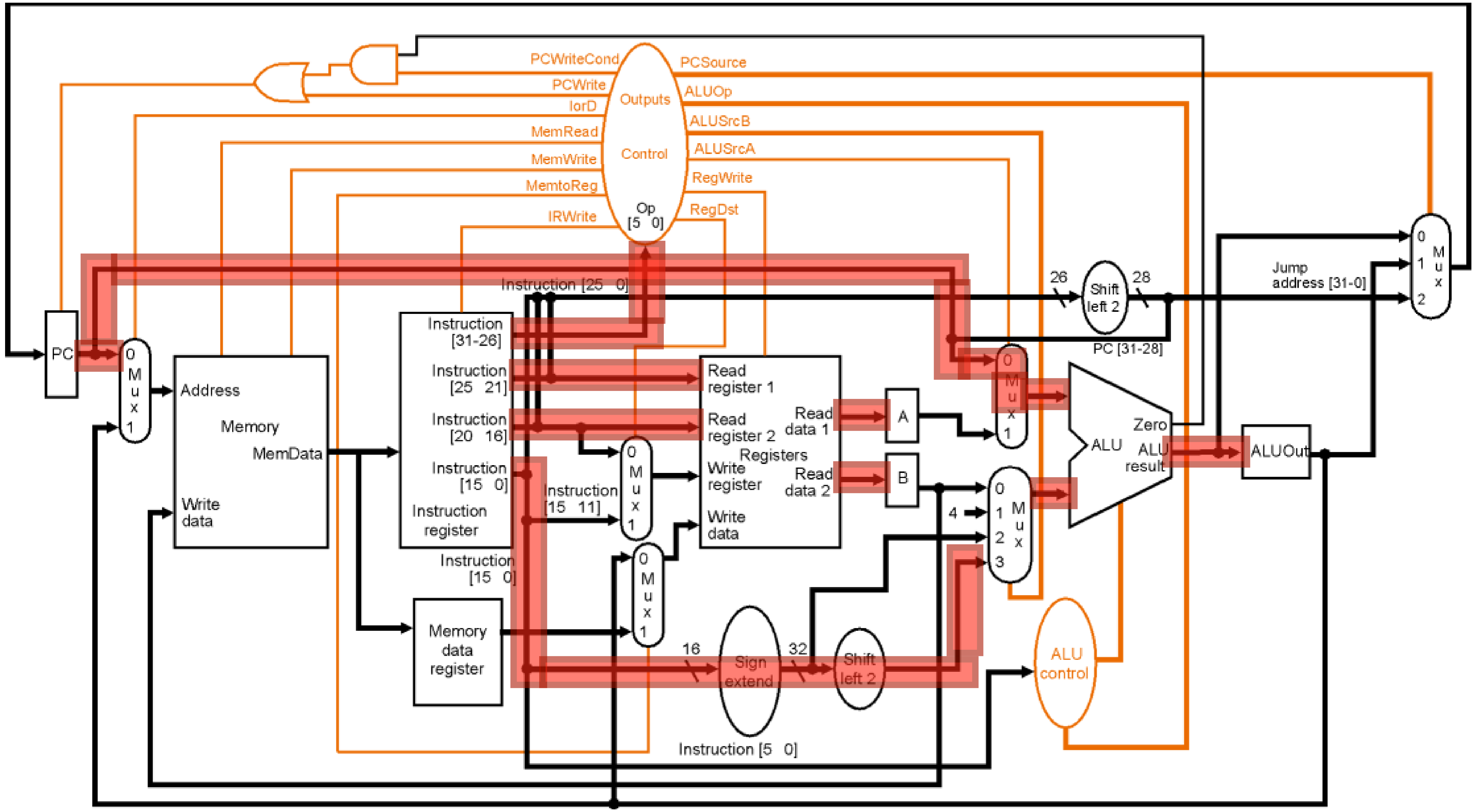

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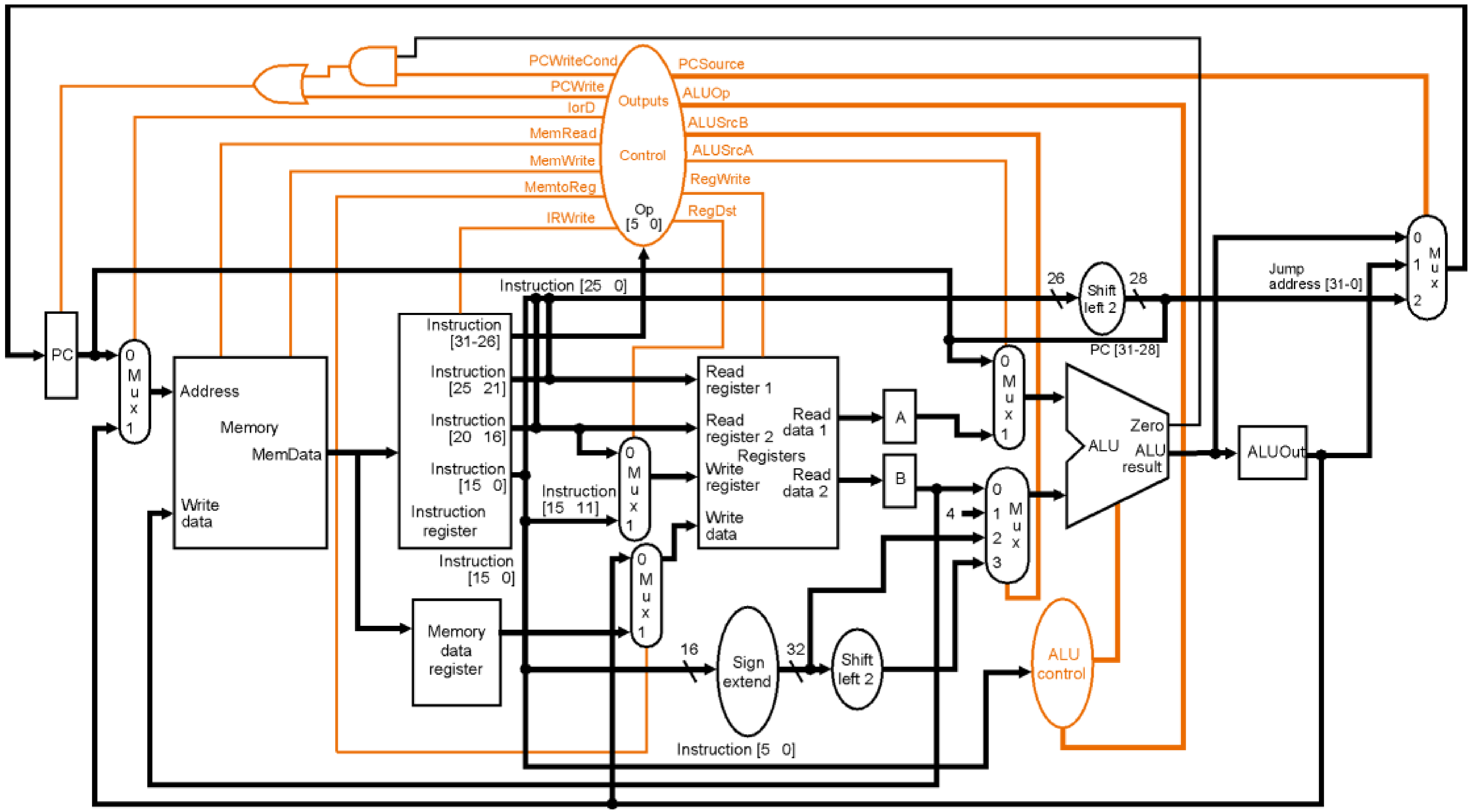

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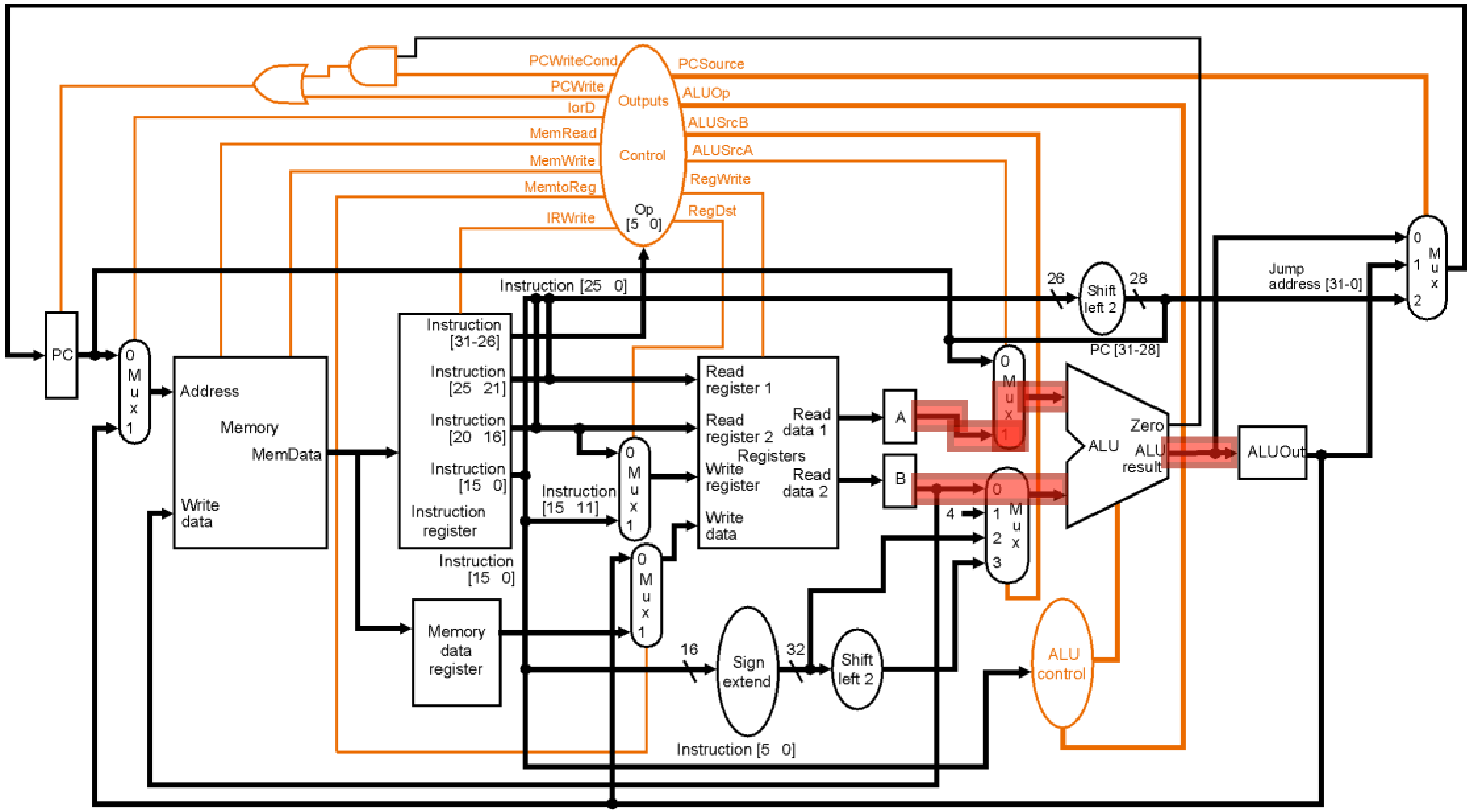

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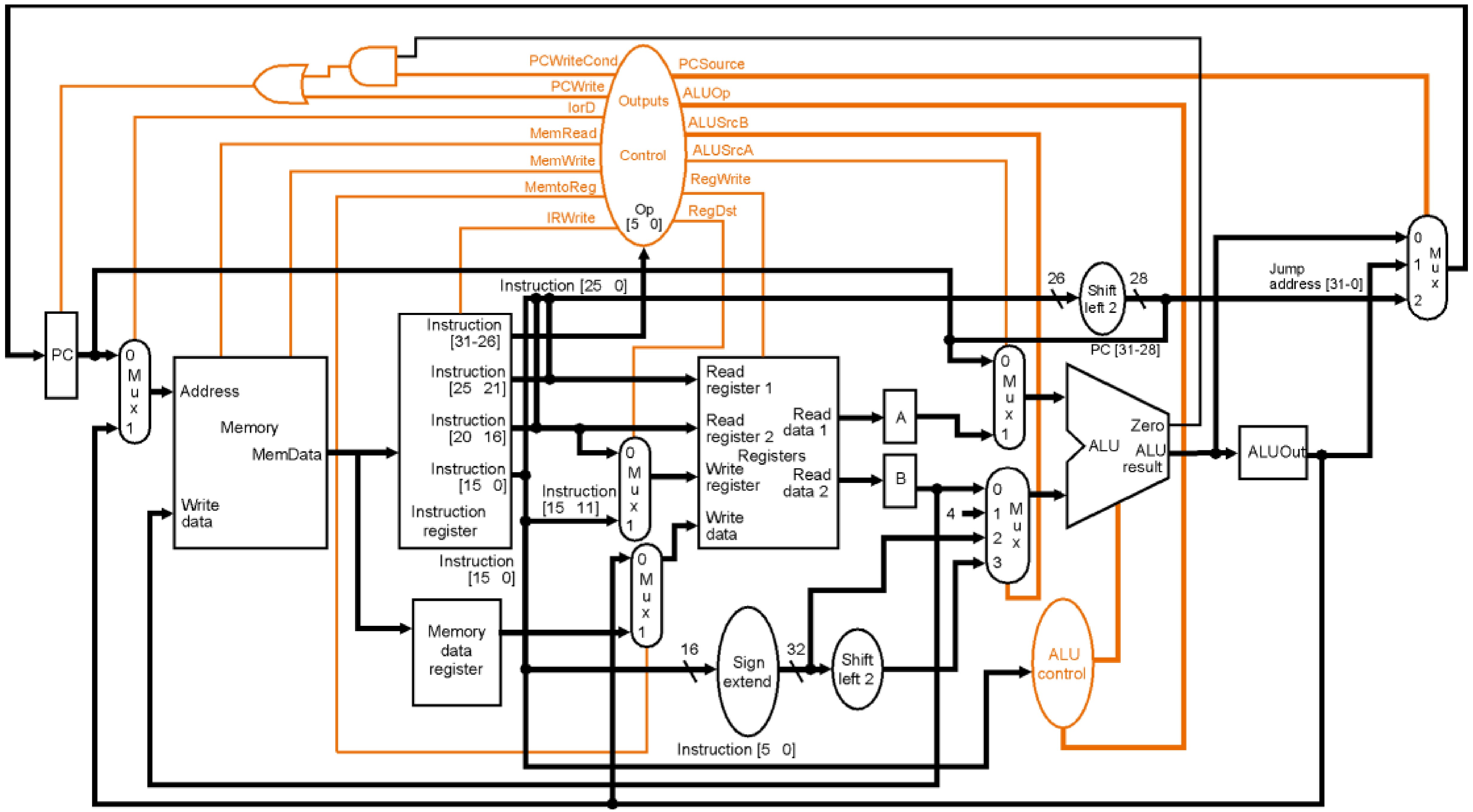

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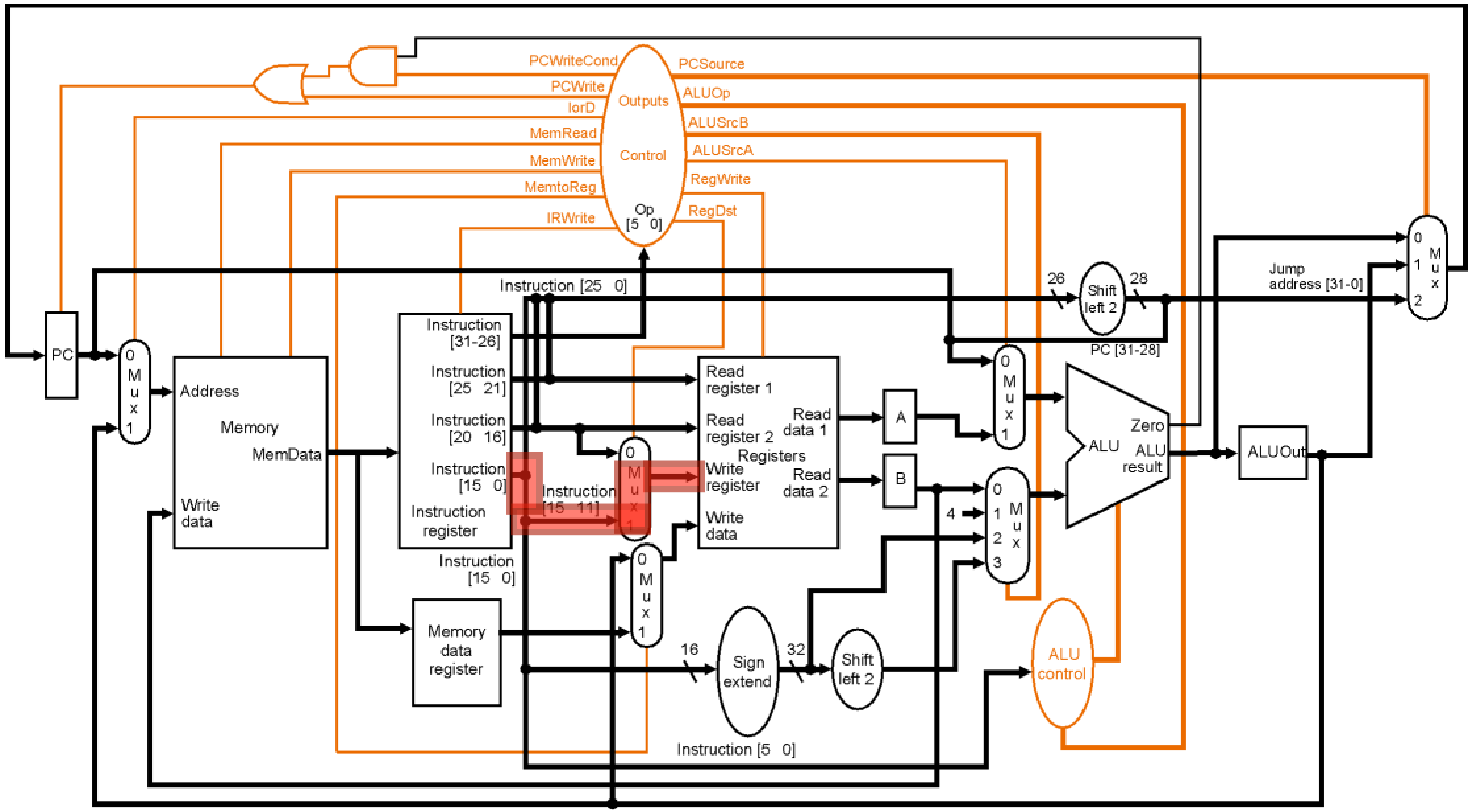

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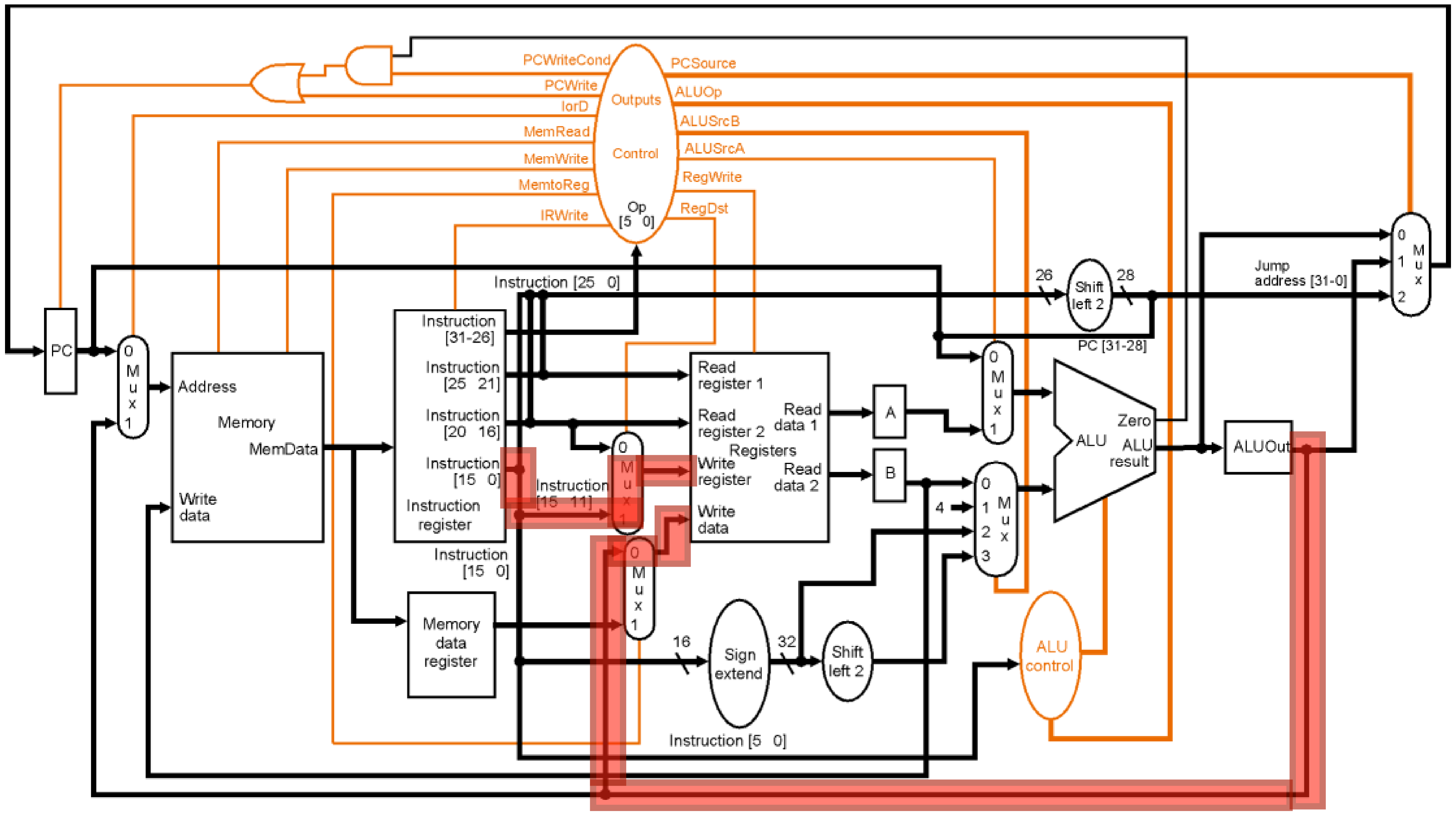

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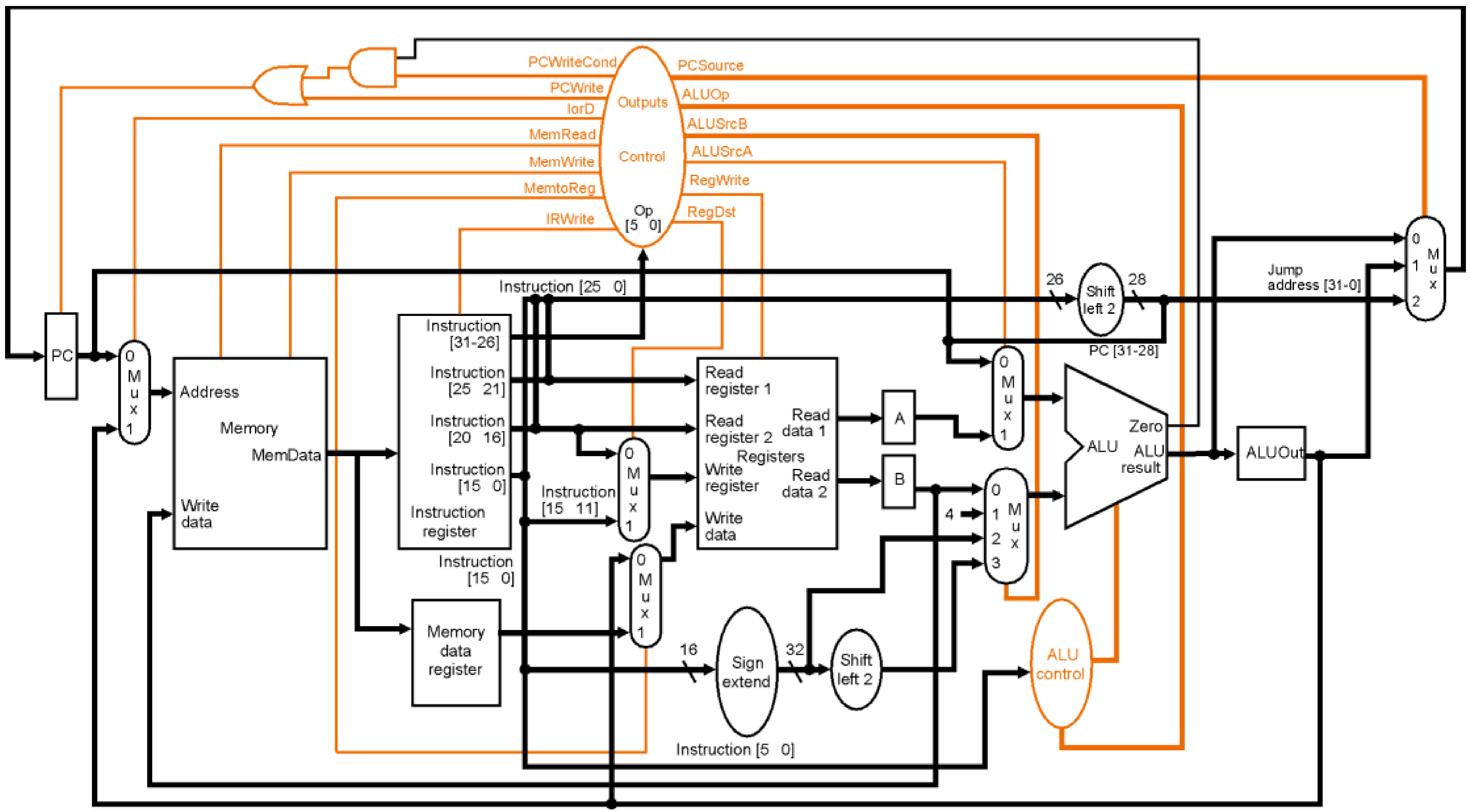

**if (A == B) PC = ALUOut**

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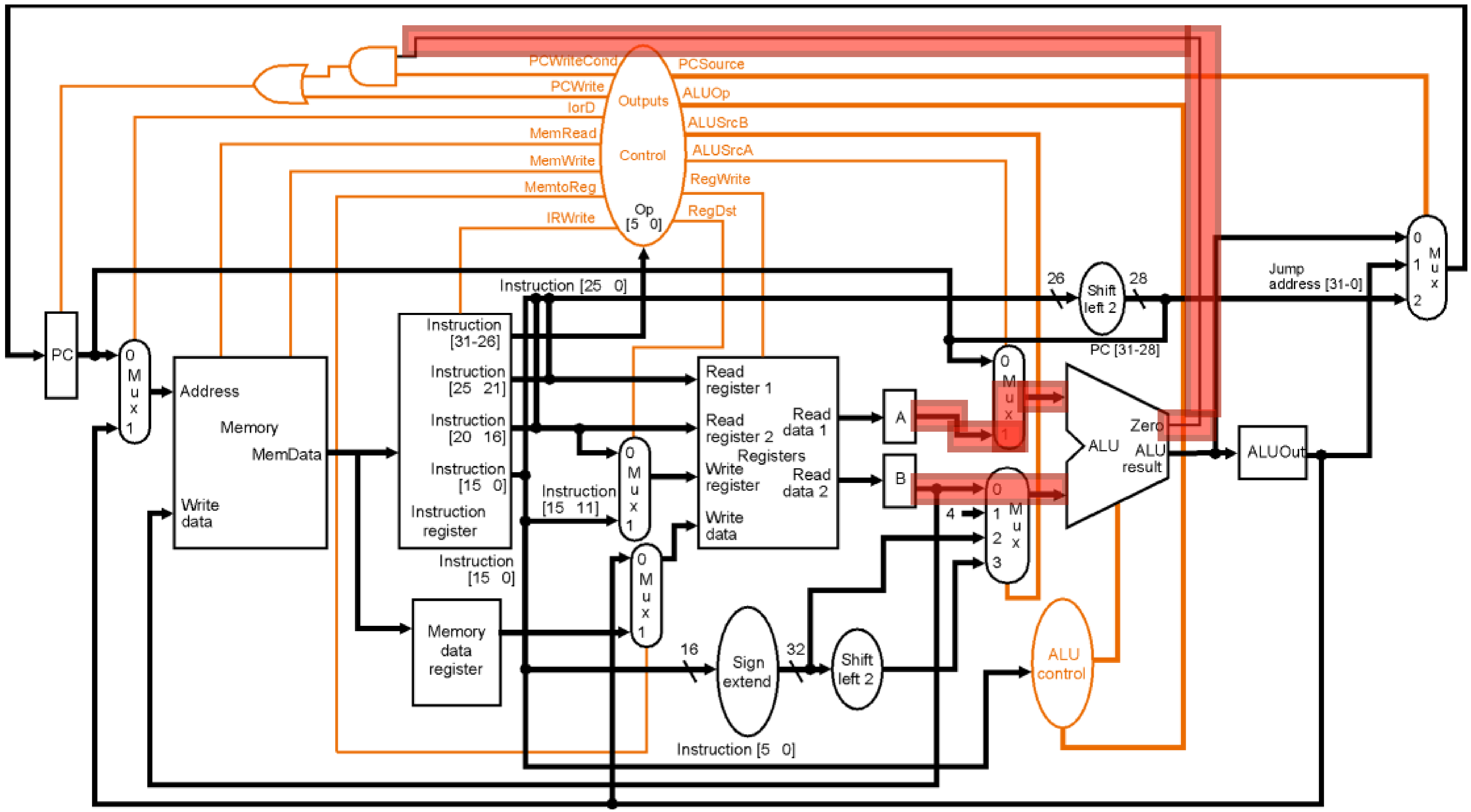

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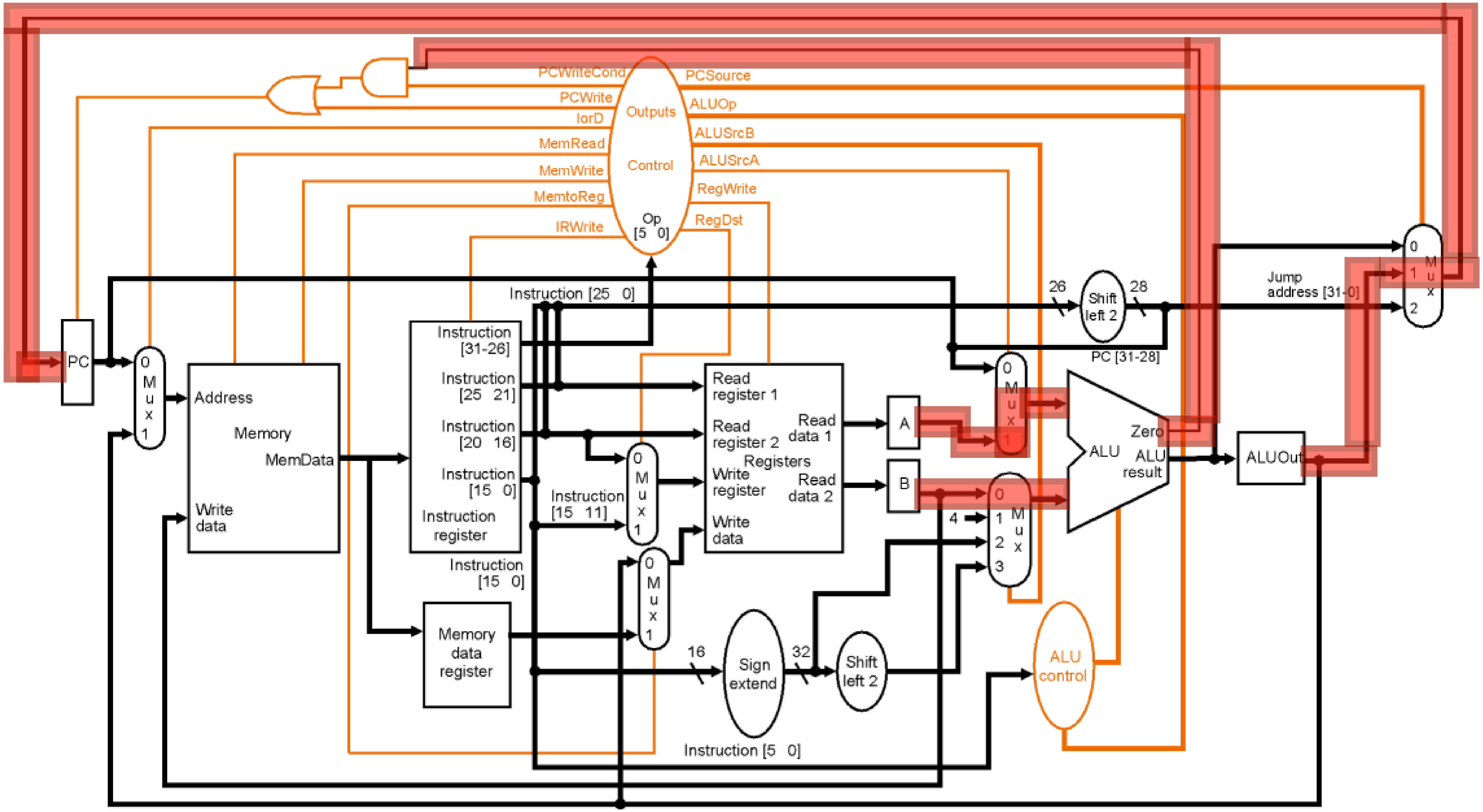

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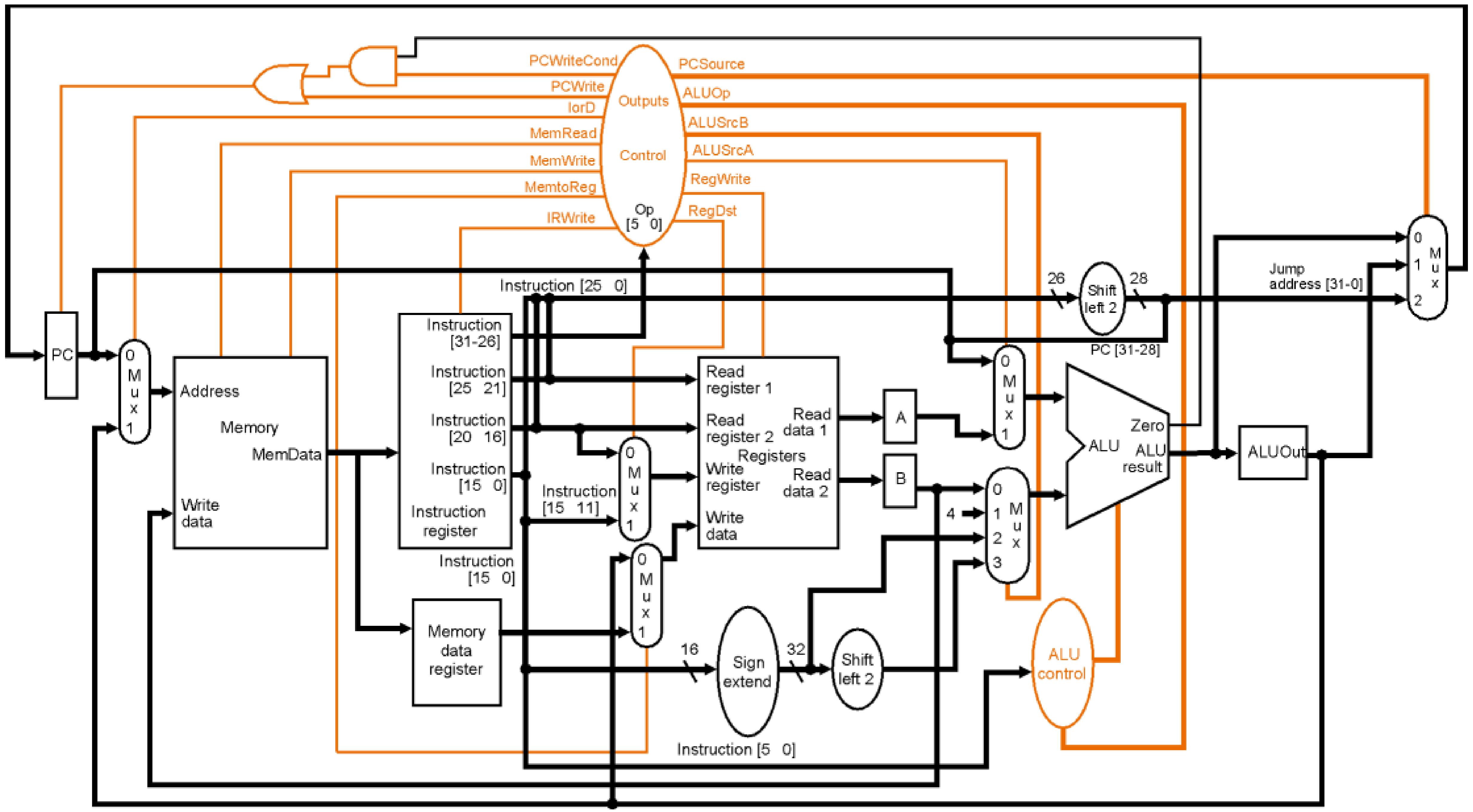

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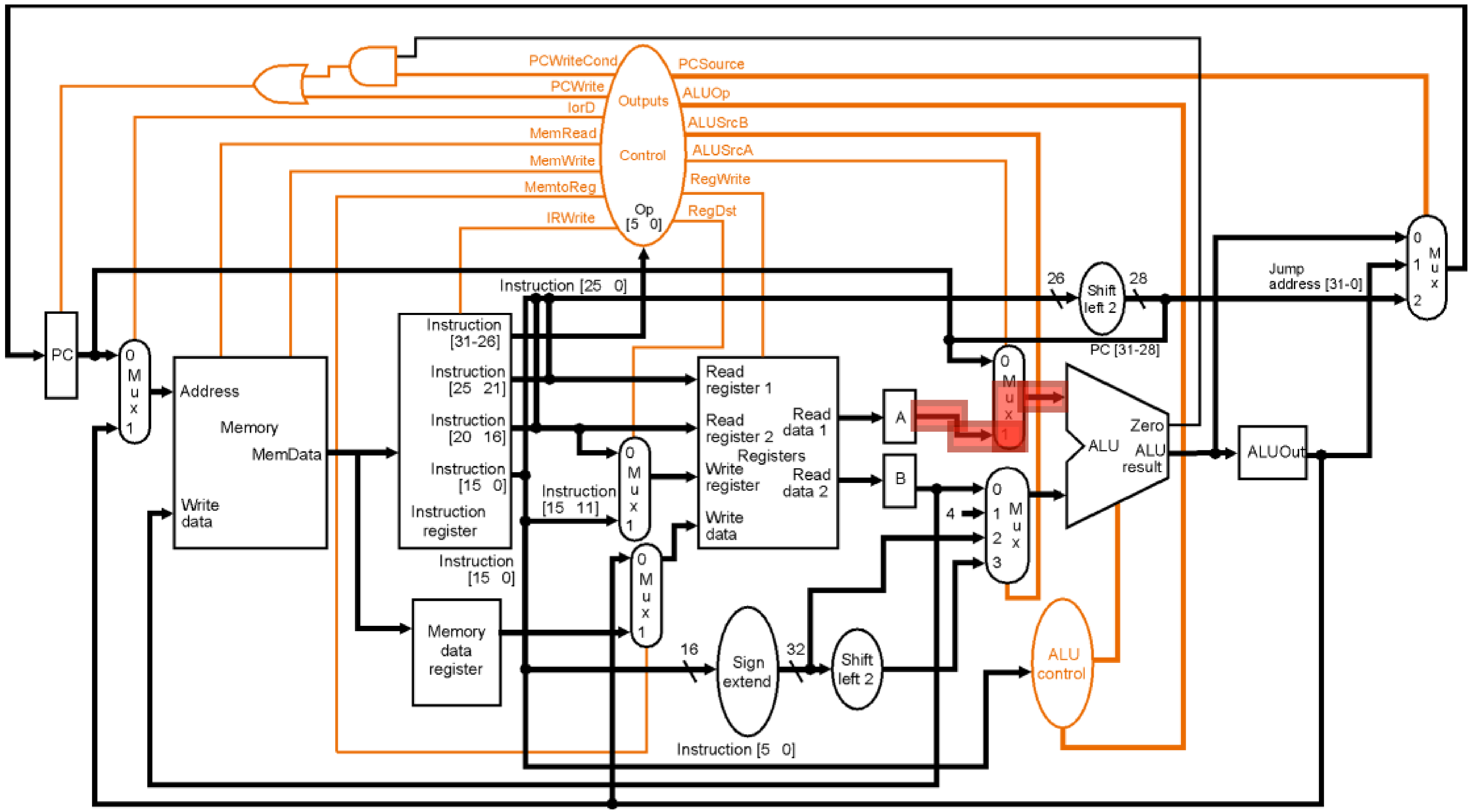

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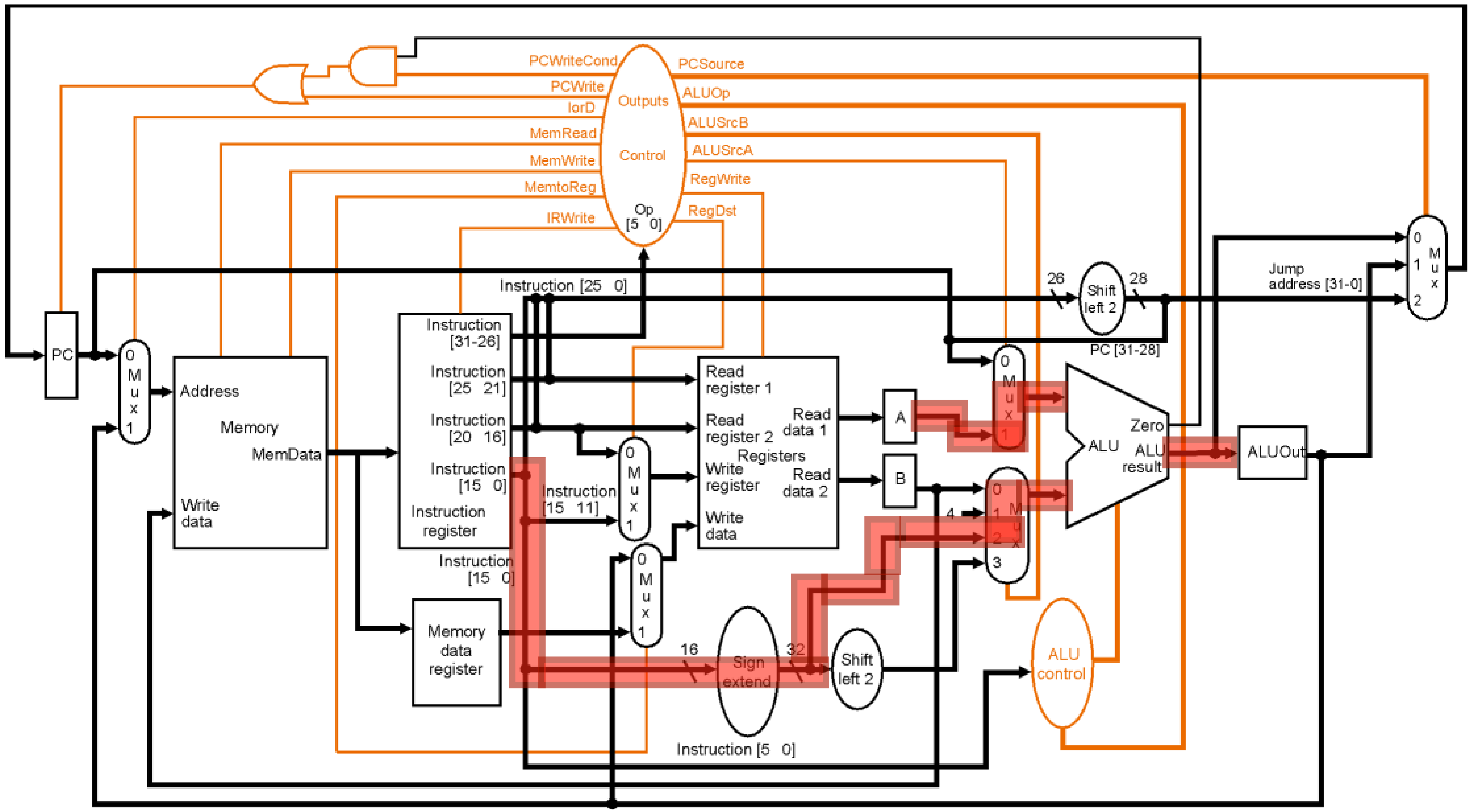

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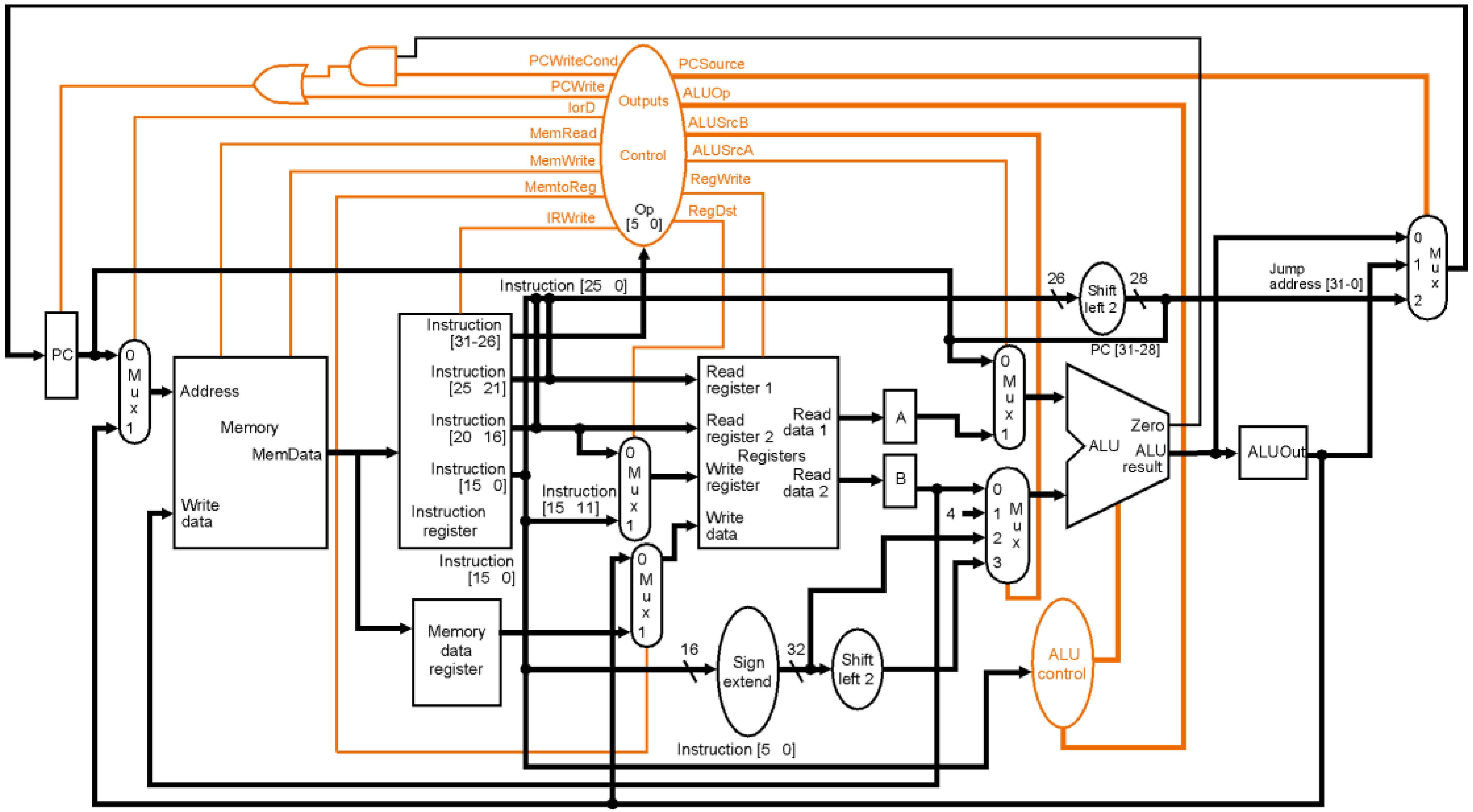

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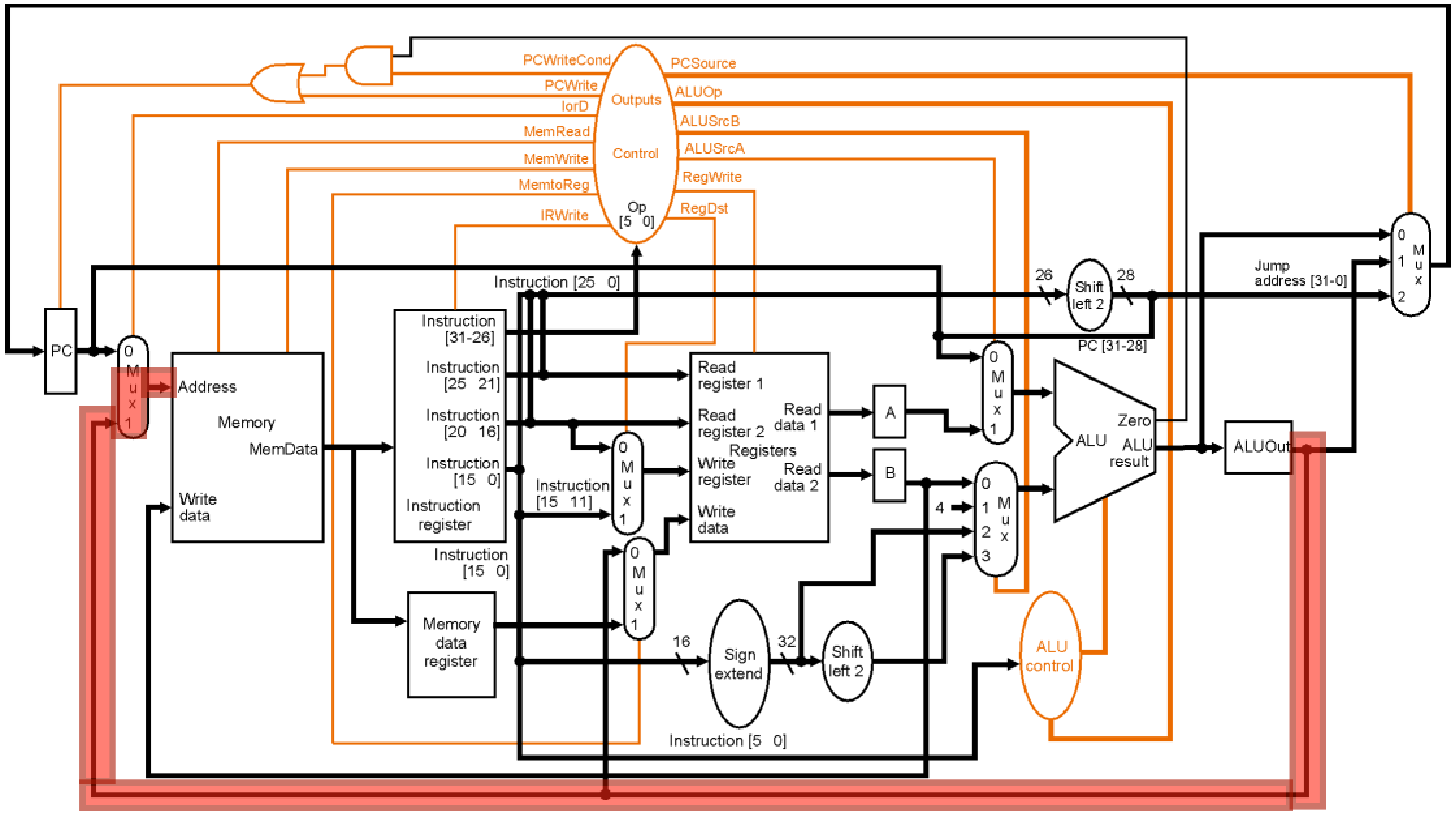

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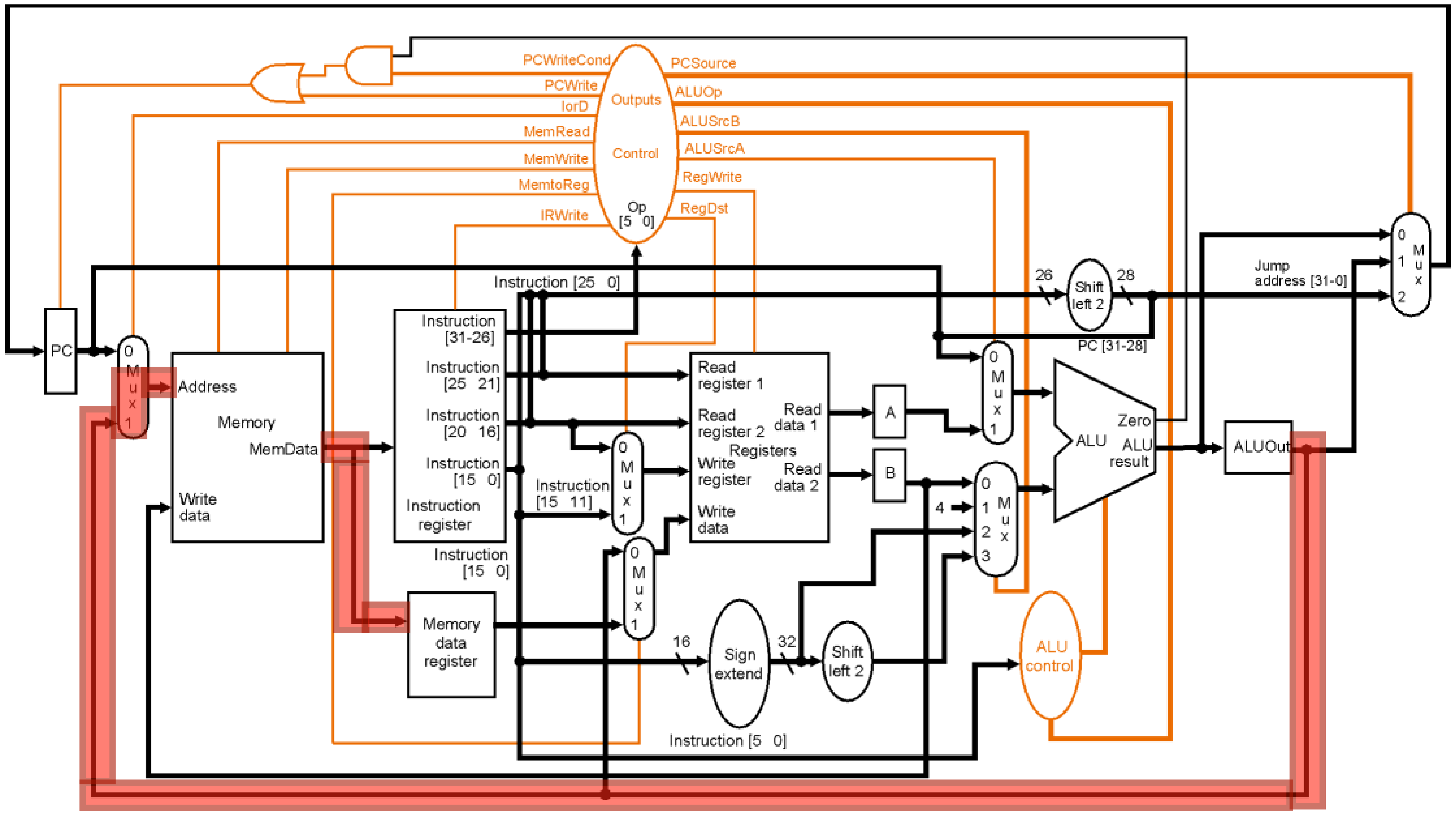

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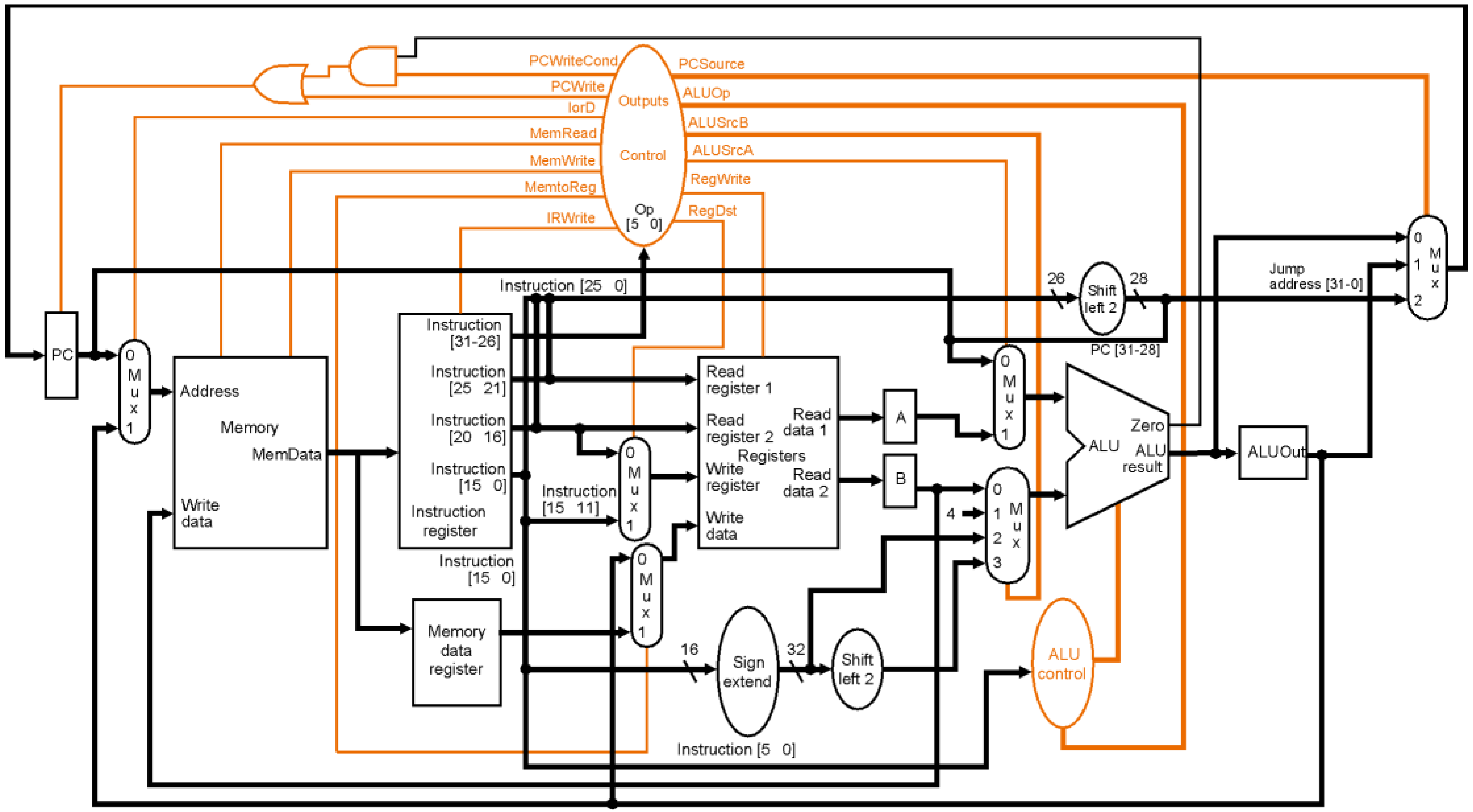

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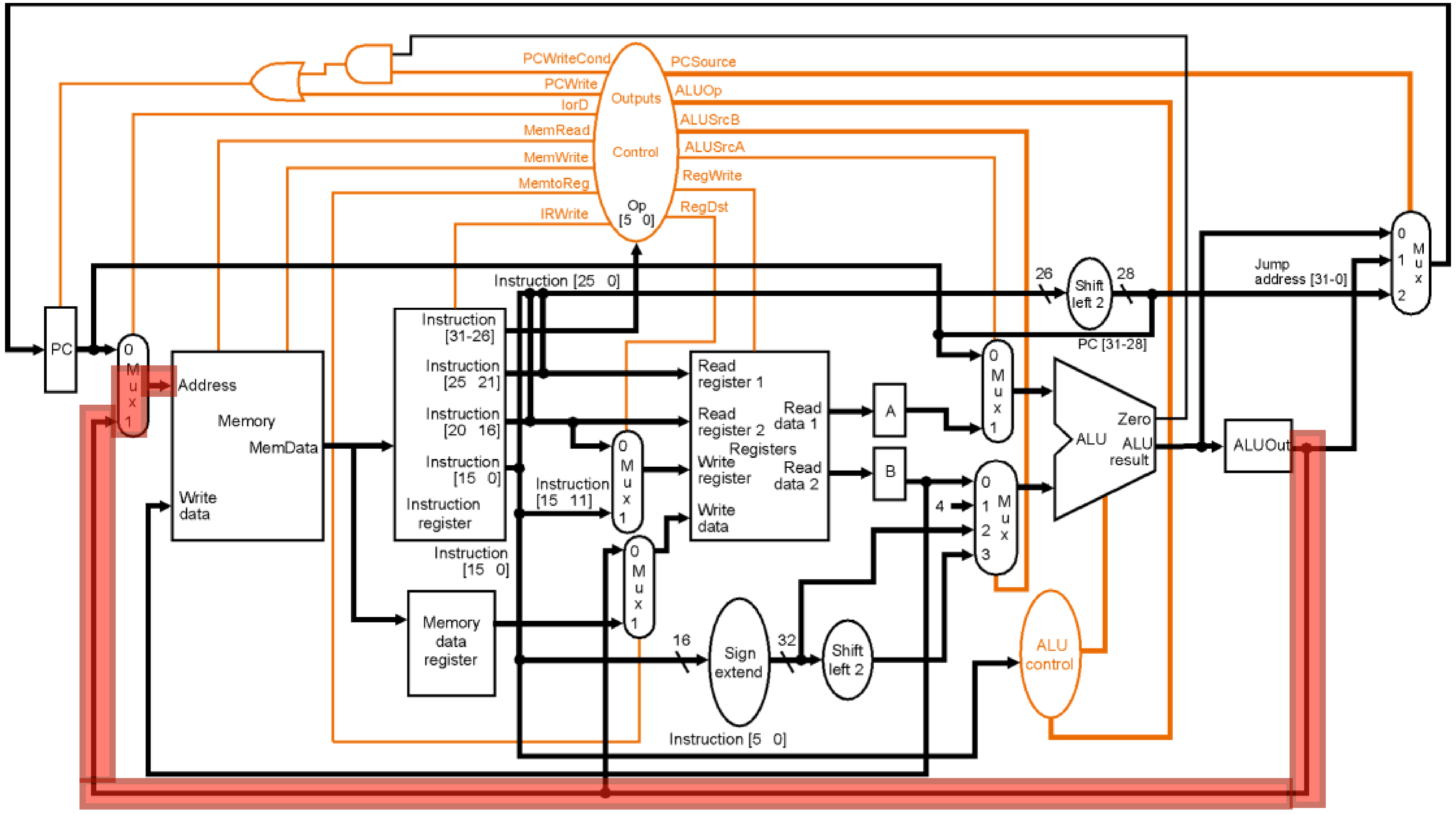

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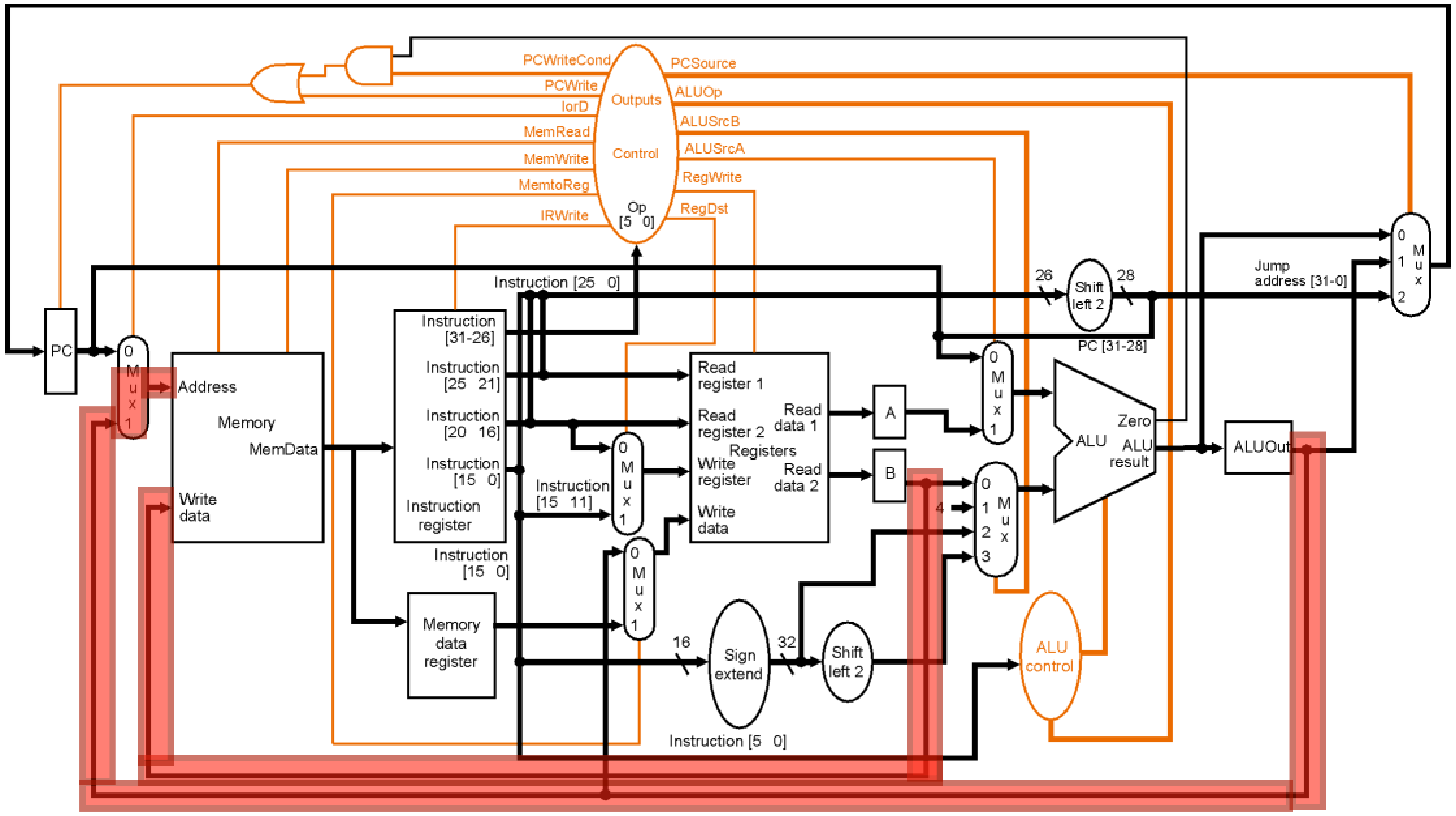

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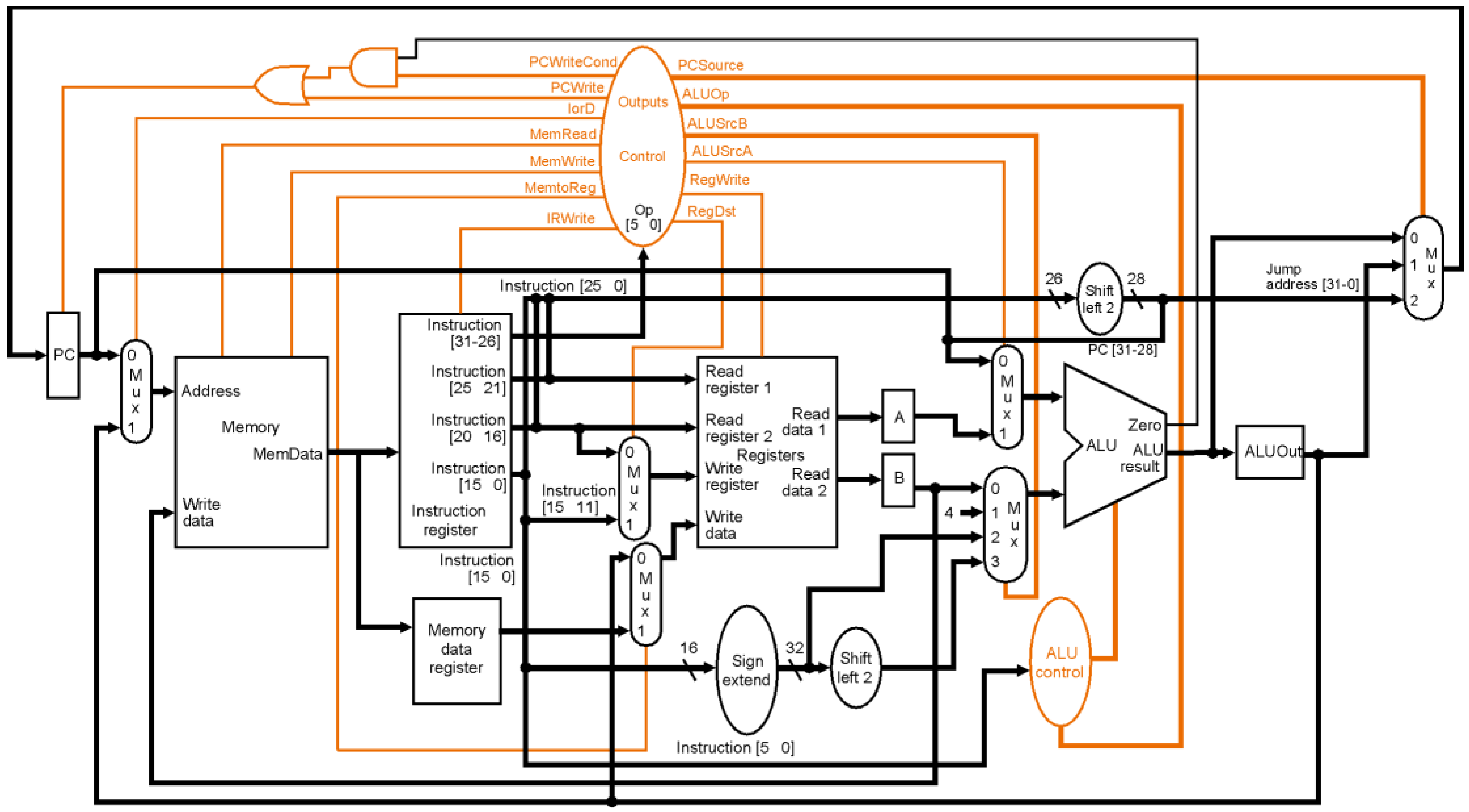

**Reg[IR[20-16]] = memory-data**

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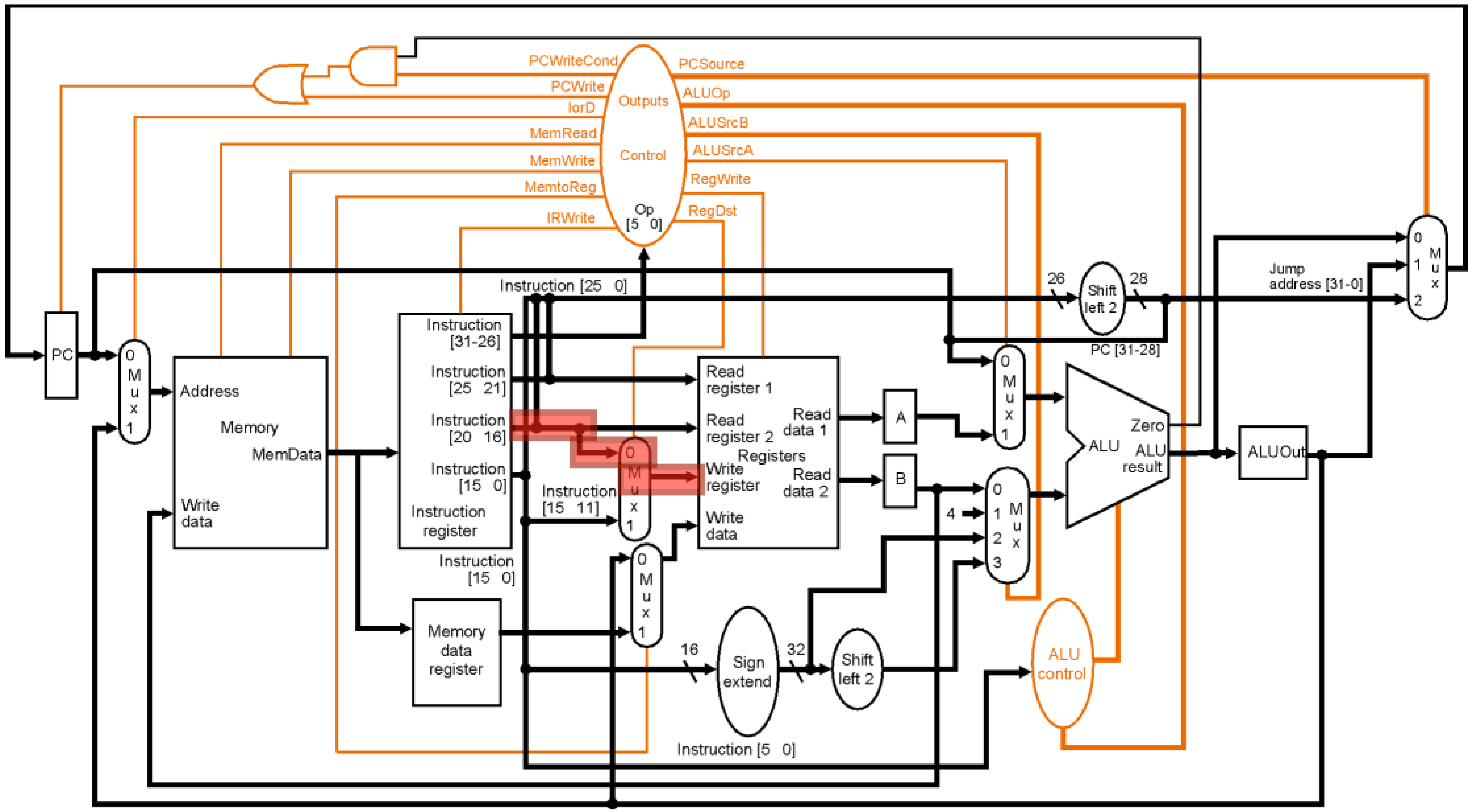

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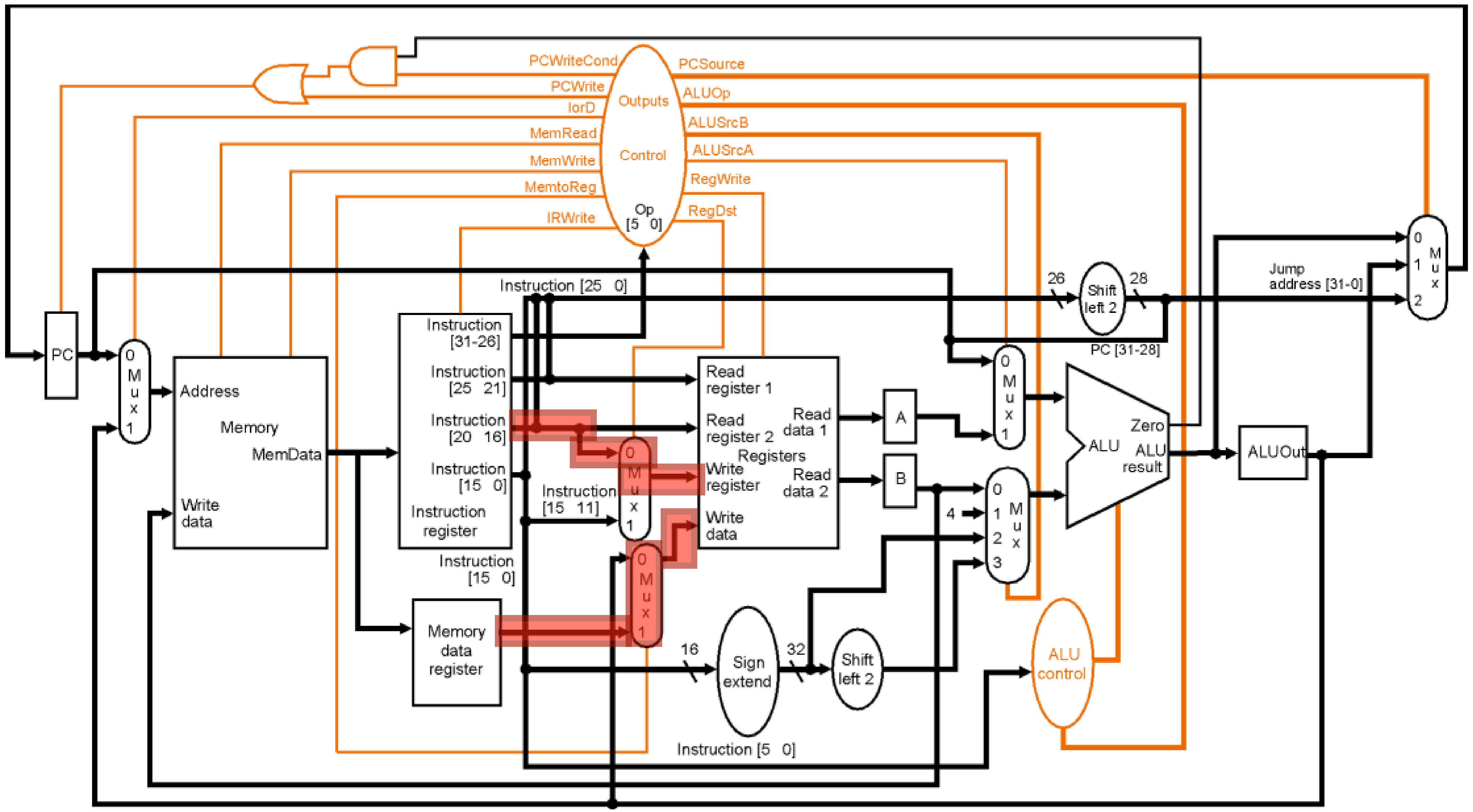

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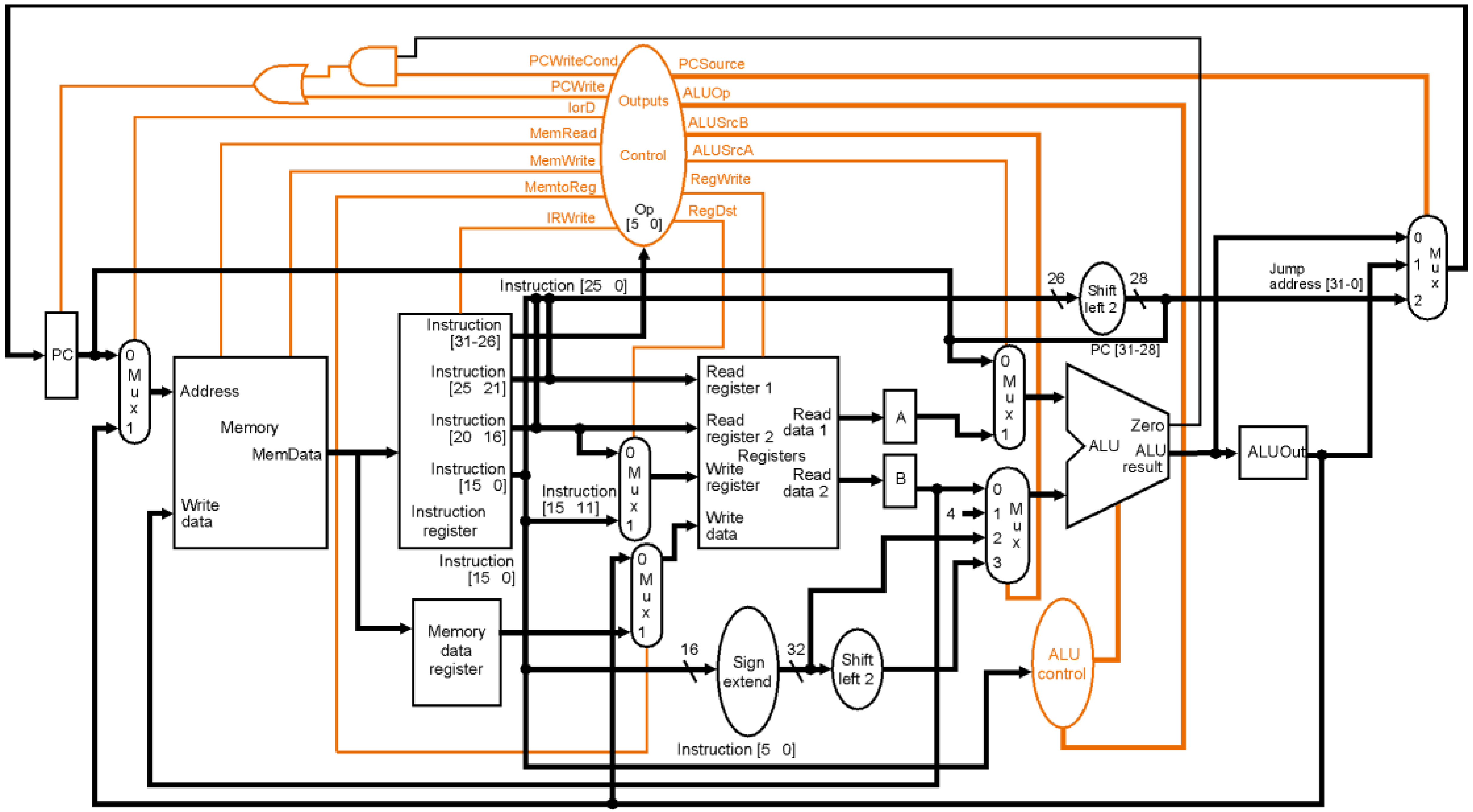

**PC = PC[31-28] | (IR[25-0] <<2)**

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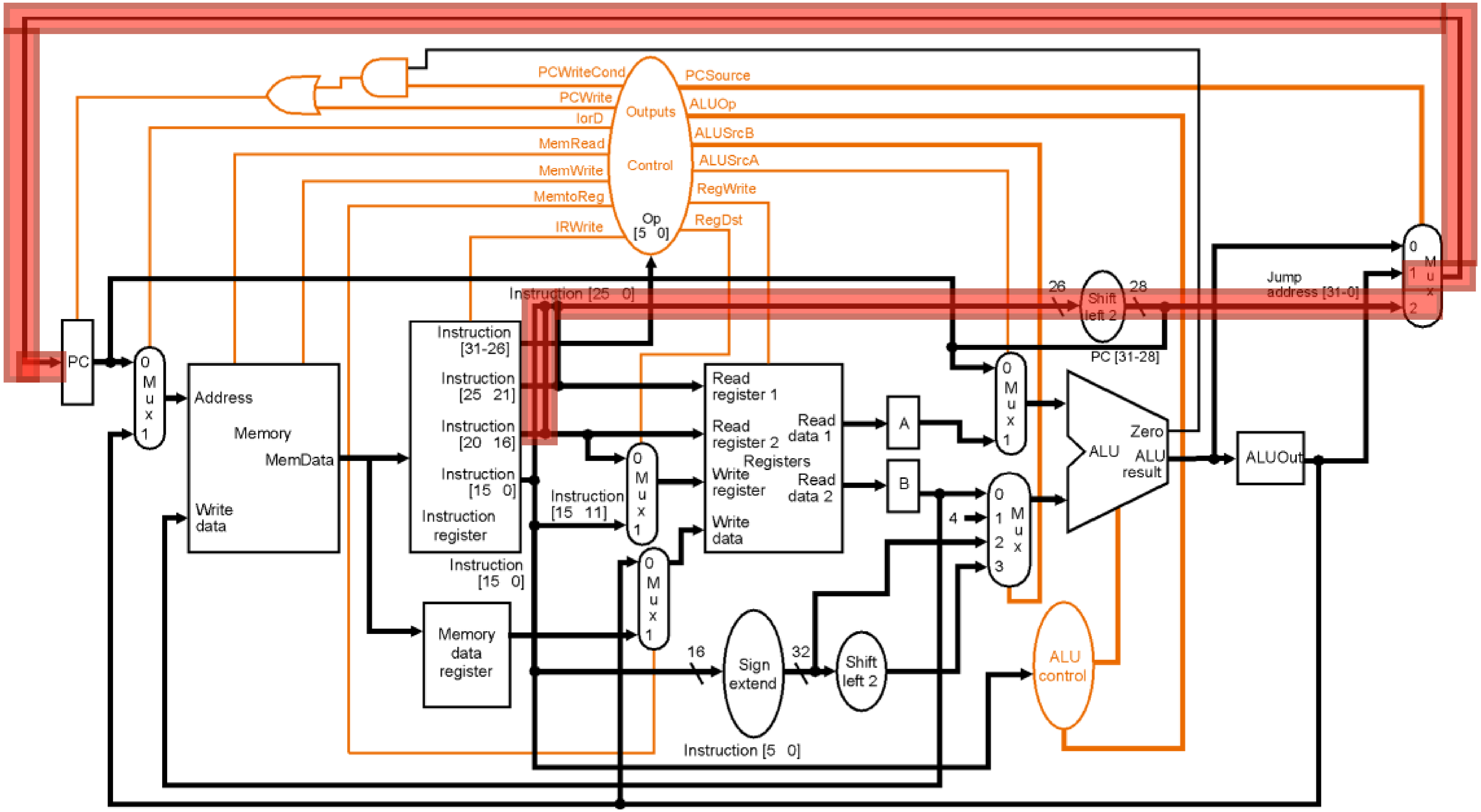
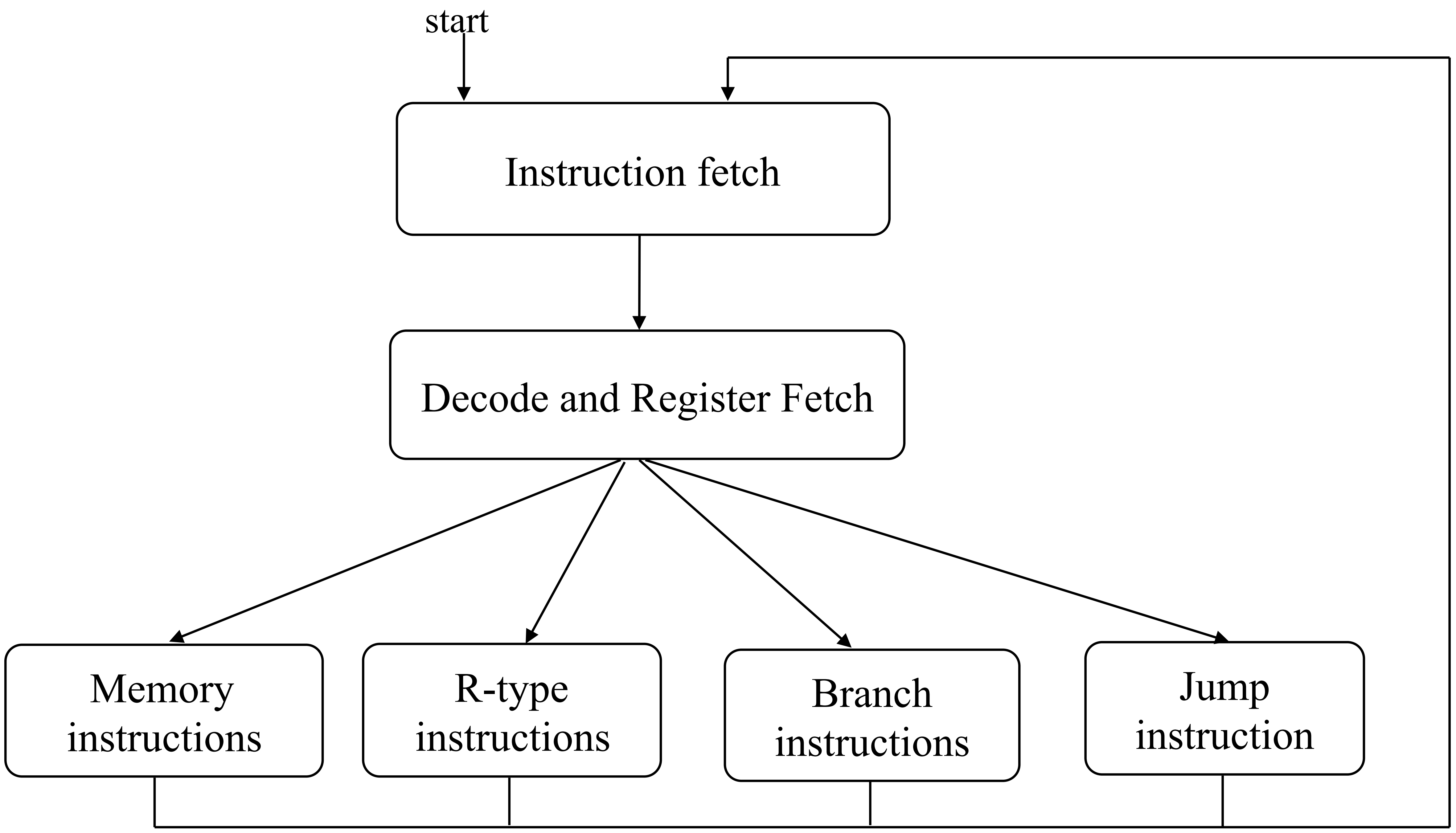


**PC = PC[31-28] | (IR[25-0] <<2)**

## What About the Control?

- Single-cycle control used combinational logic
- What does Multi-cycle control use?
  - FSM defines a succession of states, transitions between states (based on inputs), and outputs (based on state)
  - First two states same for every instruction, next state depends on opcode

## Multi-Cycle Control



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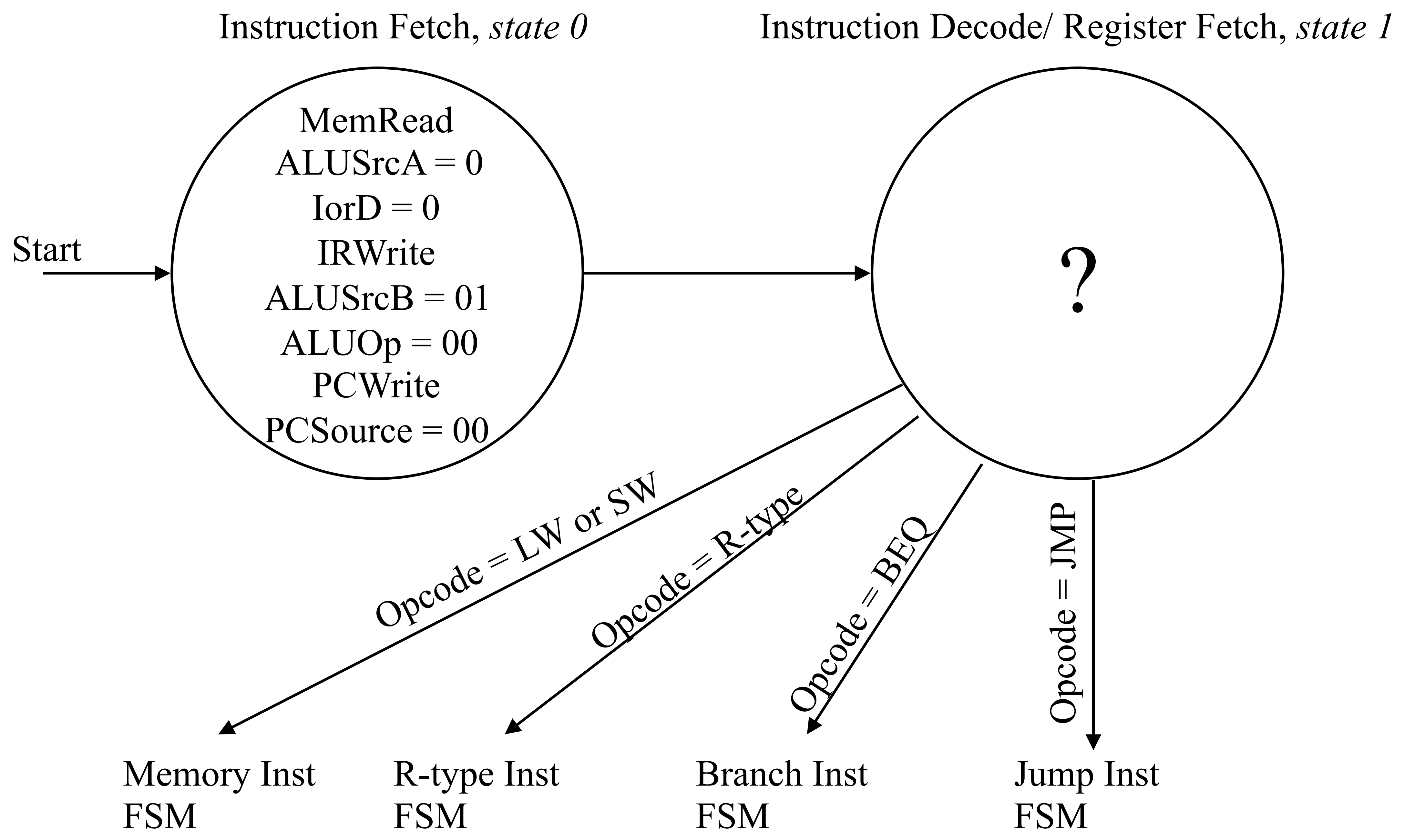
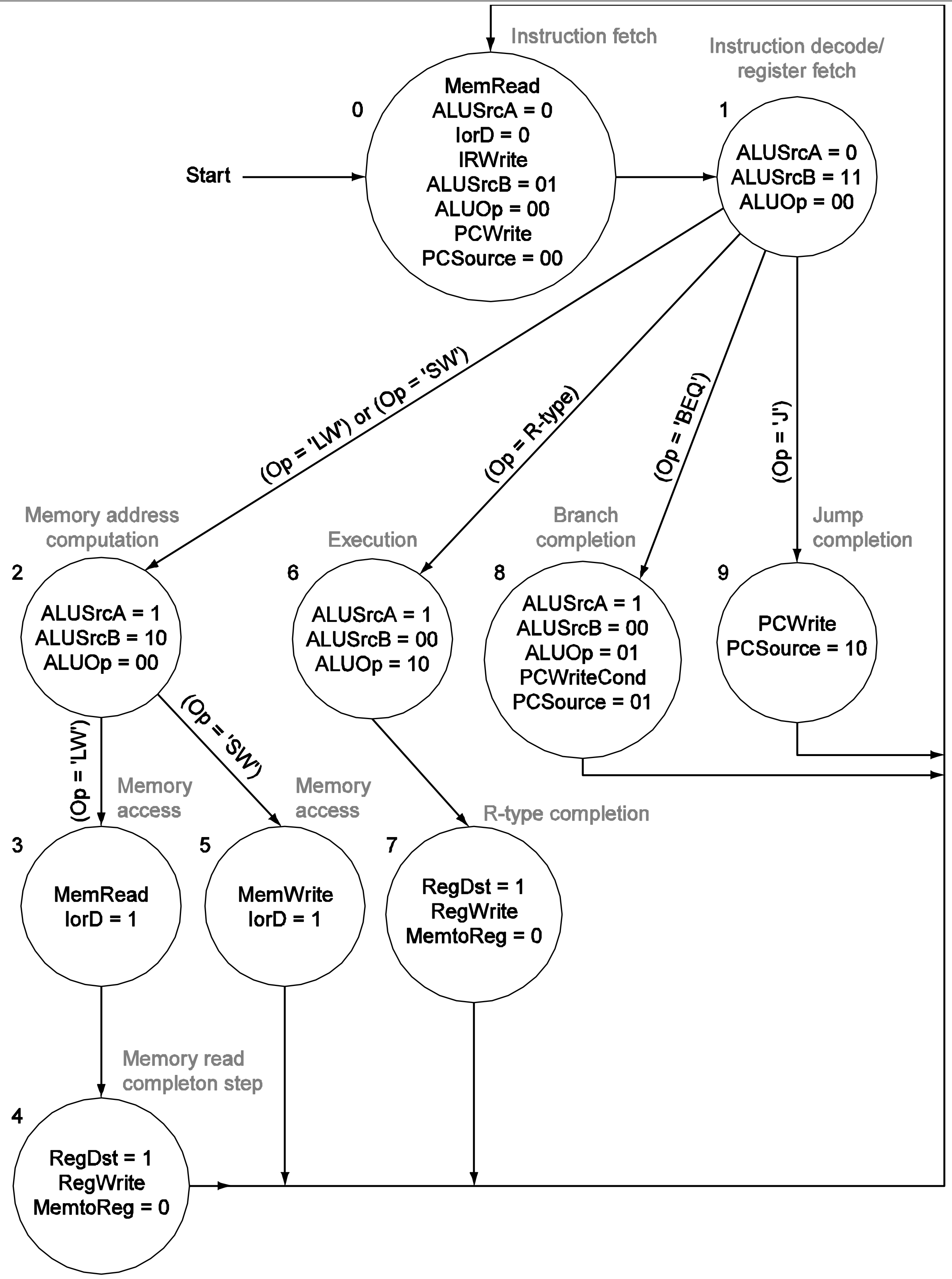


# Multi-Cycle Control - The Full FSM



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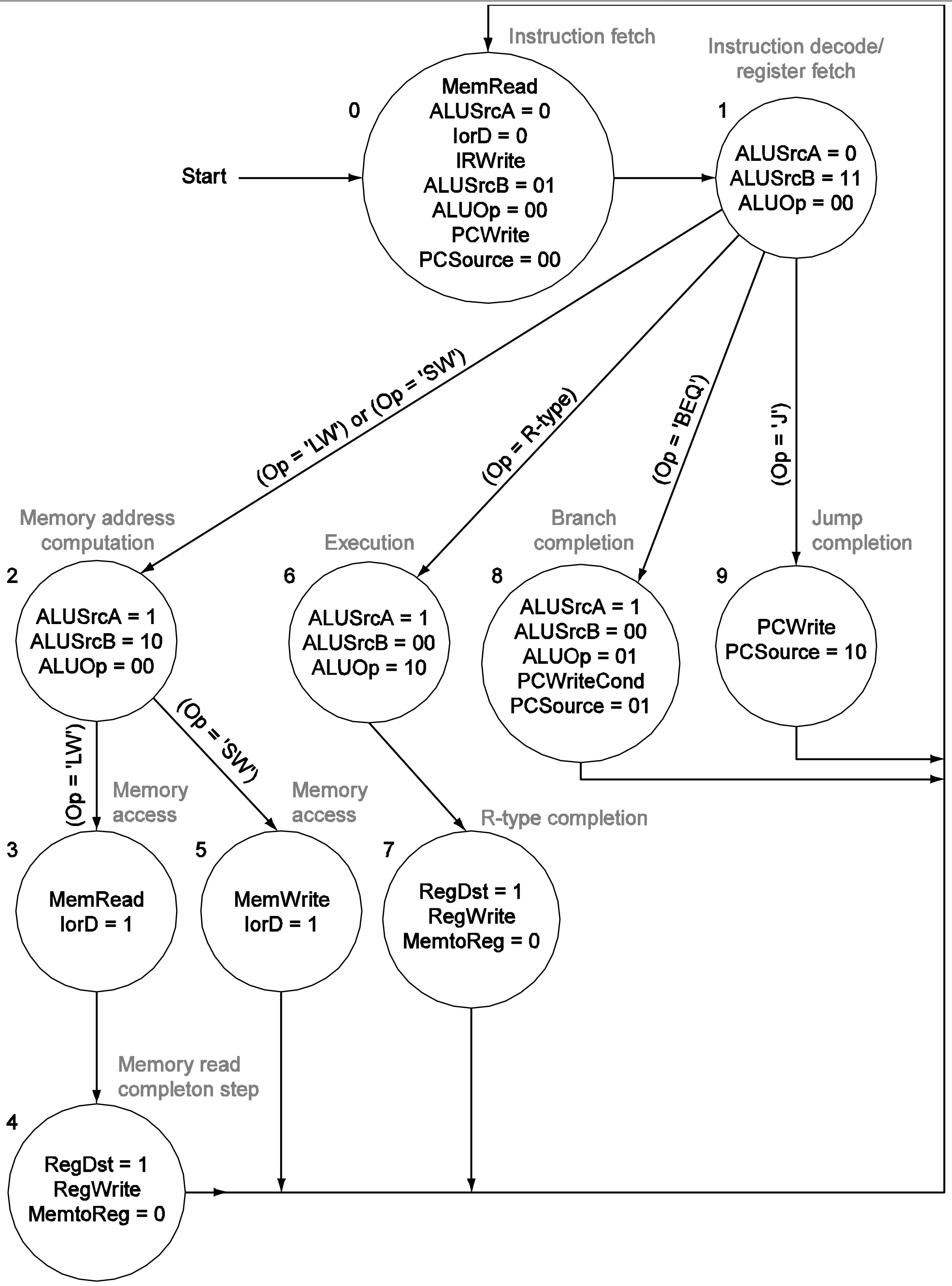
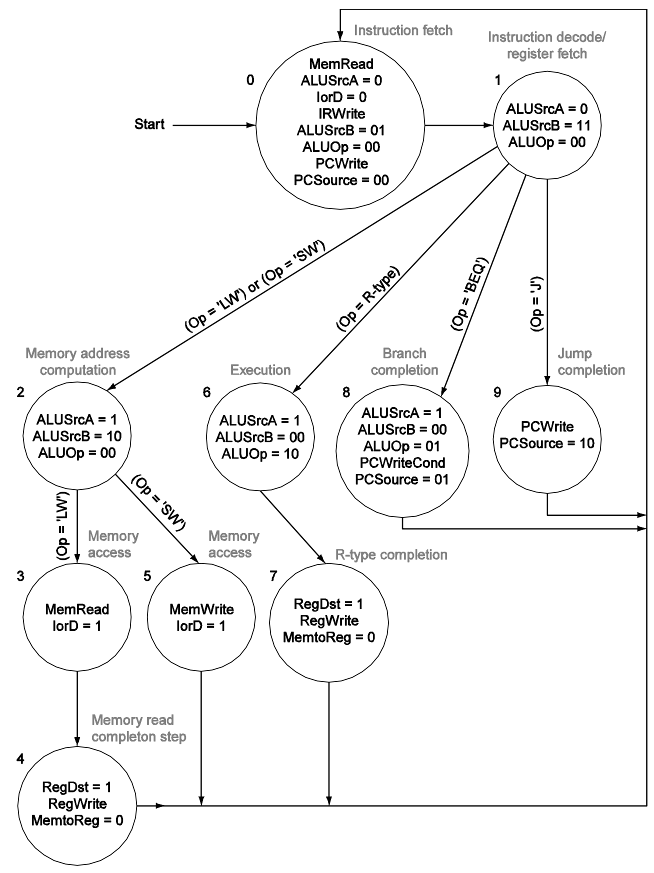


Which type of instruction is the slowest?

# Some Juicy Questions

- How many cycles will it take to execute this code?

```
lw $t2, 0($t3)
lw $t3, 4($t3)
beq $t2, $t3, Label  #assume not taken
add $t5, $t2, $t3
sw $t5, 8($t3)
Label:  ...
```



Instruction fetch
Instruction decode/ register fetch
0
MemRead ALUSrcA = 0 IorD = 0 IRWrite ALUSrcB = 01 ALUOp = 00 PCWrite PCSource = 00
Start
1
ALUSrcA = 0 ALUSrcB = 11 ALUOp = 00
(Op = 'LW') or (Op = 'SW')
(Op = R-type)
(Op = 'BEQ')
(Op = 'J')
Memory address computation
2
ALUSrcA = 1 ALUSrcB = 10 ALUOp = 00
Execution
6
ALUSrcA = 1 ALUSrcB = 00 ALUOp = 10
Branch completion
8
ALUSrcA = 1 ALUSrcB = 00 ALUOp = 01 PCWriteCond PCSource = 01
Jump completion
9
PCWrite PCSource = 10
(Op = 'LW')
(Op = 'SW')
Memory access
Memory access
R-type completion
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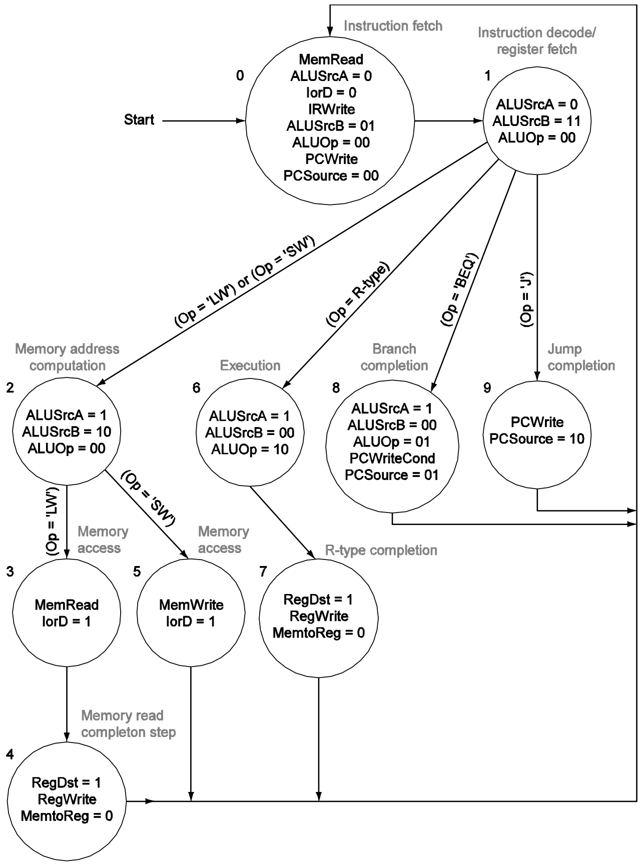

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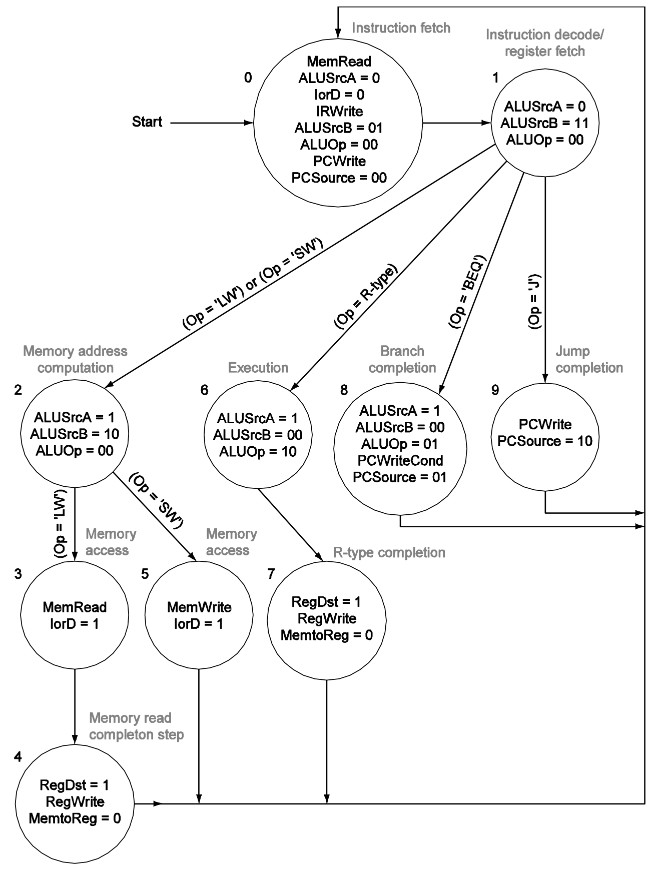

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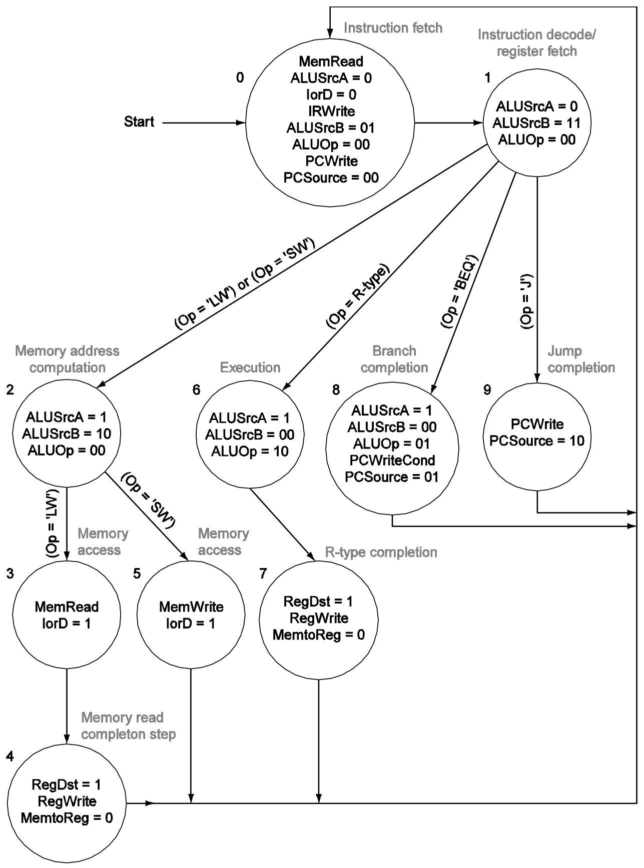

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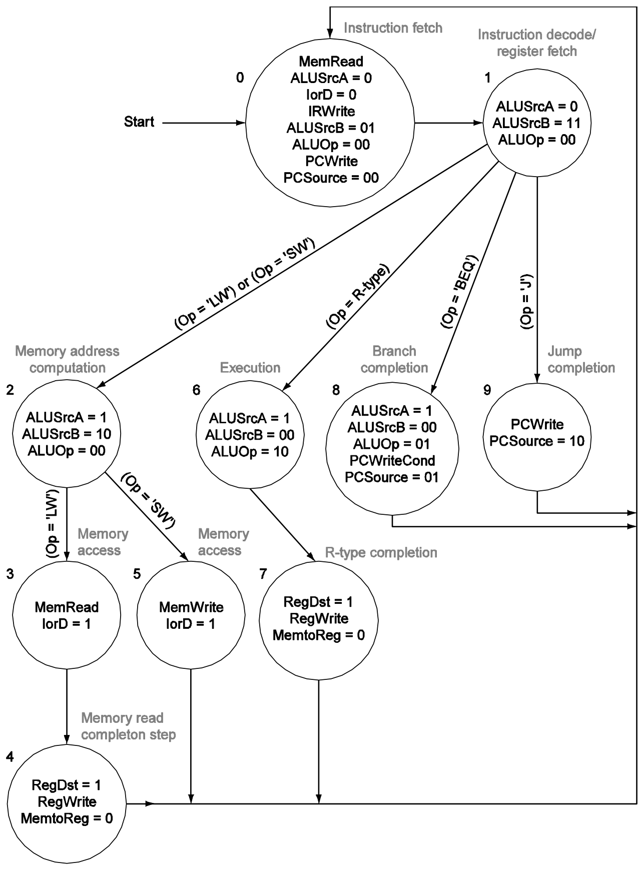

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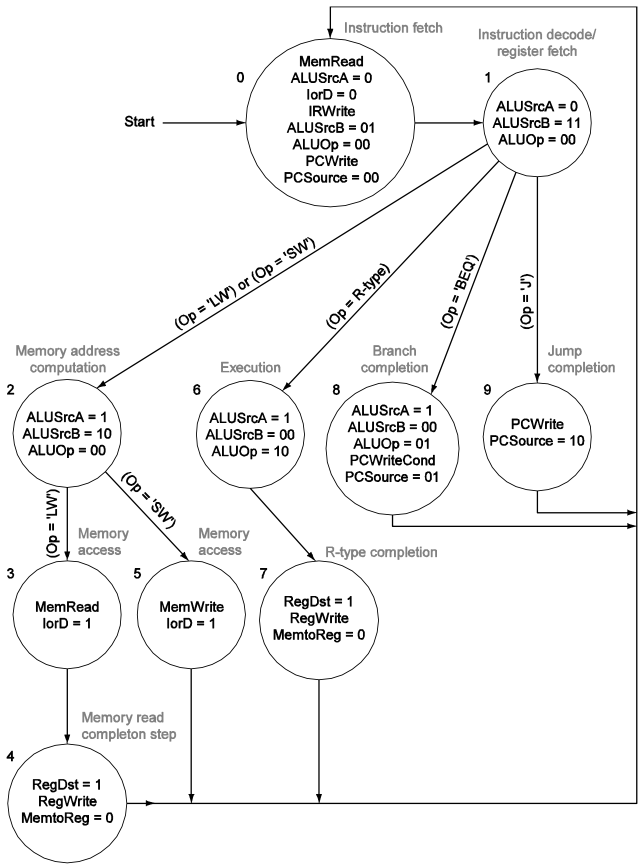

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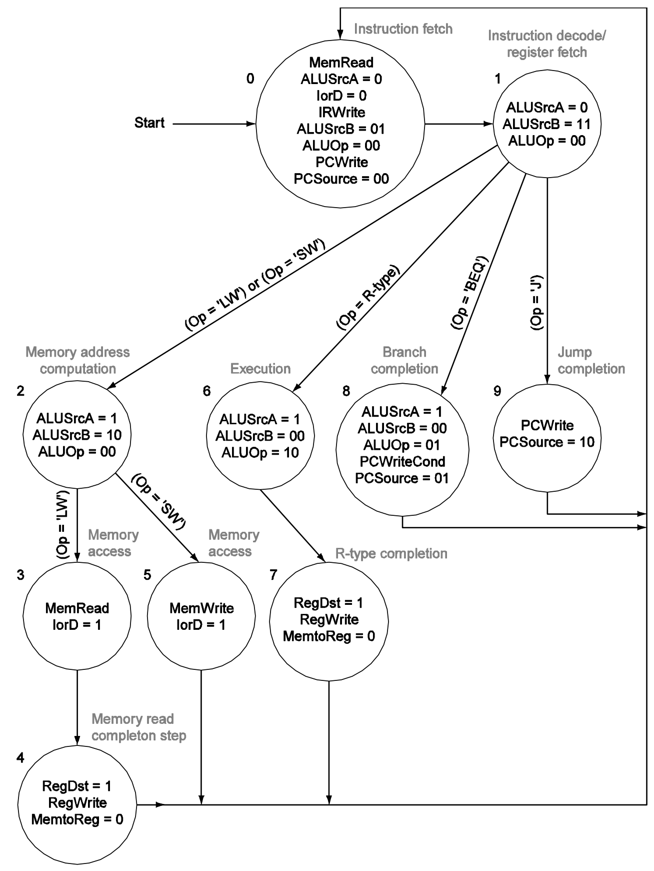

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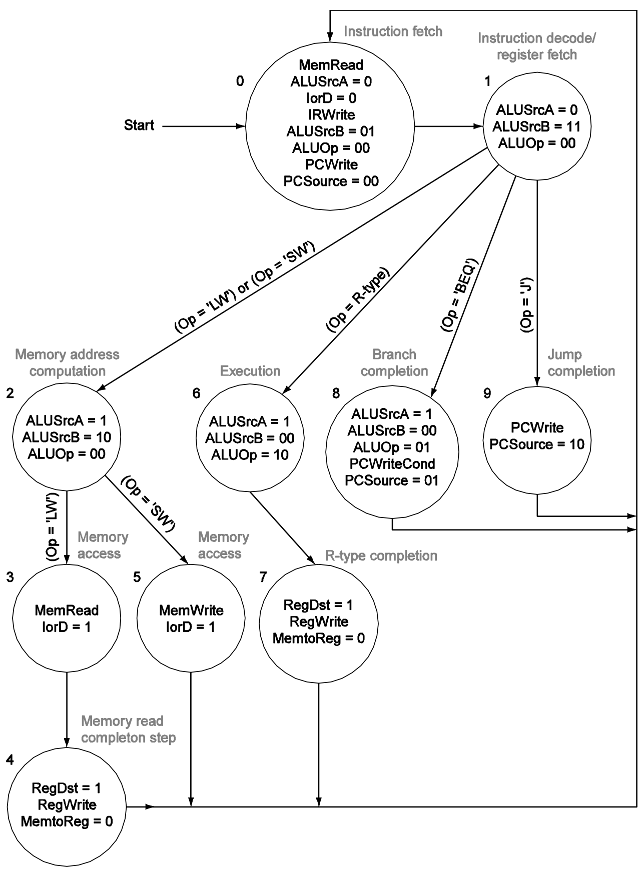
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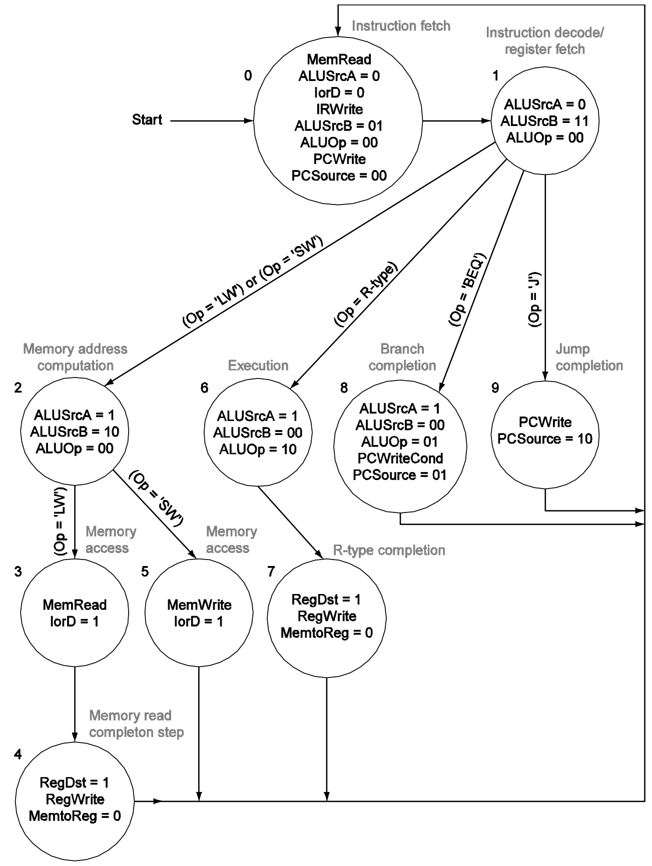

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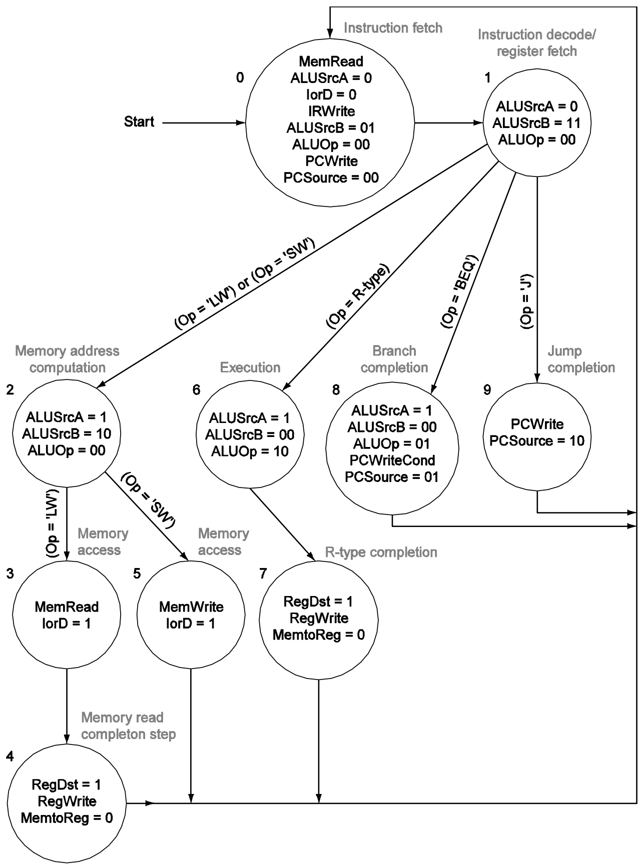
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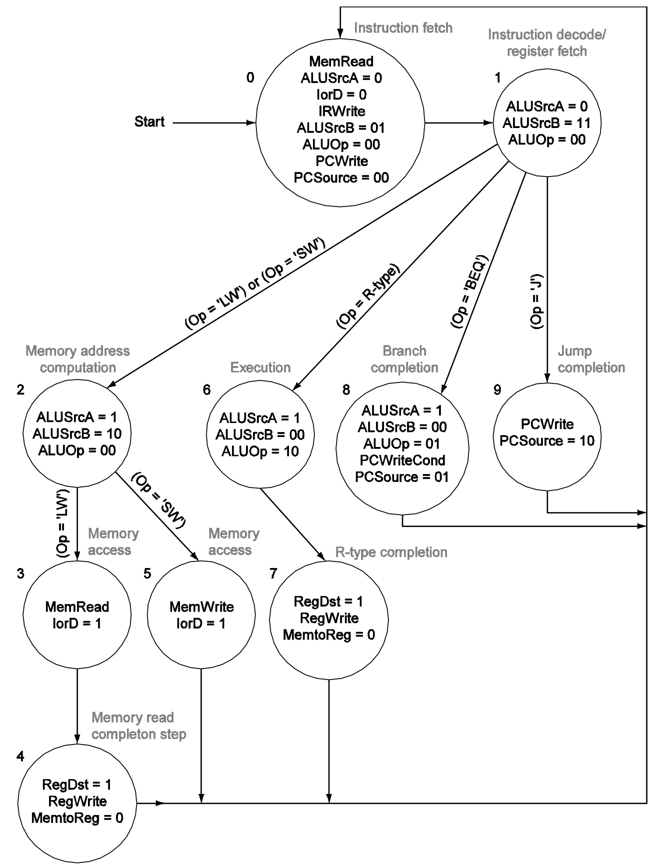

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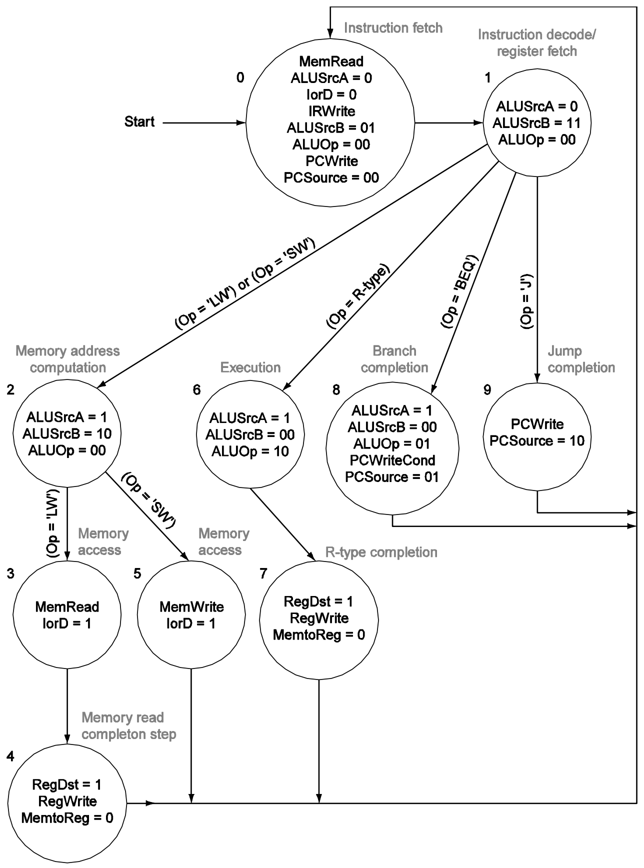

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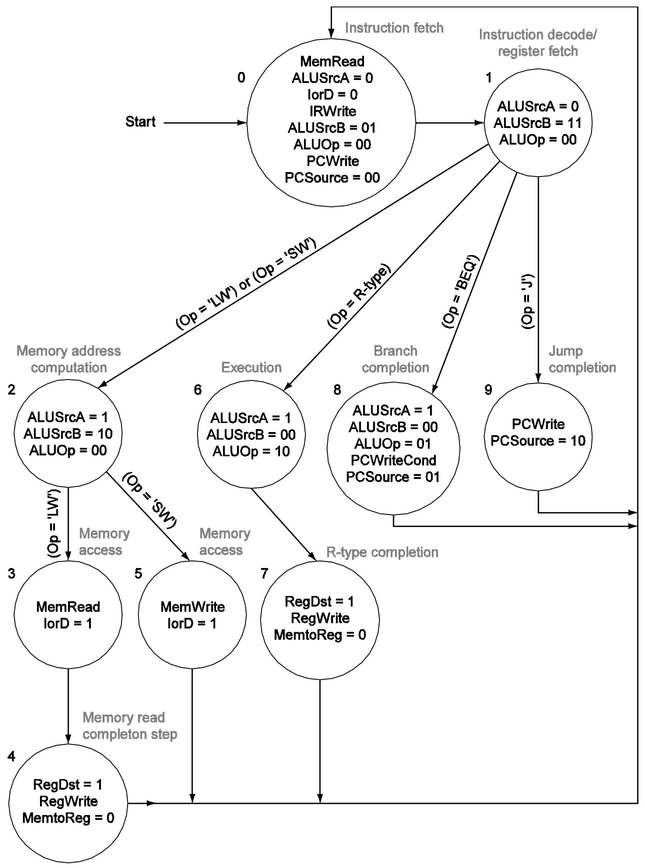

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- ET = IC * CPI * cycle time
- Required very few new state elements
- More, and more complex, control signals
- Control requires FSM

## Exceptions

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- There are two sources of non-sequential control flow in a processor
  - explicit branch and jump instructions
  - exceptions
- *Branches* are synchronous and deterministic
- *Exceptions* are typically asynchronous and non-deterministic
- Guess which is more difficult to handle?

*(control flow refers to the movement of the program counter through memory)*

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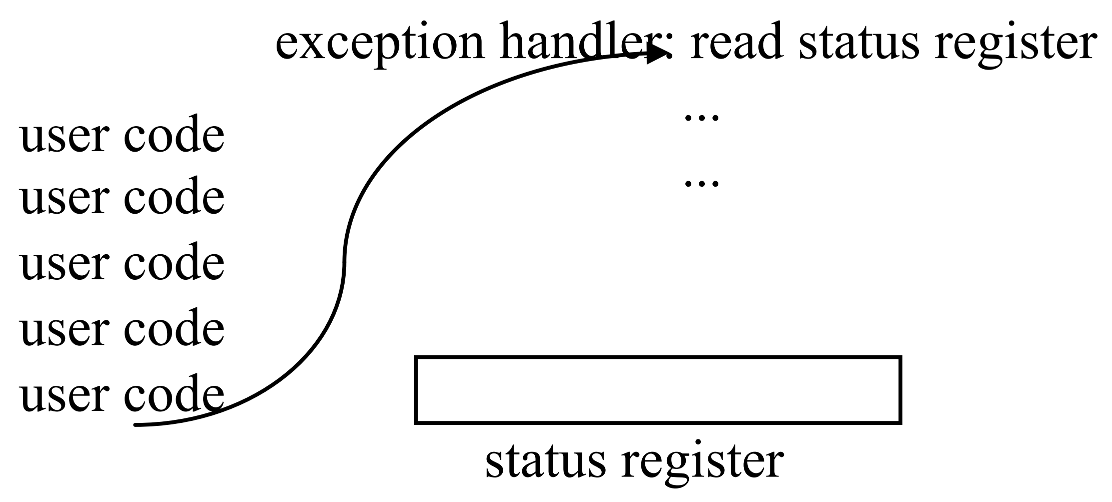
- So what is...
  - arithmetic overflow
  - divide by zero
  - I/O device signals completion to CPU
  - user program invokes the OS
  - memory parity error
  - illegal instruction
  - timer signal

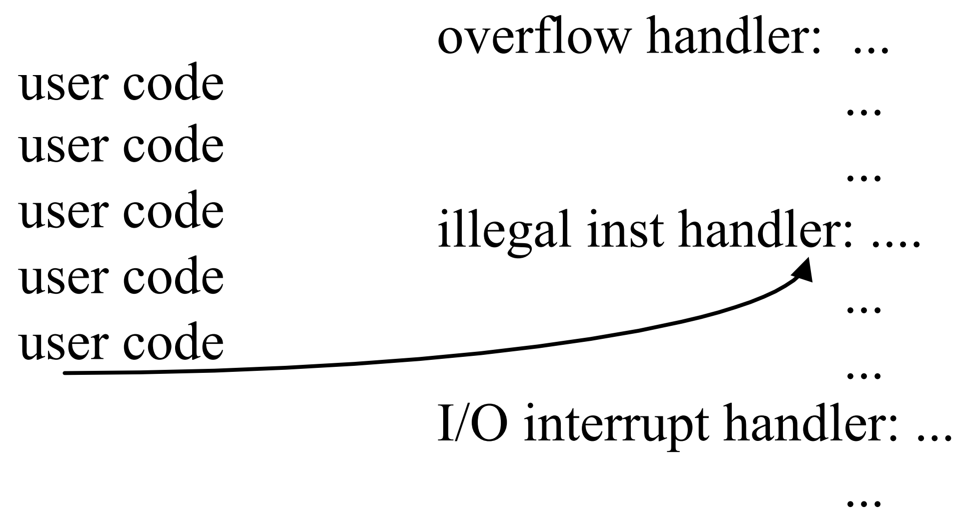
## So Far...

- The machine we’ve been designing in class can generate two types of exceptions.
    - arithmetic overflow
    - illegal instruction
- On an exception, we need to
    - save the PC (invisible to user code)
    - record the nature of the exception/interrupt
    - transfer control to OS

## Handling Exceptions

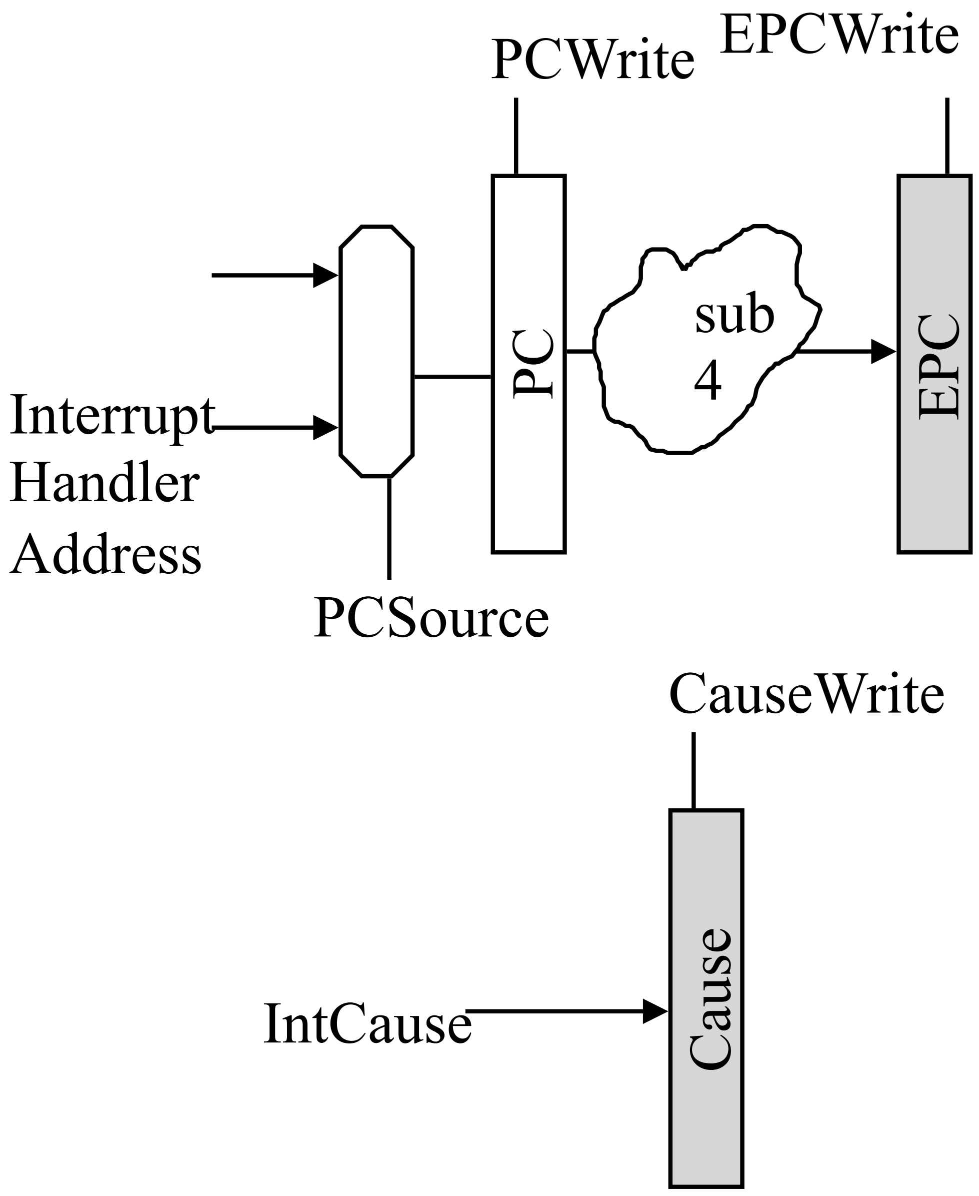
- PC saved in EPC (exception program counter), which the OS may read and store in kernel memory
- A status register, and a single exception handler may be used to record the exception and transfer control, or
- A vectored interrupt transfers control to a different location for each possible type of interrupt/exception



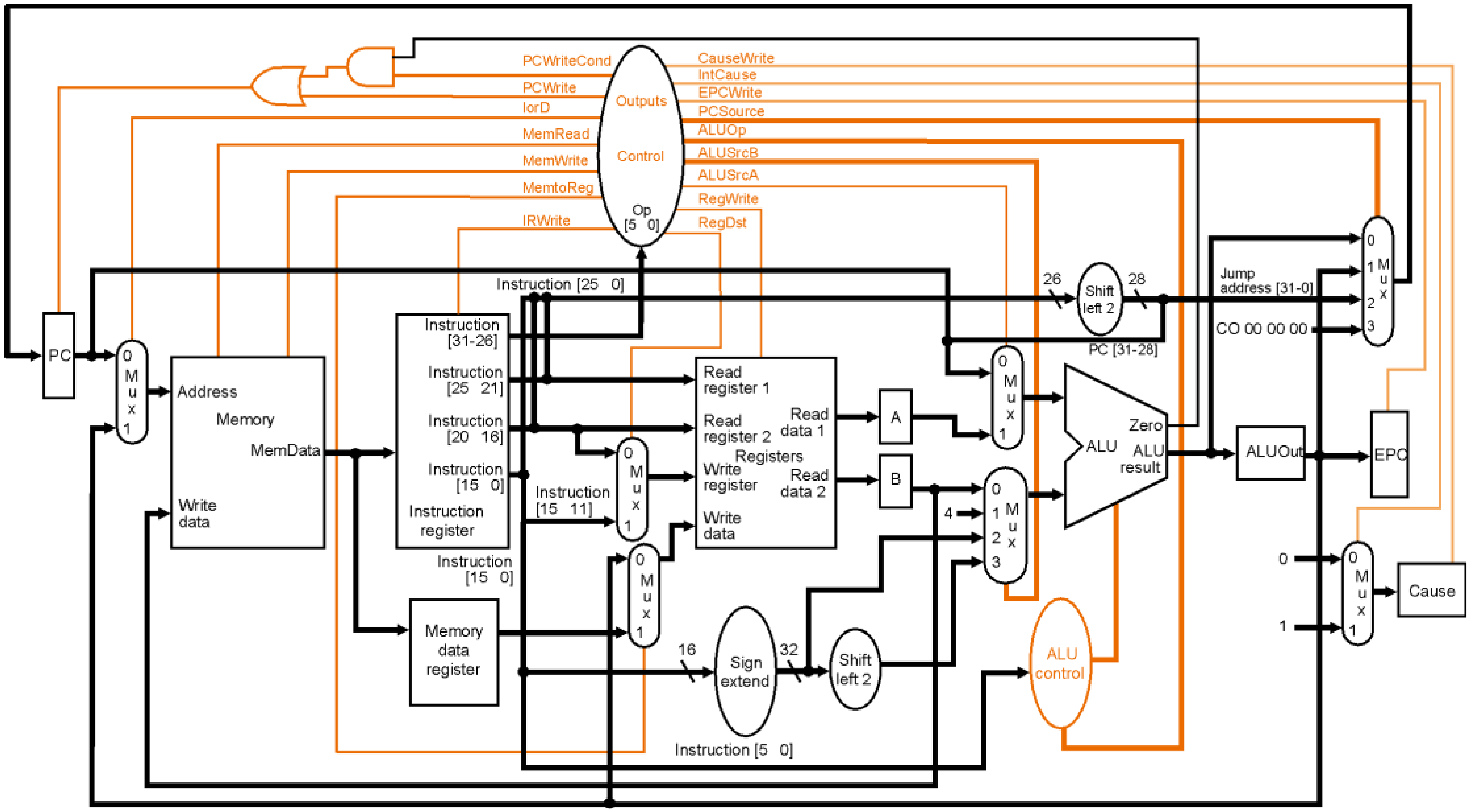


# Supporting Exceptions

- For our MIPS-subset architecture, we will add two registers:
  - EPC: a 32-bit register to hold the user's PC
  - Cause: A register to record the cause of the exception
    - we'll assume undefined inst = 0, overflow = 1
- We will also add three control signals:
  - EPCWrite (will need to be able to subtract 4 from PC)
  - CauseWrite
  - IntCause
- We will extend PCSource multiplexor to be able to latch the interrupt handler address into the PC.



# Supporting Exceptions in our Datapath



## Key Take-away

- Exception-handling is difficult in the CPU
    - because the interactions between the executing instructions and the interrupt are complex and sometimes unpredictable.