MCQ (Single Correct Answer)

GATE CSE 1996

Both's algorithm for integer multiplication gives worst performance when the multiplier pattern is

A) 101010....1010

B) 100000.....0001

C) 111111.....11111

D) 011111.....11100

MCQ (Single Correct Answer)

GATE CSE 1997

An N-bit carry look ahead adder, where NN is a multiple of 4, employs Ics 74181 (4bit ALUALU) and 74182 (4 bit carry look ahead generator). The minimum addition time using the best architecture for this adder is

A) proportional to N

B) proportional to log N

C) a constant

D) None of the above

MCQ (Single Correct Answer)

GATE CSE 2002

In 2′s complement addition, the overflow

A) is flagged whenever there is carry from sign bit addition

B) cannot occur when a +ve value is added to a −ve value

C) is flagged when the carries from sign bit and previous bit match

D) None of the above

MCQ (Single Correct Answer)

GATE CSE 2004

What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

(113. + -111.) + 7.51

113. + (-111. + 7.51)

A) 9.51 and 10.0 respectively

B) 10.0 and 9.51 respectively

C) 9.51 and 9.51 respectively

D) 10.0 and 10.0 respectively

MCQ (Single Correct Answer)

GATE CSE 2008

In the IEEE floating point representation, the hexadecimal value 0 × 00000000 corresponds to

(A) the normalized value 2^{-127}

(B) the normalized value 2^{-126}

(C) the normalized value +0

(D) the special value +0

MCQ (Single Correct Answer)

GATE CSE 2012

T he decimal value 0.5 in IEEE single precision floating point representation has

A) fraction bits of 000…000 and exponent value of 0

B) fraction bits of 000…000 and exponent value of −1

C) fraction bits of 100…000 and exponent value of 0

D) no exact representation

MCQ (Single Correct Answer)

GATE CSE 2017 SET 1

The n-bit fixed-point representation of an unsigned real number X uses f bits for the fraction part. Let i = n – f. The range of decimal values for X in this representation is

(A) 2^{-f}

(B) 2^{-f} to ($2^{i} – 2^{-f}$)

(C) 0 to 2^{-i}

(D) 0 to $2^{i} – 2^{-f}$)

MCQ (Single Correct Answer)

GATE CSE 2017 SET 2

Given the following binary number in 32 bit (single precision) IEEE-754 format:
00111110011011010000000000000000
The decimal value closest to this floating-point number is:
(A) 1.45×10^{1}
(B) 1.45×10^{-1}
(C) 2.27×10^{-1}
(D) 2.27×10^{1}

MCQ (Single Correct Answer)

GATE CSE 1996

Consider the following floating point number representation

The exponent is in 2's complement representation and mantissa is in the sign magnitude representation. The range of the magnitude of the normalized numbers in this representation is

a). 0 to 1

b). 0.5 to 1

c). 2^{-23} to 0.5

d). 0.5 to $(1-2^{-23})$

MCQ (Single Correct Answer)

GATE CSE 1999

The number of full and half-adders required to add 16-bit numbers is:

A) 8 half-adders, 8 full-adders

B) 1 half-adder, 15 full-adders

C) 16 half-adders, 0 full-adders

D) 4 half-adders, 12 full-adders

MCQ (Single Correct Answer)

GATE CSE 1999

Using Booth's Algorithm for multiplication, the multiplier -57 will be recoded as

(A) 0 -1 0 0 1 0 0 -1

(B) 1 1 0 0 0 1 1 1

(C) 0 -1 0 0 1 0 0 0

(D) 0 1 0 0 -1 0 0 1

MCQ (Single Correct Answer)

GATE CSE 2002

Sign extension is the step in

A) Floating point multiplication

B) Signed 16 bit integer addition

C) Arithmetic left shift

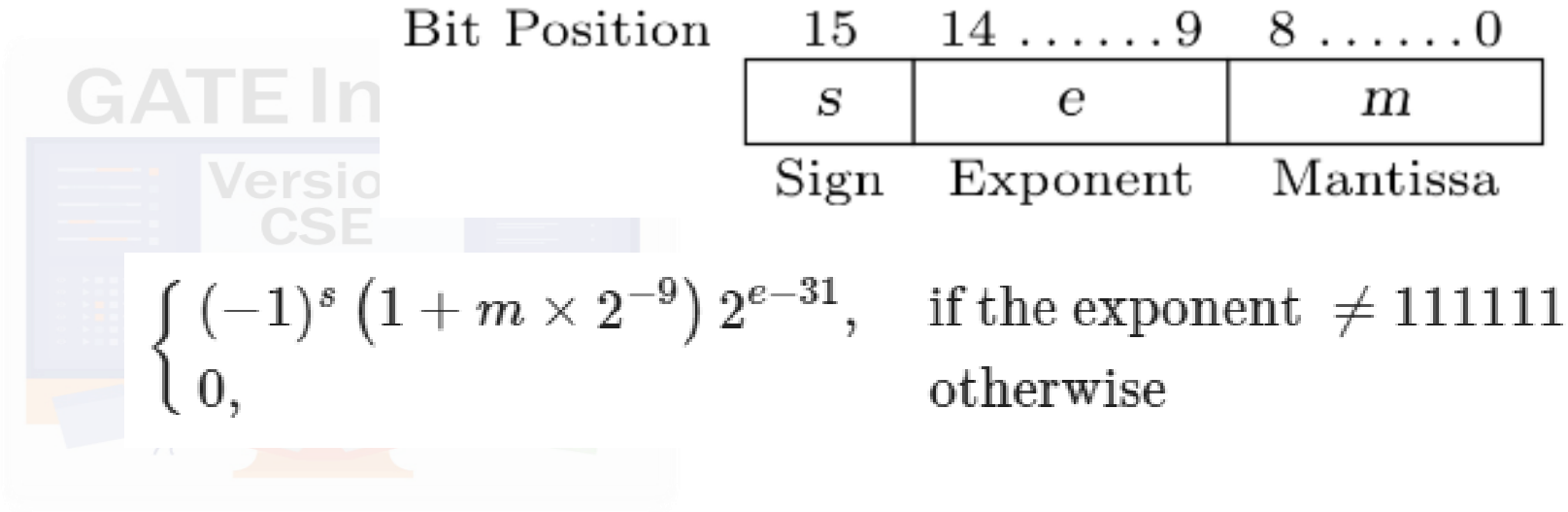
D) Converting a signed integer from one size to another

MCQ (Single Correct Answer)

GATE CSE 2003

The following is a scheme for floating point number representation using 16 bits.
Let s,e, and m be the numbers represented in binary in the sign, exponent, and mantissa fields respectively.
Then the floating point number represented is:
What is the maximum difference between two successive real numbers representable in this system?

(A) 2^{-40}
(B) 2^{-9}
(C) 2^{22}
(D) 2^{31}



$$\begin{cases} (-1)^s \left(1 + m \times 2^{-9}\right) 2^{e-31}, & \text{if the exponent } \neq 111111 \\ 0, & \text{otherwise} \end{cases}$$

MCQ (Single Correct Answer)

GATE CSE 2004

A 4-bit carry lookahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

(A) 4 time units
(B) 6 time units
(C) 10 time units
(D) 12 time units

MCQ (Single Correct Answer)

GATE CSE 2005

Consider the following floating point format

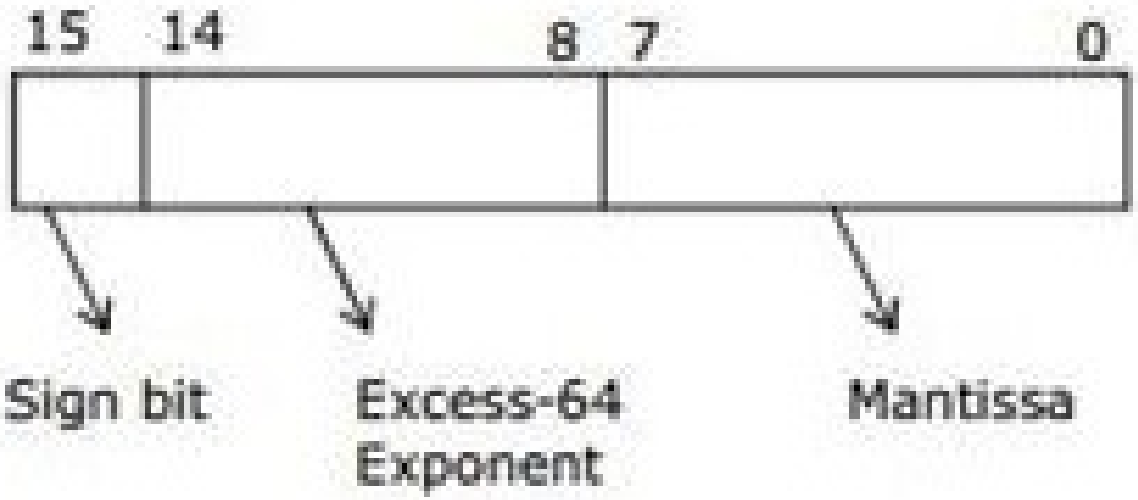
Mantissa is a pure fraction in sign-magnitude form. The decimal number 0.239×2^{13} has the following hexadecimal representation (without normalization and rounding off :

(A) 0D 24

(B) 0D 4D

(C) 4D 0D

(D) 4D 3D



MCQ (Single Correct Answer)

GATE CSE 2005

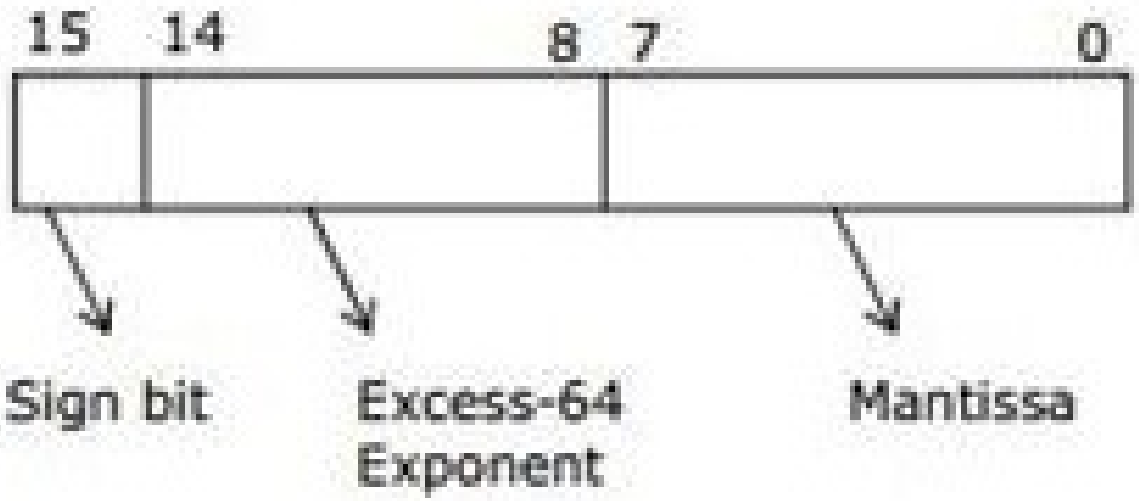
Mantissa is a pure fraction in sign-magnitude form. The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field. The normalized representation of the above number (0.239×2^{13}) is:

(A) 0A 20

(B) 11 34

(C) 4D D0

(D) 4A E8



MCQ (Single Correct Answer)

GATE CSE 2006

Given two three bit numbers a2a1a0 and b2b1b0 and c, the carry in, the function that represents the carry generate function when these two numbers are added is:

A. $a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2a_0b_1b_0 + a_1b_2b_1 + a_1a_0b_2b_0 + a_0b_2b_1b_0$

B. $a_2b_2 + a_2b_1b_0 + a_2a_1b_1b_0 + a_1a_0b_2b_1 + a_1a_0b_2 + a_1a_0b_2b_0 + a_2a_0b_1b_0$

C. $a_2 + b_2 + (a_2 \oplus b_2)(a_1 + b_1 + (a_1 \oplus b_1) + (a_0 + b_0))$

D. $a_2b_2 + \overline{a_2}a_1b_1 + \overline{a_2a_1}a_0b_0 + \overline{a_2}a_0\overline{b_1}b_0 + a_1\overline{b_2}b_1 + \overline{a_1}a_0\overline{b_2}b_0 + a_0\overline{b_2b_1}b_0$

MCQ (Single Correct Answer)

GATE CSE 2007

In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:

$P_i = A_i \oplus B_i$ and $G_i = A_iB_i$

The expressions for the sum bit S_i and the carry bit C_{i+1} of the look-ahead carry adder are given by:

$S_i = P_i \oplus C_i$ and $C_{i+1} = G_i + P_iC_i$, where C_0 is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S3, S2, S1, S0 and C4 as its outputs are respectively:

A) 6, 3

B) 10, 4

C) 6, 4

D) 10, 5

MCQ (Single Correct Answer)

GATE CSE 2014 Set 2

The value of a float type variable is represented using the single-precision 32-bit floating point format IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of −14.25. The representation of X in hexadecimal notation is

(A) C1640000H

(B) 416C0000H

(C) 41640000H

(D) C16C0000H

MCQ (Single Correct Answer)

GATE CSE 2016 Set 1

Consider a carry lookahead adder for adding two n-bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is

(A) Θ(1)

(B) Θ(Log (n))

(C) Θ(√ n)

(D) Θ(n)

YT Channel name:- GATE Insights Version: CSE

Website link :- www.education4fun.com

MCQ (Single Correct Answer)

GATE CSE 2018

Consider the unsigned 8-bit fixed point binary number representation, below,

$b_7b_6b_5b_4b_3 \cdot b_2b_1b_0$

where the position of the binary point is between b_3 and b_2 . Assume b_7 is the most significant bit. Some of the decimal numbers listed below cannot be represented exactly in the above representation:

(i) 31.500 (ii) 0.875 (iii) 12.100 (iv) 3.001

Which one of the following statements is true?

(A) None of (i), (ii), (iii), (iv) can be exactly represented

(B) Only (ii) cannot be exactly represented

(C) Only (iii) and (iv) cannot be exactly represented

(D) Only (i) and (ii) cannot be exactly represented

MCQ (Single Correct Answer)

GATE CSE 2020

Consider three registers R1, R2, and R3 that store numbers in IEEE−754 single precision floating point format. Assume that R1 and R2 contain the values (in hexadecimal notation) 0x42200000 and 0xC1200000, respectively. If R3 = R1 / R2, what is the value stored in R3 ?

(A) 0x40800000

(B) 0xC0800000

(C) 0x83400000

(D) 0xC8500000

Subjective

GATE CSE 1993

A ROM is used to store a truth table for a binary multiplier unit that will multiply two 4 bit numbers. The size of the ROM (number of words × number of bits) that is required to accommodate the truth table is M words × N bits. Write the values of M and N.

Subjective

GATE CSE 1995

The capacity of a memory unit is defined by the number of words multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of 4K × 16?

A)10 address, 16 data lines
B)11 address, 8 data lines
C)12 address, 16 data lines
D)12 address, 12 data lines

MCQ (Single Correct Answer)

GATE CSE 1995

A computer system has a 4K word cache organized in block set associative manner with 4 blocks per set, 64 words per block. The number of bits in the SETSET and WORDWORD fields of the main memory address format is

A) 15,40

B) 6,4

C) 7,2

D) 4,6

MCQ (Single Correct Answer)

GATE CSE 1996

A ROM is used to store the table for multiplication of two 8 bit unsigned integers. The size of ROM required is

A) 256×16

B) 64K×8

C) 4K×16

D) 64K×16

MCQ (Single Correct Answer)

GATE CSE 1999

The main memory of a computer has 2 cm blocks while the cache has 2c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then the block k of main memory maps to the set:

A) (k mod m) of the cache

B) (k mod c) of the cache

C) (k mod 2c) of the cache

D) (k mod 2cm) of the cache

MCQ (Single Correct Answer)

GATE CSE 2001

More than one word are put in one cache block to

A) Exploit the temporal locality of reference in a program

B) Exploit the spatial locality of reference in a program

C) Reduce the miss penalty

D) None of the above

YT Channel name:- GATE Insights Version: CSE
Website link :- www.education4fun.com

MCQ (Single Correct Answer)

GATE CSE 2005

Increasing the RAM of a computer typically improves performance because

A) Virtual memory increases

B) Larger RAMs are faster

C) Fewer page faults occur

D) Fewer segmentation faults occur

MCQ (Single Correct Answer)

GATE CSE 2007

Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The numbers of bits in the TAG, LINE and WORD fields are respectively

A) 9,6,5

B) 7,7,6

C) 7,5,8

D) 9,5,6

MCQ (Single Correct Answer)

GATE CSE 2009

How many 32k x 1 RAM chips are needed to provide a memory capacity of 256 K-bytes?

A) 8

B) 32

C) 64

D) 128

MCQ (Single Correct Answer)

GATE CSE 2010

A main memory unit with a capacity of 4 megabytes is built using 1M × 1-bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is

A) 100 nanoseconds

B) 100×2^{10} nanoseconds

C) 100×2^{20} nanoseconds

D) 3200×2^{20} nanoseconds

MCQ (Single Correct Answer)

GATE CSE 2012

The amount of ROM needed to implement a 4 bit multiplier is

A) 64 bits

B) 128 bits

C) 1 Kbits

D) 2 Kbits

MCQ (Single Correct Answer)

GATE CSE 2013

In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from.

(A) (j mod v) * k to (j mod v) * k + (k-1)
(B) (j mod v) to (j mod v) + (k-1)
(C) (j mod k) to (j mod k) + (v-1)
(D) (j mod k) * v to (j mod k) * v + (v-1)

MCQ (Single Correct Answer)

GATE CSE 2014 Set 1

An access sequence of cache block address is of length N and contains n unique block addresses. The number of unique block addresses between two consecutive accesses to the same block address is bounded above by k. What is the miss ration is the access sequence is passed through a cache of associativity A >= k exercising least-recently used replacement policy.

A) n/N

B) 1/N

C) 1/A

D) k/n

Numerical

GATE CSE 2015 Set 2

Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is _____.

Numerical

GATE CSE 2015 Set 2

A computer system implements a 40 bit virtual address, page size of 8 kilobytes, and a 128-entry translation look-aside buffer (TLB) organized into 32 sets each having four ways. Assume that the TLB tag does not store any process id. The minimum length of the TLB tag in bits is _____

A) 20
B) 10
C) 11
D) 22

MCQ (Single Correct Answer)

GATE CSE 2015 Set 3

Consider a machine with a byte addressable main memory of 2^{20} bytes, block size of 16 bytes and a direct mapped cache having 2^{12} cache lines. Let the addresses of two consecutive bytes in main memory be $(E201F)_{16}$ and $(E2020)_{16}$. What are the tag and cache line address (in hex) for main memory address $(E201F)_{16}$?

(A) E, 201

(B) F, 201

(C) E, E20

(D) 2, 01F

Numerical

GATE CSE 2016 Set 1

A processor can support a maximum memory of 4 GB, where the memory is word-addressable (a word consists of two bytes). The size of the address bus of the processor is at ____ least bits.

Numerical

GATE CSE 2018

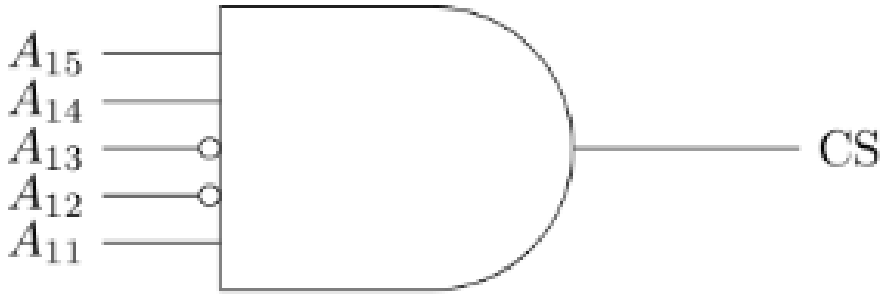
A 32 – bit wide main memory unit with a capacity of 1 GB is built using 256M X 4-bit DRAM chips. The number of rows of memory cells in the DRAM chip is 2^{14}. The time taken to perform one refresh operation is 50 nanoseconds. The refresh period is 2 milliseconds. The percentage (rounded to the closet integer) of the time available for performing the memory read/write operations in the main memory unit is _____ .

MCQ (Single Correct Answer)

GATE CSE 2019

The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A_{15} to A_0. What is the range of addresses (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?

A) C800 to CFFF
B) C800 to C8FF
C) DA00 to DFFF
D) CA00 to CAFF



MCQ (Single Correct Answer)

GATE CSE 2019

A certain processor uses a fully associative cache of size 16 kB. The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32-bit address. How many bits are required for the Tag and the Index fields resectively in the addresses generated by the processor?

A) 28 bits and 4 bits

B) 24 bits and 4 bits

C) 24 bits and 0 bits

D) 28 bits and 0 bits

Numerical

GATE CSE 2020

A direct mapped cache memory of 1 MB has a block ize of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is _____.

Subjective

GATE CSE 1990

A block -set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each blocks contains 256 eight bit words.

(i) How many bits are required for addressing the main memory?

(ii) How many bits are needed to represent the TAG, SET and WORD fields?

MCQ (Single Correct Answer)

GATE CSE 2004

Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8, 12, 0, 12, 8

(A) 2
(B) 3
(C) 4
(D) 5

MCQ (Single Correct Answer)

GATE CSE 2005

Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively

A) 10, 17

B) 10, 22

C) 15, 17

D) 5, 17

MCQ (Single Correct Answer)

GATE CSE 2006

A CPU has a cache with block size 64 bytes. The main memory has k banks, each bank being c bytes wide. Consecutive c − byte chunks are mapped on consecutive banks with wrap-around. All the k banks can be accessed in parallel, but two accesses to the same bank must be serialized. A cache block access may involve multiple iterations of parallel bank accesses depending on the amount of data obtained by accessing all the k banks in parallel. Each iteration requires decoding the bank numbers to be accessed in parallel and this takes. k/2 ns The latency of one bank access is 80 ns. If c = 2 and k = 24, the latency of retrieving a cache block starting at address zero from main memory is:

(A) 92 ns

(B) 104 ns

(C) 172 ns

(D) 184 ns

MCQ (Single Correct Answer)

GATE CSE 2006

Consider two cache organizations: The first one is 32 KB 2-way set associative with 32-byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has a latency of 0.6 ns while a kbit comparator has a latency of k/10 ns. The hit latency of the set associative
organization is h1 while that of the direct mapped one is h2.
The value of h1 is:

A) 2.4 ns
B) 2.3 ns
C) 1.8 ns
D) 1.7 ns

MCQ (Single Correct Answer)

GATE CSE 2006

Consider two cache organizations: The first one is 32 KB 2-way set associative with 32-byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has a latency of 0.6 ns while a kbit comparator has a latency of k/10 ns. The hit latency of the set associative
organization is h1 while that of the direct mapped one is h2.
The value of h2 is:

(A) 2.4 ns
(B) 2.3
(C) 1.8
(D) 1.7

MCQ (Single Correct Answer)

GATE CSE 2006

A CPU has a 32 KB direct mapped cache with 128-byte block size. Suppose A is a two dimensional array of size 512×512 with elements that occupy 8-bytes each. Consider the following two C code segments, P1 and P2.

P1 and P2 are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by P1 be M1 and that for P2 be M2 .

The value of M1 is:

1.0

2.20482

3.16384

4.262144


```
for (i=0; i<512; i++) {
    for (j=0; j<512; j++) {
        x += A[i][j];
    }
}
```

```
for (i=0; i<512; i++) {
    for (j=0; j<512; j++) {
        x += A[j][i];
    }
}
```

MCQ (Single Correct Answer)

GATE CSE 2006

A CPU has a 32 KB direct mapped cache with 128-byte block size. Suppose A is a twodimensional array of size 512×512 with elements that occupy 8-bytes each. Consider the following two C code segments, P1 and P2.

P1 and P2 are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by P1 be M1 and that for P2 be M2 .

The value of the ratio M1/M2 is:

(A) 0

(B) 1/16

(C) 1/8

(D) 16


```
for (i=0; i<512; i++) {
    for (j=0; j<512; j++) {
        x += A[i][j];
    }
}

for (i=0; i<512; i++) {
    for (j=0; j<512; j++) {
        x += A[j][i];
    }
}
```

MCQ (Single Correct Answer)

GATE CSE 2007

Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50 × 50 two-dimensional array of bytes is stored in the main memory starting from memory location 1100H. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

How many data cache misses will occur in total?

A) 40

B) 50

C) 56

D) 59

MCQ (Single Correct Answer)

GATE CSE 2007

Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50 × 50 two-dimensional array of bytes is stored in the main memory starting from memory location 1100H. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

Which of the following lines of the data cache will be replaced by new blocks in accessing the array for the second time?

(A) line 4 to line 11

(B) line 4 to line 12

(C) line 0 to line 7

(D) line 0 to line 8

MCQ (Single Correct Answer)

GATE CSE 2008

For inclusion to hold between two cache levels L1 and L2 in a multi-level cache hierarchy, which of the following are necessary?

I. L1 must be a write-through cache

II. L2 must be a write-through cache

III. The associativity of L2 must be greater than that of L1

IV. The L2 cache must be at least as large as the L1 cache

A) IV only

B) I and IV only

C) I, III and IV only

D) I, II, III and IV

MCQ (Single Correct Answer)

GATE CSE 2008

Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

The size of double is 8 Bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

The total size of the tags in the cache directory is

(A) 32 Kbits
(B) 34 Kbits
(C) 64 Kbits
(D) 68 Kbits

```
double ARR[1024][1024];
int i, j;

// Initialize array ARR to 0.0
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

MCQ (Single Correct Answer)

GATE CSE 2008

Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

The size of double is 8 Bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

Which of the following array elements has the same cache index as ARR[0][0]?

(A) ARR[0][4]
(B) ARR[4][0]
(C) ARR[0][5]
(D) ARR[5][0]

```
double ARR[1024][1024];
int i, j;

// Initialize array ARR to 0.0
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

MCQ (Single Correct Answer)

GATE CSE 2008

Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

The size of double is 8 Bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

The cache hit ratio for this initialization loop is

(A) 0%
(B) 25%
(C) 50%
(D) 75%


```
double ARR[1024][1024];
int i, j;

// Initialize array ARR to 0.0
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

MCQ (Single Correct Answer)

GATE CSE 2009

Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order:

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155.

Which one of the following memory block will NOT be in cache if LRU replacement policy is used?

A) 3

B) 8

C) 129

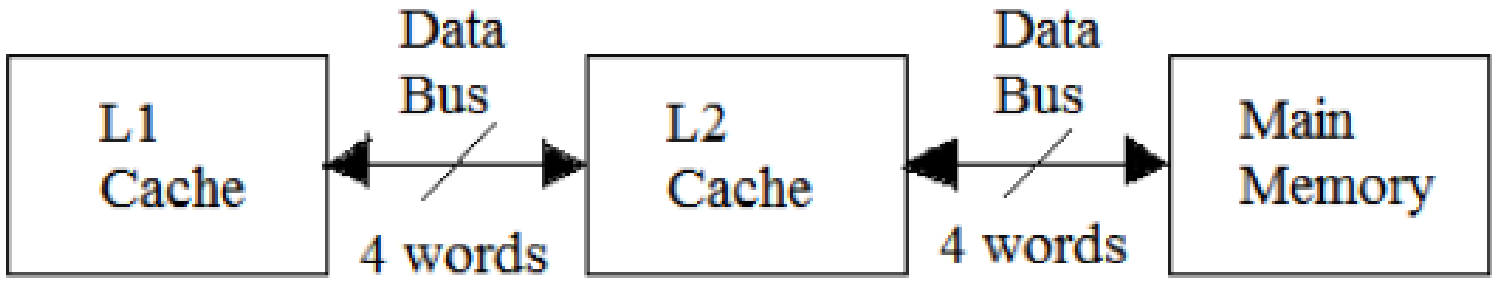
D) 216

MCQ (Single Correct Answer)

GATE CSE 2010

A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds. 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively. When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer?

A) 2 nanoseconds
B) 20 nanoseconds
C) 22 nanoseconds
D) 88 nanoseconds

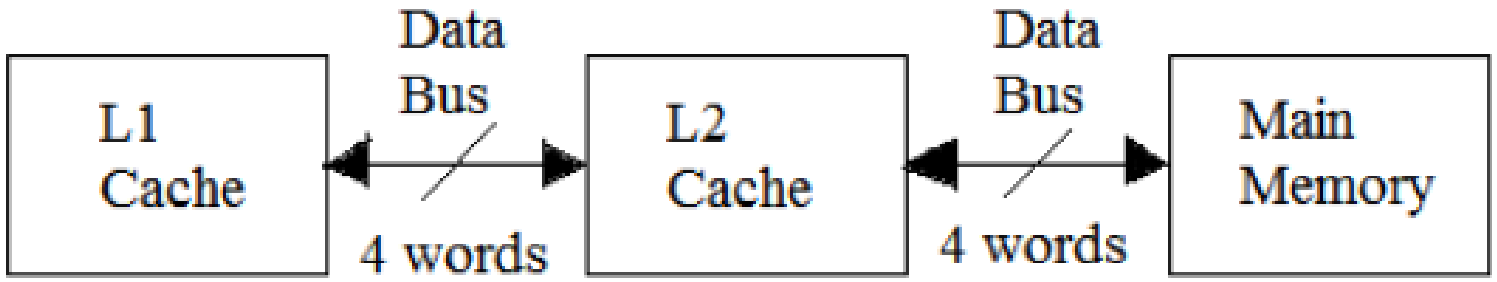


MCQ (Single Correct Answer)

GATE CSE 2010

A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds. 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively. When there is a miss in both L1 cache and L2 cache, first a block is transferred from main memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers?

(A) 222 nanoseconds
(B) 888 nanoseconds
(C) 902 nanoseconds
(D) 968 nanoseconds



MCQ (Single Correct Answer)

GATE CSE 2011

An 8KB direct-mapped write-back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprising of the following.

1 Valid bit

1 Modified bit

As many bits as the minimum needed to identify the memory block mapped in the cache. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

(A) 4864 bits

(B) 6144 bits

(C) 6656 bits

(D) 5376 bits

MCQ (Single Correct Answer)

GATE CSE 2012

A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The number of bits in the tag field of an address is

A) 11

B) 14

C) 16

D) 27

MCQ (Single Correct Answer)

GATE CSE 2012

A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The size of the cache tag directory is

(A) 160 Kbits

(B) 136 bits

(C) 40 Kbits

(D) 32 bits

MCQ (Single Correct Answer)

GATE CSE 2013

A RAM chip has a capacity of 1024 words of 8 bits each (1K × 8). The number of 2 × 4 decoders with enable line needed to construct a 16K × 16 RAM from 1K × 8 RAM is

A) 4
B) 5
C) 6
D) 7

Numerical

GATE CSE 2014 Set 2

A 4-way set-associative cache memory unit with a capacity of 16KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB.GB. The number of bit for the TAG field is _____.

MCQ (Single Correct Answer)

GATE CSE 2014 Set 2

In designing a computer's cache system, the cache block (or cache line) size is an important parameter. Which one of the following statements is correct in this context?

A) A smaller block size implies better spatial locality

B) A smaller block size implies a smaller cache tag and hence lower cache tag overhead

C) A smaller block size implies a larger cache tag and hence lower cache hit time

D) A smaller block size incurs a lower cache miss penalty

MCQ (Single Correct Answer)

GATE CSE 2014 Set 2

If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?

A) Width of tag comparator

B) Width of set index decoder

C) Width of way selection multiplexor

D) Width of processor to main memory data bus

Numerical

GATE CSE 2014 Set 3

The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is _____.

Numerical

GATE CSE 2014 Set 2

Consider a main memory system that consists of 8 memory modules attached to the system bus, which is one word wide. When a write request is made, the bus is occupied for 100 nanoseconds (ns) by the data, address, and control signals. During the same 100 ns, and for 500 ns thereafter, the addressed memory module executes one cycle accepting and storing the data. The (internal) operation of different memory modules may overlap in time, but only one request can be on the bus at any time. The maximum number of stores (of one word each) that can be initiated in 1 millisecond is _____

Numerical

GATE CSE 2016 Set 2

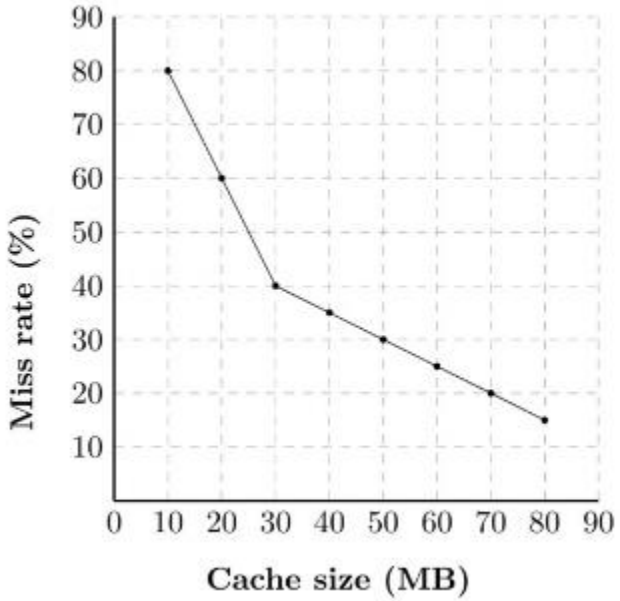
The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is _____ bits.

Numerical

GATE CSE 2017 Set 1

A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure. The latency to read a block from the cache is 1 ms and to read a block from the disk is 10 ms. Assume that the cost of checking whether a block exists in the cache is negligible. Available cache sizes are in multiples of 10 MB.

The smallest cache size required to ensure an average read latency of less than 6 ms is _____ MB.



Numerical

GATE CSE 2017 Set 1

A cache memory unit with capacity of N words and block size of B words is to be designed. If it is designed as direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, the length of the TAG field is _____ bits.

Numerical

GATE CSE 2017 Set 1

Consider a 2-way set associative cache with 256 blocks and uses LRU replacement, Initially the cache is empty. Conflict misses are those misses which occur due the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of accesses to memory blocks

(0,128,256,128,0,128,256,128,1,129,257,129,1,129,257,129)

is repeated 10 times. The number of conflict misses experienced by the cache is _____.

Numerical

GATE CSE 2017 Set 2

The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

The read access time of main memory in 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the writeback policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% od memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is _____

Cache	Read access time (in nanoseconds)	Hit ratio
I-cache	2	0.8
D-cache	2	0.9
*L*2-cache	8	0.9

Numerical

GATE CSE 2017 Set 2

Consider a machine with byte addressable memory of 2^{32} bytes divided into blocks of size 32 bytes. Assume a direct mapped cache having 512 cache lines is used with this machine. The size of tag field in bits is _____

MCQ (Single Correct Answer)

GATE CSE 2017 Set 2

In a two-level cache system, the access times of L_1 and L_2 1 and 8 clock cycles, respectively. The miss penalty from the L_2 cache to main memory is 18 clock cycles. The miss rate of L_1 cache is twice that of L_2. The average memory access time(AMAT) of this cache system is 2 cycles. The miss rates of L_1 and L_2 respectively are:

(A) 0.111 and 0.056

(B) 0.056 and 0.111

(C) 0.0892 and 0.1784

(D) 0.1784 and 0.0892

MCQ (Single Correct Answer)

GATE CSE 2018

The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K-way set-associative cache memory, the length (in number of bits) of the tag field is

(A) $P - N - \log_2 K$

(B) $P - N + \log_2 K$

(C) $P - N - M - W - \log_2 K$

(D) $P - N - M - W + \log_2 K$

Numerical

GATE CSE 2019

A certain processor deploys a single-level cache. The cache block size is 8 words and the word size is 4 bytes. The memory system uses a 60 MHz clock. To service a cache-miss, the memory controller first takes 1 cycle to accept the starting address of the block, it then takes 3 cycles to fetch all the eight words of the block, and finally transmits the words of the requested block at the rate of 1 word per cycle.

The maximum bandwidth for the memory system when the program running on the processor issues a series of read operations is _____ $\times 10^6$ bytes/sec.

MCQ (Single Correct Answer)

GATE CSE 2020

A computer system with a word length of 32 bits has a 16 MB byte- addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.A

Which one of the following is TRUE ?

A1 = 0x42C8A4

A2 = 0x546888

A3 = 0x6A289C

A4 = 0x5E4880

(A) A1 and A4 are mapped to different cache sets.

(B) A2 and A3 are mapped to the same cache set.

(C) A3 and A4 are mapped to the same cache set.

(D) A1 and A3 are mapped to the same cache set.

MCQ (Single Correct Answer)

GATE CSE 2000

Comparing the time T1 taken for a single instruction on a pipelined CPU with time T2 taken on a non pipelined but identical CPU, we can say that

A) T1 <= T2

B) T1 >= T2

C) T1 < T2

D) T1 is T2 plus the time taken for one instruction fetch cycle

MCQ (Single Correct Answer)

GATE CSE 2003

For a pipelined CPU with a single ALU, consider the following situations

1. The j + 1-st instruction uses the result of the j-th instruction as an operand
2. The execution of a conditional jump instruction
3. The j-th and j + 1-st instructions require the ALU at the same time

Which of the above can cause a hazard ?

(A) 1 and 2 only
(B) 2 and 3 only
(C) 3 only
(D) All of above

MCQ (Single Correct Answer)

GATE CSE 2012

Register renaming is done in pipelined processors

A) as an alternative to register allocation at compile time

B) for efficient access to function parameters and local variables

C) to handle certain kinds of hazards

D) as part of address translation

Numerical

GATE CSE 2020

If there are m input lines n output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of m+n is _____ .

MCQ (Single Correct Answer)

GATE CSE 2002

The performance of a pipelined processor suffers if

A) The pipeline stages have different delays

B) Consecutive instructions are depend on each other

C) The pipeline stages share single hardware resources

D) All of the above

MCQ (Single Correct Answer)

GATE CSE 2004

A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

(A) 120.4 microseconds

(B) 160.5 microseconds

(C) 165.5 microseconds

(D) 590.0 microseconds

MCQ (Single Correct Answer)

GATE CSE 2005

A 5 stage pipelined CPU has the following sequence of stages:

What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of I1 ?

A) 8
B) 10
C) 12
D) 15

```
IF – Instruction fetch from instruction memory,
RD – Instruction decode and register read,
EX – Execute: ALU operation for data and address computation,
MA – Data memory access - for write access, the register read
     at RD stage is used,
WB – Register write back.
Consider the following sequence of instructions:
I1 : L R0, 1oc1;         R0 <= M[1oc1]
I2 : A R0, R0;            R0 <= R0 + R0
I3 : S R2, R0;            R2 <= R2 - R0
Let each stage take one clock cycle.
```

MCQ (Single Correct Answer)

GATE CSE 2006

A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction
computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is:

A) 1.0 second
B) 1.2 seconds
C) 1.4 seconds
D) 1.6 seconds

MCQ (Single Correct Answer)

GATE CSE 2007

Consider a pipelined processor with the following four stages:

IF: Instruction Fetch ID: Instruction Decode and Operand Fetch EX: Execute WB: Write Back

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage dependson the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to

```
ADD R2, R1, R0        R2 <- R0 + R1
MUL R4, R3, R2        R4 <- R3 * R2
SUB R6, R5, R4        R6 <- R5 - R4
```

(A) 7
(B) 8
(C) 10
(D) 14

MCQ (Single Correct Answer)

GATE CSE 2008

The use of multiple register windows with overlap causes a reduction in the number of memory accesses for

1. Function locals and parameters
2. Register saves and restores
3. Instruction fetches

A) 1 only

B) 2 only

C) 3 only

D) 1,2 and 3

MCQ (Single Correct Answer)

GATE CSE 2008

Which of the following are NOT true in a pipelined processor?

1. Bypassing can handle all RAW hazards
2. Register renaming can eliminate all register carried WAR hazards
3. Control hazard penalties can be eliminated by dynamic branch prediction.

A) 1 and 2 only
B) 1 and 3 only
C) 2 and 3 only
D) 1,2 and 3

MCQ (Single Correct Answer)

GATE CSE 2008

Delayed branching can help in the handling of control hazards
The following code is to run on a pipelined
processor with one branch delay slot:

Which of the instructions I1, I2, I3 or I4 can legitimately occupy the delay slot
without any other program modification?

A) I1
B) I2
C) I3
D) I4


```
I1: ADD R2←R7+R8

I2 : SUB R4← R5-R6

I3 : ADD R1← R2+R3

I4 : STORE Memory [R4]←[R1]

BRANCH to Label if R1== 0
```

MCQ (Single Correct Answer)

GATE CSE 2008

In an instruction execution pipeline, the earliest that the data TLB (Translation Look aside Buffer) can be accessed is

A) Before effective address calculation has started

B) During effective address calculation

C) After effective address calculation has completed

D)After data cache lookup has completed

MCQ (Single Correct Answer)

GATE CSE 2009

Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

	S_1	S_2	S_3	S_4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?
For (i=1 to 2) {I1; I2; I3; I4;}

(A) 16
(B) 23
(C) 28
(D) 30

MCQ (Single Correct Answer)

GATE CSE 2010

A 5-stage pipelined processor has Instruction Fetch(IF),Instruction Decode(ID),Operand Fetch(OF),Perform Operation(PO)and Write Operand(WO)stages.The IF,ID,OF and WO stages take 1 clock cycle each for any instruction.The PO stage takes 1 clock cycle for ADD and SUB instructions,3 clock cycles for MUL instruction,and 6 clock cycles for DIV instruction respectively.Operand forwarding is used in the pipeline.What is the number of clock cycles needed to execute the following sequence of instructions?

A) 13
B) 15
C) 17
D) 19

Instruction	Meaning of instruction
I0 :MUL R2 ,R0 ,R1	R2 ¬ R0 *R1
I1 :DIV R5 ,R3 ,R4	R5 ¬ R3/R4
I2 :ADD R2 ,R5 ,R2	R2 ¬ R5+R2
I3 :SUB R5 ,R2 ,R6	R5 ¬ R2-R6

MCQ (Single Correct Answer)

GATE CSE 2011

Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure:

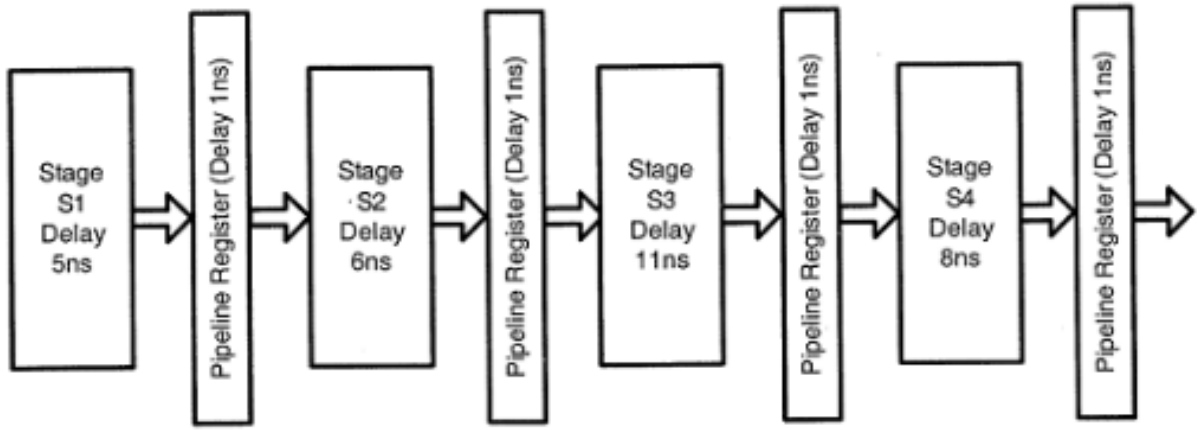
What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

A) 4.0

B) 2.5

C) 1.1

D) 3.0



MCQ (Single Correct Answer)

GATE CSE 2013

Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3, …, I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

A) 132

B) 165

C) 176

D) 328

Numerical

GATE CSE 2014 Set 1

Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is

MCQ (Single Correct Answer)

GATE CSE 2014 Set 3

Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

Which processor has the highest peak clock frequency?

(A) P1

(B) P2

(C) P3

(D) P4

```
P1: Four-stage pipeline with stage
    latencies 1 ns, 2 ns, 2 ns, 1 ns.
P2: Four-stage pipeline with stage
    latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.
P3: Five-stage pipeline with stage
    latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.
P4: Five-stage pipeline with stage
    latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.
```

Numerical

GATE CSE 2014 Set 3

An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is _____.

Numerical

GATE CSE 2015 Set 1

Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is_____.

Numerical

GATE CSE 2015 Set 2

Consider the sequence of machine instructions given below:

In the above sequence, R0 to R8 are general purpose registers. In the instructions shown, the first register stores the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operation (PO) and (4) Write back the Result (WB). The IF, OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycles taken for the execution of the above sequence of instructions is _____

```
MUL R5, R0, R1
DIV R6, R2, R3
ADD R7, R5, R6
SUB R8, R7, R4
```

Numerical

GATE CSE 2015 Set 3

Consider the following reservation table for a pipeline having three stages S1, S2 and S3.
The minimum average latency (MAL) is _____

Time →	1	2	3	4	5
S_1	X				X
S_2		X		X	
S_3			X		

MCQ (Single Correct Answer)

GATE CSE 2015 Set 3

Consider the following code sequence having five instructions I1 to I5. Each of these instructions has the following format.
OP Ri, Rj, Rk

where operation OP is performed on contents of registers Rj and Rk and the result is stored in register Ri.(A) P1
Consider the following three statements:

S1: There is an anti-dependence between instructions I2 and I5.
S2: There is an anti-dependence between instructions I2 and I4.
S3: Within an instruction pipeline an anti-dependence always creates one or more stalls.
Which one of above statements is/are correct?
A) Only S1 is true
B) Only S2 is true
C) Only S1 and S2 are true
D) Only S2 and S3 are true

```
I1 : ADD R1, R2, R3
I2 : MUL R7, R1, R3
I3 : SUB R4, R1, R5
I4 : ADD R3, R2, R4
I5 : MUL R7, R8, R9
```

Numerical

GATE CSE 2016 Set 2

Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units U_F and U_G, respectively. Given two instances of U_F and two instances of U_G, it is required to implement the computation F(G(Xi)) for 1 <= i <= 10. ignoring all other delays, the minimum time required to complete this computation is _____ nanoseconds

Numerical

GATE CSE 2016 Set 2

Consider a 3 GHz (gigahertz) processor with a three-stage pipeline and stage latencies v1, v2, and v3 such that v1 = 3v2/4 = 2v3. If the longest pipeline stage is split into two pipeline stages of equal latency, the new frequency is _____ GHz, ignoring delays in the pipeline registers

Numerical

GATE CSE 2017 Set 1

Instruction execution in a processor is divided into 5 stages. *Instruction Fetch(IF), Instruction Decode (ID), Operand Fetch(OF), Execute(EX), and Write Back(WB),* These stages take 5,4,20, 10 and 3 nanoseconds (ns) respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns. Two pipelined implementations of the processor are contemplated:

(i) a naïve pipeline implementation (NP) with 5 stages and
(ii) an efficient pipeline (EP) where the OF stage id divided into stages OF1 and OF2 with execution times of 12 ns and 8 ns respectively.
The speedup (correct to two decimals places) achieved by EP over NP in executing 20 independent instructions with no hazards is _____.

Numerical

GATE CSE 2018

The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.
The number of clock cycles required for completion of execution of the sequence of instruction is _____ .

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Numerical

GATE CSE 2020

Consider a non-pipelined processor operating at 2.5 GHz. It takes 5 clock cycles to complete an instruction. You are going to make a 5-stage pipeline out of this processor. Overheads associated with pipelining force you to operate the pipelined processor at 2 GHz. In a given program, assume that 30% are memory instructions, 60% are ALU instructions and the rest are branch instructions. 5% of the memory instructions cause stalls of 50 clock cycles each due to cache misses and 50% of the branch instructions cause stalls of 2 cycles each. Assume that there are no stalls associated with the execution of ALU instructions. For this program, the speedup achieved by the pipelined processor over the non-pipelined processor (round off to 2 decimal places) is _____.

MCQ (Single Correct Answer)

GATE CSE 1995

Which of the following statements is true?

1.ROM is a Read/Write memory

2.PC points to the last instruction that was executed

3.Stack works on the principle of LIFO

4.All instructions affect the flags

MCQ (Single Correct Answer)

GATE CSE 1998

Which of the following addressing modes permits relocation without any change whatsoever in the code?

A) Indirect addressing

B) Indexed addressing

C) Base register addressing

D) PC relative addressing

MCQ (Single Correct Answer)

GATE CSE 2000

The most appropriate matching for the following pairs

(A) X-3, Y-2, Z-1
(B) X-I, Y-3, Z-2
(C) X-2, Y-3, Z-1
(D) X-3, Y-l, Z-2

X: Indirect addressing	1 : Loops
Y: Immediate addressing	2 : Pointers
Z: Auto decrement addressing	3: Constants

MCQ (Single Correct Answer)

GATE CSE 2002

Which of the following is not a form of memory?

A) Instruction cache

B) Instruction register

C) Instruction opcode

D) Translation look aside buffer

MCQ (Single Correct Answer)

GATE CSE 2002

In absolute addressing mode

A) the operand is inside the instruction

B) the address of the operand is inside the instruction

C) the register containing the address of the operand is specified inside the instruction

D) the location of the operand is implicit

MCQ (Single Correct Answer)

GATE CSE 2004

Which of the following addressing modes are suitable for program relocation at run time ?
(i) Absolute addressing (ii) Based addressing (iii) Relative addressing (iv) Indirect addressing

(A) (i) and (iv)
(B) (i) and (ii)
(C) (ii) and (iii)
(D) (i), (ii) and (iv)

MCQ (Single Correct Answer)

GATE CSE 2002

Which of the following is not a form of memory?

(A) instruction cache

(B) instruction register

(C) instruction opcode

(D) translation lookaside buffer

MCQ (Single Correct Answer)

GATE CSE 2006

A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

(A) 400

(B) 500

(C) 600

(D) 700

MCQ (Single Correct Answer)

GATE CSE 2015 Set 1

For computers based on three-address instruction formats, each address field can be used to specify which of the following:

(S1) A memory operand

(S2) A processor register

(S3) An implied accumulator register

A) Either S1 or S2

B) Either S2 or S3

C) Only S2 and S3

D) All of S1, S2 and S3

Numerical

GATE CSE 2016 Set 2

A processor has 40 distinct instructions and 24 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is _____ .

MCQ (Single Correct Answer)

GATE CSE 2017 Set 1

Consider the C struct defines below:

```
struct data {
    int marks [100] ;
    char grade;
    int cnumber;
};

struct data student;
```

The base address of student is available in register R1. The field student.grade can be accessed efficiently using

(A) Post-increment addressing mode. (R1)+

(B) Pre-decrement addressing mode, -(R1)

(C) Register direct addressing mode, R1

(D) Index addressing mode, X(R1), where X is an offset represented in 2's complement 16-bit representation.

MCQ (Single Correct Answer)

GATE CSE 2018

The following are some events that occur after a device controller issues an interrupt while process L is under execution.

(P) The processor pushes the process status of L onto the control stack.

(Q) The processor finishes the execution of the current instruction.

(R) The processor executes the interrupt service routine.

(S) The processor pops the process status of L from the control stack.

(T) The processor loads the new PC value based on the interrupt.

Which of the following is the correct order in the which the events above occur?

(A) QPTRS

(B) PTRSQ

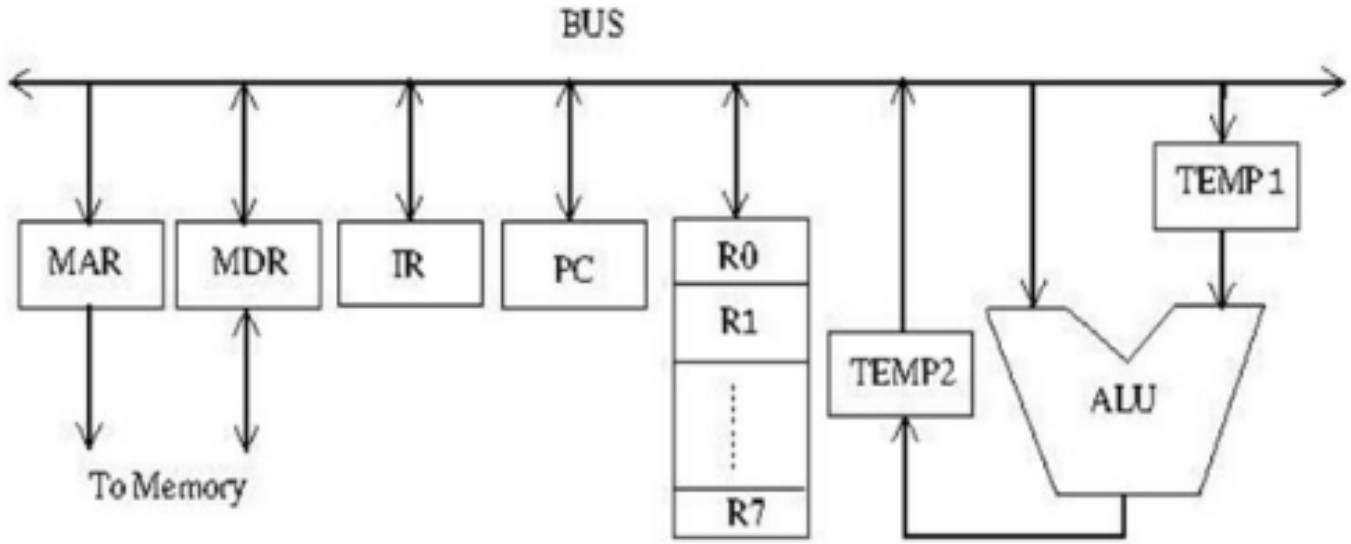
(C) TRPQS

(D) QTPRS

MCQ (Single Correct Answer)

GATE CSE 2020

Consider the following data path diagram.



Consider an instruction:

R0 ← R1 + R2

The following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts r and w indicate read and write operations, respectively.

1.$R2_r$, $TEMP1_r$, ALU_{add}, $TEMP2_w$
2.$R1_r$, $TEMP1_w$
3.PC_r, MAR_w, MEM_r
4.$TEMP2_r$, $R0_w$
5.MDR_r, IR_w

Which one of the following is the correct order of execution of the above steps ?

(A) 2, 1, 4, 5, 3
(B) 1, 2, 4, 3, 5
(C) 3, 5, 2, 1, 4
(D) 3, 5, 1, 2, 4

MCQ (Single Correct Answer)

GATE CSE 2001

Which is the most appropriate match for the items in the first column with the items in the second column

X. Indirect Addressing	I. Array implementation
Y. Indexed Addressing	II. Writing re-locatable code
Z. Base Register Addressing	III. Passing array as parameter

(A) (X, III) (Y, I) (Z, II)
(B) (X, II) (Y, III) (Z, I)
(C) (X, III) (Y, II) (Z, I)
(D) (X, I) (Y, III) (Z, II)

MCQ (Single Correct Answer)

GATE CSE 2003

Consider the following assembly language program for a hypothetical processor. A, B, and C are 8 bit registers. The meanings of various instructions are shown as comments.

If the initial value of register A is A0 the value of register B after the program execution will be

(A) the number of 0 bits in A0

(B) the number of 1 bits in A0

(C) A0

(D) 8

```
      MOV B, #0     ;  B ← 0
      MOV C, #8     ;  C ← 8
Z:    CMP C, #0     ;  compare C with 0
      JZ X          ;  jump to X if zero flag is set
      SUB C, #1     ;  C ← C − 1
      RRC A, #1     ;  right rotate A through carry by one bit. Thus:
                    ;  If the initial values of A and the carry flag are a7...a0 and
                    ;  c0 respectively, their values after the execution of this
                    ;  instruction will be c0a7...a1 and a0 respectively.
      JC Y          ;  jump to Y if carry flag is set
      JMP Z         ;  jump to Z
Y:    ADD B, #1     ;  B ← B + 1
      JMP Z         ;  jump to Z
X:                  ;
```

MCQ (Single Correct Answer)

GATE CSE 2003

Consider the following assembly language program for a hypothetical processor. A, B, and C are 8 bit registers. The meanings of various instructions are shown as comments.

```
      MOV B, #0     ;  B ← 0
      MOV C, #8     ;  C ← 8
Z:    CMP C, #0     ;  compare C with 0
      JZ X          ;  jump to X if zero flag is set
      SUB C, #1     ;  C ← C − 1
      RRC A, #1     ;  right rotate A through carry by one bit. Thus:
                    ;  If the initial values of A and the carry flag are a7...a0 and
                    ;  c0 respectively, their values after the execution of this
                    ;  instruction will be c0a7...a1 and a0 respectively.
      JC Y          ;  jump to Y if carry flag is set
      JMP Z         ;  jump to Z
Y:    ADD B, #1     ;  B ← B + 1
      JMP Z         ;  jump to Z
X:                  ;
```

Which of the following instructions when inserted at location X will ensure that the value of register A after program execution is the same as its initial value ?

(A) RRC A, #

(B) NOP ; no operation

(C) LRC A, # 1 ; left rotate A through carry flag by one bit

(D) ADD A, # 1

MCQ (Single Correct Answer)

GATE CSE 2004

Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3.

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

(A) 1007
(B) 1020
(C) 1024
(D) 1028

Instruction	Operation	Instruction Size(in words)
MOV R1,5000;	R1 ¬ Memory[5000]	2
MOV R2, (R1);	R2 ¬ Memory[(R1)]	1
ADD R2, R3;	R2 ¬ R2 + R3	1
MOV 6000, R2;	Memory [6000] ¬ R2	2
HALT	Machine halts	1

MCQ (Single Correct Answer)

GATE CSE 2004

Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3.

Let the clock cycles required for various operations be as follows: Register to/ from memory transfer: 3 clock cycles ADD with both operands in register : 1 clock cycle Instruction fetch and decode : 2 clock cycles per word The total number of clock cycles required to execute the program is

(A) 29
(B) 24
(C) 23
(D) 20

Instruction	Operation	Instruction Size(in words)
MOV R1,5000;	R1 ¬ Memory[5000]	2
MOV R2, (R1);	R2 ¬ Memory[(R1)]	1
ADD R2, R3;	R2 ¬ R2 + R3	1
MOV 6000, R2;	Memory [6000] ¬ R2	2
HALT	Machine halts	1

MCQ (Single Correct Answer)

GATE CSE 2005

Consider a three word machine instruction
ADD A[R0], @ B
The first operand (destination) “A [R0]” uses indexed addressing mode with R0 as the index register. The second operand (source) “@ B” uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).
The number of memory cycles needed during the execution cycle of the instruction is
(A) 3
(B) 4
(C) 5
(D) 6

MCQ (Single Correct Answer)

GATE CSE 2005

Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

1 A[1] = B[J]; a Indirect addressing
2 while [*A++]; b Indexed, addressing
3 int temp = *x; c Autoincrement

(A) (1, c), (2, b), (3, a)
(B) (1, a), (2, c), (3, b)
(C) (1, b), (2, c), (3, a)
(D) (1, a), (2, b), (3, c)

MCQ (Single Correct Answer)

GATE CSE 2007

In a simplified computer the instructions are:

The computer has only two registers, and OP is either ADD or SUB. Consider the following basic block:

t1=a+b
t2=*c*+*d*
t3=*e*–*t*2
t4=t1–t3

OP R_j, R_i	- Performs R_j OP R_i and stores the result in register R_i.
OP m,R_i	- Performs *val* OP R_i and stores the result in R_i. *val* denotes the content of memory location *m*.
MOV *m*, R_i	- Moves the content of memory location *m* to register R_i.
MOV R_i, *m*	- Moves the content of register R_i to memory location *m*.

Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

(A) 2
(B) 3
(C) 5
(D) 6

MCQ (Single Correct Answer)

GATE CSE 2007

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal. Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is:

(A) 10
(B) 11
(C) 20
(D) 21

	Instruction	Operation	Instruction size (no.of words)
	MOV R1, (3000)	R1 ← m[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2, R1	R2 ← R1 + R2	1
	MOV (R3), R2	M[R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

MCQ (Single Correct Answer)

GATE CSE 2007

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

Consider the data given in above question. Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

(A) 100
(B) 101
(C) 102
(D) 110

	Instruction	Operation	Instruction size (no.of words)
	MOV R1, (3000)	R1 ← m[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2, R1	R2 ← R1 + R2	1
	MOV (R3), R2	M[R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

MCQ (Single Correct Answer)

GATE CSE 2007

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

Consider the data given in above questions. Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on to the stack?

(A) 1005
(B) 1020
(C) 1024
(D) 1040

	Instruction	Operation	Instruction size (no.of words)
	MOV R1, (3000)	R1 ← m[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2, R1	R2 ← R1 + R2	1
	MOV (R3), R2	M[R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

MCQ (Single Correct Answer)

GATE CSE 2008

Which of the following must be true for the RFE (Return from Exception) instruction on a general purpose processor?

I. It must be a trap instruction

II. It must be a privileged instruction

III. An exception cannot be allowed to occur during execution of an RFE instruction

(A) I only

(B) II only

(C) I and II only

(D) I, II and III only

MCQ (Single Correct Answer)

GATE CSE 2008

Which of the following is/are true of the auto-increment addressing mode?

I. It is useful in creating self-relocating code.

II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation.

III. The amount of increment depends on the size of the data item accessed.

(A) I only

(B) II only

(C) III Only

(D) II and III only

MCQ (Single Correct Answer)

GATE CSE 2008

For all delayed conditional branch instructions, irrespective of whether the condition evaluate true or false,

A) the instruction following the conditional branch instruction in memory is executed

B) the first instruction in the fall through path is executed

C) the first instruction in the taken path is executed

D) the branch takes longer to execute than any other instruction

MCQ (Single Correct Answer)

GATE CSE 2011

On a non-pipelined sequential processor, a program segment, which is a part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

Assume that each statement in this program is equivalent to machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.
The designer of the system also has an alternate approach of using DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.
What is the approximate speedup when the DMA controller based design is used in place of the interrupt driven program based input-output?

(A) 3.4
(B) 4.4
(C) 5.1
(D) 6.7

```
      Initialize the address register
      Initialize the count to 500
LOOP: Load a byte from device
      Store in memory at address given by address register
      Increment the address register
      Decrement the count
      If count != 0 go to LOOP
```

MCQ (Single Correct Answer)

GATE CSE 2011

Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?

(A) Immediate Addressing
(B) Register Addressing
(C) Register Indirect Scaled Addressing
(D) Base Indexed Addressing

Numerical

GATE CSE 2014 Set 1

A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____.

Numerical

GATE CSE 2014 Set 1

Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P1. If the clock frequency of P1 is 1GHz, then the clock frequency of P2 (in GHz) is _____.

MCQ (Single Correct Answer)

GATE CSE 2015 Set 2

Consider a processor with byte-addressable memory. Assume that all registers, including Program Counter (PC) and Program Status Word (PSW), are of size 2 bytes. A stack in the main memory is implemented from memory location $(0100)_{16}$ and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is $(016E)_{16}$. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack.
- Store the value of PSW register in the stack.
- Load the starting address of the subroutine in PC.

The content of PC just before the fetch of a CALL instruction is $(5FA0)_{16}$. After execution of the CALL instruction, the value of the stack pointer is

(A) $(016A)_{16}$
(B) $(016C)_{16}$
(C) $(0170)_{16}$
(D) $(0172)_{16}$

MCQ (Single Correct Answer)

GATE CSE 2015 Set 3

Consider the following code sequence having five instructions I1 to I5. Each of these instructions has the following format.

OP Ri, Rj, Rk

where operation OP is performed on contents of registers Rj and Rk and the result is stored in register Ri.

I1 : ADD R1, R2, R3

I2 : MUL R7, R1, R3

I3 : SUB R4, R1, R5

I4 : ADD R3, R2, R4

I5 : MUL R7, R8, R9

Consider the following three statements:

S1: There is an anti-dependence between instructions I2 and I5. S2: There is an anti-dependence between instructions I2 and I4. S3: Within an instruction pipeline an anti-dependence always creates one or more stalls.

Which one of above statements is/are correct?

(A) Only S1 is true

(B) Only S2 is true

(C) Only S1 and S2 are true

(D) Only S2 and S3 are true

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Numerical

GATE CSE 2016 Set 2

Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____

Numerical

GATE CSE 2017 SET 1

Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____

Numerical

GATE CSE 2018

A processor has 16 integer registers (R0, R1, … , R15) and 64 floating point registers (F0, F1, … , F63). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type 4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F).
The maximum value of N is _____ .

Numerical

GATE CSE 2020

A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then the maximum number of distinct R-type opcodes is _____.

Numerical

GATE CSE 2002

A device employing INTR line for device interrupt puts the CALL instruction on the data bus while

A) (INTR)' is active
B) HOLD is active
C) READY is active
D) None of these

MCQ (Single Correct Answer)

GATE CSE 2018

Consider the following processor design characteristics.

I. Register-to-register arithmetic operations only

II. Fixed-length instruction format

III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

(A) I and II only

(B) II and III only

(C) I and III only

(D) I, II and III

Numerical

GATE CSE 2020

A multiplexer is placed between a group of 32 registers and an accumulator to regulate data movement such that at any given point in time the content of only one register will move to the accumulator. The number of select lines needed for the multiplexer is _____ .

Numerical

GATE CSE 1997

A micro instruction into be designed to specify

a. none or one of the three micro operations of one kind and

b. none or upto six micro operations of another kind

The minimum number of bits in the micro-instruction is

A) 9

B) 5

C) 8

D) None of the above

MCQ (More than One Correct Answer)

GATE CSE 1999

The main difference(s) between a CISC and a RISC processor is/are that a USC processor typically:

a) has fewer instructions
b) has fewer addressing modes
c) has more registers
d) is easier to implement using hardwired control logic

(A) a and b
(B) b and c
(C) a and d
(D) a, b, c and d

MCQ (Single Correct Answer)

GATE CSE 2001

Arrange the following configurations for CPU in decreasing order of operating speeds;
Hardwired Control, vertical microprogramming, horizontal microprogramming
(A) Hardwired control, Vertical microprogramming, Horizontal microprogramming.
(B) Hardwired control, Horizontal microprogramming, Vertical microprogramming.
(C) Horizontal microprogramming, Vertical microprogramming, Hardwired control.
(D) Vertical microprogramming, Horizontal microprogramming, Hardwired control.

MCQ (Single Correct Answer)

GATE CSE 2001

Consider the following data path of a simple non-pilelined CPU. The registers A, B, A1, A2, MDR, the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size 8 × (2:1) and the DEMUX is of size 8 × (1:2). Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally. The CPU instruction "push r", where = A or B, has the specification

M [SP]

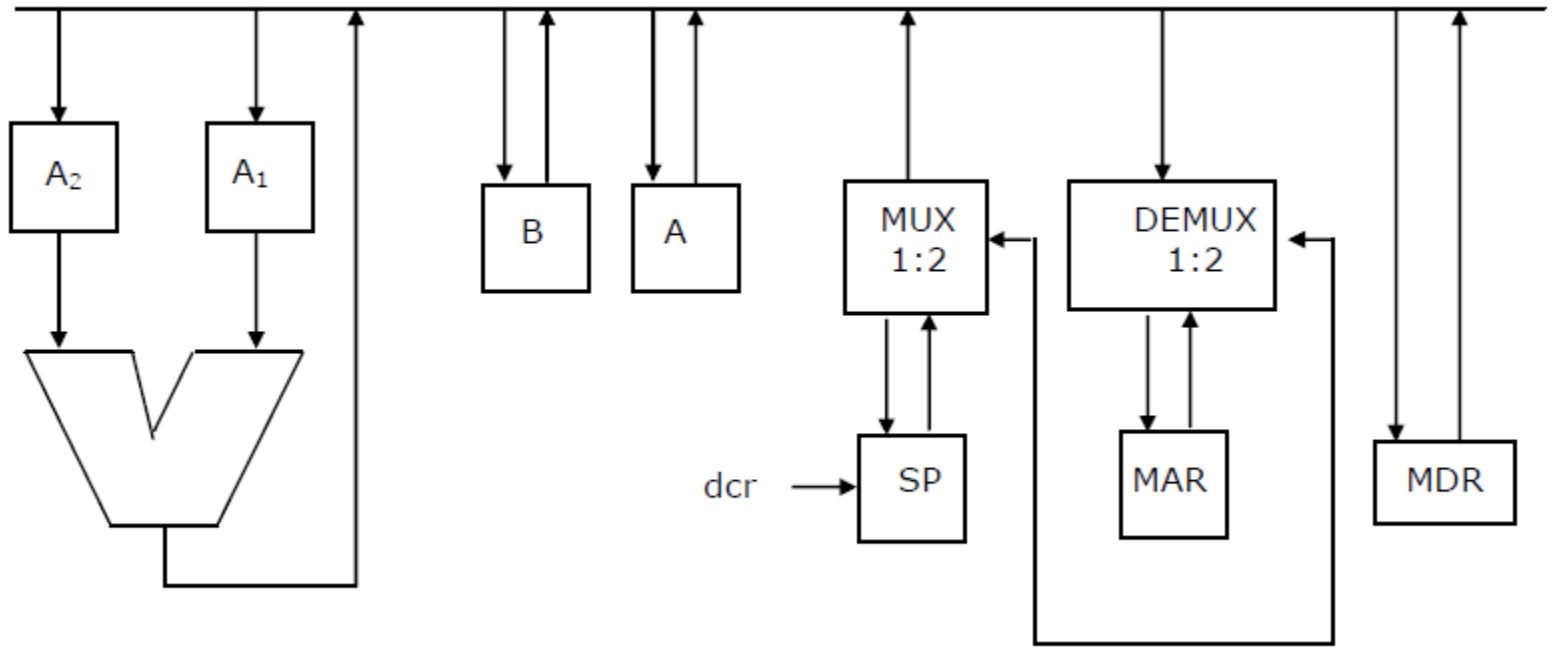
How many CPU clock cycles are needed to execute the "push r" instruction?

(A) 1

(B) 3

(C) 4

(D) 5



MCQ (Single Correct Answer)

GATE CSE 2002

Horizontal microprogramming :
(A) does not require use of signal decoders
(B) results in larger sized microinstructions than vertical microprogramming
(C) uses one bit for each control signal
(D) all of the above.

MCQ (Single Correct Answer)

GATE CSE 2004

The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX.

How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

(A) 10, 3, 1024
(B) 8, 5, 256
(C) 5, 8, 2048
(D) 10, 3, 512

MCQ (Single Correct Answer)

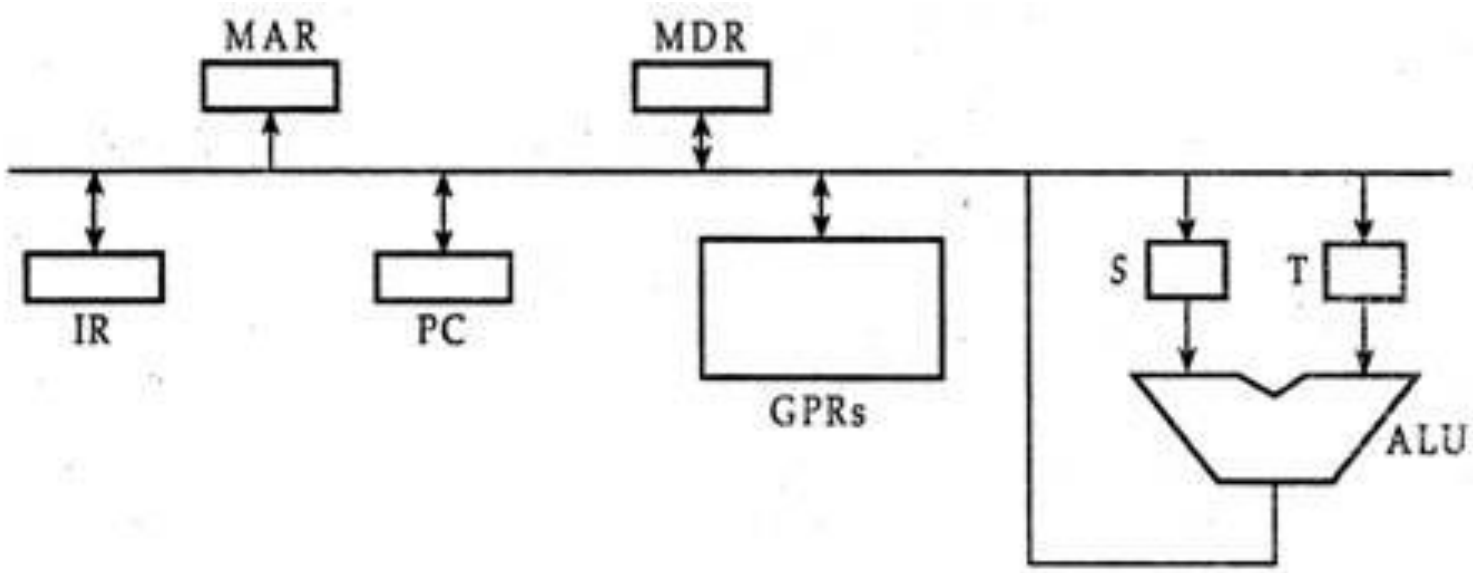
GATE CSE 2005

Consider the following data path of a CPU.

The, ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR

The instruction "add R0, R1" has the register transfer interpretation R0 < = R0 + R1. The minimum number of clock cycles needed for execution cycle of this instruction is.

(A) 2
(B) 3
(C) 4
(D) 5



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Website link :- www.education4fun.com

MCQ (Single Correct Answer)

GATE CSE 2005

Consider the following data path of a CPU.

The, ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR

The instruction "call Rn, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

Rn < = PC + 1; PC < = M[PC];

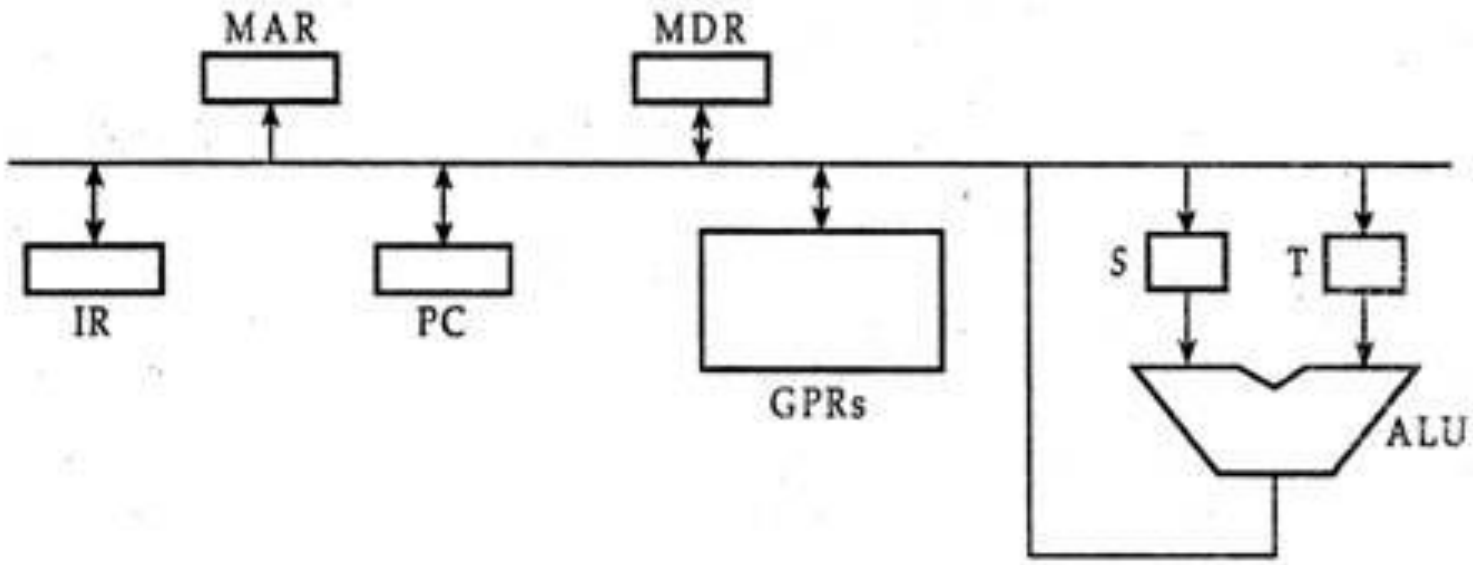
The minimum number of CPU clock cycles needed during the execution cycle of this instruction is:

(A) 2

(B) 3

(C) 4

(D) 5



MCQ (Single Correct Answer)

GATE CSE 2013

Consider the following sequence of micro-operations.

MBR ← PC

MAR ← X

PC ← Y

Memory ← MBR

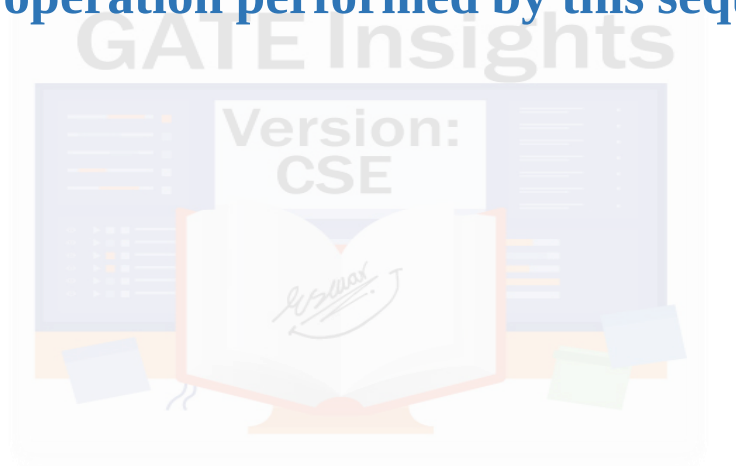
Which one of the following is a possible operation performed by this sequence?

(A) Instruction fetch

(B) Operand fetch

(C) Conditional branch

(D) Initiation of interrupt service



Numerical

GATE CSE 2017 Set 1

Consider a RISC machine where each instruction is exactly 4 bytes long. Conditional and unconditional branch instructions use PC- relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence

If the target of the branch instruction is i, then the decimal value of the Offest is _____.

Instr. No.	Instruction
i:	add R2, R3, R4
i +1:	sub R5, R6, R7
i + 2:	cmp R1, R9, R10
i + 3	beq R1, Offset

MCQ (Single Correct Answer)

GATE CSE 1992

Start and stop bits do not contain 'information' but these are used in serial communication for

A) Error detection

B) Error correction

C) Synchronization

D) Slowing down the communication

MCQ (Single Correct Answer)

GATE CSE 1995

Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line?

(A) Neither vectored interrupt nor multiple interrupting devices are possible.

(B) Vectored interrupts are not possible but multiple interrupting devices are possible.

(C) Vectored interrupts and multiple interrupting devices are both possible.

(D) Vectored interrupt is possible but multiple interrupting devices are not possible.

MCQ (Single Correct Answer)

GATE CSE 1996

For the daisy chain scheme of connecting I/O devices, which of the following statement is true?

(A) It gives non-uniform priority to various devices

(B) It gives uniform priority to all devices

(C) It is only useful for connecting slow devices to a processor

(D) It requires a separate interrupt pin on the processor for each device

MCQ (Single Correct Answer)

GATE CSE 1997

The correct matching for the following pairs is

(A) DMA I/O	(1) High speed RAM
(B) Cache	(2) Disk
(C) Interrupt I/O	(3) Printer
(D) Condition Code Register	(4) ALU

Codes:

	A	B	C	D
a	4	3	1	2
b	2	1	3	4
c	4	3	2	1
d	2	3	4	1

MCQ (Single Correct Answer)

GATE CSE 1998

Which of the following devices should get higher priority in assigning interrupts?

(A) Hard disk

(B) Printer

(C) Keyboard

(D) Floppy disk

MCQ (Single Correct Answer)

GATE CSE 1998

Which of the following is true?

A) Unless enabled, a CPU will not be able to process interrupts.

B) Loop instructions cannot be interrupted till they complete.

C) A processor checks for interrupts before executing a new instruction.

D) Only level triggered interrupts are possible on microprocessors.

MCQ (Single Correct Answer)

GATE CSE 2001

A processor needs software interrupt to

(A) test the interrupt system of the processor

(B) implement co-routines

(C) obtain system services which need execution of privileged instructions

(D) return from subroutine

MCQ (Single Correct Answer)

GATE CSE 2002

In serial data transmission, every byte of data is padded with a ‘0’ in the beginning and one or two ‘I’ s at the end of byte because

(A) Receiver is to be synchronized for byte reception

(B) Receiver recovers lost ‘0’ and ‘1’s from these padded bits

(C) Padded bits are useful in parity computation

(D) None of these

MCQ (Single Correct Answer)

GATE CSE 2004

Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line?

(A) Neither vectored interrupt nor multiple interrupting devices are possible.

(B) Vectored interrupts are not possible but multiple interrupting devices are possible.

(C) Vectored interrupts and multiple interrupting devices are both possible.

(D) Vectored interrupt is possible but multiple interrupting devices are not possible.

MCQ (Single Correct Answer)

GATE CSE 2004

How many 8-bit characters can be transmitted per second over a 9600 baud serial communication link using asynchronous mode of transmission with one start bit, eight data bits, two stop bits, and one parity bit ?

(A) 600

(B) 800

(C) 876

(D) 1200

MCQ (Single Correct Answer)

GATE CSE 2005

Normally user programs are prevented from handling I/O directly by I/O instructions in them. For CPUs having explicit I/O instructions, such I/O protection is ensured by having the I/O instructions privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is true for a CPU with memory mapped I/O?

(A) I/O protection is ensured by operating system routine (s)

(B) I/O protection is ensured by a hardware trap

(C) I/O protection is ensured during system configuration

(D) I/O protection is not possible

MCQ (Single Correct Answer)

GATE CSE 2009

A CPU generally handles an interrupt by executing an interrupt service routine:

A) As soon as an interrupt is raised.

B) By checking the interrupt register at the end of fetch cycle.

C) By checking the interrupt register after finishing the execution of the current instruction.

D) By checking the interrupt register at fixed time intervals.

MCQ (Single Correct Answer)

GATE CSE 2011

A computer handles several interrupt sources of which the following are relevant for this question.

. Interrupt from CPU temperature sensor (raises interrupt if CPU temperature is too high)

. Interrupt from Mouse(raises interrupt if the mouse is moved or a button is pressed)

. Interrupt from Keyboard(raises interrupt when a key is pressed or released)

. Interrupt from Hard Disk(raises interrupt when a disk read is completed)

Which one of these will be handled at the HIGHEST priority?

(A) Interrupt from Hard Disk

(B) Interrupt from Mouse

(C) Interrupt from Keyboard

(D) Interrupt from CPU temperature sensor

MCQ (Single Correct Answer)

GATE CSE 2020

Consider the following statements.

I. Daisy chaining is used to assign priorities in attending interrupts.
II. When a device raises a vectored interrupt, the CPU does polling to identify the source of the interrupt.
III. In polling, the CPU periodically checks the status bits to know if any device needs its attention.
IV. During DMA, both the CPU and DMA controller can be bus masters at the same time.

Which of the above statements is/are TRUE?
A) I and IV only
B) I and II only
C) III only
D) I and III only

MCQ (Single Correct Answer)

GATE CSE 1993

Assume that each character code consists of 88 bits. The number of characters that can be transmitted per second through an asynchronous serial line at 24002400 baud rate, and with two stop bits is

1.109

2.216

3.218

4.219

MCQ (More than One Correct Answer)

GATE CSE 1999

RAID configurations of disks are used to provide

A) Fault-tolerance

B) High speed

C) High data density

D) None of the above

MCQ (Single Correct Answer)

GATE CSE 2000

A graphics card has on board memory of 1 MB. Which of the following modes can the card not support?

(A) 1600 x 400 resolution with 256 colours on a 17-inch monitor

(B) 1600 x 400 resolution with 16 million colours on a 14-inch monitor

(C) 800 x 400 resolution with 16 million colours on a 17-inch monitor

(D) 800 x 800 resolution with 256 colours on a 14-inch monitor

MCQ (Single Correct Answer)

GATE CSE 2005

A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 microsec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

(A) 15

(B) 25

(C) 35

(D) 45

MCQ (Single Correct Answer)

GATE CSE 2005

Consider a disk drive with the following specifications:
16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:

(A) 10
(B) 25
(C) 40
(D) 50

Numerical

GATE CSE 2016 Set 1

The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 29,154 kilobytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____

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MCQ (Single Correct Answer)

GATE CSE 2007

Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively:

(A) 256 Mbyte, 19 bits

(B) 256 Mbyte, 28 bits

(C) 512 Mbyte, 20 bits

(D) 64 Gbyte, 28 bit

Numerical

GATE CSE 1993

A certain moving arm disk storage, with one head, has the following specifications:

- **Number of tracks/recording surface =200**
- **Disk rotation speed =2400 rpm**
- **Track storage capacity =62,500 bits**

The average latency of this device is P ms and the data transfer rate is Q bits/sec. Write the values of P and Q.

MCQ (Single Correct Answer)

GATE CSE 2004

A hard disk with a transfer rate of 10 Mbytes/ second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation ?

(A) 5.0%
(B) 1.0%
(C) 0.5%
(D) 0.1%

MCQ (Single Correct Answer)

GATE CSE 2008

For a magnetic disk with concentric circular tracks, the seek latency is not linearly proportional to the seek distance due to

(A) non-uniform distribution of requests

(B) arm starting and stopping inertia

(C) higher capacity of tracks on the periphery of the platter

(D) use of unfair arm scheduling policies

MCQ (Single Correct Answer)

GATE CSE 2009

A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple (c, h, s), where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0th sector is addressed as (0, 0, 0), the 1st sector as (0, 0, 1), and so on

The address <400,16,29> corresponds to sector number:

(A) 505035

(B) 505036

(C) 505037

(D) 505038

MCQ (Single Correct Answer)

GATE CSE 2009

A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple (c, h, s), where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0th sector is addressed as (0, 0, 0), the 1st sector as (0, 0, 1), and so on

Consider the data given in previous question. The address of the 1039th sector is

(A) (0, 15, 31)

(B) (0, 16, 30)

(C) (0, 16, 31)

(D) (0, 17, 31)

MCQ (Single Correct Answer)

GATE CSE 2011

An application loads 100 libraries at start-up. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10 ms. Rotational speed of disk is 6000 rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected)

(A) 0.50 s

(B) 1.50 s

(C) 1.25 s

(D) 1.00 s

MCQ (Single Correct Answer)

GATE CSE 2013

Consider a hard disk with 16 recording surfaces (0-15) having 16384 cylinders (0-16383) and each cylinder contains 64 sectors (0-63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder-wise and the addressing format is . A file of size 42797 KB is stored in the disk and the starting disk location of the file is <1200, 9, 40>. What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner?

(A) 1281
(B) 1282
(C) 1283
(D) 1284

Numerical

GATE CSE 2015 Set 1

Consider a disk pack with a seek time of 4 milliseconds and rotational speed of 10000 rotations per minute (RPM). It has 600 sectors per track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sectors. Assume that every sector access necessitates a seek, and the average rotational latency for accessing each sector is half of the time for one complete rotation. The total time (in milliseconds) needed to read the entire file is _____.

(A) 14020
(B) 14000
(C) 25030
(D) 15000

Numerical

GATE CSE 2015 Set 2

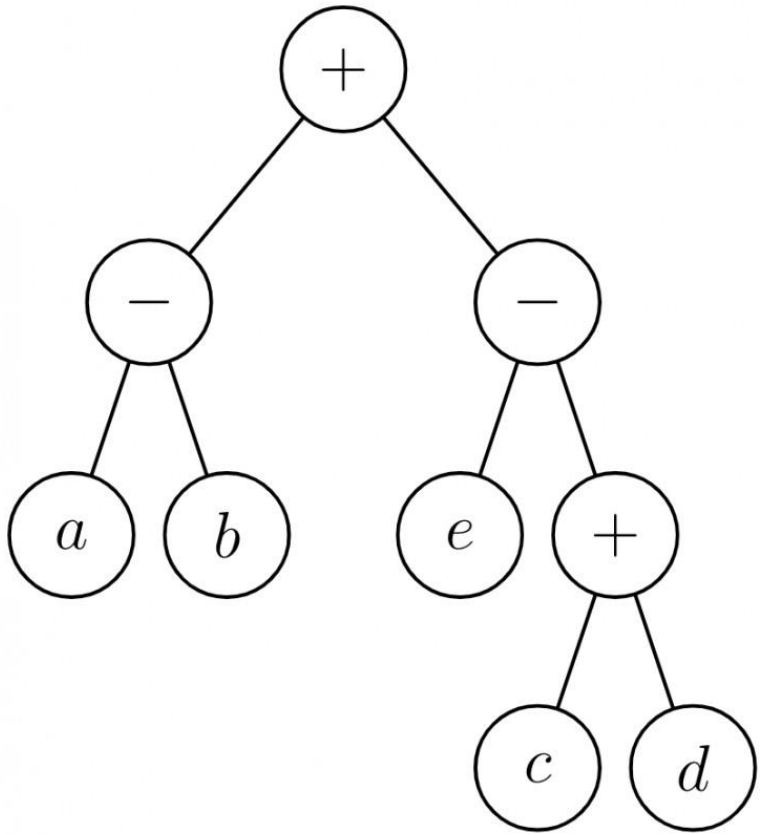
Consider a typical disk that rotates at 15000 rotations per minute (RPM) and has a transfer rate of 50 × 10^6 bytes/sec. If the average seek time of the disk is twice the average rotational delay and the controller's transfer time is 10 times the disk transfer time, the average time (in milliseconds) to read or write a 512 byte sector of the disk is _____

Numerical

GATE CSE 2011

Consider evaluating the following expression tree on a machine with load-store architecture in which memory can be accessed only through load and store instructions. The variables a, b, c, d and e initially stored in memory. The binary operators used in this expression tree can be evaluate by the machine only when the operands are in registers. The instructions produce results only in a register. If no intermediate results can be stored in memory, what is the minimum number of registers needed to evaluate this expression?

(A) 2
(B) 9
(C) 5
(D) 3



Numerical

GATE CSE 2013

The following code segment is executed on a processor which allows only register operands in its instructions. Each instruction can have atmost two source operands and one destination operand. Assume that all variables are dead after this code segment.

Suppose the instruction set architecture of the processor has only two registers. The only allowed compiler optimization is code motion, which moves statements from one place to another while preserving correctness. What is the minimum number of spills to memory in the compiled code?

(A) 0
(B) 1
(C) 2
(D) 3

```
c = a + b;
d = c * a;
e = c + a;
x = c * c;
if (x > a) {
    y = a * a;
}
else {
   d = d * d;
   e = e * e;
}
```

Numerical

GATE CSE 2013

The following code segment is executed on a processor which allows only register operands in its instructions. Each instruction can have atmost two source operands and one destination operand. Assume that all variables are dead after this code segment.

Consider the same data as above question. What is the minimum number of registers needed in the instruction set architecture of the processor to compile this code segment without any spill to memory? Do not apply any optimization other than optimizing register allocation.

(A) 3
(B) 4
(C) 5
(D) 6


```
c = a + b;
d = c * a;
e = c + a;
x = c * c;
if (x > a) {
    y = a * a;
}
else {
  d = d * d;
  e = e * e;
}
```