Computer Engineering Department, S V N I T, Surat.
End Sem. Examinations, Nov - Dec 2019

B Tech II (CO) – 3rd semester
Course: Computer Organization (CO201)

Dated: 2nd Dec 2019 Time: 15:30 hrs to 18:30 hrs Max Marks: 100

Instructions:

1. Write your B. Tech. Admission No./Roll No. and other details clearly on the answer books while write your B. Tech. Admission No. on the question paper, too.
2. Assume any necessary data but give proper justifications.
3. Be precise and clear in answering the questions.

Q. 1 Answer the following for the given MIPS code of 'c' code for the machine with 2 GHz clock: **[30]**

'c' code

count=0;
n=5;
for (i=0; i<n-1; i++)
if (A[i]==A[i+1])
{
count++;
}

Line No.	MIPS code
0	Addi $s1, $0, 5
1	___(1)___ $s1, $s1, -1
2	add ___(2)___, $0, $0
3	Loop: lw $t0, ___(3)___
4	lw $t1, ___(4)___
5	bne $t0, $t1, ___(5)___
6	addi $s2, $s2, ___(6)___
7	Skip: addi $s0, $s0, ___(7)___
8	___(8)___ $s1, $s1, -1
9	bne $s1, ___(9)___, ___(10)___

[A] a) By considering the registers for 'c' variables as $s2 for count, $s1 for array size n and $s0 for base address of array, fill in the blanks with the justification. [05]

b) For the single cycle processor architecture, enlist and explain instruction(s) which will work correctly, if RegWrite and AluSrc control signals are stuck to 1. [04]

c) Write the description and RTL of uncommon MIPS instruction execution stages of multi cycle and pipelined processor. [04]

[B] a) Calculate the target address offset with the help of addressing mode explanation for the Line No. 9 of MIPS code, if starting location of code is 20000_{10}. [02]

b) Explain the fields of the microprogrammed control unit. [03]

c) For the single cycle processor and for the Line No. 4 of MIPS code, draw data path components. [04]

d) Above MIPS code is to be executed on a multi cycle MIPS processor for 1 million times with the same data. Calculate MIPS rate and explain drawback of it. [04]

e) Write the instruction name and all control signals values for the multi cycle processor which will be performed during the clock cycle no. 20. [04]

OR

[B] a) Distinguish between the traditional programming language and the language used to design FPGA/ASICs. [02]

b) Explain the type of processor architecture(s) that can be identified from the given instructions. [03]

c) For the MIPS, write all the common control signal names of single cycle processor and multi cycle processor. From this list, explain the changes required in control signals for the pipelined processor. [04]

d) Above MIPS code is to be executed on a multi cycle MIPS processor. Calculate the CPI. [04]

e) With the help of diagram for the multi cycle processor, explain the ALU input multiplexers. [04]

Q. 2 Consider the 5-stage pipeline for the MIPS code: [20]

Line No.	MIPS Code		
1		lw	$s1, 8($s0)
2		add	$s2, $s1, $s0
3		bne	$s0, $s1, Exit
4		or	$s3, $s1, $s2
5		lw	$s4, 4($s3)
6	Exit:	add	$s5, $s3, $s4

a) Write and identify all four data hazard types. Also with the help of diagram explain the hazard detection unit to resolve the data dependencies with hazard conditions. **OR** Identify the control hazard, if any and explain its four different solutions. [12]

b) Discuss the hazards which occur due to storage component read/write usage within the same clock cycle together with their solution justification. [08]

Q. 3 Answer the following [Any Three]: [12]

a) Let A = 1111 1010 and B = 0000 1010 be two 8-bit 2's complement numbers. Calculate the product in 2s complement.

b) P is a 16-bit signed integer. The 2's complement representation of P is (F87B)16. Calculate 2's complement representation of 8*P.

c) A computer with 32 bits word size uses 2's compliment to represent numbers. What is the range of integers that can be represented by this computer?

d) The value of a float type variable is represented using the single-precision 32-bit floating point format IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of −14.25. Find the representation of X in binary notation.

Q. 4 Answer the following: [14]

a) For two numbers that are to be multiplied using the Booth's algorithm. Multiplier is 0111 0111 1011 1101. How many additions/Subtractions are required for the multiplication of the above two numbers? [06]

b) How does the CPU respond to various interrupt requests generated simultaneously? Explain that mechanism along with its types. [04]

c) Differentiate between Static RAM and Dynamic RAM. Also enlist their major applications and justify the same. [04]

Q. 5 Answer the following: [24]

a) Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. Find the number of bits needed for cache indexing and the number of tag bits are respectively.

b) A two-way set associative cache memory uses a block of four words. The cache can accommodate 2048 words from the main memory. The main memory size is 128K*32. Find out: i) No of bits in the tag field, ii) No of bits in the index field, iii) Size of cache memory.

c) What are the different mechanisms of implementing virtual memory concept? Explain them in detail. **OR** Explain the concept of Direct Memory Access along with its block diagram.

d) The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words in each. Physical memory consists of 4K blocks of 4K words in each. Formulate the logical and physical address formats.

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