Computer Engineering Department, S V N I T, Surat
Mid Semester Exam, September 2017
B. Tech II (CO) – 3rd semester
Course: Computer Organization (CO201)

Date: 19th September 2017 Time: 11:00 - 12:30 pm Total Marks: 30

Instructions:
1. Be precise and clear in answering the questions.
2. Assume any necessary data but give proper justifications.
3. Write your B. Tech Admission No/Roll No and other details clearly on the answer books while write your B. Tech Admission No on the question paper, too.

Q.1 Answer the following [Any Five]: **[05]**

1) Define computer organization. Describe the benefits of learning.
2) What features are considered by the compiler to compile the high level language program?
3) Describe ISA and explain the elements of instruction.
4) Justify the statement: One of the design principle states that smaller is faster.
5) Differentiate between register-register and load-store architecture.
6) Why registers are used for variables?

Q.2 Answer the following: **[10]**

1) Explain the stored program concept and its model. [02]
2) Explain how CISC processor achieves shorten execution time. [02]
3) Write instructions for 32-bits MIPS processor for the high level language instructions (consider $s0-base address of Ans, $s1-base address of No, $s2-i : [03]

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for (i=5; i>=0; i--)    Ans[i]=No[i]*16;
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4) For the Q.2(3), show 32-bits MIPS instruction mnemonics only on the memory location for PC=80000. Provide the calculated memory address component and target address calculation for branch instruction. Note: Ignore calculation of memory address component for jump instruction. [03]

Q.3 Answer the following: **[09]**

1) Perform the arithmetic operations (+42) + (-13) and (-42) – (-13) in binary using signed-2's complement representation for negative numbers using 8-bit. [02]
2) Design a 4-bit combinational circuit of Incrementer using half adders. [03]
3) Explain Booth multiplication algorithm with its flowchart. [04]

OR

3) Show stepwise execution of Booth Multiplication for the given numbers (-9) * (-13) with values of Q_nQ_{n+1}, AC and QR. Consider 5 bit registers for the signed numbers. [04]

Q.4 Answer the following [Any Two]: **[06]**

1) a) Perform Subtraction (20 – 100) by taking the 10's complement of the subtrahend.
   b) Explain overflow by performing the arithmetic operation (+70) + (+80) and (-70) + (-80).
2) If the values of j and k are 3 and 4 respectively. Design an array multiplier using AND gates and adders. Consider j = multiplier bit, k = multiplicand bit.
3) Draw and explain flowchart of signed magnitude data for addition and subtraction.

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