In this topic we’ll learn

LED with their applications

Basic theory of BJT

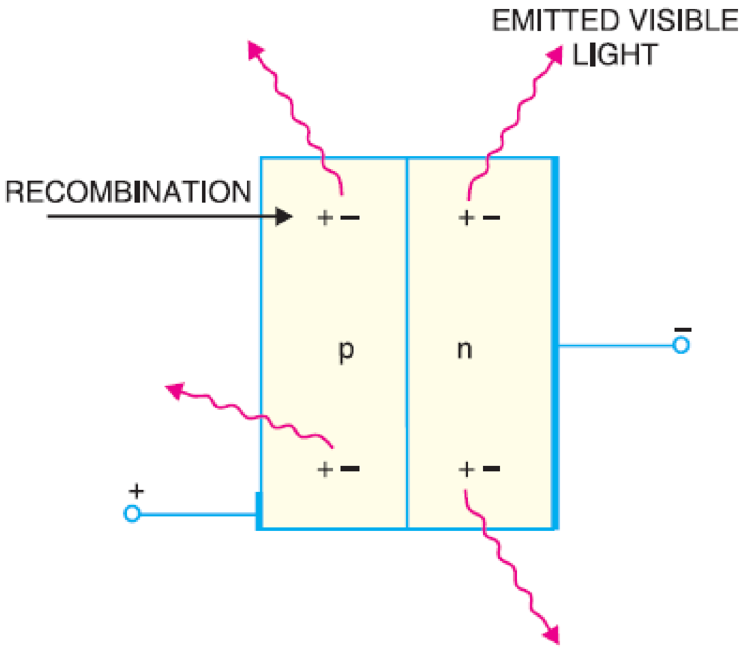
Different models of BJT

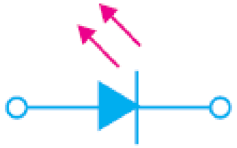
BJT as an amplifier

Introduction to FET

LIGHT EMMITING DIODES (LED)

A **light-emitting diode (LED)** *is a diode that gives off visible light when forward biased*





The free electrons are in the conduction band and at a higher energy level than the holes in the valence band.

When recombination takes place, the recombining electrons release energy in the form of heat and light.

In germanium and silicon diodes, almost the entire energy is given up in the form of heat and emitted light is insignificant.

However, in materials like gallium arsenide, the number of photons of light energy is sufficient to produce quite intense visible light.

Although LEDs are available in several colours (red, green, yellow and orange are the most common), the schematic symbol is the same for all LEDs.

Advantages of LED:

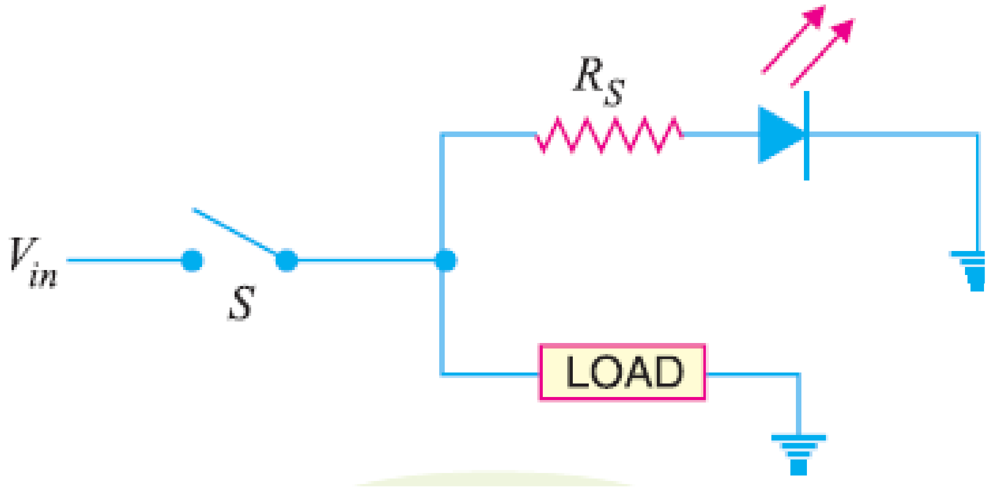
- Low voltage
- Longer life (more than 20 years)
- Fast on-off switching

Applications of LED:

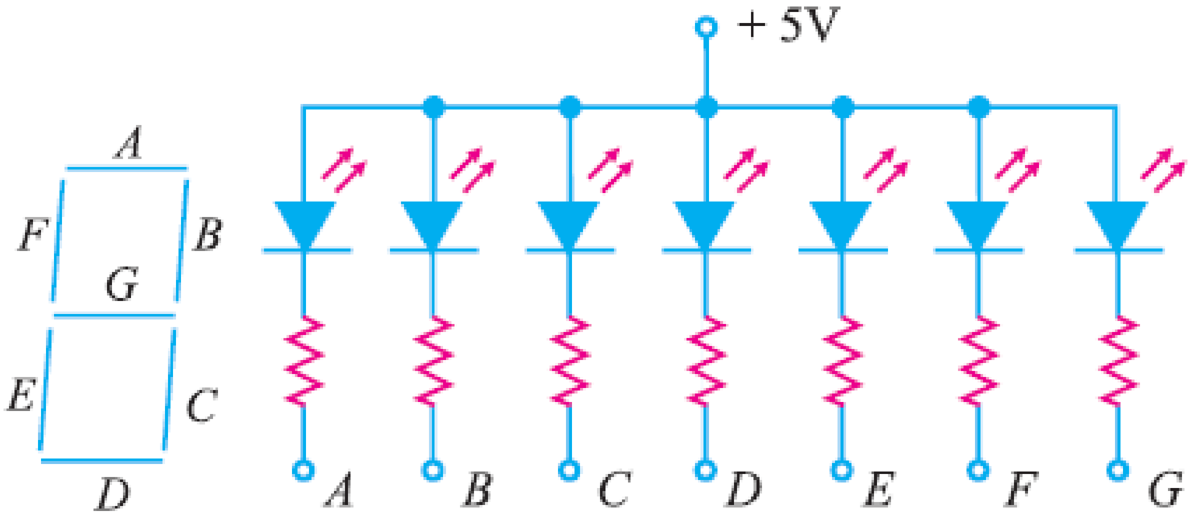
The two most common applications for visible LEDs are

(i) as a power indicator

(ii) seven-segment display.



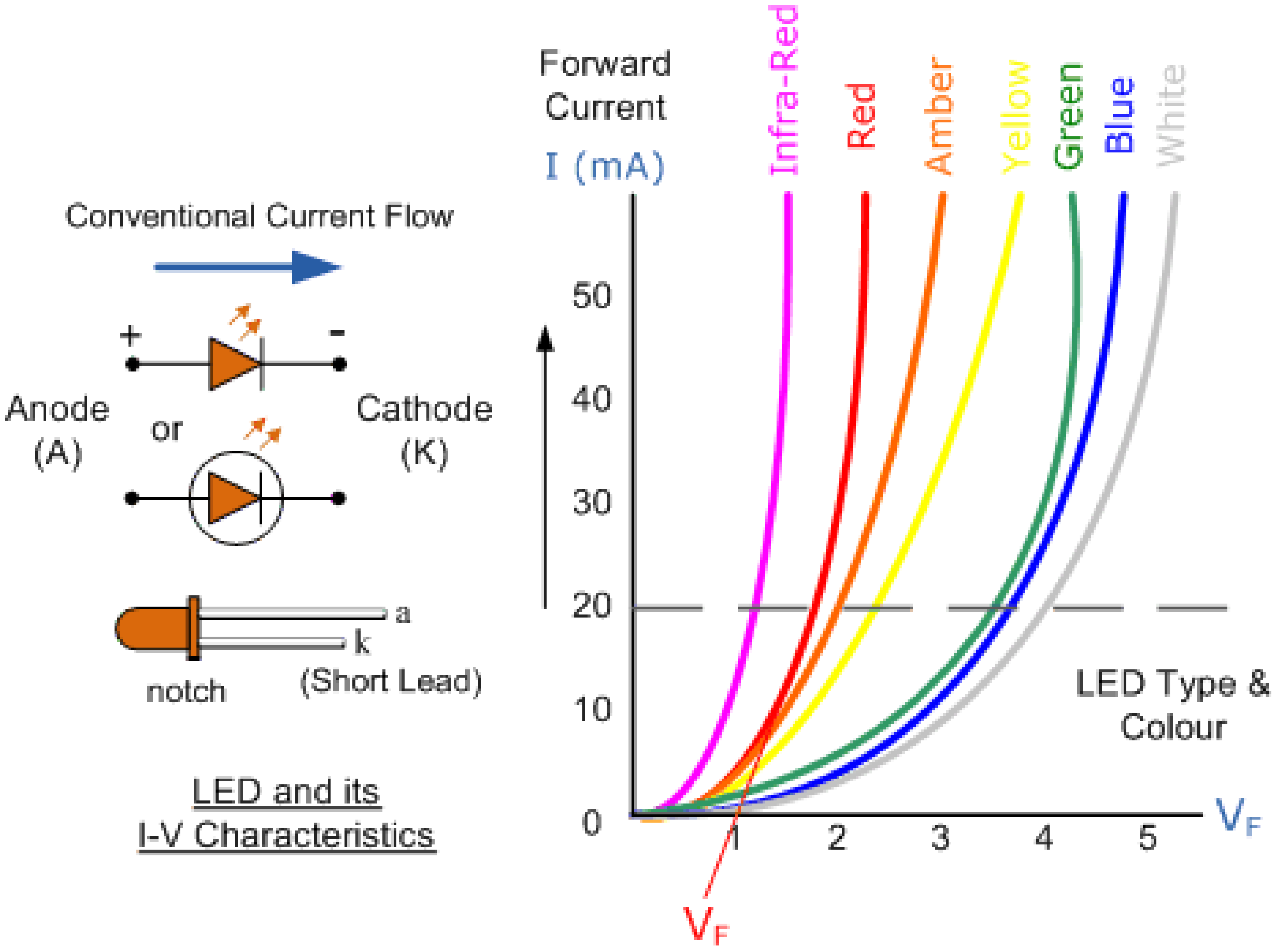
Circuit for power indication



Schematic for 7 segment display

The anodes of all seven LEDs are connected to a common positive voltage source of +5 V. This arrangement is known as *common-anode type*.

In order to light a particular LED, say *A*, we ground the point *A*. It forward biases the LED *A* which will be lit.



I-V Characteristics

Photodiode

A **photo-diode** *is a reverse-biased silicon or germanium pn-junction in which reverse current increases when the junction is exposed to light*.

The reverse current in a photo-diode is directly proportional to the intensity of light falling on its *pn* junction.

This means that greater the intensity of light falling on the *pn* junction of photo-diode, the greater will be the reverse current.

Principle

A photo-diode differs from a rectifier diode in that when its pn junction is exposed to light, the reverse current increases with the increase in light intensity and vice-versa. This is explained as follows.

When light (photons) falls on the *pn* junction, the energy is imparted by the photons to the atoms in the junction.

This will create more free electrons (and more holes). These additional free electrons will increase the reverse current.

As the intensity of light incident on the *pn* junction increases, the reverse current also increases.

In other words, as the incident light intensity increases, the resistance of the device (photo-diode) decreases.

(i) Reverse current-Illumination curve.

Fig. i shows the graph between reverse current (*IR*) and illumination (*E*) of a photo-diode.

The reverse current is shown on the vertical axis and is measured in µA.

The illumination is indicated on the horizontal axis and is measured in mW/cm2.

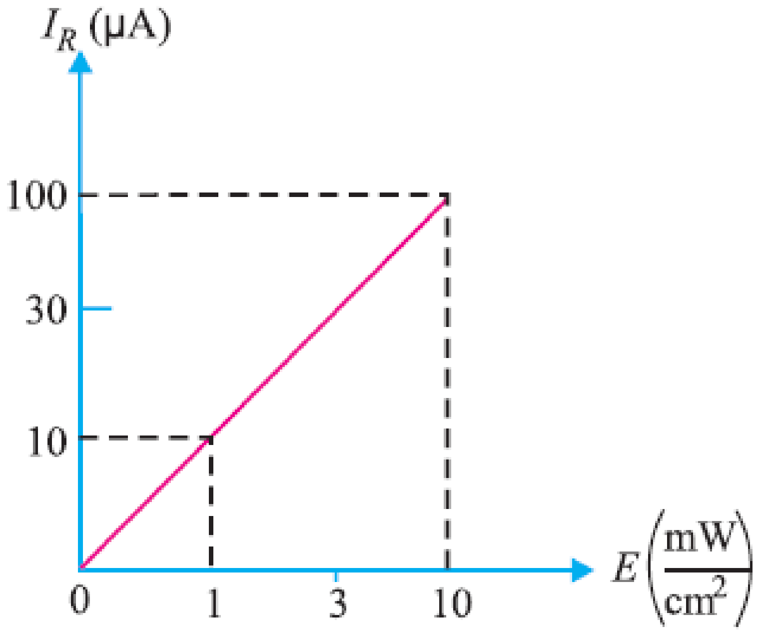
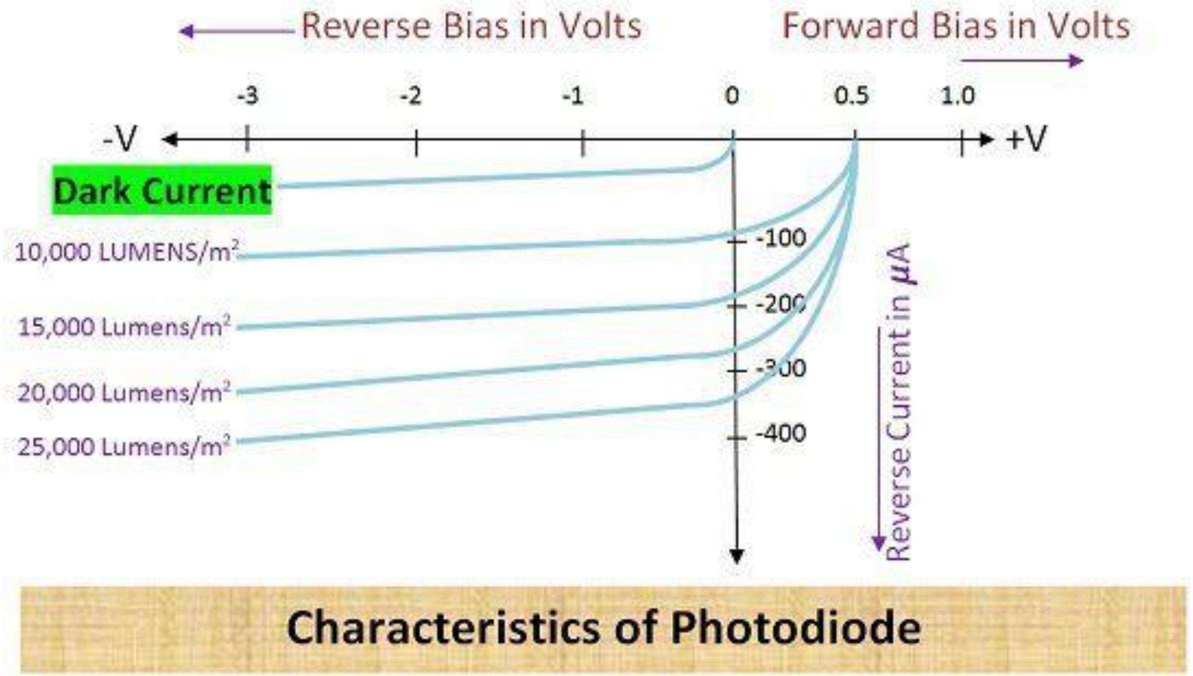


Fig. i

(*ii*) Reverse voltage-Reverse current curve.

Fig. (ii) shows the graph between reverse current (IR) and reverse voltage (VR) for various illumination levels. It is clear that for a given reverse-biased voltage V_R, the reverse current I_R increases as the illumination (E) on the pn junction of photo-diode is increased.

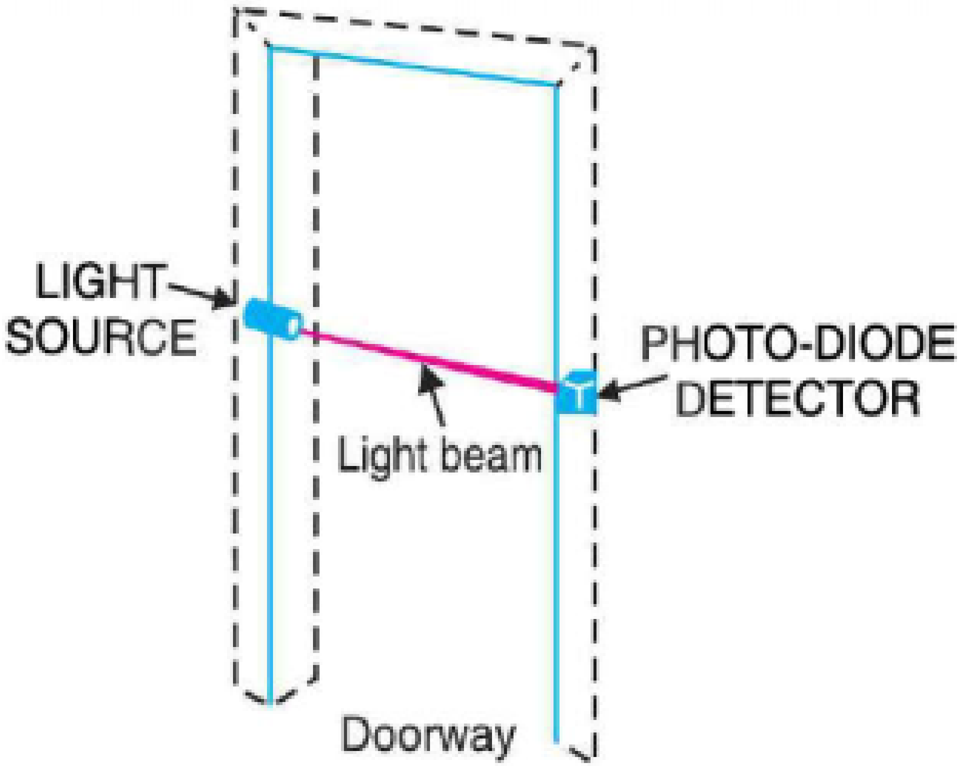
Fig. (ii)



The lumen is the unit of luminous flux, a measure of the total quantity of visible light emitted by a source per unit of time

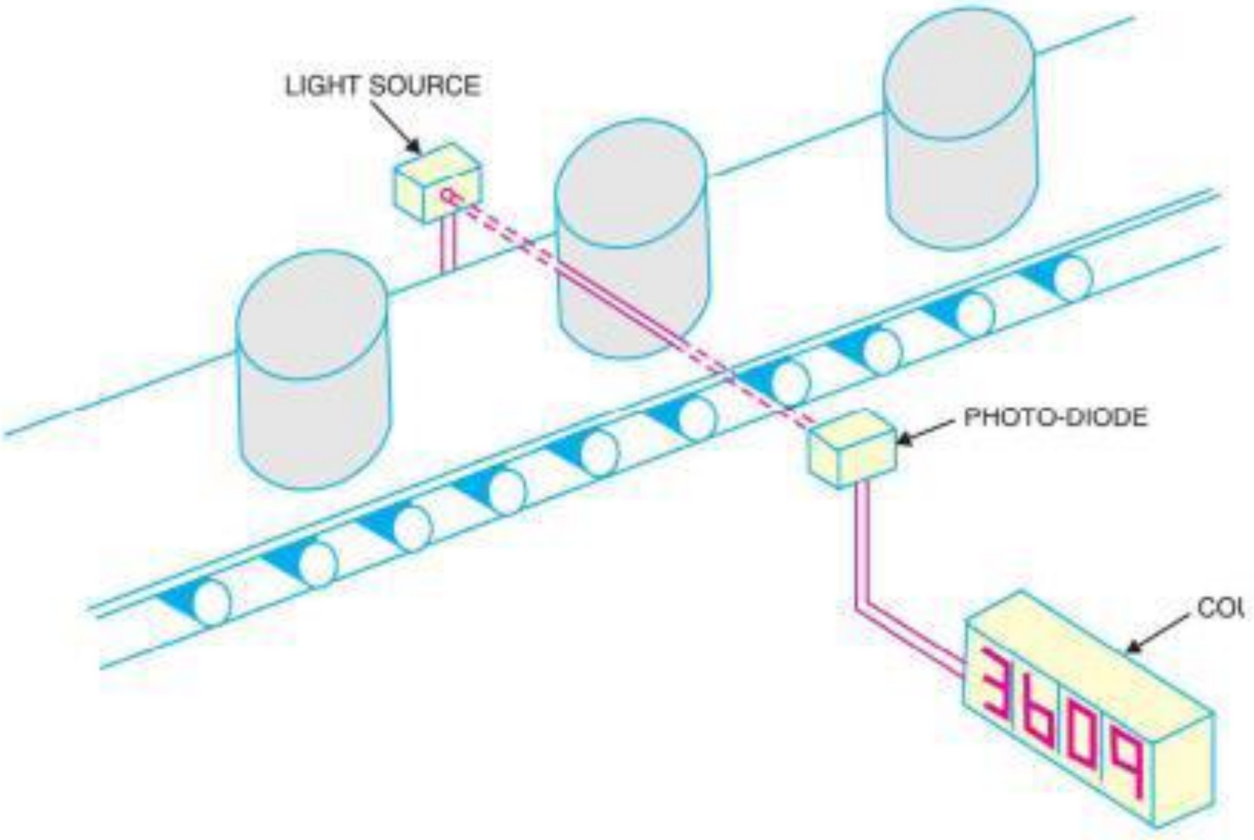
Alarm Circuit

- Light from a beam is allowed to fall on a photo-diode
- Reverse current will continue to flow till beam is not broken
- If a person passes, the beam breaks, the reverse current drops down to the dark current level
- This can be used to sound an alarm



Counter Circuit

- ❑ Source sends a concentrated beam to a photo-diode across a conveyor.
- ❑ As the object passes, the beam breaks, the reverse current drops down to the dark current level and the count increases by one.



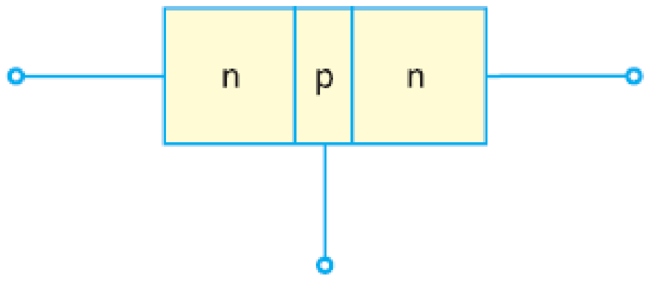
BIPOLAR JUNCTION TRANSISTOR

A ***transistor*** *consists of two pn junctions formed by sandwiching either p-type or n-type semiconductor between a pair of opposite types.*

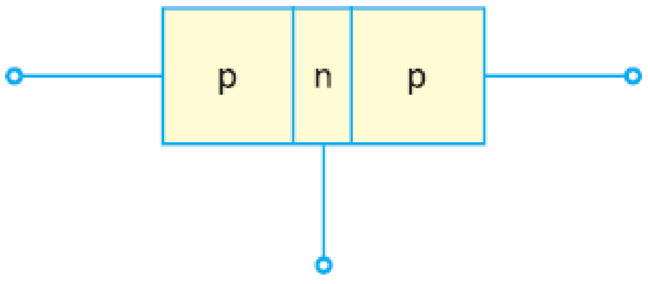
Accordingly ; there are two types of transistors, namely;
(*i*) *n-p-n* transistor (*ii*) *p-n-p* transistor

An *n-p-n* transistor is composed of two *n*-type semiconductors separated by a thin section of *p*-type as shown Fig. (*i*).

However, a *p-n-p* transistor is formed by two *p*-sections separated by a thin section of *n*-type as shown in Fig. (*ii*).



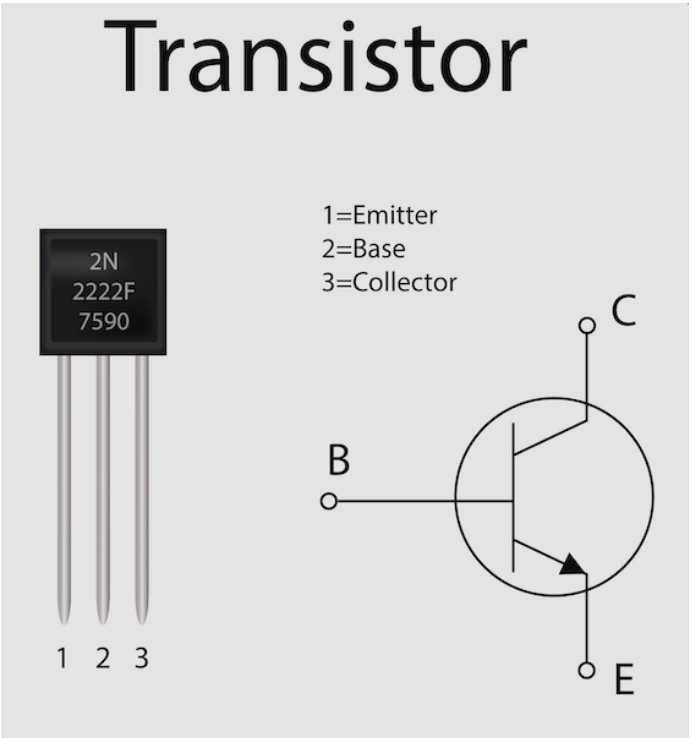
(*i*)



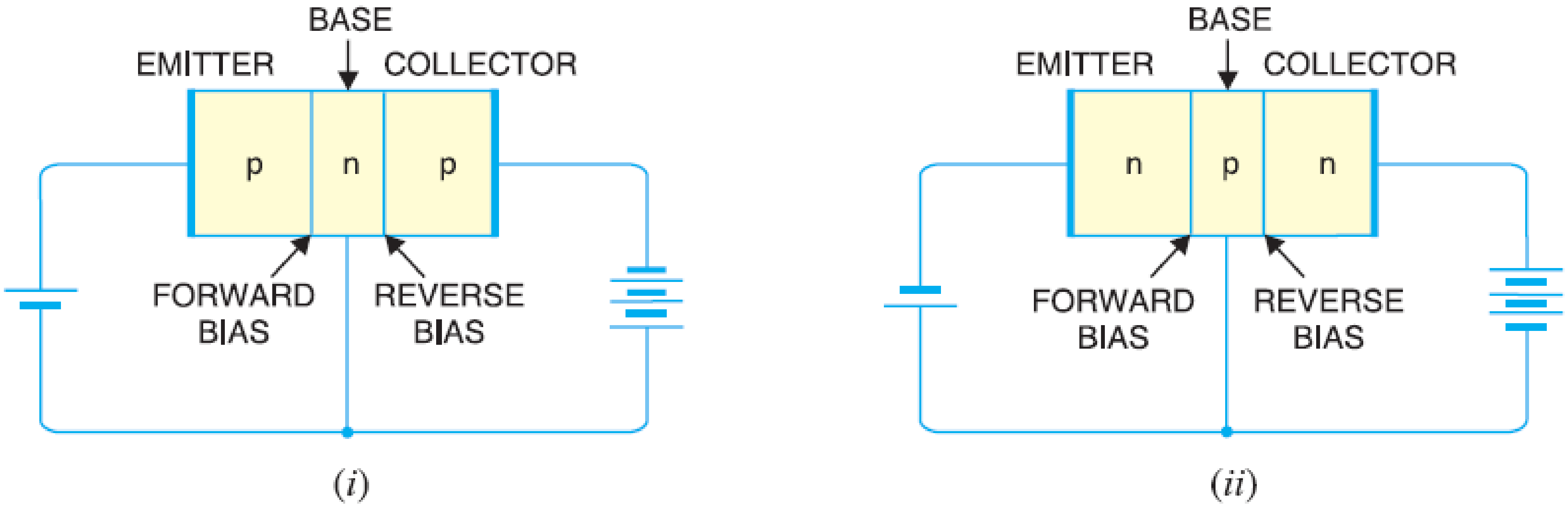
(*ii*)

A transistor (*pnp* or *npn*) has three sections of doped semiconductors.

The section on one side is the *emitter* and the section on the opposite side is the *collector*. The middle section is called the *base* and forms two junctions between the emitter and collector.



Therefore, a transistor *transfers* a signal from a low resistance to high resistance. The prefix ‘trans’ means the signal transfer property of the device while ‘istor’ classifies it as a solid element in the same general family with resistors.



The section on one side that supplies charge carriers (electrons or holes) is called the *emitter*. *The emitter is always forward biased w.r.t. base* so that it can supply a large number of majority carriers.

The section on the other side that collects the charges is called the *collector*. *The collector is always reverse biased.* Its function is to remove charges from its junction with the base.

The middle section which forms two *pn*-junctions between the emitter and collector is called the *base*.

The base-emitter junction is forward biased, allowing low resistance for the emitter circuit. The base-collector junction is reverse biased and provides high resistance in the collector circuit.

The base is *much thinner* than the emitter while collector is *wider* than both. However, for the sake of convenience, it is customary to show emitter and collector to be of equal size.

The emitter is *heavily doped* so that it can inject a large number of charge carriers (electrons or holes) into the base. The base is *lightly doped* and very thin; it passes most of the emitter injected charge carriers to the collector. The collector is *moderately doped*.

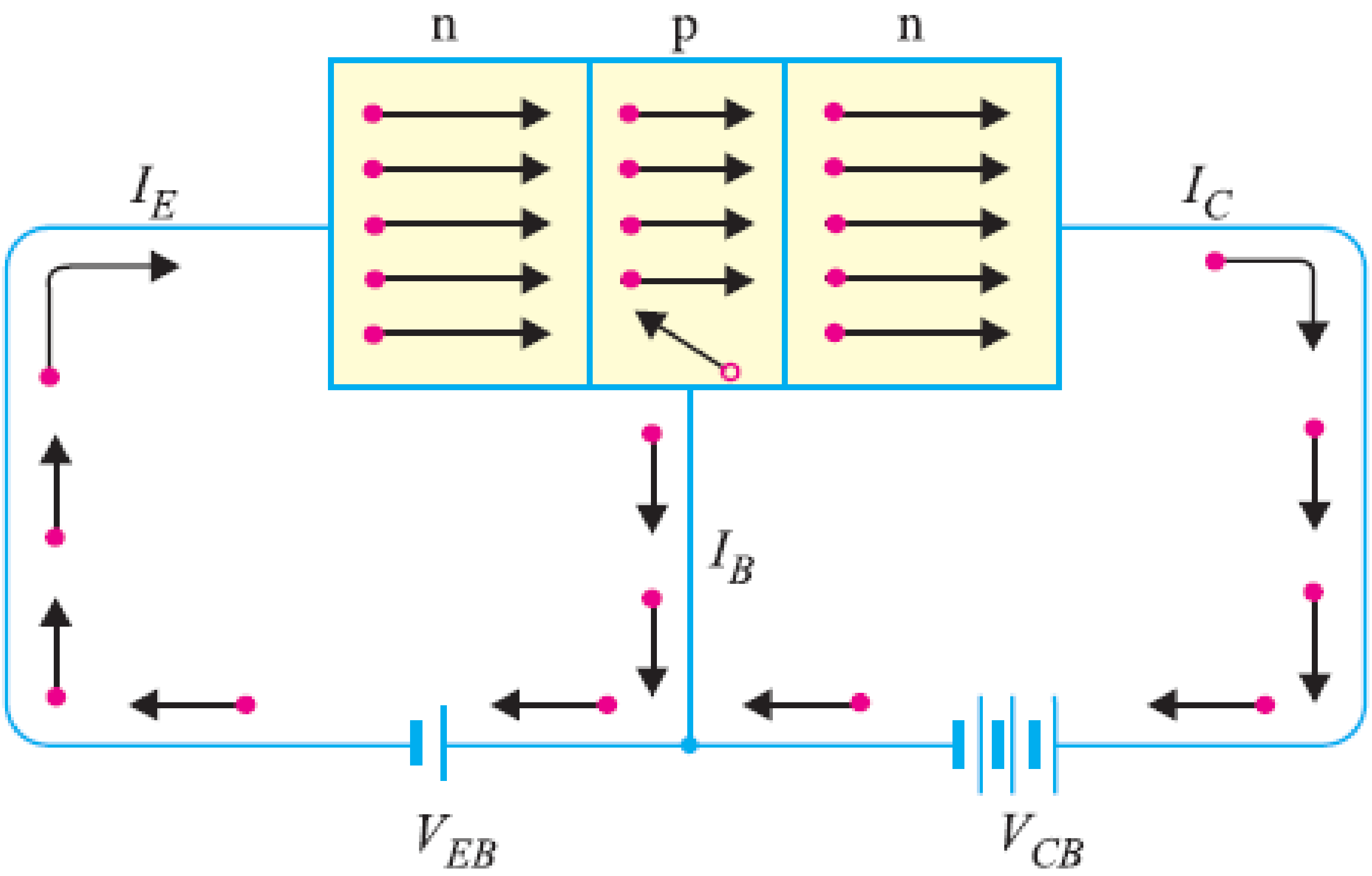
Working of npn transistor. Fig. shows the *npn* transistor with forward bias to emitter-base junction and reverse bias to collector-base junction.

The forward bias causes the electrons in the *n*-type emitter to flow towards the base. This constitutes the emitter current I_E. As these electrons flow through the *p*-type base, they tend to combine with holes.

As the base is lightly doped and very thin, therefore, only a few electrons (less than 5%) combine with holes to constitute base current I_B. The remainder cross over into the collector region to constitute collector current I_C.

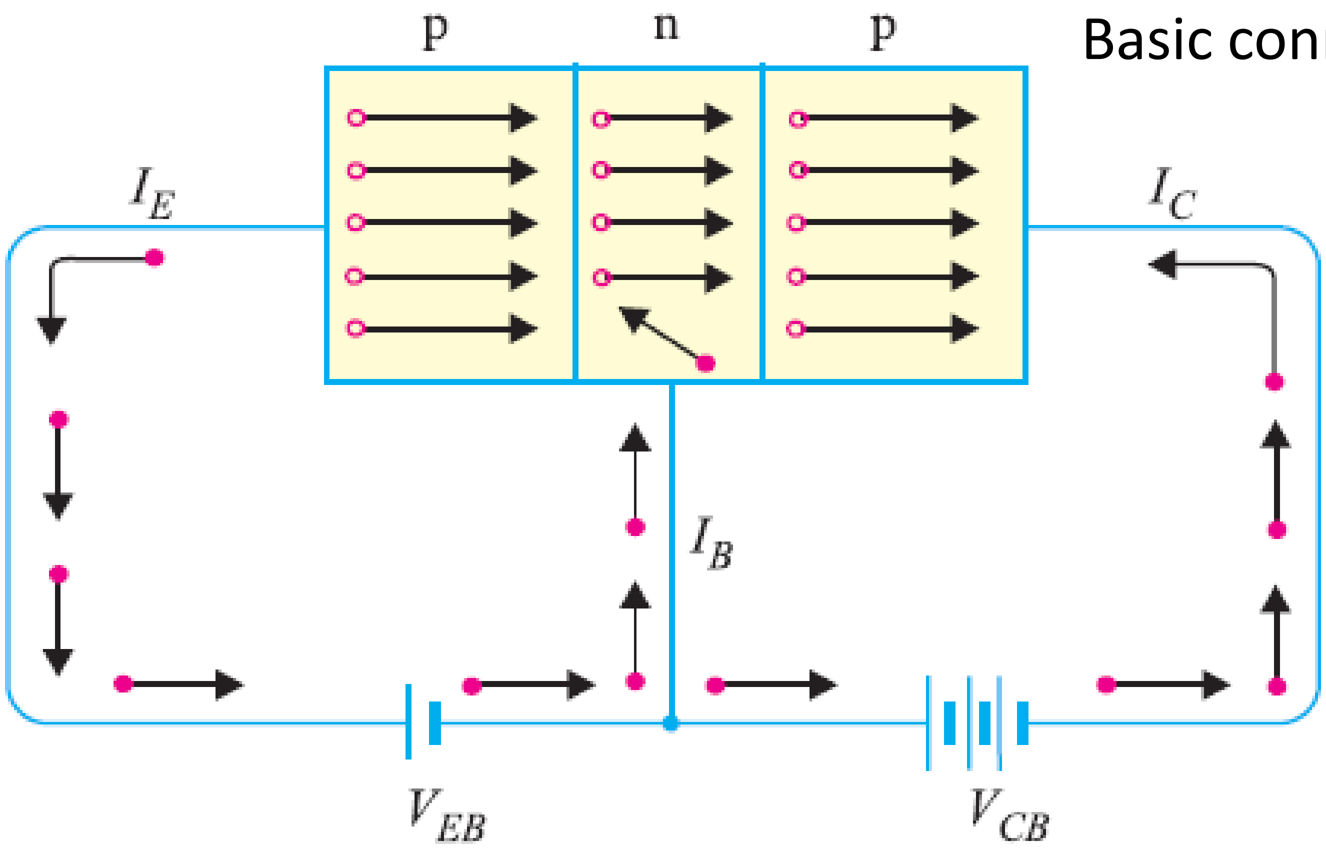
In this way, almost the entire emitter current flows in the collector circuit. It is clear that emitter current is the sum of collector and base currents *i.e.*

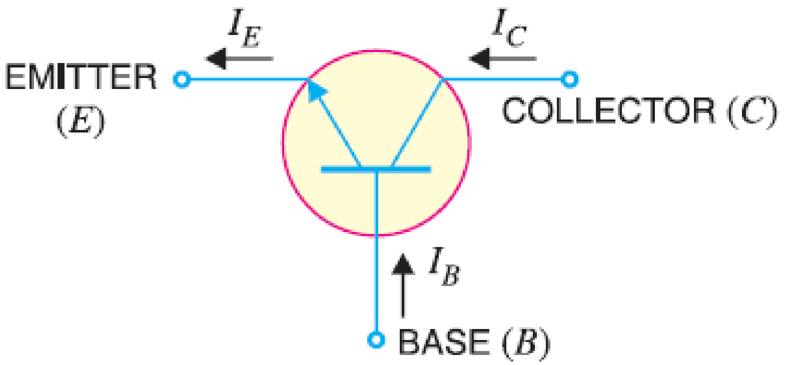
$$I_E = I_B + I_C$$

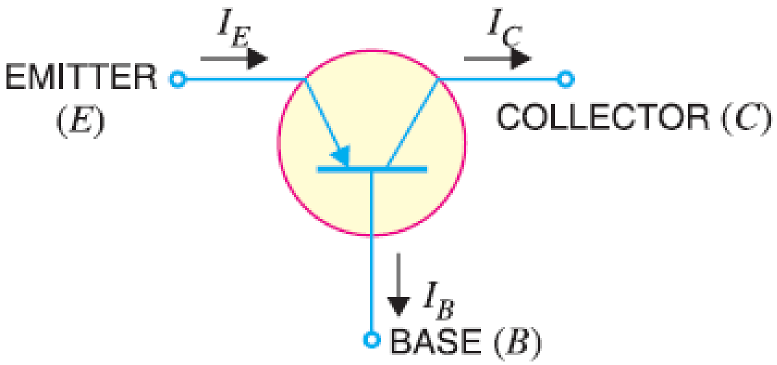


Basic connection for npn transistor

Basic connection for pnp transistor



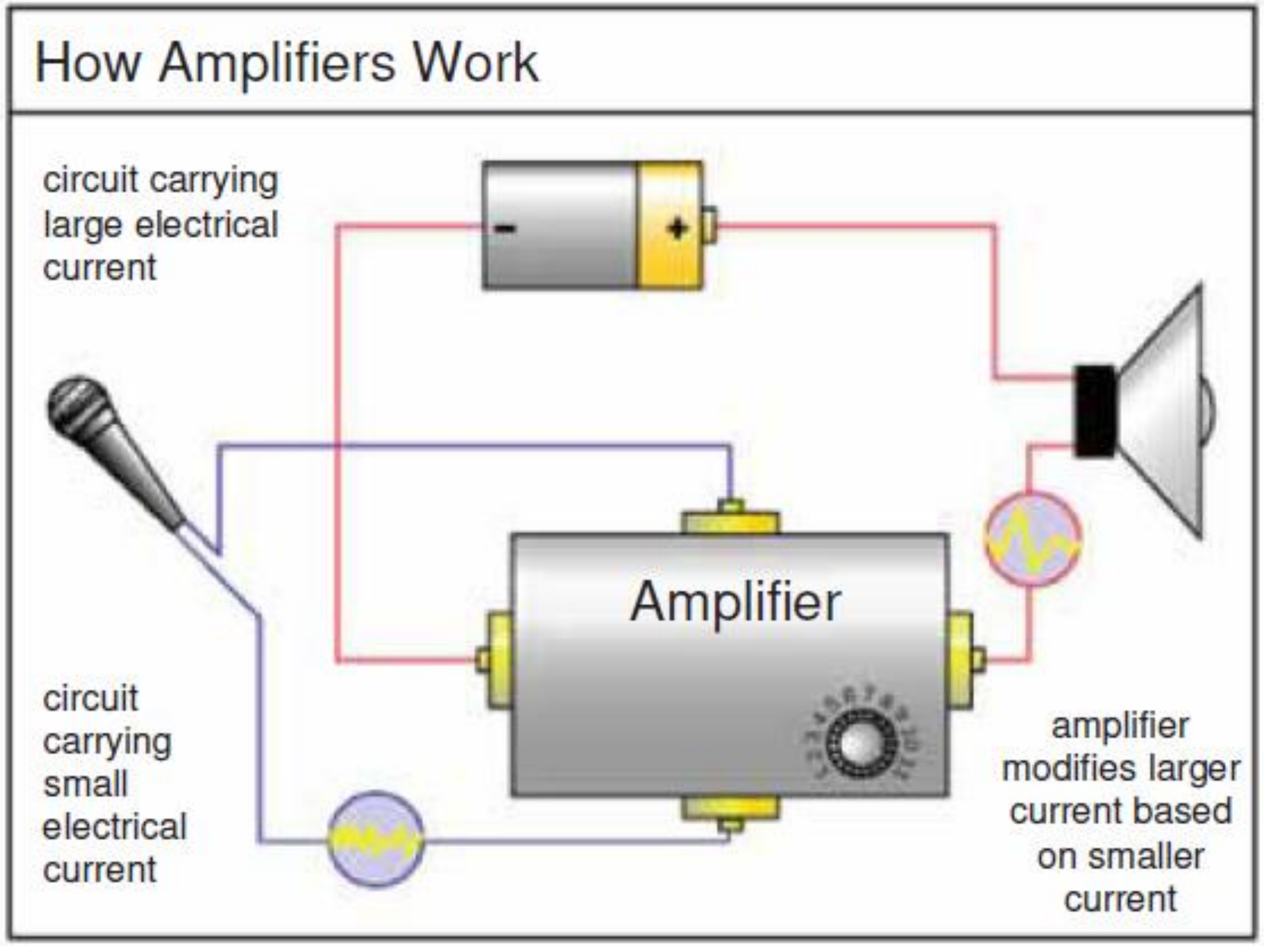




Suppose collector load resistance R_C = 5 kΩ. Let us further assume that a change of 0.1V in signal voltage produces a change of 1 mA in emitter current.

Obviously, the change in collector current would also be approximately 1 mA.

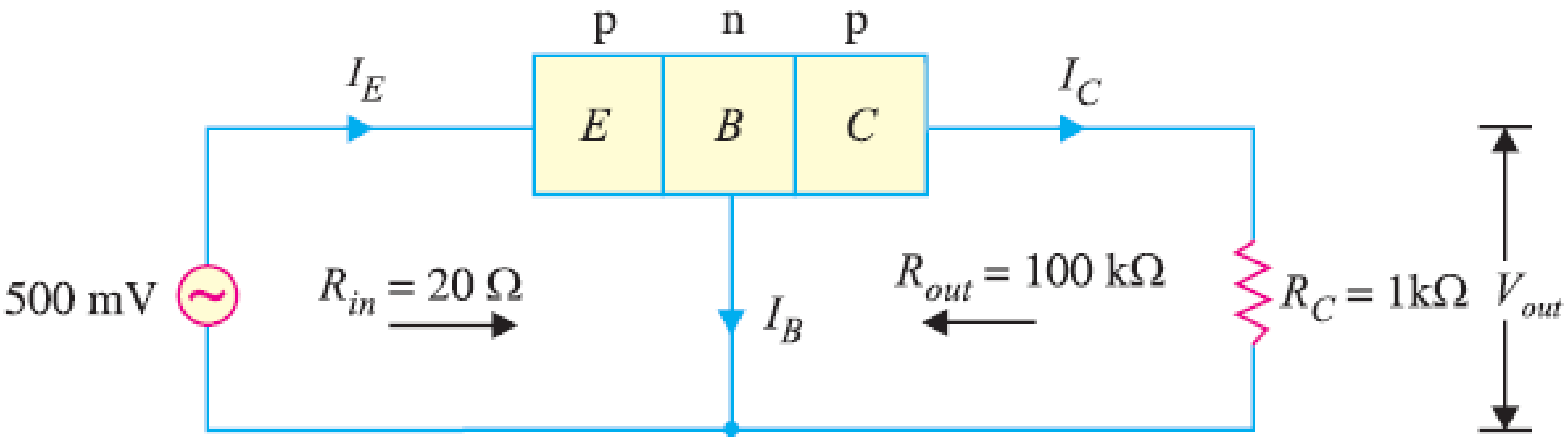
This collector current flowing through collector load R_C would produce a voltage = 5 kΩ × 1 mA = 5 V.



Thus, a change of 0.1 V in the signal has caused a change of 5 V in the output circuit. In other words, the transistor has been able to raise the voltage level of the signal from 0.1 V to 5 V *i.e.* voltage amplification is 50.

Example 8.1. *A common base transistor amplifier has an input resistance of 20 Ω and output resistance of 100 kΩ. The collector load is 1 kΩ. If a signal of 500 mV is applied between emitter and base, find the voltage amplification. Assume α_{ac} to be nearly one.*

Solution. **Fig. 8.8 shows the conditions of the problem. Note that output resistance is very high as compared to input resistance. This is not surprising because input junction (base to emitter) of the transistor is forward biased while the output junction (base to collector) is reverse biased.



Input current, $I_E = \dfrac{\text{Signal}}{R_{in}} = \dfrac{500 \text{ mV}}{20\ \Omega} = 25$ mA. Since α_{ac} is nearly 1, output current, $I_C = I_E =$ 25 mA.

$$\text{Output voltage, } V_{out} = I_C R_C = 25 \text{ mA} \times 1 \text{ k}\Omega = 25 \text{ V}$$

$$\therefore \quad \text{Voltage amplification, } A_v = \frac{V_{out}}{\text{signal}} = \frac{25\,V}{500\,mV} = \mathbf{50}$$

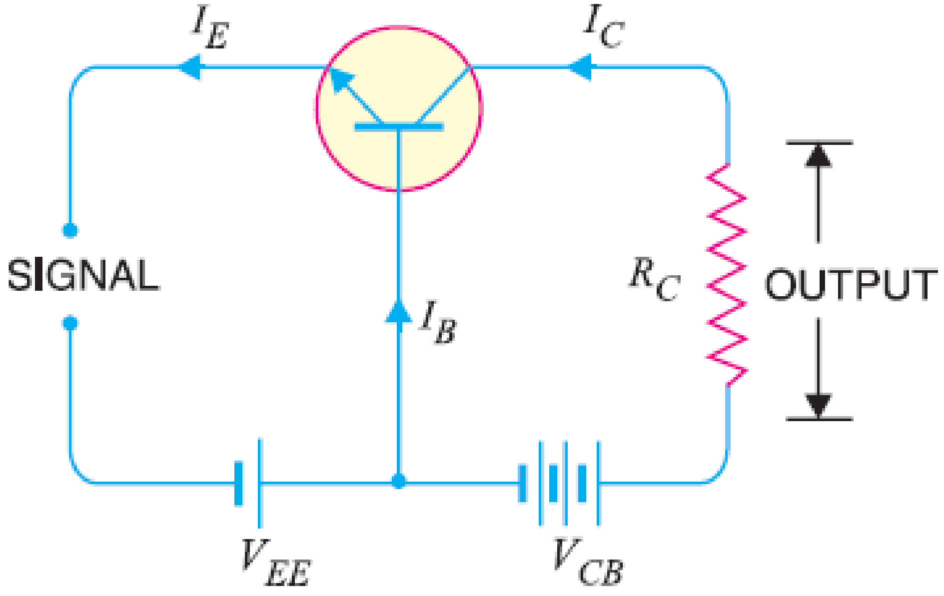
TRANSISTOR CONFIGURATIONS

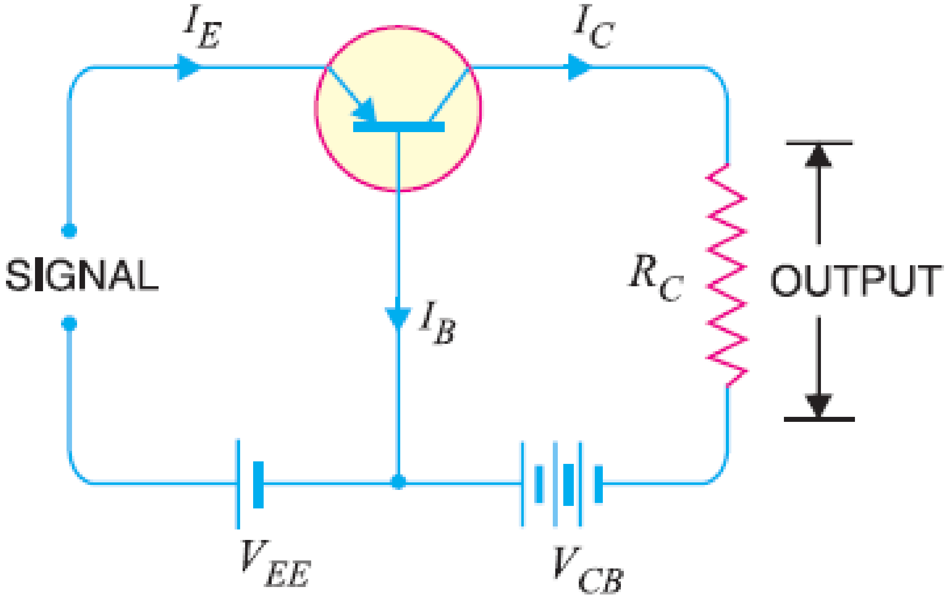
Common Base

Common Emitter

Common Collector

COMMON BASE CONNECTION





The ratio of change in collector current to the change in emitter current at constant collector-base voltage VCB is known as **current amplification factor** *i.e.*

$$^{*}\alpha = \frac{\Delta I_C}{\Delta I_E} \text{ at constant } V_{CB}$$

If only d.c. values are considered, then $\alpha = I_C/I_E$

It is clear that current amplification factor is less than unity.

This value can be increased (but not more than unity) by decreasing the base current. This is achieved by making the base thin and doping it lightly.

Practical values of α in commercial transistors range from 0.9 to 0.99.

The total collector current consists of :

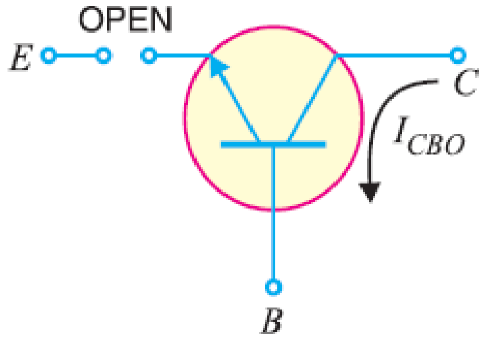
(*i*) That part of emitter current which reaches the collector terminal *i.e.* αI_E.

(*ii*) The leakage current $I_{leakage}$. This current is due to the movement of minority carriers across base-collector junction on account of it being reverse biased. This is generally much smaller than αI_E.

$$\text{Total collector current,} \quad I_C = \alpha I_E + I_{leakage}$$

It is clear that if *IE* = 0 (*i.e.*, emitter circuit is open), a small leakage current still flows in the collector circuit.

This Il_{eakage} is abbreviated as I_{CBO}, meaning collector-base current with emitter open. The I_{CBO} is indicated in Fig.



$$\therefore \quad I_C = \alpha I_E + I_{CBO}$$

Now $$I_E = I_C + I_B$$

$$\therefore \quad I_C = \alpha (I_C + I_B) + I_{CBO}$$

or $$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

or $$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

Characteristics of Common Base Connection

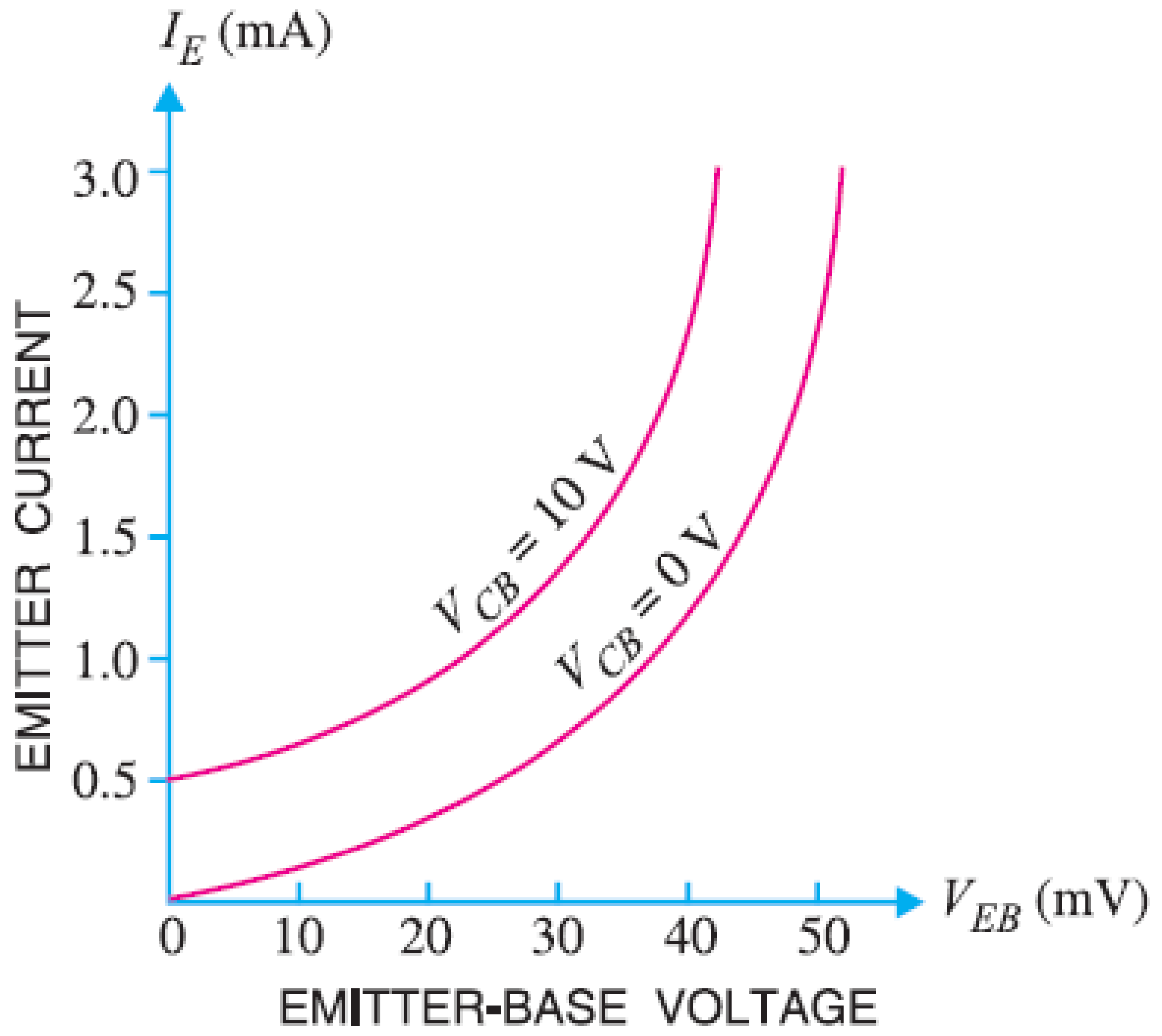
Input characteristic. It is the curve between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}. The emitter current is generally taken along *y*-axis and emitter-base voltage along *x*-axis.

(*i*) The emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}. It means that input resistance is very small.

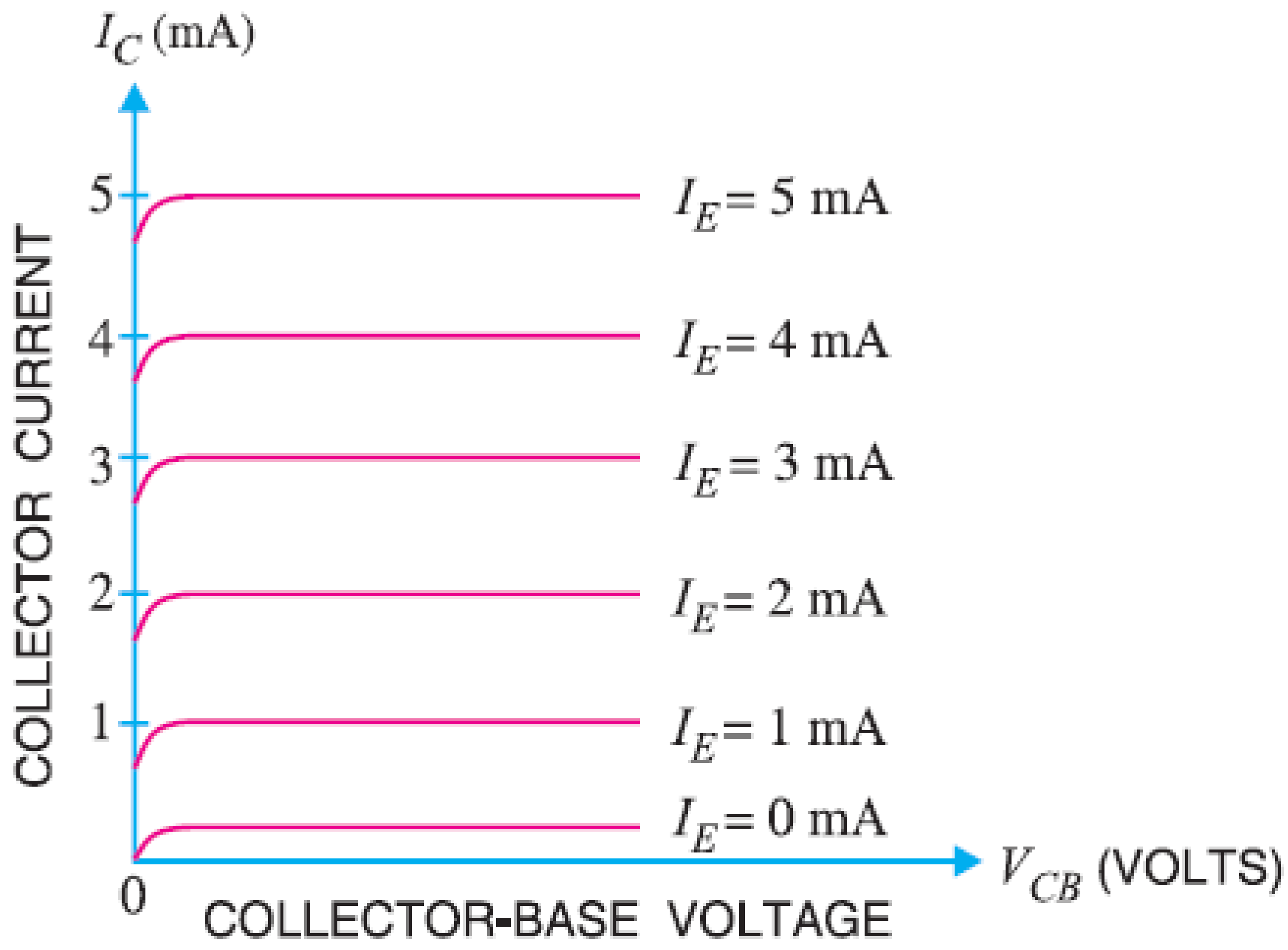
(*ii*) The emitter current is almost independent of collector-base voltage V_{CB}. This leads to the conclusion that emitter current (and hence collector current) is almost independent of collector voltage.

Input resistance. It is the ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB})

$$\text{Input resistance, } r_i = \frac{\Delta V_{BE}}{\Delta I_E} \text{ at constant } V_{CB}$$



I_E (mA)
3.0
2.5
2.0
1.5
1.0
0.5
EMITTER CURRENT
$V_{CB} = 10$ V
$V_{CB} = 0$ V
0
10
20
30
40
50
V_{EB} (mV)
EMITTER-BASE VOLTAGE



I_C (mA)
COLLECTOR CURRENT
5
4
3
2
1
0
$I_E = 5$ mA
$I_E = 4$ mA
$I_E = 3$ mA
$I_E = 2$ mA
$I_E = 1$ mA
$I_E = 0$ mA
V_{CB} (VOLTS)
COLLECTOR-BASE VOLTAGE

It is the curve between collector current I_C and collector-base voltage V_{CB} at constant emitter current I_E.

(i) The collector current I_C varies with V_{CB} only at very low voltages (< 1V). The transistor is never operated in this region.

(ii) When the value of V_{CB} is raised above 1 − 2 V, the collector current becomes constant as indicated by straight horizontal curves. It means that now I_C is independent of V_{CB} and depends upon IE only. This is consistent with the theory that the emitter current flows almost entirely to the collector terminal. The transistor is always operated in this region.

(iii) A very large change in collector-base voltage produces only a tiny change in collector current.
This means that output resistance is very high.

Ex. For the common base circuit shown in Fig., determine I_C and V_{CB}. Assume the transistor to be of silicon.

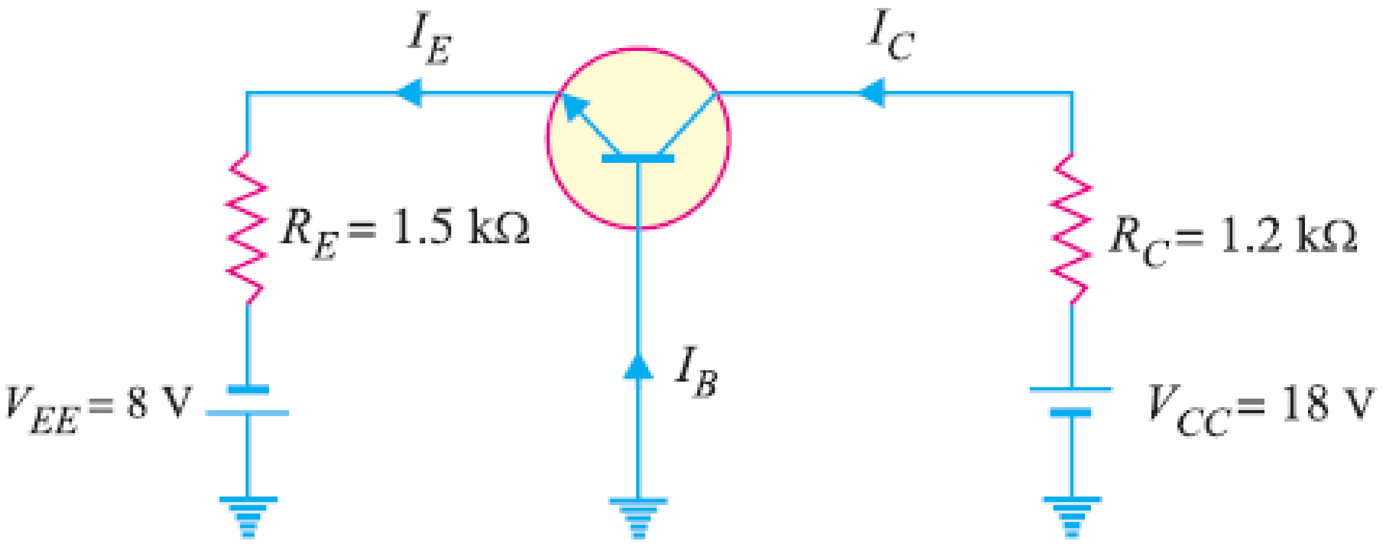
Since the transistor is of silicon, V_{BE} = 0.7V. Applying Kirchhoff's voltage law to the emitter-side loop, we get

$$V_{EE} = I_E R_E + V_{BE}$$

or $$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{8V - 0.7V}{1.5\ \text{k}\Omega} = 4.87\ \text{mA}$$

$$\therefore \quad I_C \simeq I_E = \mathbf{4.87\ mA}$$



Applying Kirchhoff's voltage law to the collector-side loop, we have,

$$V_{CC} = I_C R_C + V_{CB}$$

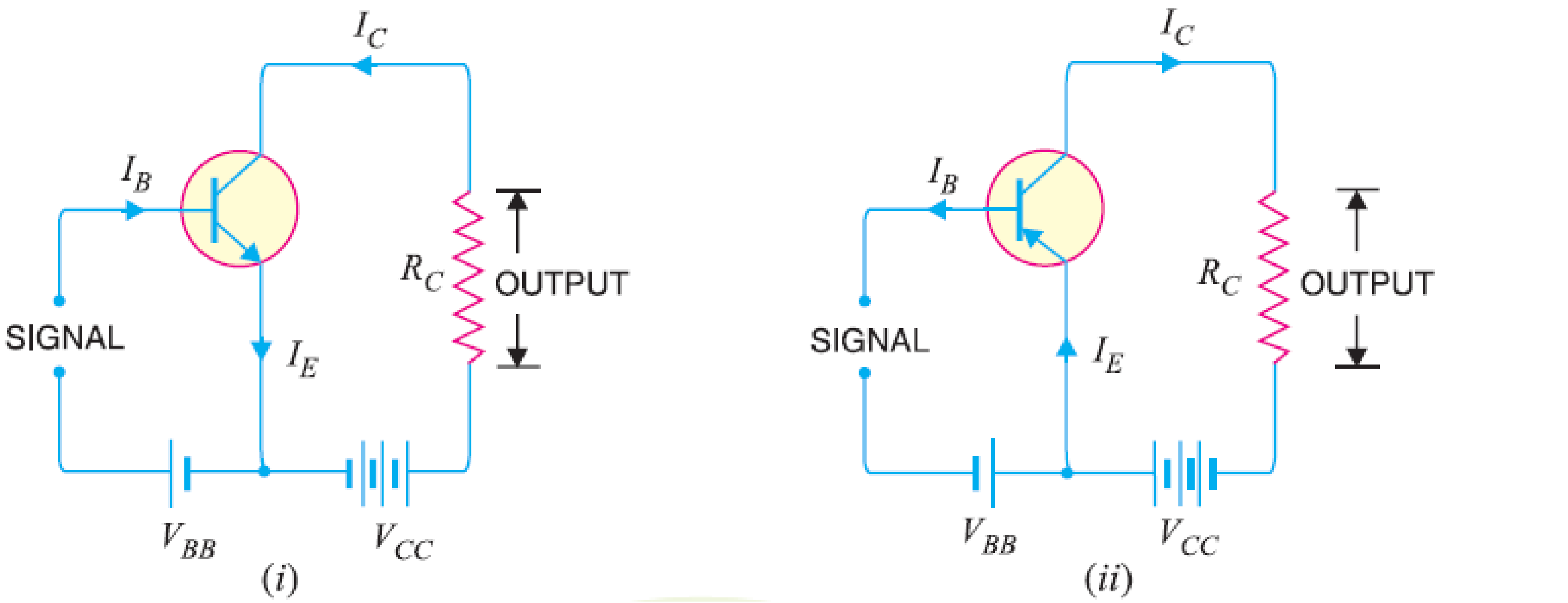
$$\therefore \quad V_{CB} = V_{CC} - I_C R_C$$

$$= 18\ \text{V} - 4.87\ \text{mA} \times 1.2\ \text{k}\Omega = \mathbf{12.16\ V}$$

Common Emitter Connection

In this circuit arrangement, input is applied between base and emitter and output is taken from the collector and emitter.

Here, emitter of the transistor is common to both input and output circuits and hence the name common emitter connection.



1. Base current amplification factor (β). In common emitter connection, input current is I_B and output current is I_C.

The ratio of change in collector current (ΔI_C) *to the change in base current* (ΔI_B) *is known as* **base current amplification factor** *i.e.*

$$\beta^* = \frac{\Delta I_C}{\Delta I_B}$$

In almost any transistor, less than 5% of emitter current flows as the base current. Therefore, the value of β is generally greater than 20.

Usually, its value ranges from 20 to 500. This type of connection is frequently used as it gives appreciable current gain as well as voltage gain.

Relation between β and α. A simple relation exists between β and α. This can be derived as follows :

$$\beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{...}(i)$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \text{...}(ii)$$

Now $I_E = I_B + I_C$

or $\Delta I_E = \Delta I_B + \Delta I_C$

or $\Delta I_B = \Delta I_E - \Delta I_C$

Substituting the value of ΔI_B in exp. (*i*), we get,

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} \quad \text{...}(iii)$$

Dividing the numerator and denominator of R.H.S. of exp. (*iii*) by ΔI_E, we get,

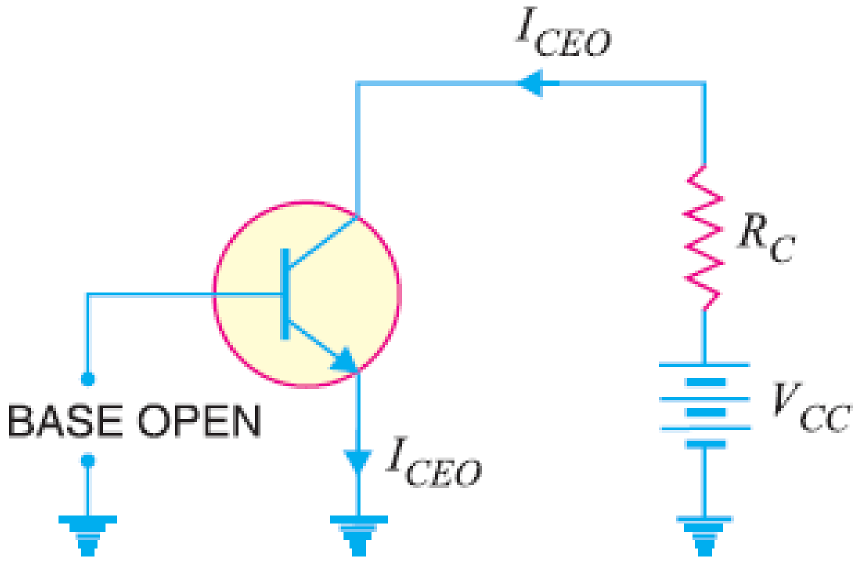
$$\beta = \frac{\Delta I_C / \Delta I_E}{\dfrac{\Delta I_E}{\Delta I_E} - \dfrac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1-\alpha} \quad \left[\because \ \alpha = \frac{\Delta I_C}{\Delta I_E}\right]$$

$\therefore$ $$\beta = \frac{\alpha}{1-\alpha}$$

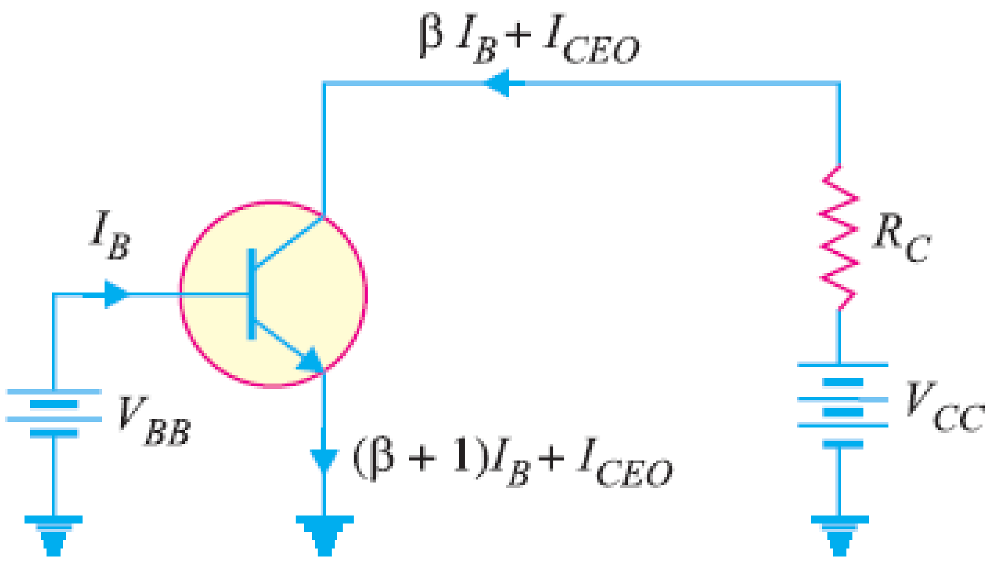
It is clear that as α approaches unity, β approaches infinity.

In other words, the current gain in common emitter connection is very high.

It is due to this reason that this circuit arrangement is used in about 90 to 95 percent of all transistor applications.



(i)



(ii)

2. Expression for collector current. In common emitter circuit, I_B is the input current and I_C is the output current.

$$\text{We know } I_E = I_B + I_C \qquad \text{...}(i)$$

and

$$I_C = \alpha I_E + I_{CBO} \qquad \text{...}(ii)$$

From exp. (*ii*), we get,

$$I_C = \alpha I_E + I_{CBO} = \alpha (I_B + I_C) + I_{CBO}$$

or

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

or

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \qquad \text{...}(iii)$$

From exp. (*iii*), it is apparent that if $I_B = 0$ (*i.e.* base circuit is open), the collector current will be the current to the emitter. This is abbreviated as I_{CEO}, meaning collector-emitter current with base open.

$$\therefore \quad I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$

Substituting the value of $\frac{1}{1-\alpha} I_{CBO} = I_{CEO}$ in exp. (*iii*), we get,

$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO}$$

or

$$I_C = \beta I_B + I_{CEO} \qquad \left(\because \beta = \frac{\alpha}{1-\alpha} \right)$$

When the base voltage is applied as shown in Fig. (*ii*), then the various currents are :

$$\text{Base current} = I_B$$

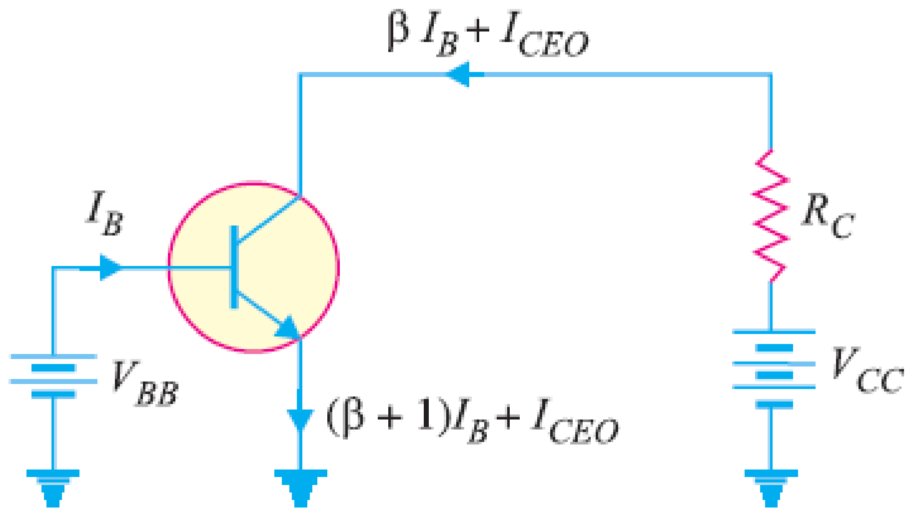
$$\text{Collector current} = \beta I_B + I_{CEO}$$

$$\text{Emitter current} = \text{Collector current} + \text{Base current}$$

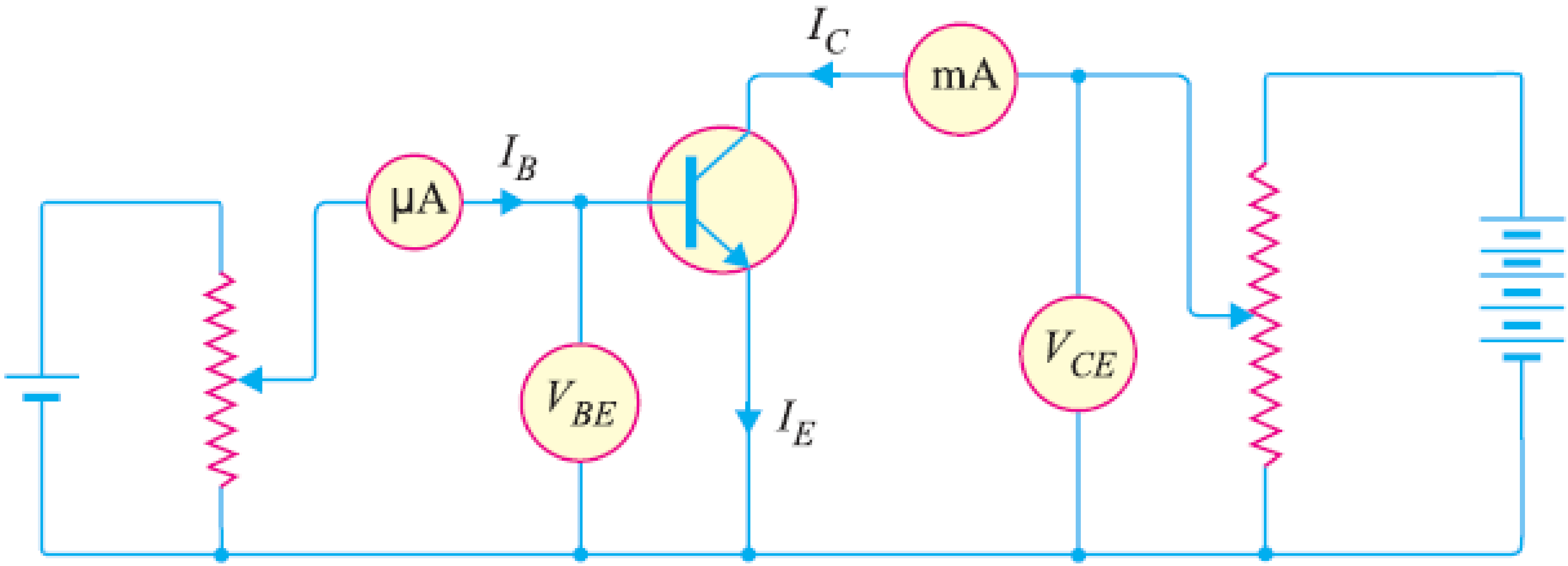
$$= (\beta I_B + I_{CEO}) + I_B = (\beta + 1) I_B + I_{CEO}$$

It may be noted here that :

$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO} = (\beta + 1) I_{CBO} \qquad \left[\because \frac{1}{1-\alpha} = \beta + 1\right]$$



Characteristics of Common Emitter Connection



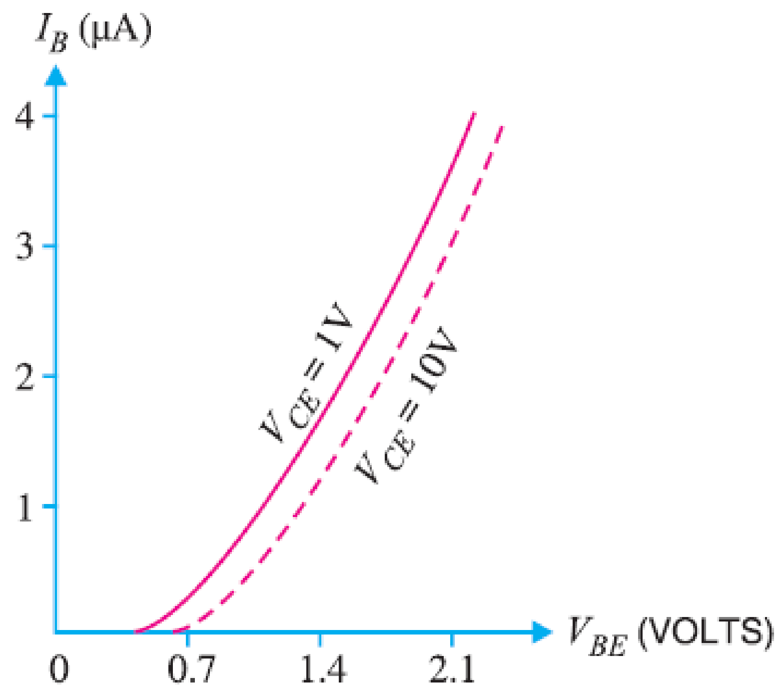
Input characteristic: *It is the curve between base current I_B and base-emitter voltage V_{BE} at a constant collector-emitter voltage V_{CE}.*

The following points may be noted from the characteristics :

(*i*) The characteristic resembles that of a forward biased diode curve. (since the base-emitter section is forward biased)

(*ii*) As compared to *CB* arrangement, I_B increases less rapidly with V_{BE}. Therefore, input resistance of a *CE* circuit is higher than that of *CB* circuit.

Input resistance. It is the ratio of change in base-emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant V_{CE} *i.e.*

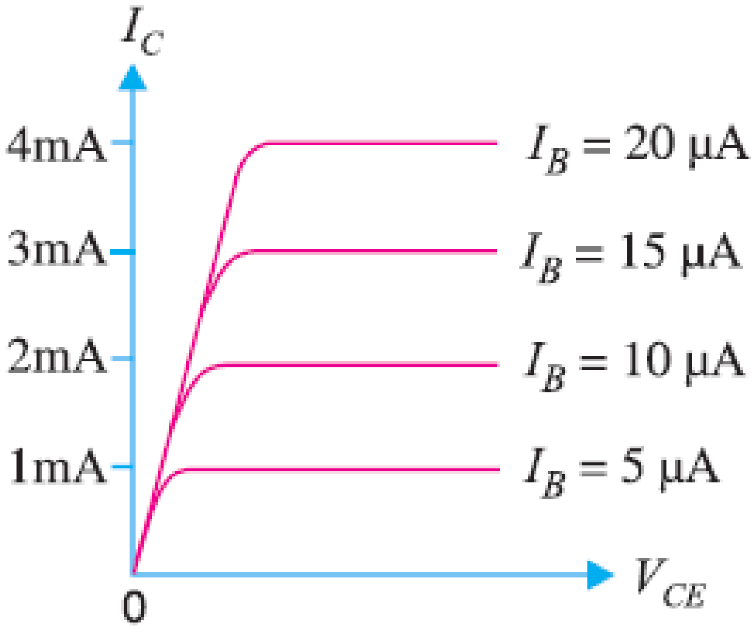


$$\text{Input resistance, } \quad r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$

Output characteristic. *It is the curve between collector current I_C and collector-emitter voltage V_{CE} at constant base current I_B.*

The following points may be noted from the characteristics:

(i) The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V only. After this, collector current becomes *almost* constant and independent of V_{CE}.



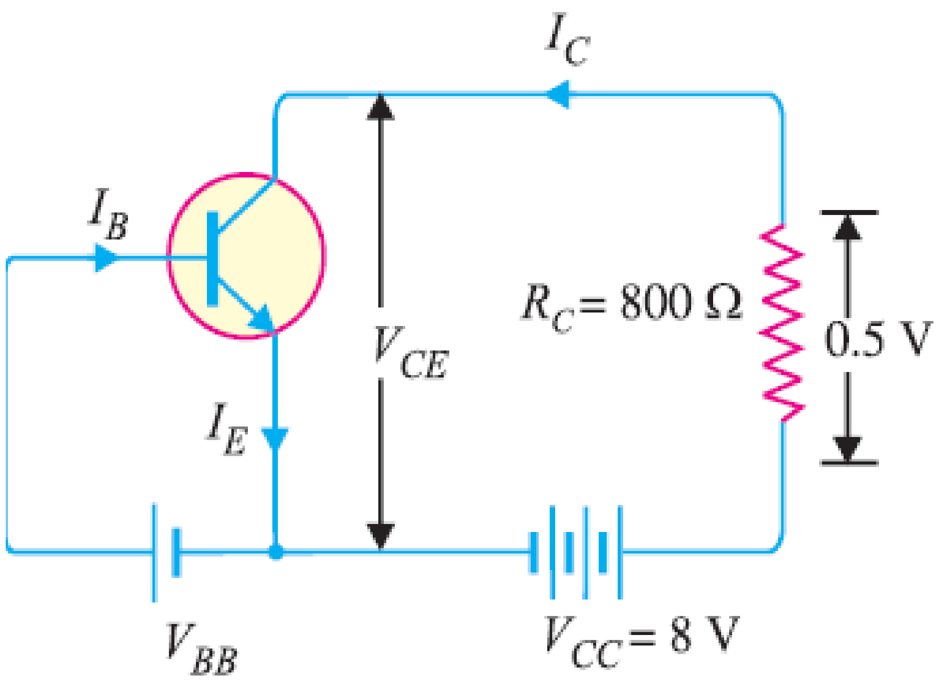
This value of V_{CE} upto which collector current I_C changes with V_{CE} is called the *knee voltage* (V_{knee}). *The transistors are always operated in the region above knee voltage.*

(*ii*) Above knee voltage, I_C is almost constant. However, a small increase in I_C with increasing V_{CE} is caused by the collector depletion layer getting wider and capturing a few more majority carriers before electron-hole combinations occur in the base area.

(*iii*) For any value of V_{CE} above knee voltage, the collector current I_C is approximately equal to $\beta \times I_B$.

$$\text{Output resistance, } r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

A transistor is connected in common emitter (CE) configuration in which collector supply is 8V and the voltage drop across resistance Rc connected in the collector circuit is 0.5V. The value of Rc = 800 Ω.
If α = 0.96, determine :
(i) collector-emitter voltage
(ii) base current



Solution. Fig. 8.22 shows the required common emitter connection with various values.

(*i*) Collector-emitter voltage,

$$V_{CE} = V_{CC} - 0.5 = 8 - 0.5 = \mathbf{7.5\ V}$$

(*ii*) The voltage drop across R_C (= 800 Ω) is 0.5 V.

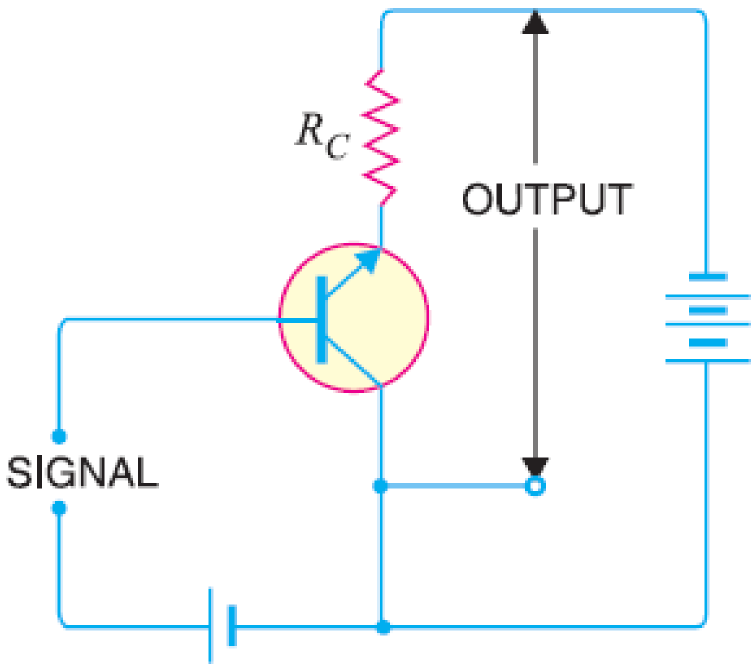
$$\therefore \quad I_C = \frac{0.5\ \text{V}}{800\ \Omega} = \frac{5}{8}\ \text{mA} = 0.625\ \text{mA}$$

$$\text{Now} \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = 24$$

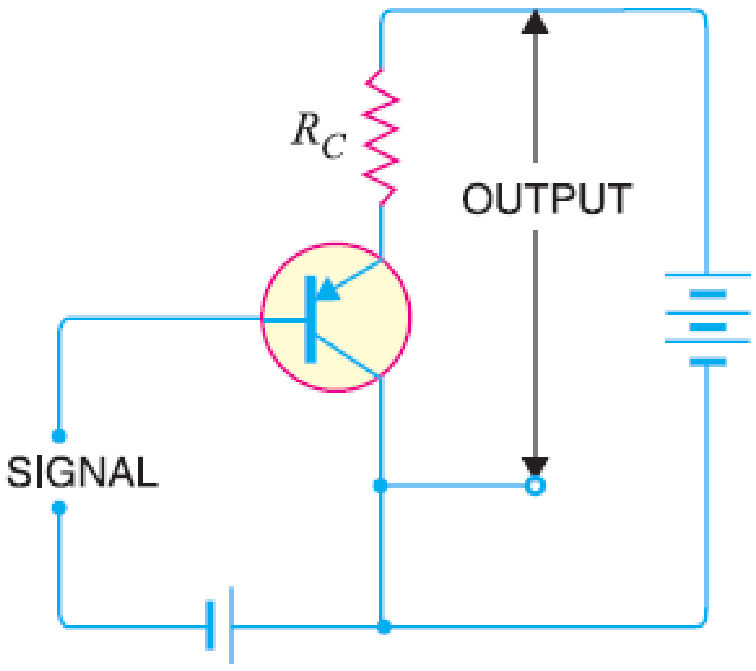
$$\therefore \quad \text{Base current, } I_B = \frac{I_C}{\beta} = \frac{0.625}{24} = \mathbf{0.026\ mA}$$

Common Collector Connection

In this circuit arrangement, input is applied between base and collector while output is taken between the emitter and collector.



(i)



(ii)

(i) Current amplification factor γ. In common collector circuit, input current is the base current I_B and output current is the emitter current I_E. Therefore, current amplification in this circuit arrangement can be defined as under :

The ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as **current amplification factor** *in common collector (CC) arrangement i.e.*

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Relation between γ and α

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \qquad ...(i)$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \qquad ...(ii)$$

Now $$I_E = I_B + I_C$$

or $$\Delta I_E = \Delta I_B + \Delta I_C$$

or $$\Delta I_B = \Delta I_E - \Delta I_C$$

Substituting the value of ΔI_B in exp. (i), we get,

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator of R.H.S. by ΔI_E, we get,

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha} \qquad \left(\because \alpha = \frac{\Delta I_C}{\Delta I_E}\right)$$

$\therefore$ $$\gamma = \frac{1}{1-\alpha}$$

(*ii*) Expression for collector current

We know $$I_C = \alpha I_E + I_{CBO}$$

Also $$I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$$

$$\therefore \quad I_E(1-\alpha) = I_B + I_{CBO}$$

or $$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

or $$I_C \simeq I_E = {}^{*}(\beta+1)\, I_B + (\beta+1)\, I_{CBO}$$

(*iii*) Applications. The common collector circuit has very high input resistance (about 750 kΩ) and very low output resistance (about 25 Ω). Due to this reason, the voltage gain provided by this circuit is always less than 1. Therefore, this circuit arrangement is seldom used for amplification.

However, due to relatively high input resistance and low output resistance, this circuit is primarily used for impedance matching *i.e.* for driving a low impedance load from a high impedance source.

Comparison of Transistor Connections

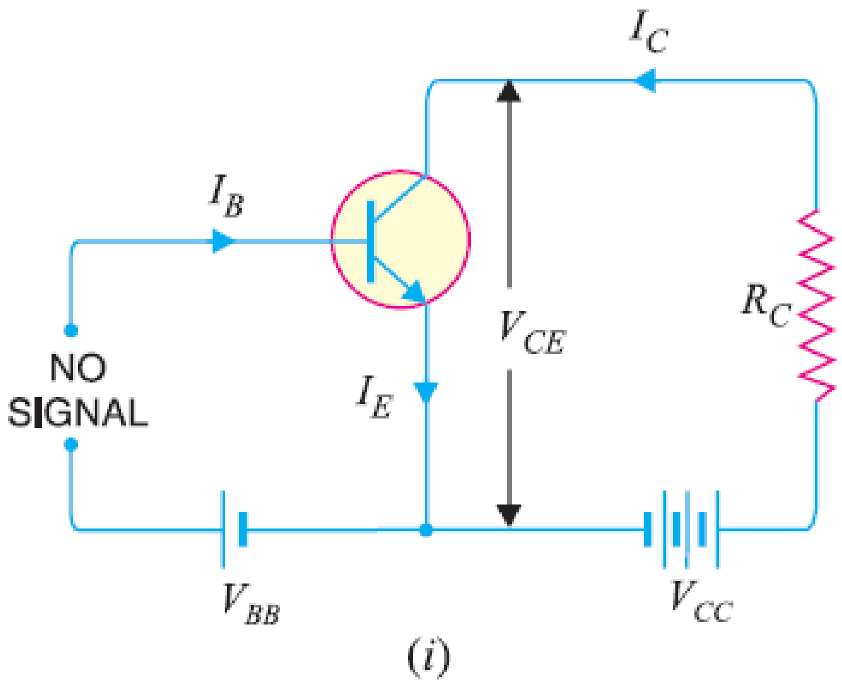
S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

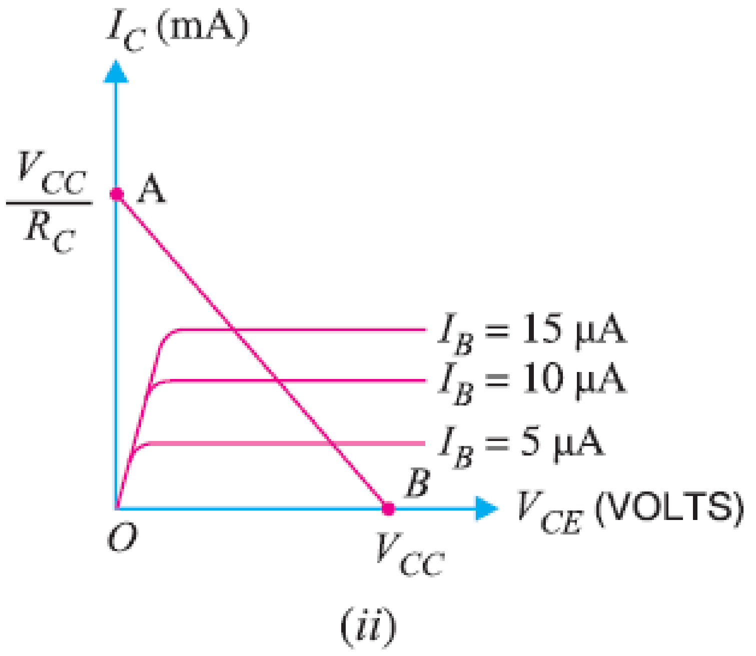
Transistor Load Line Analysis

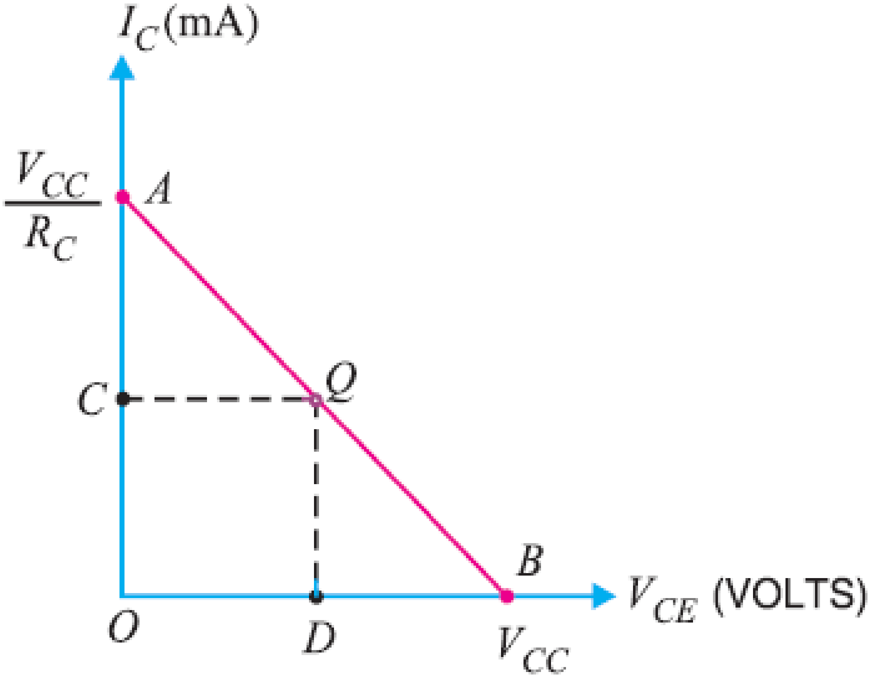
Consider a common emitter *npn* transistor circuit shown in Fig. where no signal is applied. Therefore, d.c. conditions prevail in the circuit. The output characteristics of this circuit are shown in Fig.

The value of collector-emitter voltage V_{CE} at any time is given by

$V_{CE} = V_{CC} - I_C R_C$







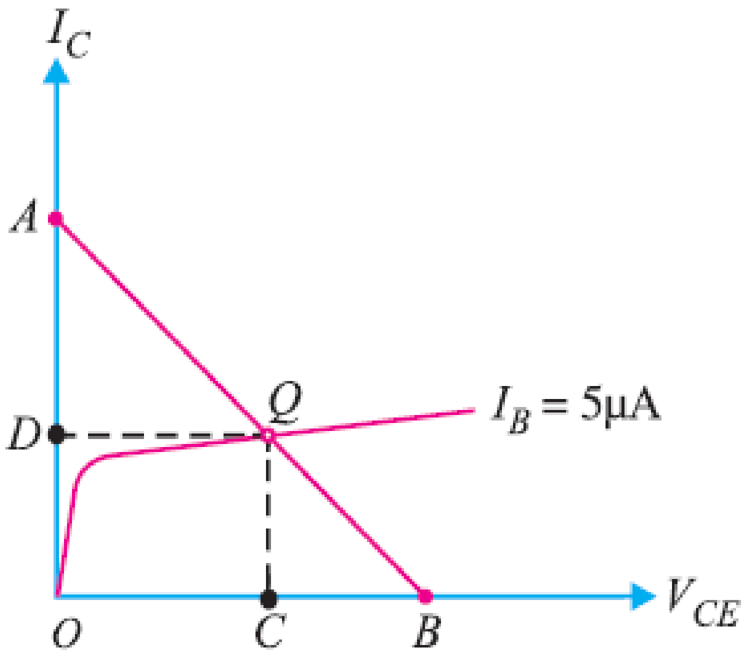
Importance. The current (I_C) and voltage (V_{CE}) conditions in the transistor circuit are represented by some point on the output characteristics.

The same information can be obtained from the load line. Thus when I_C is maximum ($= V_{CC}/R_C$), then $V_{CE} = 0$ as shown in Fig. above. If $I_C = 0$, then V_{CE} is maximum and is equal to V_{CC}. For any other value of collector current say OC, the collector-emitter voltage V_{CE} = OD.

Operating Point

The zero signal values of I_C and V_{CE} are known as the operating point. It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied.

It is also called quiescent (silent) point or Q-point because it is the point on $I_C - V_{CE}$ characteristic when the transistor is silent i.e. in the absence of the signal.



For the circuit shown in Fig. below, draw the d.c. load line.

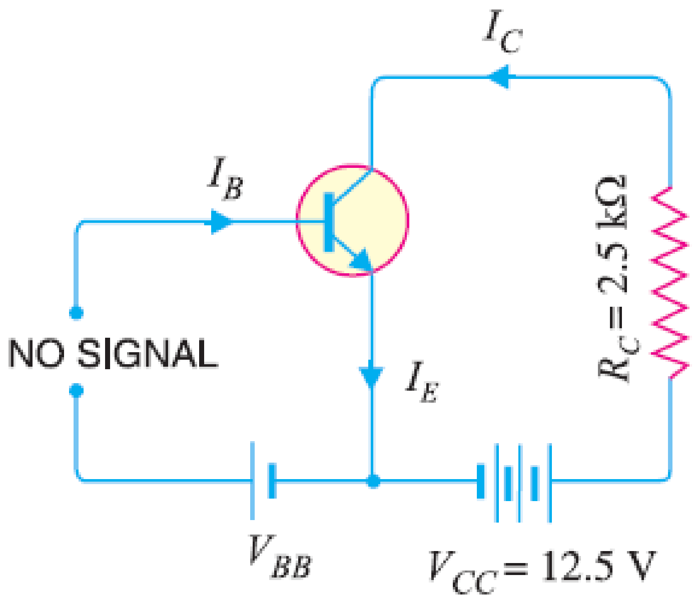
Solution. The collector-emitter voltage V_{CE} is given by ;

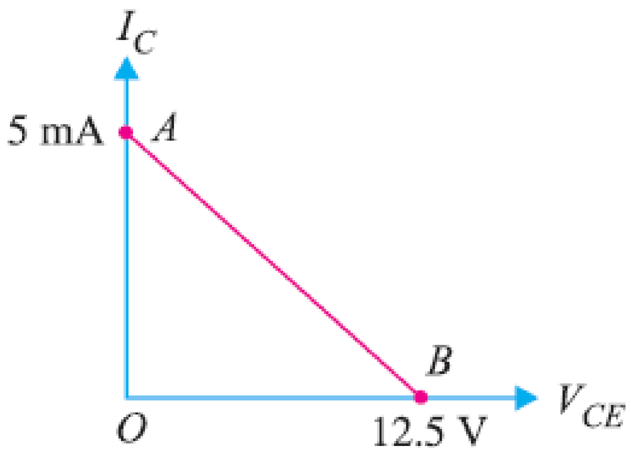
$$V_{CE} = V_{CC} - I_C R_C \qquad \text{...(i)}$$

$$\text{When } I_C = 0, \text{ then,}$$

$$V_{CE} = V_{CC} = 12.5 \text{ V}$$

This locates the point B of the load line on the collector-emitter voltage axis.





In the circuit diagram shown in Fig. below, if Vcc = 12V and Rc = 6 kΩ, draw the d.c. load line. What will be the Q point if zero signal base current is 20μA and β = 50 ?

Solution. The collector-emitter voltage V_{CE} is given by :

$$V_{CE} = V_{CC} - I_C R_C$$

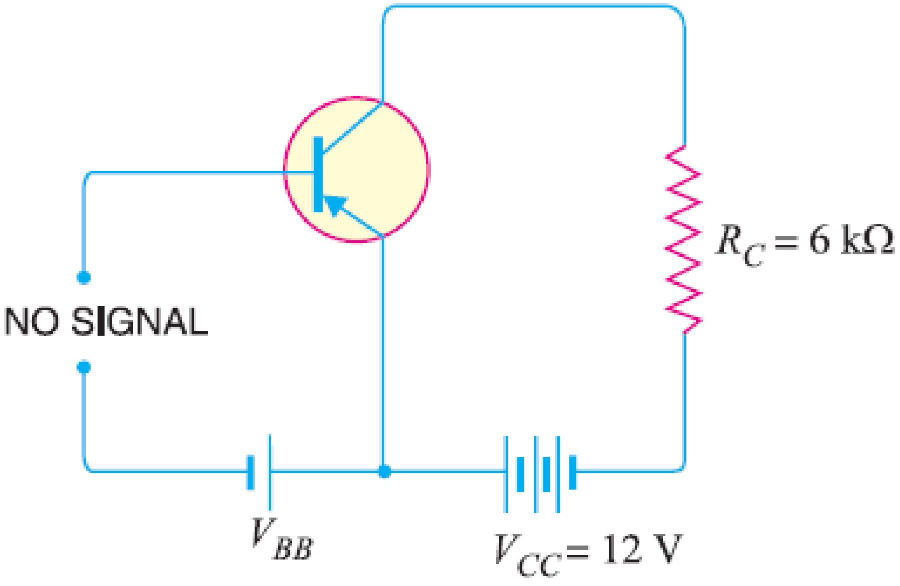
When $I_C = 0$, $V_{CE} = V_{CC} = 12$ V. This locates the point B of the load line. When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 12 \text{ V}/6 \text{ k}\Omega = 2$ mA. This locates the point A of the load line. By joining these two points, load line AB is constructed as shown in Fig. 8.39 (*ii*).

Zero signal base current, $I_B = 20\ \mu\text{A} = 0.02$ mA

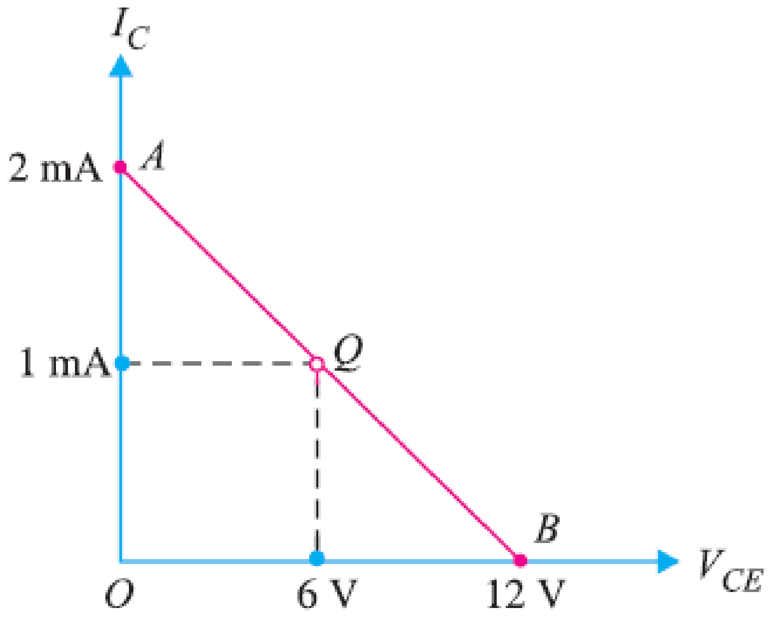
Current amplification factor, $\beta = 50$

$\therefore$ Zero signal collector current, $I_C = \beta I_B = 50 \times 0.02 = 1$ mA

The zero signal VCE is given by VCE = VCC – IC RC = 12- (1x6) = 6 V.



(*i*)



(*ii*)

Determine the Q point of the transistor circuit shown in Fig. below. Also draw the d.c. load line. Given β = 200 and VBE = 0.7V.

Solution. The presence of resistor R_B in the base circuit should not disturb you because we can apply Kirchhoff's voltage law to find the value of I_B and hence I_C ($= \beta I_B$). Referring to Fig. 8.40 and applying Kirchhoff's voltage law to base-emitter loop, we have,

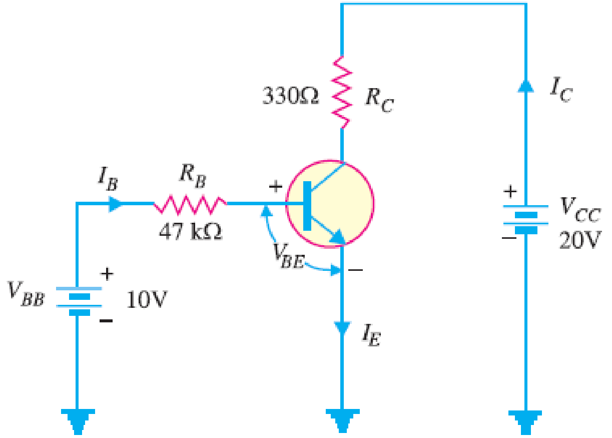
$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10V - 0.7V}{47\,k\Omega} = 198\ \mu A$$

Now $\quad I_C = \beta I_B = (200)(198\ \mu A) = 39.6\ mA$

Also $\quad V_{CE} = V_{CC} - I_C R_C = 20V - (39.6mA)(330\ \Omega) = 20V - 13.07V = 6.93V$

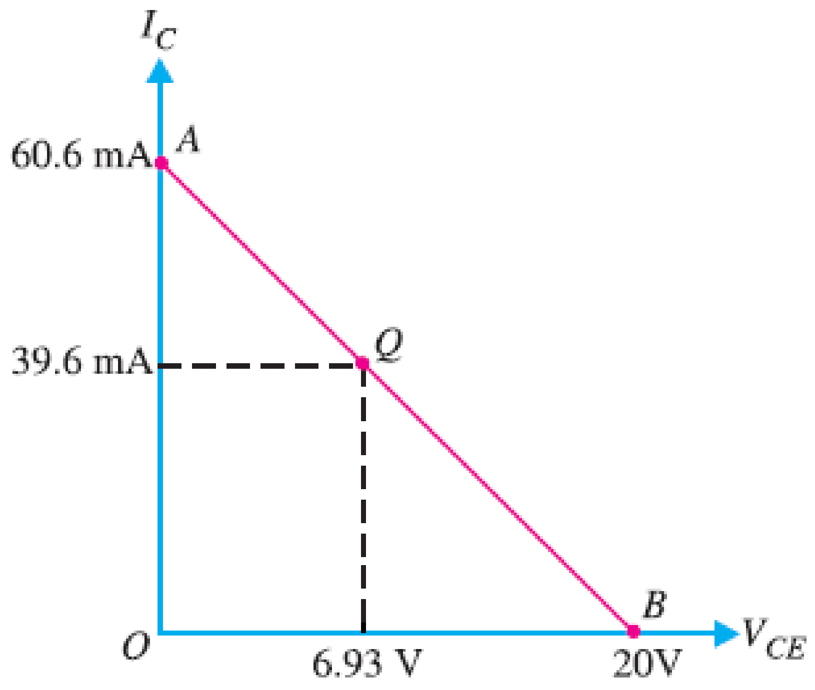
Therefore, the Q-point is I_C = **39.6 mA** and V_{CE} = **6.93V.**



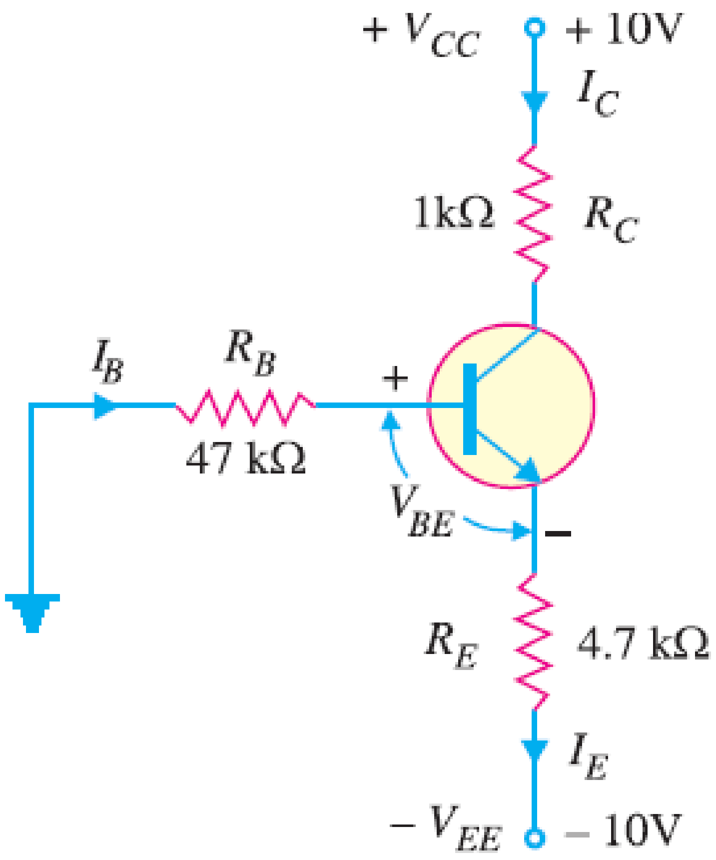
D.C. load line. In order to draw the d.c. load line, we need two end points.

$$V_{CE} = V_{CC} - I_C R_C$$

When $I_C = 0$, $V_{CE} = V_{CC} = 20V$. This locates the point B of the load line on the collector-emitter voltage axis as shown in Fig. 8.41. When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 20V/330\Omega = 60.6$ mA. This locates the point A of the load line on the collector current axis. By joining these two points, d.c. load line AB is constructed as shown in Fig. 8.41.



Determine the Q point of the transistor circuit shown in Fig. below. Also draw the d.c. load line. Given β = 100 and V_{BE} = 0.7V.



Solution. The transistor circuit shown in Fig. 8.42 may look complex but we can easily apply Kirchhoff's voltage law to find the various voltages and currents in the * circuit.

Applying Kirchhoff's voltage law to the base-emitter loop, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0 \quad \text{or} \quad V_{EE} = I_B R_B + I_E R_E + V_{BE}$$

Now $I_C = \beta I_B$ and $I_C \simeq I_E$. $\therefore$ $I_B = I_E/\beta$. Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or $$I_E\left(\frac{R_B}{\beta} + R_E\right) = V_{EE} - V_{BE} \quad \text{or} \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$, $$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{10\text{V} - 0.7\text{V}}{4.7\ \text{k}\Omega + 47\ \text{k}\Omega/100} = \frac{9.3\ \text{V}}{5.17\ \text{k}\Omega} = 1.8\ \text{mA}$$

Applying Kirchhoff's voltage law to the collector side, we have,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E + V_{EE} = 0$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

$$= 10\text{V} + 10\text{V} - 1.8\ \text{mA}\ (1\ \text{k}\Omega + 4.7\ \text{k}\Omega) = 9.74\text{V}$$

Therefore, the operating point of the circuit is I_C = **1.8 mA** and V_{CE} = **9.74V.**

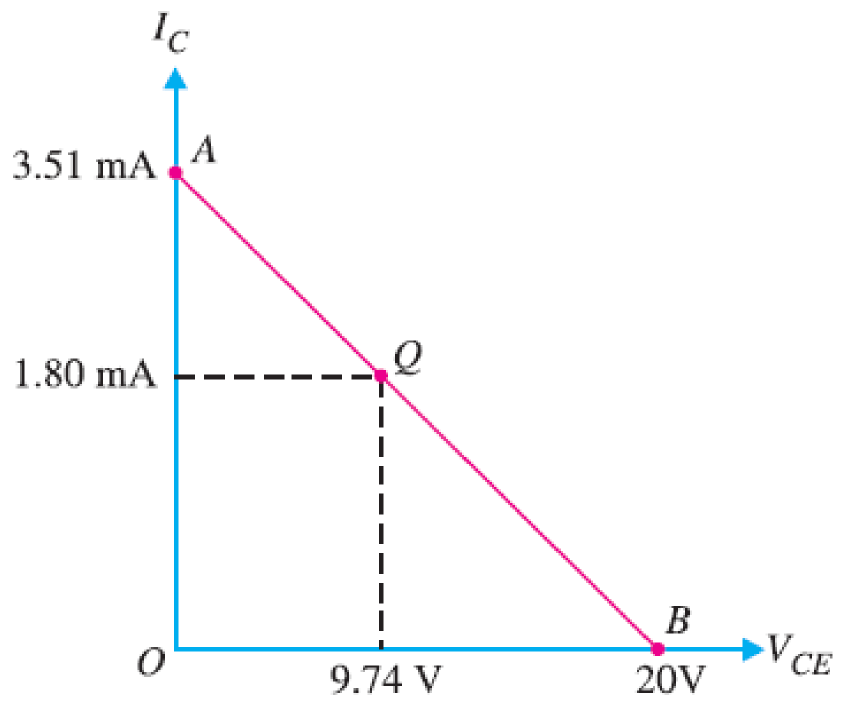
D.C. load line. The d.c. load line can be constructed as under :

$$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

When $I_C = 0$; $V_{CE} = V_{CC} + V_{EE} = 10V + 10V = 20V$. This locates the first point B ($OB = 20V$) of the load line on the collector-emitter voltage axis. When $V_{CE} = 0$,

$$I_C = \frac{V_{CC} + V_{EE}}{R_C + R_E} = \frac{10V + 10V}{1\,k\Omega + 4.7\,k\Omega} = \frac{20V}{5.7\,k\Omega} = 3.51 \text{ mA}$$

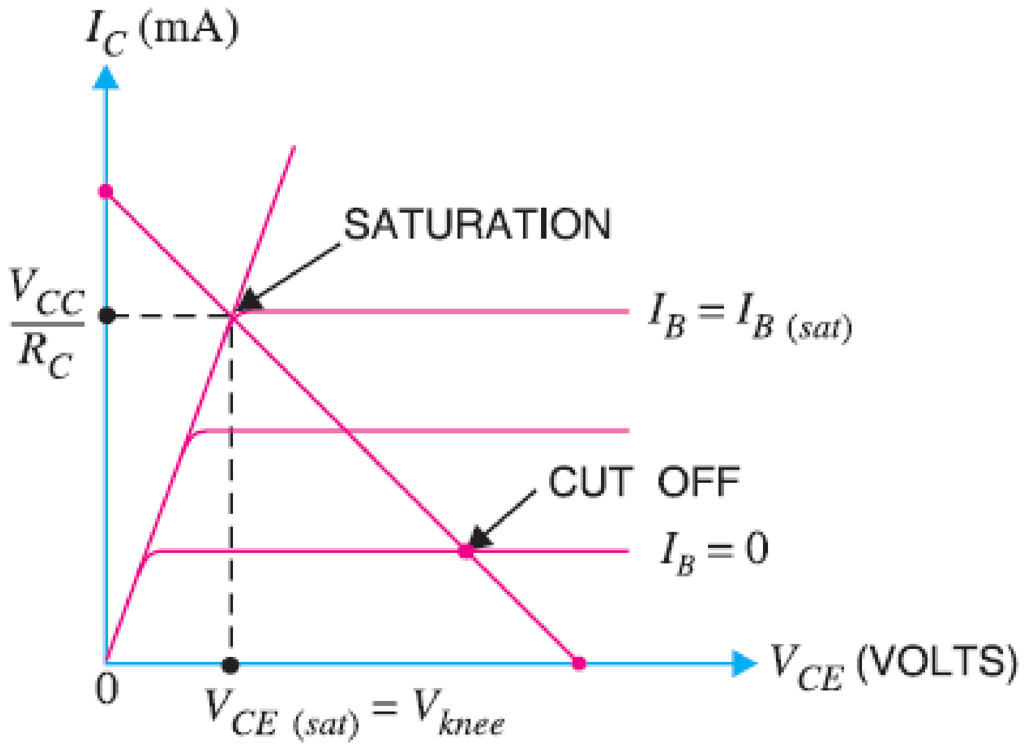
This locates the second point A ($OA = 3.51$ mA) of the load line on the collector current axis. By joining points A and B, d.c. load line AB is constructed as shown in Fig. 8.43.



Cut off and Saturation Points

(i) **Cut off:** The point where the load line intersects the $IB = 0$ curve is known as *cut off*. Both of the transistor junctions remains reverse biased.

(ii) **Saturation:** The point where the load line intersects the IB = IB(sat) curve is called saturation. Both of the transistor junctions remains forward biased

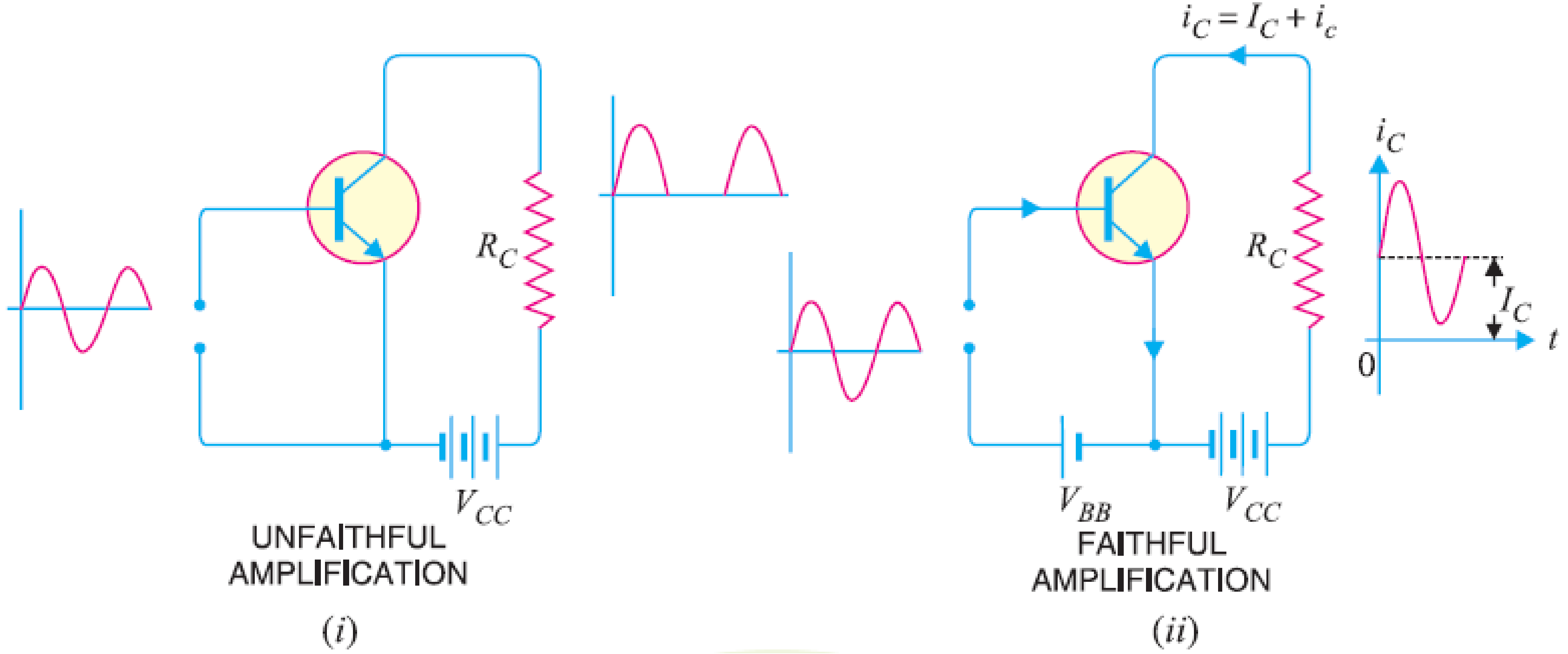


TRANSISTOR BIASING

The process of raising the strength of a weak signal without any change in its general shape is known as **faithful amplification.**

To ensure this, the following basic conditions must be satisfied :

(*i*) Proper zero signal collector current
(*ii*) Minimum proper base-emitter voltage (V_{BE}) at any instant
(*iii*) Minimum proper collector-emitter voltage (V_{CE}) at any instant



Now, introduce a battery source V_{BB} in the base circuit as shown in Fig. (*ii*). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as *zero signal collector current* I_C.

Stabilization

The collector current in a transistor changes rapidly when
(*i*) the temperature changes,
(*ii*) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

Need for stabilization. Stabilization of the operating point is necessary due to the following reasons :
(*i*) Temperature dependence of I_C
(*ii*) Individual variations
(*iii*) Thermal runaway

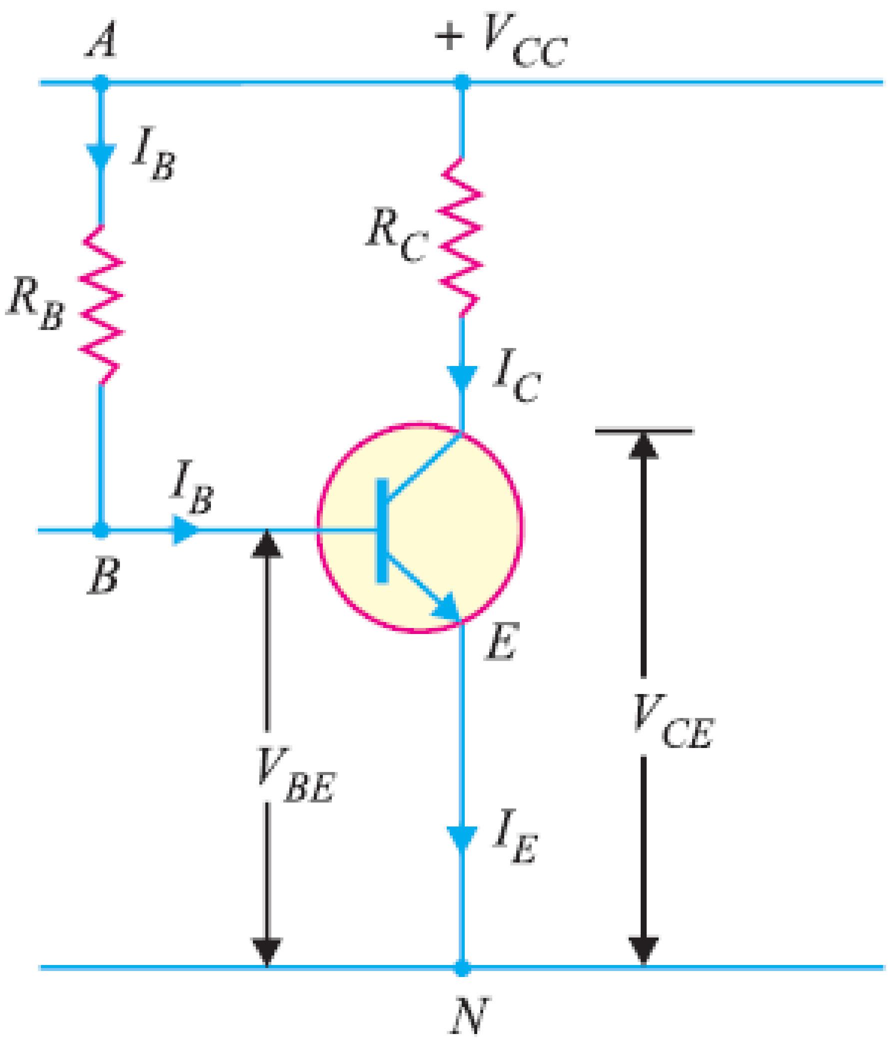
Methods of Transistor Biasing

(*i*) Base resistor method

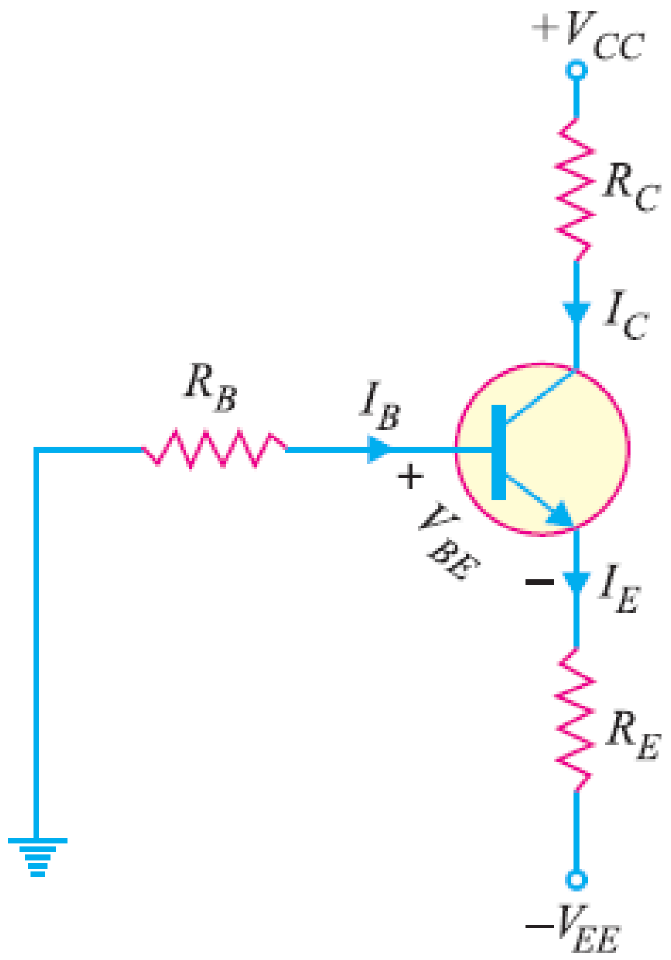
(*ii*) Emitter bias method

(*iii*) Biasing with collector-feedback resistor

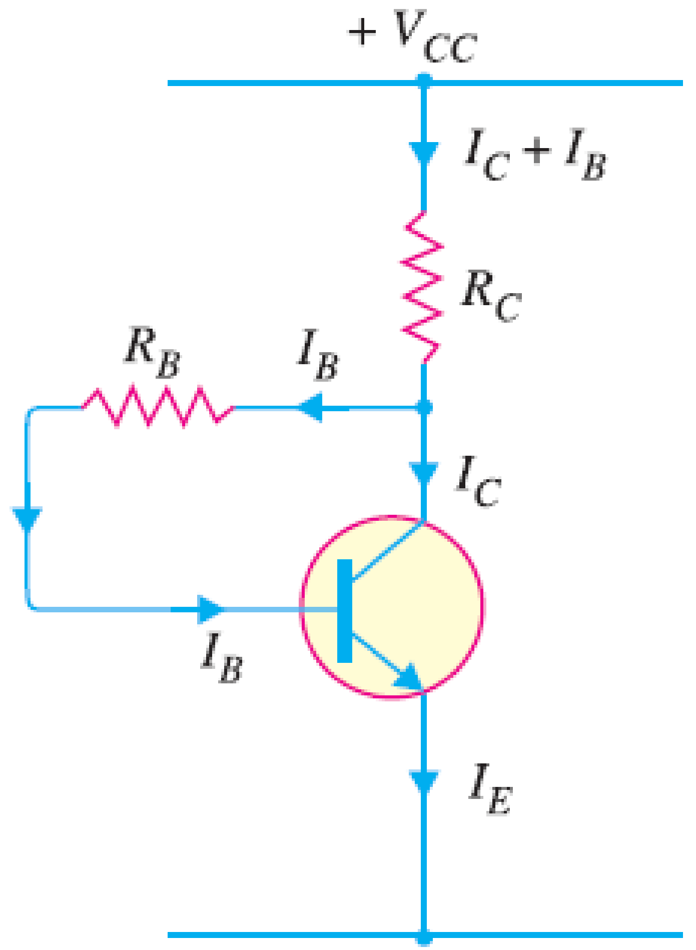
(*iv*) Voltage-divider bias



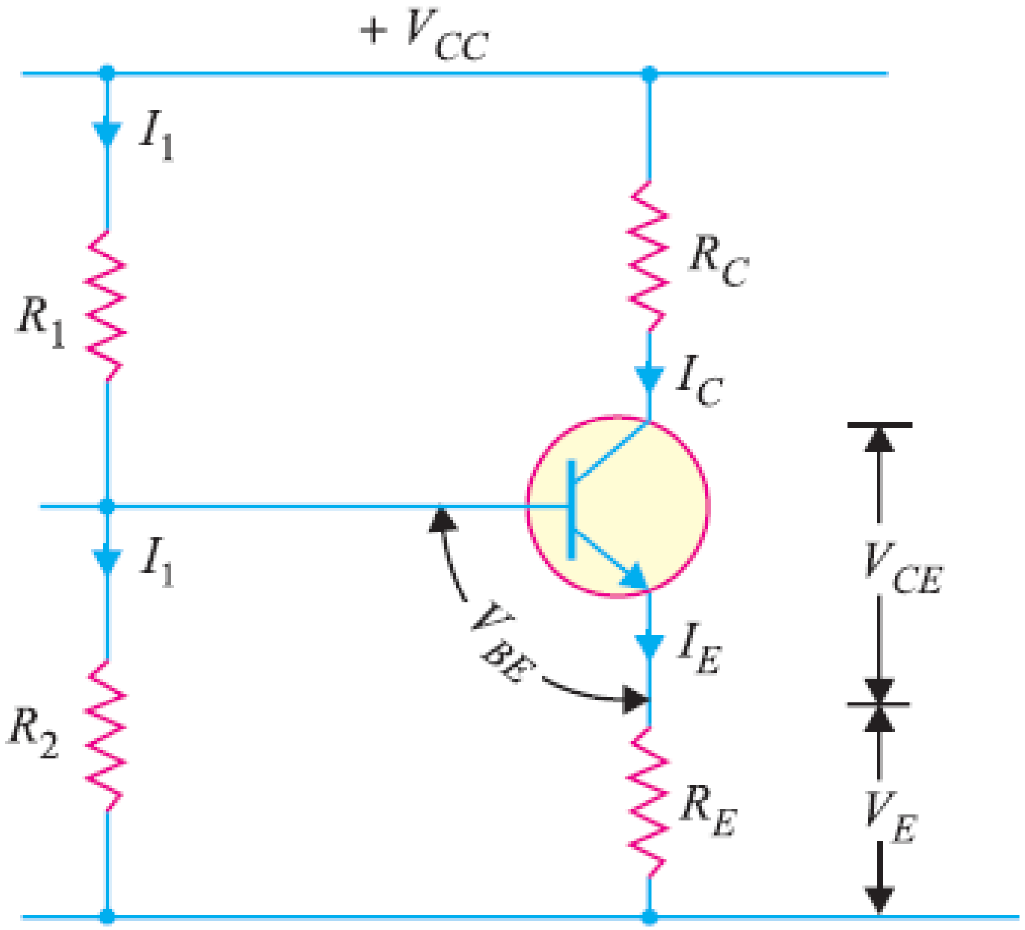
(*i*)



(ii)



(*iii*)



(iv)

FIELD EFFECT TRANSISTOR

The ordinary or bipolar transistor has two principal disadvantages.

- First, it has a low input impedance because of forward biased emitter junction.
- Secondly, it has considerable noise level.

- Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms.

- The field effect transistor (*FET*) has, by virtue of its construction and biasing, large input impedance which may be more than 100 megaohms.

- The *FET* is generally much less noisy than the ordinary or bipolar transistor.

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage.

However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current.

There are two types of FET:

(*i*) Junction field effect transistor (*JFET*)

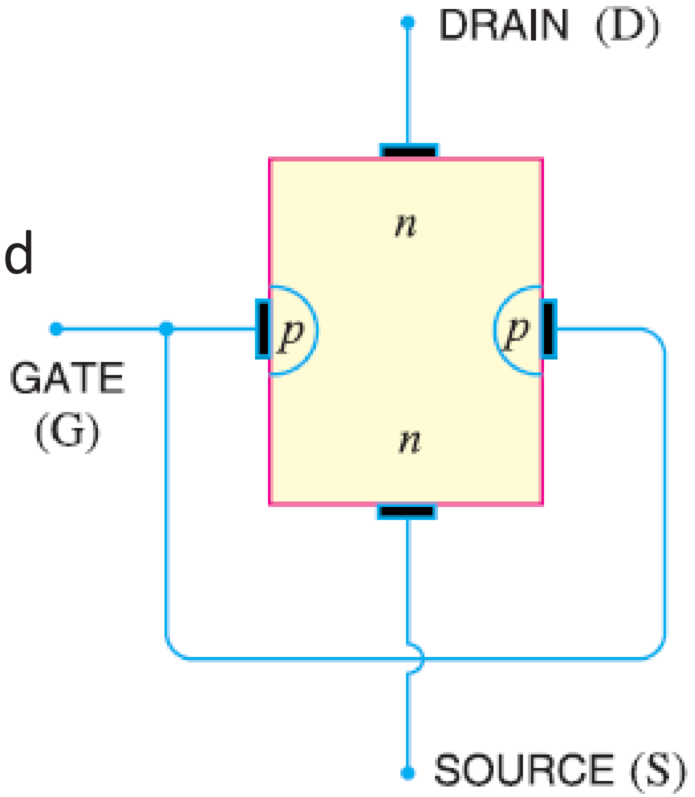
(*ii*) Metal oxide semiconductor field effect transistor (*MOSFET*)

A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig.

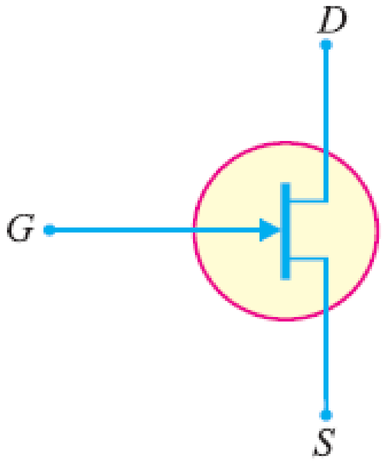
The bar forms the conducting channel for the charge carriers.
If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. and if the bar is of *p*-type, it is called a *p-channel JFET*.

The two *pn* junctions forming diodes are connected internally and a common terminal called *gate* is taken out.

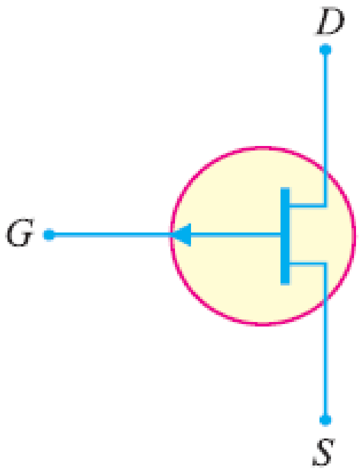
Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz*., *gate* (*G*), *source* (*S*) and *drain* (*D*).



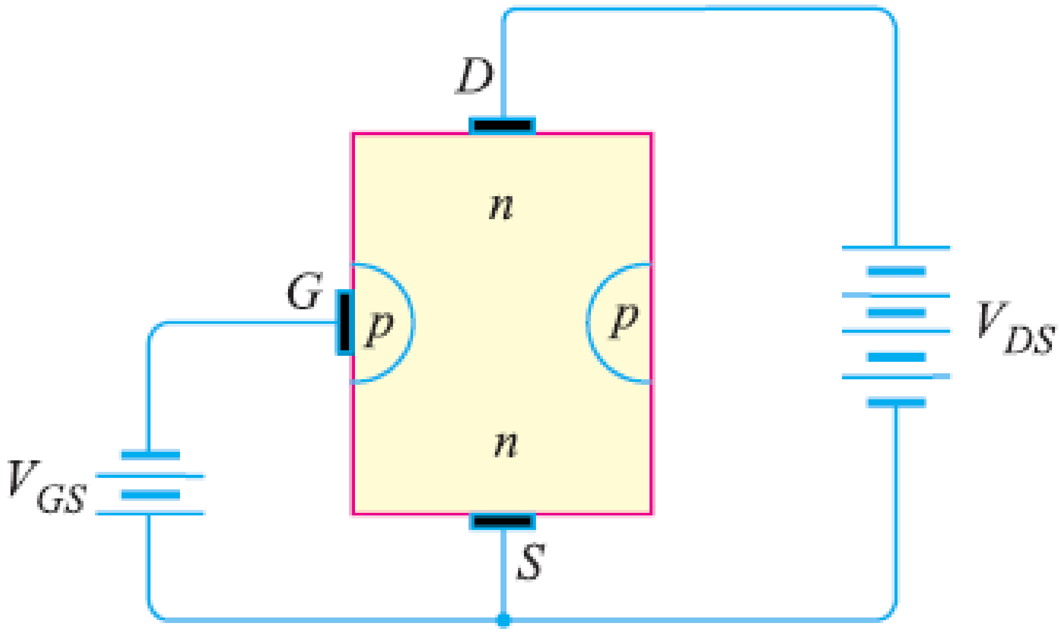
n-Channel JFET



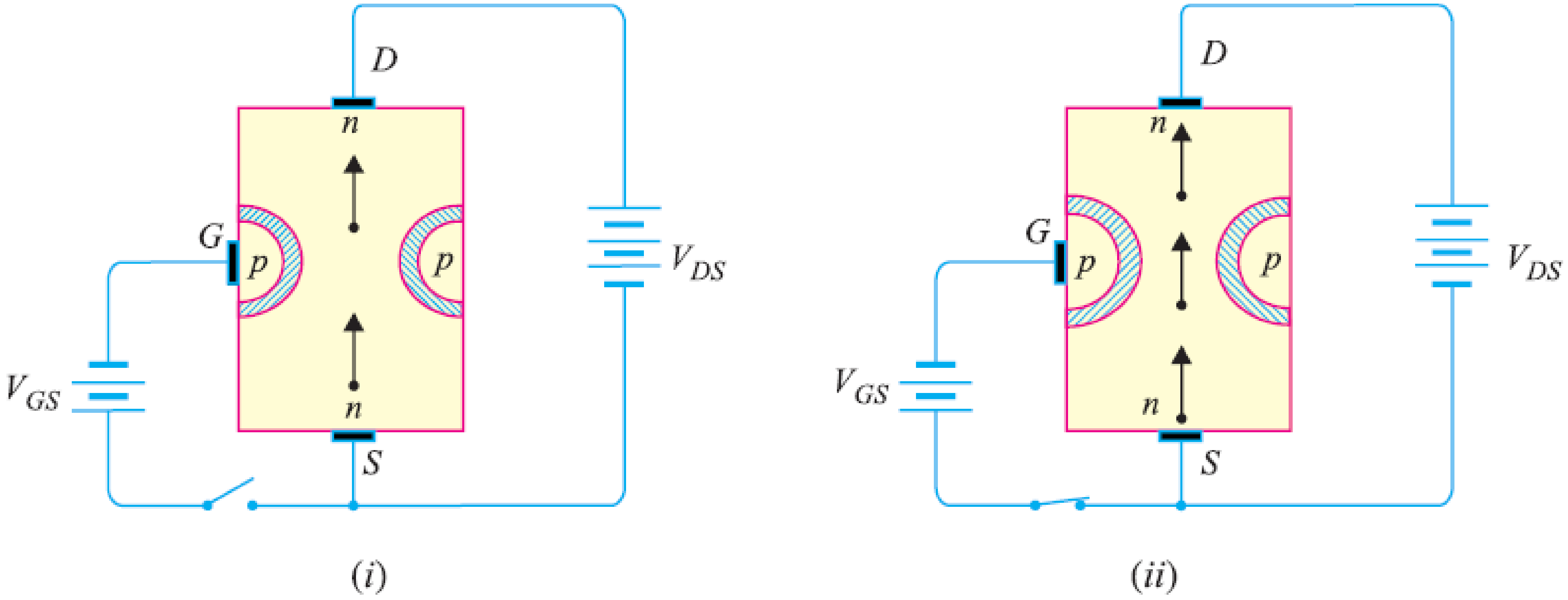
n-Channel *JFET*
(i)



p-Channel *JFET*
(ii)



Biasing of JFET transistor



Principle. The two *pn* junctions at the sides form two depletion layers. The current conduction by charge carriers (*i.e.* free electrons in this case) is through the channel between the two depletion layers and out of the drain.

The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS}.

The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel.

The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease.

Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}

Difference Between JFET and Bipolar Transistor

Unipolar transistor

High Input impedance

When Ig = 0, the current is nearly zero (1000 times less than current in BJT)

JFET gain is characterized as a transconductance i.e., the ratio of change in output current (drain current) to the input (gate) voltage.

No junction device

Output Characteristics of JFET

The following points may be noted from the characteristics :

(i) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant.

(ii) The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*.

(iii) Thus in Fig., *OA* is the *pinch off voltage* V_P.

(iv) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other.

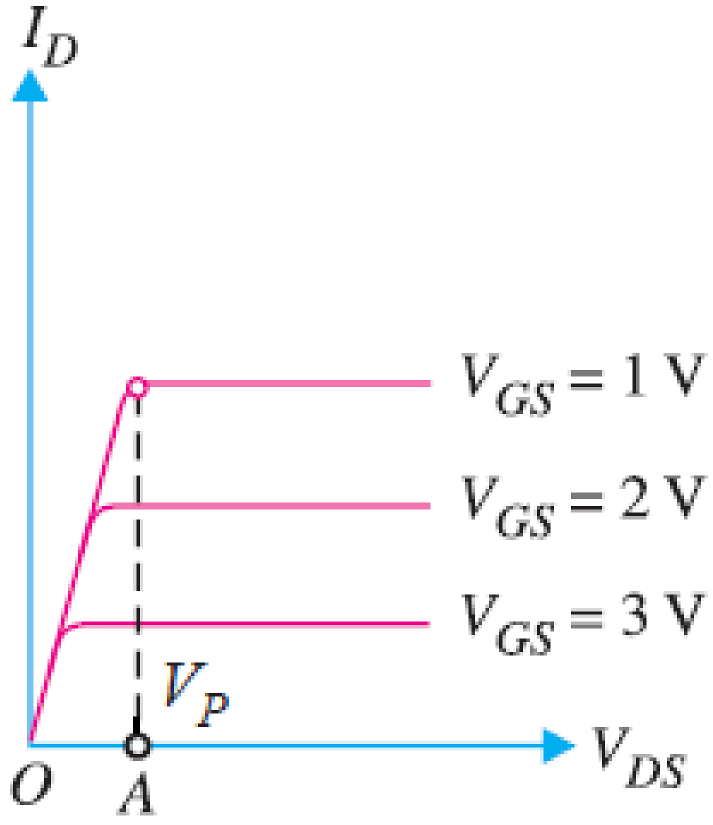
(v)The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage.

(vi) Consequently, drain current remains constant.

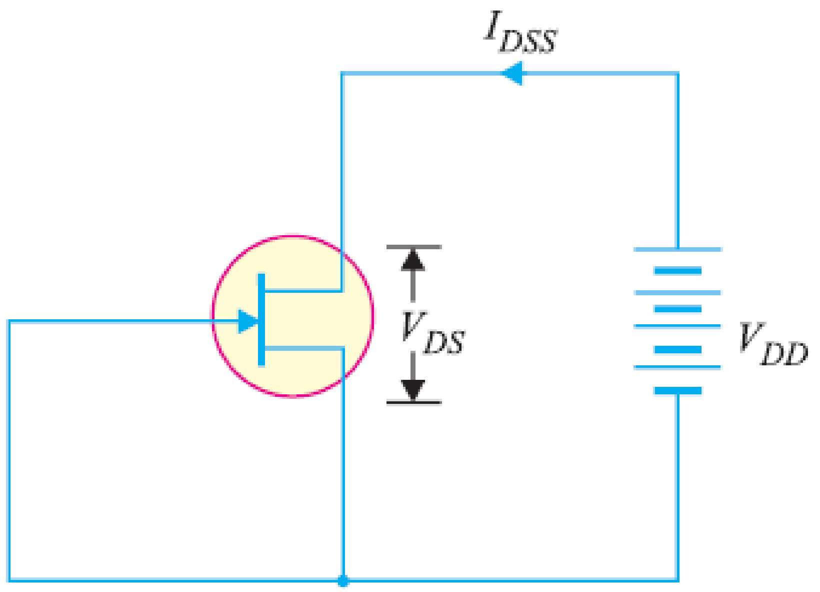
Important Terms

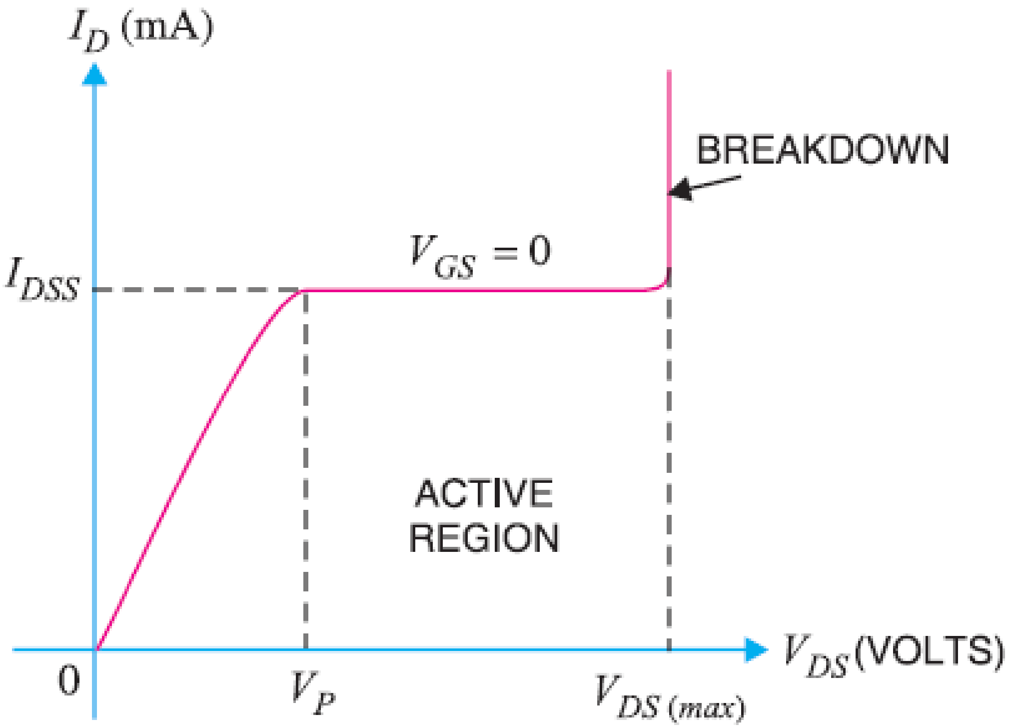
In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})
2. Pinch off voltage (V_P)
3. Gate-source cut off voltage [$V_{GS\,(off)}$]

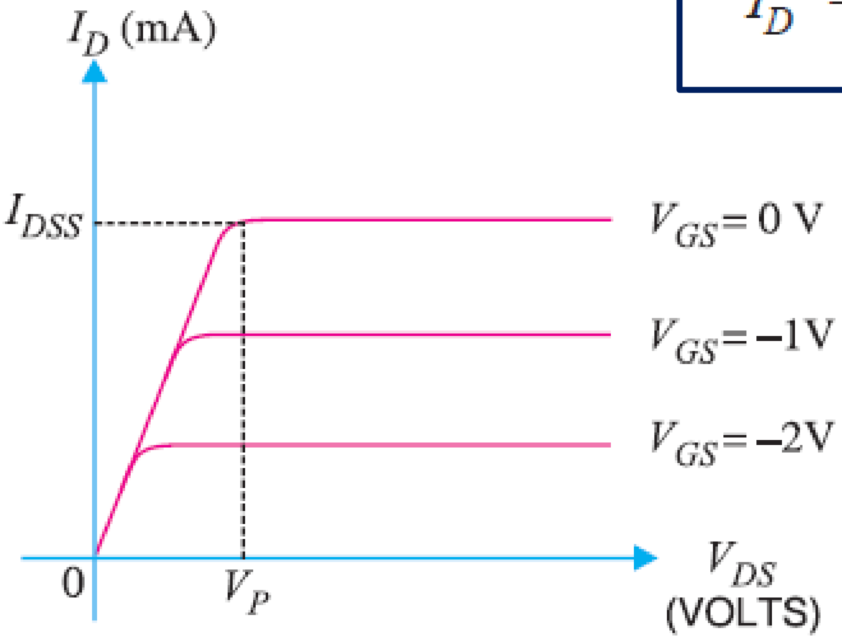


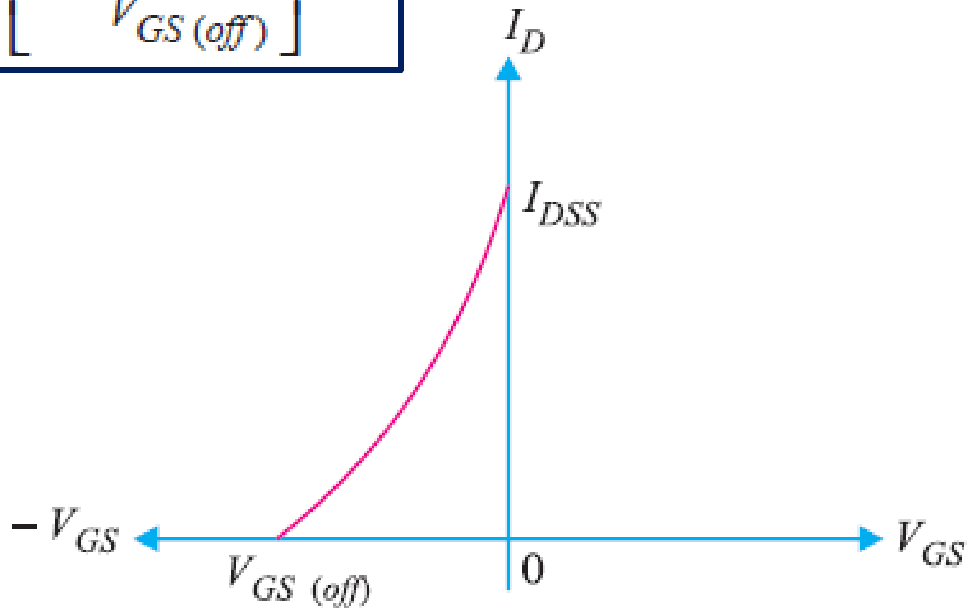
Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. V_{GS} = 0) and drain voltage (V_{DS}) equal to pinch off voltage*. It is sometimes called *zero-bias current*.





$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$





2. Pinch off Voltage (V_P). *It is the minimum drain-source voltage at which the drain current essentially becomes constant.*

3. Gate-source cut off voltage $V_{GS\,(off)}$. *It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.*

A JFET has a drain current of 5 mA. If I_{DSS} = 10 mA and $V_{GS\,(off)}$ = – 6 V, find the value of (i) V_{GS} and (ii) V_P.

Solution.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

or

$$5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2$$

or

$$1 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$

(i) ∴ $V_{GS} = \mathbf{-\,1.76\ V}$

(ii) and $V_P = -\,V_{GS\,(off)} = \mathbf{6\ V}$