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EC551: Lab Assignment #1

I) Half –Adder

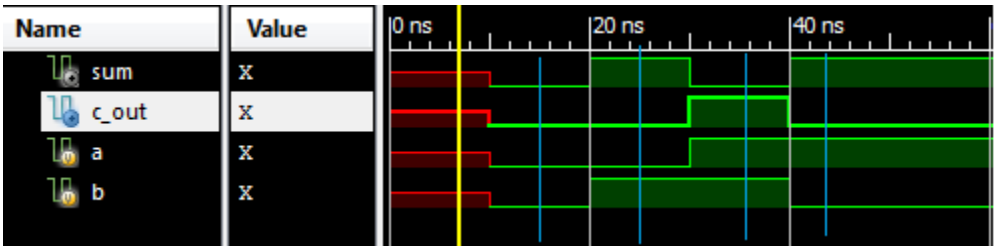
1) **Verilog Module File** – Add_half_0_dealy.v

```
module Add_half_0_delay(sum, c_out, a, b);
        input a, b;
        output c_out, sum;
        xor (sum, a, b);
        and (c_out, a, b);
endmodule
```

2) **Verilog Test Fixture File –** t_Add_half.v

```
module t_Add_half();

        // Inputs
        wire sum, c_out;
        reg a, b;

        Add_half_0_delay M1(sum, c_out, a, b); //UUT

        initial begin
        #10 a = 0; b = 0;
        #10 b = 1;
        #10 a = 1;
        #10 b = 0;
        end

endmodule
```

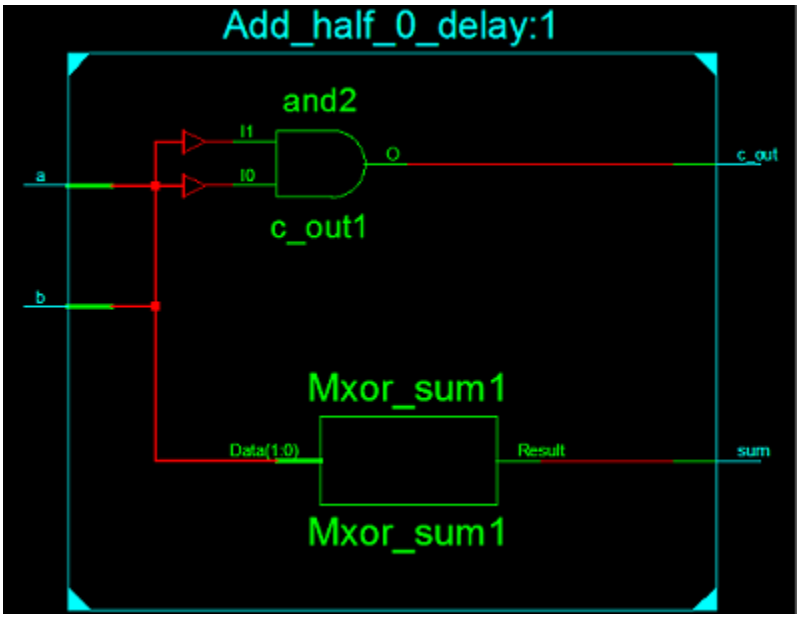
3) **ISIM Waveforms**



Instead of Circling I used blue lines for easier clarity. First blue line = 1 and so on.

1st Line : **A**=0, **B**=0, **A**+**B** = 0, **Sum** is zero, **C_out** is zero
2nd Line: **A**=0, **B**=1, **A+B =** 1, **Sum** is one, **C_out** is zero
3rd Line: **A**=1, **B**=1, **A+B =** 2, **Sum** is zero, **C_out** is one
4th Line: **A**=1, **B**=0, **A+B =** 1, **Sum** is one, **C_out** is zero

4) RTL Schematic



5) Place & Route Report- At End of Document

II) Full-Adder

1) Verilog Module File – Full_add.v

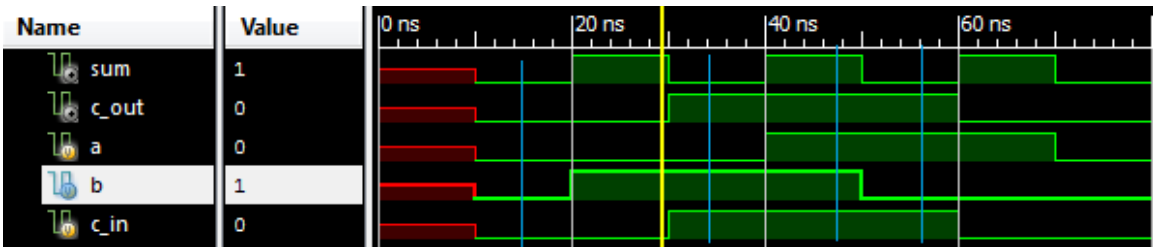
```
module Full_add( sum, c_out, a, b, c_in);
        output sum, c_out;
        input a, b, c_in;
        wire partial_c_out1, partial_c_out2, partial_sum;
        Add_half_0_delay M1(partial_sum, partial_c_out1, a, b);
        Add_half_0_delay M2(sum, partial_c_out2, c_in, partial_sum);
        or(c_out, partial_c_out1, partial_c_out2);
endmodule
```

2) Verilog Test Fixture File – t_add_full.v

```
module t_add_full();
    wire sum, c_out;
    reg a, b,c_in;
```

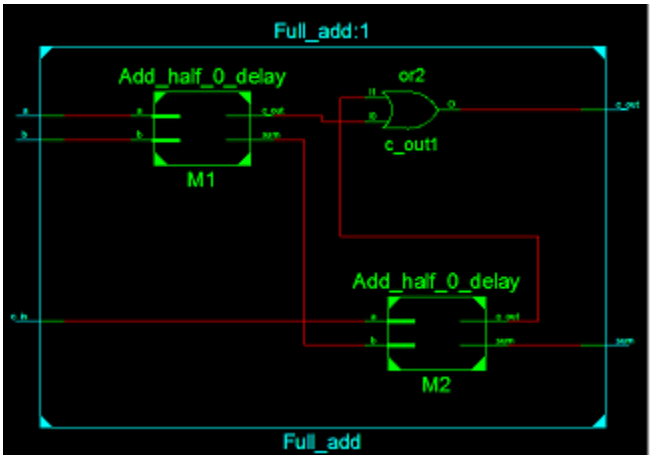
```
    Full_add F2(sum, c_out, a, b, c_in); //UUT

    initial begin
    #10 a = 0; b = 0; c_in =0;
    #10 b = 1;
    #10 c_in = 1;
    #10 a = 1;
    #10 b = 0;
    #10 c_in = 0;
    #10 a = 0;
    end
endmodule
```

3) ISIM Waveforms



1st Line: **A**=0, **B**=0 ,**C_in**=0, **A+B+C_in** = 0, **Sum** is zero, **C_out** is zero
2nd Line: **A**=0, **B**=1, **C_in**=1, **A+B+C_in** = 2, **Sum** is zero, **C_out** is one
3rd Line: **A**=1, **B**=1, **C_in**=1, **A+B+C_in** = 3, **Sum** is one, **C_out** is one
4th Line: **A**=1, **B**=0, **C_in**=1, **A+B+C_in** = 2, **Sum** is zero, **C_out** is one

4) RTL Schematic



5) Place & Route Report- At End of Document

6) User Constraints File

```
# PlanAhead Generated physical constraints
```

```
NET "a" LOC = C4;
NET "b" LOC = D9;
NET "c_in" LOC = B8;
NET "c_out" LOC = U16;
NET "sum" LOC = V16;

# PlanAhead Generated IO constraints

NET "a" IOSTANDARD = LVCMOS25;
NET "c_out" DRIVE = 12;
```

III) Multiplier From Figure 5A

1) **Verilog Module File –** multi_5A.v

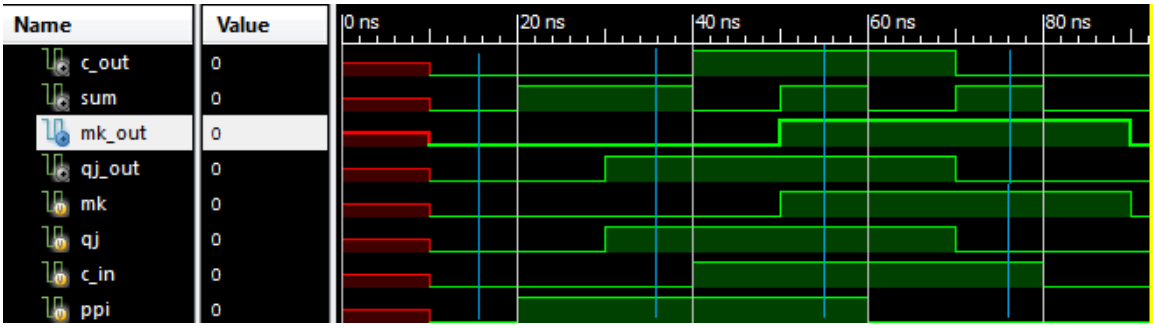
```
module multi_5A(c_out, sum, mk_out, qj_out, mk, qj, c_in, ppi);
        output mk_out, qj_out, sum, c_out;
        input qj, mk, c_in, ppi;
        wire or_out;

        and (or_out, qj, mk);
        and (mk_out, mk, mk);
        and (qj_out, qj, qj);

        Full_add F1(sum, c_out, or_out, ppi, c_in);

endmodule
```

2) **Verilog Test Fixture File –** test_multi_5A.v

```
module test_multi_5A();

        reg mk;
        reg qj;
        reg c_in;
        reg ppi;

        wire c_out;
        wire sum;
        wire mk_out;
        wire qj_out;

        multi_5A uut (
                .c_out(c_out),
                .sum(sum),
                .mk_out(mk_out),
                .qj_out(qj_out),
                .mk(mk),
                .qj(qj),
                .c_in(c_in),
                .ppi(ppi)
        );
```

```
initial begin
        #10 mk = 0; qj = 0; c_in =0; ppi = 0;
        #10 ppi = 1;
        #10 qj = 1;
        #10 c_in = 1;
        #10 mk = 1;
        #10 ppi = 0;
        #10 qj = 0;
        #10 c_in = 0;
        #10 mk = 0;
end

endmodule
```

3) ISIM Waveforms



mk_out and **qj_out** should always equal **mk** and **qj** respectively, **sum** and **c_out** are the outputs of a full adder with inputs of **ppi** and (**qj** and **mk**)

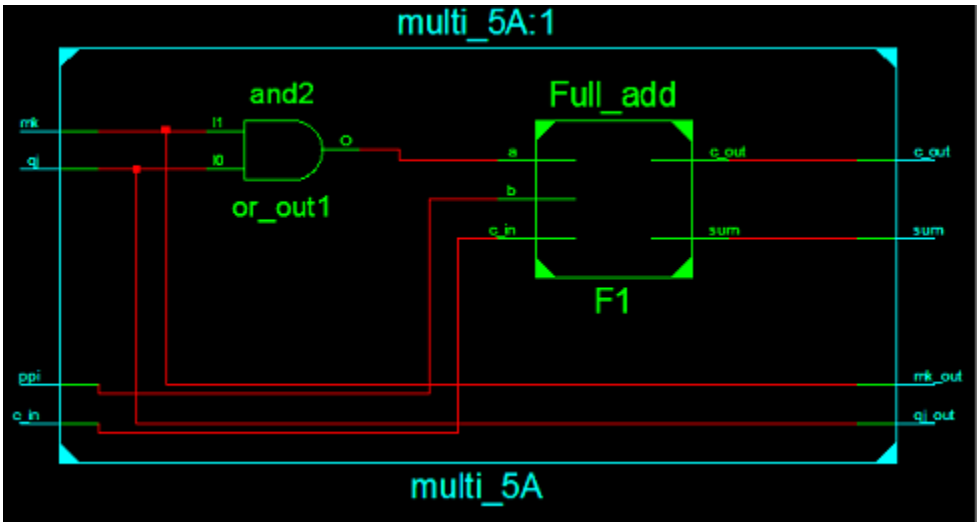
1st Line: **ppi**=0, **c_in**=0 , **qj**=0, **mk** = 0, **(qj and mk) + ppi = 0**, **Sum** is zero, **C_out** is zero, **mk_out** is zero, **qj_out** is zero

2nd Line: **ppi**=1, **c_in**=0 , **qj**=1, **mk** = 0, **(qj and mk) + ppi = 1**, **Sum** is one, **C_out** is zero, **mk_out** is zero, **qj_out** is one

3rd Line: **ppi**=1, **c_in**=1 , **qj**=1, **mk** = 1, **(qj and mk) + ppi = 2**, **Sum** is one, **C_out** is 1, **mk_out** is 1, **qj_out** is 1

4th Line: **ppi**=0, **c_in**=1 , **qj**=0, **mk** = 1, **(qj and mk) + ppi = 1**, **Sum** is one, **C_out** is zero, **mk_out** is 1, **qj_out** is 0

4) RTL Schematic



5) Place & Route Report- At End of Document

IV) Multiplier From Figure 5B

1) Verilog Module File - mulit_5b.v

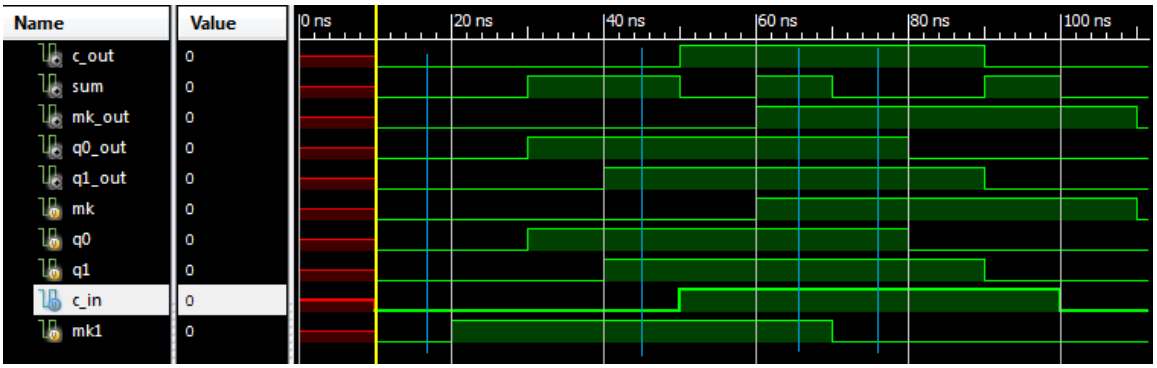
```
module multi_5b(c_out, sum, mk_out, q0_out, q1_out, mk, q0, q1, c_in, mk1);
        output mk_out, q0_out, q1_out, sum, c_out;
        input q0, q1, mk, mk1, c_in;
        wire or_out, or_out2;

        and (or_out, q1, mk);
        and (or_out2, q0, mk1);

        and (mk_out, mk, mk);
        and (q0_out, q0, q0);
        and (q1_out, q1, q1);

        Full_add F1(sum, c_out, or_out, or_out2, c_in);

endmodule
```

2) **Verliog Test Fixture File –** test_multi_5b.v

```
module test_multi_5b;

        // Inputs
        reg mk;
        reg q0;
        reg q1;
        reg c_in;
        reg mk1;

        // Outputs
        wire c_out;
```

```
        wire sum;
        wire mk_out;
        wire q0_out;
        wire q1_out;

        // Instantiate the Unit Under Test (UUT)
        multi_5b uut (
                .c_out(c_out),
                .sum(sum),
                .mk_out(mk_out),
                .q0_out(q0_out),
                .q1_out(q1_out),
                .mk(mk),
                .q0(q0),
                .q1(q1),
                .c_in(c_in),
                .mk1(mk1)
        );
        initial begin
                #10 mk = 0; q0 = 0; q1 = 0; c_in =0; mk1 = 0;
                #10 mk1 = 1;
                #10 q0 = 1;
                #10 q1 = 1;
                #10 c_in = 1;
                #10 mk = 1;
                #10 mk1 = 0;
                #10 q0 = 0;
                #10 q1 = 0;
                #10 c_in = 0;
                #10 mk = 0;
        end
endmodule
```

3) **ISIM Waveforms**



mk_out , **q1_out and q0_out** should always equal **mk** and **q1** and **q0** respectively, **sum** and **c_out** are the outputs of a full adder with inputs of **ppi** and (**qj** and **mk**)

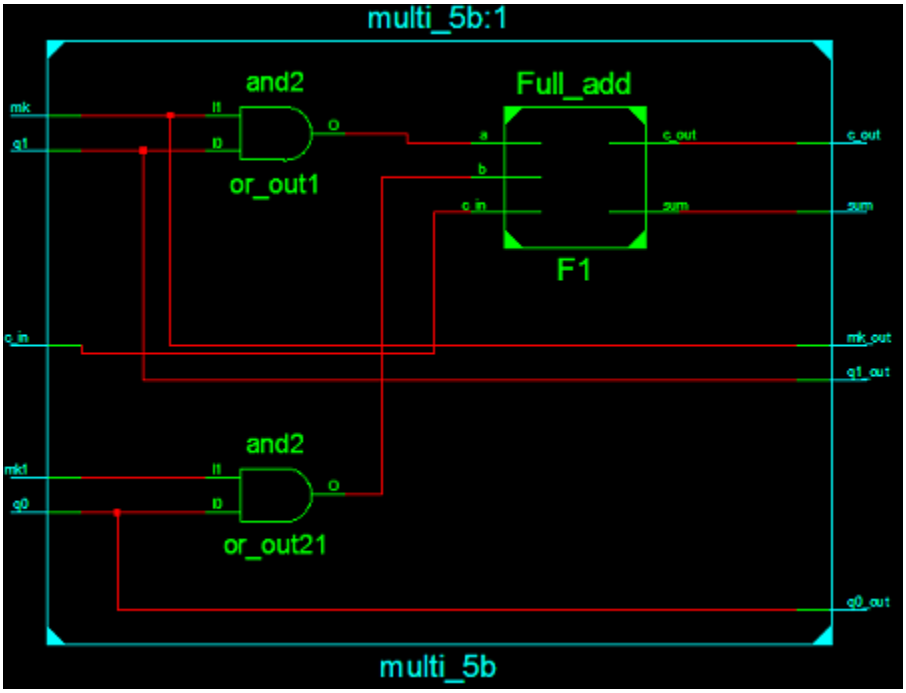
1st Line: **c_in**=0 , **q0**=0, **q1**=0, **mk** = 0, **mk1** = 0, **(q1 and mk) + (q0 and mk1) = 0**, **Sum** is zero, **C_out** is zero, **mk_out** is zero, **q0_out** is zero, ,**q1_out** is zero

2nd Line: **c_in**=0 , **q0**=1, **q1**=1, **mk** = 0, **mk1** = 1, **(q1 and mk) + (q0 and mk1) = 1**, **Sum** is one, **C_out** is zero, **mk_out** is zero, **q0_out** is one, ,**q1_out** is one

3rd Line: **c_in**=1 , **q0**=1, **q1**=1, **mk** = 0 , **mk1** = 0, **(q1 and mk) + (q0 and mk1) = 2**, **Sum** is zero, **C_out** is one, **mk_out** is one, **q0_out** is one, ,**q1_out** is one

4th Line: **c_in**=1 , **q0**=1, **q1**=1, **mk** = 0 , **mk1** = 1, **(q1 and mk) + (q0 and mk1) = 1**, **Sum** is one, **C_out** is one, **mk_out** is one, **q0_out** is one, ,**q1_out** is one

4) **RTL Schematic**



5) **Place & Route Report-** At End of Document

V) 4 x 4 Multiplier Structural

1) **Verilog Module File**- mulit_4by4_struct.v

```
module multi_4by4_struct(p,m,q);
        input [3:0] q;
        input [3:0] m;
        output [7:0] p;

wire c_out1, c_out2, c_out3, c_out4, c_out5, c_out6, c_out7, c_out8, c_out9, c_out10, c_out11;
wire p_out1, p_out2, p_out3, p_out4, p_out5, p_out6, p_out7, p_out8, p_out9;
wire diag_1, diag_2, diag_3, diag_4, diag_5, diag_6, diag_7, diag_8,diag_9, diag_10, diag_11, diag_12;
wire q_prop1, q_prop2, q_prop3, q_prop4, q_prop5, q_prop6, q_prop7, q_prop8;
wire q1_out1, q1_out2, q1_out3, q1_out4, q0out1, q0out2, q0out3, q0out4;
```

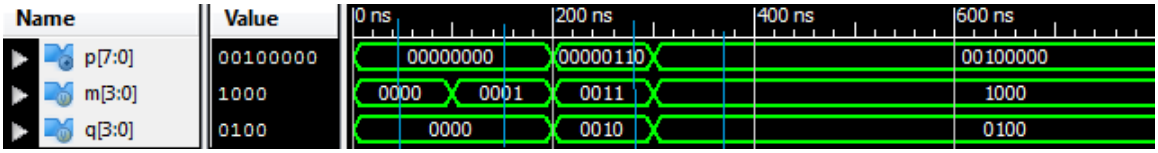
```
and (p[0], m[0], q[0]);

//first row
multi_5b B11(c_out1, p[1], diag_1, q0out1, q1_out1, m[0], q[0], q[1], 1'b0, m[1]);

multi_5b B12(c_out2, p_out1 , diag_2, q0out2, q1_out2, m[1], q0out1, q1_out1, c_out1, m[2]);

multi_5b B13(c_out3, p_out2 , diag_3, q0out3, q1_out3, m[2], q0out2, q1_out2, c_out2, m[3]);

multi_5b B14(c_out4, p_out3 , diag_4, q0out4, q1_out4, m[3], q0out3, q1_out3, c_out3, 1'b0);

//second row
multi_5A A21(c_out5, p[2], diag_5, q_prop1, diag_1, q[2], 1'b0, p_out1);

multi_5A A22(c_out6, p_out4, diag_6, q_prop2, diag_2, q_prop1, c_out5, p_out2);

multi_5A A23(c_out7, p_out5, diag_7, q_prop3, diag_3, q_prop2, c_out6, p_out3);

multi_5A A24(c_out8, p_out6, diag_8, q_prop4, diag_4, q_prop3, c_out7, c_out4);

//thrid row row
multi_5A A31(c_out9, p[3], diag_9, q_prop5, diag_5, q[3], 1'b0, p_out4);

multi_5A A32(c_out10, p[4], diag_10, q_prop6, diag_6, q_prop5, c_out9, p_out5);

multi_5A A33(c_out11, p[5], diag_11, q_prop7, diag_7, q_prop6, c_out10, p_out6);

multi_5A A34(p[7], p[6], diag_12, q_prop8, diag_5, q_prop7, c_out4, c_out8);

endmodule
```

2) **Verilog Test Fixture File –** test_multi_4by4_struct

```
module test_multi_4by4_struct;

        reg [3:0] m;
        reg [3:0] q;

        // Outputs
        wire [7:0] p;

        multi_4by4_struct uut (
                .p(p),
                .m(m),
                .q(q)
        );
                initial begin
                m = 4'b0000;
                q = 4'b0000;
                #100;
                m = 4'b0001;
                q = 4'b0000;
                #100;
                m = 4'b0011;
                q = 4'b0010;
                #100;
```

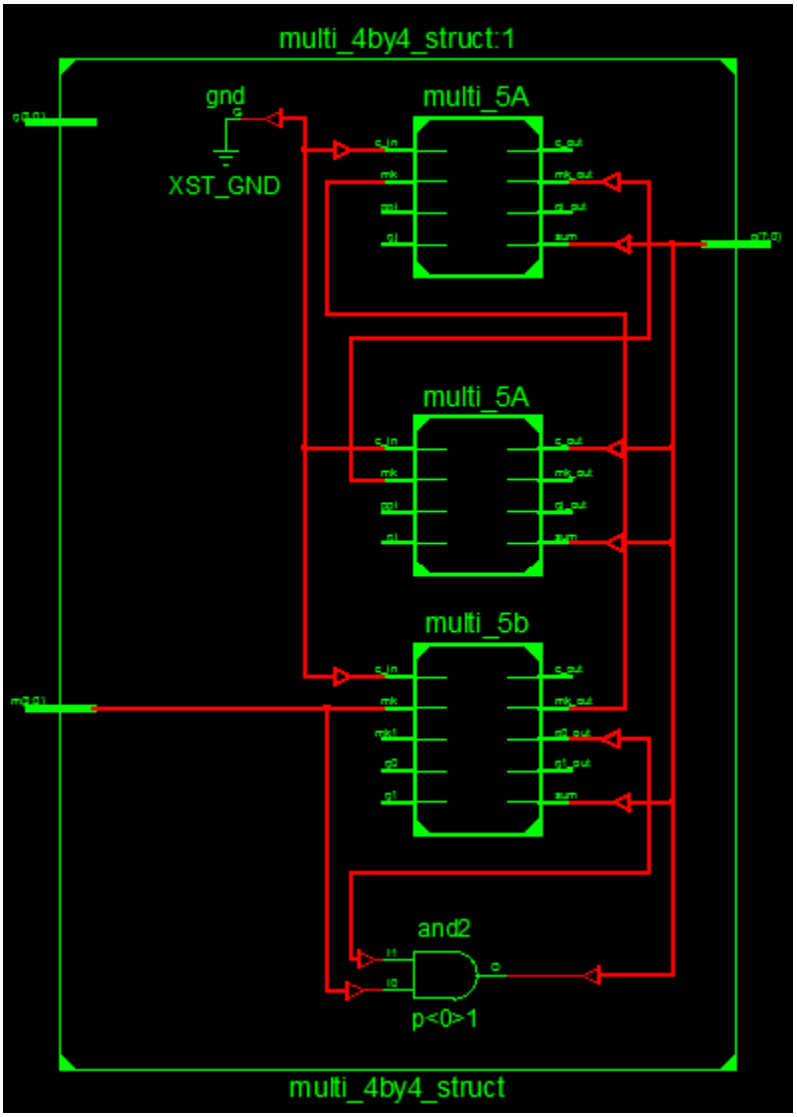
```
            m = 4'b1000;
            q = 4'b0100;
        end

endmodule
```

3) ISIM Waveforms



1st Line: 0 * 0 = 0
2ndLine: 0 * 1 = 0
3rdLine: 2 * 3 = 6
4thLine: 4 * 8 = 32

4) RTL Schematic



5) **Place & Route Report-** At End of Document

VI) 4 x 4 Multiplier Behavioral

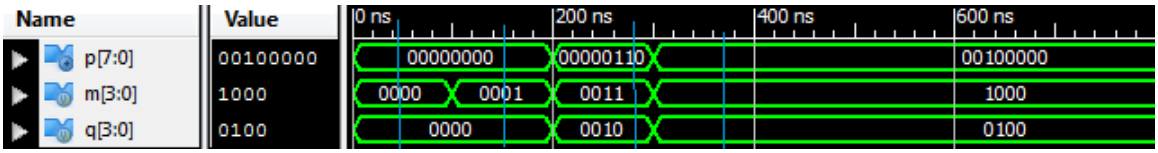
1) **Verlog Module File –** mulit_4by4_behav.v

```
module multi_4by4_behav(p,m,q);
	input [3:0] q;
	input [3:0] m;
	output [7:0] p;

	assign p = q * m;
endmodule
```

2) **Verliog Test Fixture File** – test_mulit_4by4_behav.v

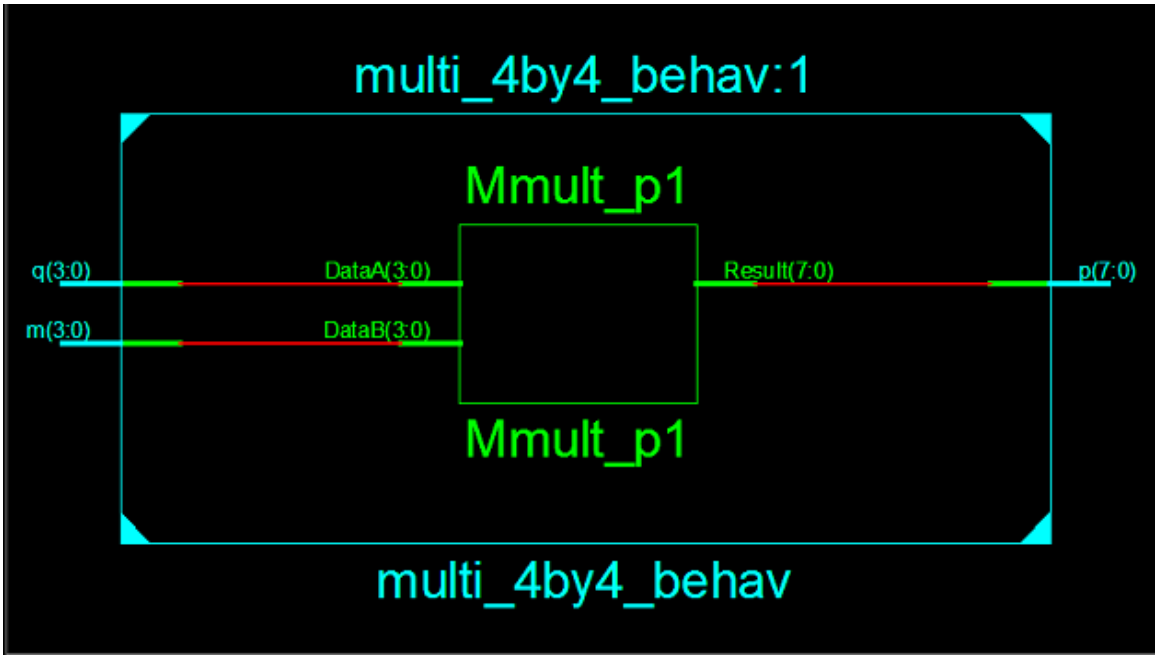
```
module test_multi_4by4_behav;

	// Inputs
	reg [3:0] m;
	reg [3:0] q;

	// Outputs
	wire [7:0] p;

	// Instantiate the Unit Under Test (UUT)
	multi_4by4_behav uut (
		.p(p),
		.m(m),
		.q(q)
	);

	initial begin
		m = 4'b0000;
		q = 4'b0000;

		#100;
		m = 4'b0001;
		q = 4'b0000;

		#100;
		m = 4'b0011;
		q = 4'b0010;

		#100;
		m = 4'b1000;
		q = 4'b0100;
	end

endmodule
```

3) **ISIM Waveforms**



1st Line: 0 * 0 = 0
2ndLine: 0 * 1 = 0
3rdLine: 2 * 3 = 6
4thLine: 4 * 8 = 32

4) RTL Schematic



5) Place & Route Report- At End of Document

VII) N x N Multiplier with N as parameter

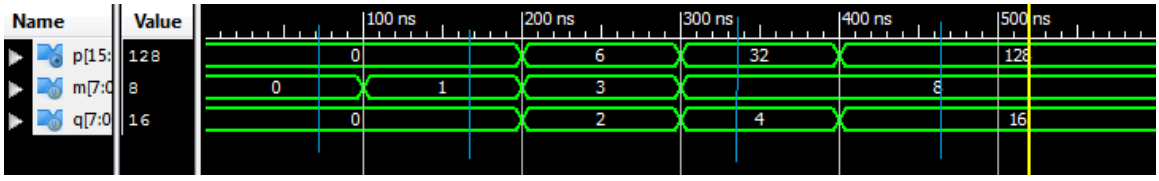
1) **Verilog Module File –** multi_NbyN_behav.v

```
module multi_NbyN_behav(p,m,q);
    parameter N = 4;
    input [(N-1):0] q;
    input [(N-1):0] m;
    output [(2*N-1):0] p;

    assign p = q * m;
endmodule
```

2) Verilog Test Fixture File – test_multi_NbyN_behav.v

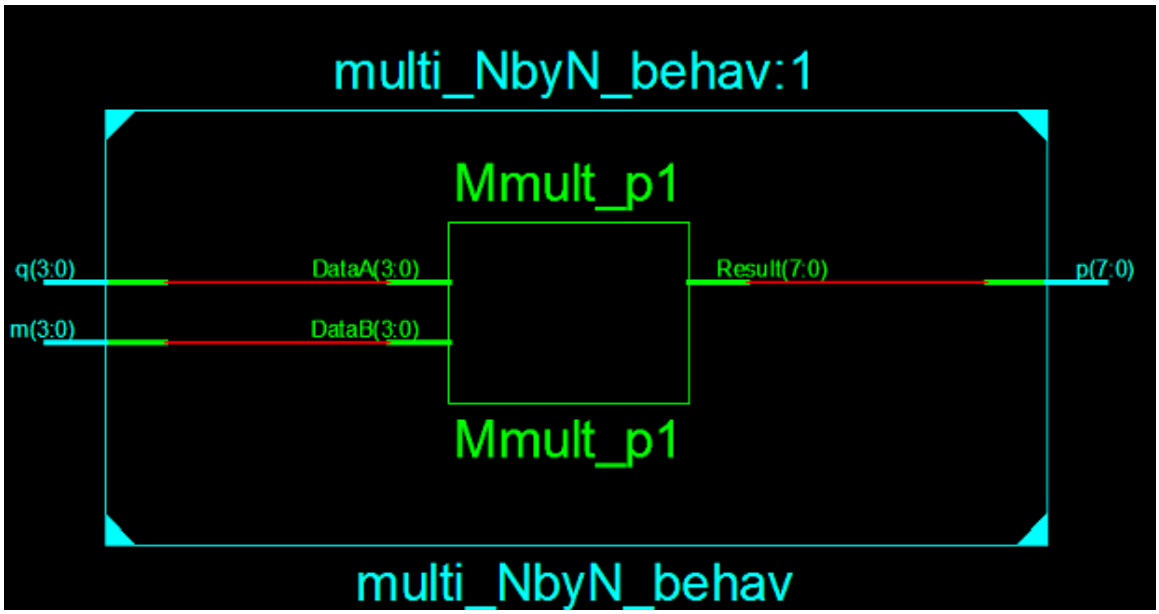
```
module test_multi_NbyN_behav;

	// Inputs
	reg [7:0] m;
	reg [7:0] q;

	// Outputs
	wire [15:0] p;

	// Instantiate the Unit Under Test (UUT)
	multi_NbyN_behav #(8) uut (
		.p(p),
		.m(m),
		.q(q)
	);

	initial begin
		m = 8'b00000000;
		q = 8'b00000000;

		#100;
		m = 8'b00000001;
		q = 8'b00000000;

		#100;
		m = 8'b00000011;
		q = 8'b00000010;

		#100;
		m = 8'b00001000;
		q = 8'b00000100;

		#100;
		m = 8'b00001000;
		q = 8'b00010000;
	end

endmodule
```

3) ISIM Waveforms



1st Line: 0 * 0 = 0
2ndLine: 0 * 1 = 0
3rdLine: 2 * 3 = 6
4thLine: 16 * 8 = 128

4) **RTL schematic**



5) Place & Route Report- At End of Document

Questions:

The behavioral implementation of the multiplier used 16 slices of logic while the structural implementation only used one.

The structural implementation of the multiplier has a maximum pin delay of 11.4 ns.

Overall the structural multiplier is better(less logic, faster) but requires more effort and detail in coding.

Timing Report:


```
C:\Xilinx\13.3\ISE_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v 3 -s 3
-n 3 -fastpaths -xml Full_add.twx Full_add.ncd -o Full_add.twr Full_add.pcf
-ucf Full_add.ucf

Design file:              Full_add.ncd
Physical constraint file: Full_add.pcf
Device,package,speed:     xc6slx16,csg324,C,-3 (PRODUCTION 1.20 2011-10-03)
Report level:             verbose report

Environment Variable      Effect
------------------------  ------
NONE                      No environment variables were set
--------------------------------------------------------------------------------

INFO:Timing:2698 - No timing constraints found, doing default enumeration.
INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths
```

option. All paths that are not constrained will be reported in the
unconstrained paths section(s) of the report.
INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on
a 50 Ohm transmission line loading model. For the details of this model,
and for more information on accounting for different loading conditions,
please see the device datasheet.

Data Sheet report:

All values displayed in nanoseconds (ns)

Pad to Pad

Source Pad	Destination Pad	Delay
a	c_out	11.410
a	sum	11.777
b	c_out	10.531
b	sum	10.898
c_in	c_out	10.431
c_in	sum	10.798

Analysis completed Fri Sep 28 13:54:26 2012

Trace Settings:

Trace Settings

Peak Memory Usage: 213 MB

Place & Route Report Half Adder

Release 13.3 par O.76xd (nt64)

ECE-PHO115-01:: Fri Sep 28 13:07:27 2012

par -w -intstyle ise -ol high -mt off Add_half_0_delay_map.ncd
Add_half_0_delay.ncd Add_half_0_delay.pcf

Constraints file: Add_half_0_delay.pcf.
Loading device for application Rf_Device from file '6slx16.nph' in environment
C:\Xilinx\13.3\ISE_DS\ISE\.
"Add_half_0_delay" is an NCD, version 3.2, device xc6slx16, package csg324, speed -
3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par
  -x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all
  internal clocks in this design. Because there are not defined timing requirements, a timing score will not be
  reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.
  Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.20 2011-10-03".

Device Utilization Summary:

Slice Logic Utilization:
  Number of Slice Registers: 0 out of 18,224 0%
  Number of Slice LUTs: 1 out of 9,112 1%
    Number used as logic: 1 out of 9,112 1%
      Number using O6 output only: 0
      Number using O5 output only: 0
      Number using O5 and O6: 1
      Number used as ROM: 0
    Number used as Memory: 0 out of 2,176 0%

Slice Logic Distribution:
  Number of occupied Slices: 1 out of 2,278 1%
  Nummber of MUXCYs used: 0 out of 4,556 0%
  Number of LUT Flip Flop pairs used: 1
    Number with an unused Flip Flop: 1 out of 1 100%
    Number with an unused LUT: 0 out of 1 0%
    Number of fully used LUT-FF pairs: 0 out of 1 0%
    Number of slice register sites lost
      to control set restrictions: 0 out of 18,224 0%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice. A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs: 4 out of 232 1%

Specific Feature Utilization:
  Number of RAMB16BWERs: 0 out of 32 0%
  Number of RAMB8BWERs: 0 out of 64 0%
  Number of BUFIO2/BUFIO2_2CLKs: 0 out of 32 0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs: 0 out of 32 0%
  Number of BUFG/BUFGMUXs: 0 out of 16 0%
  Number of DCM/DCM_CLKGENs: 0 out of 4 0%
  Number of ILOGIC2/ISERDES2s: 0 out of 248 0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs: 0 out of 248 0%

```
Number of OLOGIC2/OSERDES2s:              0 out of    248    0%
Number of BSCANs:                         0 out of      4    0%
Number of BUFHs:                          0 out of    128    0%
Number of BUFPLLs:                        0 out of      8    0%
Number of BUFPLL_MCBs:                    0 out of      4    0%
Number of DSP48A1s:                       0 out of     32    0%
Number of ICAPs:                          0 out of      1    0%
Number of MCBs:                           0 out of      2    0%
Number of PCILOGICSEs:                    0 out of      2    0%
Number of PLL_ADVs:                       0 out of      2    0%
Number of PMVs:                           0 out of      1    0%
Number of STARTUPs:                       0 out of      1    0%
Number of SUSPEND_SYNCs:                  0 out of      1    0%


Overall effort level (-ol):   High
Router effort level (-rl):    High

Starting initial Timing Analysis.  REAL time: 5 secs
Finished initial Timing Analysis.  REAL time: 5 secs

Starting Router


Phase  1  : 5 unrouted;      REAL time: 5 secs

Phase  2  : 5 unrouted;      REAL time: 5 secs

Phase  3  : 0 unrouted;      REAL time: 5 secs

Phase  4  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Updating file: Add_half_0_delay.ncd with current fully routed design.

Phase  5  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs

Phase  6  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs

Phase  7  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs

Phase  8  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs

Phase  9  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs

Phase 10  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs
Total REAL time to Router completion: 7 secs
Total CPU time to Router completion: 5 secs

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

Generating "PAR" statistics.
```

INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.
Timing Score: 0 (Setup: 0, Hold: 0)

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 18 secs
Total CPU time to PAR completion: 7 secs

Peak Memory Usage: 303 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file Add_half_0_delay.ncd

PAR done!

Place & Route Report Full Adder

ECE-PHO115-01:: Fri Sep 28 13:30:19 2012

par -w -intstyle ise -ol high -mt off Full_add_map.ncd Full_add.ncd
Full_add.pcf

Constraints file: Full_add.pcf.
Loading device for application Rf_Device from file '6slx16.nph' in environment
C:\Xilinx\13.3\ISE_DS\ISE\.
  "Full_add" is an NCD, version 3.2, device xc6slx16, package csg324, speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par
  -x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all
  internal clocks in this design. Because there are not defined timing requirements, a timing score will not be
  reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.
  Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.20 2011-10-03".

Device Utilization Summary:

Slice Logic Utilization:
  Number of Slice Registers: 0 out of 18,224 0%
  Number of Slice LUTs: 1 out of 9,112 1%
    Number used as logic: 1 out of 9,112 1%
      Number using O6 output only: 0
      Number using O5 output only: 0
      Number using O5 and O6: 1
      Number used as ROM: 0
    Number used as Memory: 0 out of 2,176 0%

Slice Logic Distribution:
  Number of occupied Slices: 1 out of 2,278 1%
  Nummber of MUXCYs used: 0 out of 4,556 0%
  Number of LUT Flip Flop pairs used: 1
    Number with an unused Flip Flop: 1 out of 1 100%
    Number with an unused LUT: 0 out of 1 0%
    Number of fully used LUT-FF pairs: 0 out of 1 0%
    Number of slice register sites lost
      to control set restrictions: 0 out of 18,224 0%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice. A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs: 5 out of 232 2%

Specific Feature Utilization:
  Number of RAMB16BWERs: 0 out of 32 0%
  Number of RAMB8BWERs: 0 out of 64 0%
  Number of BUFIO2/BUFIO2_2CLKs: 0 out of 32 0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs: 0 out of 32 0%
  Number of BUFG/BUFGMUXs: 0 out of 16 0%
  Number of DCM/DCM_CLKGENs: 0 out of 4 0%
  Number of ILOGIC2/ISERDES2s: 0 out of 248 0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs: 0 out of 248 0%
  Number of OLOGIC2/OSERDES2s: 0 out of 248 0%
  Number of BSCANs: 0 out of 4 0%
  Number of BUFHs: 0 out of 128 0%
  Number of BUFPLLs: 0 out of 8 0%
  Number of BUFPLL_MCBs: 0 out of 4 0%
  Number of DSP48A1s: 0 out of 32 0%
  Number of ICAPs: 0 out of 1 0%
  Number of MCBs: 0 out of 2 0%
  Number of PCILOGICSEs: 0 out of 2 0%
  Number of PLL_ADVs: 0 out of 2 0%
  Number of PMVs: 0 out of 1 0%

```
  Number of STARTUPs:                  0 out of     1    0%
  Number of SUSPEND_SYNCs:             0 out of     1    0%


Overall effort level (-ol):   High
Router effort level (-rl):    High

Starting initial Timing Analysis.  REAL time: 5 secs
Finished initial Timing Analysis.  REAL time: 5 secs

Starting Router


Phase  1  : 6 unrouted;      REAL time: 5 secs

Phase  2  : 6 unrouted;      REAL time: 5 secs

Phase  3  : 0 unrouted;      REAL time: 5 secs

Phase  4  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Updating file: Full_add.ncd with current fully routed design.

Phase  5  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  6  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  7  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  8  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  9  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase 10  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs
Total REAL time to Router completion: 6 secs
Total CPU time to Router completion: 5 secs

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

Generating "PAR" statistics.
INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.
Timing Score: 0 (Setup: 0, Hold: 0)


Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 16 secs
Total CPU time to PAR completion: 6 secs
```

Peak Memory Usage: 305 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file Full_add.ncd

PAR done!

Place & Route Report multiplier figure 5A

ECE-PHO115-01:: Fri Sep 28 14:18:26 2012

par -w -intstyle ise -ol high -mt off multi_5A_map.ncd multi_5A.ncd
multi_5A.pcf

Constraints file: multi_5A.pcf.
Loading device for application Rf_Device from file '6slx16.nph' in environment
C:\Xilinx\13.3\ISE_DS\ISE\.
   "multi_5A" is an NCD, version 3.2, device xc6slx16, package csg324, speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par
   -x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all
   internal clocks in this design. Because there are not defined timing requirements, a timing score will not be
   reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.
   Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.20 2011-10-03".

Device Utilization Summary:

Slice Logic Utilization:
  Number of Slice Registers: 0 out of 18,224   0%
  Number of Slice LUTs: 1 out of   9,112   1%
    Number used as logic: 1 out of   9,112   1%
      Number using O6 output only: 0
      Number using O5 output only: 0
      Number using O5 and O6:   1
      Number used as ROM: 0

```
   Number used as Memory:                  0 out of   2,176    0%

Slice Logic Distribution:
  Number of occupied Slices:               1 out of   2,278    1%
  Nummber of MUXCYs used:                  0 out of   4,556    0%
  Number of LUT Flip Flop pairs used:      1
    Number with an unused Flip Flop:       1 out of       1  100%
    Number with an unused LUT:             0 out of       1    0%
    Number of fully used LUT-FF pairs:     0 out of       1    0%
    Number of slice register sites lost
      to control set restrictions:         0 out of  18,224    0%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                   8 out of     232    3%

Specific Feature Utilization:
  Number of RAMB16BWERs:                   0 out of      32    0%
  Number of RAMB8BWERs:                    0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:           0 out of      32    0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs:       0 out of      32    0%
  Number of BUFG/BUFGMUXs:                 0 out of      16    0%
  Number of DCM/DCM_CLKGENs:               0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:             0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:   0 out of     248    0%
  Number of OLOGIC2/OSERDES2s:             0 out of     248    0%
  Number of BSCANs:                        0 out of       4    0%
  Number of BUFHs:                         0 out of     128    0%
  Number of BUFPLLs:                       0 out of       8    0%
  Number of BUFPLL_MCBs:                   0 out of       4    0%
  Number of DSP48A1s:                      0 out of      32    0%
  Number of ICAPs:                         0 out of       1    0%
  Number of MCBs:                          0 out of       2    0%
  Number of PCILOGICSEs:                   0 out of       2    0%
  Number of PLL_ADVs:                      0 out of       2    0%
  Number of PMVs:                          0 out of       1    0%
  Number of STARTUPs:                      0 out of       1    0%
  Number of SUSPEND_SYNCs:                 0 out of       1    0%


Overall effort level (-ol):   High
Router effort level (-rl):    High

Starting initial Timing Analysis.  REAL time: 5 secs
Finished initial Timing Analysis.  REAL time: 5 secs

Starting Router


Phase  1  : 9 unrouted;      REAL time: 5 secs
```

Phase 2 : 9 unrouted;   REAL time: 5 secs

Phase 3 : 10 unrouted;   REAL time: 5 secs

Phase 4 : 10 unrouted; (Par is working to improve performance)   REAL time: 6 secs

Updating file: multi_5A.ncd with current fully routed design.

Phase 5 : 0 unrouted; (Par is working to improve performance)   REAL time: 6 secs

Phase 6 : 0 unrouted; (Par is working to improve performance)   REAL time: 6 secs

Phase 7 : 0 unrouted; (Par is working to improve performance)   REAL time: 6 secs

Phase 8 : 0 unrouted; (Par is working to improve performance)   REAL time: 6 secs

Phase 9 : 0 unrouted; (Par is working to improve performance)   REAL time: 6 secs

Phase 10 : 0 unrouted; (Par is working to improve performance)   REAL time: 6 secs
Total REAL time to Router completion: 6 secs
Total CPU time to Router completion: 5 secs

Partition Implementation Status

  No Partitions were found in this design.

Generating "PAR" statistics.
INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.
Timing Score: 0 (Setup: 0, Hold: 0)

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 20 secs
Total CPU time to PAR completion: 7 secs

Peak Memory Usage: 305 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file multi_5A.ncd

PAR done!

Place & Route Report multiplier figure 5b

ECE-PHO115-01:: Fri Sep 28 14:40:11 2012

par -w -intstyle ise -ol high -mt off multi_5b_map.ncd multi_5b.ncd
multi_5b.pcf

Constraints file: multi_5b.pcf.
Loading device for application Rf_Device from file '6slx16.nph' in environment
C:\Xilinx\13.3\ISE_DS\ISE\.
  "multi_5b" is an NCD, version 3.2, device xc6slx16, package csg324, speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par
  -x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all
  internal clocks in this design. Because there are not defined timing requirements, a timing score will not be
  reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.
  Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.20 2011-10-03".

Device Utilization Summary:

Slice Logic Utilization:
  Number of Slice Registers: 0 out of 18,224   0%
  Number of Slice LUTs: 1 out of   9,112   1%
    Number used as logic: 1 out of   9,112   1%
      Number using O6 output only: 0
      Number using O5 output only: 0
      Number using O5 and O6:   1
      Number used as ROM: 0
    Number used as Memory: 0 out of   2,176   0%

Slice Logic Distribution:
  Number of occupied Slices: 1 out of   2,278   1%
  Nummber of MUXCYs used: 0 out of   4,556   0%
  Number of LUT Flip Flop pairs used: 1
    Number with an unused Flip Flop: 1 out of   1 100%
    Number with an unused LUT: 0 out of   1   0%
    Number of fully used LUT-FF pairs: 0 out of   1   0%
    Number of slice register sites lost
      to control set restrictions: 0 out of 18,224   0%

A LUT Flip Flop pair for this architecture represents one LUT paired with
one Flip Flop within a slice. A control set is a unique combination of
clock, reset, set, and enable signals for a registered element.
The Slice Logic Distribution report is not meaningful if the design is
over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
Number of bonded IOBs: 10 out of 232 4%

Specific Feature Utilization:
Number of RAMB16BWERs: 0 out of 32 0%
Number of RAMB8BWERs: 0 out of 64 0%
Number of BUFIO2/BUFIO2_2CLKs: 0 out of 32 0%
Number of BUFIO2FB/BUFIO2FB_2CLKs: 0 out of 32 0%
Number of BUFG/BUFGMUXs: 0 out of 16 0%
Number of DCM/DCM_CLKGENs: 0 out of 4 0%
Number of ILOGIC2/ISERDES2s: 0 out of 248 0%
Number of IODELAY2/IODRP2/IODRP2_MCBs: 0 out of 248 0%
Number of OLOGIC2/OSERDES2s: 0 out of 248 0%
Number of BSCANs: 0 out of 4 0%
Number of BUFHs: 0 out of 128 0%
Number of BUFPLLs: 0 out of 8 0%
Number of BUFPLL_MCBs: 0 out of 4 0%
Number of DSP48A1s: 0 out of 32 0%
Number of ICAPs: 0 out of 1 0%
Number of MCBs: 0 out of 2 0%
Number of PCILOGICSEs: 0 out of 2 0%
Number of PLL_ADVs: 0 out of 2 0%
Number of PMVs: 0 out of 1 0%
Number of STARTUPs: 0 out of 1 0%
Number of SUSPEND_SYNCs: 0 out of 1 0%

Overall effort level (-ol): High
Router effort level (-rl): High

Starting initial Timing Analysis. REAL time: 5 secs
Finished initial Timing Analysis. REAL time: 5 secs

Starting Router

Phase 1 : 11 unrouted; REAL time: 5 secs

Phase 2 : 11 unrouted; REAL time: 5 secs

Phase 3 : 2 unrouted; REAL time: 5 secs

Phase 4 : 2 unrouted; (Par is working to improve performance) REAL time: 6 secs

Updating file: multi_5b.ncd with current fully routed design.

Phase 5 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 6 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 7 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 8 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 9 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 10 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs
Total REAL time to Router completion: 6 secs
Total CPU time to Router completion: 5 secs

Partition Implementation Status

No Partitions were found in this design.

Generating "PAR" statistics.
INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.
Timing Score: 0 (Setup: 0, Hold: 0)

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 19 secs
Total CPU time to PAR completion: 7 secs

Peak Memory Usage: 305 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file multi_5b.ncd

PAR done!

Place & Route Report 4x4 Structural Multiplier

Release 13.3 par O.76xd (nt64)

ECE-PHO115-01:: Fri Sep 28 13:53:57 2012

par -w -intstyle ise -ol high -mt off Full_add_map.ncd Full_add.ncd
Full_add.pcf

Constraints file: Full_add.pcf.
Loading device for application Rf_Device from file '6slx16.nph' in environment C:\Xilinx\13.3\ISE_DS\ISE\.
"Full_add" is an NCD, version 3.2, device xc6slx16, package csg324, speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par
-x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all
internal clocks in this design. Because there are not defined timing requirements, a timing score will not be
reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.
Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.20 2011-10-03".

Device Utilization Summary:

Slice Logic Utilization:
Number of Slice Registers: 0 out of 18,224 0%
Number of Slice LUTs: 1 out of 9,112 1%
Number used as logic: 1 out of 9,112 1%
Number using O6 output only: 0
Number using O5 output only: 0
Number using O5 and O6: 1
Number used as ROM: 0
Number used as Memory: 0 out of 2,176 0%

Slice Logic Distribution:
Number of occupied Slices: 1 out of 2,278 1%
Nummber of MUXCYs used: 0 out of 4,556 0%
Number of LUT Flip Flop pairs used: 1
Number with an unused Flip Flop: 1 out of 1 100%
Number with an unused LUT: 0 out of 1 0%
Number of fully used LUT-FF pairs: 0 out of 1 0%
Number of slice register sites lost
to control set restrictions: 0 out of 18,224 0%

A LUT Flip Flop pair for this architecture represents one LUT paired with
one Flip Flop within a slice. A control set is a unique combination of
clock, reset, set, and enable signals for a registered element.
The Slice Logic Distribution report is not meaningful if the design is
over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
Number of bonded IOBs: 5 out of 232 2%
Number of LOCed IOBs: 5 out of 5 100%

Specific Feature Utilization:

```
Number of RAMB16BWERs:                  0 out of     32    0%
Number of RAMB8BWERs:                   0 out of     64    0%
Number of BUFIO2/BUFIO2_2CLKs:          0 out of     32    0%
Number of BUFIO2FB/BUFIO2FB_2CLKs:      0 out of     32    0%
Number of BUFG/BUFGMUXs:                0 out of     16    0%
Number of DCM/DCM_CLKGENs:              0 out of      4    0%
Number of ILOGIC2/ISERDES2s:            0 out of    248    0%
Number of IODELAY2/IODRP2/IODRP2_MCBs:  0 out of    248    0%
Number of OLOGIC2/OSERDES2s:            0 out of    248    0%
Number of BSCANs:                       0 out of      4    0%
Number of BUFHs:                        0 out of    128    0%
Number of BUFPLLs:                      0 out of      8    0%
Number of BUFPLL_MCBs:                  0 out of      4    0%
Number of DSP48A1s:                     0 out of     32    0%
Number of ICAPs:                        0 out of      1    0%
Number of MCBs:                         0 out of      2    0%
Number of PCILOGICSEs:                  0 out of      2    0%
Number of PLL_ADVs:                     0 out of      2    0%
Number of PMVs:                         0 out of      1    0%
Number of STARTUPs:                     0 out of      1    0%
Number of SUSPEND_SYNCs:                0 out of      1    0%

Overall effort level (-ol):   High
Router effort level (-rl):    High

Starting initial Timing Analysis.  REAL time: 5 secs
Finished initial Timing Analysis.  REAL time: 5 secs

Starting Router


Phase  1  : 6 unrouted;      REAL time: 5 secs

Phase  2  : 6 unrouted;      REAL time: 5 secs

Phase  3  : 4 unrouted;      REAL time: 5 secs

Phase  4  : 4 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Updating file: Full_add.ncd with current fully routed design.

Phase  5  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  6  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  7  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  8  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  9  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase 10  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs
Total REAL time to Router completion: 6 secs
Total CPU time to Router completion: 5 secs
```

Partition Implementation Status

No Partitions were found in this design.

Generating "PAR" statistics.
INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.
Timing Score: 0 (Setup: 0, Hold: 0)

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 18 secs
Total CPU time to PAR completion: 7 secs

Peak Memory Usage: 305 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file Full_add.ncd

PAR done!

Place & Route Report 4x4 Behavioral Multiplier

Release 13.3 par O.76xd (nt64)

ECE-PHO115-08:: Tue Oct 02 14:41:57 2012

par -w -intstyle ise -ol high -mt off multi_4by4_behav_map.ncd
multi_4by4_behav.ncd multi_4by4_behav.pcf

Constraints file: multi_4by4_behav.pcf.
Loading device for application Rf_Device from file '6slx16.nph' in environment
C:\Xilinx\13.3\ISE_DS\ISE\.
   "multi_4by4_behav" is an NCD, version 3.2, device xc6slx16, package csg324, speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing
constraints ("par

-x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all
internal clocks in this design. Because there are not defined timing requirements, a timing score will not be
reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.
Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.20 2011-10-03".

Device Utilization Summary:

Slice Logic Utilization:

Number of Slice Registers:	0 out of 18,224 0%
Number of Slice LUTs:	16 out of 9,112 1%
Number used as logic:	16 out of 9,112 1%
Number using O6 output only:	15
Number using O5 output only:	0
Number using O5 and O6:	1
Number used as ROM:	0
Number used as Memory:	0 out of 2,176 0%

Slice Logic Distribution:

Number of occupied Slices:	7 out of 2,278 1%
Nummber of MUXCYs used:	8 out of 4,556 1%
Number of LUT Flip Flop pairs used:	16
Number with an unused Flip Flop:	16 out of 16 100%
Number with an unused LUT:	0 out of 16 0%
Number of fully used LUT-FF pairs:	0 out of 16 0%
Number of slice register sites lost to control set restrictions:	0 out of 18,224 0%

A LUT Flip Flop pair for this architecture represents one LUT paired with one Flip Flop within a slice. A control set is a unique combination of clock, reset, set, and enable signals for a registered element.
The Slice Logic Distribution report is not meaningful if the design is over-mapped for a non-slice resource or if Placement fails.

IO Utilization:

Number of bonded IOBs:	16 out of 232 6%

Specific Feature Utilization:

Number of RAMB16BWERs:	0 out of 32 0%
Number of RAMB8BWERs:	0 out of 64 0%
Number of BUFIO2/BUFIO2_2CLKs:	0 out of 32 0%
Number of BUFIO2FB/BUFIO2FB_2CLKs:	0 out of 32 0%
Number of BUFG/BUFGMUXs:	0 out of 16 0%
Number of DCM/DCM_CLKGENs:	0 out of 4 0%
Number of ILOGIC2/ISERDES2s:	0 out of 248 0%
Number of IODELAY2/IODRP2/IODRP2_MCBs:	0 out of 248 0%
Number of OLOGIC2/OSERDES2s:	0 out of 248 0%
Number of BSCANs:	0 out of 4 0%
Number of BUFHs:	0 out of 128 0%

```
Number of BUFPLLs:                    0 out of      8    0%
Number of BUFPLL_MCBs:                0 out of      4    0%
Number of DSP48A1s:                   0 out of     32    0%
Number of ICAPs:                      0 out of      1    0%
Number of MCBs:                       0 out of      2    0%
Number of PCILOGICSEs:                0 out of      2    0%
Number of PLL_ADVs:                   0 out of      2    0%
Number of PMVs:                       0 out of      1    0%
Number of STARTUPs:                   0 out of      1    0%
Number of SUSPEND_SYNCs:              0 out of      1    0%
```

Overall effort level (-ol): High
Router effort level (-rl): High

Starting initial Timing Analysis. REAL time: 5 secs
Finished initial Timing Analysis. REAL time: 5 secs

Starting Router

Phase 1 : 97 unrouted; REAL time: 5 secs

Phase 2 : 97 unrouted; REAL time: 5 secs

Phase 3 : 59 unrouted; REAL time: 5 secs

Phase 4 : 59 unrouted; (Par is working to improve performance) REAL time: 6 secs

Updating file: multi_4by4_behav.ncd with current fully routed design.

Phase 5 : 0 unrouted; (Par is working to improve performance) REAL time: 7 secs

Phase 6 : 0 unrouted; (Par is working to improve performance) REAL time: 7 secs

Phase 7 : 0 unrouted; (Par is working to improve performance) REAL time: 7 secs

Phase 8 : 0 unrouted; (Par is working to improve performance) REAL time: 7 secs

Phase 9 : 0 unrouted; (Par is working to improve performance) REAL time: 7 secs

Phase 10 : 0 unrouted; (Par is working to improve performance) REAL time: 7 secs
Total REAL time to Router completion: 7 secs
Total CPU time to Router completion: 5 secs

Partition Implementation Status

No Partitions were found in this design.

Generating "PAR" statistics.
INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.
Timing Score: 0 (Setup: 0, Hold: 0)

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 20 secs
Total CPU time to PAR completion: 6 secs

Peak Memory Usage: 308 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file multi_4by4_behav.ncd

PAR done!

Place & Route Report NxN Muliplier

Release 13.3 par O.76xd (nt64)

ECE-PHO115-08:: Tue Oct 02 14:58:21 2012

par -w -intstyle ise -ol high -mt off multi_NbyN_behav_map.ncd
multi_NbyN_behav.ncd multi_NbyN_behav.pcf

Constraints file: multi_NbyN_behav.pcf.
Loading device for application Rf_Device from file '6slx16.nph' in environment
C:\Xilinx\13.3\ISE_DS\ISE\.
  "multi_NbyN_behav" is an NCD, version 3.2, device xc6slx16, package csg324, speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par
  -x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all
  internal clocks in this design. Because there are not defined timing requirements, a timing score will not be
  reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.
  Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.20 2011-10-03".

Device Utilization Summary:

Slice Logic Utilization:
- Number of Slice Registers: 0 out of 18,224 0%
- Number of Slice LUTs: 16 out of 9,112 1%
  - Number used as logic: 16 out of 9,112 1%
    - Number using O6 output only: 15
    - Number using O5 output only: 0
    - Number using O5 and O6: 1
    - Number used as ROM: 0
  - Number used as Memory: 0 out of 2,176 0%

Slice Logic Distribution:
- Number of occupied Slices: 7 out of 2,278 1%
- Nummber of MUXCYs used: 8 out of 4,556 1%
- Number of LUT Flip Flop pairs used: 16
  - Number with an unused Flip Flop: 16 out of 16 100%
  - Number with an unused LUT: 0 out of 16 0%
  - Number of fully used LUT-FF pairs: 0 out of 16 0%
  - Number of slice register sites lost to control set restrictions: 0 out of 18,224 0%

A LUT Flip Flop pair for this architecture represents one LUT paired with one Flip Flop within a slice. A control set is a unique combination of clock, reset, set, and enable signals for a registered element.
The Slice Logic Distribution report is not meaningful if the design is over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
- Number of bonded IOBs: 16 out of 232 6%

Specific Feature Utilization:
- Number of RAMB16BWERs: 0 out of 32 0%
- Number of RAMB8BWERs: 0 out of 64 0%
- Number of BUFIO2/BUFIO2_2CLKs: 0 out of 32 0%
- Number of BUFIO2FB/BUFIO2FB_2CLKs: 0 out of 32 0%
- Number of BUFG/BUFGMUXs: 0 out of 16 0%
- Number of DCM/DCM_CLKGENs: 0 out of 4 0%
- Number of ILOGIC2/ISERDES2s: 0 out of 248 0%
- Number of IODELAY2/IODRP2/IODRP2_MCBs: 0 out of 248 0%
- Number of OLOGIC2/OSERDES2s: 0 out of 248 0%
- Number of BSCANs: 0 out of 4 0%
- Number of BUFHs: 0 out of 128 0%
- Number of BUFPLLs: 0 out of 8 0%
- Number of BUFPLL_MCBs: 0 out of 4 0%
- Number of DSP48A1s: 0 out of 32 0%
- Number of ICAPs: 0 out of 1 0%
- Number of MCBs: 0 out of 2 0%
- Number of PCILOGICSEs: 0 out of 2 0%
- Number of PLL_ADVs: 0 out of 2 0%
- Number of PMVs: 0 out of 1 0%
- Number of STARTUPs: 0 out of 1 0%
- Number of SUSPEND_SYNCs: 0 out of 1 0%

Overall effort level (-ol): High
Router effort level (-rl): High

Starting initial Timing Analysis. REAL time: 5 secs
Finished initial Timing Analysis. REAL time: 5 secs

Starting Router

Phase 1 : 97 unrouted; REAL time: 5 secs

Phase 2 : 97 unrouted; REAL time: 5 secs

Phase 3 : 59 unrouted; REAL time: 5 secs

Phase 4 : 59 unrouted; (Par is working to improve performance) REAL time: 6 secs

Updating file: multi_NbyN_behav.ncd with current fully routed design.

Phase 5 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 6 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 7 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 8 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 9 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs

Phase 10 : 0 unrouted; (Par is working to improve performance) REAL time: 6 secs
Total REAL time to Router completion: 6 secs
Total CPU time to Router completion: 5 secs

Partition Implementation Status

  No Partitions were found in this design.

Generating "PAR" statistics.
INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.
Timing Score: 0 (Setup: 0, Hold: 0)

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 20 secs
Total CPU time to PAR completion: 7 secs

Peak Memory Usage: 307 MB

Placer: Placement generated during map.

Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file multi_NbyN_behav.ncd

PAR done!