University of Sri Jayewardenepura

B.Sc. (General) Degree First Year
First Semester Terminal Course Unit Examination – May, 2017

CSC 106 1.5 Computer System Organization
(Time: 1 ½ hours)

This paper consists of three (3) questions on two (2) pages.
Answer all questions.

Question 01 [*A total of 35 Marks*]

(a) A university offering 4-year degree programs consists of four faculties; namely Arts, Management, Medical and Science. The size of intake in each year is 700 for the faculty of Arts, 950 for Management, 200 for Medical, and 500 for Science. Number of female students in each year of study in the faculty of Arts is between 475 and 500. In the faculty of Management, it is between 450 and 500.

(i) Design a binary encoding system, with a minimum number of bits, to represent all the students in the university. Your system could easily be decoded to extract information such as faculty, year of study and gender.

(ii) Using your design in (i), how do you represent a second-year male student in the faculty of Science?

[10 Marks]

(b) Perform the following arithmetic operations with signed-2's complement forms in 8-bit registers.

(i) Addition of $(-128)_{10}$ and $(+127)_{10}$.

(ii) Subtraction of $(-42)_{10}$ from $(+24)_{10}$.

[10 Marks]

(c) What are the components of an IEEE standard 754 single precision floating-point number?

Suppose you are required to design a scheme to represent positive and negative 32-bit floating-point binary numbers. Magnitudes (in decimal) of the smallest and the largest number to be represented are 7.231×10^{-273} and 6.984×10^{325} respectively. The numbers are to be represented with the highest possible accuracy. Further, there is no provision to allocate a separate sign bit for the exponent, and hence, a suitable bias has to be used.

(i) Allocate the 32 bits for various components in order to satisfy the given requirement.

(ii) Show the bit configuration of the register when $(129.375)_{10}$ is represented using your design.

(iii) What is the smallest positive number that can be represented in your scheme? Show the bit configuration.

[15 Marks]

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Question 02 [*A total of 25 Marks*]

(a) Briefly describe the progression of computer technology components from vacuum tubes to VLSI (very large scale integration).

[05 Marks]

(b) State the similarities as well as the differences between ROM and PROM with respect to computer memories.

[05 Marks]

(c) Explain two different ways of translating instructions in high-level languages to machine instructions.

[05 Marks]

(d) Some specifications of two processors are provided in Table 2.1. State, with justification, which processor is faster in terms of

(i) the maximum amount of memory the processor can handle.

(ii) the amount of data that can be transferred from memory to processor per second.

	Processor *A*	**Processor *B***
Clock frequency	2.2GHz	2.5GHz
Number of cores	4	2
Width of data I/O bus	32 bits	64 bits
Speed of data I/O bus	1600MHz	1333MHz
Width of address bus	40 bits	38 bits

Table 2.1

[10 Marks]

Question 03 [*A total of 40 Marks*]

(a) Using the rules of Boolean algebra, show that

$$(a \oplus b)c + (b \oplus c)a = (b \oplus c)a + (c \oplus a)b = (c \oplus a)b + (a \oplus b)c$$

[10 Marks]

(b) What is a 1-bit full adder? Draw the block diagram of it. Explain how you would wire three 1-bit full adder circuits to calculate the sum of two 3-bit binary numbers ($a_1a_2a_3$) and ($a_4a_5a_6$), where a_i (i = 1..6) is either 0 or 1. Clearly show how the output is obtained.

[10 Marks]

(c) You are required to design a circuit to detect whether a given BCD number is either less than 6 or divisible by 3. In other words, the input to the circuit is the bit combination of the BCD number and the output from the circuit will be 1 if BCD number is less than 6 or divisible by 3, and output will be 0 otherwise.

(i) Using Karnaugh maps. obtain a simplified algebraic expression for the output in terms of inputs.
[Hint: use don't care conditions.]

(ii) Draw the logic diagram of your circuit using 2-input NAND gates alone. You may use up to a maximum of 6 such NAND gates.

[20 Marks]

*** End of Paper ***

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