Laboratory Exercise 8 - Week 2
Dedicated Microprocessor Part III

The purpose of this exercise is to build and use Datapath and finite state machine. The designed circuits are to be implemented on an Altera DE0-CV, DE1-SoC, or DE2-115 Board.

Part III

The dedicated microprocessor consisting of a Control unit and a Datapath shown in Figure 5.

Figure 5: Dedicated microprocessor for counting 1 to 10.

You are to implement a dedicated microprocessor by assembling the Control unit and Datapath.

1. Write a VHDL file that defines component circuit (created in Part I and Part II), depicted in Figure 5. Modify the control unit to be able to operate with system internal clock (use a counter to transform 50 MHz to 1 Hz trigger or clock signal with period of 1 second). Compile the circuit. How many logic elements (LEs) are used to implement your circuit?
2. Simulate your circuit to verify its correctness.
3. Augment your VHDL file to use a pushbutton KEY0 as Reset, and a 7-segment display HEX0 to display the 1 to 10 ('A') count as your circuit operates. Make the necessary pin assignments needed to implement the circuit on your DE-series board and compile the circuit.
4. Download your circuit into the FPGA chip and test its functionality by operating the implemented switches.

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