

# reInstruct: Toward OS-aware CPU microcode reprogramming

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# What is Microcode?

High-level Code  
(C, Python, etc.)

Compiler or Interpreter

x86 CISC Instructions

Microcode and Microsequencer  
(vendor-defined, hidden)

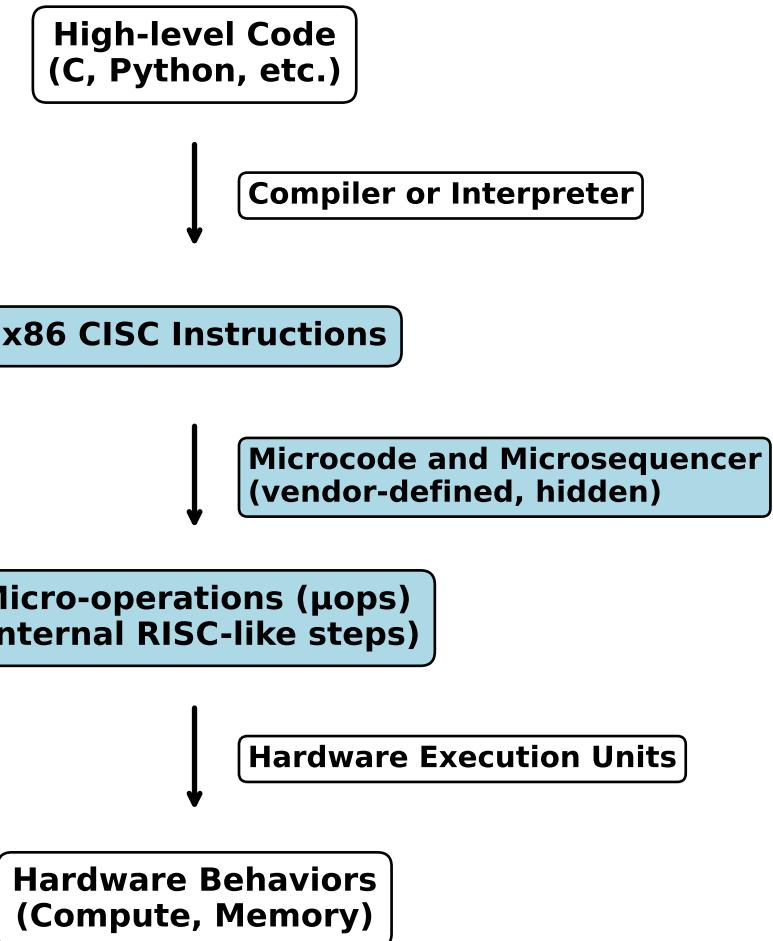
Micro-operations ( $\mu$ ops)  
(internal RISC-like steps)

Hardware Execution Units

Hardware Behaviors  
(Compute, Memory)

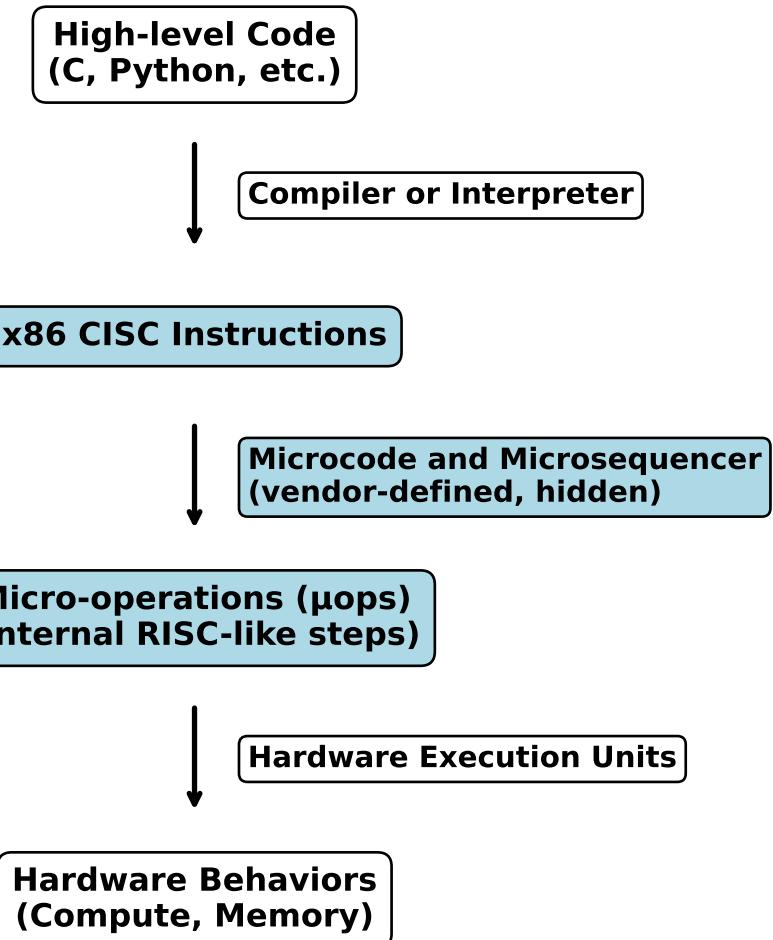
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- **Role:** Works like firmware for the processor. **Defines** how each **instruction behaves**.



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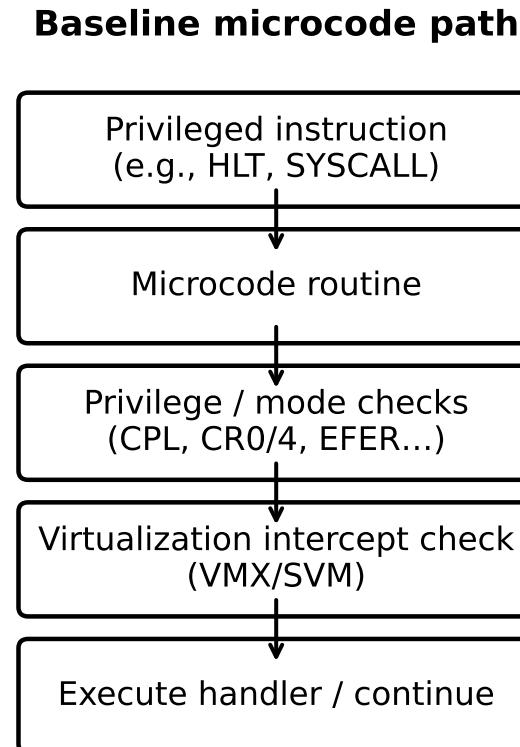
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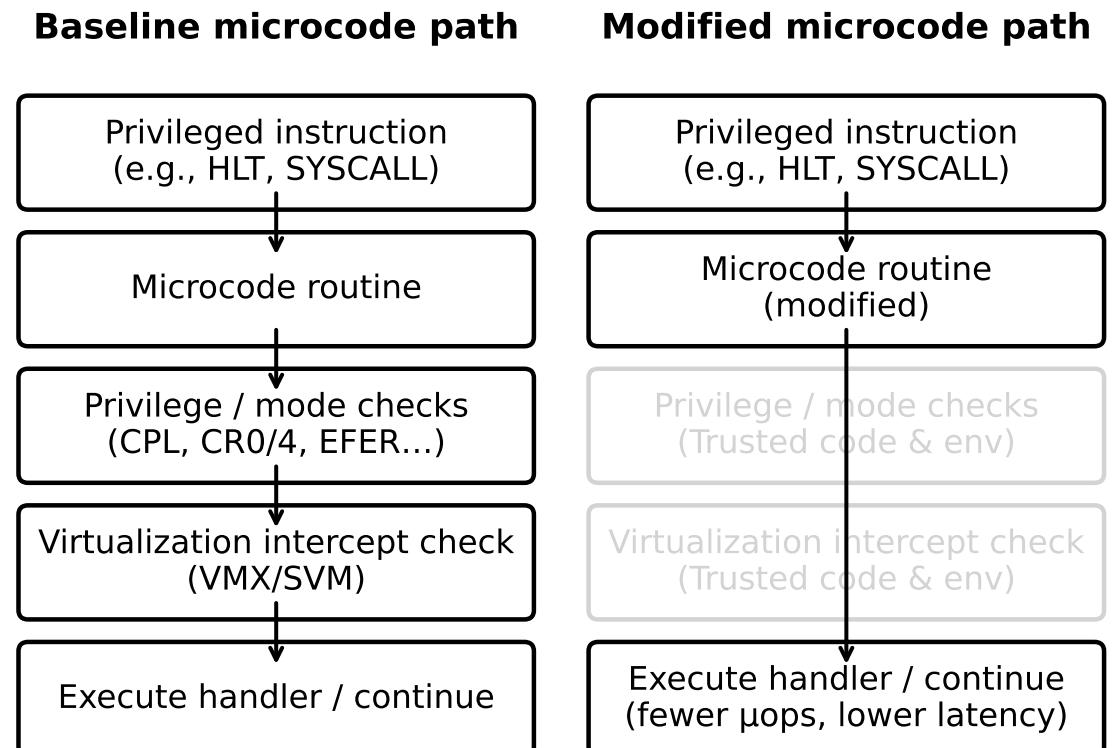
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# The Status Quo: **Locked** by Vendors

- Microcode is **proprietary**: no documentation, updates cryptographically signed, only distributed via vendor BIOS/OS channels.
- System software and researchers **cannot observe or modify** instruction behavior.
- So, the problem is, if we want to observe or modify the microcode layer, it is very difficult.

# **Emerging Possibility**

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**uCode Research Team**  
chip-red-pill

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Research Team Members: Dmitry Sklyarov (@\_Dmit), Mark Ermolov (@\_markel\_\_), Maxim Goryachy (@h0t)

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Moscow

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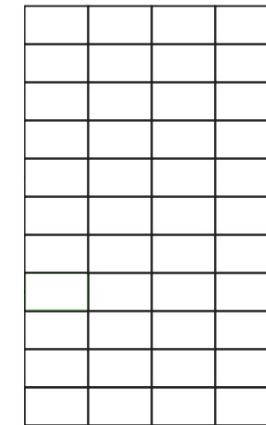
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- INTEL-SA-00086: grants privilege escalation.
- CHIP-RED-PILL enabled a hidden “Red Unlock” mode to access CPU microcode internals.
- CHIP-RED-PILL revealed the vendor μop format and encodings, which made authoring custom microcode feasible.



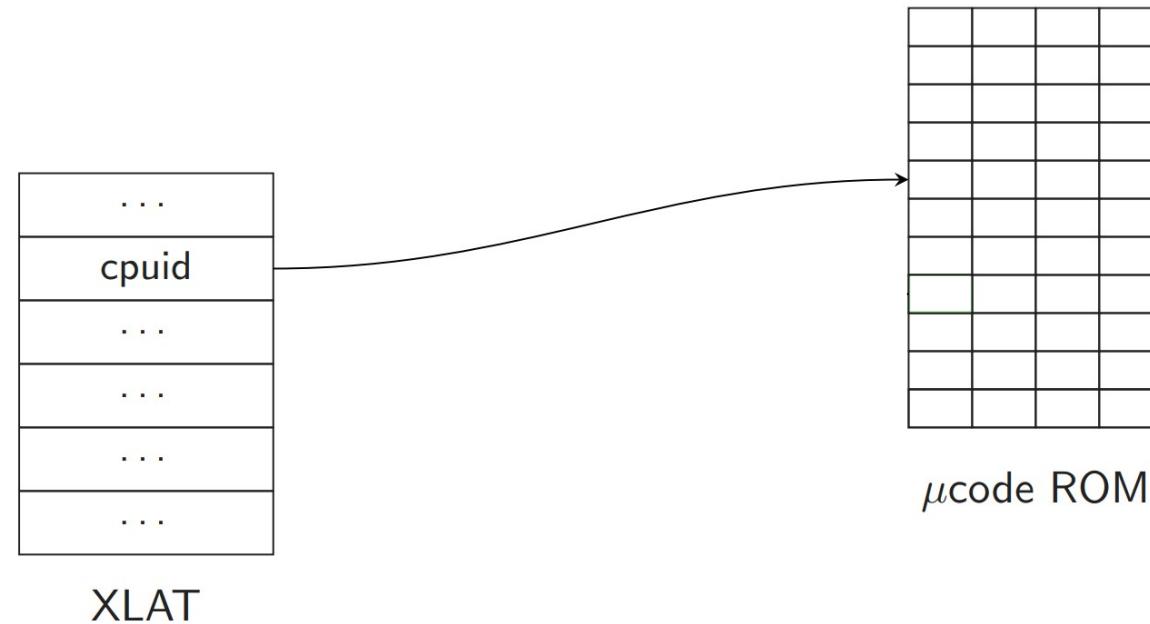
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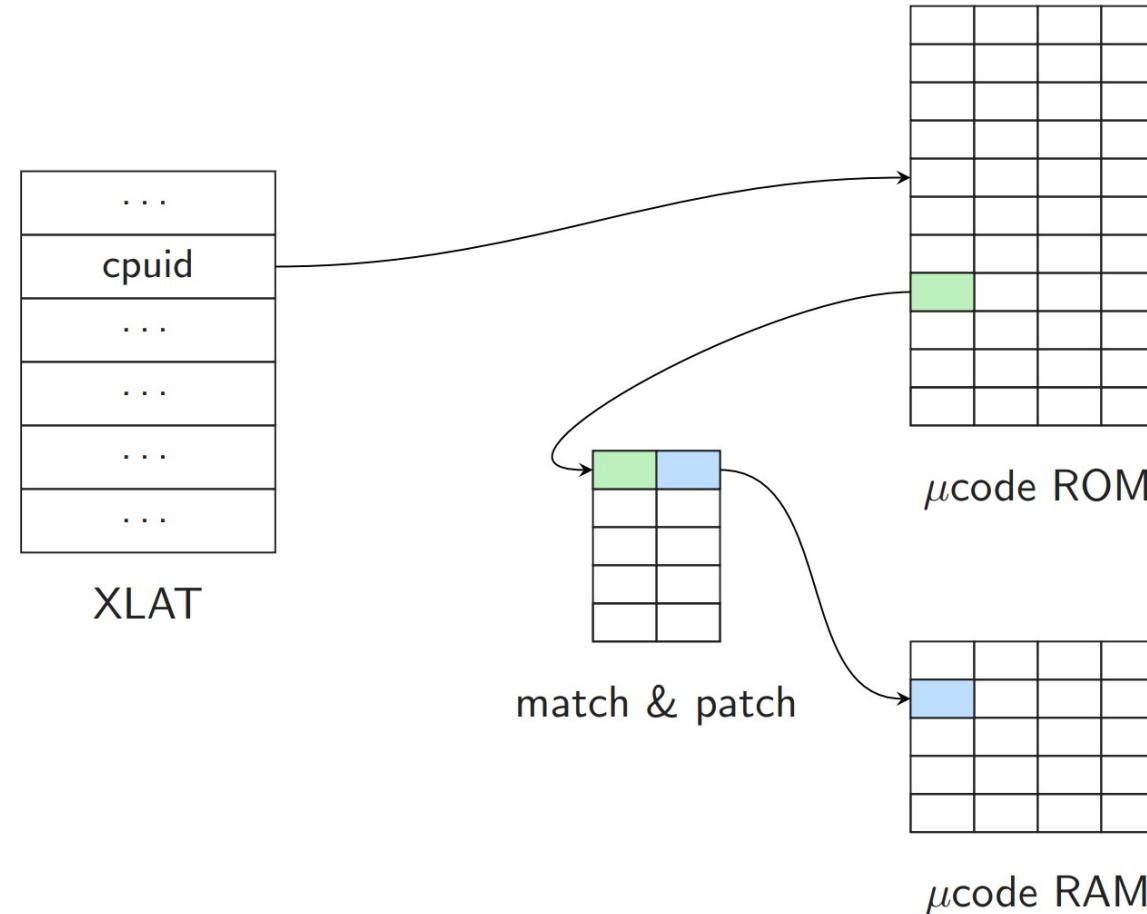


$\mu$ code ROM

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# Prior Microcode Research Efforts

Work

**CHIP-RED-PILL**  
(Ermolov et al., 2021)

Main Contributions

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These efforts proved that **microcode can be modified**.  
But **not in a standard Linux runtime environment**.

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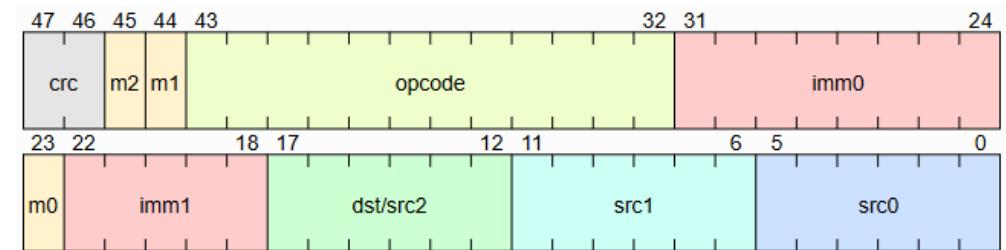
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- We adopted **CustomProcessingUnit**'s microcode toolchain (DSL and assembler/serializer).

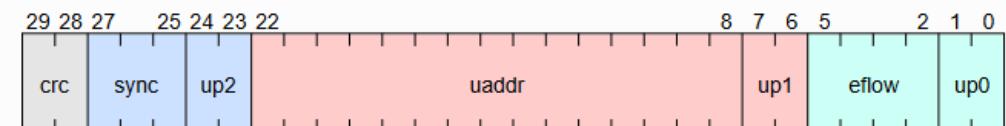
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.org 0x7c00
.patch 0x428
.entry 0

r64src := ZEROEXT_DSZ64(0x1146)
labuser@bmax-1:~/microcode-project/ucode_patches$ cat rdrand.h
struct ucode_patch_req rdrand_req = {
    .name = "rdrand",
    .addr = 0x7c00,
    .hook_address = 0x0428,
    .hook_entry = 0x00,
    .patch_rows = 1,
    .patch_data = {
        // U7c00: r64src := ZEROEXT_DSZ64(0x1146); unk_256() !m1; NOP SEQW LFNCEWAIT, UEND0
        {0x404846442008, 0x125600000000, 0x0, 0x130000f2},
    }
};
```

**μop:**



**Seqword:**



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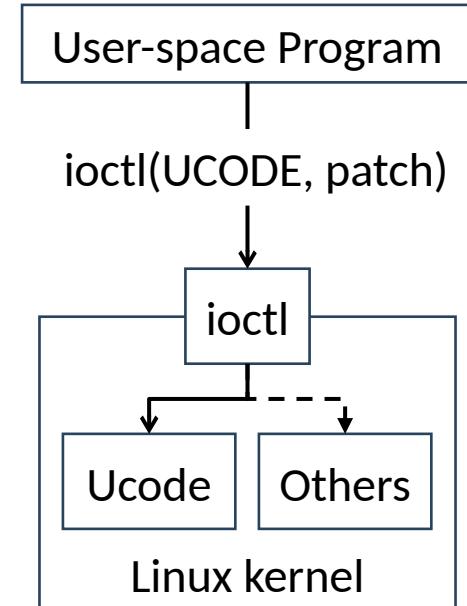
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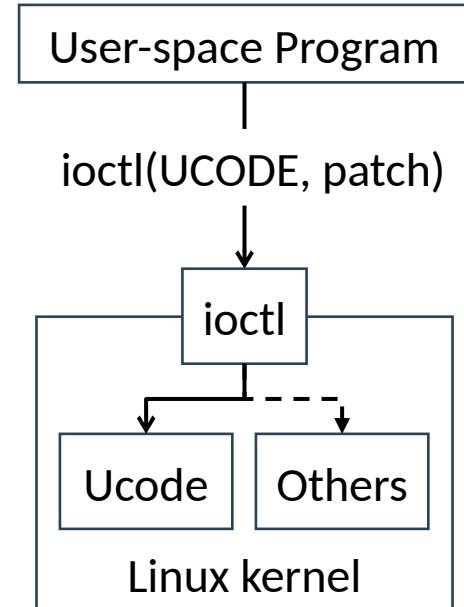
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- Developed a Linux kernel module “**Ucode**”:



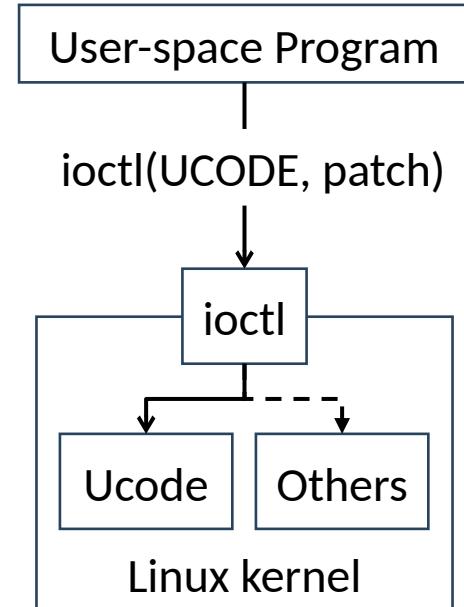
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  - Accepts and applies custom microcode patches.



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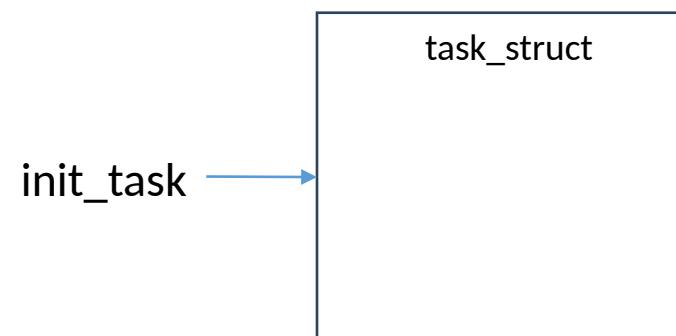
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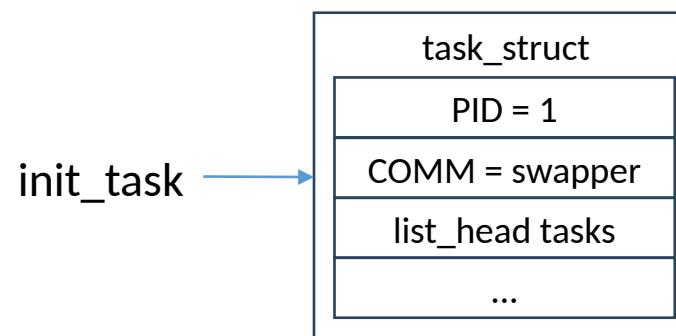
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  - Locate the symbol init\_task, which gives us the address of the first task\_struct.
  - Once a task\_struct is found, we can **extract fields by their known offsets**:
    - For example, to read the process name: `comm = *(task_addr + comm_offset)`

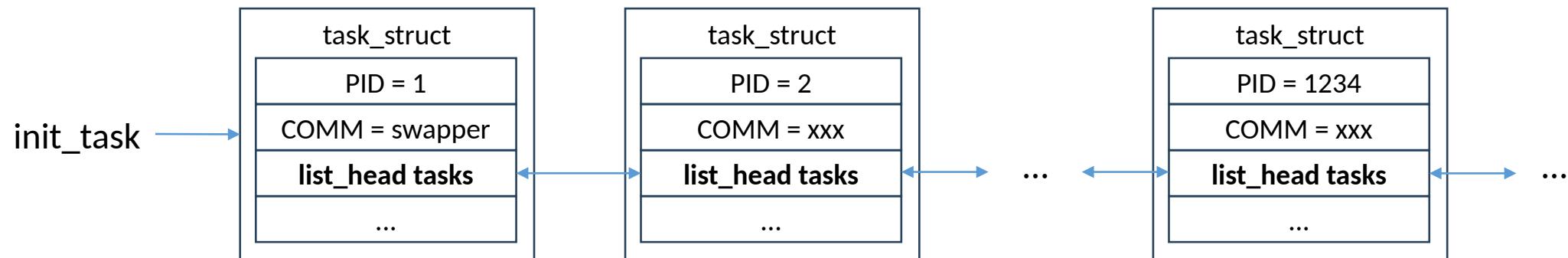


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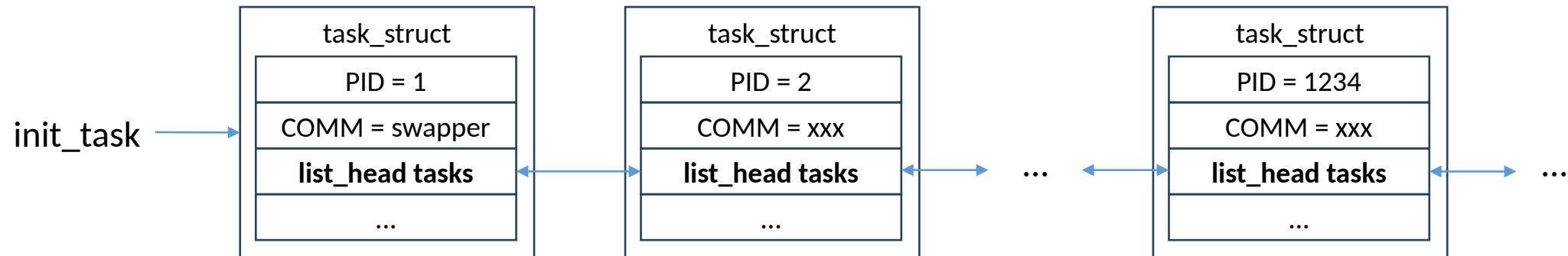
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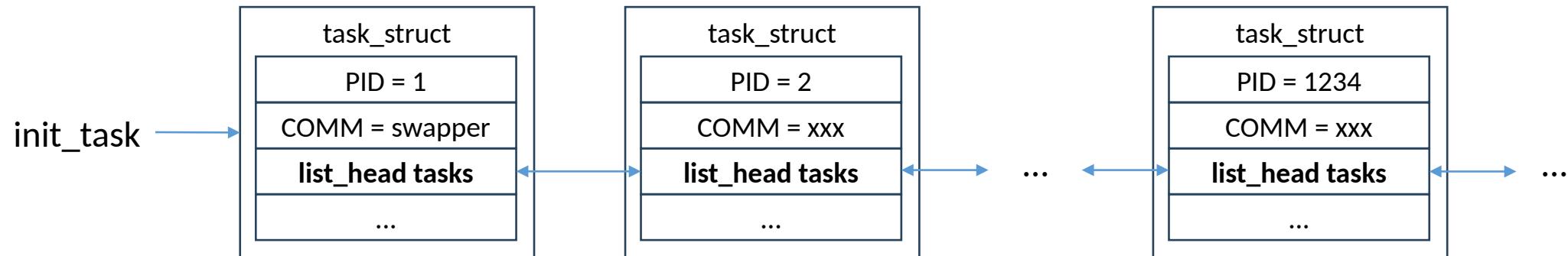
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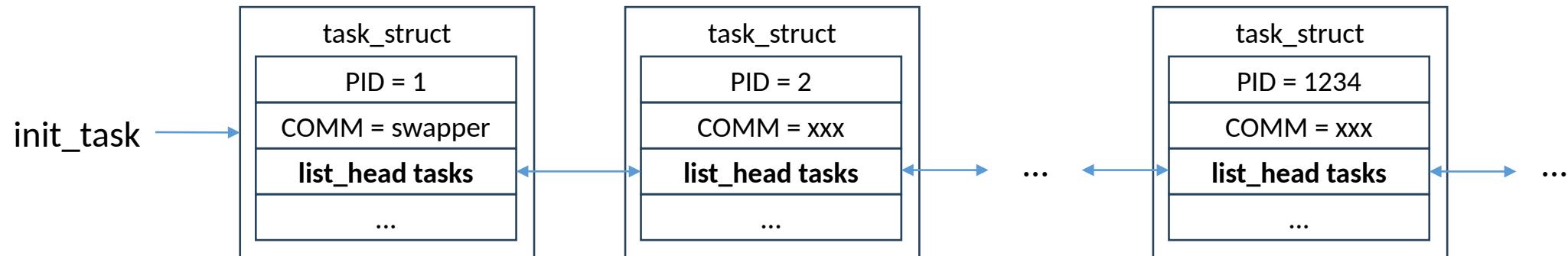
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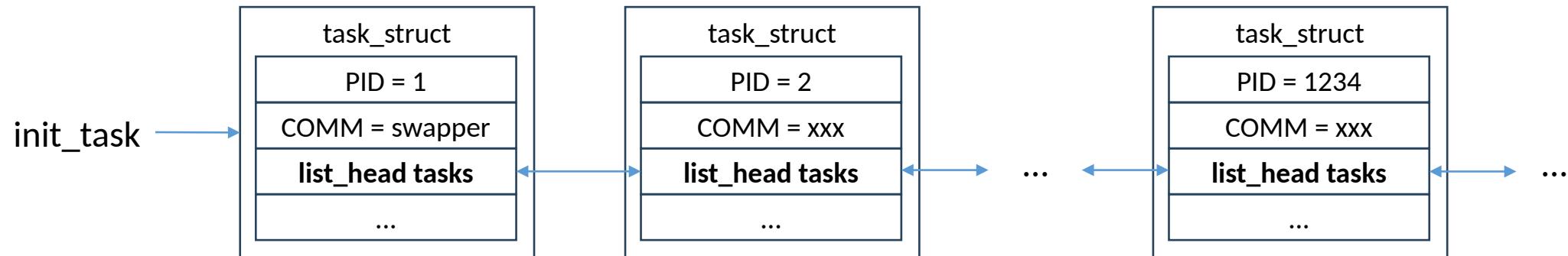
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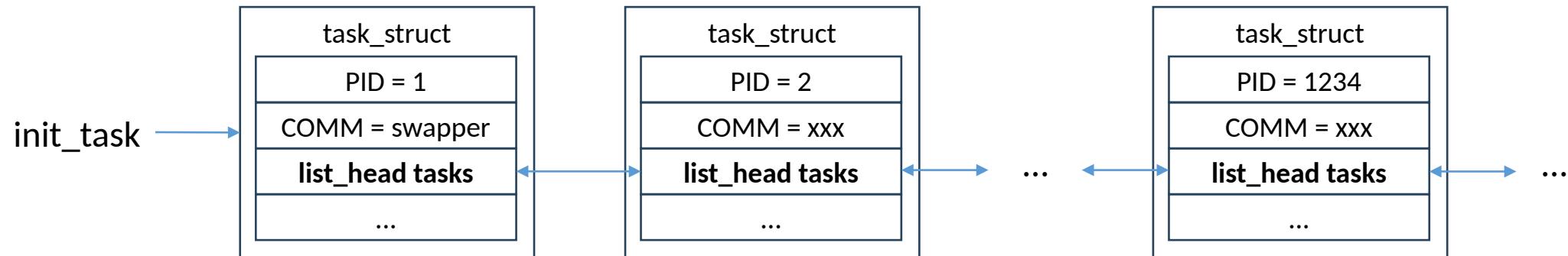
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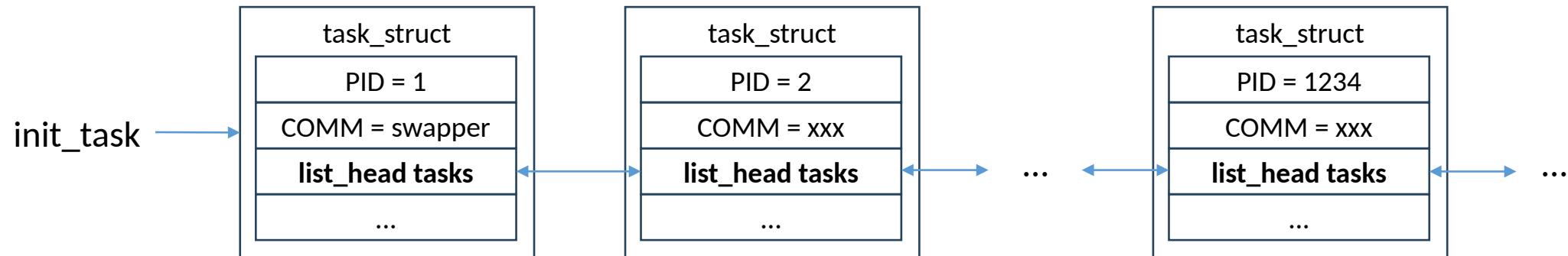
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gcc test_read_tasks.c -o test_read_tasks.o
./test_read_tasks.o
Patch applied successfully!
== init_task ==
Task @ 0xfffffffffab010940: PID = 0, COMM = swapper/0

== Iterating through all task_struct ==
Task @ 0xfffff974e402a3200: PID = 1, COMM = systemd
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Task @ 0xfffff974e4032b200: PID = 6, COMM = kworker/R-slub_
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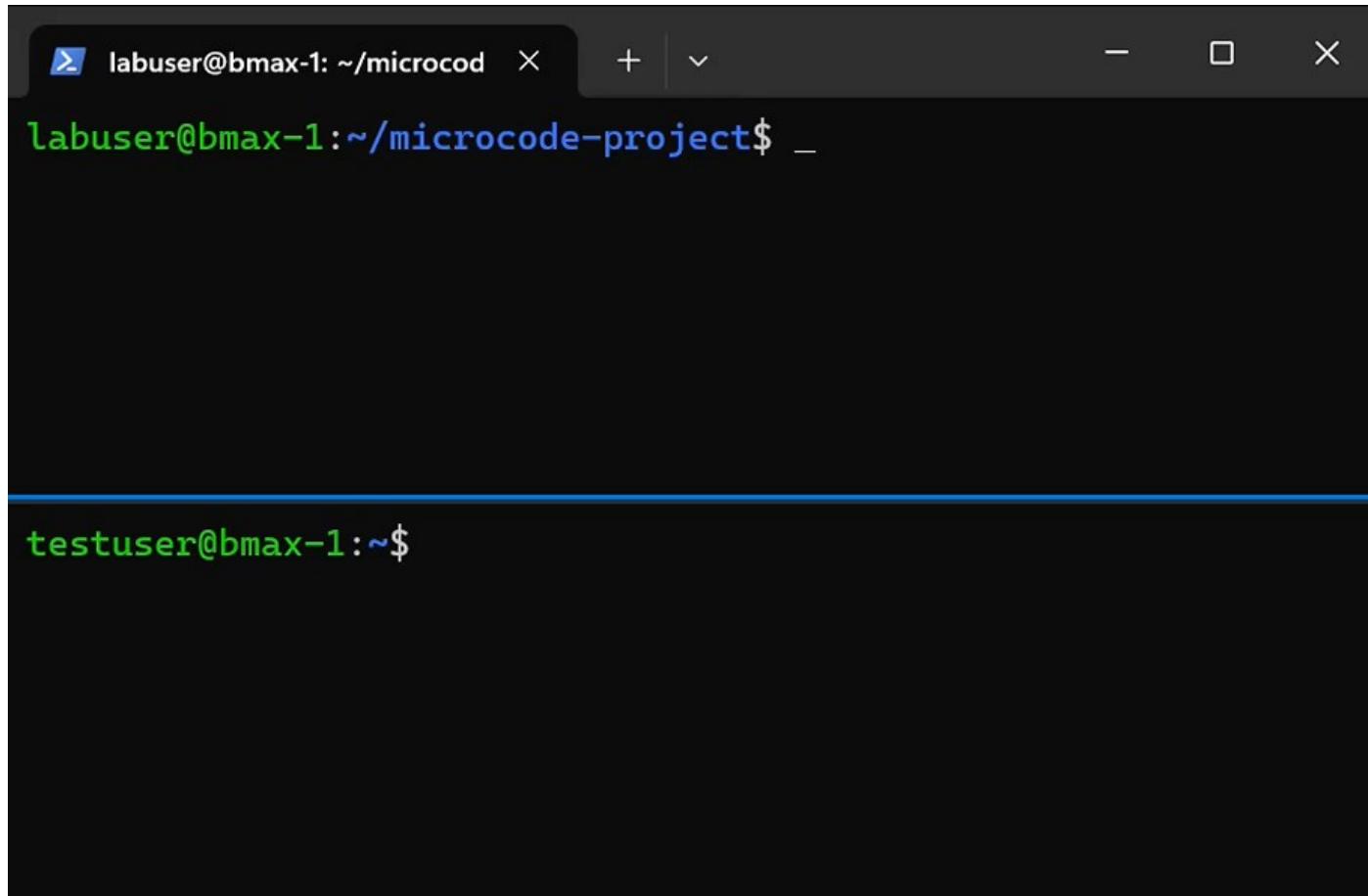
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  - Read the password from the buffer.

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The image shows a terminal window with two sessions. The top session is for user `labuser`, with the command `cat /etc/sudoers` running. The bottom session is for user `testuser`, which is a root shell. The password for the `sudo` command is visible in the `testuser` session.

```
labuser@bmax-1: ~/microcod
labuser@bmax-1:~/microcode-project$ cat /etc/sudoers
testuser@bmax-1:~$
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- User program executes RDRAND → immediate core ID returned (no syscall, no kernel transition).

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- Demonstrates microcode as a viable fast path for frequent syscalls.

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- **Better Framework**  
Build a microcode framework that supports **per-core** and **per-thread** customization, integrates with the Linux kernel, and provides easier user-space access.
- **AMD Support**  
Port and test on AMD Zen CPUs to explore cross-vendor compatibility and new customization opportunities.

# Q & A

# Thank you!

*This work is supported in part by the US Office of Naval Research (ONR) under grant N000142412642.*

