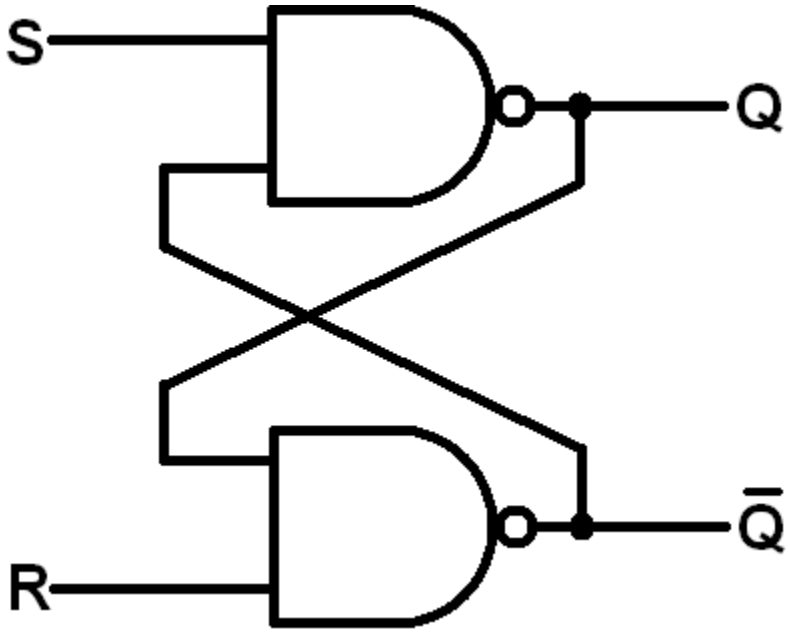
CSCIU 210 – Computer Organization

Homework-5Key, Weight: 30 points

Due on Wednesday, October 31, 2018 at the beginning of the lecture (Hard Copy)

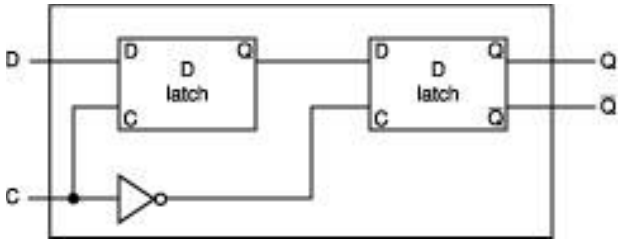
Note: You need to include your calculation details to receive full credit!

Q1. [10 points] Draw a NAND SR latch and write out its truth table.

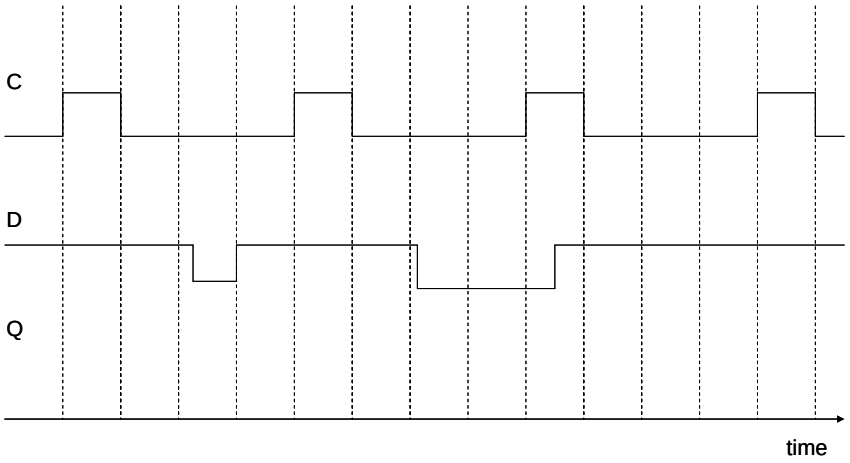


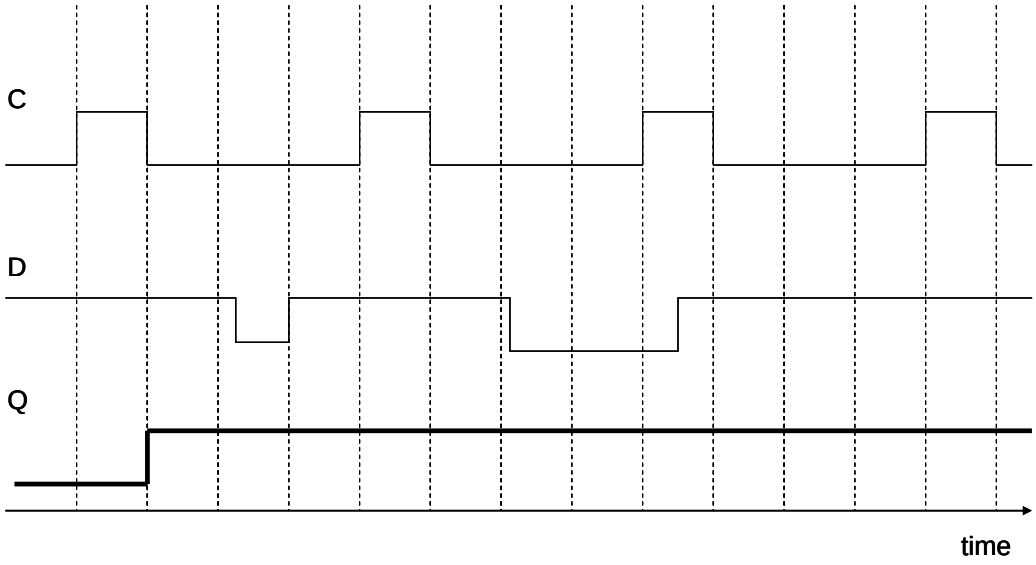
S	R	Q	$\bar{Q}$
0	0	Undefined	
0	1	1	0
1	0	0	1
1	1	Memory State	

Q2. [5 points] A D flip-flop output diagram is illustrated below

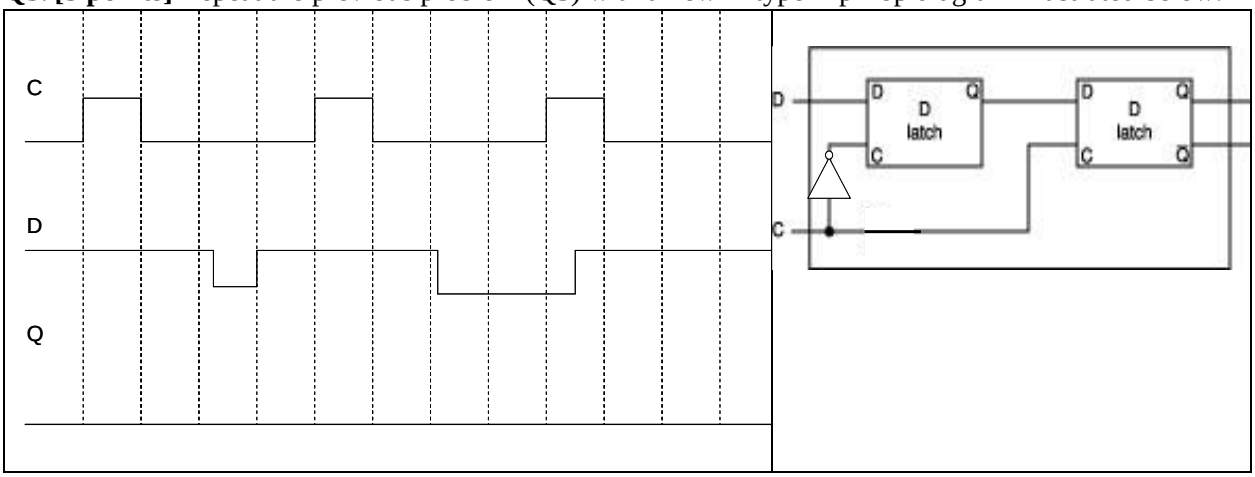


Assuming that (i) the initial value of Q is 0 and (ii) setup and hold time of D-type flip flop is zero, then, based on the clock and input waveform below, plot its output (Q) waveform.

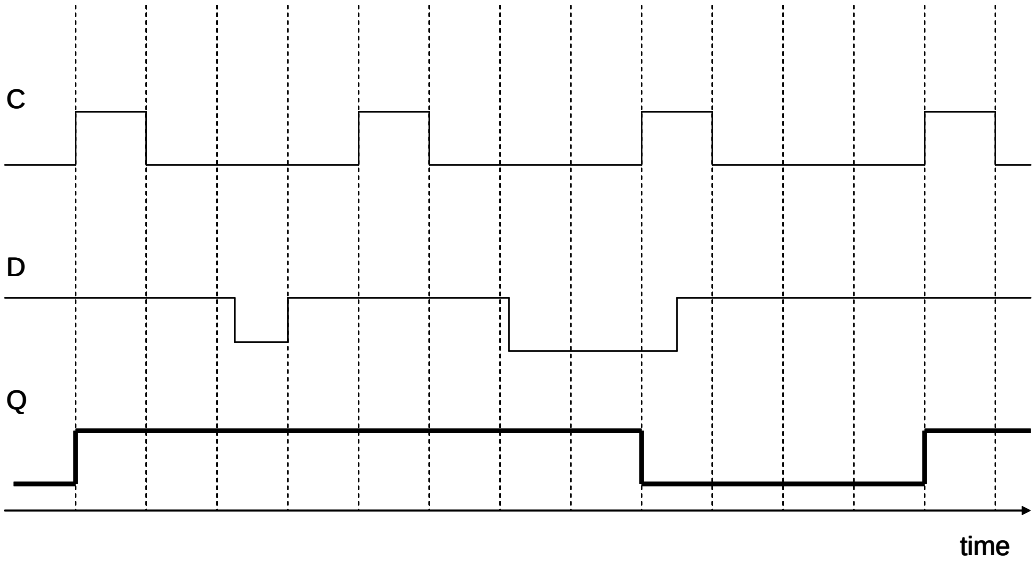




Q3. [5 points] Repeat the previous problem (Q3) with a new D-type flip flop diagram illustrated below.



Ans:



Q4. [10 points] Based on the processor covered in the lecture notes of March 2, answer the following questions

(a) Translate the assembly code "add r4, r5, r0" to the machine code used in the processor covered in the lecture.

ANS: 0010100000100101

(b) Translate the machine code [0111100111100110] back to assembly code used in the processor covered in the lecture.

ANS: `sub r12, r15, r3`