Sample Final Exam

29-Apr-19

1 May, 2019

_____ , _____
Last Name , First Name

Instructions:

- ***Show all work on the front of the test papers. No work shown may mean 0 points given!*** *If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will* ***not*** *be graded without an indication on the front.*
- ***Read*** *each question* ***carefully*** *and* ***follow the instructions****. Unless otherwise stated,* ***you must show your work and clearly illustrate your steps****.*
- *If you round a numerical answer, you must give at least* ***3 significant digits****.*
- *Put your name at the top of* ***each*** *test page and be sure your exam consists of the number of pages designated in the headers.*
- *The space provided does* ***NOT*** *necessarily represent the amount of writing necessary.*
- *You may* ***not*** *use any notes, homework, labs, or other books. Only* ***memoryless*** *calculator is allowed.*
- ***You may not use any notes, homework, labs, or other books.***

COMMENTS, FEEDBACK, or any special instructions for the professor:

Problem	Available	Points
1		
2		
3		
4		
5		
6		
7		
Total	100	

Important: *In completing this exam, I used a calculator with no communications capability, and no information of relevance to the course was stored in the calculator. I did not use any other electronic device or any other references. My work was solely my own.*

Your Calculator's Maker and Model#: _____

Signature: _____

You must sign this to receive credit for the exam.

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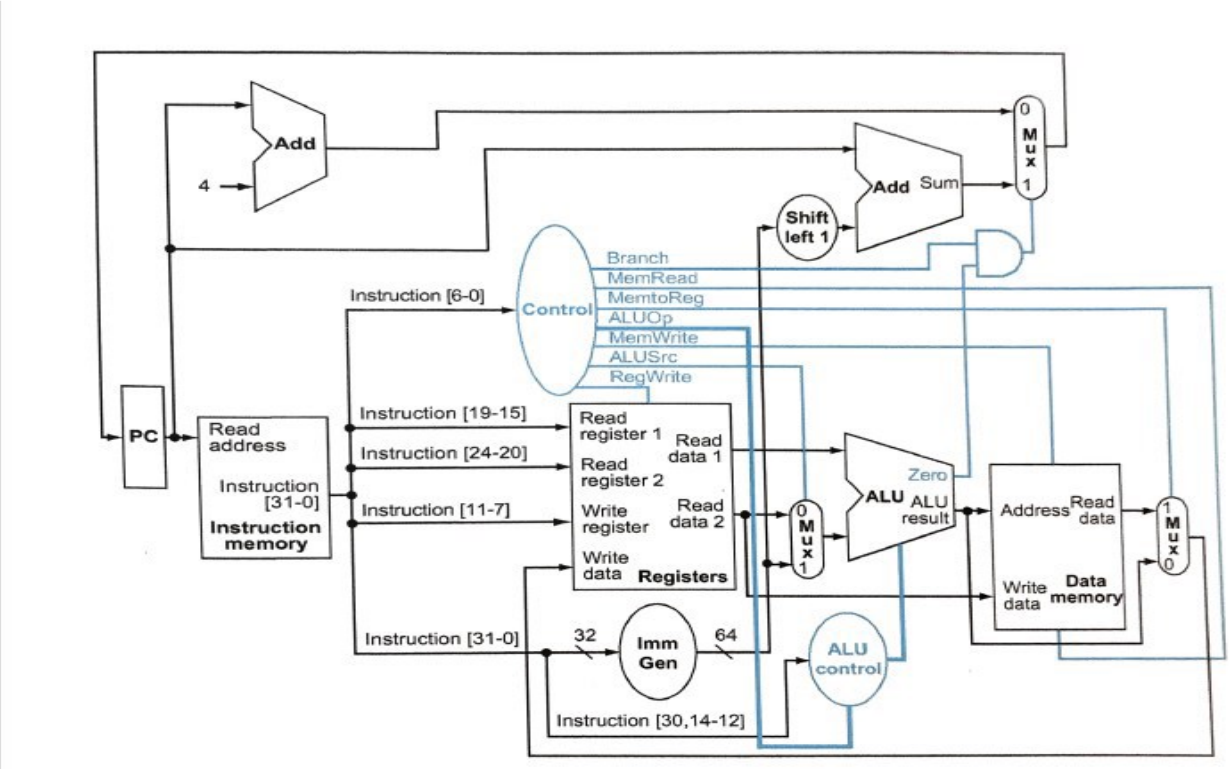
Remember to show ALL work here and in EVERY problem on this exam.

Q1. The following processor diagram is the single cycle processor we covered in the class. This processor can handle selected MIPS R, I, and J type instructions. **(Please try yourself)**



RegWrite: when equal to 1, enabling the computer to write data into the register file
MemRead: when equal to 1, enabling the computer to read data from data memory
MemWrite: when equal to 1, enabling the computer to write data into data memory

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(Note: While working on the following problems, if you decide the value of some control signal does not matter, then you must use X as your answer.)

a) Complete the following control signal table for MIPS command `add`.

MIPS Instruction	Reg Write	Memto-Reg	Branch	ALUSrc		
add						

b) Complete the following control signal table for MIPS command `lw`.

MIPS Instruction	Reg Write	Memto-Reg	Branch	ALUSrc		
lw						

c) Complete the following control signal table for MIPS command `sw`.

MIPS Instruction	Reg Write	Memto-Reg	Branch	ALUSrc		
sw						

a) Complete the following control signal table for MIPS command `beq`.

MIPS Instruction	Reg Write	Memto-Reg	Branch	ALUSrc		
beq						

e) Complete the following control signal table for MIPS command `j`.

MIPS Instruction	Reg Write	Memto-Reg	Branch	ALUSrc		
j						

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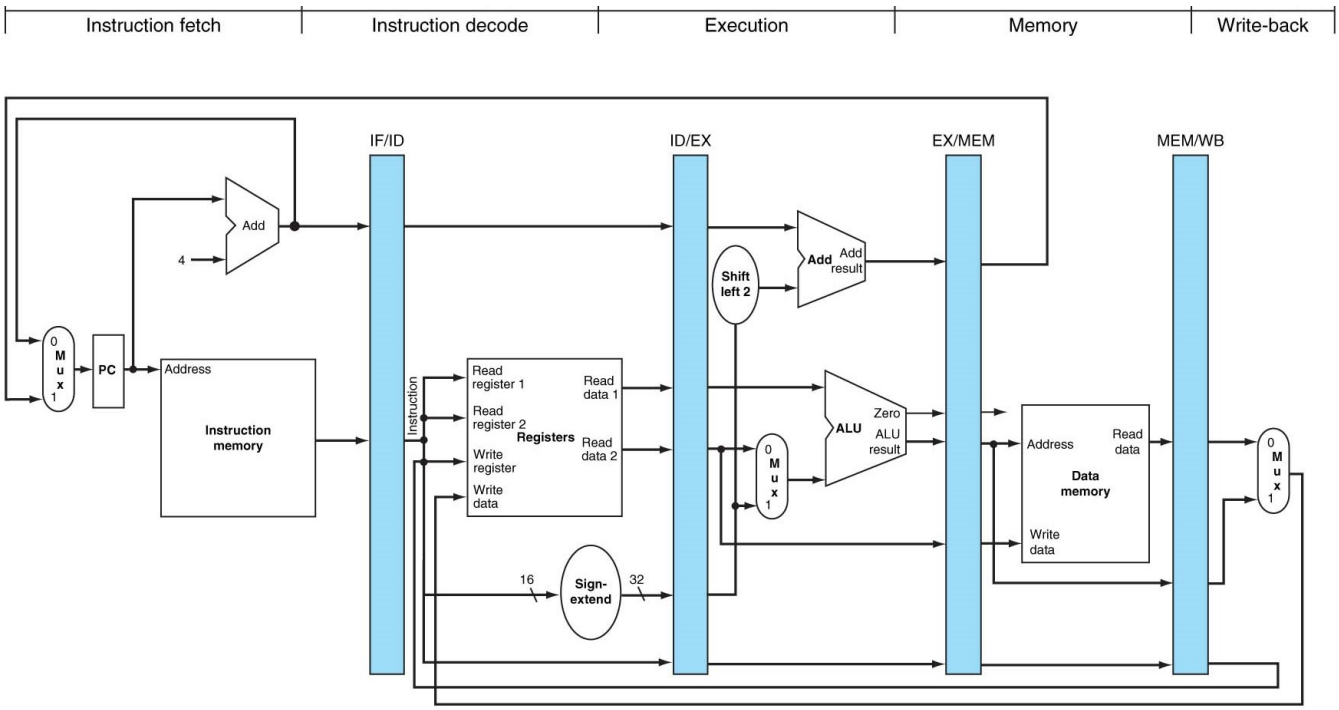
Q2. The processor diagram below is the pipelined MIPS datapath we covered in class.



Assume the individual stages of the datapath above have the foloowing latencies

IF	ID	EX	MEM	WB
200ps	300ps	150ps	330ps	200ps

a) What is the clock cycle time in a pipelined and non-pipelined processor?
Answer: pipelined: 330 ps and non-pipelined: 1180 ps

b) Assume NO forwarding or other advanced technologies used in the pipelined processor illustrated above, identify where stalling might happen in the program below.

```
add     $s0, $s1, $s2
sub     $s0, $s0, $s3  - wait for the result from add inst.
beq     $s1, $s3, L    - wait for branch determination
ori     $t1, $t2, $t3
lw      $t2, 12($t5)
add     $t8, $t2, $t1   - wait for $t2 to load
.
.
.
L:…
```

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Q3.

a) Represent -9.125_{10} with single precision IEEE 754 standard. (Note: You must write your answer as a 32-bit binary sequence).

Answer: 1 10000010 00100100000000000000000

b) Determine the object which is represented with single precision IEEE 754 standard as `01111111111000000000000000000000`. Write your answer in decimal format if possible.

Answer: 5.95×10^{38}

c) Determine the object which is represented with the single precision IEEE 754 standard as `01000001111000000000000000000000`. Write your answer in decimal format if possible.

Answer: $(28)_{10}$

Q8. Using the sample table shown in below calculate seven (7) divided by two (2) using non-performing division. You need to show the contents of each register on each step.

Solution:

Iteration	Step	Quotient	Divisor	Remainder
0	Initial values	0000	0010 0000	0000 0111
1	1: Rem = Rem – Div	0000	0010 0000	1110 0111
	2b: Rem < 0 ⟹ +Div, SLL Q, Q0 = 0	0000	0010 0000	0000 0111
	3: Shift Div right	0000	0001 0000	0000 0111
2	1: Rem = Rem – Div	0000	0001 0000	1111 0111
	2b: Rem < 0 ⟹ +Div, SLL Q, Q0 = 0	0000	0001 0000	0000 0111
	3: Shift Div right	0000	0000 1000	0000 0111
3	1: Rem = Rem – Div	0000	0000 1000	1111 1111
	2b: Rem < 0 ⟹ +Div, SLL Q, Q0 = 0	0000	0000 1000	0000 0111
	3: Shift Div right	0000	0000 0100	0000 0111
4	1: Rem = Rem – Div	0000	0000 0100	0000 0011
	2a: Rem ≥ 0 ⟹ SLL Q, Q0 = 1	0001	0000 0100	0000 0011
	3: Shift Div right	0001	0000 0010	0000 0011
5	1: Rem = Rem – Div	0001	0000 0010	0000 0001
	2a: Rem ≥ 0 ⟹ SLL Q, Q0 = 1	0011	0000 0010	0000 0001
	3: Shift Div right	0011	0000 0001	0000 0001

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Q4.

(a) Write the MIPS code for the following statement using the following mapping: a:$s1; b:$s2; c:$s3; and d:$s4

a =c / d;
b = c % d;

ANS:

```
div   $s3, $s4      # lo=c/d, hi=c%d
mflo  $s1           # get quotient
mfhi  $s2           # get remainder
```

(b) Write the MIPS code for the following multiplication using the following mapping: b:$s0; c:$s1; and let a be $s2 and $s3 (since it may be up to 64 bits)

a = b * c

ANS:

```
mult $s0, $s1     # b*c
mfhi $s2          # upper half of
                  # product into $s0
mflo $s3          # lower half of
                  # product into $s1
```

(c) List three floating-point operations that cause NaN to be created?

ANS:

(1) Divide 0 by 0
(2) Multiply 0 by infinity
(3) Adding infinity to negative infinity

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Q5.

(a) Why is miss rate not a good metric for evaluating cache performance? What is the appropriate metric? Give its definition. What is the reason for using a combination of first and second- level caches rather than using the same chip area for a larger first-level cache?

Answer:

The ultimate metric for cache performance is average access time: tavg = thit + miss-rate * tmiss. The miss rate is only one component of this equation. A cache may have a low miss rate, but an extremely high penalty per miss, making it lower-performing than a cache with a higher miss rate but a substantially lower miss penalty. Alternatively, it may have a low miss rate but a high hit time (this is true for large fully associative caches, for instance).

Multiple levels of cache are used for exactly this reason. Not all of the performance factors can be optimized in a single cache. Specifically, with tmiss (memory latency) given, it is difficult to design a cache which is both fast in the common case (a hit) and minimizes the costly uncommon case by having a low miss rate. These two design goals are achieved using two caches. The first level cache minimizes the hit time, therefore it is usually small with a low-associativity. The second level cache minimizes the miss rate, it is usually large with large blocks and a higher associativity.

(b) Design a 128KB direct-mapped data cache that uses a 32-bit address and 16 bytes per block. Calculate the following:

(i) How many bits are used for the byte offset?

7 bits

(ii) How many bits are used for the set (index) field?

15 bits

(iii) How many bits are used for the tag?

10 its

(c) The memory architecture of a machine X is summarized in the following table.

Virtual Address	54 bits
Page Size	16 K bytes
PTE Size	4 bytes

Assume that there are 8 bits reserved for the operating system functions (protection, replacement, valid, modified, and Hit/Miss- All overhead bits) other than required by the hardware translation algorithm. Derive the largest physical memory size (in bytes) allowed by this PTE format. Make sure you consider all the fields required by the translation algorithm.

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Solution:

Since each Page Table element has 4 bytes (32 bits) and the page size is 16K bytes:

(1) we need $\log_2(16*2^{10}*2^3)$, ie, 17 bits to hold the page offset

(2) we need 32 – 8 (used for protection) = 24 bits for page number

The largest physical memory size is $2^{(17+24)}/2^{(3)}$ bytes = 2^{38} bytes = 256 GB

Q6.

(a) Assume you could make a decision upon each memory reference whether or not you want the requested address to be cached. What impact could this have on miss rate? (2 pts.)

ANS: If you knew that an address had limited temporal locality and would conflict with another block in the cache, it could improve miss rate. On the other hand, you could worsen the miss rate by choosing poorly which addresses to cache.

(b) 16KB of data, direct-mapped, 4 word blocks

What would happen if you read data from the Following two address? Please Explain? (8 pts.)
Chose from: Cache: Hit, Miss, Miss w. replace
Values returned: a, b, c, d, e, ..., k, l

Read address 0x00000030?
00000000000000000 0000000011 0000

Read address 0x0000001c?
00000000000000000 0000000001 1100

Index	Valid	Tag	0x0-3	0x4-7	0x8-b	0xc-f
0	0					
1	1	2	i	j	k	l
2	0					
3	1	0	e	f	g	h
4	0					
5	0					
6	0					
7	0					

… …..

ANS:

- 0x00000030 a hit

Index = 3, Tag matches, Offset = 0, value = e

Address (hex)	Value of Word
…	…
00000010	a
00000014	b
00000018	c
0000001C	d
…	…
00000030	e
00000034	f
00000038	g
0000003C	h
…	…
00008010	i
00008014	j
00008018	k
0000801C	l
…	…

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- 0x0000001c a miss

Index = 1, Tag mismatch, so replace from memory,
Offset = 0xc, value = d

- Since reads, values must = memory values whether or not cached:
  - 0x00000030 = e
  - 0x0000001c = d

Q7.

(a) When an interrupt is detected, the status register is saved and all but the highest priority interrupt is disabled. Why low-priority interrupts are disabled?

ANS:

Low-priority interrupts are disabled to prevent them from interrupting the handling of the current interrupt that is higher priority. The status register is saved to assure that any lower priority interrupts that have been detected are handled when the status register is restored following handling of the current interrupt.

(b) In memory system, assuming:

- 1 memory bus clock cycle to send the address
- 15 memory bus clock cycles for each DRAM access initiated
- 1 memory bus clock cycle to send a word of data

Calculate the miss penalty and bandwidth for **1-word-wide bank of DRAMs**, **4-word wide memory, and 4-bank interleaved memory** if we have a cache block of 4 words.

ANS:

- **For 4-word block, 1-word-wide DRAM**
  - Miss penalty = 1 + 4×15 + 4×1 = 65 bus cycles
  - Bandwidth = 16 bytes / 65 cycles = 0.25 B/cycle

- **4-word wide memory**
  - Miss penalty = 1 + 15 + 1 = 17 bus cycles
  - Bandwidth = 16 bytes / 17 cycles = 0.94 B/cycle

- **4-bank interleaved memory**
  - Miss penalty = 1 + 15 + 4×1 = 20 bus cycles
  - Bandwidth = 16 bytes / 20 cycles = 0.8 B/cycle

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