CSCIU 210 – Computer Organization

Homework-1 Solutions

Due on Wednesday, September 5, 2018 at the beginning of the lecture (Hard Copy)

Q1.

Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

		Clock Rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
a.	P1	2.5 GHz	1	2	3	3
	P2	3 GHz	2	2	2	2
b.	P1	2.5 GHz	2	1.5	2	1
	P2	3 GHz	1	2	1	1

A. **[10 points]** Given a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

B. **[5 points]** What is the global CPI for each implementation?

C. **[5 points]** Find the clock cycles required in both cases. The following table shows the number of instructions for a program.

	Arith	Store	Load	Branch	Total
a.	650	100	600	50	1400
b.	750	250	500	500	2000

D. **[5 points]** Assuming that arith instructions take 1 cycle, load and store 5 cycles, and branches 2 cycles, what is the execution time of the program in a 2 GHz processor?

E. **[5 points]** Find the CPI for the program.

F. **[10 points]** If the number of load instructions can be reduced by one half, what is the speedup and the CPI?

Q2.

Compilers can have a profound impact on the performance of an application on given a processor. This problem will explore the impact compilers have on execution time.

	Compiler A		Compiler B	
	No. Instructions	**Execution Time**	**No. Instructions**	**Execution Time**
a.	$\mathbf{1 \times 10^9}$	1.8 s	$\mathbf{1.20 \times 10^9}$	1.8 s
b.	$\mathbf{1 \times 10^9}$	1.1 s	$\mathbf{1.20 \times 10^9}$	1.5 s

A. **[5 points]** For the same program, two different compilers are used. The table above shows the execution time of the two different compiled programs. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

B. **[5 points]** Assume the average CPIs found in (a), but that the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

C. **[10 points]** A new compiler is developed that uses only 600 million instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using Compiler A or B on the original processor of (a)?

Consider two different implementations, P1 and P2, of the same instruction set. There are five classes of instructions (A,B,C,D, and E) in the instruction set. P1 has a clock rate of 4 GHz, and P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 are listed in the following table.

		CPI Class A	CPI Class B	CPI Class C	CPI Class D	CPI Class E
a.	P1	1	2	3	4	5
	P2	3	3	3	5	5
b.	P1	1	2	3	4	5
	P2	2	2	2	2	6

D. **[10 points]** Assume that peak performance is defined as the fastest rate that a computer can execute any instruction sequence. What are the peak performances of P1 and P2 expressed in instructions per second?

E. **[5 points]** If the number of instructions executed in a certain program is divided equally among the five classes of instructions except for class A, which occurs twice as often as each of the others, how much faster is P2 than P1?

F. **[5 points]** At what frequency does P1 have the same performance of P2 for the instruction mix given in (e)?

Q3.
Suppose we have developed new versions of a processor with the following characteristics.

	Version	Voltage	Clock Rate
a.	Version 1	1.75 V	1.5 GHz
	Version 2	1.2 V	2 GHz
b.	Version 1	1.1 V	3 GHz
	Version 2	0.8 V	4 GHZ

A. **[5 points]** How much has the capacitive load varied between versions if the dynamic power has been reduced by 10%.
B. **[5 points]** How much has the dynamic power been reduced if the capacitive load does not change?

C. **[10 points]** Assuming that the capacitive load of version 2 is 80% the capacitive load of version 1, find the voltage for version 2 if the dynamic power of version 2 is reduced by 40% from version 1.

Solutions:

Q1

A

Class A: 10^5 instr.
Class B: 2×10^5 instr.
Class C: 5×10^5 instr.
Class D: 2×10^5 instr.

Time = No. instr × CPI/clock rate

a.	Total time P1 = $(10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3)/(2.5 \times 10^9) = 10.4 \times 10^{-4}$ s Total time P2 = $(10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2)/(3 \times 10^9) = 6.66 \times 10^{-4}$ s
b.	Total time P1 = $(10^5 \times 2 + 2 \times 10^5 \times 1.5 + 5 \times 10^5 \times 2 + 2 \times 10^5)/(2.5 \times 10^9) = 6.8 \times 10^{-4}$ s Total time P2 = $(10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 + 2 \times 10^5)/(3 \times 10^9) = 4 \times 10^{-4}$ s

B

CPI = time × clock rate/No. instr

a.	CPI (P1) = $10.4 \times 10^{-4} \times 2.5 \times 10^9/10^6 = 2.6$ CPI (P2) = $6.66 \times 10^{-4} \times 3 \times 10^9/10^6 = 2.0$
b.	CPI (P1) = $6.8 \times 10^{-4} \times 2.5 \times 10^9/10^6 = 1.7$ CPI (P2) = $4 \times 10^{-4} \times 3 \times 10^9/10^6 = 1.2$

C

a.	clock cycles (P1) = $10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3 = 26 \times 10^5$ clock cycles (P2) = $10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$
b.	clock cycles (P1) = 17×10^5 clock cycles (P2) = 12×10^5

D

a.	$(650 \times 1 + 100 \times 5 + 600 \times 5 + 50 \times 2) \times 0.5 \times 10^{-9} = 2{,}125$ ns
b.	$(750 \times 1 + 250 \times 5 + 500 \times 5 + 500 \times 2) \times 0.5 \times 10^{-9} = 2{,}750$ ns

E

CPI = time × clock rate/No. instr

a.	CPI = $2{,}125 \times 10^{-9} \times 2 \times 10^9/1{,}400 = 3.03$
b.	CPI = $2{,}750 \times 10^{-9} \times 2 \times 10^9/2{,}000 = 2.75$

F

a.	Time = $(650 \times 1 + 100 \times 5 + 300 \times 5 + 50 \times 2) \times 0.5 \times 10^{-9}$ = 1,375 ns Speedup = 2,125 ns/1,375 ns = 1.54 CPI = $1{,}375 \times 10^{-9} \times 2 \times 10^{9}/1{,}100$ = 2.5
b.	Time = $(750 \times 1 + 250 \times 5 + 250 \times 5 + 500 \times 2) \times 0.5 \times 10^{-9}$ = 2,125 ns Speedup = 2,750 ns/2,125 ns = 1.29 CPI = $2{,}125 \times 10^{-9} \times 2 \times 10^{9}/1{,}750$ = 2.43

Q2

A

$CPI = T_{exec} \times f/\text{No. Instr}$

	Compiler A CPI	Compiler B CPI
a.	1.8	1.5
b.	1.1	1.25

B

$f_A/f_B = (\text{No. Instr(A)} \times \text{CPI(A)})/(\text{No. Instr(B)} \times \text{CPI(B)})$

a.	$f_A/f_B = 1$
b.	$f_A/f_B = 0.73$

C

	Speedup vs. Compiler A	Speedup vs. Compiler B
a.	$T_{new}/T_A = 0.36$	$T_{new}/T_B = 0.36$
b.	$T_{new}/T_A = 0.6$	$T_{new}/T_B = 0.44$

D

	P1 Peak	P2 Peak
a.	4×10^9 Inst/s	2×10^9 Inst/s
b.	4×10^9 Inst/s	3×10^9 Inst/s

E

Speedup, P1 versus P2:

a.	$T_1/T_2 = 1.9$
b.	$T_1/T_2 = 1.5$

F

a.	4.37 GHz
b.	6 GHz

Q3

A

Power = $V^2 \times$ clock rate $\times$ C. $\text{Power}_2 = 0.9\ \text{Power}_1$

a.	$C_2/C_1 = 0.9 \times 1.75^2 \times 1.5 \times 10^9/(1.2^2 \times 2 \times 10^9) = 1.43$
b.	$C_2/C_1 = 0.9 \times 1.1^2 \times 3 \times 10^9/(0.8^2 \times 4 \times 10^9) = 1.27$

B

$\text{Power}_2/\text{Power}_1 = V_2^2 \times \text{clock rate}_2/(V_1^2 \times \text{clock rate}_1)$

a.	$\text{Power}_2/\text{Power}_1 = 0.62$ => Reduction of 38%
b.	$\text{Power}_2/\text{Power}_1 = 0.7$ => Reduction of 30%

C

a.	$\text{Power}_2 = V_2^2 \times 2 \times 10^9 \times 0.8 \times C_1 = 0.6 \times \text{Power}_1$ $\text{Power}_1 = 1.75^2 \times 1.5 \times 10^9 \times C_1$ $V_2^2 \times 2 \times 10^9 \times 0.8 \times C_1 = 0.6 \times 1.75^2 \times 1.5 \times 10^9 \times C_1$ $V_2 = ((0.6 \times 1.75^2 \times 1.5)/(2 \times 0.8))^{1/2} = 1.31$ V
b.	$\text{Power}_2 = V_2^2 \times 4 \times 10^9 \times 0.8 \times C_1 = 0.6 \times \text{Power}_1$ $\text{Power}_1 = 1.1^2 \times 3 \times 10^9 \times C_1$ $V_2^2 \times 4 \times 10^9 \times 0.8 \times C_1 = 0.6 \times 1.1^2 \times 3 \times 10^9 \times C_1$ $V_2 = ((0.6 \times 1.1^2 \times 3)/(4 \times 0.8))^{1/2} = 0.825$ V