RISC-V Vector Extension in Rust

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RISC-V Vector Extension

- SIMD
- Scalable Vectors (~ ARM SVE)
  - Per-core defined size
  - Length determined at runtime
- Target agnostic → Longevity
- Needs language support!

```
let mut current_max = 0;

while length > 0 {
    // 1. Request vector of maximum size `length`
    let iteration_length = vsetvli(length);

    // 2. Adjust with iteration maximum
    let vs = vle8(x);
    current_max = u8::max(current_max, vredmax(vs));

    // 3. Housekeeping loop variables
    x += iteration_length;
    length -= iteration_length;
}
```

Challenge

`Sized` or `!Sized`

```
struct v8int {
    _inner: [u8],
}
```

Perspectives & Conclusion

- Examples are running
- Still, many fundamental issues
- On my way with RISC-V intrinsics
- Decrease maintenance burden
- Increase RISC-V adoption