ROHITH NEERATI

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EDUCATION:

The University of Texas at Dallas, Richardson, USA **May 2024**

Master of Science, Computer Engineering – VLSI and Embedded Systems **GPA: 3.52**

Courses: VLSI Design, Advanced Digital Logic, Computer Architecture, ASIC, Machine Learning, Algorithms, Design and Analysis of Reconfigurable Systems, Advanced Digital Signal Processing, Embedded Systems, HDL

Kakatiya Institute of Technology and Science **May 2021**

Bachelor of Technology, Electrical and Electronics Engineering

ACADEMIC PROJECTS:

Layout and Verification of 32 Bit Asynchronous FIFO in 70nm Technology

- Implemented Asynchronous FIFO design with Synchronizer. Tested design in VCS using systemverilog, synthesized design (9000 cells) in DesignVision. Designed Custom Standard Cell library in Virtuoso.
- Performed Automatic Placement and Routing in Innovus. Analyzed FIFO schematic and layout with PEX netlist using HSPICE. Conducted STA in PrimeTime and fixed timing violations and verified final layout by clean DRC, LVS reports.

ASIC Design and Verification of Mini Stereo Digital Audio Processor(MSDAP)

- Designed a low-cost, low-power MSDAP, featuring fully pipelined two 256 order FIR LPFs using 18nm library, SIP0, ALU, Controller, 8kb Memory, operating at 28.66 MHz System Clock and 768 KHz Data Clock.
- Synthesized Verilog RTL using Design Compiler (DC), Physical Design in IC Compiler (ICC), TCL and Perl Scripts for automation. Verified MSDAP through RTL simulation in VCS and Gate level simulation (post synthesis) in ModelSim.

I2C Controller Core Verification Using UVM Methodology

- Developed Advanced UVM Verification environment for I2C controller core with wishbone interface using transaction level and layered architecture. Environment constructed in Synopsys VCS.
- Performed functional coverage, code coverage of RTL using verification test plan consisting of constraint randomized stimulus, assertions, cover groups, directed tests. Achieved Overall coverage of 92% with cover groups.

Verification of Multi-Channel Data Formatter

- Architected UVM verification environment with essential components such as driver, sequencer, monitor, scoreboard, and reference model.
- Generated Constraint randomized stimulus and utilized conditional constraints, and inheritance to create packets. Created cover groups and attained functional, code, and toggle coverage of 95%.

Fault Analysis of Stuck at Models using Synopsys TetraMAX and ATPG

- Designed the circuit using Structural HDL and performed ATPG to determine test Vectors, Stuck at Faults and fault coverage using Synopsys TetraMAX.
- Verified results reported by tool with handwork analysis (1. Fault collapsing, 2. Test generation, 3. Fault simulation).

PROFESSIONAL EXPERIENCE:

RTL Design and Verification Trainee at Maven Silicon, India **February 2022 – March 2022**

- Certified RTL Design and Verification Engineer, Trained on Verilog, System Verilog, UVM, Hands on Experience with Memory Model Verification

Hardware Engineer Intern, Shilpa Engineering and Contractors, India **June 2021 – July 2021**

- Troubleshoot, maintain and repair of electrical equipment in industrial environments, including transformers, switchgear, energy meters, and SCADA devices. Utilized instruments like multimeters, oscilloscope.

TECHNICAL SKILLS:

Languages: C, C++, Python, Verilog, SystemVerilog, MATLAB

RTL Design Tools: Cadence (Virtuoso, Innovus, Tempus, JasperGold, Xcelium), Mentor Graphics Calibre (DRC, LVS, PEX), Synopsys (VCS, DesignVision, PrimeTime, TetraMAX, HSPICE, WaveView), Quartus Prime, Intel HLS, Perl Scripting, TCL, Perl, Shell scripting

Methodologies: UVM, SystemVerilog Assertions, Constraint Randomization, Coverage Analysis

Standards: SPI, I2C, UART, APB, JTAG, AHB

Certifications: Basic Static Timing Analysis by Cadence, Design for Test by Cadence, Metric Driven Verification