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ECE-'C' 4EO

IC Assignment

① Comparision of CMOS and TTL logic families

There are several factors to consider in TTL / CMOS interfacing, and the first is noise margin. The LOW-state DC noise margine depends on V_{OL} max of the driving output and V_{IL} max of driven input, and equal. V_{IL} max - V_{OL} max. Similarly, the HIGH-state DC noise margin equals V_{OH} min - V_{IH} min.

For example, the low state DC noise margin of HCT driving TTL is 0.8 - 0.33 = 0.47V and high state is 3.84-2.0 = 1.84V. On the other hand, the high state margin of TTL driving HC or AC doesn't work.

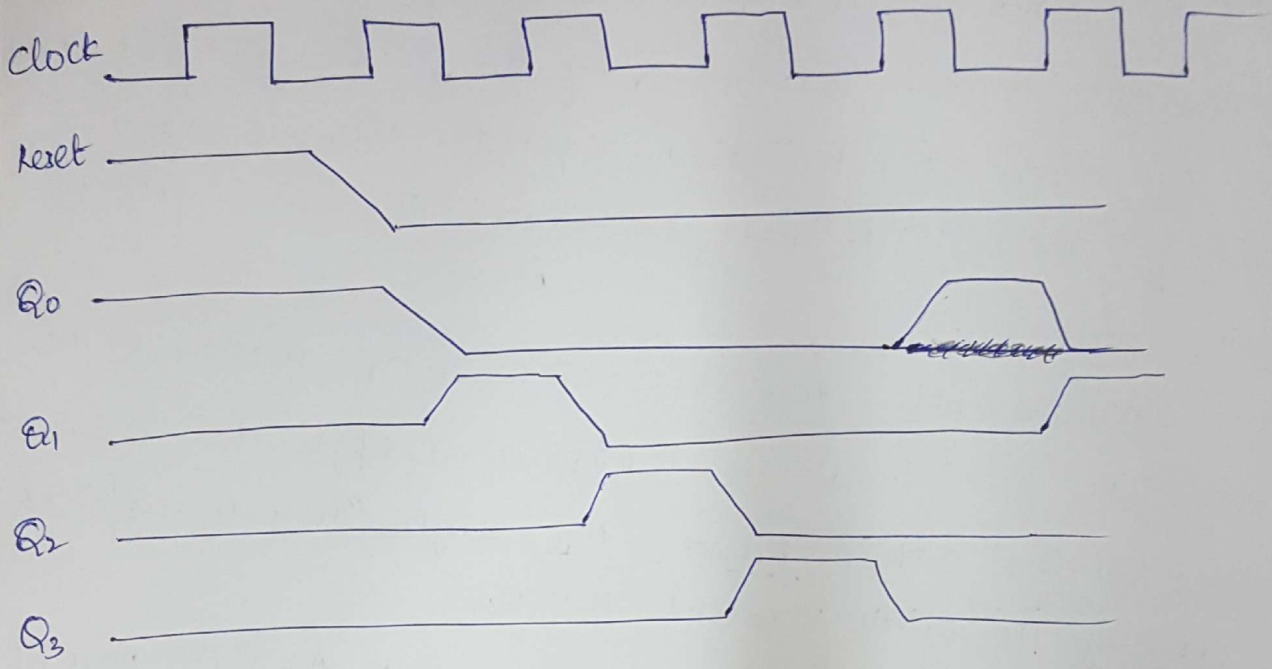
The next factor to consider is fanout. AC with pure TTL designer must sum input current requirement of devices driven by an output. when TTL drives CMOS, since CMOS input requires almost no current in either state. On the other hand, TTL i/p, especially in the low state.

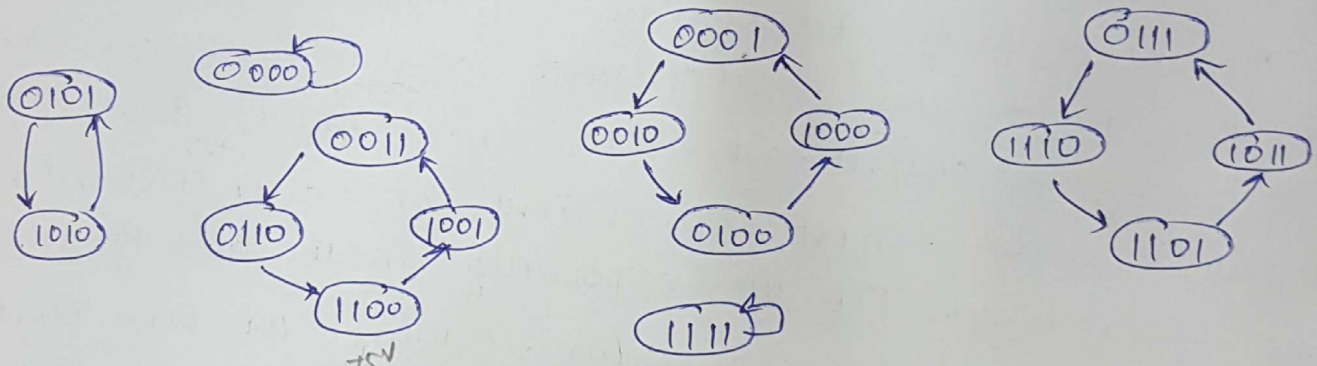
The last factor is capacitive loading. we seen that load capacitance increases both the delay and power dissipation of logic circuit.

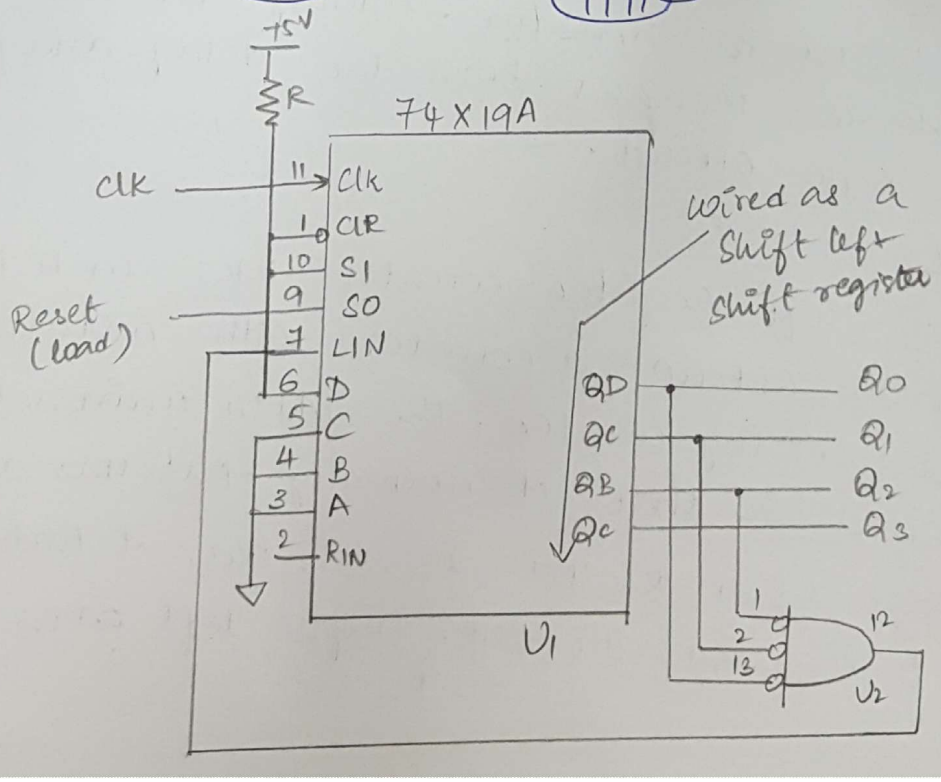
② Ring Counter:

The simplest shift register counter uses an n-bit shift register to obtain a counter with n states, and is called a ring counter. The 74194 universal shift register is wired so that it normally performs a left shift. however, when RESET is asserted, it loads 0001. Once RESET is neglected, the 194 shifts left on each clock trick.

The ring counter has one major problem, it is not robust. If its single output is lost due to a temporary hardware problem.



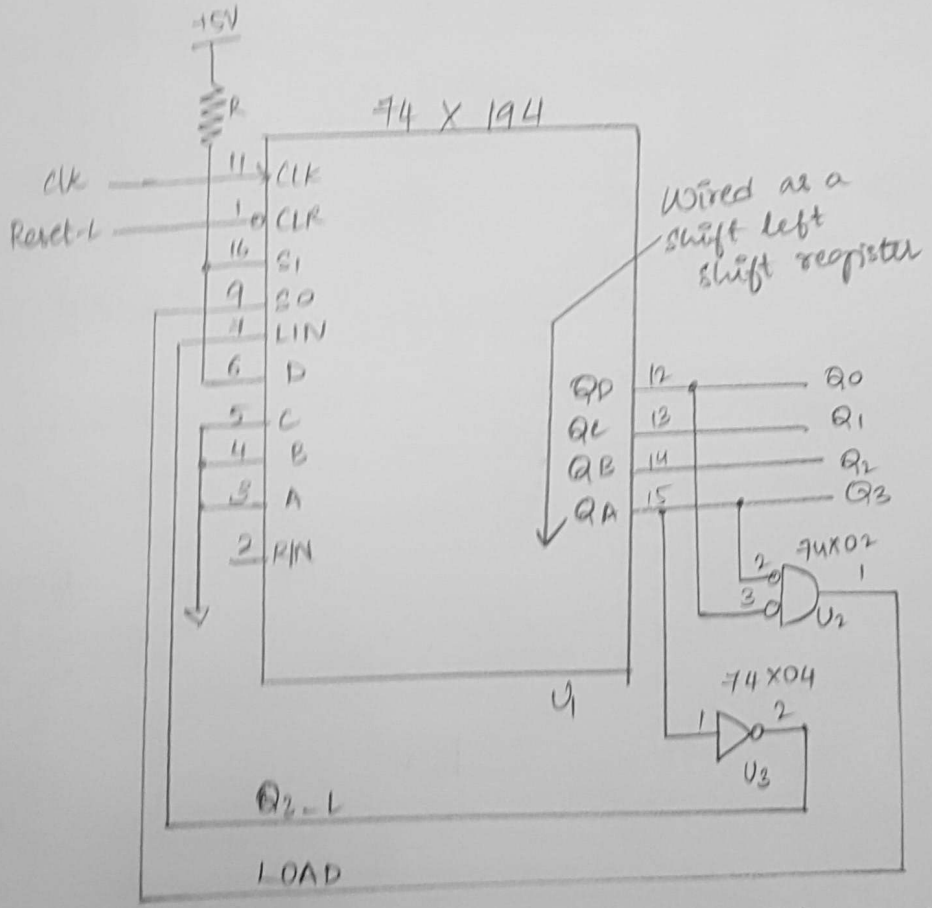




Johnson Counter:

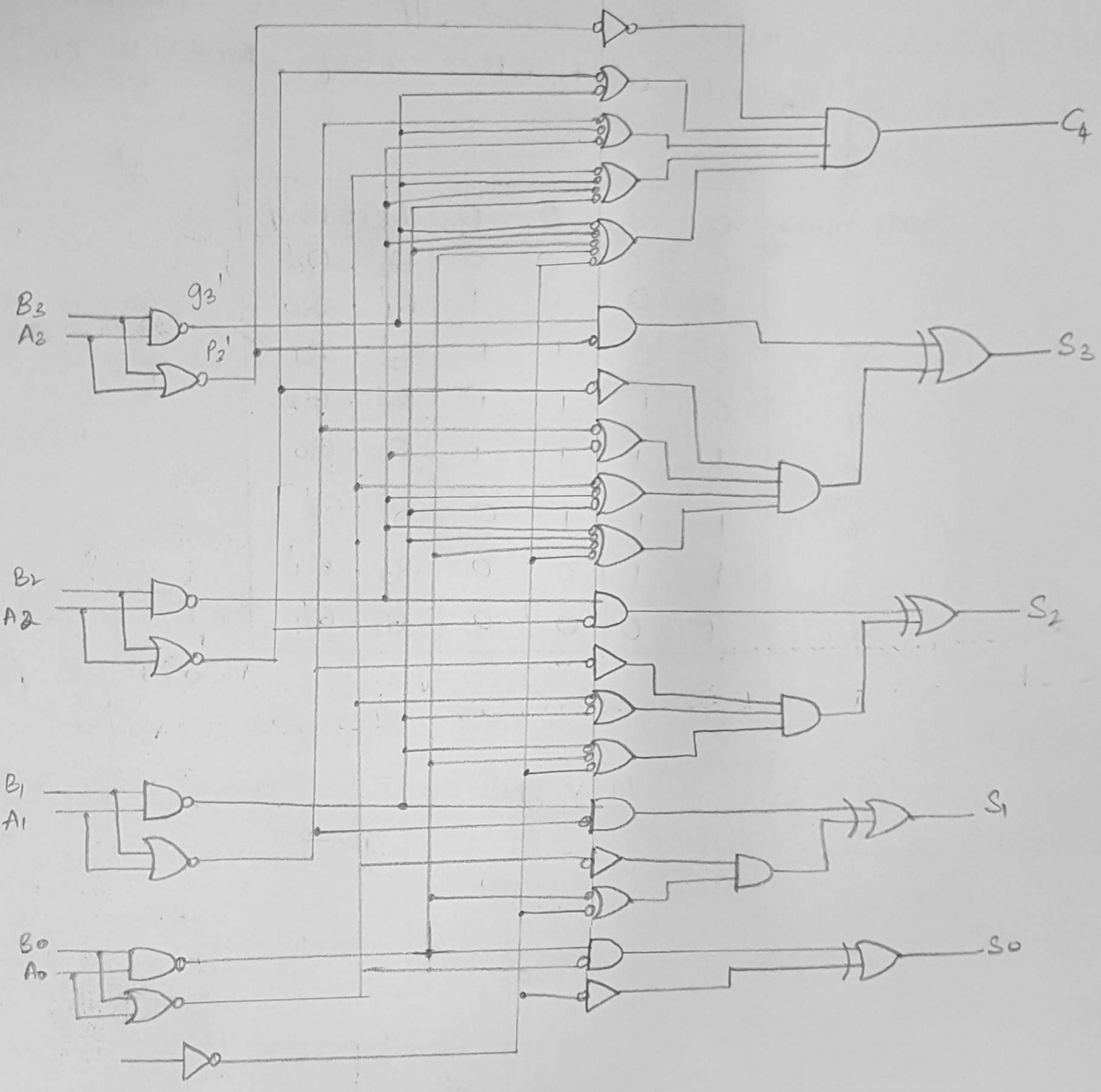
An n-bit shift register with the complement of serial output fedback into the serial i/p is a counter with 2n states and is called a twisted ring, moebius or Johnson counter.

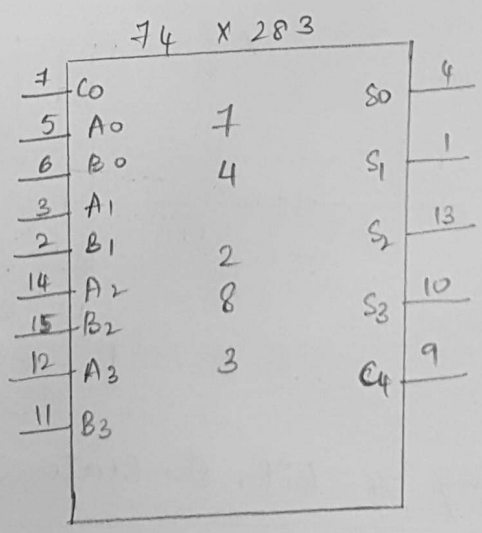
State name	Q_3	Q_2	Q_1	Q_0	Decoding
S_1	0	0	0	0	$Q_3' \cdot Q_0'$
S_2	0	0	0	1	$Q_1' \cdot Q_0$
S_3	0	0	1	1	$Q_2' \cdot Q_1$
S_4	0	1	1	1	$Q_2' \cdot Q_3$
S_5	1	1	1	1	$Q_3 \cdot Q_0$
S_6	1	1	1	0	$Q_1 \cdot Q_0'$
S_7	1	1	0	0	$Q_3 \cdot Q_1'$
S_8	1	0	0	0	$Q_3 \cdot Q_2'$



Self-correcting 4 bit, 8-State Johnson Counter

③ Carry look ahead adder and MSI adder logic diagram & IC.

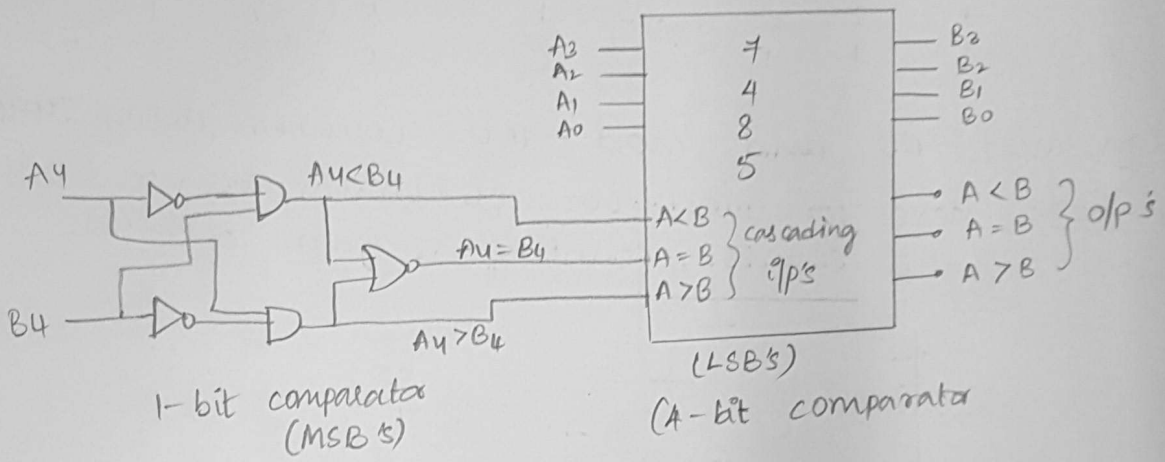




④ Design a 5-bit comparator using IC 7485.

$A = A_4\ A_3\ A_2\ A_1\ A_0$ $\quad$ $B = B_4\ B_3\ B_2\ B_1\ B_0$

Comparing starts from MSB's of given i/p number. If MSB's are same, we compare next significant bits. It can be designed using 1-bit and a 4 bit comparator.

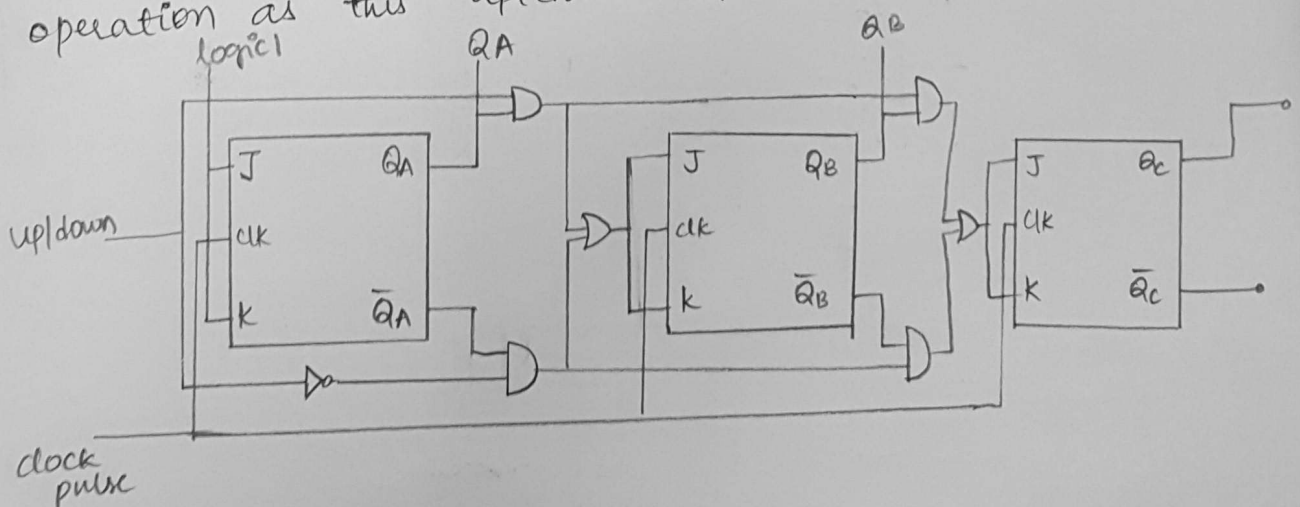


⑤ Design a 3-bit up/down counter and represent its IC.

3-bit up/down counter can be represented with 555 timer and using JK flipflop.

→ This ckt using JK flipflop configured to operate as toggle (or) T-FF giving a count of zero(000) to 111 back to 000 again.

→ An additional i/p determines the direction of count, either up (or) down the timing diag gives an example of counter operation as this up/down i/p changes state.



Truth table

Count up Mode

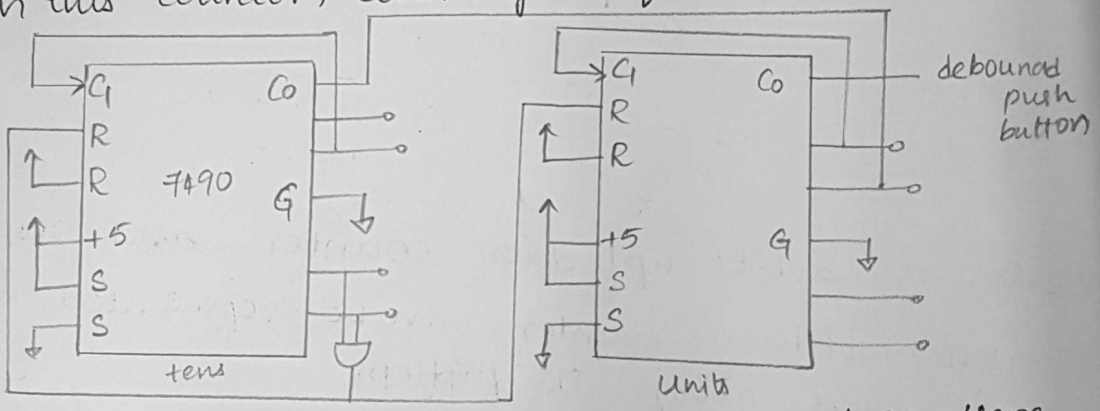
State	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Count down mode

State	Q_C	Q_B	Q_A
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

(6) Design mod-60 and mod-100 counter using 7490.

Mod-60: Here for, mod-60 BCD counter, we use two 7490 counter. In this counter, counting is from 0 to 59.



Mod-100: For mod-100, counting is from 0 to 99. Here cascading 3 7490 IC's in which Q_d of 1st goes to 14th pin of 2nd and Q_d of 2nd goes to 14th pin of 3rd.