

SEQUENTIAL CIRCUIT ICs

1. Commonly Available 74XX and CMOS 40XX

Series ICs

Device No. TTL DATA.	Device function.
7400.	Quad 2-NAND Gate.
7401.	Quad 2-NAND Gate.
7402.	Quad 2-NOR Gate.
7403	Quad 2-NAND Gate.
7404.	Hex. Inverter.
7405.	Hex. Inverter.
7406, 7.	Hex. Inverter, Hex Buffer.
7408.	Quad 2-AND Gate.
7409.	Quad. 2-AND Gate.
7410, 11	Triple 3-NAND gate, AND gate.
7412.	Triple 3-NAND gates.
7413.	Dual. 4-NAND schmitt Triggers.
7414.	Hex. schmitt Trigger Inverters.
7415	Triple. 3-AND gate.
7416, 17.	Hex. Inverter, Buffer.
7420, 21	Dual. 4-NAND Gate.

7425	Dual. 4-NOR Gate.
7426	Quad. 2-NAND Buffer.
7427	Triple. 3-NOR gate.
7428	Quad. 2-NOR. Buffer.
7430	8-Input NAND Gate.
7432	Quad 2-OR. Gate.
7433	Quad. 2-NOR Buffer.
<u>CMOS</u>	
CD4000	series p.m. configuration.
4510	BCD up/down counter.
4511	BCD. to seven segment Decoder
4514	4-16 line. Decoder.
4516	Binary. up/down counter.
4518	Dual. up counter.
4528	Monostable Multivibrator.
4543	BCD to 7 segment Decoder.
4581	4-bit Arithmetic Logic Unit.

2. RS Flip-flops

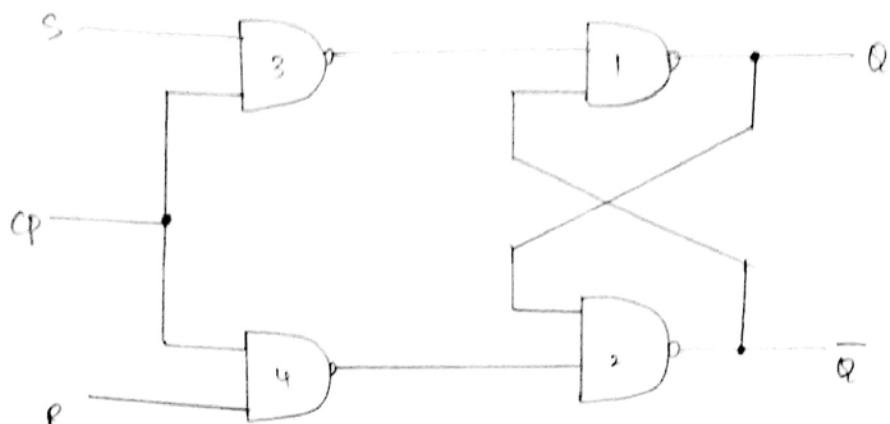


Fig (a): Clocked SR flip-flop.

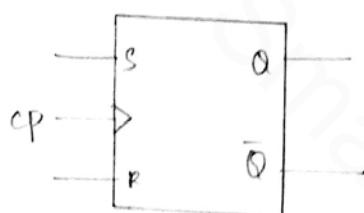


Fig (b): Logic symbol.

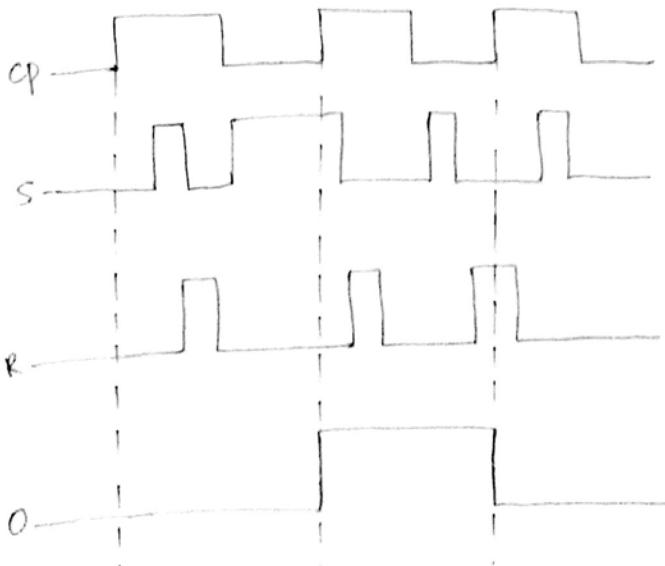


Fig (d): I/p & O/p waveforms for clocked SR flip-flop.

CP	S	R	Q _n	Q _{n+1}	State
↑	0	0	0	0	No change (Nc)
↑	0	0	1	1	
↑	0	1	0	0	
↑	0	1	1	0	Reset
↑	1	0	0	1	
↑	1	0	1	1	Set
↑	1	1	0	X	Indeterminate
↑	1	1	1	X	
0	X	X	0	0	No change (Nc)
0	X	X	1	1	

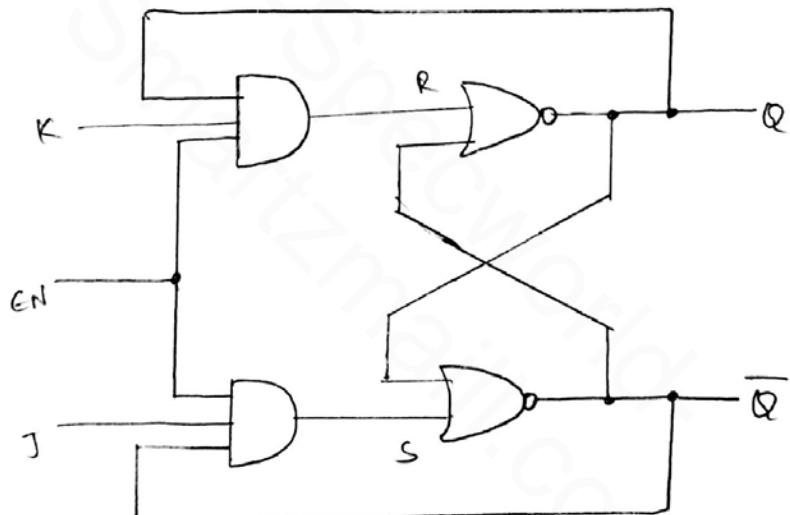
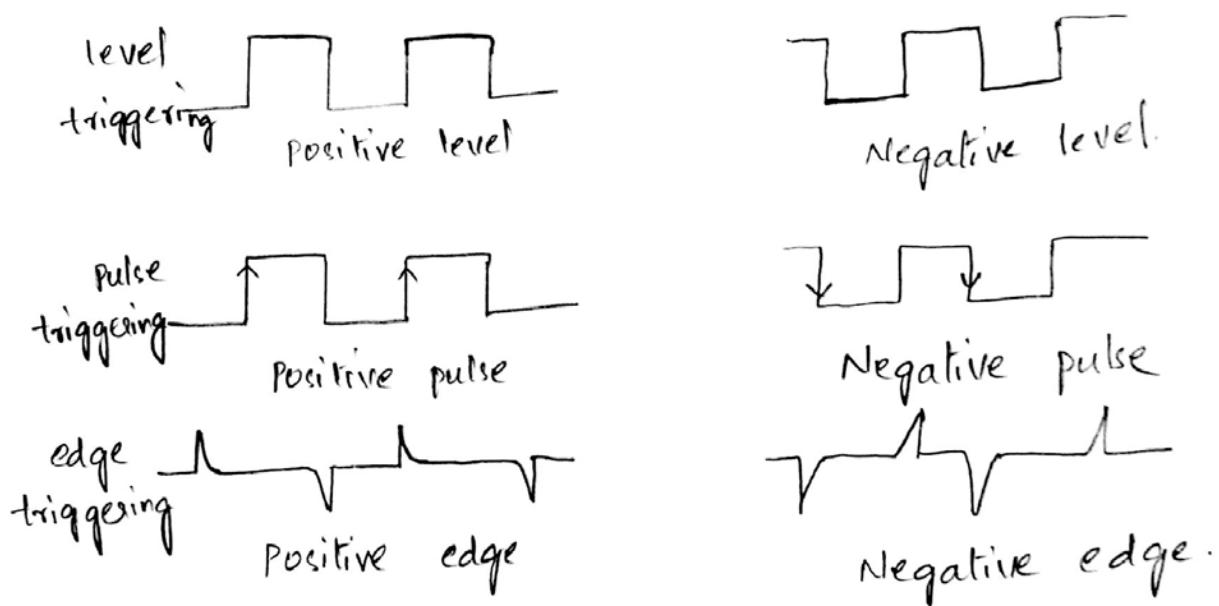
Fig(c): Truth table for clocked SR flip-flop.

	00	01	11	10
0	0	11	0	0
1	11	11	X	X

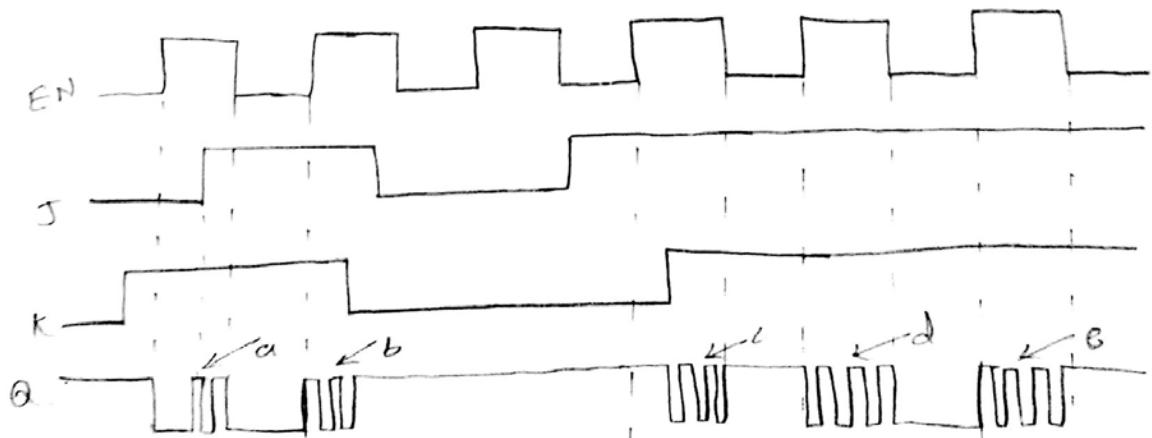
$$\therefore Q_{n+1} = S + \bar{R}Q_n$$

fig (e).

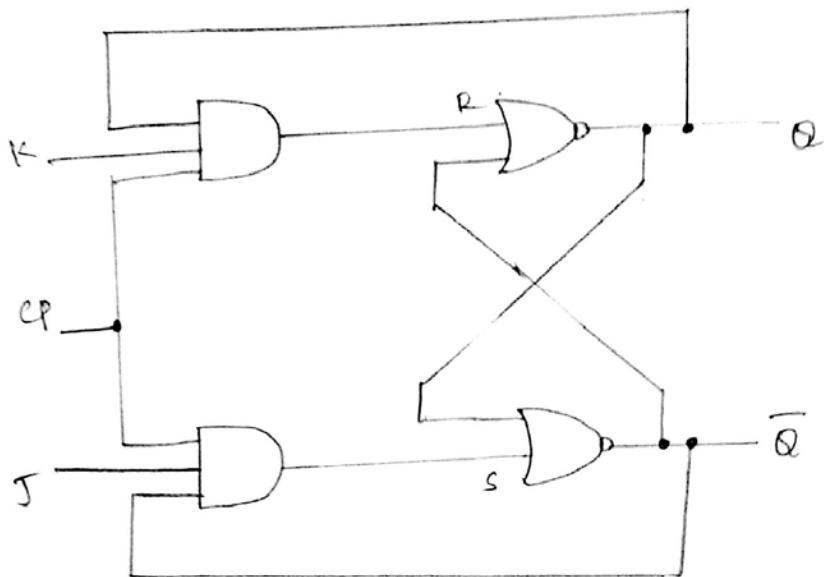
3. JK Flip-Flop



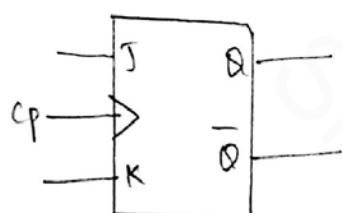
(a) JK latch.



Input and output waveforms for clocked JK flip-flop



clocked JK flip-flop

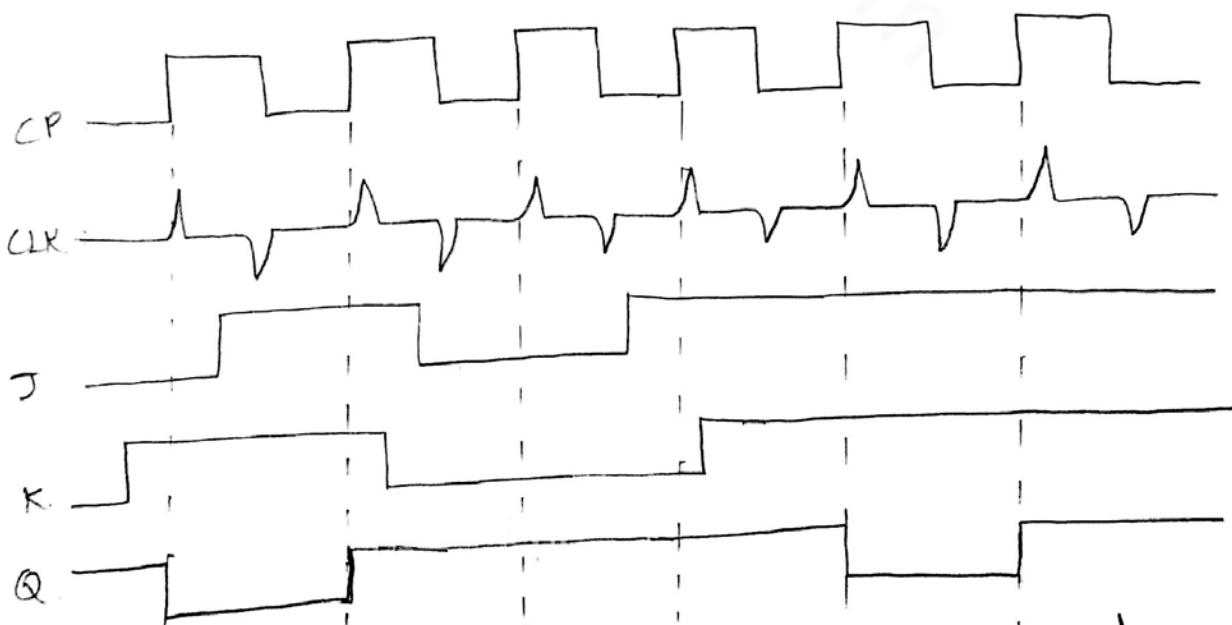


logic symbol.

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0

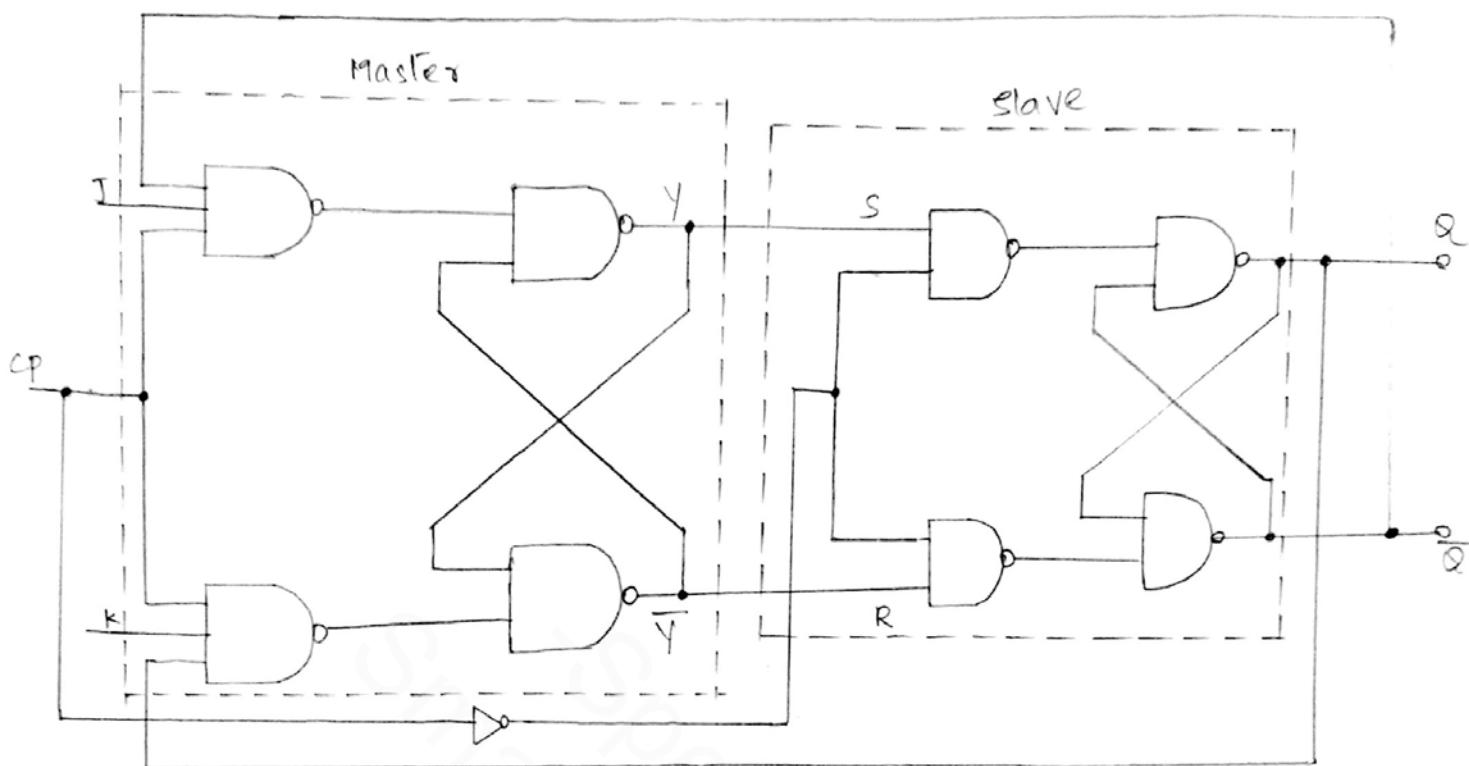
≡

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

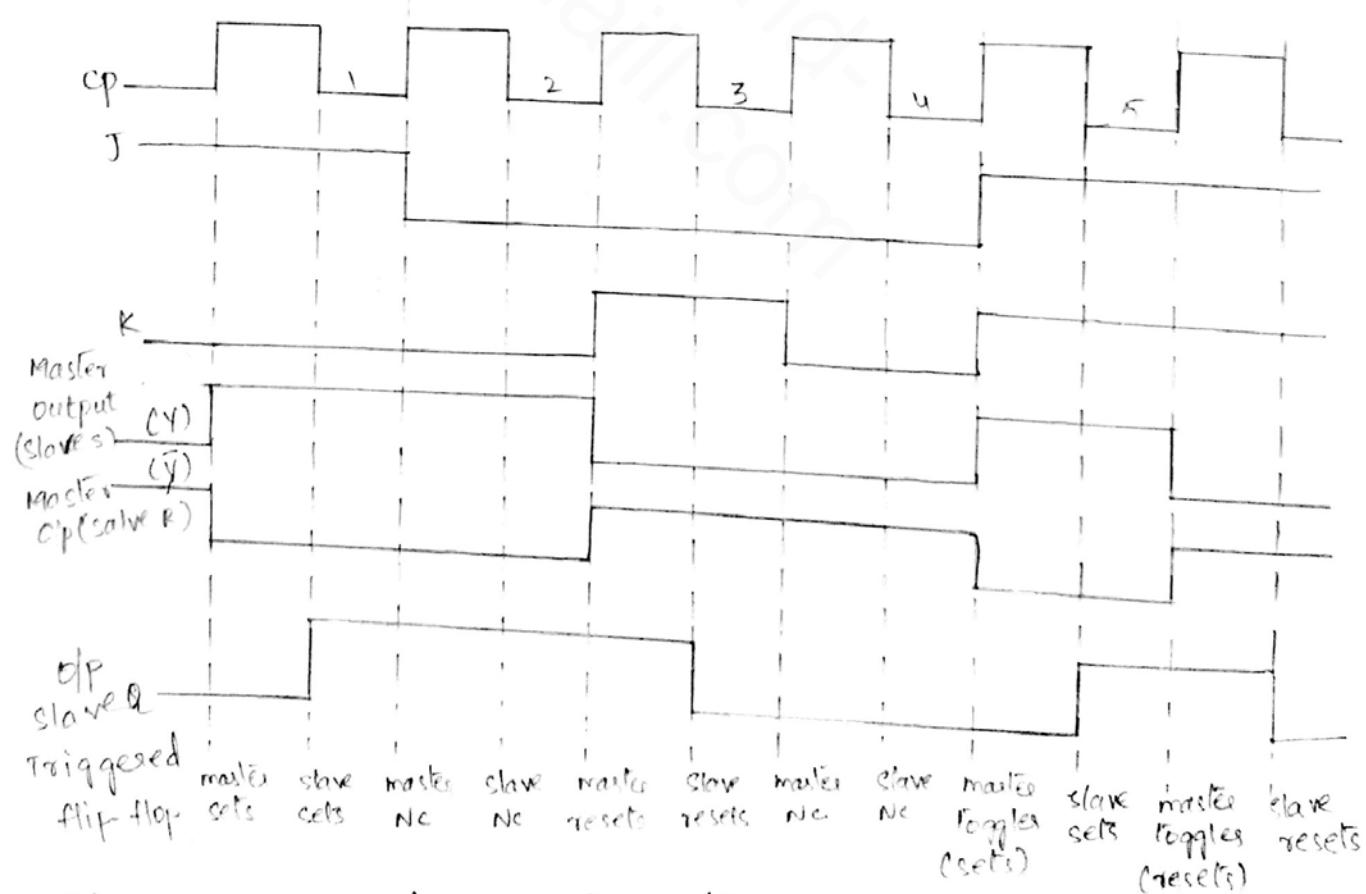
Truth Table

Input & output waveforms for the edge triggered JK flip-flop.

4. JK Master-Slave Flip-Flop



(*) Master - slave JK flip - flop.



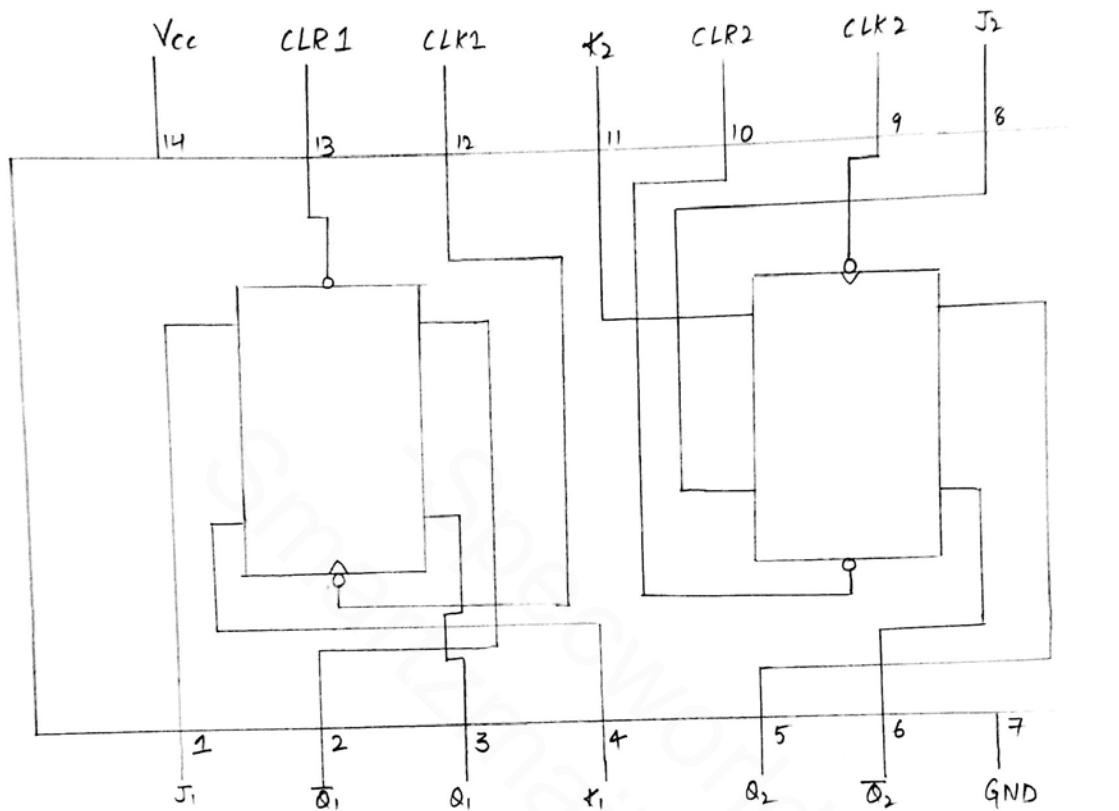
(*) IIP & OIP waveforms of master - slave JK flip-flop.

→ Truth table for master-slave JK flip-flop:

S _P	Q _n	J	K	Y	Q _{n+1}
	0	0	0	0	Nc
	0	0	0	Nc	0
	0	0	1	0	Nc
	0	0	1	Nc	0
	0	1	0	1	Nc
	0	1	0	Nc	1
	0	1	1	1	Nc
	0	1	1	Nc	1
	1	0	0	1	Nc
	1	0	0	Nc	1
	1	0	1	0	Nc
	1	0	1	Nc	0
	1	1	0	1	Nc
	1	1	0	Nc	1
	1	1	1	0	Nc
	1	1	1	Nc	0

Dual Negative - Edge- Triggered Master-slave J-K Flip-flops with clear, and complementary outputs:

Connection Diagram:



Truth Table :

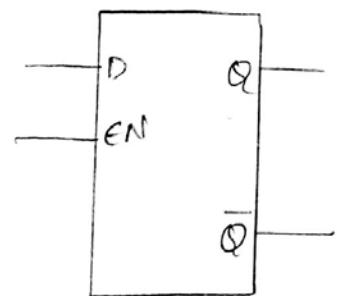
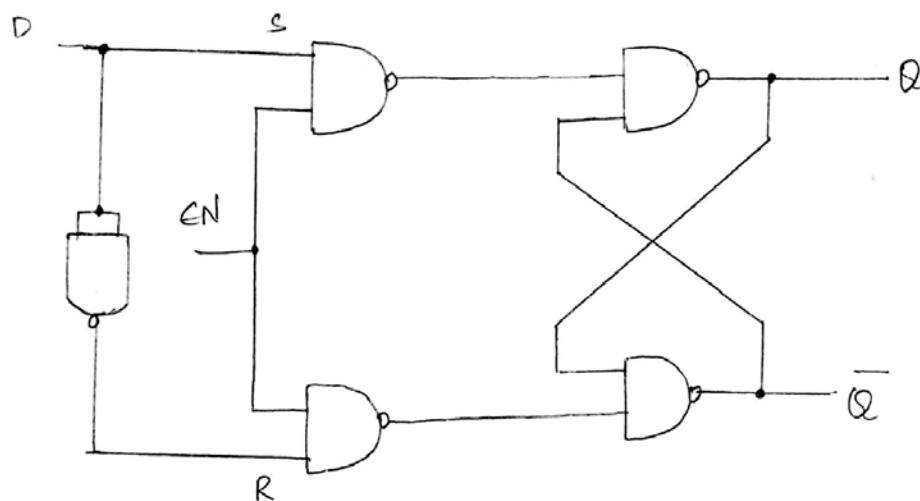
Inputs				Outputs	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	Toggle
H	H	X	X	Q_0	\bar{Q}_0

H = High Logic Level ; X = Either low (or) high logic level

L = Low logic level ; ↓ = Negative going-edge of pulse.

5. D and T Type Flip-Flops and their Conversions

D flip-flop



b) logic symbol.

a) D latch

EN	D	Q _n	Q _{n+1}	state
1	0	X	0	Reset
1	1	X	1	Set
0	X	X	Q _n	No change(N)

c) Truth table for D latch.

EN \ D _n	00	01	11	10
0	Q _n	Q _n	Q _n	Q _n
1	0	0	1	1

$$Q_{n+1} = EN \cdot D + \bar{EN} \cdot Q_n$$

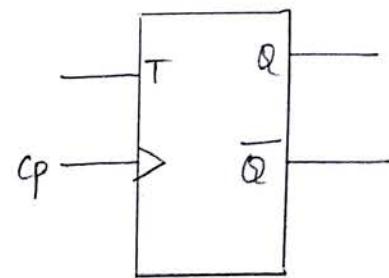
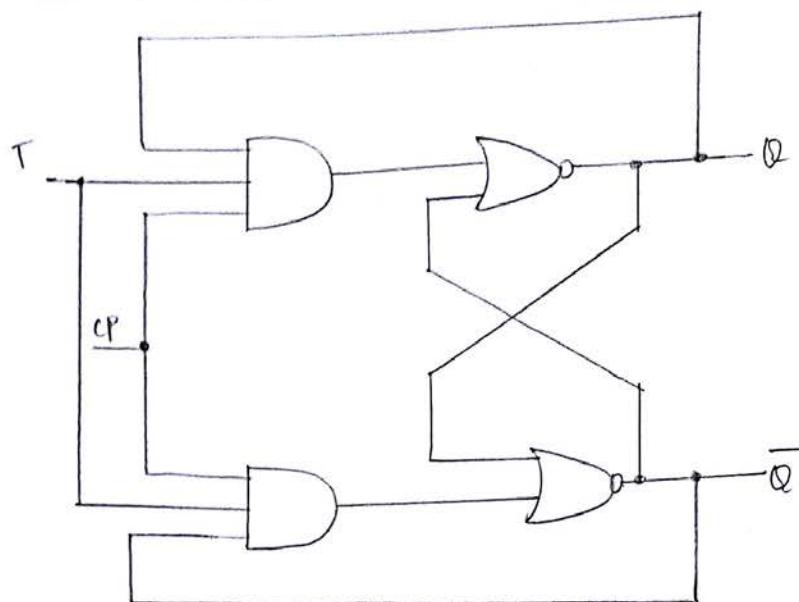
d) characteristic eq'n.

D	Q _{n+1}
0	0
1	1

e) D truth table

Q _n	Q _{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

f) D excitation table.

T flip-flop:-

a) clocked T flip-flop

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

c) logic symbol

T	Q_{n+1}
0	Q_n
1	\bar{Q}_n

d) truth table

Q_n	T	0	1
0	0	0	1
1	1	1	0

$$Q_{n+1} = T \bar{Q}_n + \bar{T} Q_n$$

e) characteristic eq'n.

conversions:-1) SR flip-flop \rightarrow D flip-flop:-

input	present state	next state	flip flop flip's	
D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

a) excitation table.

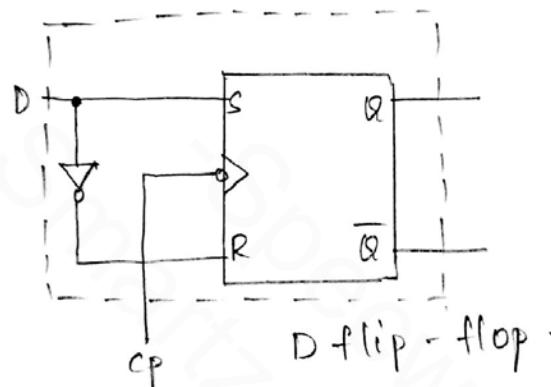
K-map simplification:-

		for S	
		0	1
D	0	0	0
1	1	X	

$S = D$

		for R	
		0	1
D	0	X	1
1	0	0	

$R = \overline{D}$

fig (b)logic diagram:-fig (c) : SR \rightarrow D2) SR flip-flop \rightarrow JK flip-flop:-

flip-flop's		present state	next state	flip-flop's	
J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

fig (a) excitation table.

for S

		Q _n			
		00	01	11	10
J		0	X	0	0
1	X	0	1	1	1

$$S = J \bar{Q}_n$$

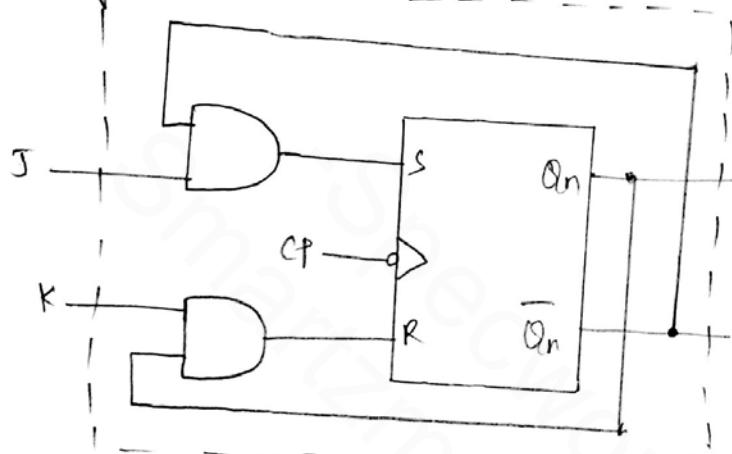
for R.

		Q _n			
		00	01	11	10
J		0	X	0	1
1	0	0	1	1	0

$$R = K \bar{Q}_n$$

fig : (b)

logic diagram:



JK flip-flop.

fig (c).

3) SR flip-flop to T flip-flop

flip-flop's	present state	next state	flip-flop flip-flop's	
T	Q _n	Q _{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

fig (a) : excitation table.

K-map simplifications:

for S

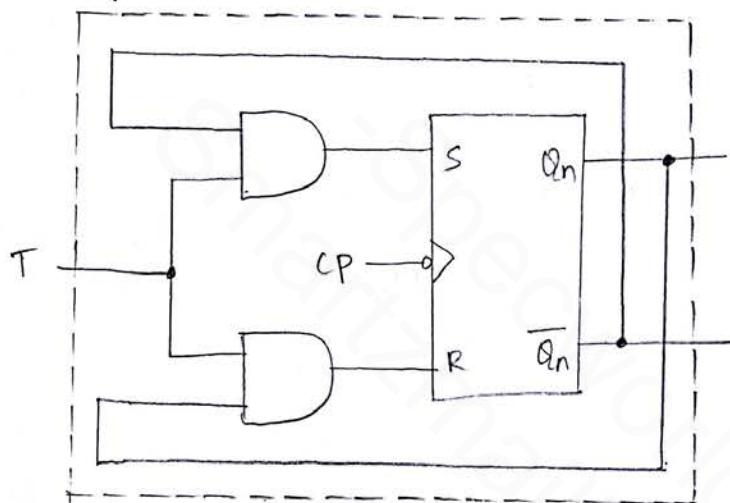
T	Q _n	0	1
0	0	X	
1	1	0	

$$S = T \bar{Q}_n$$

for R

T	Q _n	0	1
0	X	0	
1	0	1	

$$R = T Q_n$$

fig (b):logic diagram.fig (c): SR to Tu) JK flip-flop to T flip-flop

flip	present state	next state	flip-flop i/p's	
T	Q _n	Q _{n+1}	J _A	K _A
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	0

fig (a): excitation table.

K-map simplification:-for J_A

T	Q _n	0	1
0	0	0	X
1	1	1	X?

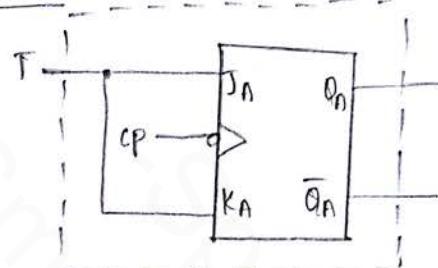
$J_A = T$

for K_A

T	Q _n	0	1
0	0	X	0
1	1	X	1

$K_A = T$

fig : (b)

logic diagram:-

T flip-flop

fig (c) : JK to T

5) JK flip-flop to D flip-flop

ip	present state	next state	flip-flop ip's	
D	Q _n	Q _{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

fig (a) : excitation table.

K-map simplification:-for J

D	Q _n	0	1
0	0	X	
1	1	X	X

$J = D$

for K

D	Q _n	0	1
0	0	X	X
1	1	X	0

$K = \overline{D}$

fig (b)

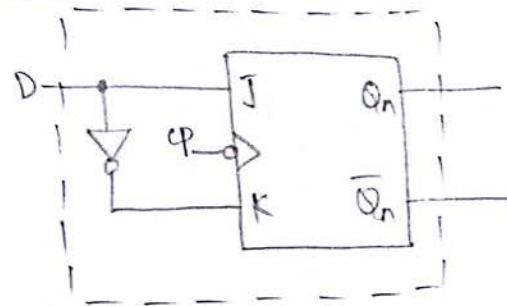
diagram.

fig : (c) : JK to D.

6. D flip-flop To T flip-flop

i/p	present state	Next state	flip-flop i/p
T	Qn	Qn+1	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

fig (a) excitation table.

K-map simplification.

for D

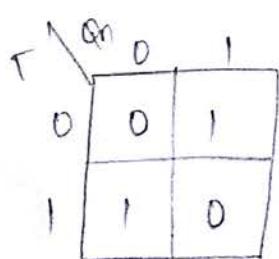
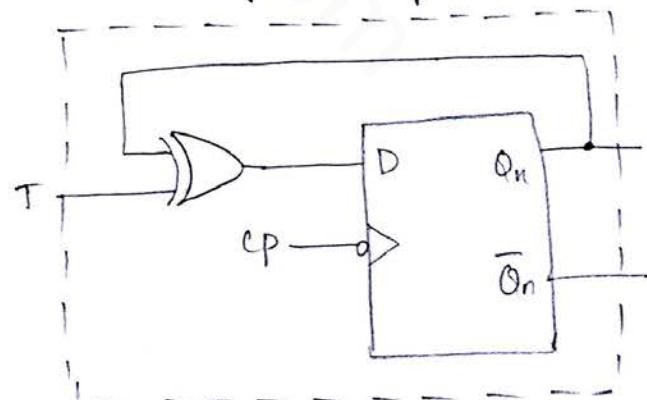
logic diagram

fig (b)

fig (c) D to T

$$\begin{aligned} D &= \overline{T} \overline{Q_n} + T \overline{Q_n} \\ &= T \oplus Q_n \end{aligned}$$

7) T flip-flop to D flip-flop :-

i/p	Present state	Next state	flip-flop i/p
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

fig (a) excitation table:

K-map simplification.

for T

D	Q_n	0	1
0	0	0	1
1	1	1	0

$$T = D \bar{Q}_n + \bar{D} Q_n$$

fig (b).

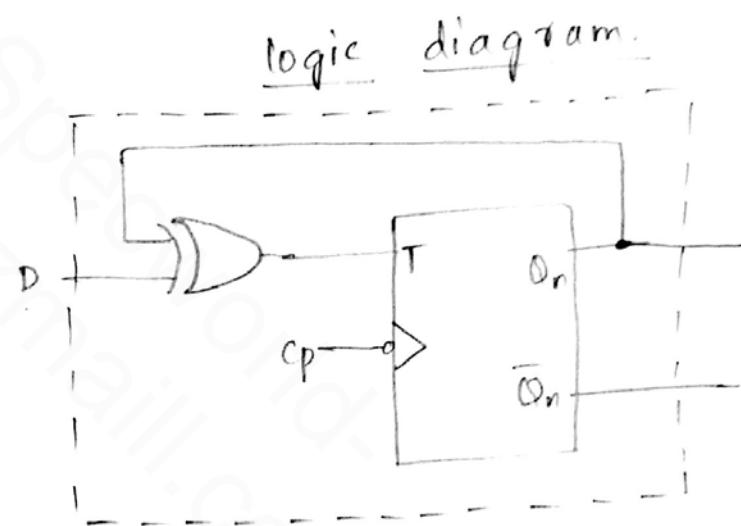
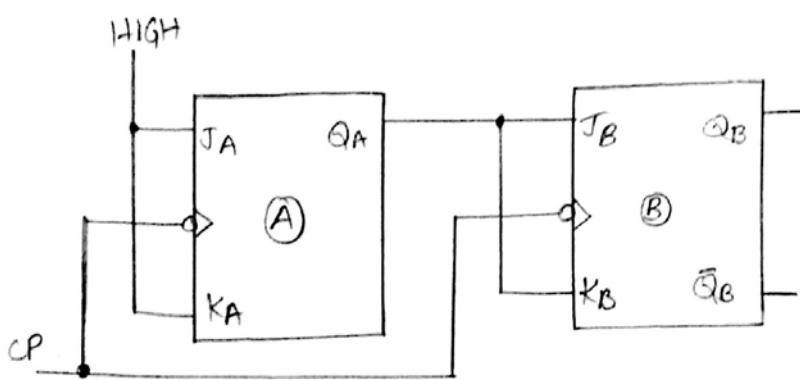


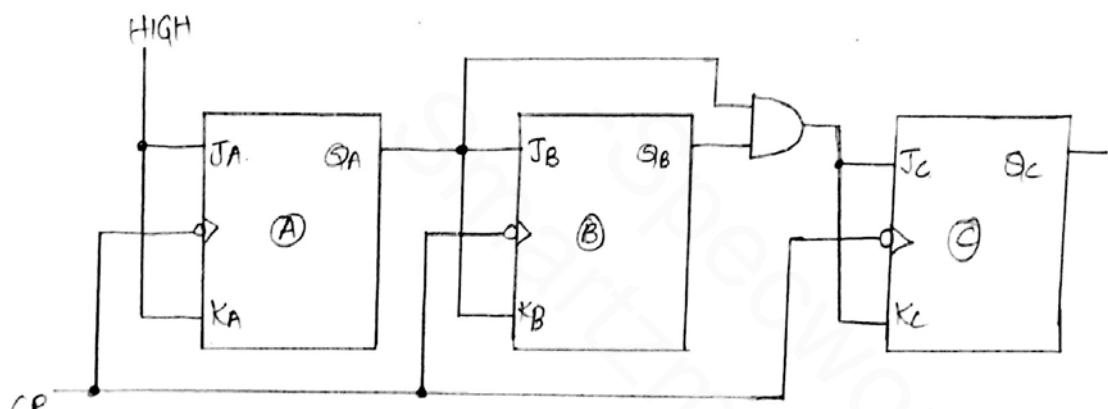
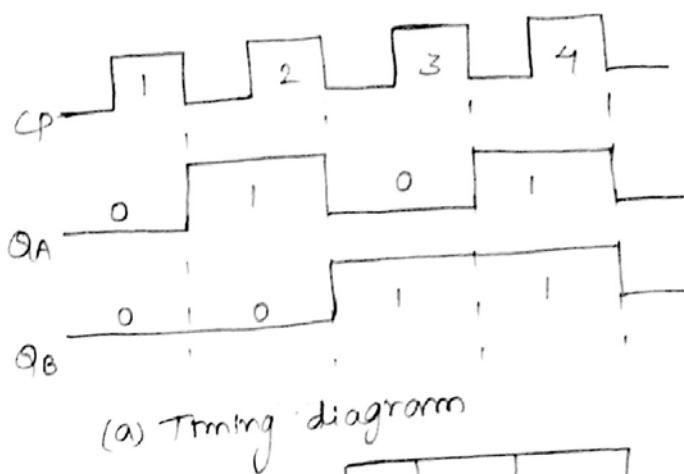
fig (c) T to D.

6. Synchronous and asynchronous Counters

Synchronous up-counters :-



(*) A two-bit synchronous binary counter.

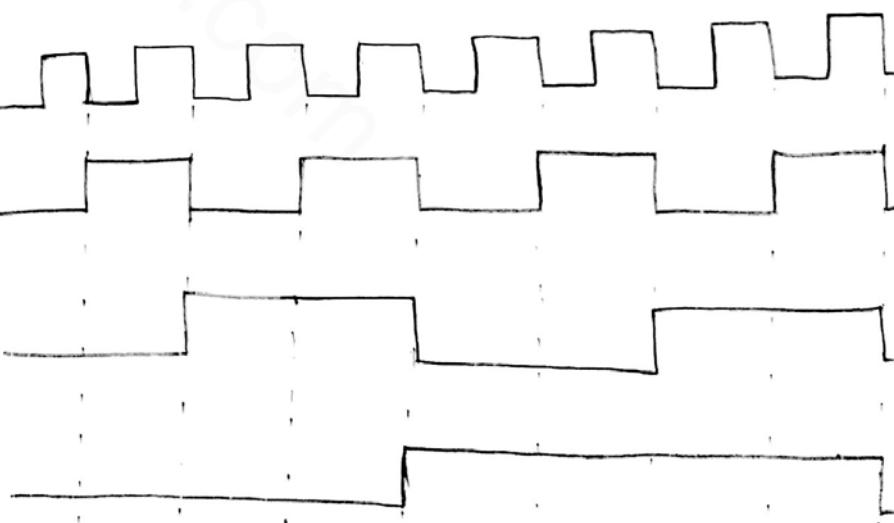


(*) A Three-bit synchronous binary counter

CP	Q _C	Q _A
0	0	0
1	0	1
2	0	0
3	0	1
4	1	0
5	1	1
6	1	0
7	1	1

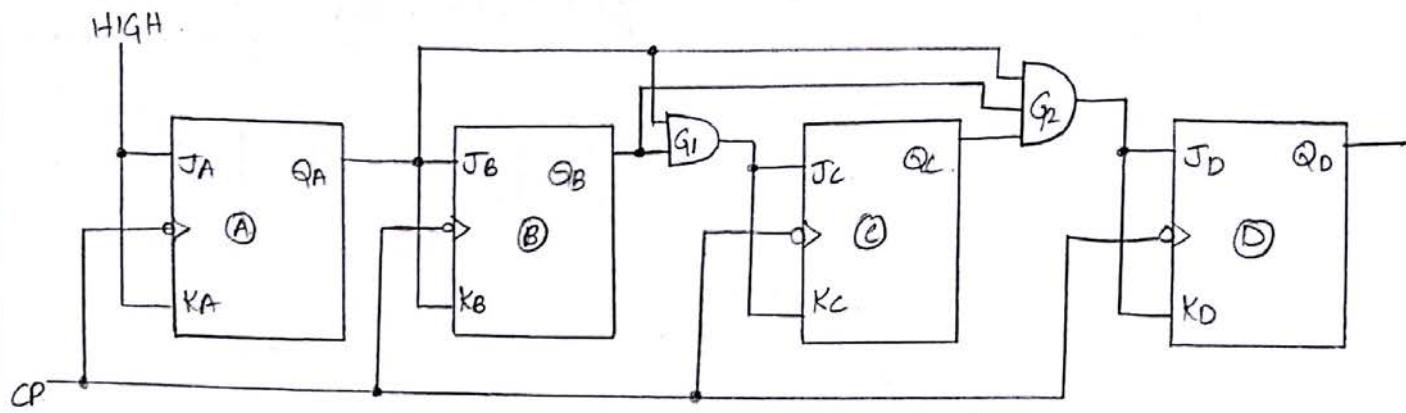
(b) state sequence

CP	Q _C	Q _B	Q _A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

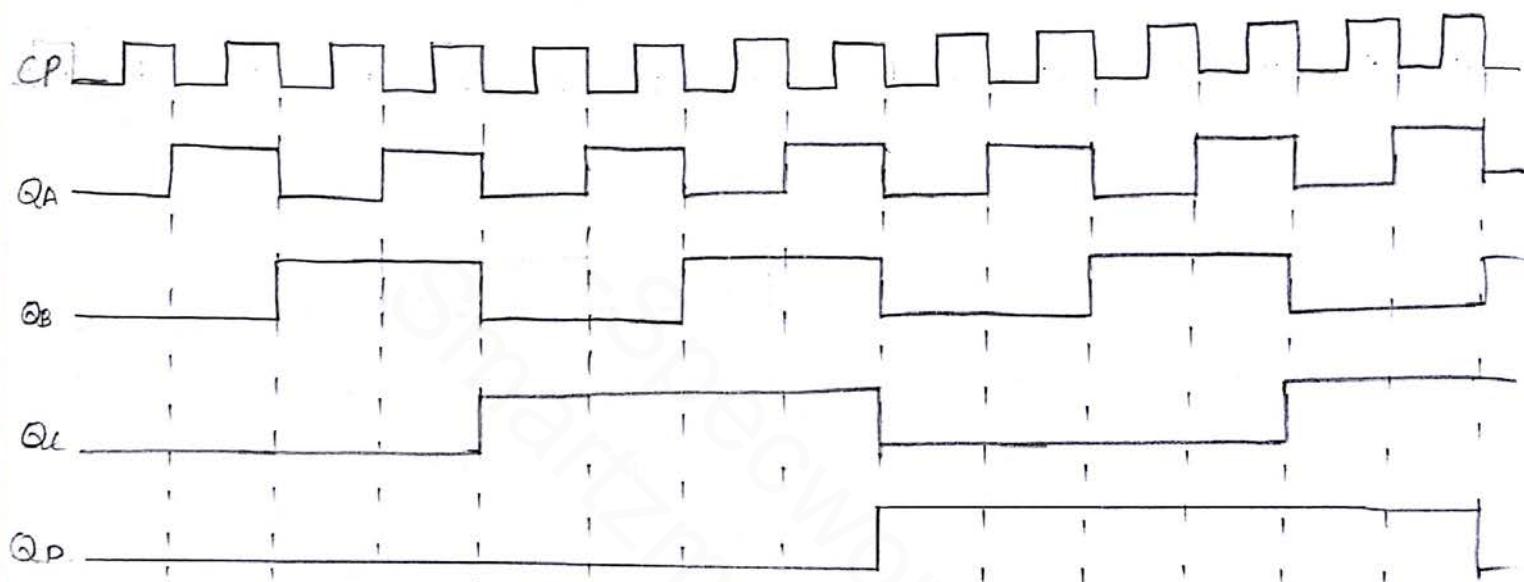


(*) Timing diagram

(*) State sequence

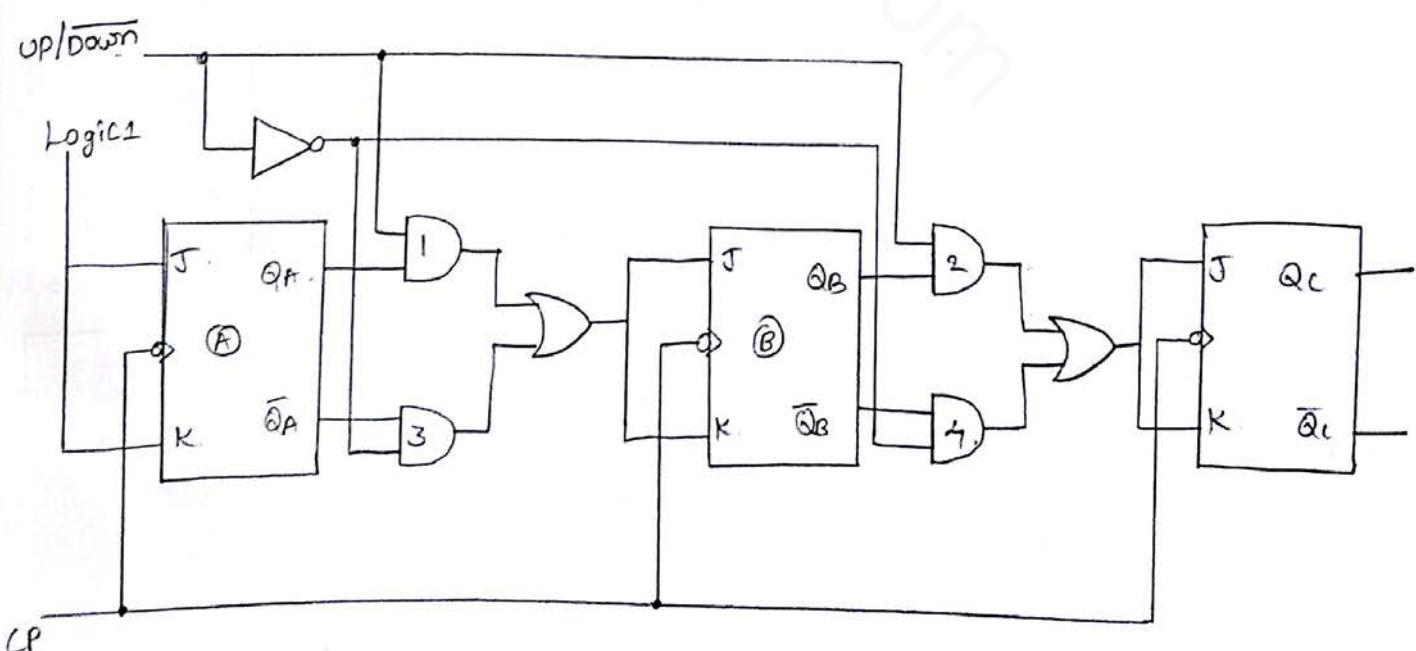


(*) A Four-Bit synchronous Binary Counter.

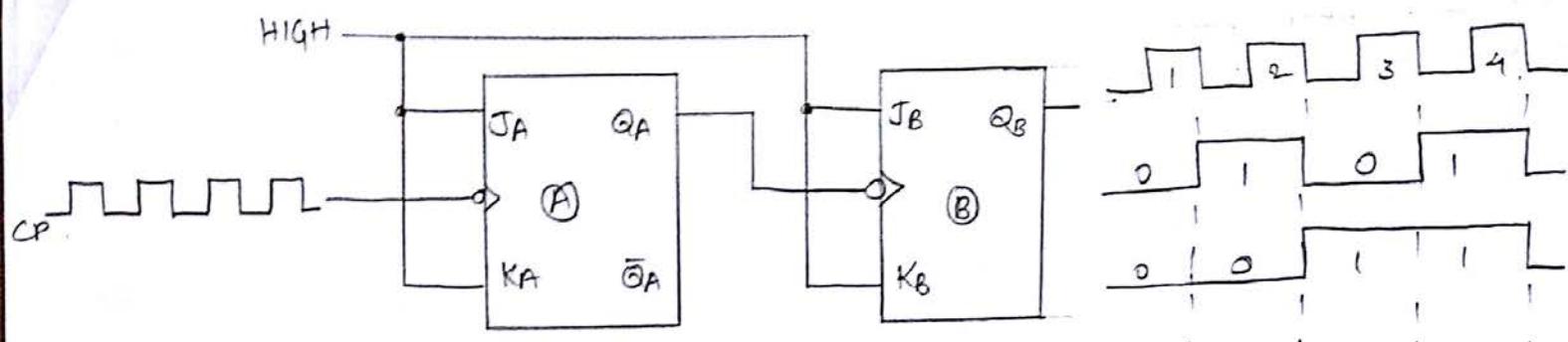


(*) Timing diagram.

Synchronous Down and up/down counters :-



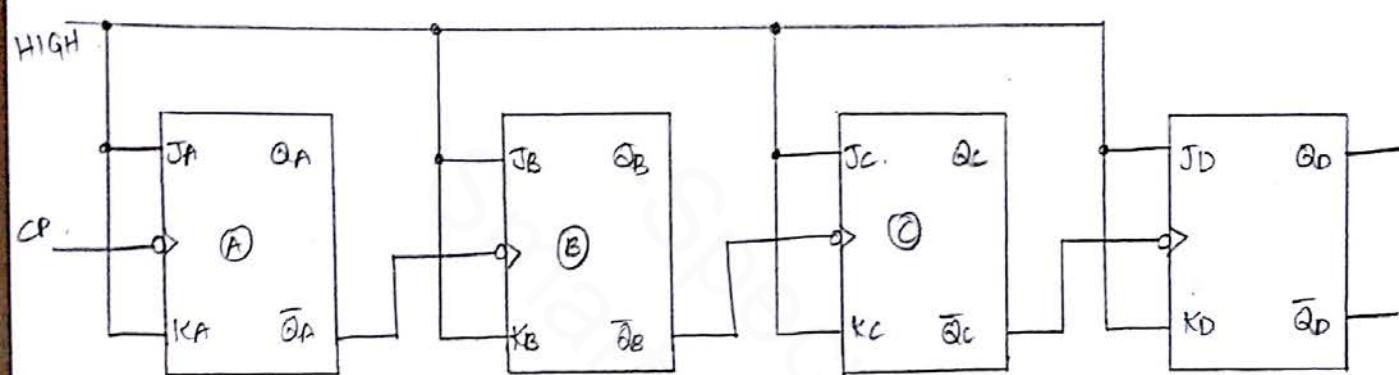
Asynchronous / Ripple up counters:-



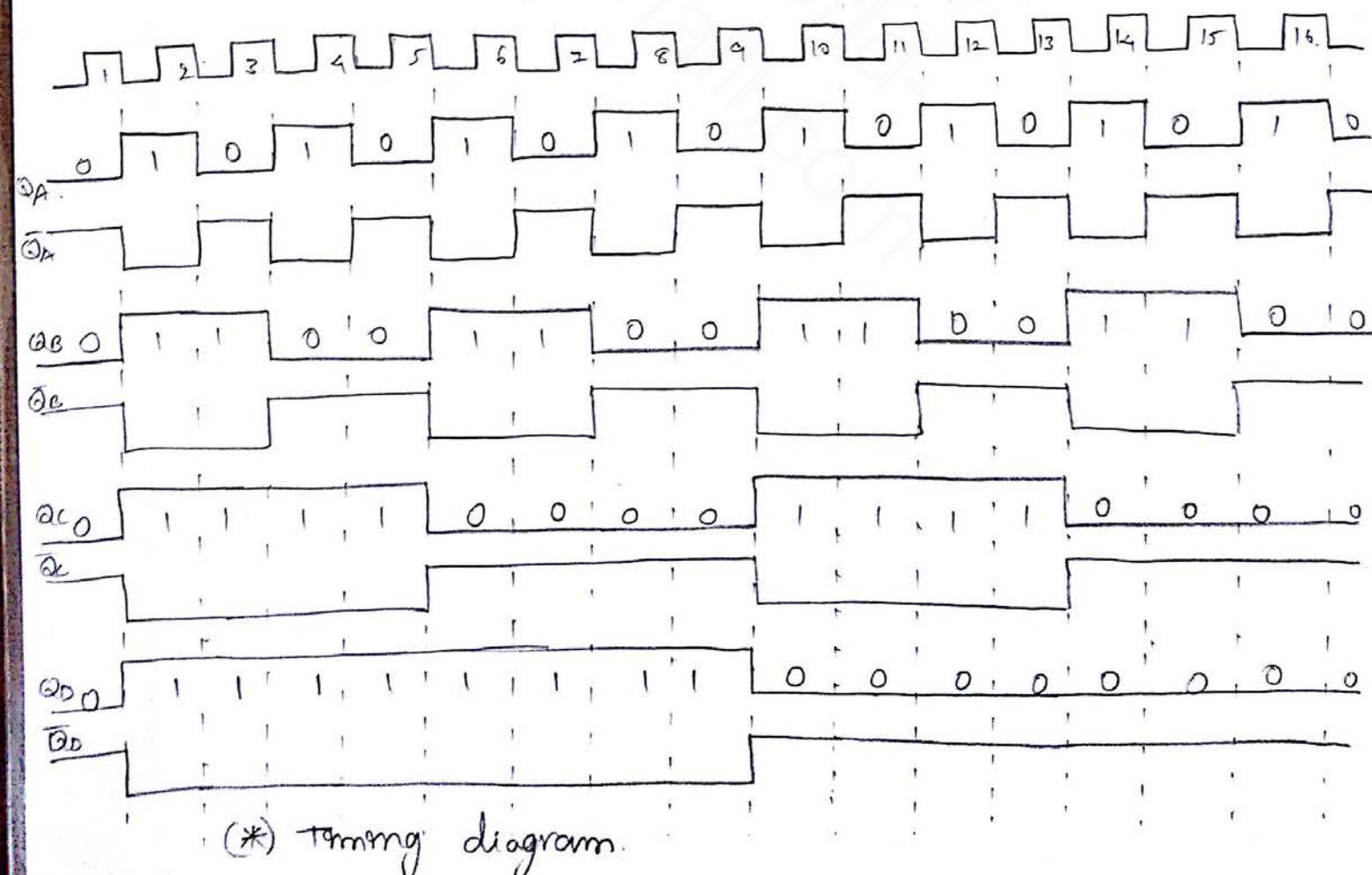
(*) Two-Bit Asynchronous binary counter

(*) Timing diagram

Asynchronous / Ripple down counter:-



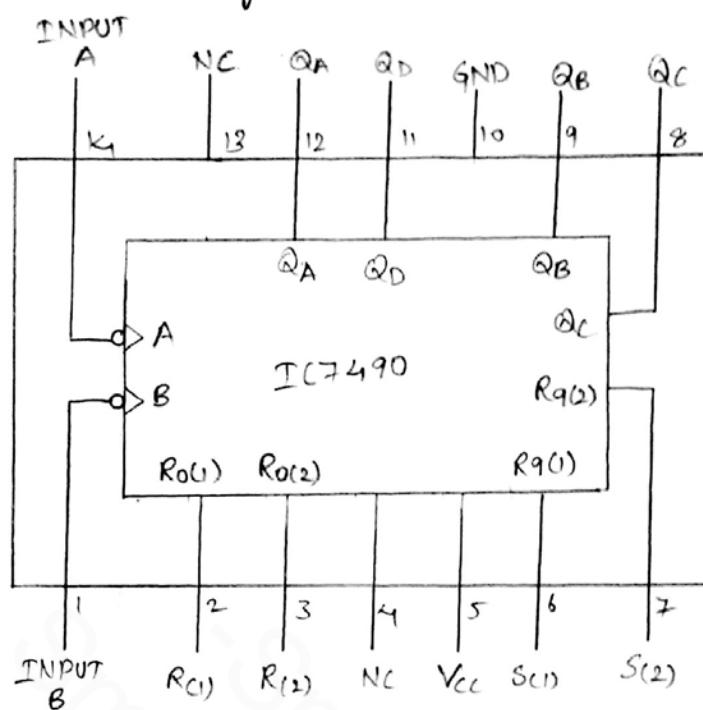
(*) 4-Bit asynchronous down counter.



(*) Timing diagram

7. Decade Counters

IC 7490 (Decade Binary Counter) :-



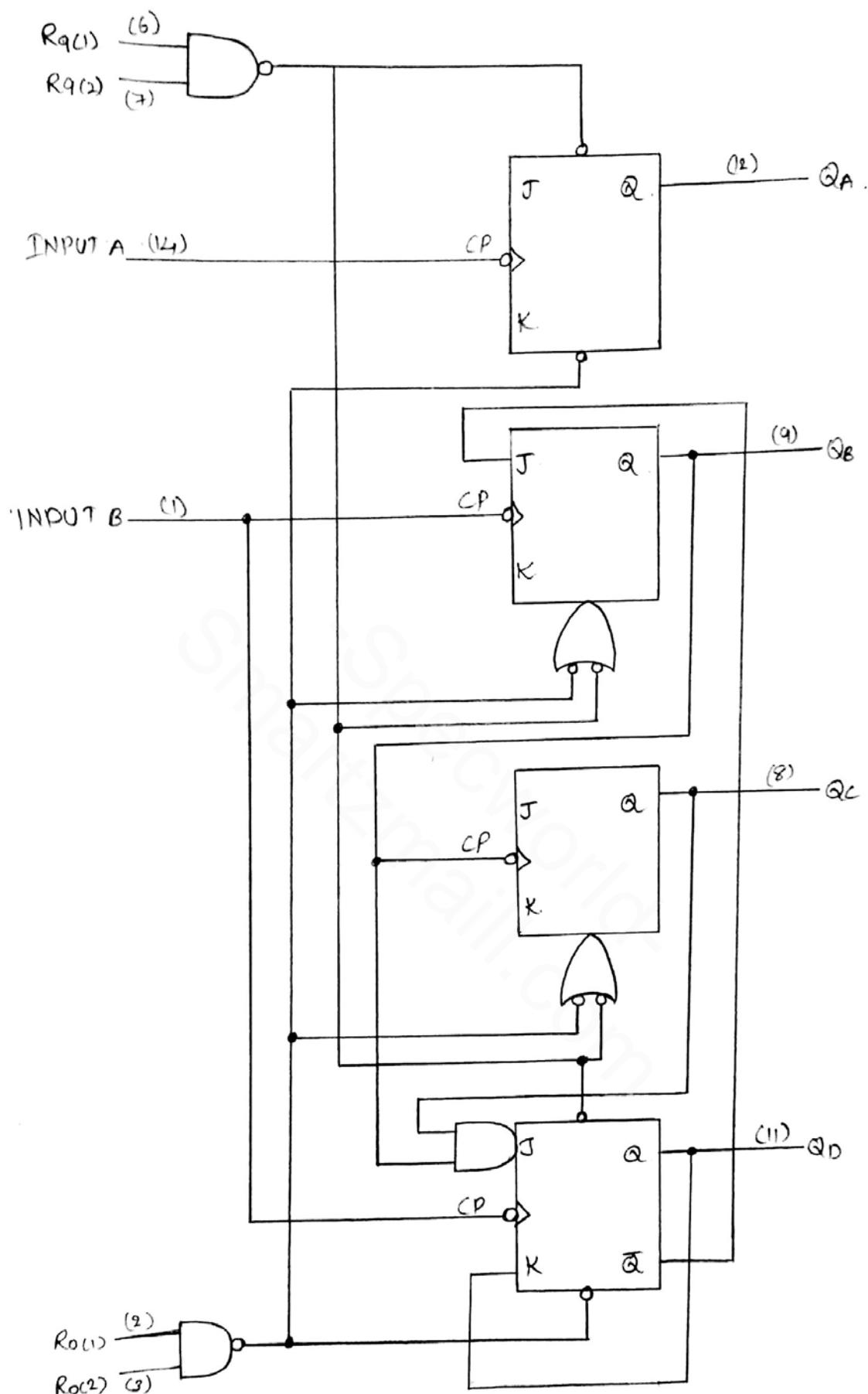
NC = No connection

(*) Connection diagram for 7490

Count	Outputs			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	L
8	H	L	L	L
9	H	L	L	H

fig : (a). BCD count sequences (Note 1)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	L
4	H	H	L	L
5	H	L	L	H
6	H	L	H	L
7	H	L	H	H
8	H	H	L	L
9	H			



Logic diagram for 7490

Reset / INPUTS				Outputs			
$R_{Q(1)}$	$R_{Q(2)}$	$R_{Q(1)}$	$R_{Q(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

Fig: (C) Reset / count function table

H : HIGH Level

L : Low Level

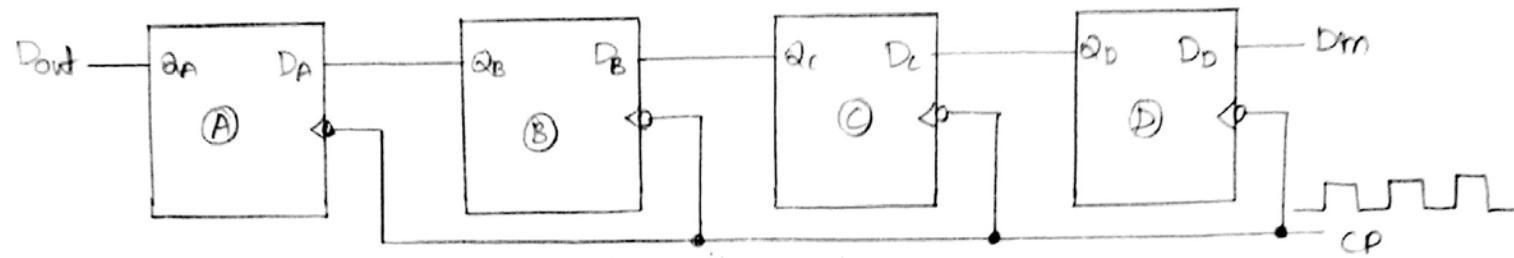
X : Don't Care

Note 1: Output Q_A is connected to input B for BCD count.

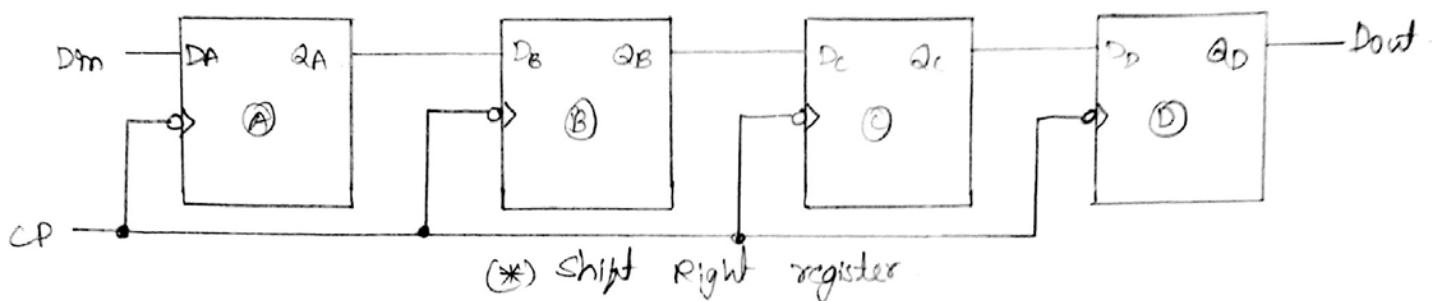
Note 2: Output Q_D is connected to input A for bi-quinary count.

8. Shift Registers and applications.

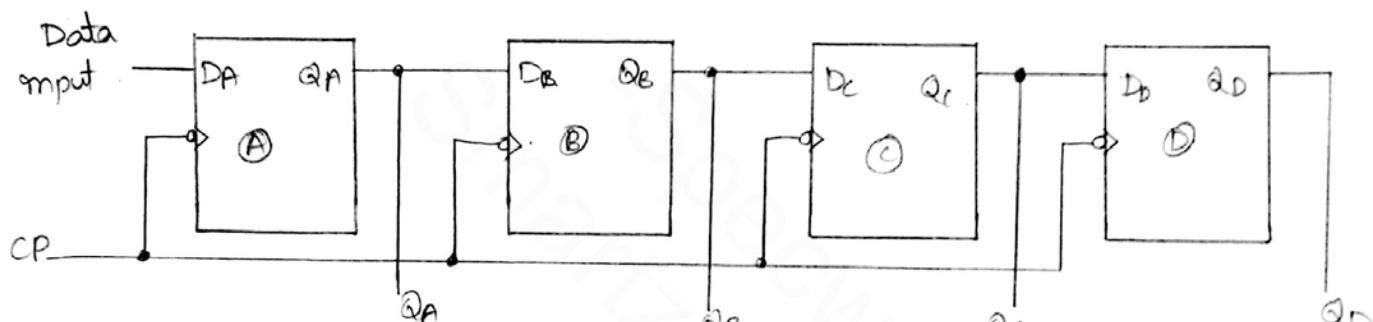
www.jptuworldupdates.org



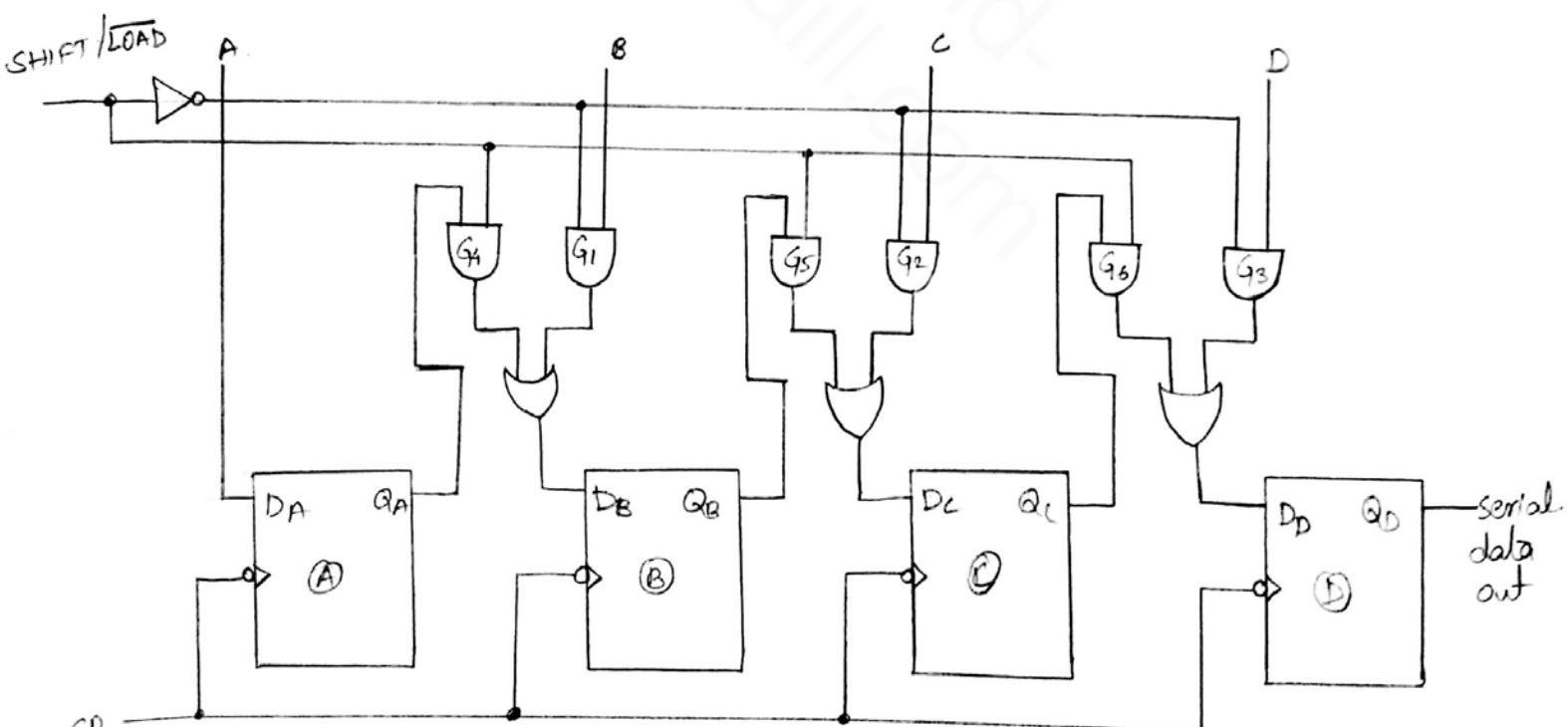
(*) shift left register



(*) shift Right register

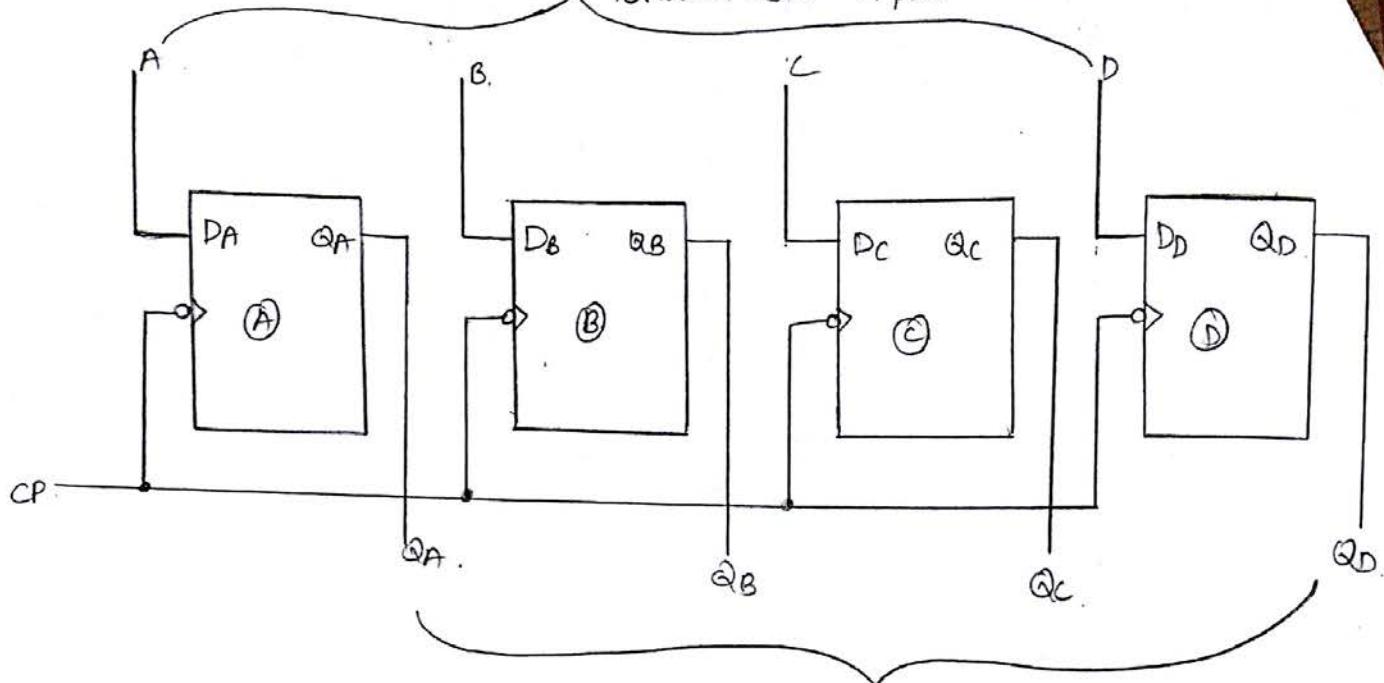


(*) A serial in parallel out shift register



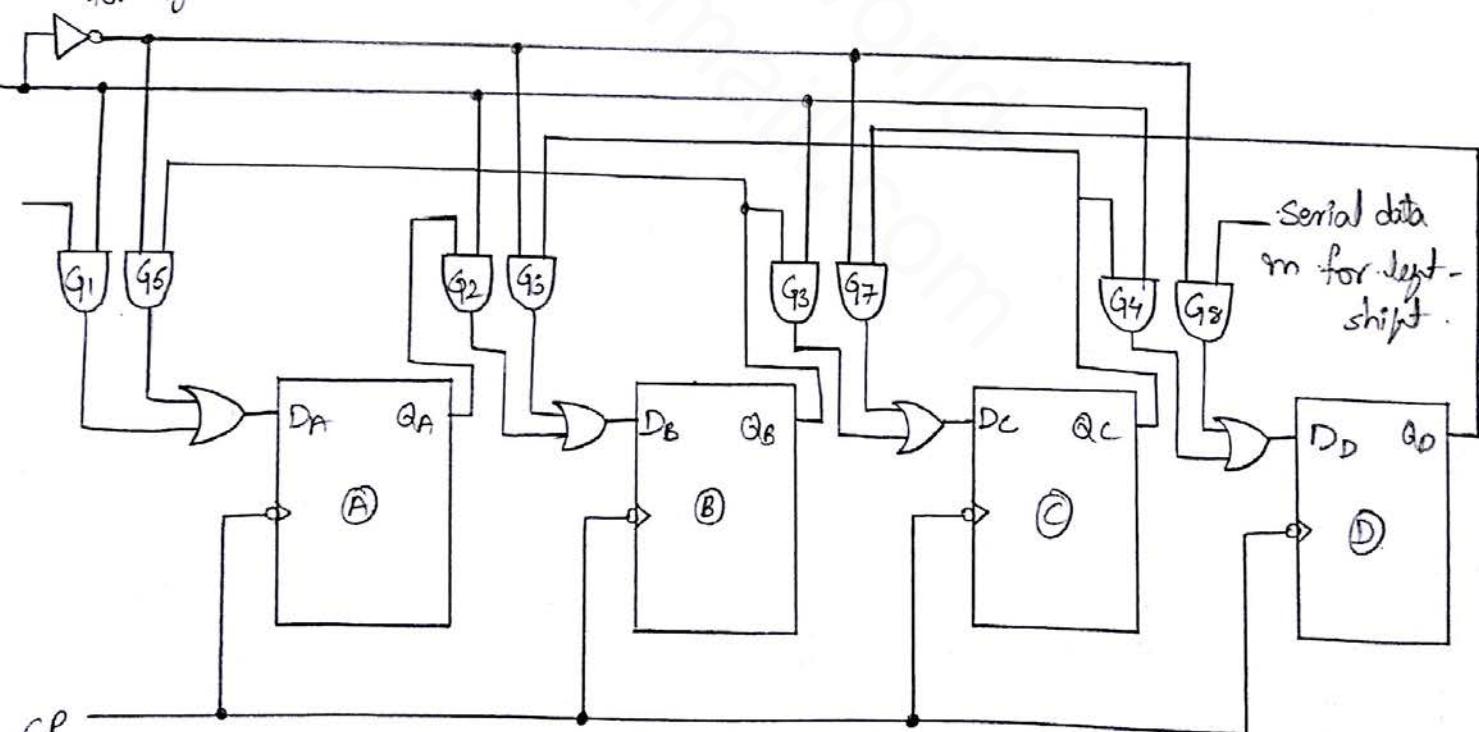
(*) Parallel in serial out shift register

Parallel data inputs

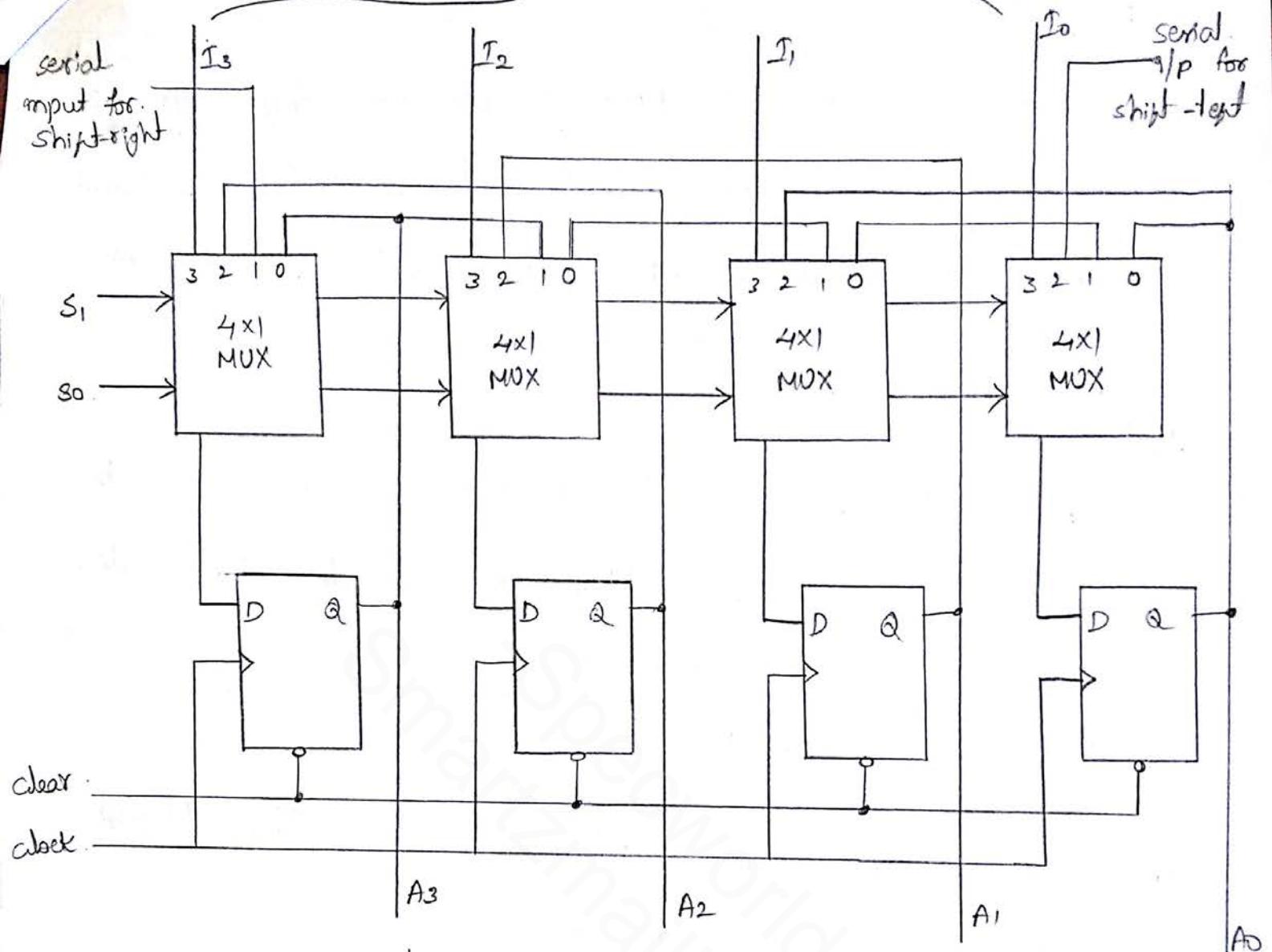


(*) Parallel in parallel out shift register.

RIGHT / LEFT
serial data in
for right-shift



(*) 4-bit bidirectional shift register



(*) Universal shift Register

Parallel output

Mode. Control		Register operation
S_1	S_0	
0	0	No change
0	1	shift-right
1	0	shift-left
1	1	parallel load.

Applications of shift Registers:-

We have seen that primary use of shift register is temporary data storage and bit manipulations. Some of the common applications of shift registers are as discussed below.

Delay Line:-

A serial-in-serial-out (SISO) shift register can be used to introduce time delay at m. digital signals. The time delay can be given as.

$$\Delta t = N \times \frac{1}{f_c}$$

where N is the number of stages (i.e., flip-flops) and f_c is the clock frequency.

Thus, an input pulse train appears at the output delayed by Δt . The amount of delay can be controlled by the clock frequency or by the number of flip-flops in the shift register.

Serial-to-Parallel Converter:-

A serial-in-parallel-out (SIPO) shift register can be used to convert data in the serial form to the parallel form.

Shift Register Counters:-

A shift register can also be used as a counter. A shift register with the serial output connected back to the serial input is called "shift register counter". Because of such a connection, special specified sequences are produced at the output. The most common shift register counters are the ring counter and the Johnson counter.

Pseudo-Random Binary sequence (PRBS) Generator:-

Another important application of shift register is a pseudo-random binary sequence generator. Hence, suitable feedback is used to generate pseudo-random sequence. The term random means the o/p. do not cycle through a normal binary count sequence. The term pseudo here refers to the fact that the sequence is not truly random because it does cycle through all possible combinations once every $2^n - 1$ clock cycles, where 'n' represents the no. of shift register stages. (No. of flip-flops)

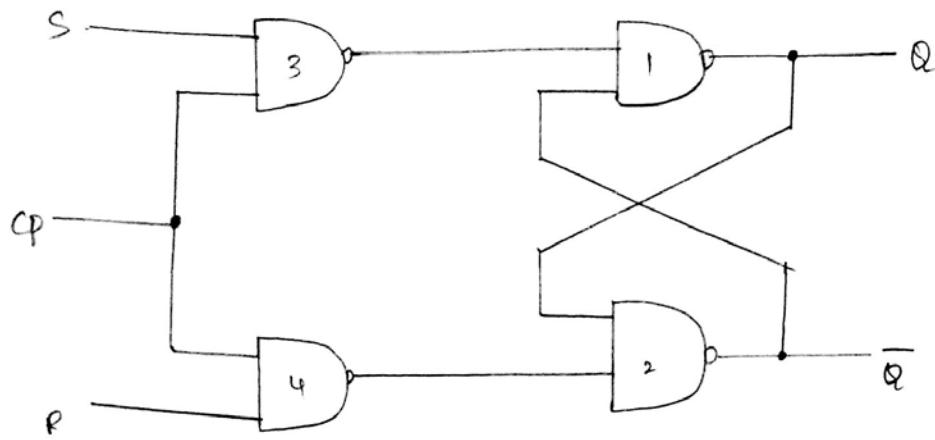


fig (a) :- clocked SR flip-flop.

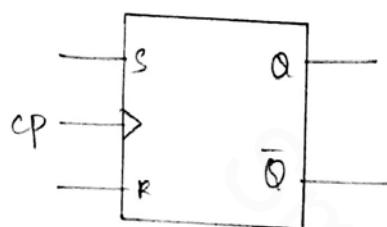


fig (b) - logic symbol.

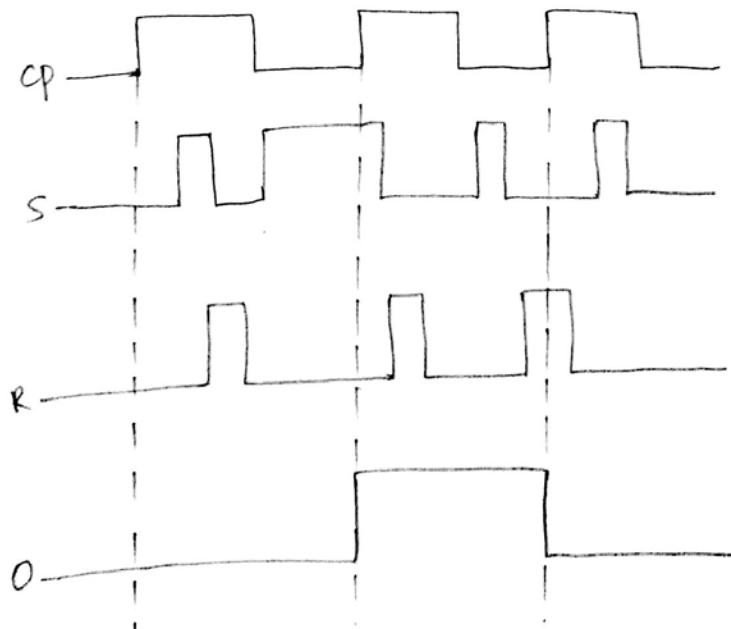


fig (d) - i/p & o/p waveforms for clocked SR flip-flop.

CP	S	R	Q _n	Q _{n+1}	State
↑	0	0	0	0	No change (Nc)
↑	0	0	1	1	
↑	0	1	0	0	
↑	0	1	1	0	Reset
↑	1	0	0	1	
↑	1	0	1	1	
↑	1	1	0	X	indeterminate
↑	1	1	1	X	
0	X	X	0	0	No change (Nc)
0	X	X	1	1	

fig (c) : Truth table for clocked SR flip-flop.