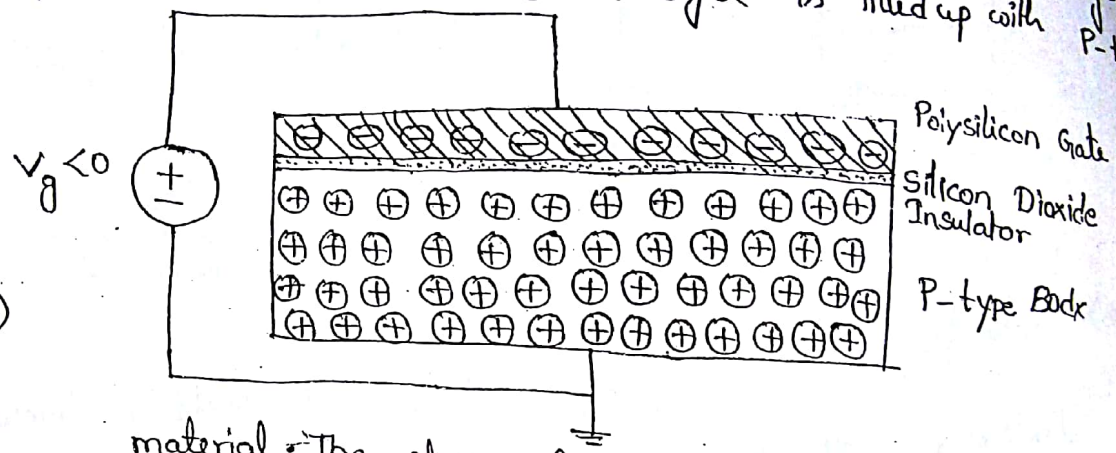
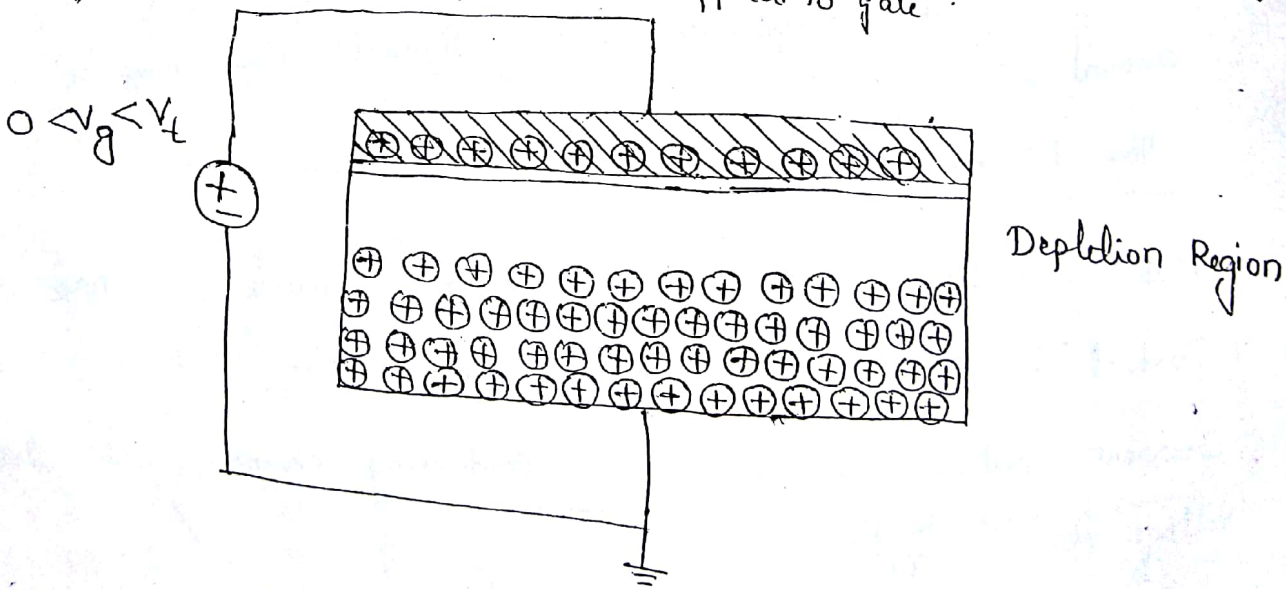
MOS structure

- The top layer is called gate. It is made up of poly. It is a good conductor.
- The middle layer is a very thin insulating film called gate oxide.
- The bottom layer is called body. The below layer doped with silicon. The below layer is filled up with P-type material. The above figure shows P-type body and majority carriers are holes. Generally the body will be grown and voltage will be applied to gate.

a)



b)



- The gate oxide is a good insulator, so almost zero current flows from the gate to the body.

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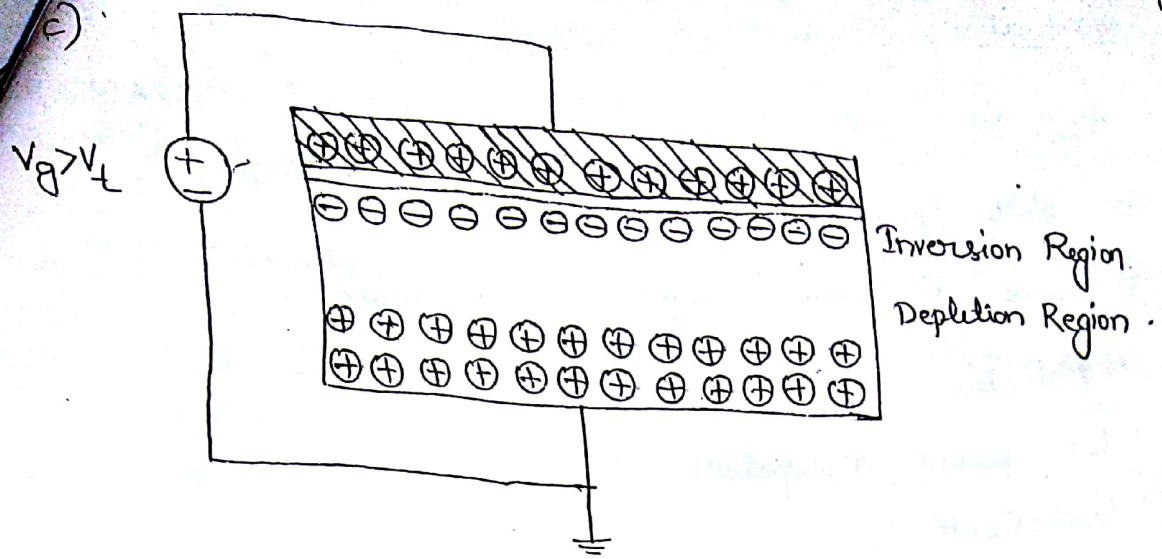
c)



From figure (a) a negative Voltage is applied to the gate, So there is negative charge on the gate. In body positive charge is there because of holes. So beneath the gate negative Voltage Carriers (electrons) and positively charged Carriers (holes) are attracted. This is called <u>accumulation</u>.

From Figure (b) a low positive voltage is applied to the gate, So positive charge will be there on the gate. The holes in the body are repelled from the region directly beneath the gate, we can call this area as depletion region forming below the gate.

From (c) apply higher potential greater than threshold Voltage V_t is applied. So more positive charge is on the gate. So holes are repelled further and a small number of free electrons in the body are attracted to the region beneath the gate. This [illegible]

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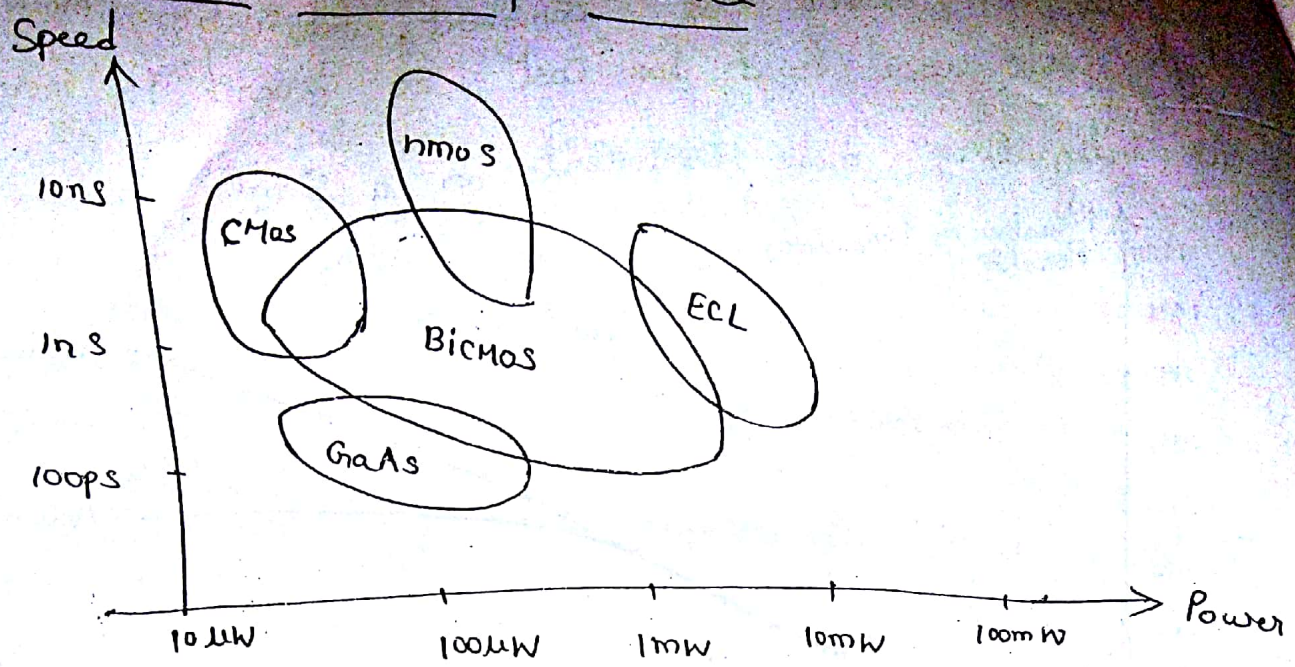
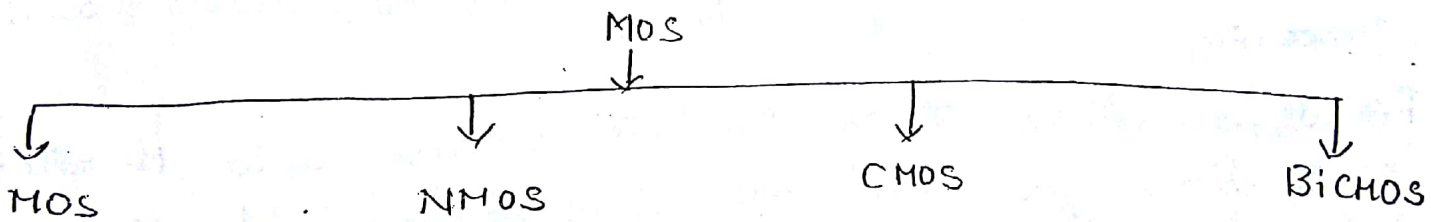
Speed - power performance



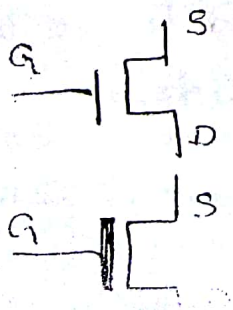
Moores law :- The number of transistors are doubled in every year. (18 months)

NMOS transistor



MOSFET — Enhancement mode / Depletion mode

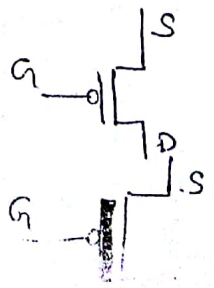
NMOS



Enhancement mode

Depletion mode

PMOS



Enhancement

Depletion

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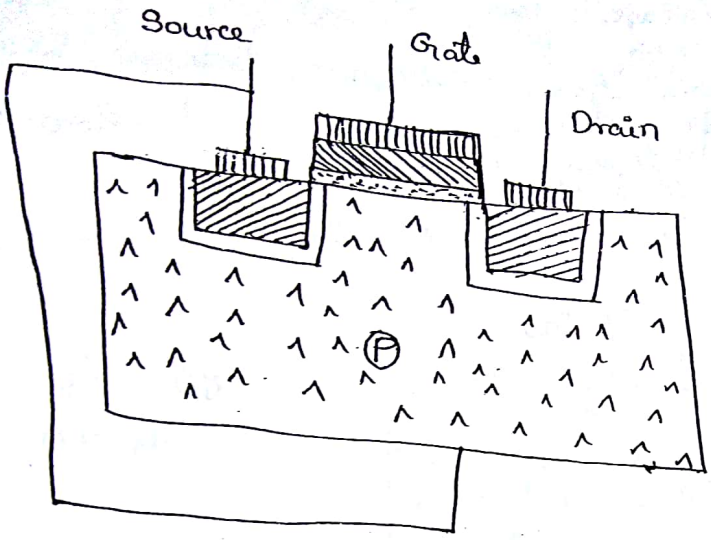
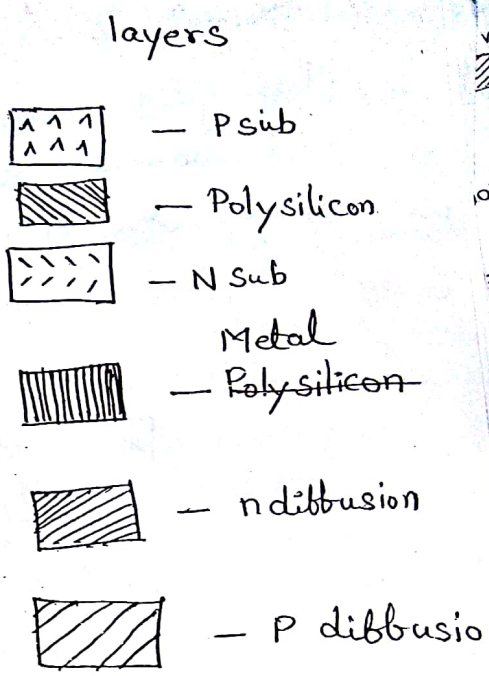
D Shivakumar

NMOS — Enhancement mode





1) Consider rectangular Silicon wafer. For designing NMOS we will consider P type material as Substrate.

2) Fill up the wafer with P-type Substrate. We know that MOSFET is having three terminal 1) Source 2) Drain 3) Gate.

3) For making Source and drain n-type impurities are diffused into P-type substrate. And to make the isolation between Source and drain Oxide layer has bee deposited on the substrate.

4) Now Source and Drain are formed. After that to make Gate poly silicon layer is deposited on the surface of Oxide layer. Now Gate has formed.

5) Now for [illegible]

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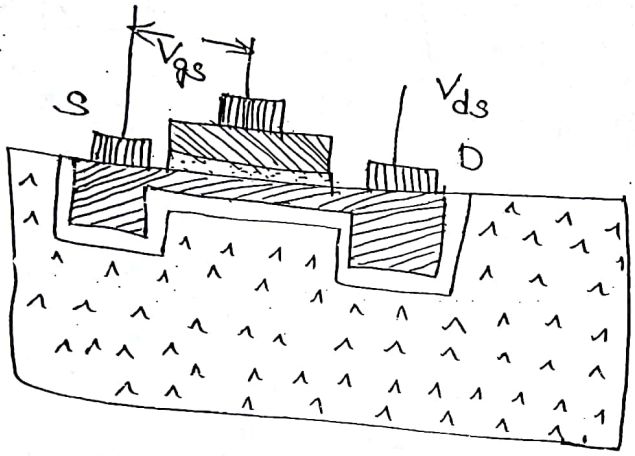
6) How it works

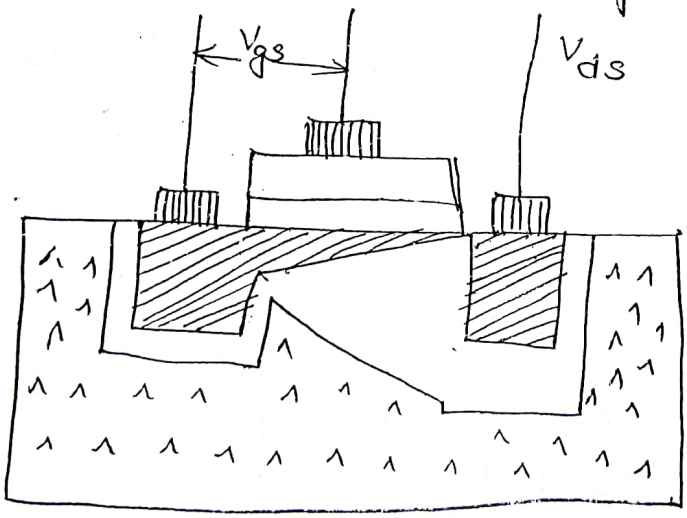
Initially no Voltage has given. In order to establish channel a minimum Voltage level of threshold Voltage has given then channel has established between Source and drain as shown in figure. But No current flow through channel ($V_{ds} = 0$)



$V_{gs} = V_t$
$V_{ds} = 0$

7) Now apply Voltage V_{ds} between drain and Source So Current Conduction takes place through channel from Source to drain. And Some Voltage drop also $V_{gs} > V_t$

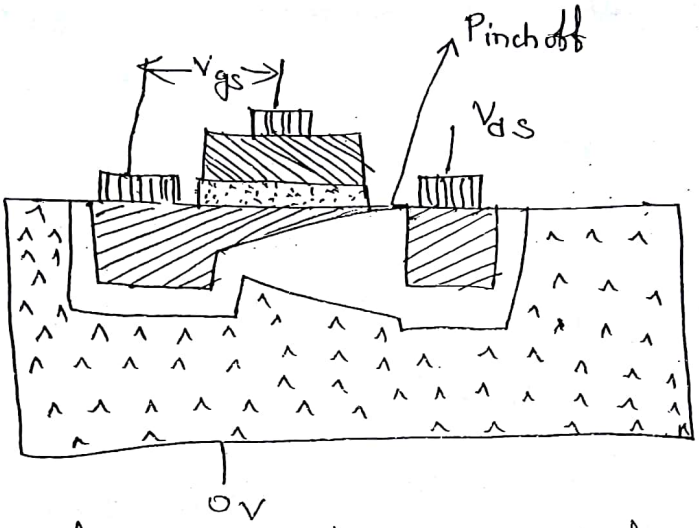
$V_{ds} < V_{gs} - V_t$



there along the channel. when the positive gate Voltage increases then channel will form and Conduction will be there from Source to drain. But every region will be their own Voltage potential. So the [illegible]

flow from Source to drain.

3). Now, increase the drain Voltage $V_{ds} > V_{gs} - V_t$ then Voltage drop will be more under the gate insulation layer, So channel will diminish from Source end to drain end. This Condition we can Call as Pinch-off Even though Current will flow from Source to drain



$V_{gs} > V_t$

$V_{ds} > V_{gs} - V_t$

The channel will act as Constant current Source. As it shows high resistance.

Normally $V_t = 1V$, $V_{DD} = 5V$, $V_t = 0.2V_{dd}$.

All the cases current will flow except $V_{gs} < V_t$.

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Basic Electrical properties of MOS and BiCMOS circuits

Drain to Source Current I_{ds} Versus Voltage V_{ds} relationship

- Voltage has given to gate to induce a charge in the channel between Source and drain.
- The charge induced is dependent on the gate to Sour Voltage V_{gs}. So Current I_{ds} is dependent on both V_{gs} and V_{ds}.

The amount of Current flow from ~~gate to~~ Source to drain is

$$I_{ds} = -I_{sd} = \frac{\text{Charge induced in channel } (Q_c)}{\text{Electron transit time } (\tau)} \quad -$$

$$\text{Transit time } \tau_{sd} = \frac{\text{Length of channel}}{\text{Velocity}} \quad -(2)$$

But Velocity $V = \mu E_{ds}$ —(3)

where μ = electron & hole mobility

E_{ds} = electric field (drain to Sourc)

$$E_{ds} = \frac{V_{ds}}{L} \quad -(4)$$

Substitute (4) in (3)

So $V = \dfrac{\mu V_{ds}}{L}$ — (5)

Now Substitute (5) in (2)

$$\tau = \frac{L^2}{\mu V_{ds}} \quad -(6)$$

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Typical Values of μ at room temperature

$$\mu_n = 650 \text{ cm}^2/\text{V sec}$$

$$\mu_p = 240 \text{ cm}^2/\text{V sec}.$$

Charge induced in channel due to gate Voltage is due to the Voltage difference b/w the gate and the channel V_g. The Voltage along the channel Varies linearly with distance X from the Source due to IR drop in the channel. Assume that the device is not saturated then the average Value is $\frac{V_{ds}}{2}$. And the effective gate Voltage $V_g = V_{gs} - V_t$. where V_t is the threshold Voltage needed to invert the channel ~~charge~~ under the gate and establish the channel.

Charge per unit area = $\boxed{E_g \epsilon_{ins} \epsilon_0}$

Induced charge $Q_c = E_g \epsilon_{ins} \epsilon_0 \omega L$

where E_g = average electric field gate to channel

ϵ_{ins} = relative permitivity of insulation b/w gate and channel.

ϵ_0 = Permitivity of free Space.

$\epsilon_0 = 8.85 \times 10^{-14} \text{ F cm}^{-1}$, $\epsilon_{ins} = 4.0$ for SiO_2

Now average electric field

$$E_g = \frac{(V_{gs} - V_t) - \frac{V_{ds}}{2}}{D}$$

where D = Oxide thickness

Thus $Q_c = \frac{(V_{gs} - V_t) - \frac{V_{ds}}{2}}{D} \cdot \epsilon_{ins} \epsilon_0 \omega L$

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$$= \frac{\epsilon_{ins}\epsilon_0 wL}{D}\left[(V_{gs}-V_t) - \frac{V_{ds}}{2}\right] \quad -(7)$$

Substitute eq (6), (7) in equation (1)

$$I_{ds} = \frac{Q_c}{\tau} = \frac{\frac{\epsilon_{ins}\epsilon_0 wL}{D}\left[(V_{gs}-V_t) - \frac{V_{ds}}{2}\right]}{\frac{L^2}{\mu V_{ds}}}$$

$$= \frac{\epsilon_{ins}\epsilon_0}{D}\frac{w}{L}\left[(V_{gs}-V_t) - \frac{V_{ds}}{2}\right]\mu V_{ds}$$

$$I_{ds} = \frac{\mu\epsilon_0\epsilon_{ins}}{D}\frac{w}{L}\left[(V_{gs}-V_t) - \frac{V_{ds}}{2}\right]V_{ds}$$

$\because K = \frac{\mu\epsilon_0\epsilon_{ins}}{D}$

$$= K\frac{w}{L}\left((V_{gs}-V_t)V_{ds} - \frac{V_{ds}^2}{2}\right) \quad -(8)$$

$\because \beta = K\frac{w}{L}$.

So $$I_{ds} = \beta\left((V_{gs}-V_t)V_{ds} - \frac{V_{ds}^2}{2}\right) \quad -(9)$$

And we know that C_g = Channel Capacitance

$$C_g = \frac{\epsilon_{ins}\epsilon_0 wL}{D} \quad -(i)$$

$$K = \frac{\epsilon_{ins}\epsilon_0\mu}{D} \quad -(ii)$$

substitute (ii) in (i)

$$C_g = \frac{K}{\mu} wL$$

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Now substitute k in I_{ds} equation

$$I_{ds} = \frac{\mu C_g}{\cancel{W} L} \cdot \frac{\cancel{W}}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

$$= \frac{\mu C_g}{L^2} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

$$I_{ds} = \frac{\mu C_g}{L^2} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \quad -(10)$$

Some times it is convenient to use gate capacitan per unit area C_o

$$C_g = C_o W L$$

Substitute $C_g = C_o W L$ in eq -(10)

$$I_{ds} = \frac{\mu C_o W \cancel{L}}{L^{\cancel{2}}} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

$$= \frac{\mu C_o W}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \quad -(11)$$

<u>In Saturation region</u>

Saturation begins when $V_{ds} = V_{gs} - V_t$. Because at this point the IR drop in the channel equals the effec gate to channel voltage at the drain. And assume that the current remains fairly constant as V_{ds} increas further.

$$I_{ds} = K \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2}$$

(or) $$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2$$

(or)

$$I_{ds} = \frac{C_g \mu}{2} (V_{gs} - V_t)^2 \text{ (or) } = \frac{C_o \mu W}{2} (V_{gs} - V_t)^2$$

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MOS transistor transconductance g_m and output Conductance g_{ds}

$$g_m = \left.\frac{\delta I_{ds}}{\delta V_{gs}}\right|_{V_{ds} = \text{const}}$$

we know that $= I_{ds} = \frac{Q_c}{\tau}$

$$\delta I_{ds} = \frac{\delta Q_c}{\tau_{ds}}$$

Now $\tau_{ds} = \frac{L^2}{\mu V_{ds}}$

$$\delta I_{ds} = \frac{\delta Q_c \, \mu V_{ds}}{L^2}$$

but we know $\delta Q_c = C_g \, \delta V_{gs}$

$$\delta I_{ds} = \frac{C_g \, \delta V_{gs} \, \mu V_{ds}}{L^2}$$

$$\Rightarrow \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{\mu C_g V_{ds}}{L^2}$$

In saturation $V_{ds} = V_{gs} - V_t$

$$g_m = \frac{\mu C_g}{L^2}(V_{gs} - V_t)$$

but $C_g = \frac{\varepsilon_0 \varepsilon_{ins} WL}{D}$

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$$g_m = \frac{\mu \epsilon_0 \epsilon_{ins} \omega}{D L} (V_{gs} - V_t)$$

$$= \frac{\mu \epsilon_0 \epsilon_{ins}}{D} \cdot \frac{\omega}{L} (V_{gs} - V_t)$$

$$= K \cdot \frac{\omega}{L} (V_{gs} - V_t)$$

$$= \beta (V_{gs} - V_t)$$

$g_{ds} \Rightarrow$

Mos transistor Figure of merit ω_0

Frequency response may be obtained from the parameter $\omega_0 = \frac{g_m}{C_g} = \frac{\mu}{L^2} (V_{gs} - V_t)$

$$= \frac{\mu}{L^2} (V_{ds}) = \frac{1}{\tau_{ds}}$$

τ_{ds} = Transit time.

From the above equation Switching Speed depends on gate Voltage above threshold and on Carrier mobilit and Inversely as the Square of channel length.

- Note: Normally electron mobility μ_n is larger than 3 times as hole mobility.

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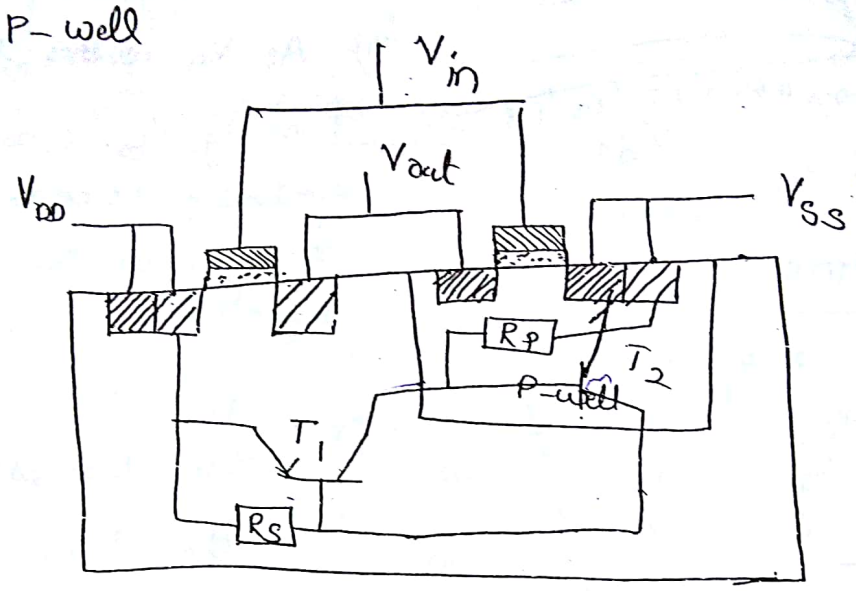
C_{GC} = gate to channel Cap

C_{GS} = gate to Source Capacitance

C_{GD} = gate to drain Capacitance.

Latch up



1) Latchup occurs because of Large number of Junctions.

2) Latch up is a Condition in which the parasi Components give rise to the establishment of low resistance Conducting paths between V_{DD} and V_{SS} because of formation of transistors and dio

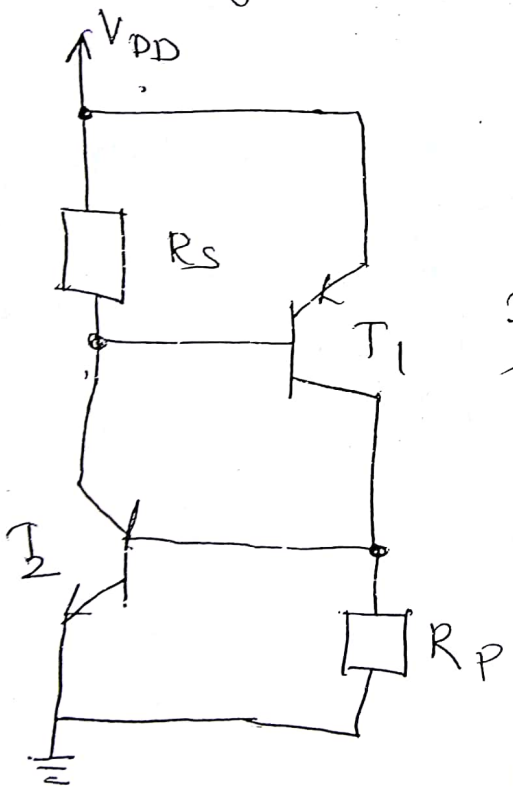
3) Latches may be induced by glitches on the supply rails.

4) Here in the above circuit two transisti

between V_{DD} and V_{SS}.

5) If Sufficient Substrate Current flows to generate enough Voltage across R_S to turn on transist T_1, this will draw Current through R_P and in P-well also If the Voltage across R_P Sufficient T_2 will also turn on.

6) It establish a low resistance path between the Supply rails.



Latch up circuit model.

7) with no injected Curr the parasitic transistors exhibit high resistance.

8) Once it is latched up, this Condition will be maintain until the latch up current dro below I_1.

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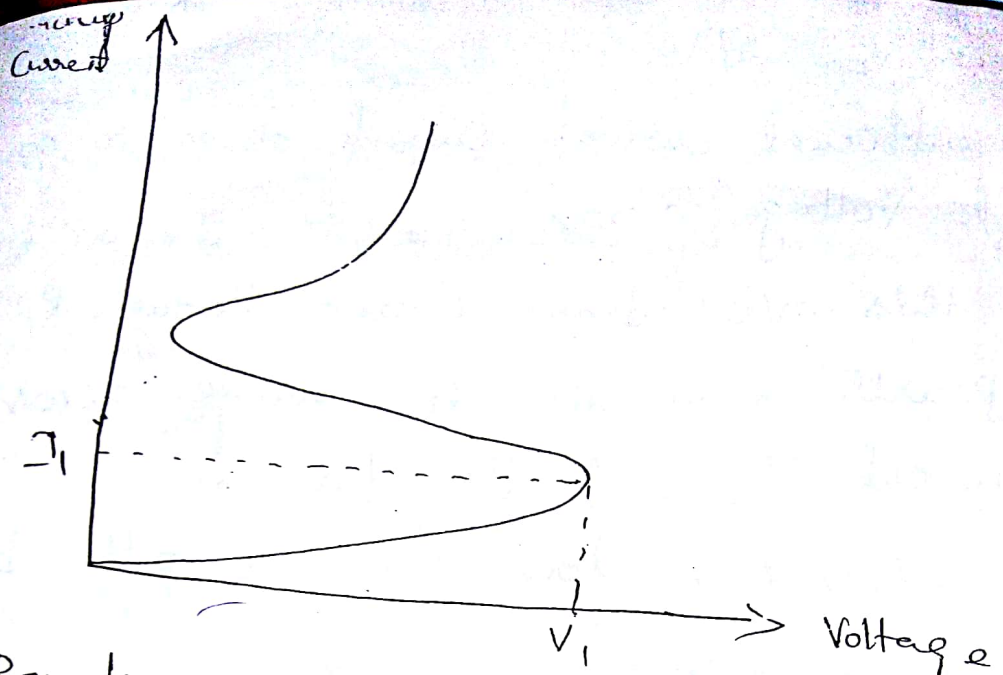

Remedies

1) Increase substrate doping levels with a consequ drop in the value of R_S.
2) Reduce R_P by control of fabrication parameters.
3) Introduction of guard rings on V_{dd} and V_{SS}

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Aspects of MOS Transistor threshold Voltage V_t

The gate structure of a MOS transistor consists electrical OFF charges stored in the dielectric layers and in the surface to surface interfaces as well as in the substrate itself.

For Enhancement mode MOS transistor we need to give (+ve voltage to make the transistor ON.

For depletion mode MOS transistor (-ve) Voltage to neutralise the charge stored.

Switching an enhancement mode MOS transistor from the OFF to the ON state consists in applying sufficien gate voltage, to neutralize these charges and enable the underlying silicon to undergo an inversion due to th electric field from the gate.

Switching a depletion mode nMOS transistor from ON to the off state consists in applying enough Voltag to the gate to add to the stored charge and invert the n-implant region to 'p'.

The threshold Voltage V_t may be expressed as

$$V_t = \phi_{ms} \frac{Q_B - Q_{ss}}{C_0} + 2\phi_{fN}$$

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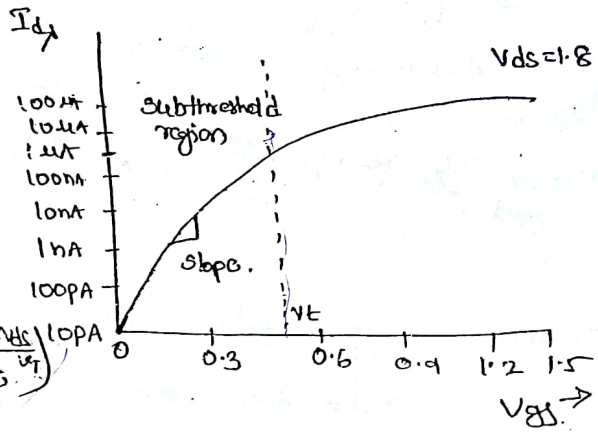
Subthreshold Conduction:-

→ The ideal transistor model assumes current only flows from source to drain when $V_{gs} > V_t$.

→ In real transistors, some current will flow even threshold vol is below.

→ The current does not abruptly cut off below threshold voltage, but rather drops off exponentially.

→ This conduction is also known as leakage. It is undesirable.



→ The subthreshold conduction or leakage current is denoted by

$$I_{ds} = I_{ds0}\, e^{\frac{V_{gs}-V_t}{nV_T}} \left(1 - e^{\frac{-V_{ds}}{V_T}}\right)$$

where,

$I_{ds0} = \beta V_T^2 e^{1.8}$ = is the current at threshold.

$e^{1.8}$ = device geometry value.

n = is process dependent term, range (1.4–1.5) for cmos.

V_T = Thermal voltage.

* Junction Leakage :-

→ In the construction of MOS devices, many P-N junctions are formed. For example, P-N diodes between diffusions and substrates, diffusions between wells and P-N junction b/w well and substrate. All these diodes should be in reverse biased. practically, reverse bias diodes still conduct a small amount of current I_D called as junction leakage.

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$$\therefore \quad I_D = I_S \left(e^{\frac{V_D}{V_T}} - 1 \right)$$

I_D = diode current

I_S = reverse saturation current

V_d = diode voltage [ex:- V_{sb} or V_{db}]

V_T = Thermal voltage.

- Tunneling:-

According to quantum mechanics, there is some probability that carriers will tunnel through the gate oxide. This results in gate leakage current flowing into the gate.

Channel Length Modulation:-

In the saturation region, the current I_{ds} is independent of V_{DS}, this makes transistor a perfect current source.

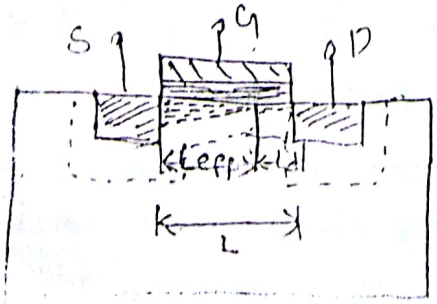
The depletion region at drain side with a width L_d increases with reversed biased voltage. This depletion region effectively shortens the channel length to

$$L_{eff} = L - L_d$$

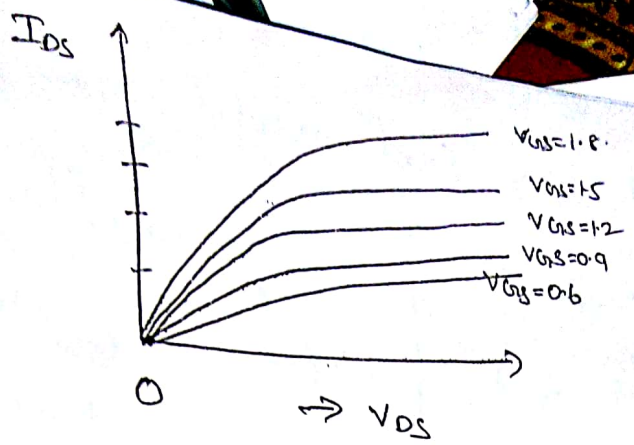
L_{eff} → change in channel length

L → actual length of channel.

L_d → length of depletion region.



⇒ The shorter channel length results in higher I_{DS} current and it also increases with V_{DS} in Saturation region.



Now, the I_{DS} in saturation region is given by:

$$I_{DS} = \beta/2\,(V_{gs}-V_t)^2 \cdot (1+\lambda V_{ds})$$

where, λ is channel length modulation factor.

→ As channel length gets shorter, the effect of channel length modulation becomes more significant.

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Comparison between CMOS and Bipolar technologies

CMOS technology	Bipolar technology
• Low static power dissipation	• High power dissipation
• High input impedance (low drive current)	• Low input impedance (high drive current)
• Scalable threshold voltage	• Fixed threshold voltage
• High noise margin	• Low voltage swing logic
• High packing density	• Low packing density
• High delay sensitivity to load	• Low delay sensitivity to load
• Low output drive current	• High output drive current
• Low g_m	• High g_m
• Bidirectional capability	• Essentially unidirectional
• Ideal switching device	

L P → Power dissipation
H I → Input impedence
H N → noise margin
H P → Packing density
L O → output drive current
H D → Delay sensitivity
L G → gand → g_m
B → Bhi → Bidirectional capability
T → Thod → Threshold voltage
Scalable

Frequency for $\omega_0 = g_m/C_g$

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* nMOS fabrication → Start with a thin wafer of Si (material used of SiO_2)

** Steps of polysilicon gate self-aligning nMOS fabrication process involves 8 steps.

(i) Wafer / P-Substrate :-

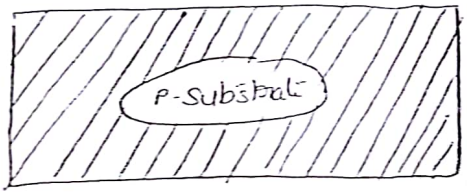
Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required P-impurities are doped as the crystal is grown.

> Diameter of wafer → 75 - 150mm

> Thickness " " → 0.3 - 0.4mm (diffusion process) (human hair - 0.1mm)

> Doping Concentration of boron → $10^{15}/cm^3$ to $10^{16}/cm^3$ → (conductor)

> Resistivity → 25 Ω-cm to 2 Ω-cm (b/w a conductor & an insulator)

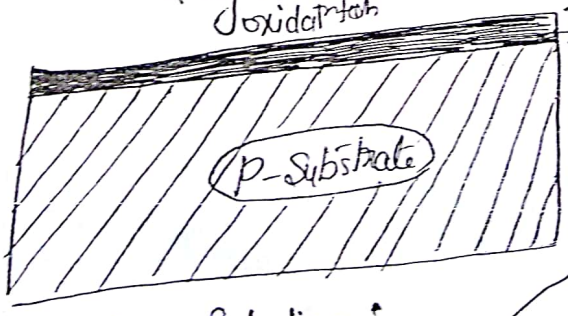


Step 2 : Oxidation over p-Substrate :

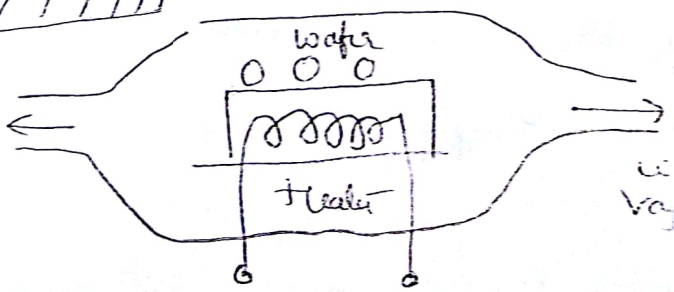
A layer of silicon dioxide (SiO_2), typically 1μm thick is grown all over the surface of the wafer to protect the surface, act as a barrier (mask) to dopants during process.

* Importance of thick oxide : To provide a insulating substrate onto which other layers may be deposited & patterned. & used as an insulating separator b/w different conducting layers)

> Thickness → 1μm using wet oxidation



furnace used for oxidation :



* The process of growing oxide layer is known as oxidation.

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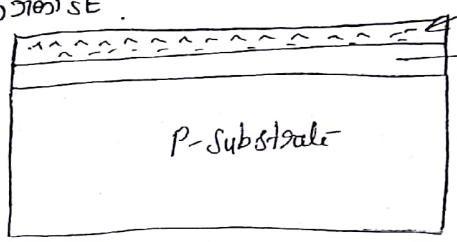
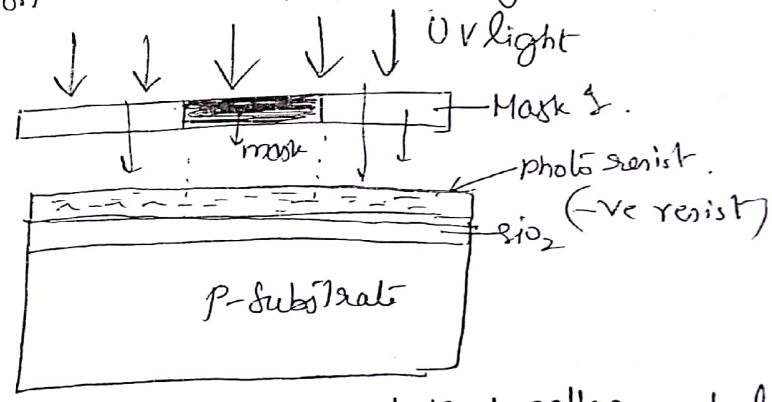
Step 3: Even distribution of thickness/patterned layers

*Photolithography: It is a technique used to pattern layers of different materials on the wafer with help of mask plates.
(expension glass plate with opaque & transparent regions)

(i) The Surface is coated with a photosensitive emulsion called photo-resist & spun at high speed to get uniform thin layer of photoresist.
(Speed 3000rpm)

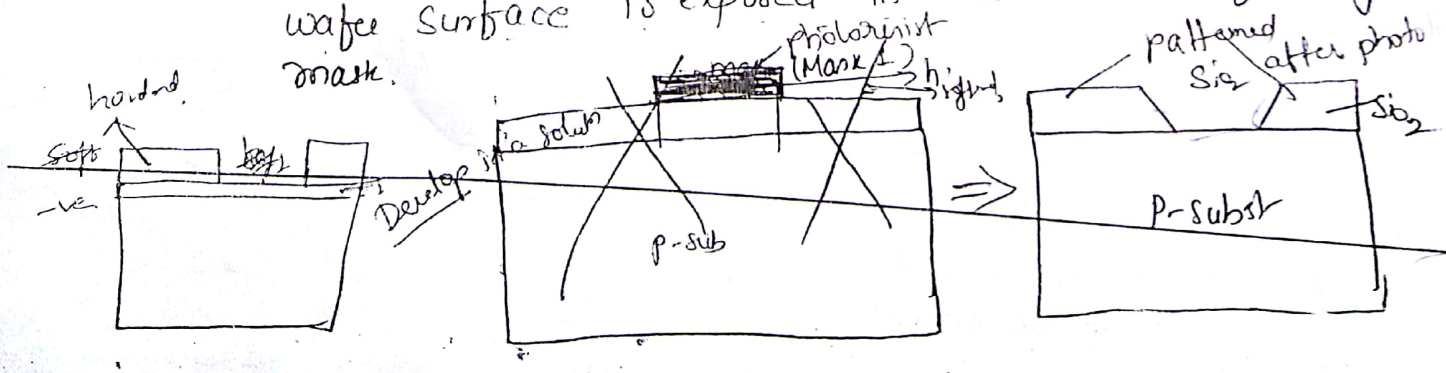


(ii) The photoresist layer is then exposed to ultraviolet light through a mask which defines those regions into which diffusion is to take place together with transistor channel.



~~Step 4~~ (iii) Etching Process: To create a desired pattern, actual removal of the material is done by etching process.

∴ Masked areas are subsequently readily etched away together with the underlying silicondioxide, so that the wafer surface is exposed in the window defined by the mask.



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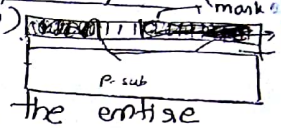
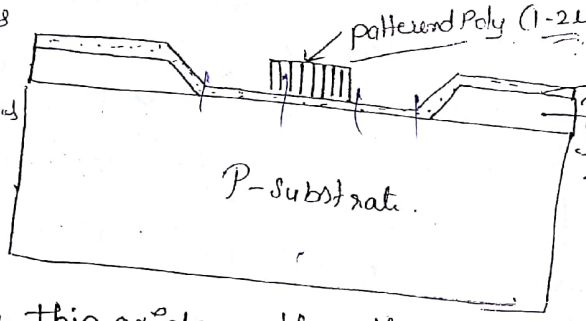
Step4: Diffusion Deposition:

In the MOS fabricat° process, conducting layers such as polysilicon + aluminium + protect° layers lik SiO_2 + Si_3N_4 are deposited onto the wafer surface by using chemical vapor deposit° tech (CVD) in high-temp chamber. (poly: $SiH_4 \xrightarrow{1000°C} Si + 2H_2$)



>> A thinlayer of SiO_2 (0.1μm) is grown over the entire wafer surface and then polysilicon is deposited on top of this to form the gate structure.

CVD is a chemical process to produce high quality, solid-materials



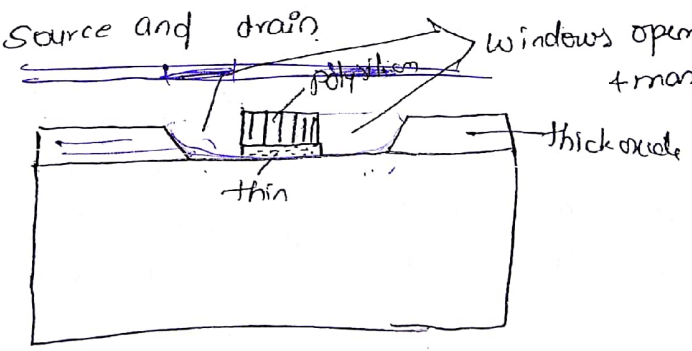
>> Again by using a mask (Mask 2) + photo process, the polysi...

$SiH_4 + O_2 \xrightarrow{400-450°C} SiO_2 + ...$

Note (* for thin oxide, the threshold voltage is low + for thick oxide, " " " is high) ($V_t = 2V$) (∵ $V_{th} \propto \frac{1}{C_{ox}}$ ↓, ↓ $C_{ox} \propto \frac{1}{t_{ox}}$ ↑)

Eg: → $V_t = 30V$ → for parasitic transistors not to be ON

Step5: Again Photolithography steps repeated to remove the thin oxide into which n-type impurities are to be diffused. to form source and drain



Step6: Diffusion: It is achieved by heating the wafer to a high temperature + passing a gas containing the desired n-type impurity (Eg: phosphorus) over the surface

Note ** (The polysilicon with underlying thin oxide + the thick oxide acts as masks during diffusion — the process is self aligning ∴ source + drain are aligned automatically w.r.to gate structure

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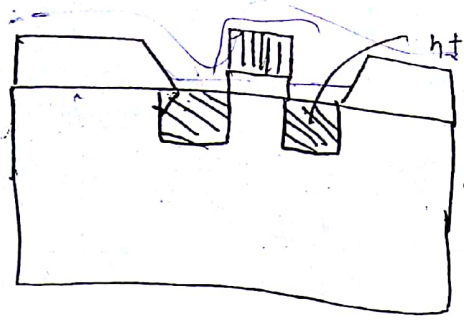
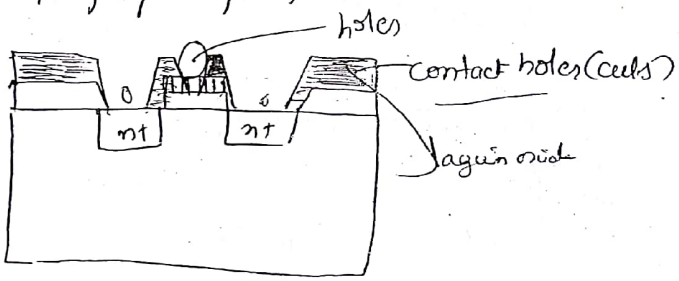


* With the polysi + underlying oxide layer as protective mask, the diff (ion implan process) is performed

Step 7: Thick oxide is grown over all again + is then masked (Mask 3) with photoresist + etched to expose areas of the polysi gate + the drain and source areas where connections are to be made.

> Photolythography steps for contact cuts

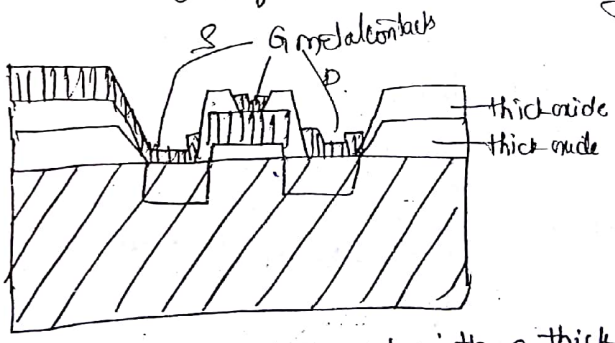


Step 8: Deposition of metal for interconnect pattern.

(i) deposition of 1um thickness of metal all over the surface using CVD

(ii) photolithography steps to get patterned metallization (Mask 4)

thick - 1um



* The entire wafer is again covered with a thick oxide layer - known as overglassing. This oxide layer act as a protective layer to protect different parts from the environment. - enhancement nMOS-type

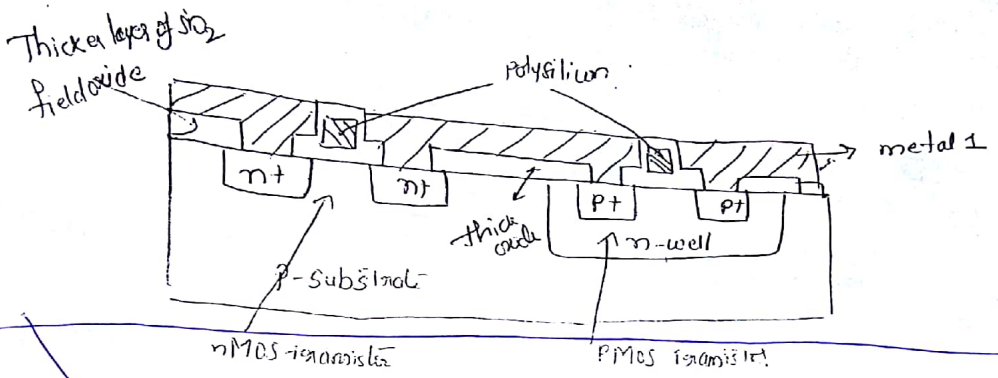
* Depletion-type: In depletion-type transistors one addition step is (in blue step + 2) necessary for the formation of ~~nMOS enhance~~ n-diffusions in the channel regions.

* To form a n-channel ~~it will require~~ one additional mask to define channel regions following a diffusion process using the ion implantation technique.

* CMOS Fabrication Steps:

CMOS - Combination of PMOS & NMOS.

Cross-Section view:



> CMOS process with a p-type substrate.

The PMOS transistor requires an n-type body region so an n-well is diffused into the substrate in its (region near) vicinity.

Note:- CMOS substrate process with an n-type substrate & p-wells to contain the nMOS transistor.

> A thicker layer of SiO_2 called field oxide prevents metal from shorting to other layers except where contacts are explicitly etched.

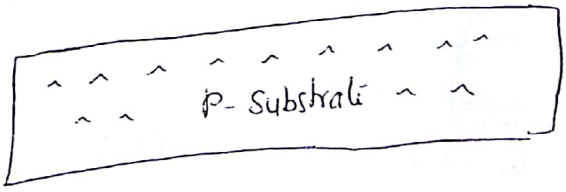
*Note: p-substrate must be tied to a low potential to avoid forward biasing the p-n junction b/w the p-type substrate & the n^+ MOS 'S' & 'D'.

Ly, n-well must be tied to a high-potential.

|| The heavily doping is required to establish a good ohmic contact that provides low resistance for bidirectional current flow.

Fabrication Steps:

Step 1: Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required p-impurities are doped



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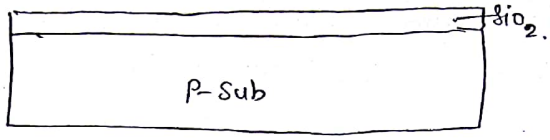
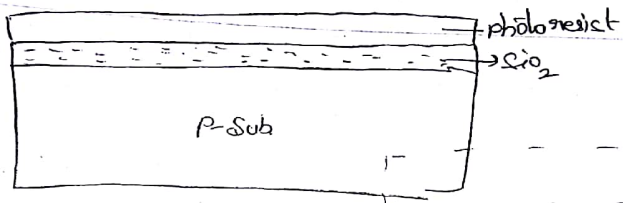
Step2: Oxidation: The wafer is oxidized at high temp (900°-12...) that causes the Si of O_2 to react & become SiO_2 on the wafer surface.

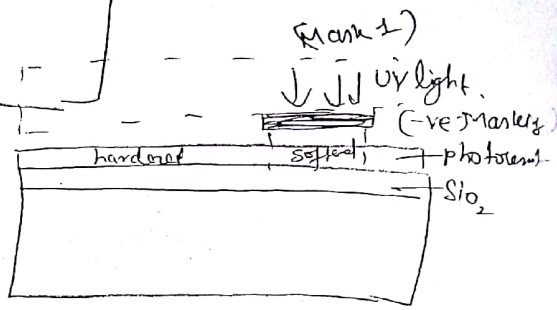


Step3: photolithography process is done, so that oxide must be patterned to define the n-well.

(i) place photoresist film

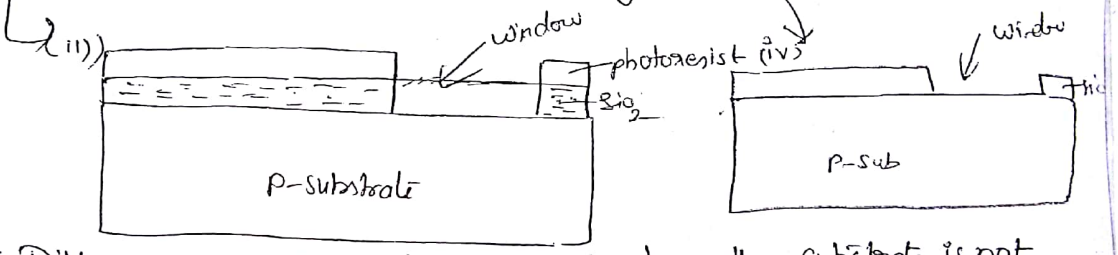


(ii) Mask: Expose to radiation which allows light to pass through only where the well should be

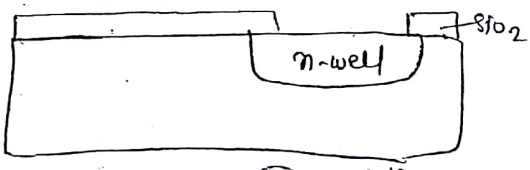


(iii) Develop pattern with photo resist

(iv) removal of extra material using etching process.



Step4: Diffusion process to form a well where the substrate is not covered with oxide. Use ion implantation for uniform doping



Step5: form Transistor Gates. Deposition.

first remove the remaining oxide. As polySi generally placed over a thin layer of oxide

> The thin oxide is grown in a furnace

> wafer is placed in a reactor with silane gas (SiH_4) & heated again to grow the polysilicon layer ~~through a process~~ called chemical vapor deposition.

*Note polySi is heavily doped to form a resonably good conductor.

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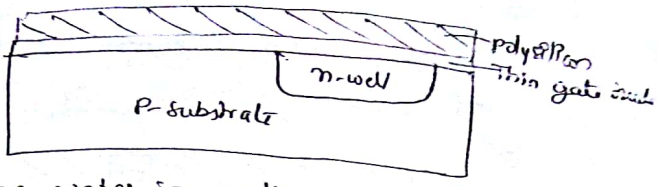
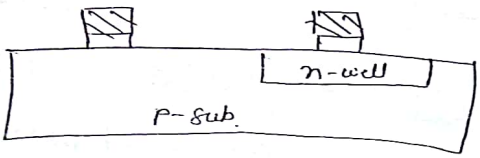
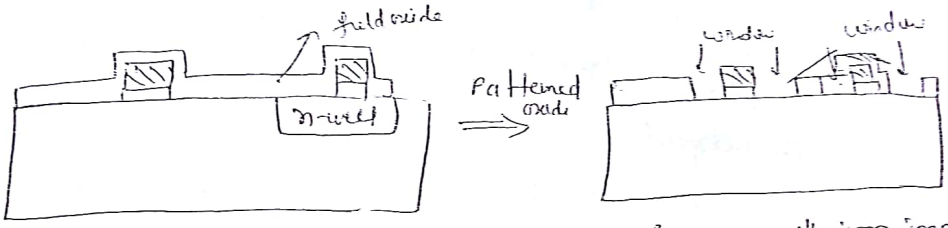


Step6: The wafer is patterned with photoresist & the polysilicon mask (Mask2) leaving the polysilicon gates

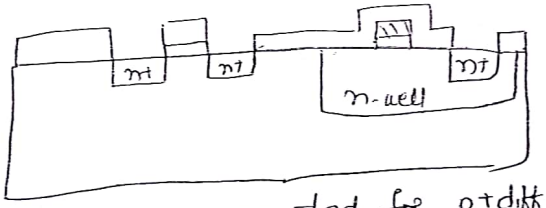


Step7: The n^+ regions are diffused to create the transistor active area & the well contact. A protective layer of oxide is formed and patterned with the n-diff mask.



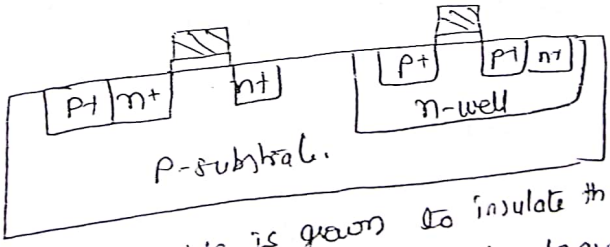
Step8: Diffusion process for n^+ region is formed with ion implantation.
* The polysi gate over the n-MOS transistor blocks the diff so the source & drain are separated by a channel under the gate. - called self-aligned

n+ diff mask

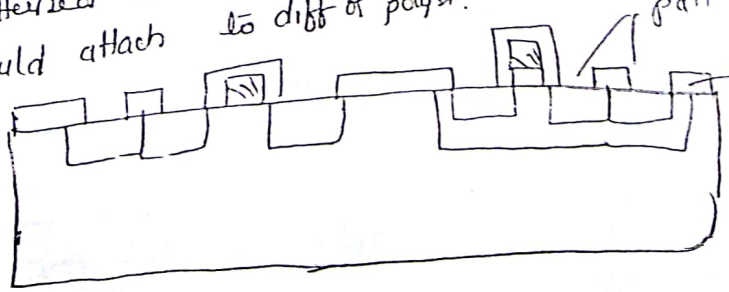


Step9: The step 7 & 8 repeated for p+diff mask to give the structure

p+ diff mask



Step10: The field oxide is grown to insulate the wafer from metal & patterned with contact mask, to leave contact cuts where metal should attach to diff or polysi.



Contact mask

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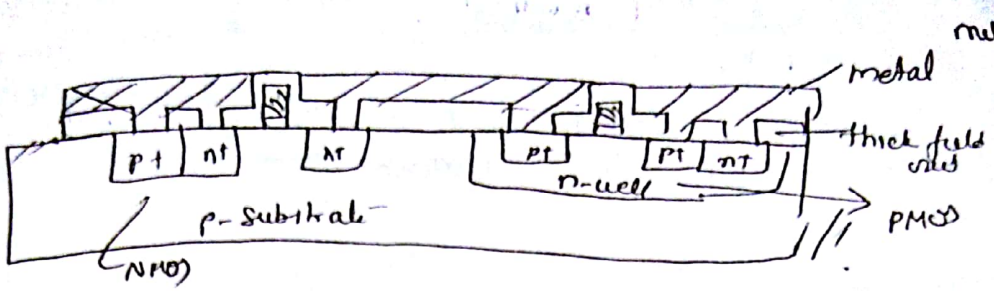
ingot

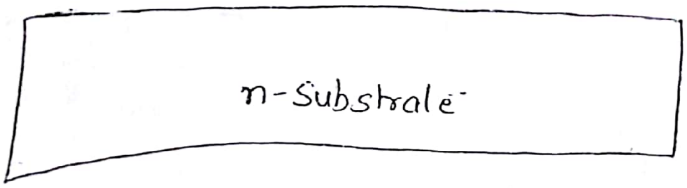
Step 11: Metallization. The metal is patterned with metal mask



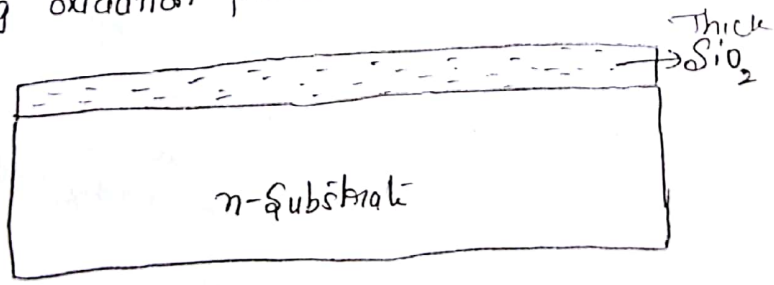
* CMOS fabrication Using p-well process:

Step 1: The basic idea behind the p-well process is the formation of an p-well or tub in the n-type substrate and fabrication of n-transistors within this well.

(i) Start with a blank wafer, comonly known as substrate, which is lightly doped.

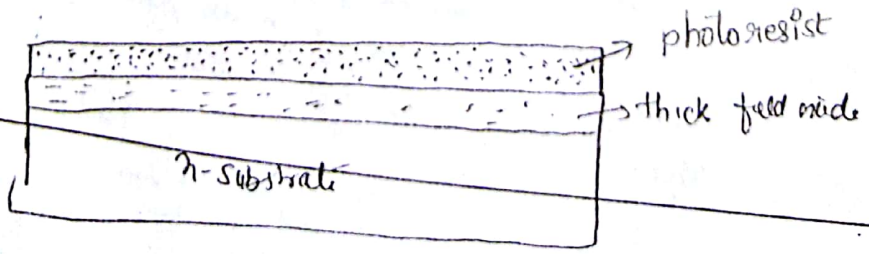


(ii) Oxidation: Cover the wafer with a protective layer of SiO_2 (o using oxidation process at 900-1200°c with H_2O (wet oxidation



(iii) Photolithography process to diffuse 'n'-impurity in a masked area.

→ Spin a photoresist, which is a light-sensitive organic polymer. It soft-ens / hardends when exposed to light
+ve. -ve resist



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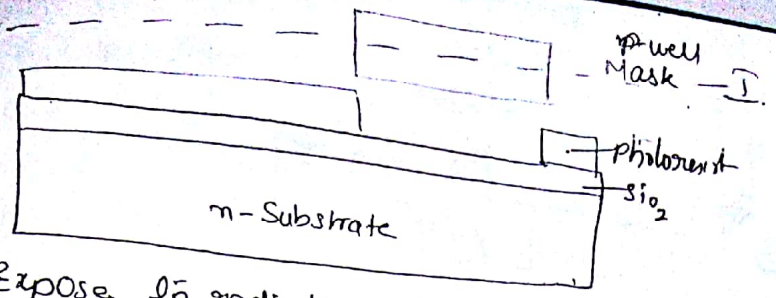
→

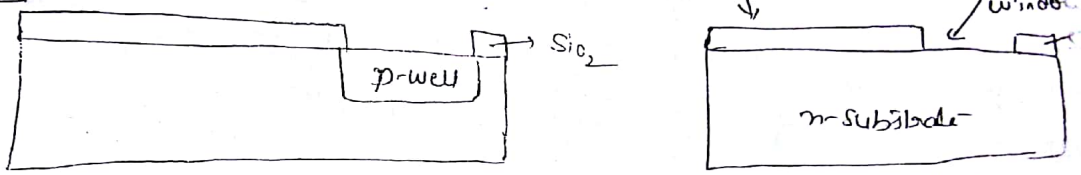


→ Expose to radiation through p-well mask. +

→ Develop - i.e. soak in a solution + strip off the photoresist

→ Etching: Etch the oxide with HF, which only attacks oxide. (mixture acids)
where the resist has been exposed + later remove photoresist

(iv) Diffusion:

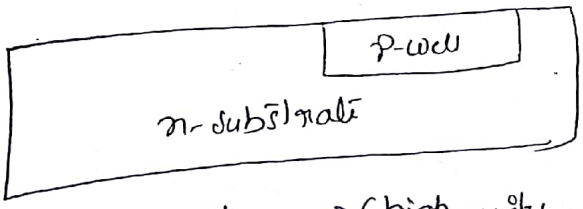


Implant or diffuse p dopants into exposed wafer using diffusion or ion implantation

> The ion implantation process allows shallower wells suitable for the fabrication of devices of smaller dimensions.

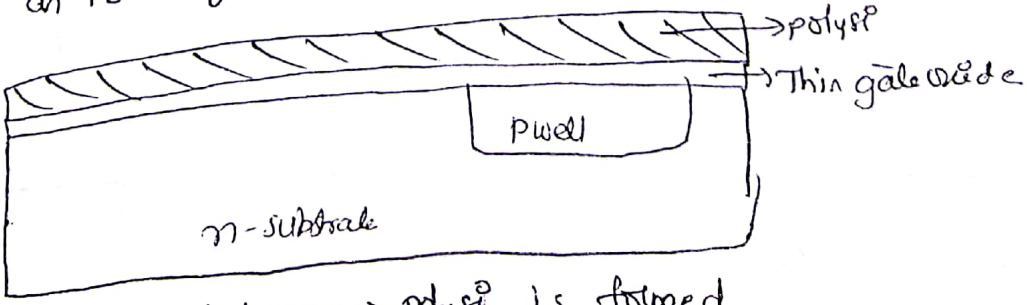
> The diffusion process occurs in all directions + dipper the diffusion more it spreads laterally.

(v) Strip off the remaining oxide using (HF), leaving behind the p-substrate + along with the p-well.



(vi) Deposition of polysilicon → (high purity, polycrystalline form of si)

→ The formation of thin oxide regions for the formation of p and n-transistors require mask 2 which is also known as active mask as it defines the thin oxide regions where gates are formed



→ Using CVD technique → polysi is formed

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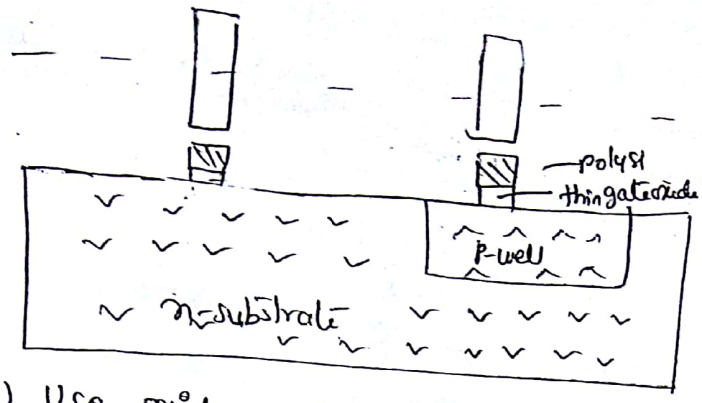
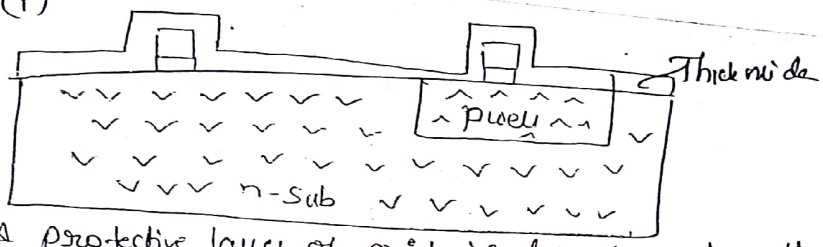


(vii) Use oxide and masking to expose where p+ dopants should be diffused or implanted.

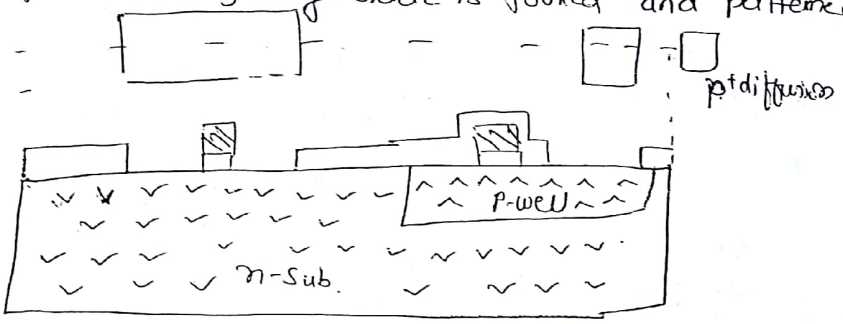
P-diff forms pMOS source & drain, and p-well contact.

(i)

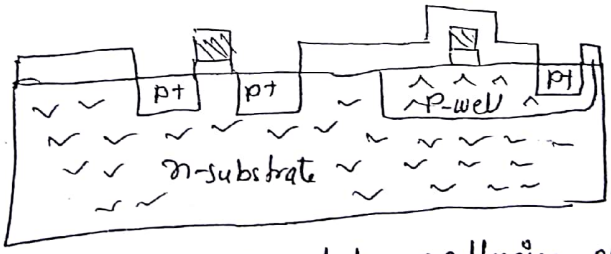


> A protective layer of oxide is formed and patterned with the P-diff mask

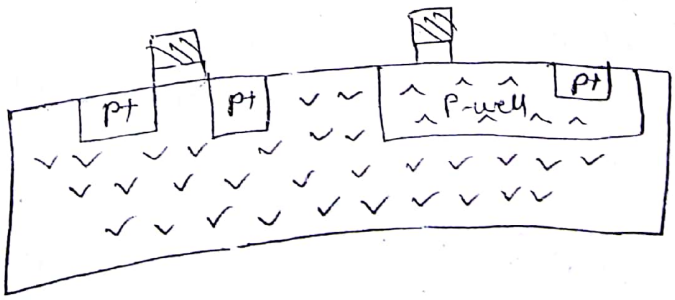
(iv)



(iii) Diffusion process for p+ region is formed with ion implantation Self-aligning process



(viii) Strip off oxide to complete patterning step



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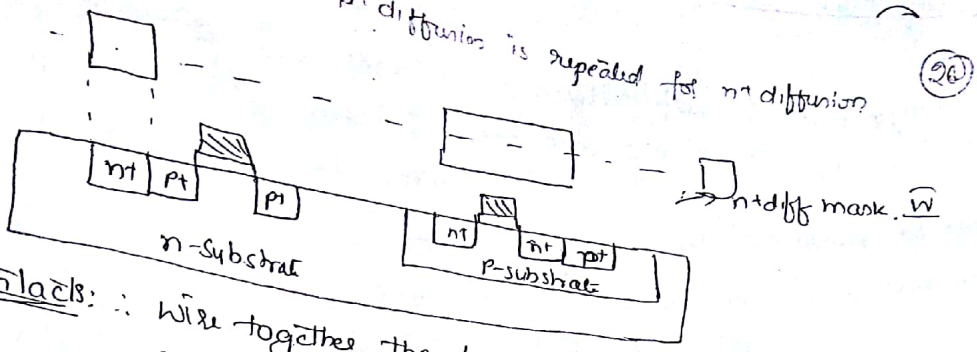
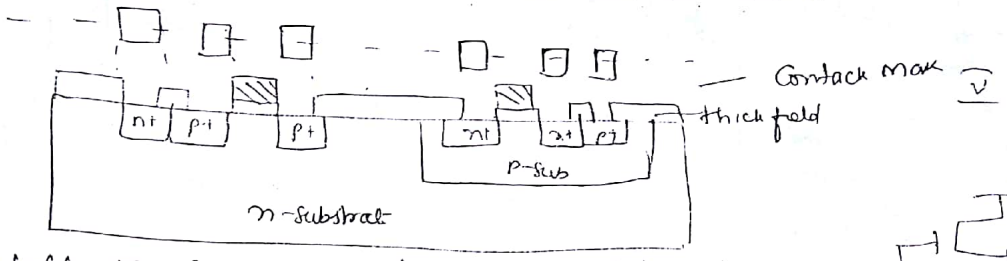
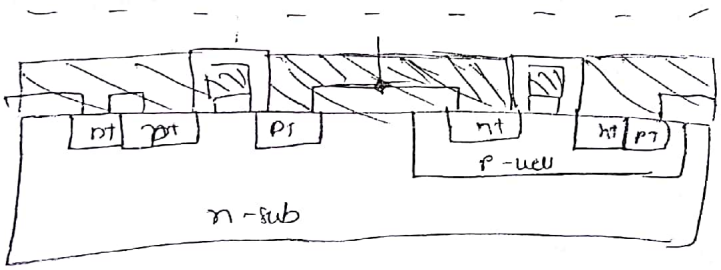
(ix) The steps used for p^+ diffusion is repeated for n^+ diffusion

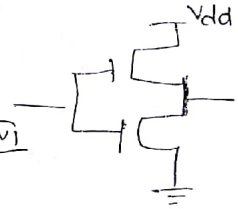


(x) Contacts: ∴ Wire together the devices, Cover chip with thick field oxide Etch oxide where contact cuts are needed.



(xi) Metallization: Sputter on aluminum over whole wafer - mask vi





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Twin Tub

(28)

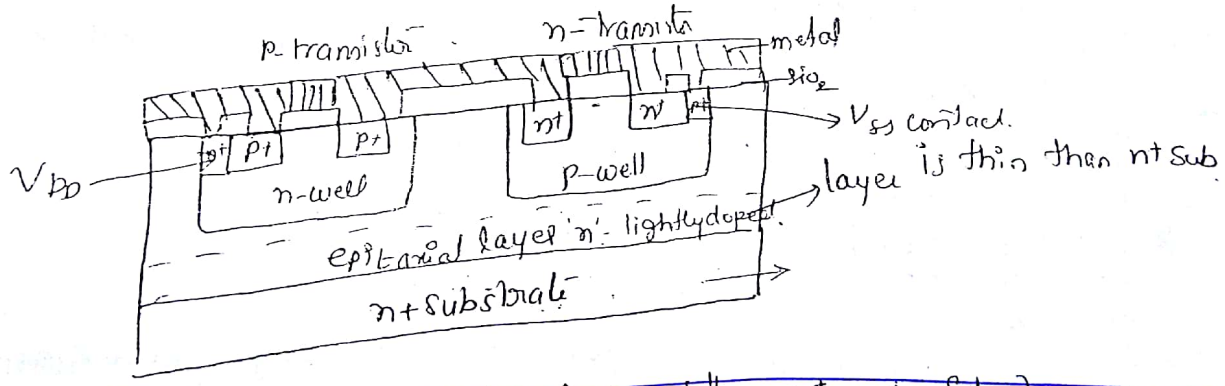
In the twin-tub process, the starting material is either an n^+ or p^+ substrate with a lightly doped epitaxial layer, which is used for protection against latch-up.

> The process is similar to the n-well process involving the following steps.

- Tub formation
- Thin oxide construction
- Source and drain implantations
- Contact cut definition
- Metallization

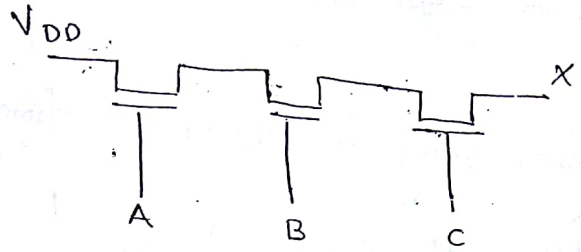
> This process allows n-transistors and p-transistors to be separately optimized to provide balanced performance of both types of transistors.

> The threshold voltage, body effect & the gain associated with n+p devices have to be independently optimized.



(i.e. the material is either n^+ or p^+ sub)

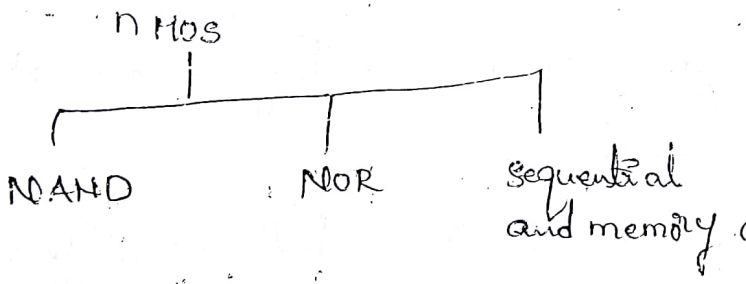
2.5 The pass transistor



$X = A \cdot B \cdot C$

These mos transistors to be used as switches in series with lines carrying logic levels. This application of the MOS device is called the pass transistor.

2.6 The nMOS inverter



The basic inverter ckt requires a transistor with source connected to ground and a load resistor connected from the drain to the positive supply rail V_{DD}. The output is taken from the drain and the i/p applied b/w gate and ground.

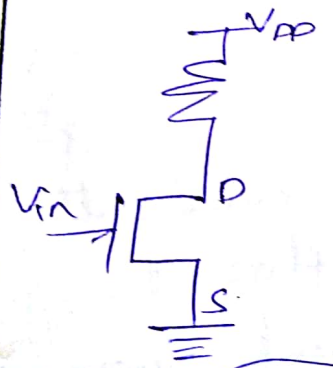
Normally every transistor is having internal

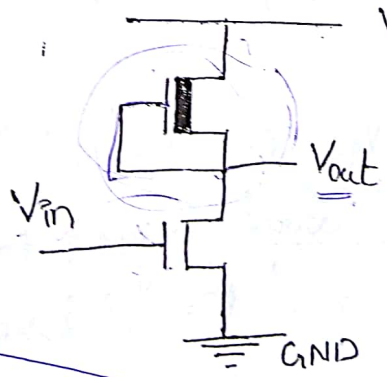
parasitic resistance and capacitances. So if we take PMOS which is larger than the NMOS by 3 time so obviously the internal parasitic resistors ~~are~~ occupy more area. So to over come this problem depletion mode transistor as the load then

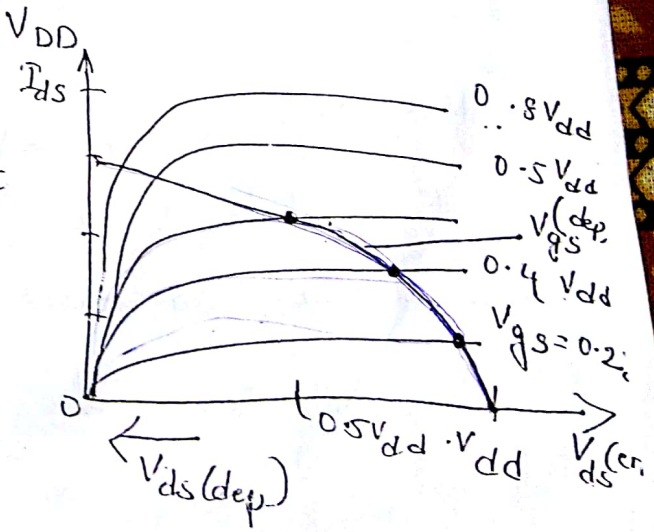
1) With no current drawn from the o/p, the currents I_{ds} for both transistors must be equal.

2) For the depletion mode transistor, the gate is connected to the source so it is always on (and only ~~the characteristic curve $V_{gs}=0$ is relevant~~).

3) In this configuration the depletion mode device is called the pull-up (P.u) and the enhancement mode device the pull-down (P.d) transistor.





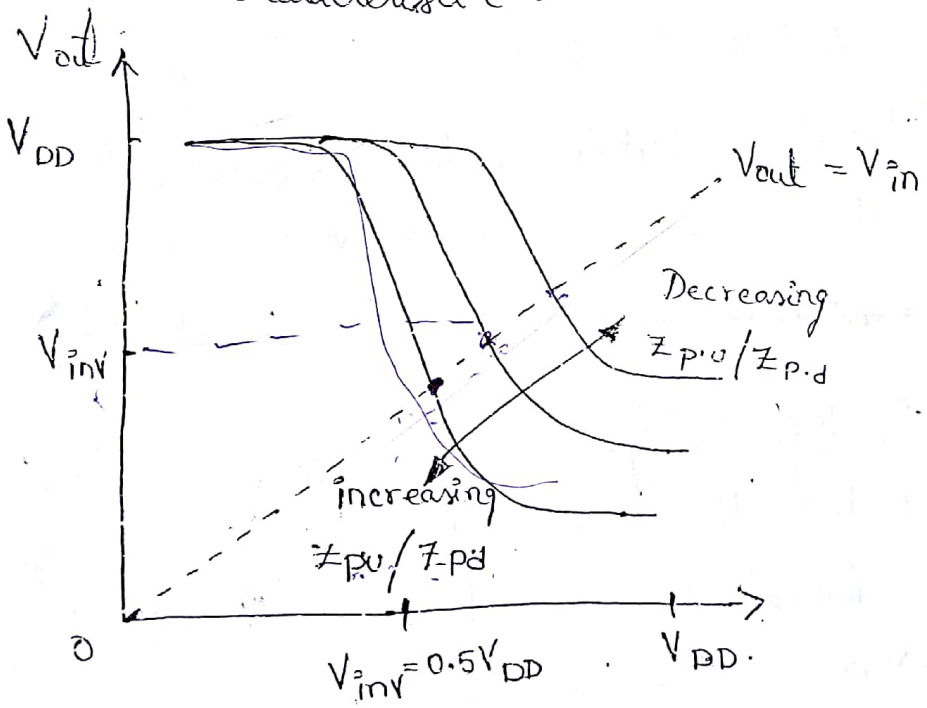


Enh → P.D → Sat

De → P.U

To obtain the inverter transfer characteristic super impose the $V_{gs}=0$ depletion mode characteristic on the family of curves for the enhancement mode device, we will note the voltage across the enhancement mode device corresponds to minimum voltage across the depletion mode transistor.

5) The points of intersection of curves give points on the transfer characteristic.



6) Note that as V_{in} (= V_{gs} p.d transistor) exceeds the p.d. threshold voltage current begins to flow. The o/p voltage thus decreases and the subsequent increase in V_{in} will cause the p.d transistor to come out of saturation and become resistive. The p.u transistor is

Initially resistive as the p.d transistor turns on

7) During transition, the slope of the transfer characteristic determines the gain.

$$\text{Gain} = \frac{\delta V_{out}}{\delta V_{in}}$$

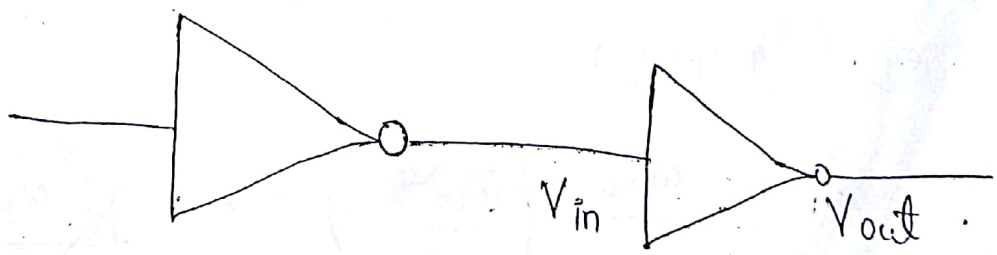
8) The point at which $V_{out} = V_{in}$ is denoted as V_{inv} and it will be noted that the transfer characteristic and V_{inv} can be shifted by variation of the ratio Pull-up to pull-down resistances.

$Z_{pu}/Z_{p.d}$ Z is the ratio of w, L.

2.7) <u>Determination of Pull-up to pull-down ratio ($Z_{p.u}/Z_{p.d}$) for an nMOS inverter driven by another nMOS inverter.</u>

4:1

$$\frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}$$



Consider the depletion mode transistor for which $V_{gs} = 0$ under all conditions, and assume that

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in order to cascade inverters with out degra
of levels we are aiming to meet the require

$$V_{in} = V_{out} = V_{inv}$$

for equal margins around the inverter threshold we set $V_{inv} = 0.5 V_{DD}$. At this point both transistors are in saturation

$$I_{ds} = k \frac{W}{L} \left(\frac{(V_{gs} - V_t)^2}{2} \right)$$

in depletion mode

$$I_{ds} = k \frac{W}{L} \left(\frac{(-V_t)^2}{2} \right) \quad \because V_{gs} = 0.$$

$$= k \frac{W_{p.u}}{L_{p.u}} \left(\frac{V_{td}^2}{2} \right) \quad \text{--(1)}$$

in enhancement mode

$$I_{ds} = k \frac{W_{pd}}{L_{p.d}} \frac{(V_{inv} - V_t)^2}{2} \quad \because V_{gs} = V_{inv} \quad \text{--(2)}$$

equating (1), (2)

$$\cancel{k} \cdot \frac{W_{p.u}}{L_{p.u}} \left(\frac{V_{td}^2}{2} \right) = \cancel{k} \frac{W_{p.d}}{L_{p.d}} \frac{(V_{inv} - V_t)}{2}$$

$$Z_{p.d} = \frac{L_{p.d}}{W_{p.d}} \; ; \quad Z_{p.u} = \frac{L_{p.u}}{W_{p.u}}$$

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$$\frac{1}{Z_{p.u}}\left(\frac{V_{td}^2}{2}\right) = \frac{Z_{p.u}}{Z_{p.d}}\left(\frac{(V_{inv}-V_t)^2}{2}\right)$$

$$\boxed{\frac{Z_{p.u}}{Z_{p.d}} = \frac{(V_{inv}-V_t)^2}{V_{td}^2}}$$

$$\frac{V_{inv}-V_t}{V_{td}} = \sqrt{\frac{Z_{p.u}}{Z_{p.d}}}$$

$$\frac{V_{td}}{V_{inv}-V_t} = \sqrt{\frac{Z_{p.d}}{Z_{p.u}}}$$

$$V_{td} = (V_{inv}-V_t)\sqrt{\frac{Z_{p.d}}{Z_{p.u}}}$$

$$V_{inv}-V_t = \cancel{\frac{V_{td}}{\sqrt{Z_{p.d}}}} \quad V_{td}\sqrt{\frac{Z_{p.u}}{Z_{p.d}}}$$

$$V_{inv}-V_t = V_{td}\sqrt{\frac{Z_{p.u}}{Z_{p.d}}}$$

$$V_{inv} = V_t + \frac{V_{td}}{\sqrt{\frac{Z_{p.d}}{Z_{p.u}}}}$$

$$= V_t + \frac{V_{td}}{\sqrt{\frac{Z_{p.d}}{Z_{p.u}}}}$$

$V_{inv} = 0.5V_{DD}$

$V_t = 0.2V_{DD}$

$V_{td} = -0.6V_{DD}$

$0.5 - 0.2 / 0.6$

$\left(\frac{S_1}{S_2}\right)^2$

$\frac{1}{4}$

$0.3 / 0.6$

$V_t = 0.2\,V_{DD}$, $V_{td} = -0.6\,V_{DD}$

$V_{inv} = 0.5\,V_{DD}$

$$0.5\,V_{DD} = 0.2\,V_{dd} + \frac{0.6\,V_{dd}}{\sqrt{Z_{p.u}/Z_{p.d}}}$$

$$0.5 - 0.2 = \frac{0.6}{\sqrt{Z_{p.u}/Z_{p.d}}}$$

$$0.3 = \frac{0.6}{\sqrt{Z_{p.u}/Z_{p.d}}}$$

$$\sqrt{\frac{Z_{p.u}}{Z_{p.d}}} = 2$$

$$\frac{Z_{p.u}}{Z_{p.d}} = 4/1$$

2.8 Pull-up to pull down ratio for an nMOS inverter driven through one & more pass transis

$$\frac{Z_{pu}}{Z_{pd}} = \frac{8}{1}$$

The i/p to inverter 2 comes from the o/p of inverter 1 but passes through one & more ~~pas~~ nMOS pass transistor used as switches

Connection of pass transistors in series will degrade the logic 1 level into inverter 2 so that the o/p will not be a proper logic 0 level.

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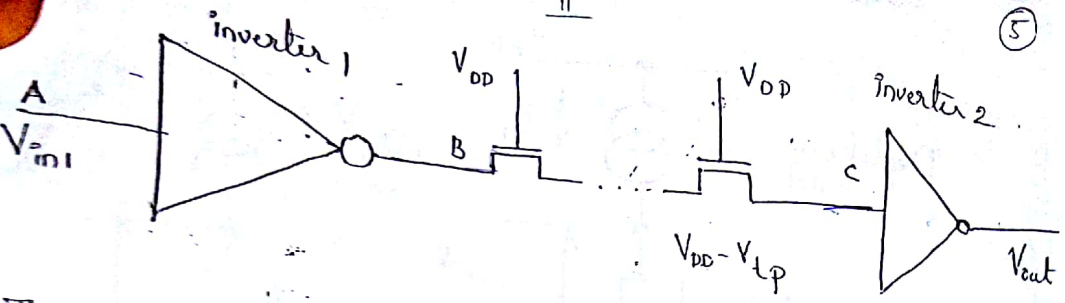
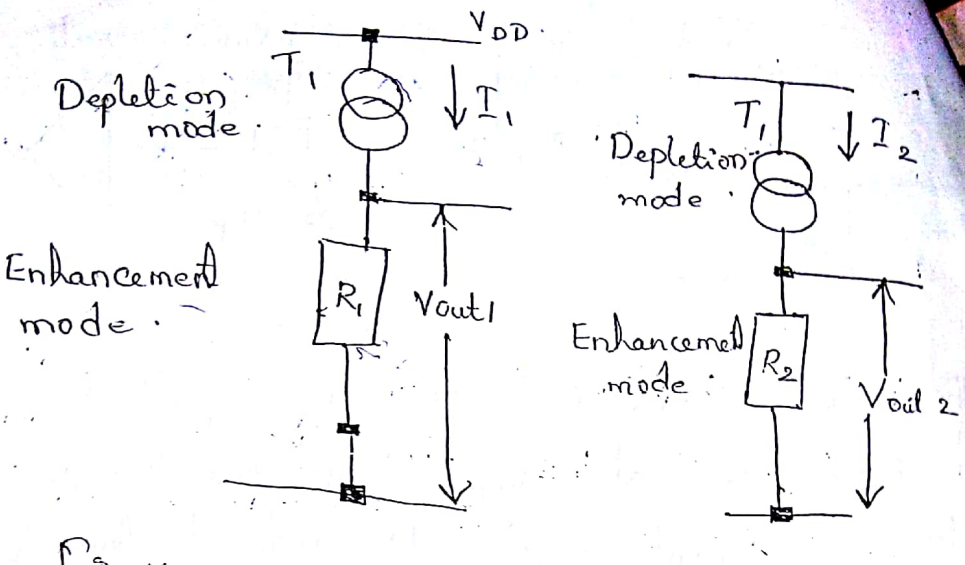


The Critical Condition is when point A is at 0 and B is thus at V_{DD}, but the Voltage into inverter 2 at point C is now reduced from V_{DD} by the threshold Voltage of the Series pass transistor. with all pass transistor gates connected to V_{DD} there is a loss of V_{tp}, however many are Connected in Series Since no static Current flows through them and there Can be no Voltage drop in the channels. Therefore the i/p Voltage at inverter 2 is

$$V_{in2} = V_{DD} - V_{tp}$$

where V_{tp} = threshold Voltage of pass transistor

Consider inverter 1 with input $= V_{DD}$. If the i/p is at V_{DD} then the p.d transistor T_2 is Conducting but with a low Voltage across it. So it is in resistive region represented by R_1. The p.u transistor T_1 is in Saturation



For the p. d transistor

$i/p = V_{DD}$

$$I_{ds} = K \frac{W_{p.d1}}{L_{p.d1}} \left((V_{DD} - V_t) V_{ds1} - \frac{V_{ds1}^2}{2} \right)$$

$$\therefore R_1 = \frac{V_{ds1}}{I_1} = \frac{1}{K} \frac{L_{p.d1}}{W_{p.d1}} \left(\frac{1}{V_{DD} - V_t - \frac{V_{ds1}}{2}} \right)$$

Note that V_{ds1} is small and $\frac{V_{ds1}}{2}$ can be ignored.

$$R_1 = \frac{1}{K} Z_{p.d1} \left(\frac{1}{V_{DD} - V_t} \right)$$

Now, for depletion mode p.u in saturation with $V_{gs} = 0$

$$I_1 = I_{ds} = K \frac{W_{p.u.1}}{L_{p.u.1}} \left(\frac{-V_{td}}{2} \right)^2$$

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The product

$$I_1 R_1 = V_{out\,1}$$

$$V_{out\,1} = I_1 R_1 = \frac{Z_{p.d.1}}{Z_{p.u.1}} \left(\frac{1}{V_{DD} - V_t}\right) \frac{\left(V_{td}\right)^2}{2}$$

Consider inverter 2 when i/p $= V_{DD} - V_{tp}$.

$$R_2 = \frac{1}{K} Z_{p.d.2} \frac{1}{(V_{DD} - V_{tp}) - V_t}$$

$$I_2 = K \cdot \frac{1}{Z_{p.u.2}} \frac{\left(-V_{td}\right)^2}{2}$$

$$V_{out\,2} = I_2 R_2 = \frac{Z_{p.d\,2}}{Z_{p.u.2}} \left(\frac{1}{V_{DD} - V_{tp} - V_t}\right)$$

$$I_1 R_1 = I_2 R_2$$

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} = \frac{Z_{p.u.1}}{Z_{p.d.1}} \frac{(V_{DD} - V_t)}{(V_{DD} - V_{tp} - V_t)}$$

Taking typical Values

$V_t = 0.2 V_{DD}$, $V_{tp} = 0.3 V_{DD}$.

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$$\frac{Z_{pu\cdot 2}}{Z_{p\cdot d\,2}} = \frac{Z_{p\cdot u\,1}}{Z_{p\cdot d_1}} \cdot \frac{0.8}{0.5}$$

$$\frac{Z_{p\cdot u\cdot 2}}{Z_{p\cdot d\cdot 2}} = 2\,\frac{Z_{p\cdot u\cdot 1}}{Z_{p\cdot d_1}} = \frac{8}{1}.$$

Summarizing for an nMOS inverter.

- An inverter driven directly from the o/p of another should have a $Z_{p\cdot u}/Z_{p\cdot d}$ ratio of $\geq 4/1$.
- An inverter driven through one or more pass trans should have a $Z_{p\cdot u}/Z_{p\cdot d}$ ratio of $\geq 8/1$.

2.9 Alternative forms of pull-up

Up to now we have assumed that the inverter circuit has a depletion mode pull-up transistor as its load. There are at least four possible arrangements

1) Load Resistance R_L :- This arrangement is not often used because of the large space requirem of resistors produced in a silicon substrate.

2) nMOS depletion mode transistor pull-up :-

a) Dissipation is high since rail to rail current flows when V_{in} = logical 1.

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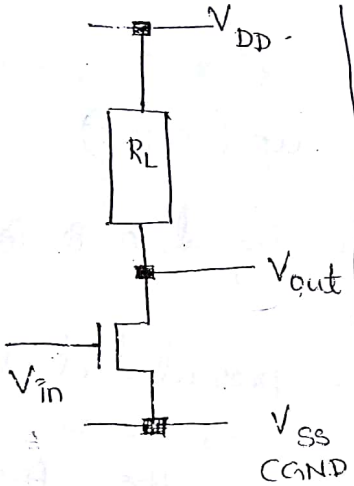
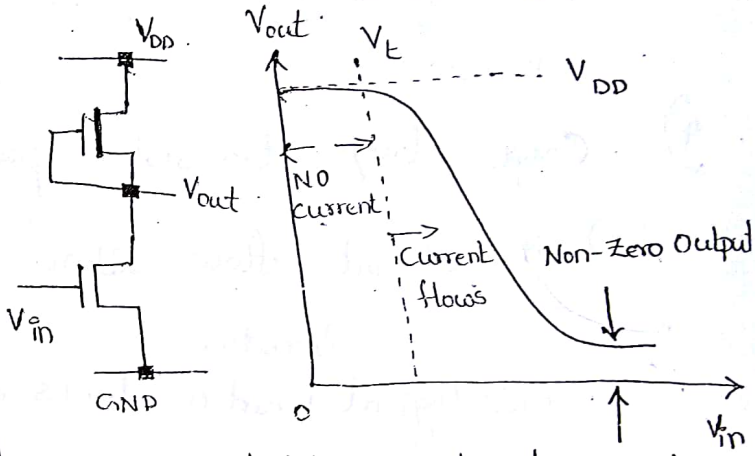
b) Switching of O/P from 1 to 0 begins when V_{in} exceeds V_t of P.d

c) when switching the output from 1 to 0, the P.u device is non-saturated initially and this presents lower resistance through which to charge capacitive loads.



Resistor pull-up



nMOS depletion mode transistor pull-up and transfer characteristic.

3) nMOS enhancement mode pull-up

a) Dissipation is high since current flows when V_{in} = logical 1 (V_{GG} is returned to V_{DD}).

b) V_{out} can never reach V_{DD} (logical 1) if $V_{GG} = V_{DD}$ as is normally the case.

c) V_{GG} may be derived from a switching source, for example one phase of a clock, so that dissipation can be greatly reduced.

d) If V_{GG} is higher than V_{DD} then an extra supply rail is required.

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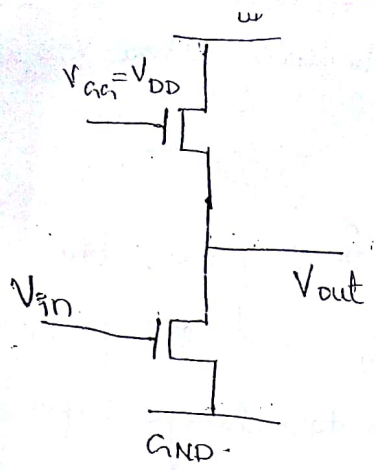
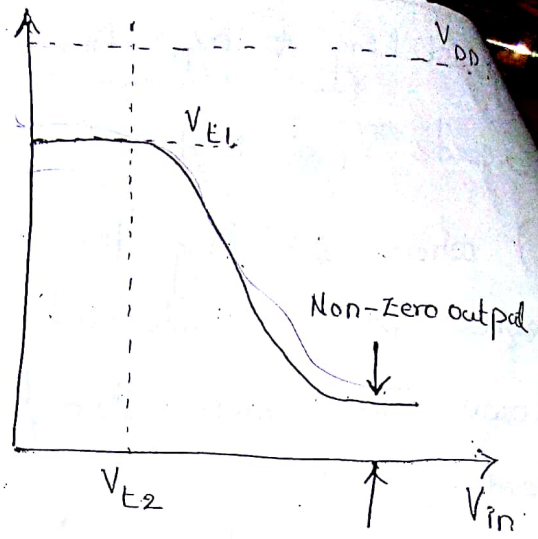


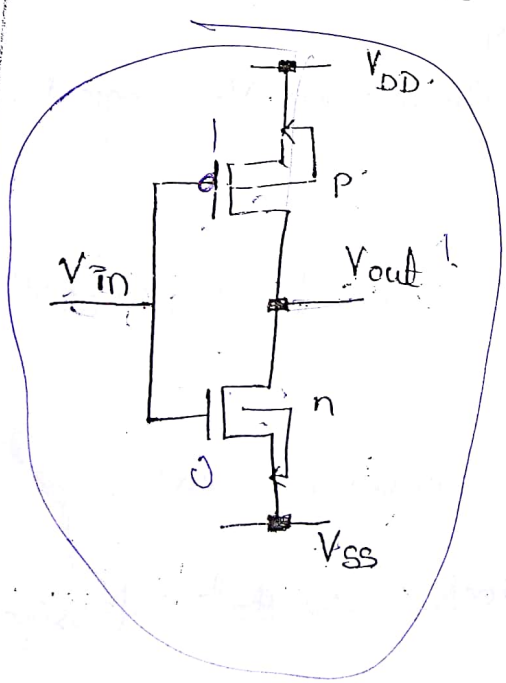


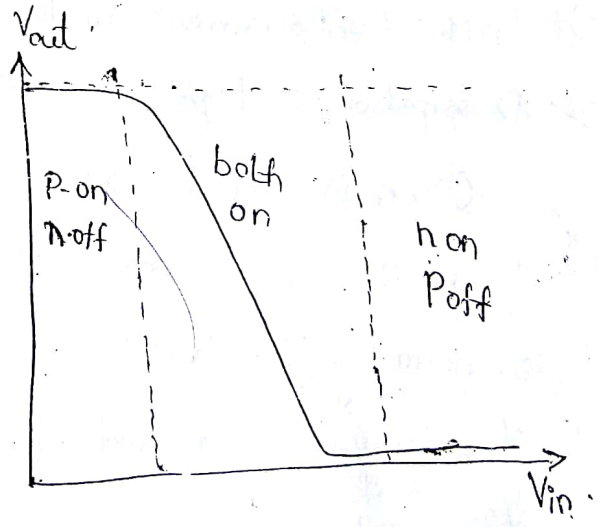
4) Complementary transistor pull-up (CMOS)

a) No current flow either for logical 0 or for logical 1 inputs.

b) full logical 1 and 0 levels are presented at the output.

c) For devices of similar dimensions the p-channel is slower than the n-channel device.





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The CMOS inverter I

$$I_{ds} = k\frac{W}{L}\left((V_{gs}-V_t)V_{ds} - \frac{V_{ds}^2}{2}\right)$$ in the resistive region.

$$I_{ds} = k\frac{W}{L}\frac{(V_{gs}-V_t)^2}{2}$$ in saturation region.

k = technology dependent parameter.

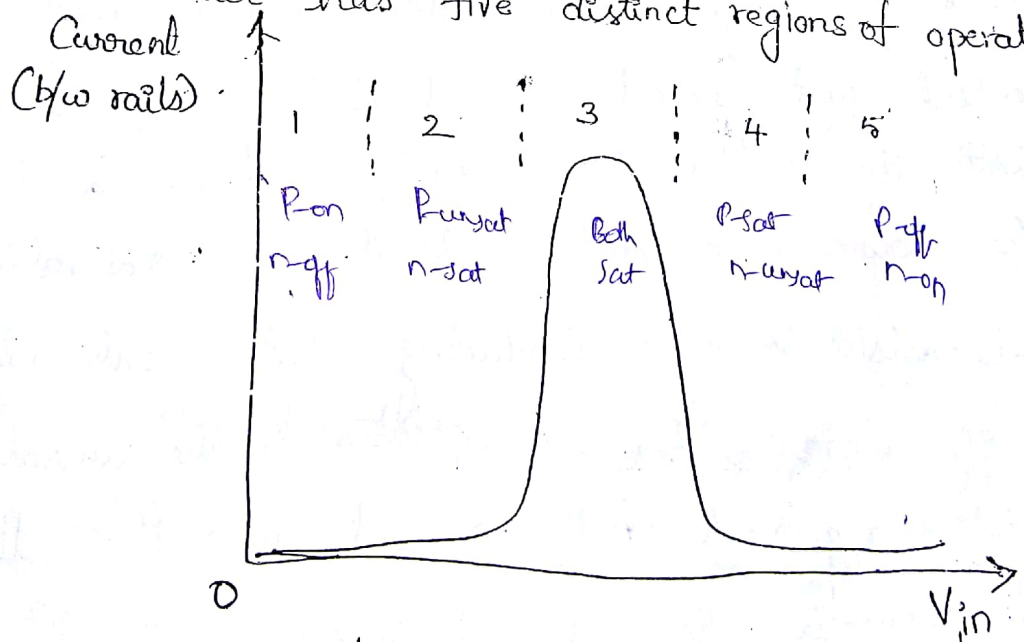
$$k = \frac{\epsilon_{ins}\epsilon_0 \mu}{D}$$

$$\beta = k\frac{W}{L}$$

$$\therefore I_{ds} = \frac{\beta}{2}(V_{gs}-V_t)^2$$ in saturation.

where W_n, L_n, W_p, L_p are the n and p transistor dimensions.

CMOS inverter has five distinct regions of operation.



β may be applied to both NMOS and PMOS transistors as follows

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$$\beta_n = \frac{\epsilon_{ins}\epsilon_0 \mu_n}{D} \frac{W_n}{L_n}$$

$$\beta_p = \frac{\epsilon_{ins}\epsilon_0 \mu_p}{D} \frac{W_p}{L_p}$$

In region 1 for which V_{in} = logic 0, we have the p-transistor fully turned on while the n-transistor is fully turned off. Thus no current flows through the inverter and the o/p is directly connected to V_{DD} through the p-transistor. A good logic 1 output is thus present at the output.

In region 5 V_{in} = logic 1, the n-transistor is fully on while the p-transistor is fully off. Again, no current flows and a good logic 0 appears at the o/p.

In region 2 the input voltage has increased to a level which just exceeds the threshold voltage of the n-transistor. The n-transistor conducts and has a large voltage b/w source and drain. So it is in saturation. The p-transistor is also conducting but with only a small voltage across it, it operates in the unsaturated resistive region. A small current now flows through the inverter from V_{DD} to V_{SS}.

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Region 4 is similar to region 2 but with the role of the p- and n transistors reversed. The current magnitudes in 2,4 regions are small and most of the energy consumed in switching from one state to the other is due to large current. Region 3 is the region in which the inverter exhibits gain and both transistors are in saturation.

The currents in each device must be the same since the transistors are in series

$$\boxed{I_{dsp} = -I_{dsn}}$$

$$I_{dsp} = \frac{\beta_p}{2}\left(V_{in} - V_{DD} - V_{tp}\right)^2$$

and

$$I_{dsn} = \frac{\beta_n}{2}\left(V_{in} - V_{tn}\right)^2$$

we can express V_{in} in terms of the β ratio and the other circuit voltages and currents

$$V_{in} = \frac{V_{DD} + V_{tp} + V_{tn}\left(\beta_n/\beta_p\right)^{1/2}}{1 + \left(\beta_n/\beta_p\right)^{1/2}}$$

Since both transistors are in saturation they act a current sources so that the equivalent ckt in this region is two current sources in series b/w V_{DD} and V_{SS}.

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If $\beta_n = \beta_p$ and if $V_{tn} = -V_{tp}$

then $V_{in} = 0.5\, V_{DD}$

$V_{in} = V_{out} = 0.5\, V_{DD}$.

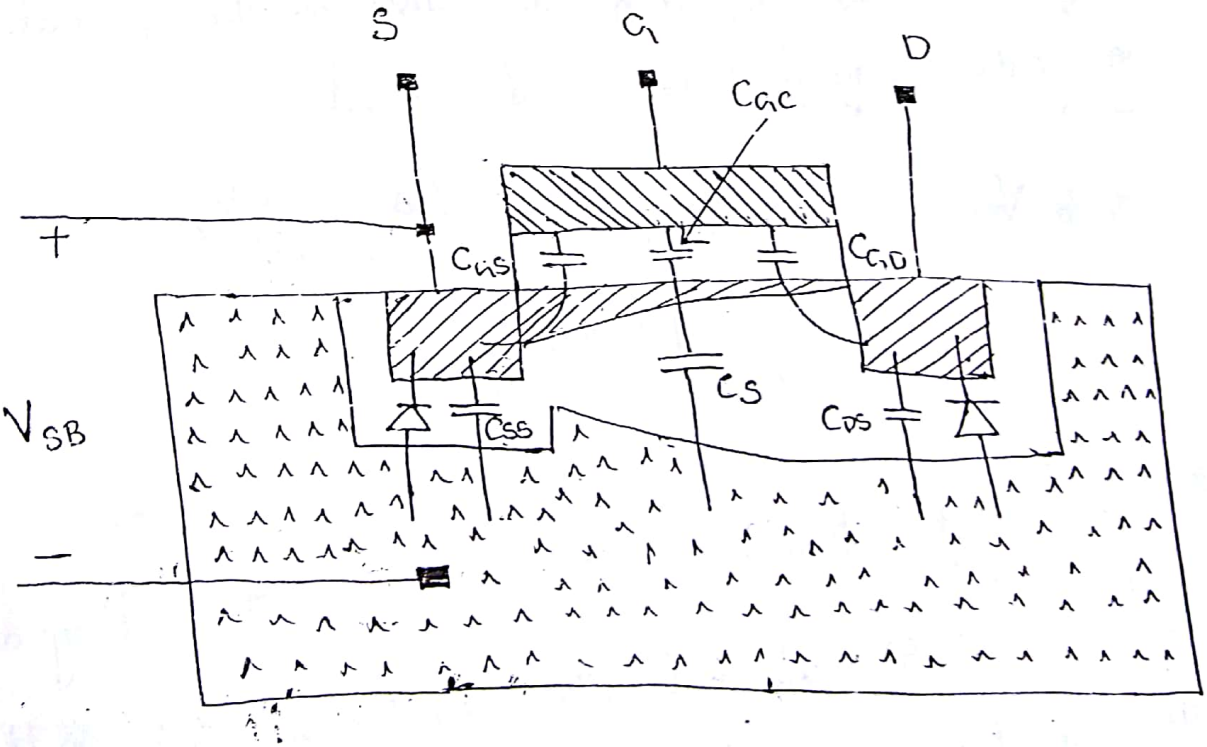
$V_{in} = \frac{V_{DD}}{2}$

for $\frac{\beta_n}{W_n} = \frac{\beta_p}{W_p}$ $\quad \frac{\mu_p W_p}{L_p} = \frac{\mu_n W_n}{L_n}$

but the mobilities are unequal and thus it is necessary for the width to length ratio of the p-device to be two to three times that of the n-device.

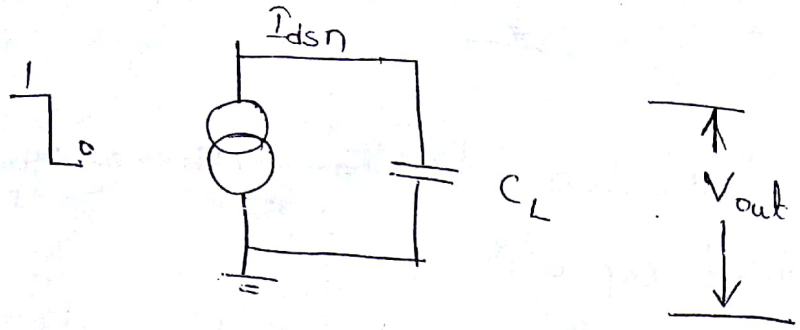
$$W_p/L_p = 2.5\, W_n/L_n.$$

2.11 MOS transistor circuit model



$$\tau_r = \frac{3C_L}{\beta_p V_{DD}}$$

Fall time



$$\tau_f = \frac{3C_L}{\beta_n V_{DD}}$$

Power Dissipation

Two types
1) Static
2) Dynamic.

1) Static power dissipation:
Static power dissipation is due to the leakage current drawn from the power supply.

2) Dynamic power dissipation:
Dynamic Power dissipation is due to switching transient current and charging and discharging of

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load capacitance II

Static Power Dissipation

1) Causes of static power dissipation are

{underline chesinavi
Gurthu
Pettuko}

2) Subthreshold conduction through OFF transistors.
3) Tunneling current through gate oxide.
4) Leakage through reverse biased diodes.
Contention current in ratioed circuits.

$$P_{static} = I_{static} \cdot V_{DD}$$

I_{static} is the current flowing supply to ground in absense of switching.

Dynamic Power Dissipation

Causes of dynamic power.

1) Charging and discharging of load capacitances.
2) Short circuit current while both PMOS and NMOS networks are partially ON.
3) for a square wave i/p of frequency f_p and input V_{in}.

$$P_{dynamic} = C V_{DD}^2 f_p$$

Short Circuit Power Dissipation

- It indicates the power dissipation due to short circuit current

$$P_{sc} = \frac{K}{12}(V_{DD} - V_t)^3 \frac{t_{rf}}{t_p}$$

t_p is Period of input waveform.

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t_{rf} is rise time of input wave form

K Constant.

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