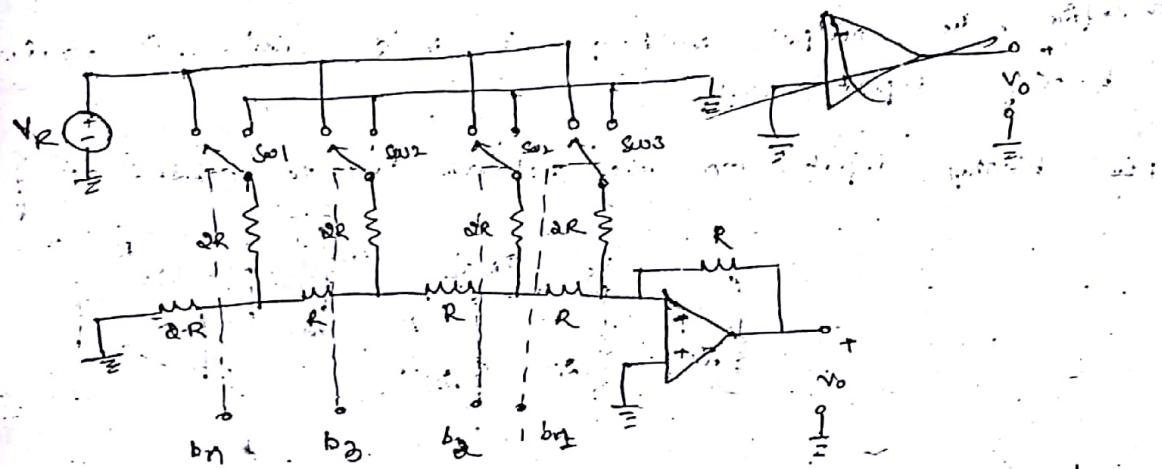


values of resistors; the loading effect may occur.  
 3. The finite resistance of the switches disturbs the binary weighted relationship among the various currents, particularly for the most significant bit positions, where the current setting resistances are smaller.  
 All these drawbacks, especially the requirements of wider range of resistors restrict the use of binary weighted resistor DACs below 8-bits.

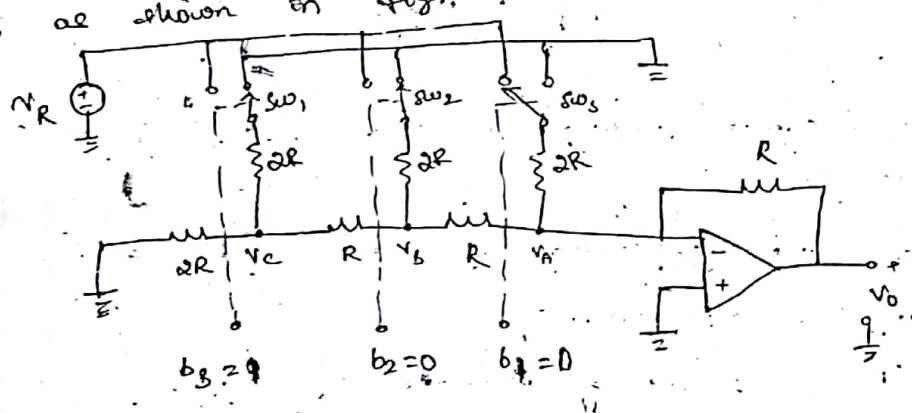
# ①

### R/2R ladder network D/A converter:

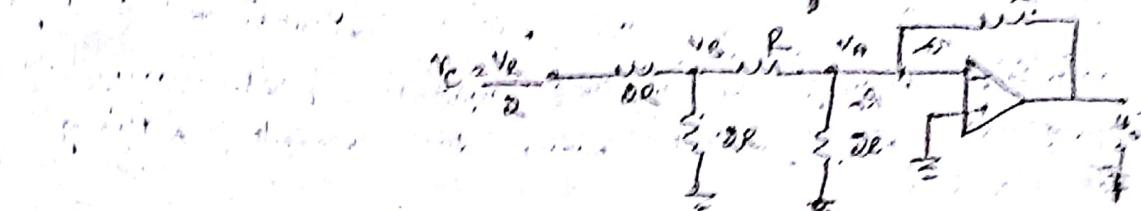
In this type, reference voltage is applied to one of the switch positions, and other switch position is connected to ground as shown in fig.



Let us consider 3-bit R/2R ladder D/A with binary input 001, as shown in fig.

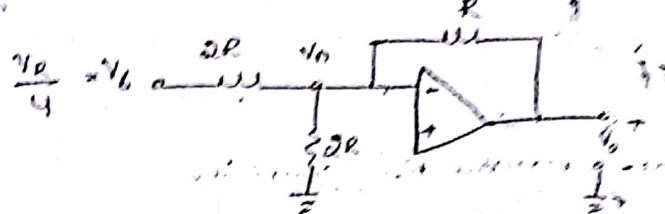


Deducting above resistors, to the left by 100 ohms

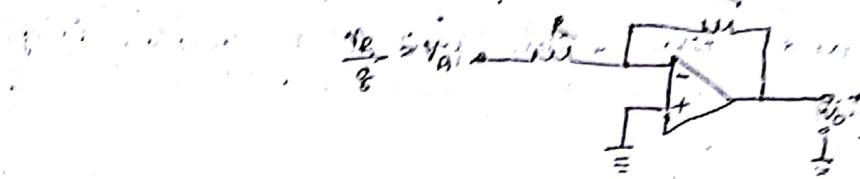


for the output voltage is  $V_{out} = \frac{V_{in}}{2} + \frac{V_{in}}{100}$

if the input voltage is 100 mV, then the output voltage is 50 mV.

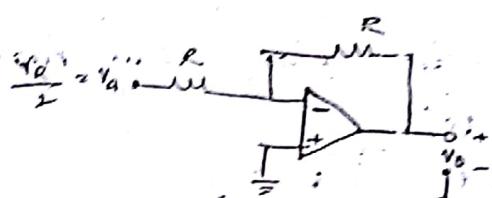
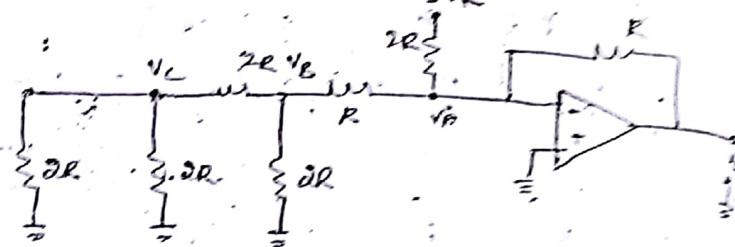


and for the output voltage is  $V_{out} = \frac{V_{in}}{2} + \frac{V_{in}}{100}$



Therefore, the output voltage is  $50\text{mV}$  which is equivalent to binary input 101.

For binary input 100 the network can be reduced as follows:



Therefore, the output voltage is  $50\text{mV}$  which is equivalent to binary input 100.

In general, the expression for  $V_{out}$  can be obtained as,

let  $I_{out}$  = op-amp current

$R_f$  = feedback resistance of op-amp

$$V_o = \frac{I_{out}}{R_f} R_f$$

Note:  $I_{out}$  = current resolution  $\times D$

$$V_o = -(\text{current resolution} \times D) R_f$$

$$= -(\text{current resolution} \times D) D$$

The coefficient of  $D$  is the voltage resolution and can be called as simple resolution.

$$\therefore V_o = \text{resolution} \times D$$

on time of digital circuit elements, it can be written as,

$$V_o = -\left[\frac{V_R}{R} \times \frac{1}{2^n} R_f\right] \times D$$

The resolution of R/2R ladder type DAC with voltage  $V_o$  is

$$\text{resolution} = \left[\frac{1}{2^n} \times \frac{V_R}{R}\right] \times R_f$$

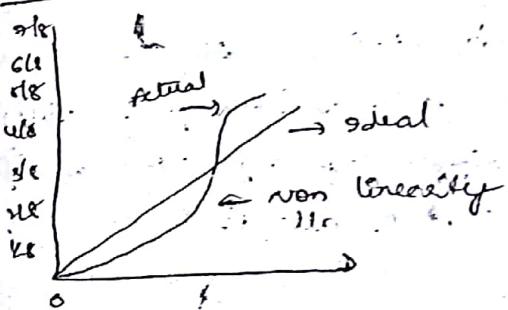
### Advantages of R/2R ladder DAC's:

1. Easier to build accurately as only two precision metal film resistors are required.
2. Number of bits can be expanded by adding more sections of same R/2R values.

### Errors of R/2R DAC:

There are mainly three errors in DAC: linearity, offset and gain errors.

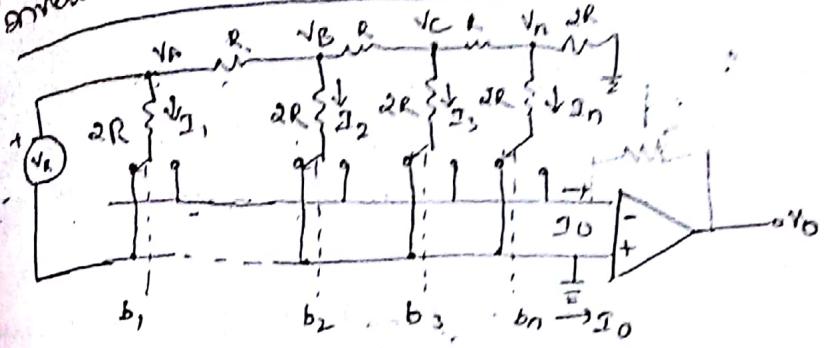
#### Linearity error:



The error is defined as amount by which the actual  $V_o$  differs from ideal straight line  $V_o$ .

It is mainly due to errors in current source resistance values.

### Inverted R-2R Ladder DAC



①

In R-2R ladder type of DAC the current flowing through the resistor changes as input data changes. Power dissipation causes heating and non-linearity of DAC arise due to varying power dissipation values corresponding to bit patterns. This becomes a serious limitation as word length increases. This is eliminated in inverted R-2R ladder D/A converter.

As shown in fig. the bit position of each of subsequent MSBs and LSBs are interchanged. Each binary input is connected through the switch to either ground or to inverting input terminal of op-amp, which is at virtual ground. Since both the positions of switch  $b_i$  are at ground potential i.e. actual or virtual ground, the current flow through any resistor is constant and it is independent of input binary bit value.

These currents can be represented as

$$I_1 = \frac{V_R}{2R} \Rightarrow V_A = V_R$$

$$I_2 = \frac{(NR/2)}{2R} = \frac{VR}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{(VR/4)}{2R} = \frac{VR}{8R} = \frac{I_1}{4}$$

$$I_n = \frac{(VR/2^{n-1})}{2R} = \frac{I_1}{2^{n-1}}$$

The output voltage  $V_0$  is given by

$$V_0 = -I_0 \times R_f$$

$$= -R_f(I_1 + I_2 + I_3 + \dots + I_n)$$

$$= -\frac{VR R_f}{R_1} (b_1^{-1} + b_2^{-2} + \dots + b_n^{-n})$$

Stability: The performance of converter changes with temperature, age and power supply variations. So, all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges. These parameters represent the stability of the converter.

### Basic Conversion Techniques:

There are mainly two techniques used before analog to digital conversion:

1. Binary weighted resistor D/A converter.

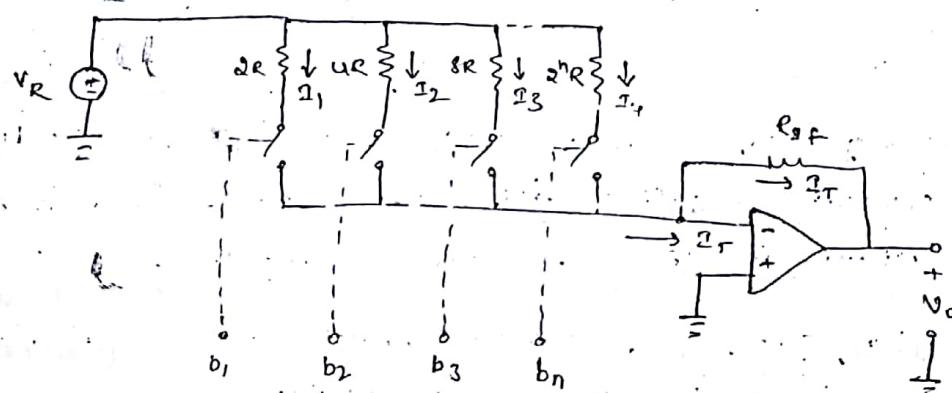
2. R/2R ladder D/A converter.

In these techniques, the current resistors are used to generate n binary weighted currents. These currents are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage equivalent to the digital input. Therefore, such digital to analog converters are called current driven DAC's.

③

### Binary weighted resistor D/A converter:

The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage  $V_R$  via current scaling resistors  $2R, 4R, 8R, \dots, 2^n R$  as shown:



As shown in fig. switch positions are controlled by the digital inputs. When digital input is logic 1, it connects the corresponding resistance to the reference voltage  $V_R$ ; otherwise it leaves resistor open. Therefore,

$$\text{For on-switch, } I = \frac{V_R}{R} \text{ and}$$

$$\text{for off-switch, } I = 0$$

Here operational amplifier is used as a summing amplifier. Due to high input impedance of op-amp, bypassing current will flow through  $R_f$ . Hence the total current through  $R_f$  can be given as

$$I_T = I_1 + I_2 + I_3 + \dots + I_n$$

The o/p voltage is the voltage across  $R_f$  and is given as

$$\begin{aligned} V_o &= -I_T R_f \\ &= -(I_1 + I_2 + I_3 + \dots + I_n) R_f \\ &= -\left[ b_1 \frac{V_R}{R} + b_2 \frac{V_R}{2R} + b_3 \frac{V_R}{4R} + \dots + b_n \frac{V_R}{2^n R} \right] R_f \\ &= -\frac{V_R}{R} R_f \left( b_1 \bar{z}^1 + b_2 \bar{z}^2 + b_3 \bar{z}^3 + \dots + b_n \bar{z}^n \right) \end{aligned}$$

when  $R_f = R$ ,  $V_o$  is given as

$$V_o = -V_R \left[ b_1 \bar{z}^1 + b_2 \bar{z}^2 + b_3 \bar{z}^3 + \dots + b_n \bar{z}^n \right]$$

equation indicates that the analog output voltage is proportional to the input digital word.

### Drawbacks:

1. wide range of resistor values are required. For 8-bit DAC, the resistors required are  $\bar{z}^1, \bar{z}^2 R, \dots$  and  $\bar{z}^8 R$ . Therefore the largest resistor is 128 times the smallest one.
2. This wide range of resistor values has restrictions on both higher and lower ends. It is impractical to fabricate large values of resistors in IC and voltage drop across such a large resistor due to the bias current also affects the accuracy. So smaller

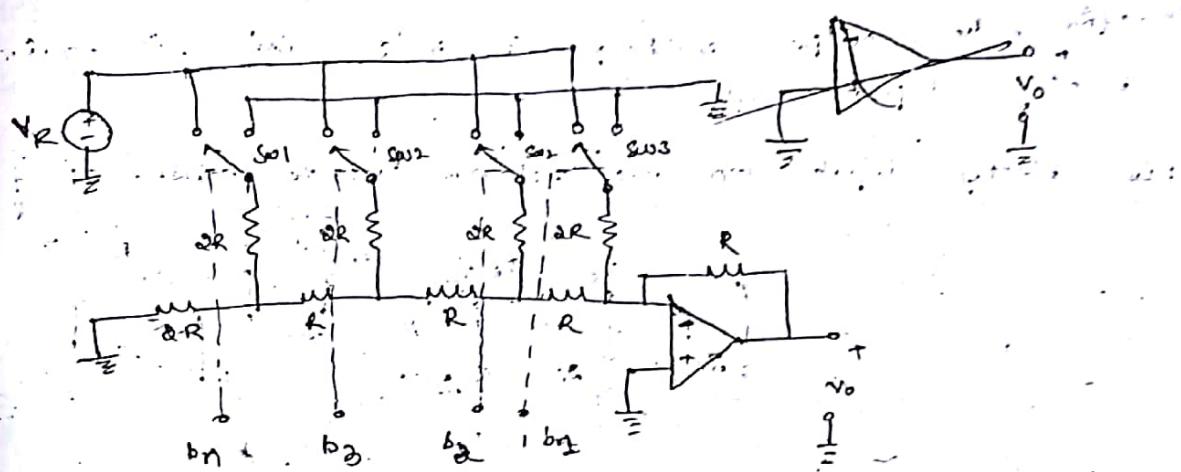
values of resistors; the loading effect may occur.  
 3. The finite resistance of the switches disturbs the binary weighted relationship among the various currents, particularly in the most significant bit positions, where the current setting resistances are smaller.

All these drawbacks, especially the requirements of wider range of resistors restrict the use of binary weighted resistor DACs below 8-bits.

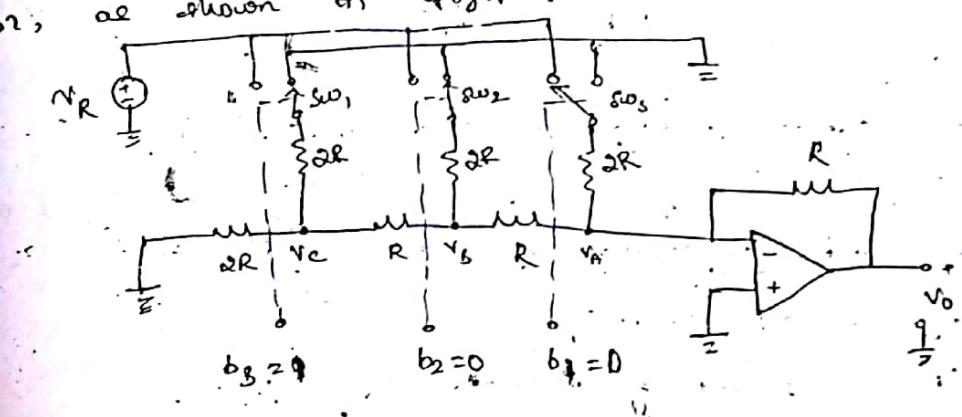
Fig 1

### R/2R ladder network D/A converter:

In this type, reference voltage is applied to one of the switch positions, and other switch positions are connected to ground as shown in fig.



Let us consider 3-bit R/2R ladder DAC with binary input 002, as shown in fig.

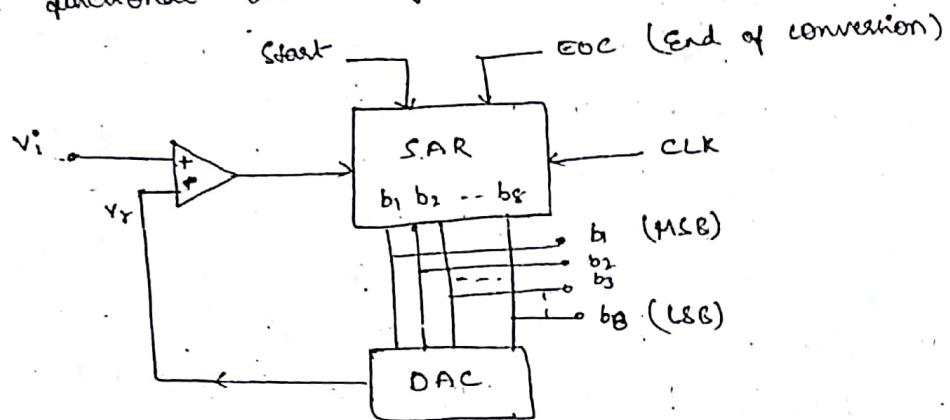


## Successive approximation ADC

The conversion time is maintained constant and it is made proportional to no. of bits in digital output.

This ADC is based on a very efficient code searching strategy called binary search. The basic principle of this ADC is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with MSB.

The functional block diagram is shown.



The circuit employs a successive approximation register (SAR) which finds the required value of each successive bit by trial and error method. The output of SAR is fed to n-bit DAC. The analog output equivalent of DAC is applied to ~~the~~ inverting terminal of comparator, while other input of comparator is connected to unknown analog input voltage  $V_i$ . The comparator output is used to activate the successive approximation logic of SAR.

When the START command is applied, the SAR sets the MSB of the digital signal, while other bits are made zero, so that trial code becomes 1 followed by zeros. For example, for an 8-bit ADC the trial code is 10000000. The output of SAR is compared converted into analog equivalent  $V_r$  and gets compared with input signal  $V_i$ . If  $V_i$  is greater than DAC output, then trial code 10000000 is less than the exact digital value. The MSB is retained as 1 and next significant bit is made 1 and testing is repeated. If analog input  $V_i$  is now less than DAC output, then value of 11000000 is greater than exact digital equivalent. Therefore the comparator rewrites the second MSB to 0 and proceeds to the next MSB. This process is repeated for all remaining.

⑤

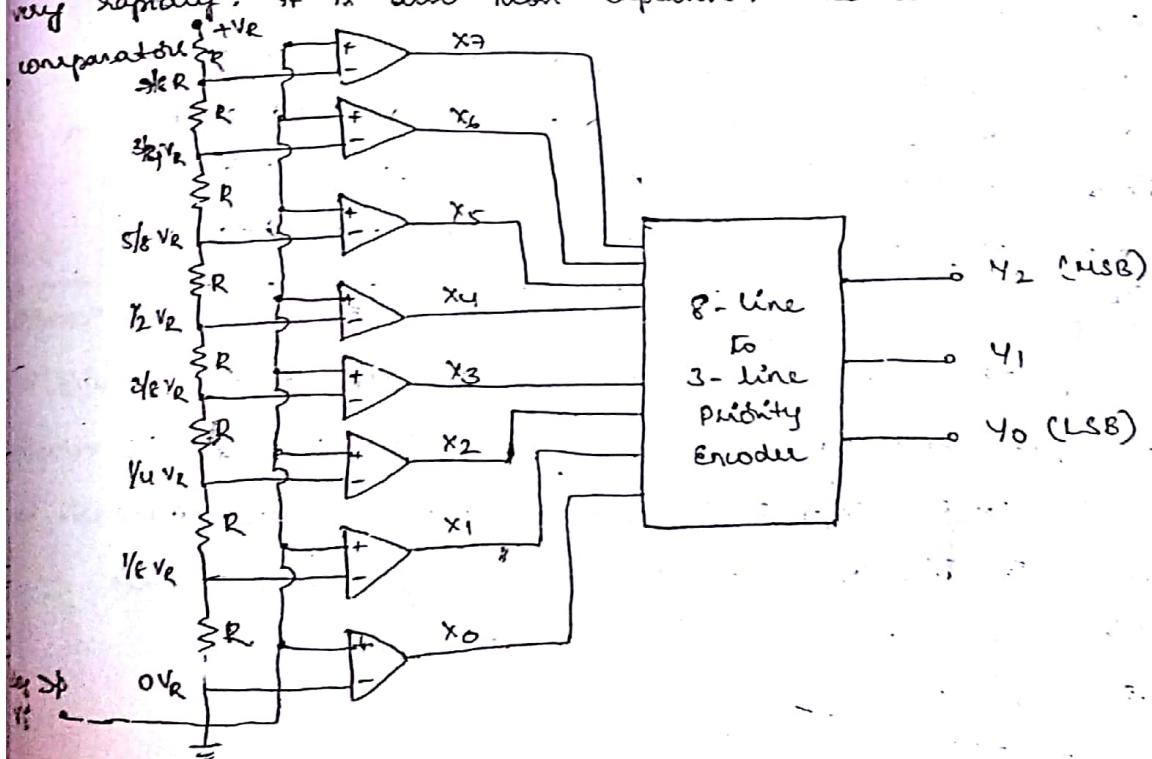
lower bits in sequence until all the bit positions are tested. The ZOC signal is sent out when all the bits are scanned and the value of DAC output just covers  $V_i$ .

correct digital representation	SAR output $V_i$ at different stages	comparator output
1010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

for an 8-bit ADC, it requires 8 pulses to compute the output irrespective of value of analog input).

### Parallel comparator ADC (Flash Type)

The parallel comparator ADC, is also known as flash ADC, finds application when very high speed is required. The conversion is done very rapidly. It is also most expensive, since it uses a large no. of comparators.



## Ch 19th Interfacing:

Interfacing; many times it becomes necessary to connect the output of one circuit (or system) to the input of another circuit (a) & the task of connecting the two circuits by suitable means is termed as interfacing. If the two circuits are with similar logic gates, then interfacing characteristics, perhaps a direct connection between them is possible, such as direct connection cannot be used between the two having different logical characteristics.

In such a situation, there is need of interface circuit, which would convert the output of one circuit to the input of other circuit.

Some basic concepts for interfacing are as follows:

1. power supplies: for interfacing between two different power supplies, there must be enough voltage & current available. For example, if the first power supply is 12VDC & 1A, then the second power supply must be 12VDC & 1A (with 1A current).
2. logic levels: property apart from the outputs, the outputs of one logic family differ from the other logic families. For example, if the output of one logic family is 1V, then the output of another logic family may be 5V. So, the logic levels should be V<sub>CC</sub>, V<sub>DD</sub> rather than 0 & V<sub>CC</sub>.

### 3. Power:

Power requirement is often a problem when two different logic families are connected. It is not a problem when both the logic families have same power requirements. On the other hand, if one logic family requires more power than the other, then the power requirement will be the sum of both the logic families. For example, if one logic family requires 12VDC & 1A, and the other logic family requires 5VDC & 0.5A, then the total power requirement will be 12VDC & 1.5A.

### 4. Capacitive loading:

Load capacitors, resistors both delay and power dissipation of logic circuits. Resistors or delay are especially noticeable with HC as they are high resistance. The output load capacitance, lower power dissipation but output voltage swing remains same. The higher the load, the smaller the output voltage swing. Between the high and low levels is smaller.

④

the input and output currents for different CMOS and TTL series, for a supply voltage of 5V.

parameter	CMOS			TTL			
$V_{IH}$ (min)	4.000	94HC/HCT	94AC/ACT	74	74LS	74AS	74ALS
$I_{IH}$ (max)	1mA	1mA	1mA	10mA	10mA	200mA	200mA
$V_{IL}$ (max)	1mA	1mA	1mA	1.6mA	0.4mA	2mA	100mA
$I_{OL}$ (max)	0.4mA	1mA	2mA	0.4mA	0.4mA	2mA	100mA
$S_{OL}$ (max)	0.4mA	1mA	2mA	16mA	8mA	20mA	8mA

### TTL during CMOS

Let it be assumed that a CMOS logic gate is to be driven by a TTL gate. We know that CMOS and TTL are two different logic families. Hence an interface circuit becomes necessary.

Hence the output voltage and current of TTL gate must be made compatible with voltage and current requirements of CMOS logic gate.

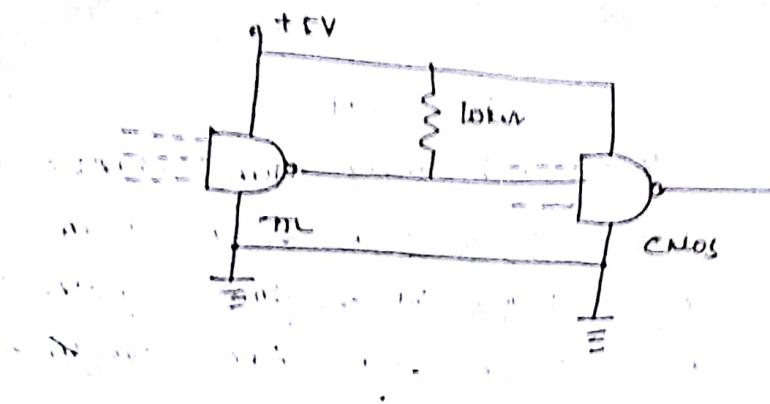
The input currents for CMOS are very low as compared to output current capabilities of any TTL device. Hence TTL can certainly meet the input current requirements of CMOS.

Next, compare the output voltages of TTL series with input voltage requirements of CMOS.

$V_{OH}$ (min)	2.0	2.7	2.7	2.5	2.5	2.5	9	TTL
$V_{OL}$ (max)	0.4	0.5	0.5	0.5	0.4	0.5		
$V_{IH}$ (min)	3.5	3.5	2.0	3.5	0.0	0	9	CMOS
$V_{IL}$ (max)	1.5	1.5	0.8	1.0	0.8	0		

We see that  $V_{OH}$  (min) of any TTL device is very low when compared with  $V_{IH}$  (min) of different CMOS series. Hence it is necessary to increase the output voltage level of TTL to meet the input voltage requirements of CMOS.

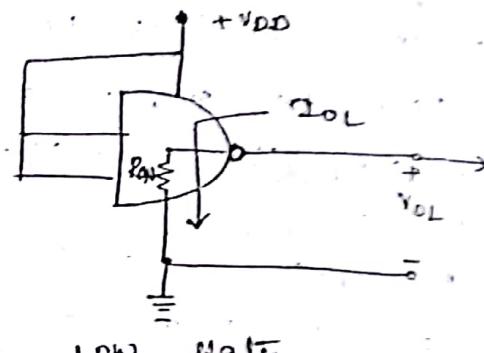
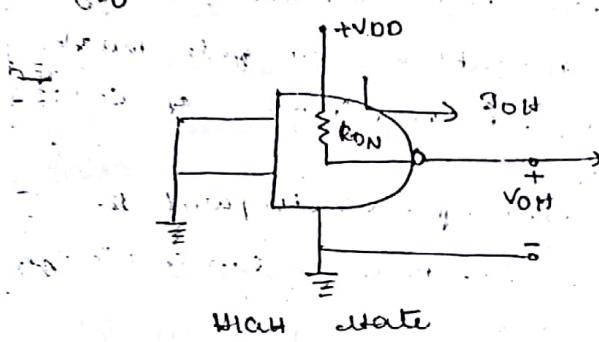
The interface circuit used after deriving a color decoder from TTL device is



other '10k' resistor acts as pull-up resistor. It is connected between output of TTL device and +5V source. Due to this resistor, the output of TTL device will appear at V<sub>O</sub> in this case and meet input voltage requirement of CMOS circuit.

### \* CMOS driving TTL

For CMOS inverter, when the input to the gate is 0V, the gate output is almost equal to V<sub>DD</sub> with a resistance R<sub>ON</sub>. In HIGH output state, the CMOS gate output acts like a voltage source V<sub>DD</sub> with a source resistance R<sub>ON</sub>.



When input to inverter is +VDD, gate output is 0V, with node connected to ground. It acts as a current sink.

CMOS outputs are adequate to meet the input voltage requirements of TTL in HIGH state and also required amount of input current to TTL. Hence no problem for HIGH state.

Considering LOW state, it is seen that TTL/HCT series device can sink upto 1mA. The input current requirement of TTL in LOW state is quite high ranging from 100μA to 2mA.

So TTL/HCT series device can drive not more than one load of any value.

A 4000B will have such low output current capability. It cannot drive even one TTL device of any value.

## MOSFET Logic

16

Digital circuits with MOSFETs can be grouped into three categories:

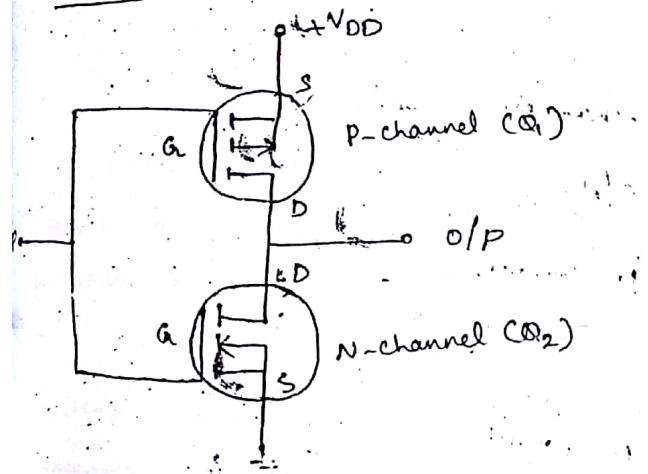
1. PMOS - uses only P-channel enhancement MOSFETs.
2. NMOS - uses only N-channel enhancement MOSFETs.
3. CMOS - uses both P- and N-channel devices.

PMOS and NMOS digital ICs are economical than CMOS ICs because they have greater packing density than CMOS. NMOS has twice the packaging density than PMOS. Further NMOS can operate at about three times faster than their PMOS counterparts. This is because NMOS has faster moving current carriers (electrons) whereas PMOS has slower moving current carriers (holes). CMOS has the greatest complexity and lowest packaging density; however it has important advantage of high speed and much lower power dissipation. NMOS and CMOS are widely used in the digital ICs but PMOS ICs are no longer part of new designs.

## CMOS:

CMOS circuits contain both NMOS and PMOS devices to speed the switching at capacitive loads. It consumes less power and can be operated at high voltages, resulting in improved noise immunity.

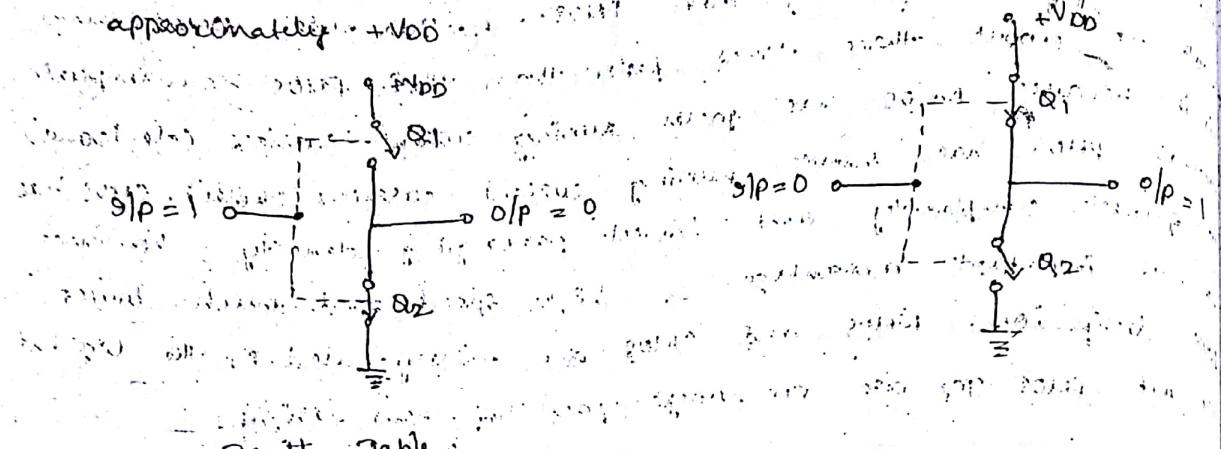
### CMOS inverter:



and drain are connected together as common o/p.

Fig. shows the basic CMOS inverter circuit. It consists of two MOSFETs in series in such a way that the P-channel device has its drain connected to +VDD (a positive voltage) and the N-channel device has its source connected to ground. The gates of the two devices are connected together as common o/p.

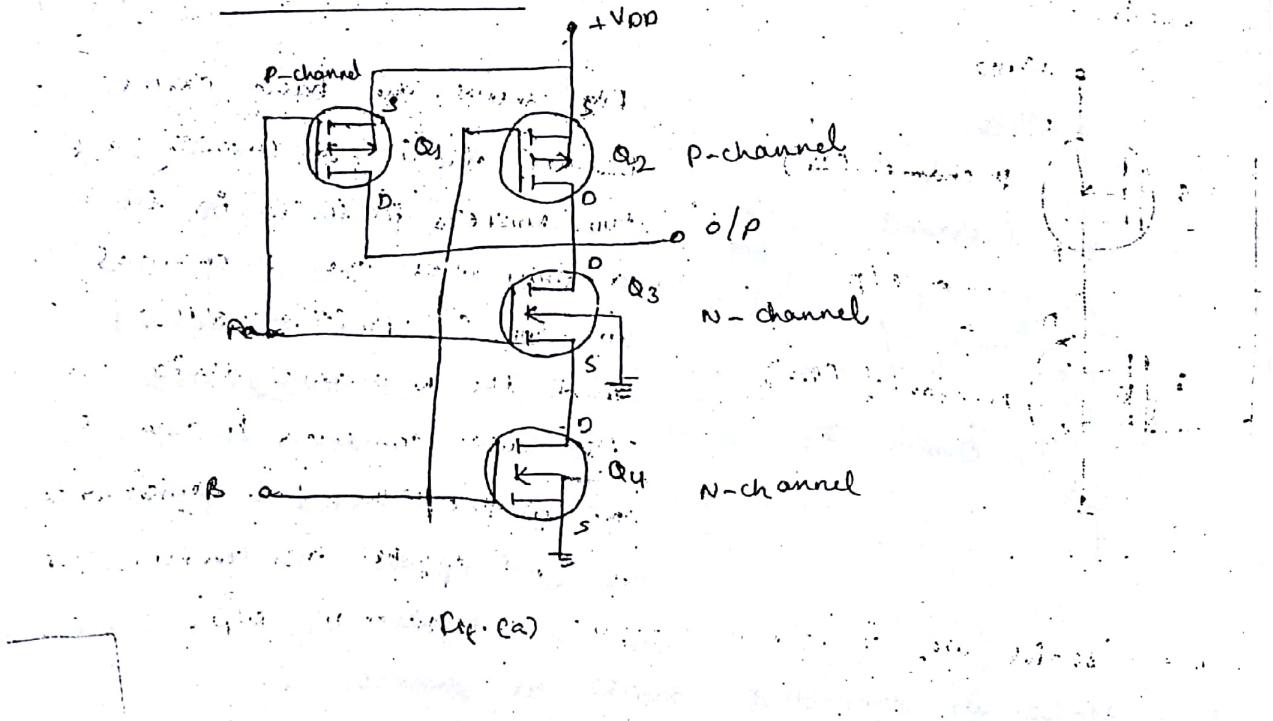
When input is High, the gate of  $Q_1$  (P channel) is relative to the source of  $Q_1$  i.e.  $V_{GS1} = 0V$ . Thus  $Q_1$  is ON. On the other hand, the gate of  $Q_2$  (N channel) is at  $+VDD$ , its source is  $V_{GS2} = +VDD$ . Thus  $Q_2$  is OFF. This will make  $V_{OUT} = 0V$ . When input is Low, the gate of  $Q_1$  (P channel) is at a negative potential relative to its source while  $Q_2$  has an approximate potential relative to its source. This produces output  $V_{OUT} = +VDD$ .



Truth Table:

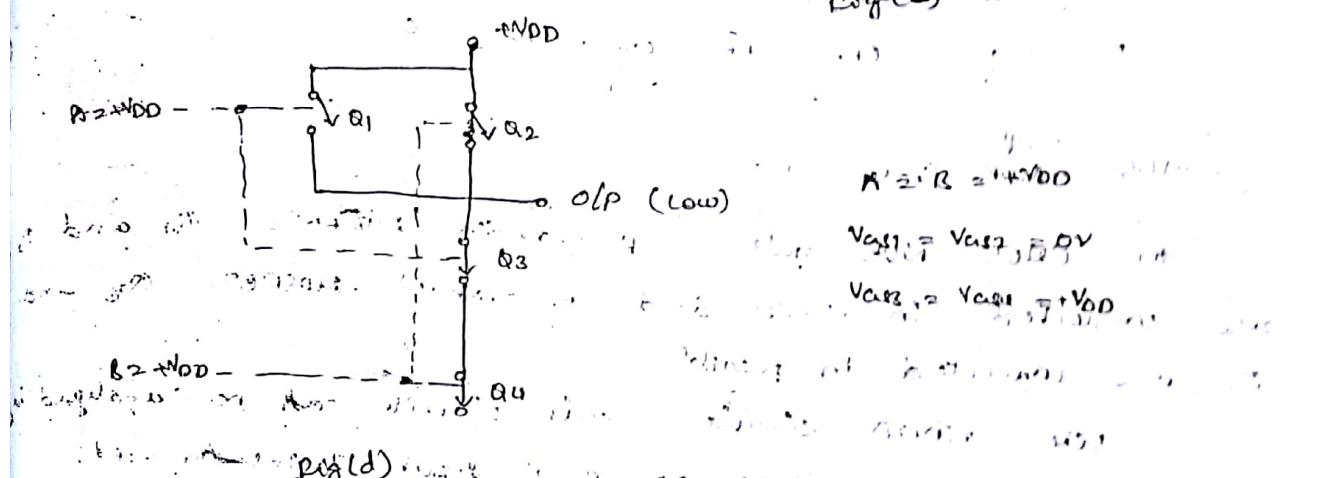
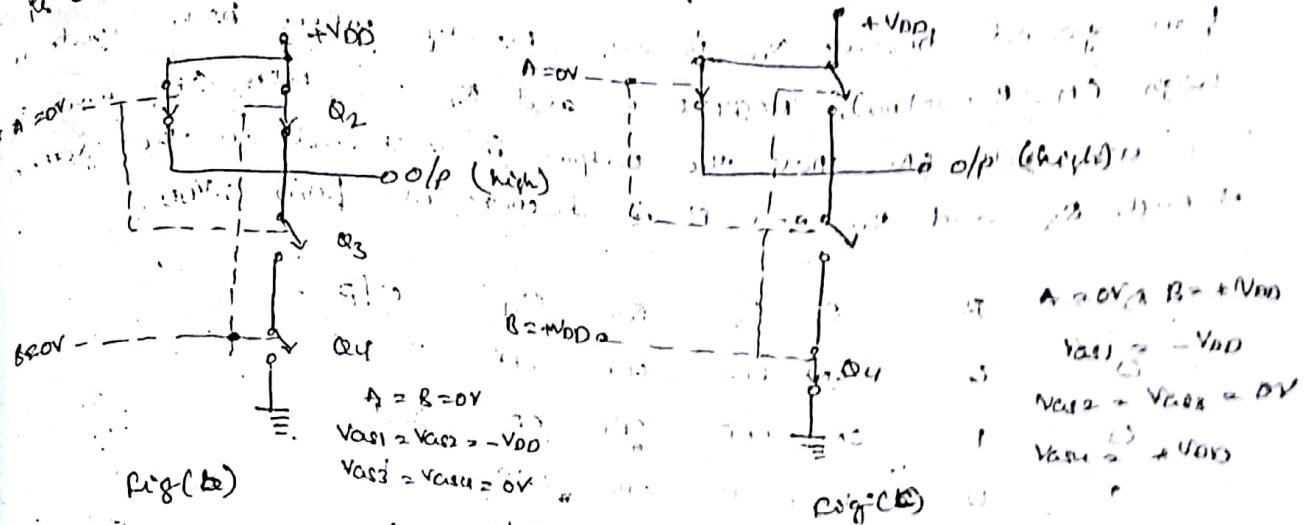
A	$Q_1$	$Q_2$	O/P
High	ON	OFF	Low
Low	OFF	ON	High

CMOS NAND Gate



(Fig. 2a)

shows CMOS 2-input NAND gate, consisting of p-channel MOSFETs  $Q_1$  and  $Q_2$ , connected in parallel, and N-channel MOSFETs  $Q_3$  and  $Q_4$ , connected in series. The p-channel MOSFET  $Q_1$  is ON when its gate voltage is negative with respect to its source terminal, N-channel MOSFET  $Q_3$  is ON when its gate voltage is positive with respect to its source terminal.



Fig(a) shows the equivalent switching circuit. Both the inputs are low. Here the gates of both P-channel MOSFETs are negative with respect to their source, since the sources are connected to +VDD. Thus Q<sub>1</sub> and Q<sub>2</sub> are both ON. Since the gate-to-source voltage of Q<sub>3</sub> and Q<sub>4</sub> (N-channel MOSFETs) are both OFF, these MOSFETs are OFF. The output is therefore connected to +VDD (HIGH) through Q<sub>1</sub> and Q<sub>2</sub> and is disconnected from ground as shown in fig.(b).

Dig-Cap switchs the equivalent switching circuit when  $A = 0$ ,  $B = +VDD$ . In this case,  $Q_1$  is on because  $V_{GS1} = -VDD$  and  $Q_2$  and  $Q_3$  are off because  $V_{GS2} = +VDD$ . MOSFETs  $Q_2$  and  $Q_3$  are off because their gate-to-source voltages are 0V. Since  $Q_1$  is on and the output is connected to  $+VDD$  and it is disconnected from ground. When  $A = +VDD$  and  $B = 0$ , the situation is opposite. The output is connected to  $+VDD$  through  $Q_3$  and it is disconnected from ground through  $Q_2$  because  $Q_2$  is off. Finally when both inputs are high ( $A = B = +VDD$ ), MOSFETs  $Q_1$  and  $Q_2$  are both OFF and  $Q_3$  and  $Q_4$  are both ON. Thus, the output is connected to the ground through  $Q_3$  and  $Q_4$  and it is disconnected from  $+VDD$ .

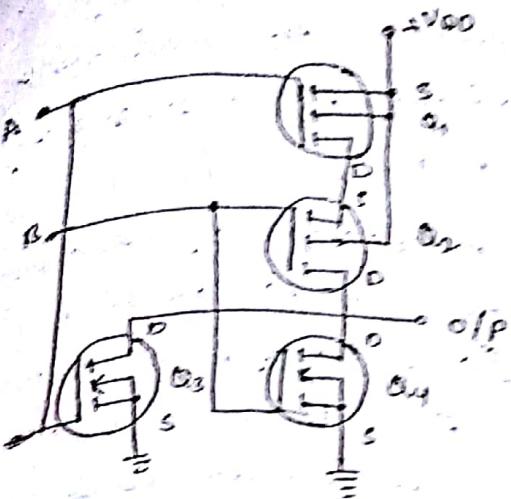
	$A$	$B$	$Q_1$	$Q_2$	$Q_3$	$Q_4$	O/P
	0	0	ON	ON	OFF	OFF	1
	0	1	ON	OFF	OFF	ON	0
	1	0	OFF	ON	ON	OFF	1
	1	1	OFF	OFF	ON	ON	0

#### CMOS NOR Gate:

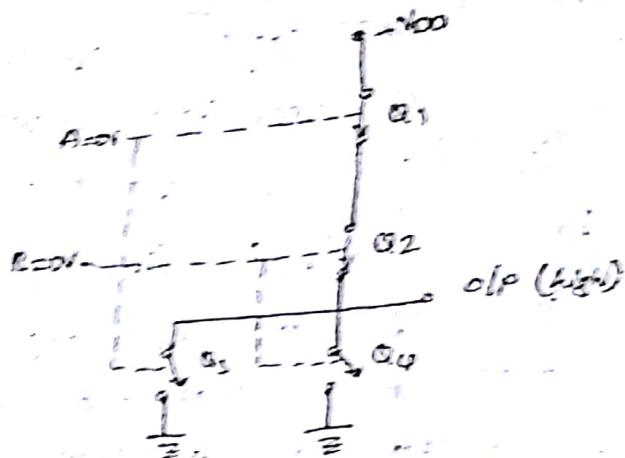
In CMOS NOR gate, p-channel MOSFETs  $Q_1$  and  $Q_2$  are connected in series and N-channel MOSFETs  $Q_3$  and  $Q_4$  are connected in parallel.

Like NAND circuit, this circuit can be analyzed by realizing that a low at any input turns on its corresponding p-channel MOSFET and turns off its corresponding N-channel MOSFET and vice versa for high input.

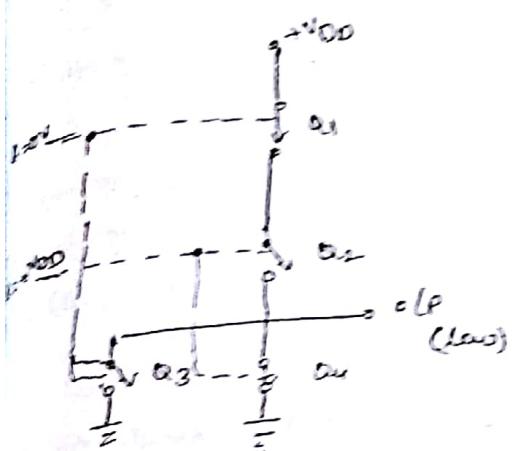
	$A$	$B$	$Q_1$	$Q_2$	$Q_3$	$Q_4$	O/P
	0	0	ON	ON	OFF	OFF	1
	0	1	ON	OFF	OFF	ON	0
	1	0	OFF	ON	ON	OFF	0
	1	1	OFF	OFF	ON	ON	0



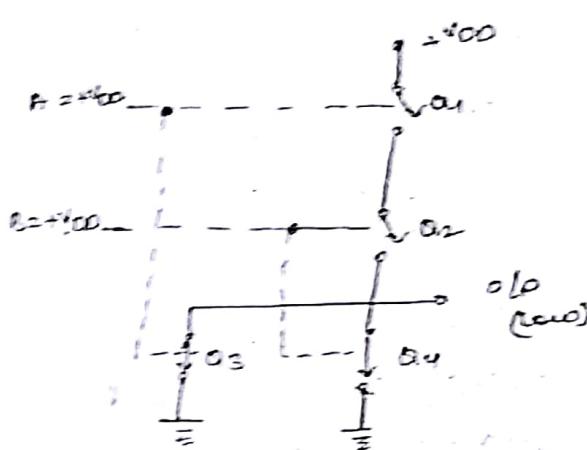
a) Schematic



$$\text{b) } A = B = 0V \\ V_{O1} = V_{O2} = \pm VDD \\ V_{O3} = V_{O4} = 0V$$



$$\text{c) } A = 0V, B = +VDD \\ V_{O1} = -VDD \\ V_{O2} = V_{O3} = 0V \\ V_{O4} = -VDD$$



$$\text{d) } A = B = +VDD \\ V_{O1} = V_{O2} = 0V \\ V_{O3} = V_{O4} = \pm VDD$$

### Characteristics of CMOS:

1. Operating Speed: CMOS is slower than TTL devices. Approximately 10 times slower. It also depends on power supply voltage.

### Voltage levels and noise margins:

The voltage levels for CMOS varies according to their technologies. Noise margins are

$$V_{NH} = V_{O1(\text{min})} - V_{I1(\text{min})}$$

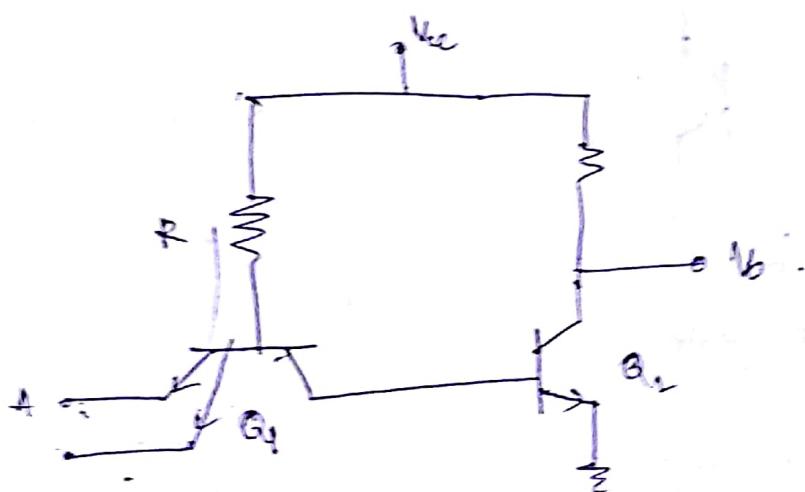
$$V_{NL} = V_{I1(\text{max})} - V_{O1(\text{max})}$$

3. fan-out: CMOS outputs are limited to a fan-out of 50 for low frequency operation; P<sub>D</sub> with frequency of operation the fan-out would be less.

Power dissipation (P<sub>D</sub>): the power dissipation of a CMOS gate is very low as long as it is in a DC condition. But P<sub>D</sub> increases in proportion to frequency. For ex. a CMOS NAND gate has P<sub>D</sub> = 10 mW under certain conditions will have P<sub>D</sub> = 0.1 mW at 100 kHz and about 1 mW at 1 MHz.

When both A and B are '1', the V<sub>be</sub> flows towards the transistor Q<sub>1</sub>, but the voltage is not sufficient to make the transistor ON, hence, the diodes D<sub>3</sub> & D<sub>2</sub> are added to increase the voltage at the base of the transistor.

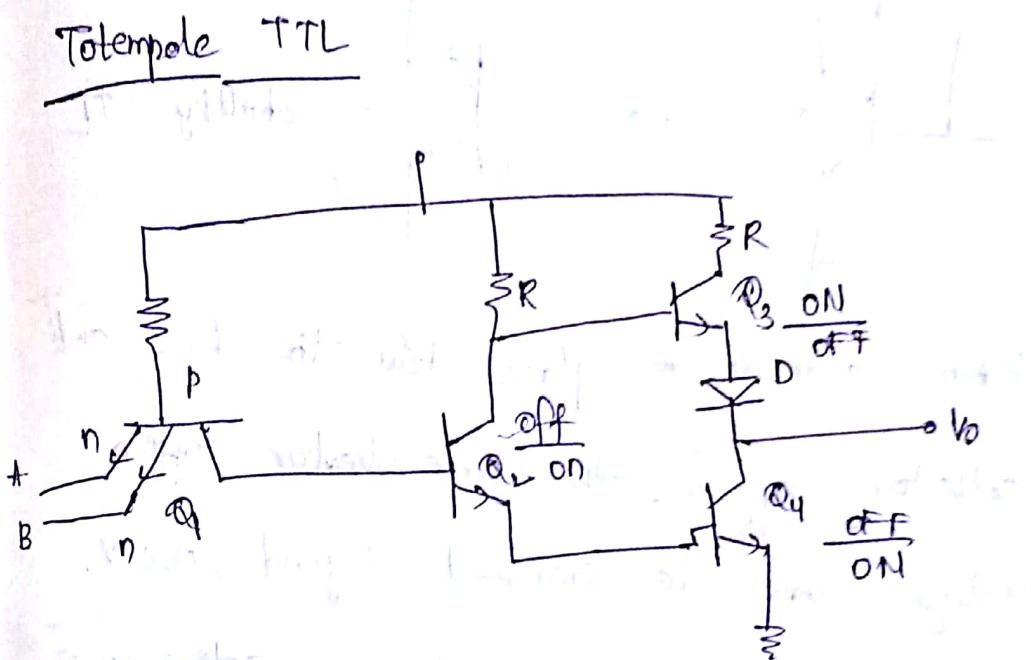
### Simple TTL gate:



The transistor Q<sub>1</sub> provides the required voltage for logic 1 of transistor Q<sub>2</sub>. Hence diode D<sub>3</sub> & D<sub>2</sub> base voltage V<sub>BB</sub> can be removed.

A	B	Q <sub>1</sub>	Q <sub>2</sub>	V <sub>b</sub>
0	0	ON	OFF	1
0	1	ON	OFF	1
1	0	ON	OFF	1
1	1	OFF	ON	0

When both  $A$  &  $B$  are '1's and the transistor  $Q_1$  is off and  $Q_2$  is ON. All the  $V_{cc}$  power supply will be flowing towards  $Q_2$  ground, which increases the sink current. Hence, to eliminate this problem ~~tetrapole~~ totem pole TTL is used.



Truth Table:

A	B	$Q_1$	$Q_2$	$Q_3$	$Q_4$	$V_0$
0	0	on	off	on	off	1
0	1	on	off	on	off	1
1	0	on	off	on	off	1
1	1	off	on	off	on	0

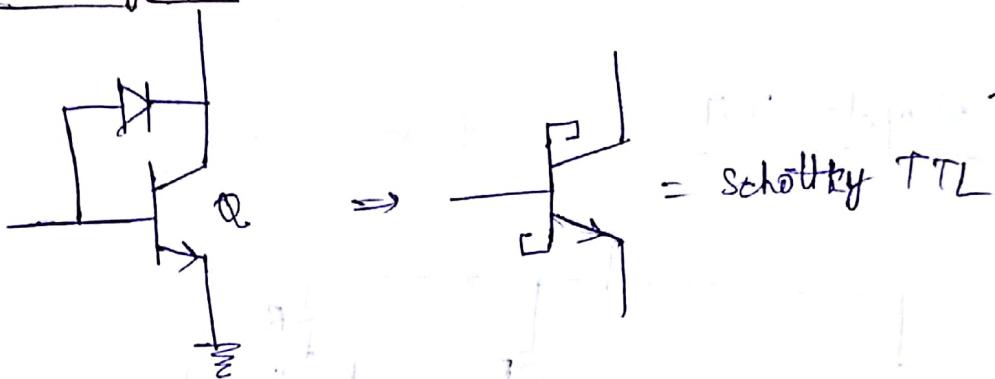
When  $A=B=0$ ,  $Q_1$ -ON,  $Q_2$ -OFF,  $Q_3$ -ON,  $Q_4$ -OFF

$$V_0 = 1$$

When  $A=B=1$ ,  $Q_1$  - off,  $Q_2$  - on,  $Q_3$  - off and  $Q_4$  - on

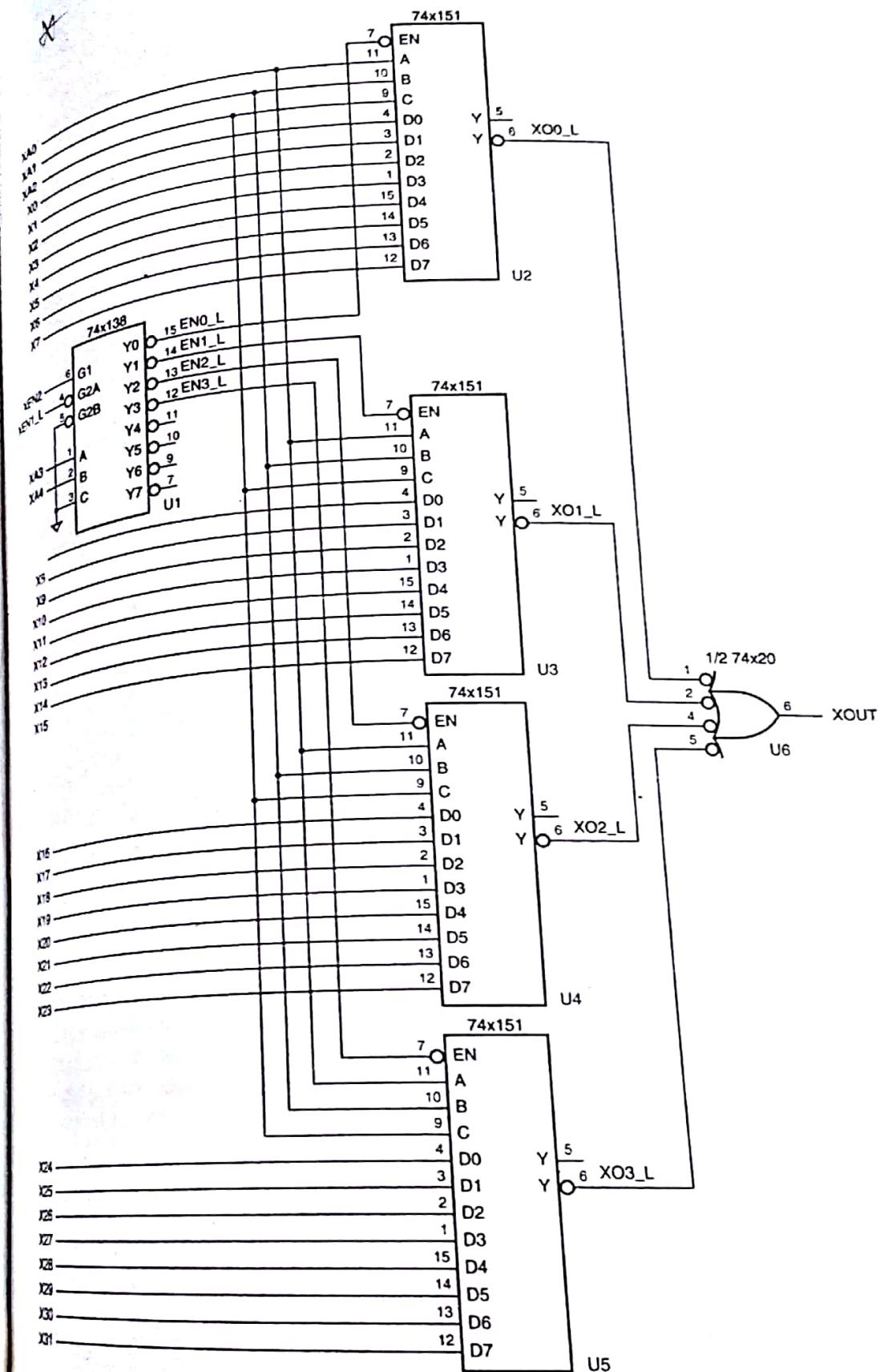
but the time taken by the  $Q_3$  - transistor to change from off state to on state is more than that of  $Q_4$  - transistor. Hence, for a short duration  $D_3$  diode  $Q_4$  is on.

### Schottky TTL:

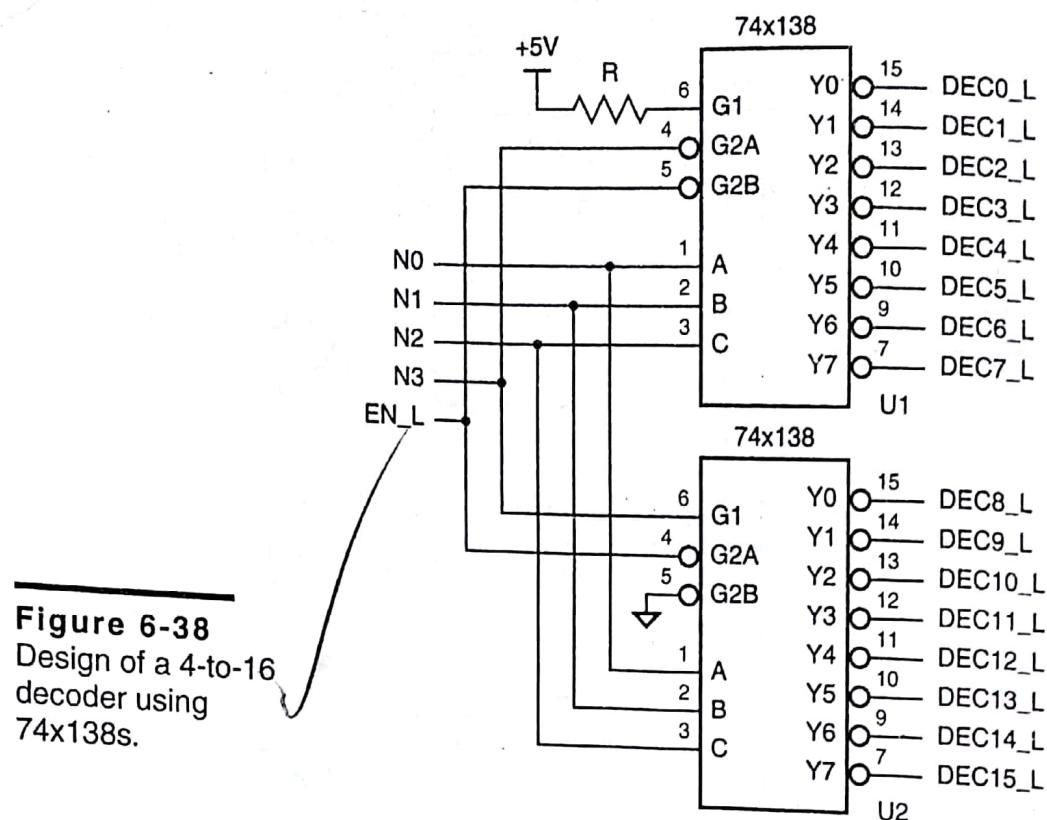


When a diode is placed b/w the base and collector region, the base-collector voltage cannot be increased beyond  $0.6\text{V}$ . Hence, the transistor is only in active region.

By making the transistor to operate only in active region, the storage time can be reduced and hence the propagation delay can be reduced.



**Figure 6-62**  
Combining 74x151s  
to make a 32-to-1  
multiplexer.



**Figure 6-38**  
Design of a 4-to-16  
decoder using  
74x138s.

For example, Table 6-7 is an ABEL program for a 74x138-like binary decoder as realized in a GAL16V8, and Figure 6-39 shows the pinouts of the device. Note that some of the input pins and all of the output pins have active-low names ("\_L" suffix) in the pin declarations, corresponding to the logic diagram in Figure 6-35 on page 388. However, the program also defines a corresponding active-high name for each signal so that the equations can all be written "naturally," in terms of active-high signals. An alternate way to achieve the same effect is described in the box on page 397.

Also note that the ABEL program defines a constant expression for ENB. Here, ENB is not an input or output signal, but merely a user-defined name. In the equations section, the compiler substitutes the expression (G1 & G2A & G2B) everywhere that "ENB" appears. Assigning the constant expression to a user-defined name improves this program's readability.

If all you needed was a '138, you'd be better off using a real '138 than a more expensive PLD. However, if you need nonstandard functionality, then the PLD can usually achieve it much more cheaply and easily than an MSU/SSI-based solution. For example, if you need the functionality of a '138 but with active-high outputs, you need only to change one line in the pin declarations of Table 6-7:

Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7

pin 19..12 istype 'com'.

(Also, the original definitions of  $Y_0$ - $Y_7$  in Table 6-7 must be deleted.) Since each of the equations requires a single product of six variables (including the three in