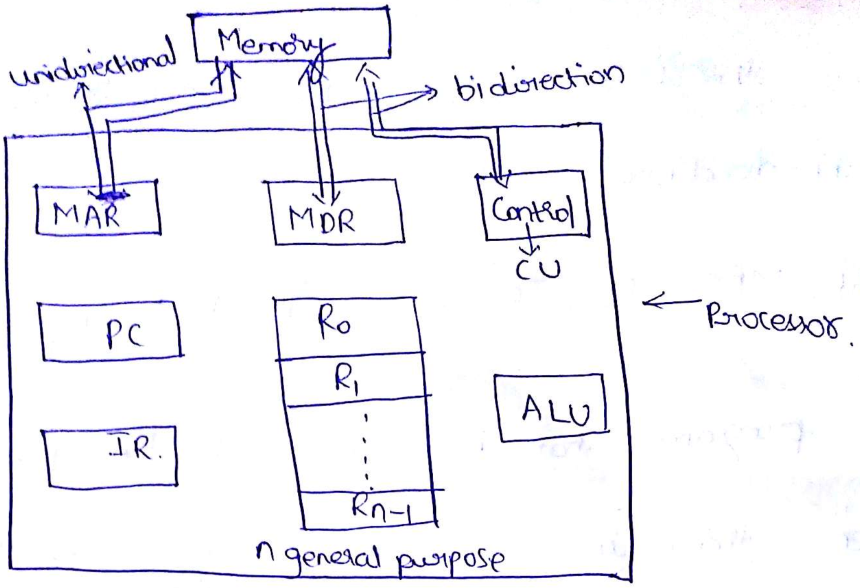


registers → to hold operands.

* Connections between the processor and the memory *

* MAR→ memory adress ~~locati~~ Register, Contains the adress of memorylocationwhich has to be accessed

* MDR → memory data register, Contains the data written in to the memory or the data that should read from the memory.

*PC→ Program Counter, Contains address of next memory that has to be Executed.

*IR→ Instruction register, Contains intruction that should be Executed. currently.

*CU:→ Same definition.

*ALU:→ Same definition

* address should be transfered from MAR to memory so uni-directional.

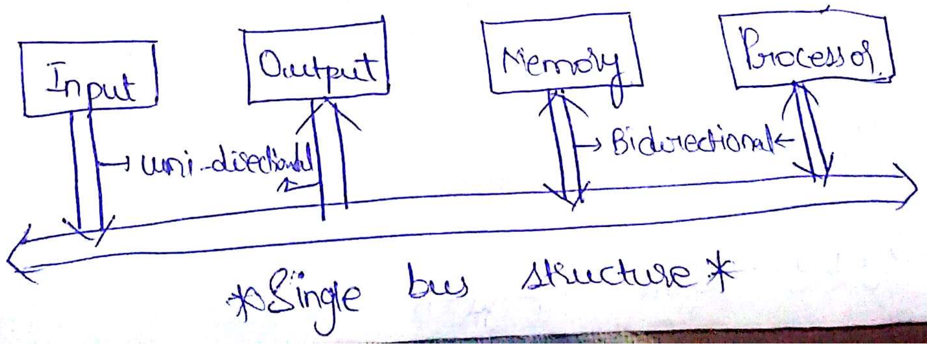
*→*MAR, MDR, PC, IR are Specialised register

* The program that is Executed by the processor, when their is a interupt from IO device is called Interupt - Service - Routine (ISR)

* At this time, it stops the present program of Normal programs and saves the data to the memory & ~~req~~ responds to the ~~status~~ interupt or
(from registers).
request of IO device.

* After Completion of ISR it will go to Normal Program Execution.

* Bus Structures:-



Single bus structure

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{ Processor transfers the data to Buffer register by Character by character}.

22\06\17

* Software :->

→ * Compiler Converts high level language to machine level language.

→ * text Editor is used for Entering & Editing the application programs.

→ * O.S Performs several functions like transfering data between memory & disk

* it allocates space in memory & disk for programs & dat

* it is used for handling IO operations

* Performance :->

* Time taken to fetch the data from main memory is more when Compared to the time taken by the processor to fetch from Cache memory.

* Data which is used to do repeatedly they are fetched from Cache memory by processor.

* Processor clock :→

* Processor circuits are Controlled by a timing signal called Clock

* The action that to be performed using some instructions are divided into number of basic steps.

* Such that Each basic step will have to be Completed by/ with in one clock cycle.

* Clock freq is of the order of 500MHZ - 1.25 GHZ.

* Basic performance Equations :→

* N → no of machine language instructions that are to be Executed.

* S → avg no. of basic steps needed to Execute an instruction.

*R → clock rate of clock frequency.

*T → program Execution time

$$T = \frac{N \times S}{R}$$

* "R" should be high ~~for~~ to have "T" small/less.

* Pipelining & superscalar operation:->

* Fetching the next instruction by processor while the Present instruction is being Executed is Called Pipelining.

* Processor contains multiple functional units that is Called as super scalar processor.

* Add R1, R2, R3

Operands present in R1 & R2 are given to i/p of ALU & stored in R3.

If the next instruction is also to add, then those operands will be transfered to i/p of ALU while the result is being stored in "R3" (Pipelining).

Clock rate :→ / Clock frequency

* Increasing clock rate ~~by~~ increases speed.

* In order to increase the Clock rate, we have to use high technology IC.

* If the processing done by basic step decreases then Clock rate increases i.e.. Clock period decreases.

* Instruction Set :→

* CISC & RISC → Reduced ISC {uses simple instructions}

→ Complex Instruction set Computers {Complex instructions}

→ * No. of instructions for RISC will be more. i.e.. N is more ⇒ S is less

* No. of instructions for CISC will be less i.e.. N is less → S is more.

→ * when CISC is combined with pipelining it gives the best performance.

* RISC Combined with pipeling is Easier to implement.

* Compiler :→

* it Converts high to machine level language

* it Can Compile into a fewer instructions.

∴ speed will be more

*it can rearrange the instructions to improve the performance

*Performance measurement :-

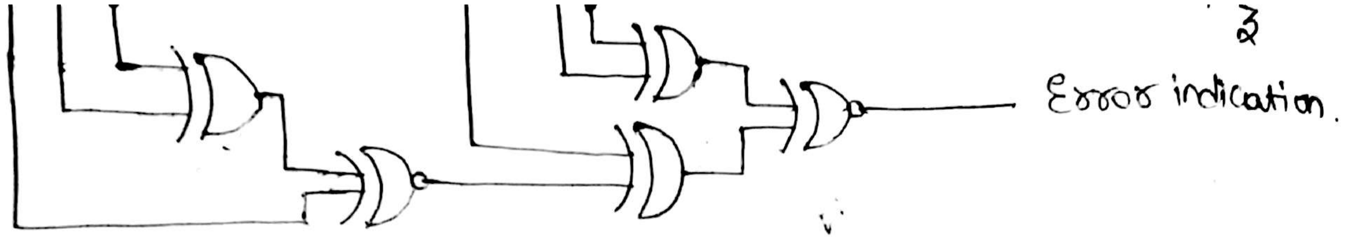
$$\text{SPEC rating} = \frac{\text{Running time on the reference computer}}{\text{Running time on the computer under test}}$$

System Spectrum Evolution Co-operation.

overall ~~Spectrum~~ Spec rating is given by

$$\text{SPEC rating} = \left(\prod_{i=1}^{n} SPEC_i\right)^{1/n}.$$

n → no of programs that are Run



Parsity generactol   Parity checker.

* Error detection with odd parity bit.

29|06|17

* Broblems*

*I) Convert the following binary numbers to decimal number.

*1) $(101110)_2$.

*Sol) $(46)_{10}$

*II) Convert the following numbers with indicated bases to decimal