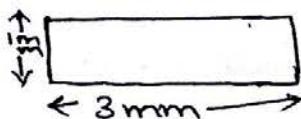


Bipolar Junction Transistor.

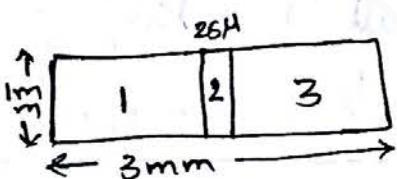
Introduction:

- Take an intrinsic material of Si crystal of 3mm length and 1mm of width.



- Divide the intrinsic material of Si in to three parts of lengths such that first Part will be moderate Area (length) and second Part will be small Area (length) and third Part will have larger Area.

- 1 Part — Moderate Area
- 2 Part — small Area
- 3 Part — large Area.



3(a) Doping of the 1 part with P type material with high doping concentration then this portion known as Emitter.

4(b) Doping the 2nd part with low concentration, this portion is known as Base

5. Doping the 3 part with moderate concentration then this portion known as collector.

Then → the transistor will be formed.

5.

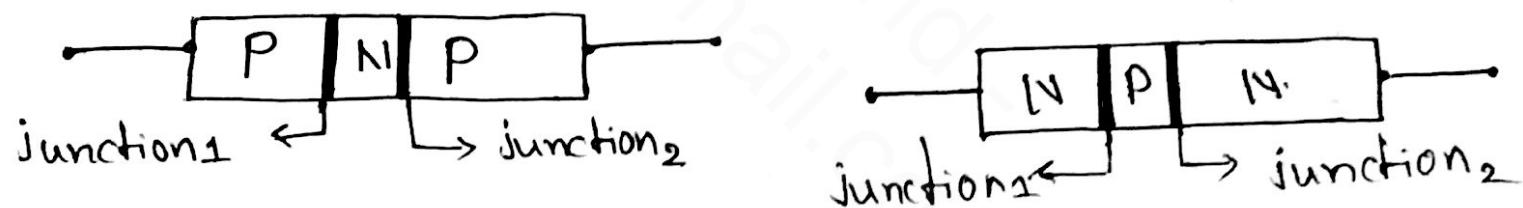
- @ If
 1 Part — N type highly doped emitter.
 2 Part — P type lightly doped base
 3 Part — N type moderately doped collector.

Then transistor is NPN transistor.

- ⑥ If
 1 Part — P type highly doped emitter
 2 Part — N type lightly doped base
 3 Part — P type moderately doped collector.

Then this transistor is known as PNP transistor.

Representation:



Type	Emitter			Base			Collector		
	Type	Area	con	Type	area	conven	Type	Area	consen
PNP	P	Mode rate	high	N	Small	Small	P	large	moderat
NPN	N	Moder ate	high	P	small	small	N	large	moderate

The Junction-transistor:

As we discussed before A junction transistor consists of a silicon crystal in which a layer of n-type silicon is sandwiched between two layers of p-type (material) silicon, then transistor known as PNP.

The potential distribution through a transistor.

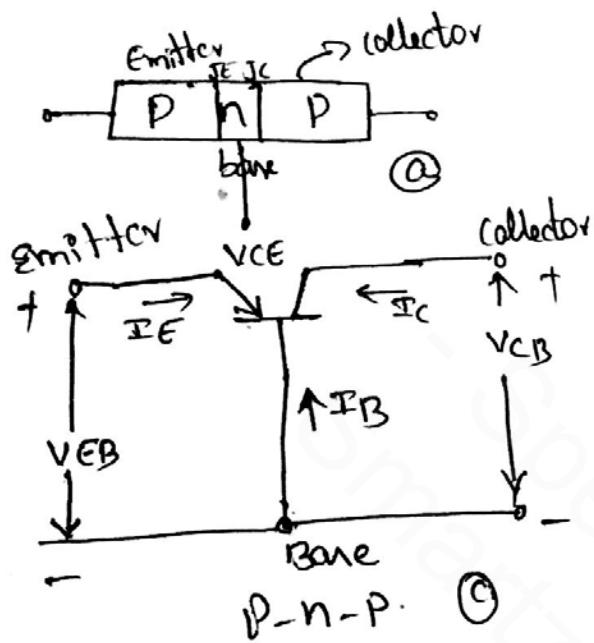
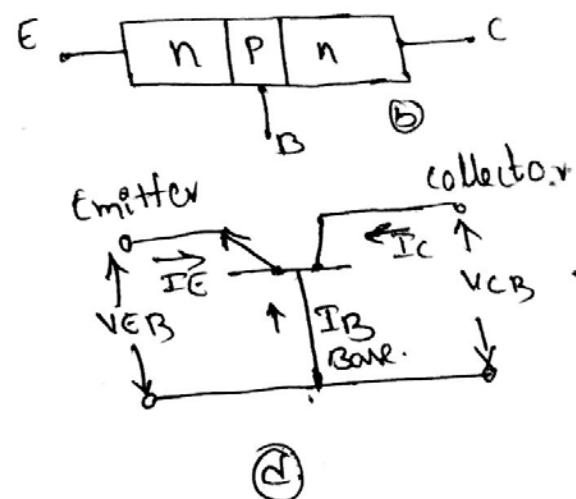


fig ④ → PNP transistor
⑤ - nPN transistor



- ⑥ circuit representation of PNP transistor
- ⑦ circuit representation of nPN transistor.

The PNP transistor is taken for showing potential distribution, The voltage sources which serve to bias the Emitter base junction in forward bias and the collector base junction in the reverse bias.

The variation of Potential through and unbaised (openckt) transistor in fig. ④(f). And potential variation through the biased transistor in fig. ④(g).

The dashed curve applies to the case before biasing and the solid curve to the case after biasing voltages are applied.

Absence of applied voltage, the potential barrier at the junction adjust themselves to the height V_0 . So no current flows across each junction.

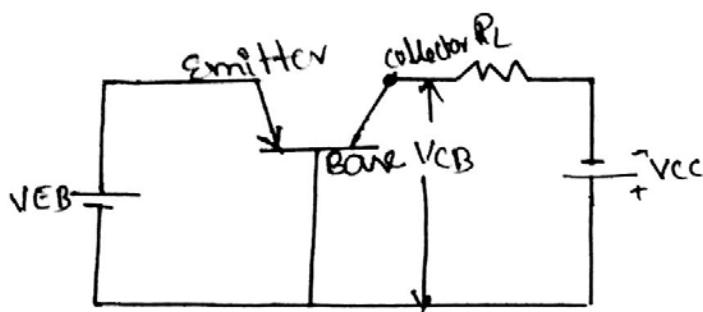
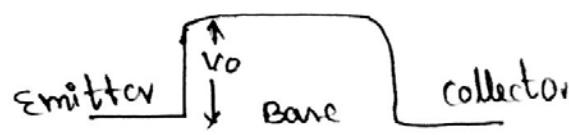
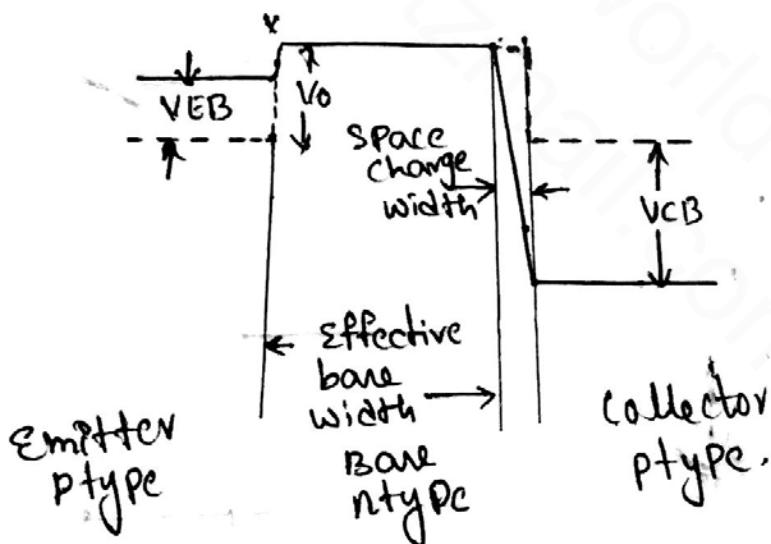


fig (e)
PNP transistor with biasing
Voltage \rightarrow



fig(f)
Potential barrier at the junction of the unbaised transistor.



fig(g)

Potential variation through the transistor under biased conditions.

If now external potentials are applied these voltages appear essentially across junctions. Hence the forward biasing of the emitter-base junction lowers the emitter-base potential barrier by $|V_{EB}|$.

barrier by $|V_{EB}|$

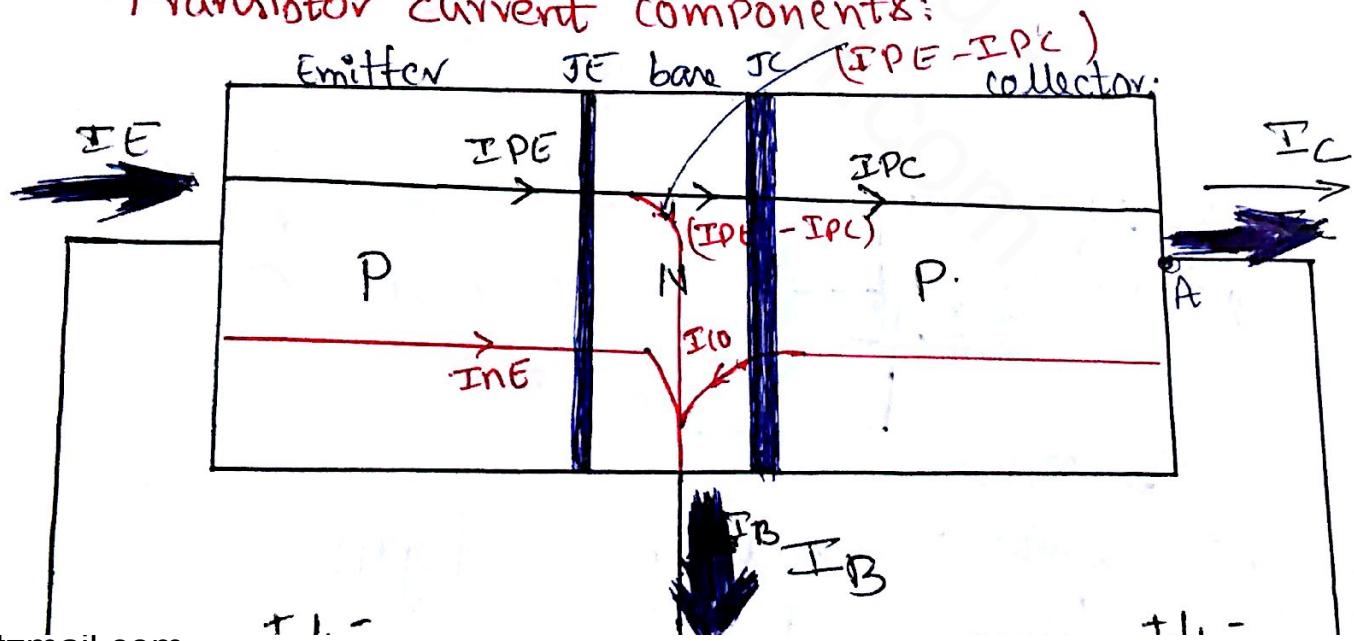
Increases the collector base potential barrier by $|V_{CB}|$.

The lowering of the emitter base barrier permits the emitter current to increase, as holes are injected in to base region. The potential is constant across the base region; as the injected holes diffuse across the n-type material to the collector base junction. The holes which reach this junction fall down the potential barrier and are collected by the collector.

Principle of operation of transistor.

OR

Transistor current components:



The current in forward bias is due to both minority carrier & majority carrier as shown in fig(b)

$$I_{Fe} = I_{\text{majority}} + I_{\text{minority}}$$

$$I_{Fe} = I_{PE} + I_{NE} \Rightarrow I_{Fe} \approx I_{PE}$$

majority carrier current

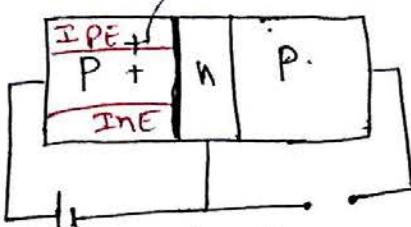
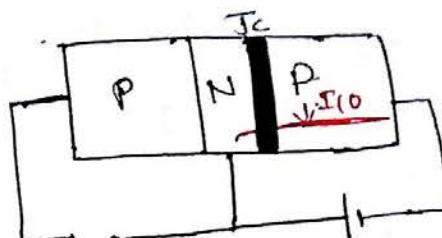


fig.(b).



fig(c)

The J_C junction is reverse biased, In reverse biased majority carrier current will be zero & resulting only the minority carrier flow the I_{CO} current shown in fig(a) & fig(c)

If both biasing potentials have been applied to the PNP transistor with resulting the majority and minority carrier flows.

The Emitter is highly doped (P type) so majority carriers holes injected into base as I_{PE} at J_E end enters into the base. The base is lightly doped & small area of N type material a small amount of recombination process occurs (combine of holes (emitter) & electron) in base. This small amount of recombination current ($I_{PE} - I_{PC}$). The remaining carrier will enter in collector as I_{PC} .

since for the reverse bias diode the injected majority carriers will appear as minority carriers in the N type material. So I_{PC} current flows.

The minority current I_{CO} , I_{NE} & $I_{PE} - I_{PC}$ recombination current treated as the base current.

All the minority carriers in the depletion region will cross the reverse biased junction of a diode.

Applying Kirchhoff's law for fig(a)

$$I_E = I_C + I_B$$

The base currents are the sum of three currents that are minority currents

1. I_{NE}
2. I_{CO}
3. $I_{PE} - I_{PC}$

Apply KCL equation at collector terminal at point A.

$$I_{PC} + I_C = I_{CO}$$

$$\Rightarrow I_C = I_{CO} - I_{PC} \quad \text{--- (1)}$$

Emitter efficiency η :

$$\eta = \frac{\text{current of injected carriers at } I_E}{\text{total emitter current}}$$

for PNP

$$\eta = \frac{I_{PE}}{I_E} \quad \text{--- (2)}$$

maximum value of η will be $B+1$

Transport factor β^*

$$\beta^* = \frac{\text{injected carrier current reaching } I_C}{\text{injected carrier current at } I_E}$$

$$\beta^* = \frac{I_{PC}}{I_{PE}}$$

$\beta \gg 1$ always greater than 1
typical value of $\beta = 49$.

large signal current gain α :

Ratio of the negative of collector current increment to the emitter current change from zero to I_E on the large signal current gain

$$\alpha = - \left(\frac{I_C - I_{C0}}{I_E - 0} \right) \Rightarrow - \frac{I_C - I_{C0}}{I_E}$$

$$\alpha = - \frac{I_C + I_{C0}}{I_E} \Rightarrow \alpha I_E = - I_C + I_{C0}$$

$$I_C = -\alpha I_E + I_{C0}$$

$$\alpha = - \left(\frac{I_C - I_{C0}}{I_E} \right) \quad \text{--- (4)} \quad \text{By } I_{C0} \approx \text{small (approximated)}$$

$$\alpha = - \frac{I_C}{I_E}$$

$$\text{from (1)} \quad I_C = I_{C0} - I_{PC} \Rightarrow I_C = -I_{PC}$$

$$\alpha = - \left(\frac{-I_{PC}}{I_E} \right) \Rightarrow \alpha = \frac{I_{PC}}{I_E}$$

Multiply numerator & denominator by I_{PE} .

$$\alpha = \frac{I_{PC}}{I_E} \times \frac{I_{PE}}{I_{PE}} \Rightarrow \frac{I_{PC}}{I_{PE}} \times \frac{I_{PE}}{I_E}$$

$$\text{from (2) \& (3)} \quad Y = \frac{I_{PE}}{I_E} \quad \text{and} \quad \beta = \frac{I_{PC}}{I_{PE}}$$

$$\alpha = \beta \cdot Y \quad \text{--- (5)}$$

α value will be max will be 1 (for ideal condition)

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

I_{C0}

collector reverse saturation current or collector leakage current or minority carrier current.

I_{C0} is doubled for every 10°C rise of temperature.

I_{C0} approximately increases by 7%.

$$I_{C0(T_2)} = I_{C0(T_1)} \cdot 2^{(T_2 - T_1)/10}$$

I_{C0} is μA for Ge transistor.
 nA for Si transistor.

I_{C0} is independent of collector junction voltage, since the reverse saturation current is const for reverse bias voltage.

Emitter current:

Emitter junction is forward biased.

To find I_E emitter current take diode current I_{D0} .

$$I = I_{C0} (e^{V/nVT})$$

$$I = I_{C0} (e^{V/nVT} - 1) \quad 1 \text{ can be neglected}$$

$$I = I_{C0} (e^{V/nVT})$$

The emitter junction current of the transistor is forward biased $\triangleright 0$

$$I_E \approx I_{C0} (e^{V_{BE}/nVT}) \quad \text{--- (6)}$$

V_T = Thermal voltage

Collector current:

$$\alpha = - \frac{(I_C - I_{C0})}{I_E} \Rightarrow \alpha = - \left(\frac{I_C - I_{C0}}{I_E} \right)$$

$$\alpha \cdot I_E = -I_C + I_{C0}$$

$$I_C = -\alpha I_E + I_{C0}$$

(+)

Bare current

$$I_E = I_C + I_B$$

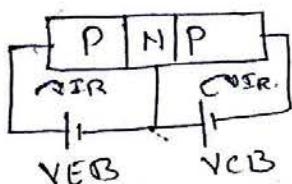
$$I_E = I_C + I_B \Rightarrow I_B = I_E - I_C - 8$$

equation for base-to-emitter voltage of transistor.

$$I_E \approx I_C \cdot e^{\frac{V_{BE}}{nV_T}}$$

For difference:

Transistor is current control current device.



If transistor operated in active region
The current majority carrier flows from
emitter to base in small amount of

current will be low due to recombination in base a
enters in to collector almost equal to I_E so that we
can say $I_E \approx I_C$.

If less amount of current enters in emitter
less amount of o/p I_C current. If large of I_E when
large of I_C .

No that the transistor is called as a current controlled
current device or Current dependent current source.

The term bipolar reflects the fact that holes as
electrons participate in the injection process in to the
oppositely polarized material.

The current in transistor is due to both
majority & minority carriers so the transistor can
be named as Bipolar junction transistor. (as it is
having two junctions)

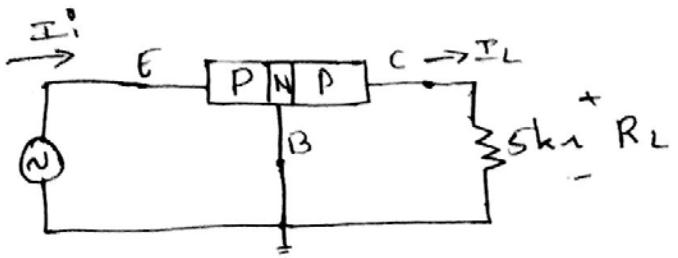


fig.(a)

A load resistance R_L is in series with the collector supply voltage V_{CC} in fig.(b).

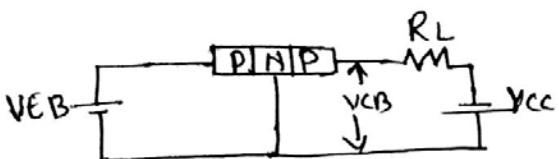


fig.(b).

A small voltage change ΔV_i between emitter & base causes a relatively large emitter current change ΔI_E . The change of o/p voltage across load is

$$V_o = I_C \cdot R_L$$

$$I_C \approx \alpha I_E$$

$$\boxed{V_o = \alpha I_E \cdot R_L}$$

The change in o/p voltage across load resistor many times the change in input voltage ΔV_i .

Can we know that forward dynamic resistance will be small for JE junction resistanc r_{fe} - is small and the reverse biased junction resistance r_{ce} is also large w/ R_L external resistance is also large.

so that the dynamic resistance of Emitter junction r_{fe} + then

$$\boxed{\Delta V_o = r_{fe} \Delta I_E}$$

voltage amplification will be equal to

$$A = \frac{\Delta V_o}{\Delta V_i} \approx A = \frac{V_o}{V_i}$$

$$A = \frac{\alpha A_{IE} R_L}{r_e' D^2 C} = \frac{\alpha' \cdot R_L}{r_e'} \quad r_e' \ll R_L$$

No $|A| > 1$

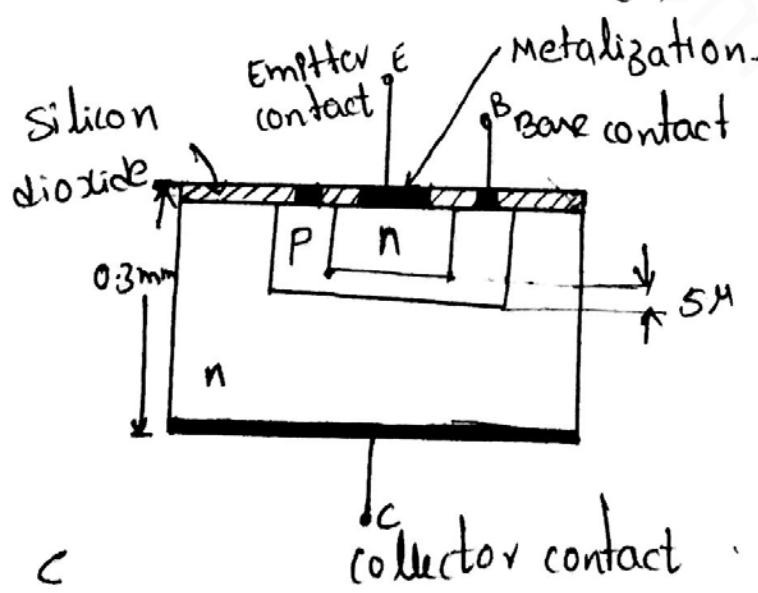
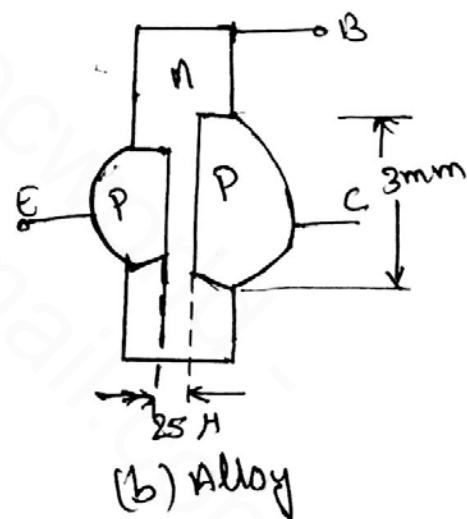
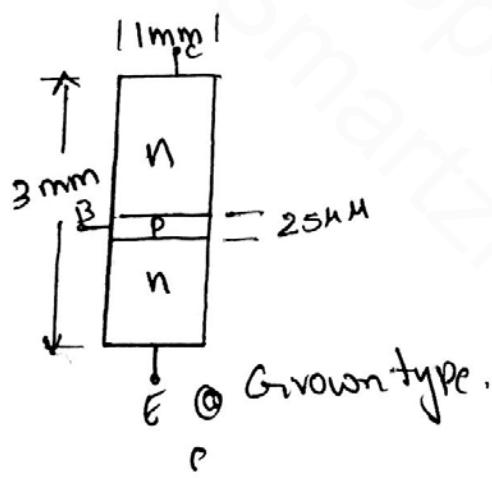
So that the transistor acts as an amplifier.

-1

Transistor construction:

There are basic five techniques have been developed for manufacture of diodes in transistors &

- 1. Growth type 2. Alloy type 3. Electro chemically Etched type
- 4. Diffusion type 5. Epitaxial type.



Grown type:

The npn grown junction transistor is fig(a) is made from a single crystal from a melt of silicon or germanium whose impurity concentration is changed during the crystal drawing operation by adding n or p-type atoms are required.

Alloy type:

This technique also called a fused construction as in fig(b) for p-n-p transistor construction. The center base section is a thin wafer of n-type material. Two small dots of indium are attached to opposite sides of the wafer and the whole structure is raised for a short time to a high temperature above the melting point of indium but below that of germanium. The indium dissolves the germanium beneath it to form a saturation solution. On cooling the germanium contact with the base material recrystallizes with enough indium concentration to change it from n-type to p-type. The collector is made larger than the emitter so that the collector subtends a large angle as viewed from the emitter. This geometrical arrangement very little emitter current flows a diffusion path which carries base

Electrochemically Etched type:

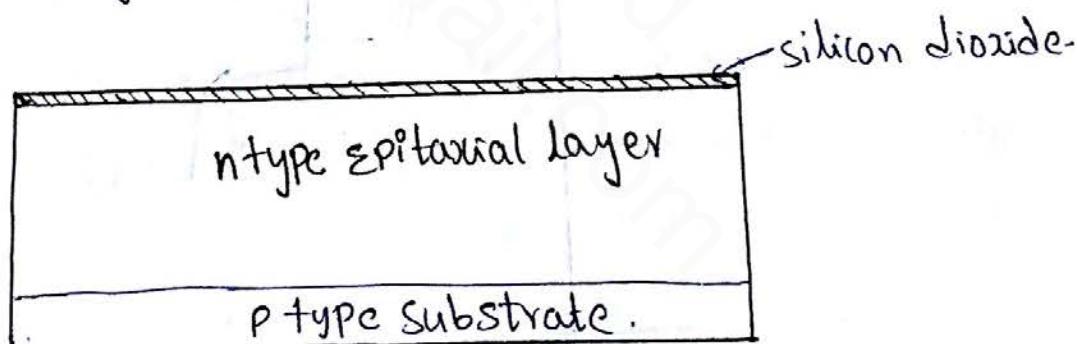
This technique consists in etching depressions on opposite sides of semiconductor wafer in order to reduce the thickness of the base section. The emitter and collector junctions are then formed by electro plating a suitable metal into the depression areas. This type of device also referred as surface barrier transistor

Diffusion type:

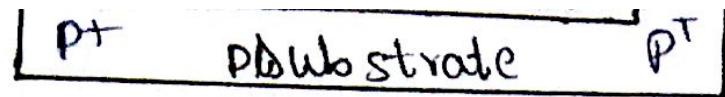
This technique consists in subjecting a semiconductor wafer to gaseous diffusion of both n & p type impurities to form both the emitter and the collector junctions. A planar silicon transistor of diffusion type is shown in fig. In this process the base collector junction area is determined by a diffusion mask which is photo etched just prior to the base diffusion. The emitter is then diffused on the base and a final layer of silicon oxide is thermally grown over the entire surface. Because of the passivation action of this oxide layer, most surface problems are avoided by very low leakage current. There is also an improvement in the current gain at low currents and in the noise figure.

Epitaxial type:

The epitaxial technique consists in growing a very thin, high purity, single crystal layer of silicon



or germanium on a heavily doped substrate of the same material. This augmented crystal forms the collector on which the base and emitter may be diffused.

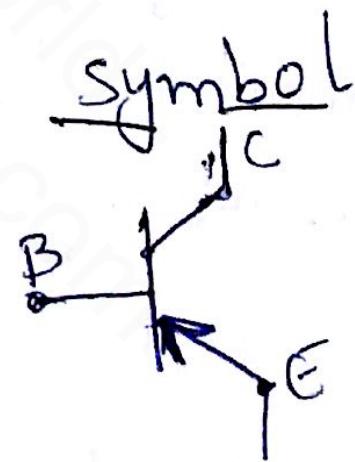


BJT operation → same notes of the transistor
current components

BJT Symbol:

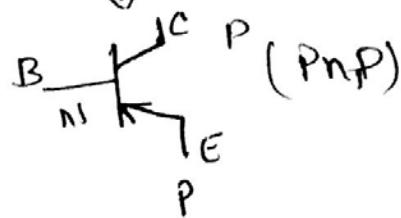
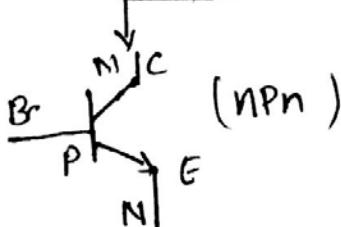
Transistor

P n P

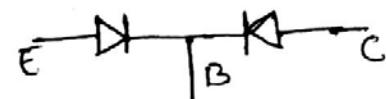
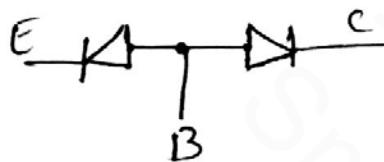
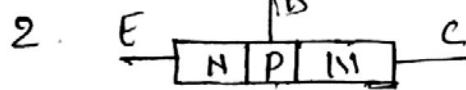


Current I_E enters
in to transistor
Arrow towards
entering in to
transistor at
across Emitter
terminal

BJT (Bipolar junction-transistor)



NPn is faster than the PnP because μ_n electron mobility greater than the hole mobility.

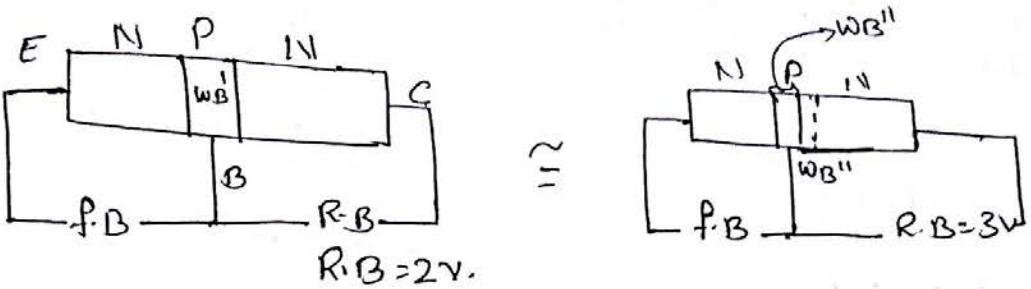
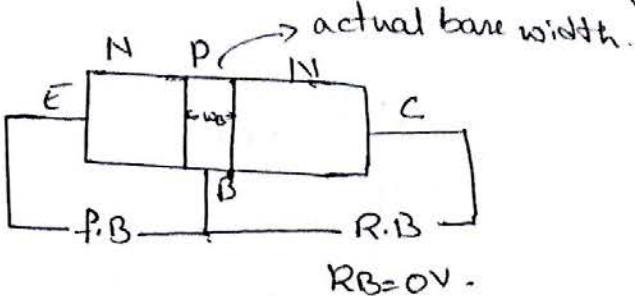


Breakdown in transistors:

- Avalanche breakdown and multiplication.

As we studied in Previous unit, the avalanche breakdown occurs when T_C junction is reverse biased the transistor is operated in Active region.

- Avalanche breakdown is an electron gain energy while the covalent bond then 2 free electrons taken place thus an multiplication process. so current will increases as a large amount for small increment of voltage.
- Punch through: This occurs due to base width modulation or Early effect.



w_B = Actual base width of transistor.

w_B' & w_B'' = Effective base width of transistor, when $R.B$ is increased.

When ever the Reverse bias voltage is increased - the Space charge region or depletion region increases. The depletion layer will penetrate more in to lightly doped region & lesser in to highly doped region.

So that depletion penetrate more in to Base so that base width decreases. If base width decreases I_B will be decreased due to area will be less so that recombination is less. If I_B is decreased I_C will be increased. This is known as early effect.

If I_C increased $\alpha = \frac{I_C}{I_E} \rightarrow \alpha$ is increased.

by small value the B will change in a large value.

$$\beta = \alpha / 1 - \alpha$$

Advantages:

1. Recombination process decreased in base so α increased.
2. switching time reduced.

Punch through effect

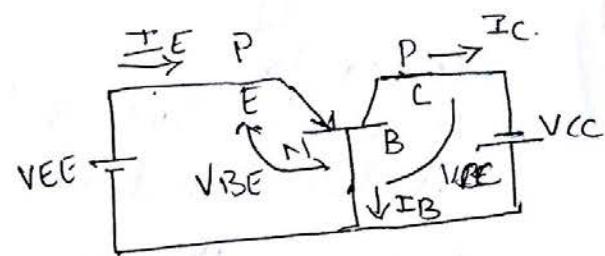
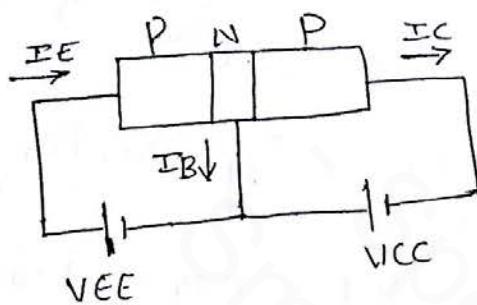
An reverse voltage goes on increases the base width goes on decreased at some reverse voltage, the base will be disappears. (that is E-C will be side by side known as only N material or P type material). So that transistor will be damaged this effect is known as punch through.

Common Base configuration:

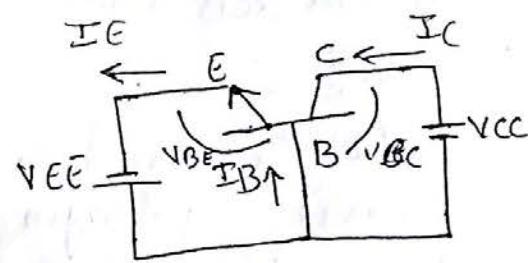
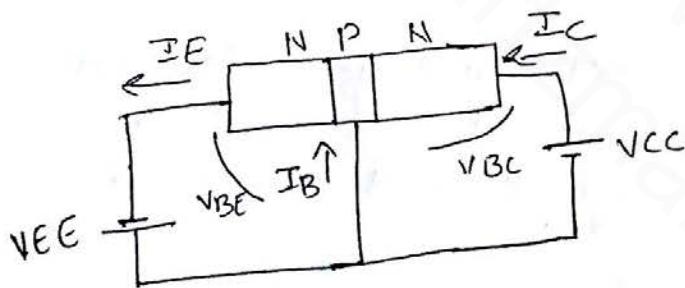
When the transistor is to be connected in a circuit one terminal is used as an input terminal, the other terminal is used as an output terminal and the third terminal is common to the input & output.

In common base configuration base is the common terminal for both i/p & o/p. Emitter is the i/p terminal and the collector is the output terminal.

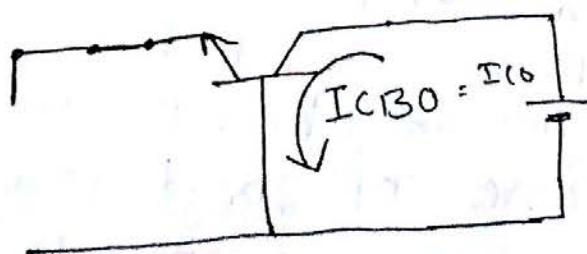
P-N-P common base



N-P-N common base:



To find how much reverse saturation current flows in common base configuration



I_{CBO}
CB → collector to base
O → Emitter open.

If Emitter terminal is opened & apply only reverse bias voltage then only minority current flows from collector to base so I_{CBO} .

I_{CBO} is the reverse saturation current flows from collector to base when emitter is opened.

To study the characteristics of common base configuration there requires two sets of characteristics

1. INPUT characteristics
2. OUTPUT characteristics

INPUT characteristics.

To study input characteristics

→ ~~Maintain~~

1. collector Base voltage V_{BC} is kept constant.

2. The Emitter current is increased by varying the supply voltage w/ note values of I_E & V_{BE}

3. Repeat the steps 1, & 2 for higher voltages of

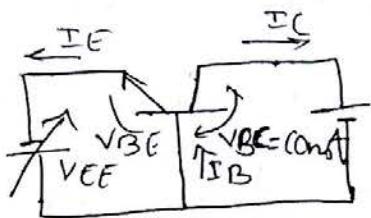
V_{BC} .
If $V_{BC} = 0$

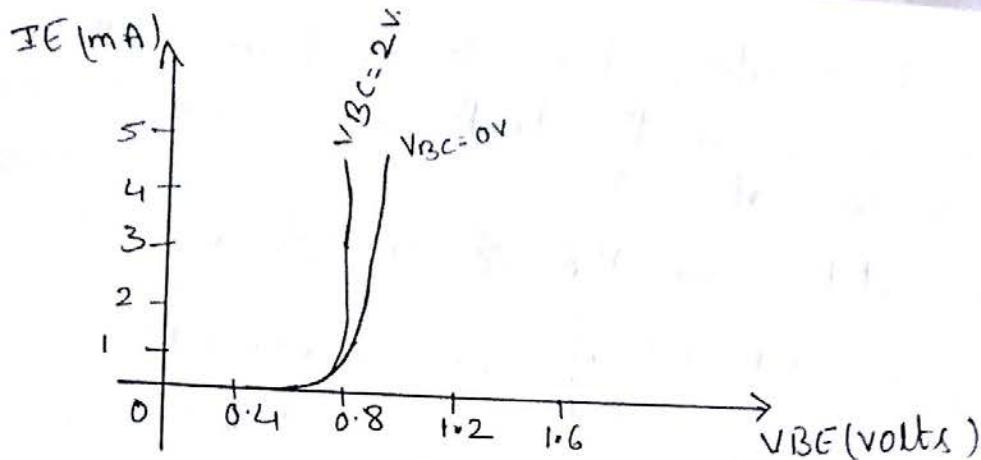
The JE junction that is Emitter w/ Base is forward biased, by varying small amount of voltage of V_{EE} (indirectly V_{BE}) there will large current variation after cut-in voltage.

know increase $V_{BC} = 2V$.

By early effect i.e if reverse bias voltage increases the depletion layer penetrates in to lightly doped base, so that base width decreases, If base width decreases recombination processes will be less so I_B decrease, If I_B decreases I_C increases, If I_C increases I_E will increases

Due to early effect I_E increases for even small values of V_{BE} so that the current will be affected towards Aviain





Output characteristics

To study output characteristics

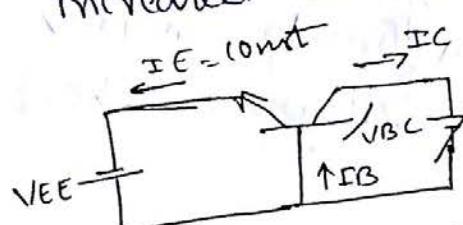
1. Emitter current kept constant.

2. vary V_{CC} voltage note the values of V_{BC} w/ I_C .

~~Repeat~~ Repeat 1, u/ 2 for higher values of emitter current.

Active If $I_E = 0\text{mA}$ then only the reverse saturation current I_{CBO} flows only.

If I_E current increased to 1mA the collector current increased 1mA & in C $I_E \approx I_C$.



Since the I_C current is $\propto I_E$

Independent of

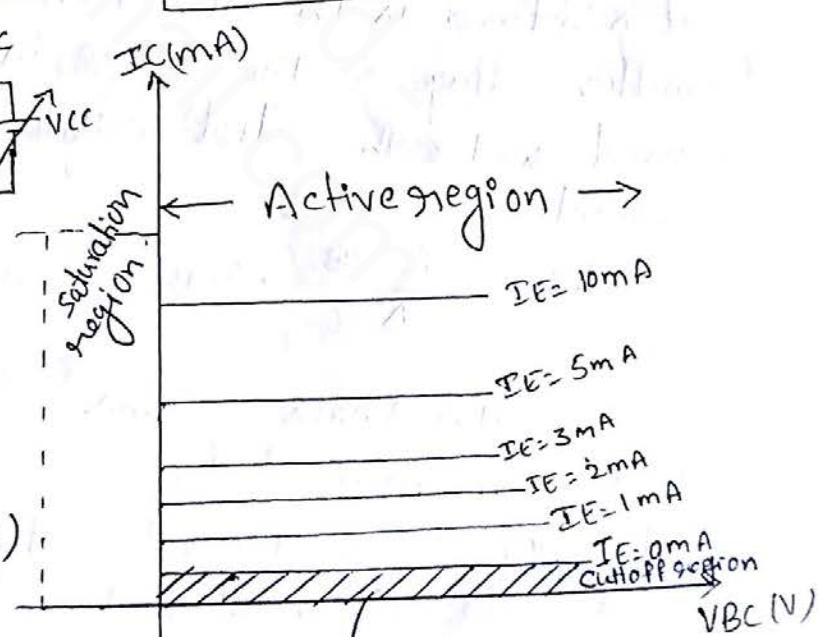
Reverse bias

voltage i.e. V_{BC} (V_{CE})

I_C only depends

on the forward

biased voltage V_{BE} (V_{EE})



Cutoff region.

so that if I_E increases; I_C increases $\therefore I_E \approx I_C$.

The current equation for I_C in terms of I_E since for I_C current output characteristic I_E current is constant.

So the relation b/w the I_C & I_E is

$$I_C = -\alpha I_E + I_{C0} \quad \text{or} \quad I_C = \alpha I_E + I_{C0}$$

$$I_C = \alpha I_E + I_{CB0}$$

The maximum value of α will be one.

$$I_C \leq I_E$$

I_C current is
independent of V_{BC}

so that for common base we get constant current of I_C . That why common base configuration called as constant current source.

H-Parameters of common base:

input impedance: (h_{ib})

It is defined as the ratio of change in the (input) emitter voltage to the change in (input) collector voltage with the (output) collector voltage (V_{CB}) kept constant.

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, V_{CB} \text{ constant}$$

$$h_{ib} = 20 \Omega \rightarrow 50 \Omega$$

h_{ib} units Ohm

output admittance (h_{ob}):

It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) emitter current I_E kept constant.

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, I_E \text{ const.}$$

$$h_{ob} = 0.1 \rightarrow 10 \mu \text{mhos}$$

h_{ob} units mhos

It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant.

$$h_{FB} = \frac{\Delta I_C}{\Delta I_E} \quad V_{CB} \text{ constant}$$

$$h_{FB} \rightarrow h_{FB} = \alpha = \\ h_{FB} = 0.9 \rightarrow 1.0$$

h_{FB} has no units.

Reverse voltage gain. h_{RB} :

It is defined as the ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current I_E , hence

$$h_{RB} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, \quad I_E \text{ constant}$$

$$h_{RB} 10^{-5} \rightarrow 10^{-4}$$

h_{RB} has no units.

Common

Cutoff region

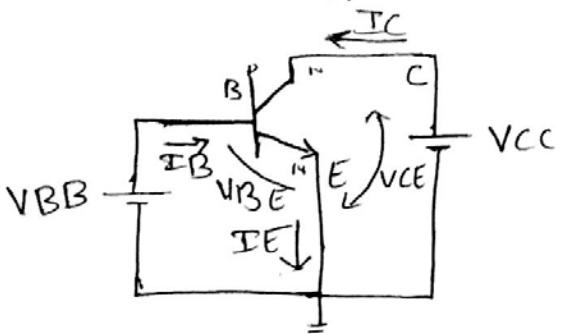
If $I_E = 0$ the transistor is in the cutoff region of its operation. If base lead is open resulting in a current of zero under this condition there is a very small amount of collector leakage current, I_{CBO} . If I_E is Reverse bias w/ the collector junction then only minority current flows i.e I_{LBO} .

Saturation region: Junction is forward biased, when base-emitter current is increased the collector current also increases ($I_C \leq I_E$). The V_{BC} decreases as a result more drop across the collector resistor ($V_{CB} = V_{CC} - I_C R_C$) when V_{BC} reaches its saturation value $V_{BC(\text{sat})}$, the base-collector junction becomes forward biased.

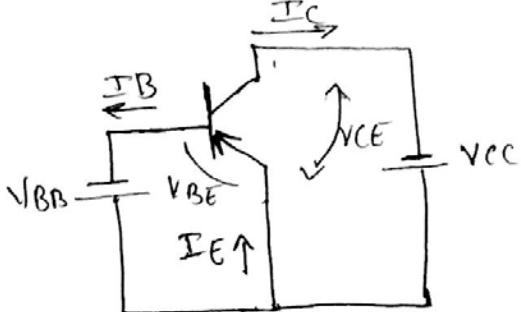
Common Emitter configuration:

In common emitter configuration Emitter is common for both input and output. Base is the input terminal collector is the output terminal.

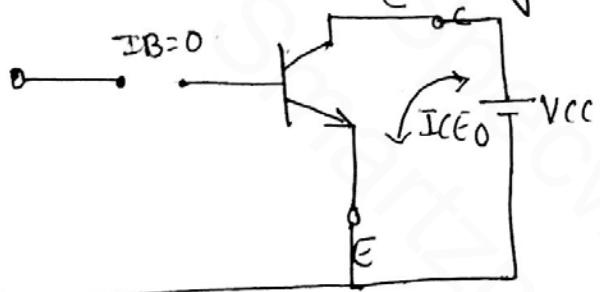
common emitter for NPN.



common emitter for PNP



To find how much reverse saturation current flows in common emitter configuration.



I_{CEO} → base open.
V
collector to emitter
when base open

If base terminal is opened and apply only reverse bias voltage then only minority current flows from collector to emitter so called as I_{CEO} .

To study the characteristics of common emitter configuration, there requires two sets of characteristics.

1. Input characteristics.

2. Output characteristics.

Input characteristics:

To study input characteristics

1. collector to emitter voltage is kept constant.

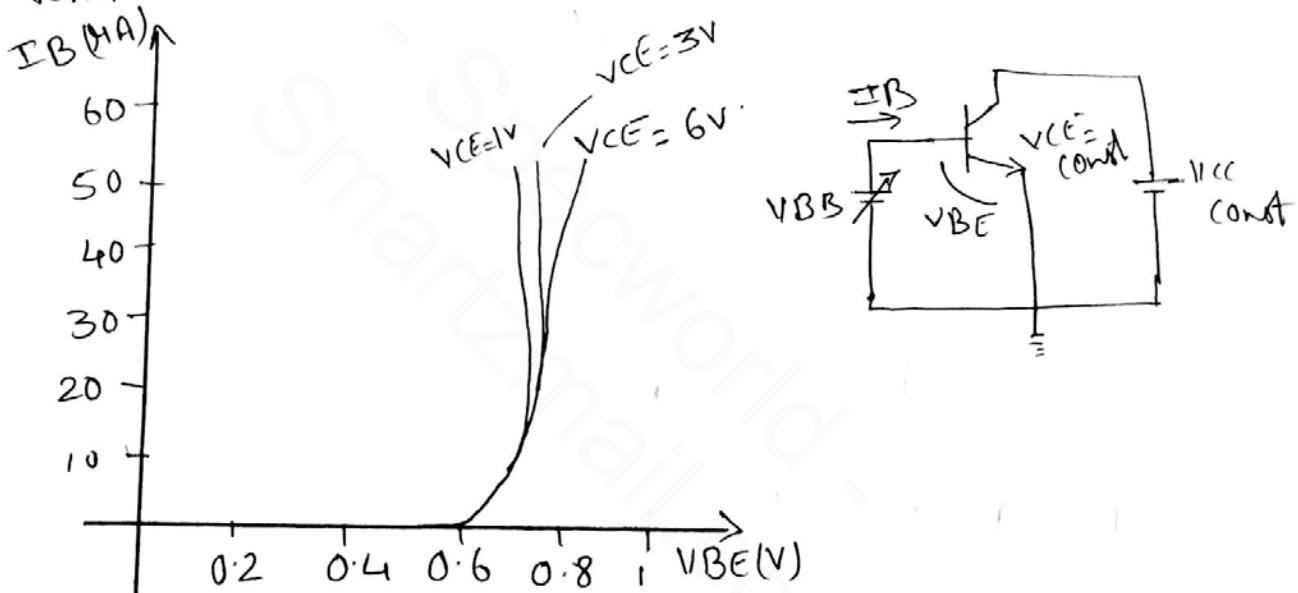
2. The Base current is increased by varying the supply voltage & Note down the values of I_B & V_{BE}

3. Repeat the steps 1 u 2 for higher voltages of V_{BE} .

The input characteristics are a plot of the Input current I_B versus the Input voltage V_{BE} for the range of values of output voltage V_{CE} .

The I_B current is in microamps since it is minority current of Emitter, recombination process current in base & minority current of collector. So that if I_B current is small amount of current that's why it will be in millamps.

The Emitterbase junction is forward bias the plot between I_B w/ V_{BE} in Exponential (format) form.



Due to early effect or Basewidth modulation the I_B current decreases that why by increasing V_{CE} voltage the input characteristics shift way from origin.

Output characteristics:

To study output characteristics

1. Base current kept constant
2. vary V_{CC} voltage note down the readings of V_{CE} w/ I_C
3. repeat 1 u 2 for the higher values of Base

Active region:

If $I_B = 0 \text{ mA}$ (no forward bias voltage) then only the reverse saturation current flows i.e. I_{CEO} .

If I_B current increases then what happens for I_C current? To we have to derive the relationship between I_B & I_C current.

$$I_C = \alpha I_E + I_{CBO} \quad \text{--- (1)}$$

$$I_E = I_B + I_C \Rightarrow I_E = I_B + I_C \quad \text{--- (2)}$$

Substitute (2) in (1)

$$I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \frac{I_{CBO}}{1-\alpha}$$

$$I_C = \beta I_B + \left(\frac{I_{CBO}}{1-\alpha}\right) \rightarrow$$

reverse saturation current (I_E) that is I_{CEO} .

$$I_C = \beta I_B + I_{CEO}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} \quad \text{When } I_B=0 \text{ mA.}$$

For output characteristics we have to plot for V_{CE} vs $I_C (\text{mA})$

If V_{CE} (reverse bias voltage) increases for I_C junction due early effect or base width modulation I_C current increases.

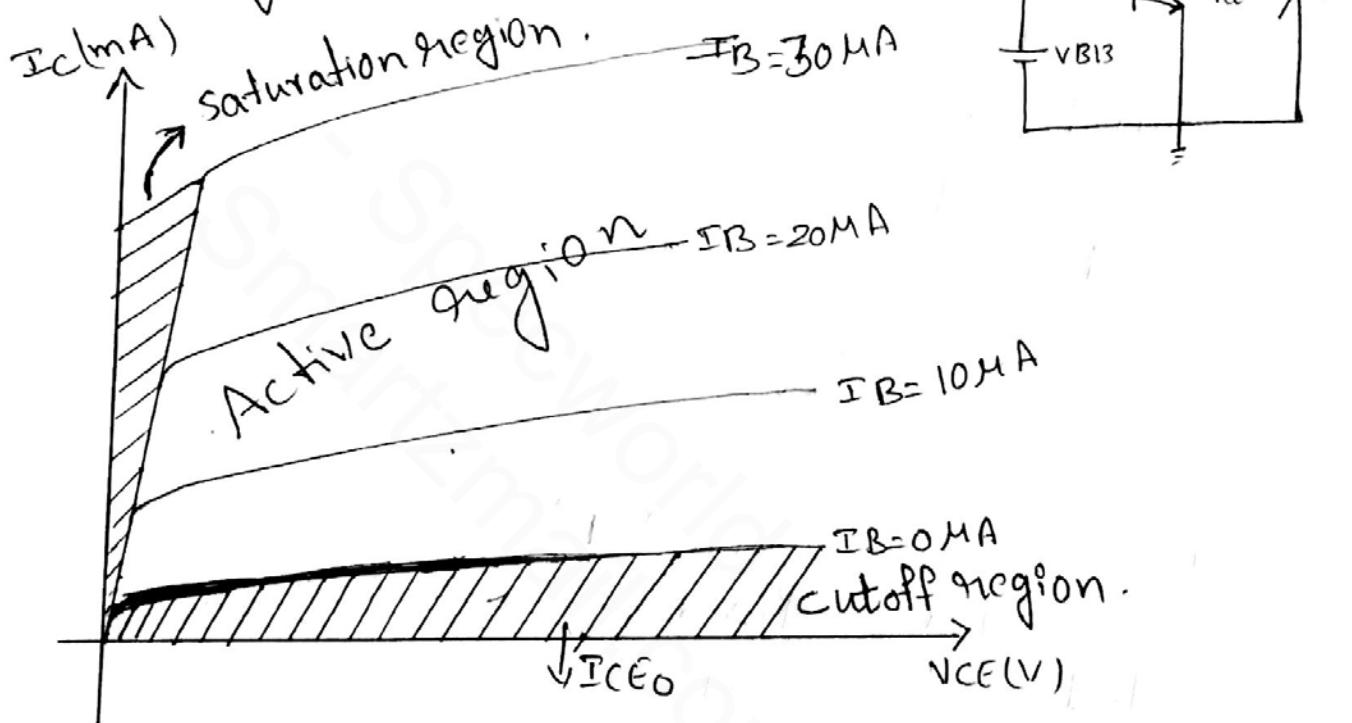
$$\alpha = \frac{I_C}{I_E}$$

increases & also increases that implies β also increases since $\beta = \alpha/1-\alpha$.

SUPPOSE $\alpha = 0.98$ then $\beta = \frac{0.98}{1-0.98} = 49$.

If $\alpha = 0.985$ then $\beta = \frac{0.985}{1-0.985} = 66$.

The α is increased only of 0.005 but β value increased 17% i.e. α by 0.5% results increasing of β by 34%. Hence the output characteristics of CE configuration show a larger slope when compared with CB configuration.



If I_B current increases I_C current increases by β times.

Cutoff

When $I_B = 0$ (base lead open) resulting base current zero under this condition there is very small amount of collector leakage current I_{CEO} . If both base-emitter & base-collector junctions are reverse biased then only minority current i.e. I_{CEO} .

Saturation

When base-emitter junction forward biased by base current increases then the collector current also increases ($I_C = \beta I_B$) as V_{CE} decreases as a result more drop across the collector-emitter junction ($V_{CE} = V_{CC} - I_C R_C$). It reaches saturation value.

Input impedance (h_{ie})

It is defined as the ratio of the change in input base emitter voltage to change in input base current with the collector voltage V_{CE} kept constant.

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, V_{CE} = \text{constant}$$

h_{ie} ranges 500 to 2000

h_{ie} units ohm, Ω

Output admittance (h_{oe})

It is defined as the ratio of change in the output collector current to the corresponding change in the output collector voltage with the input base current I_B kept constant.

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, I_B \text{ constant}$$

h_{oe} → 0.1 to 10 Mmhos

h_{oe} units mhos, Ω

Forward current gain (h_{fe}) (β)

It is defined as a ratio of the change in the output collector current to the corresponding change in the input base current keeping the collector voltage V_{CE} constant.

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} \quad V_{CE} = \text{constant}$$

h_{fe} → 20 to 200

h_{fe} has no units

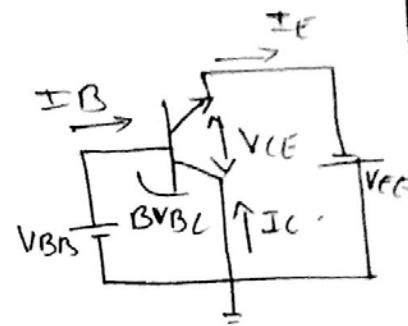
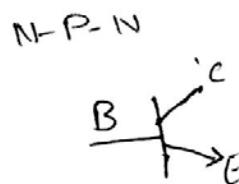
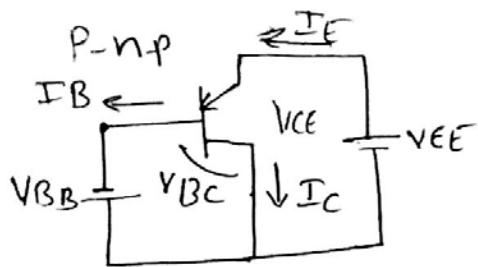
Reverse voltage gain (h_{re})

It is defined as the ratio of the change in the input base voltage and the corresponding change in output collector voltage with constant input base current I_B.

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, I_B \text{ constant}$$

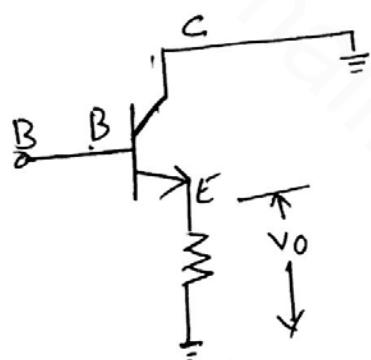
www.jntuworldupdates.org
h_{re} range 10⁻¹⁰ to 10⁻⁸
h_{re} no units.

Common collector configuration:



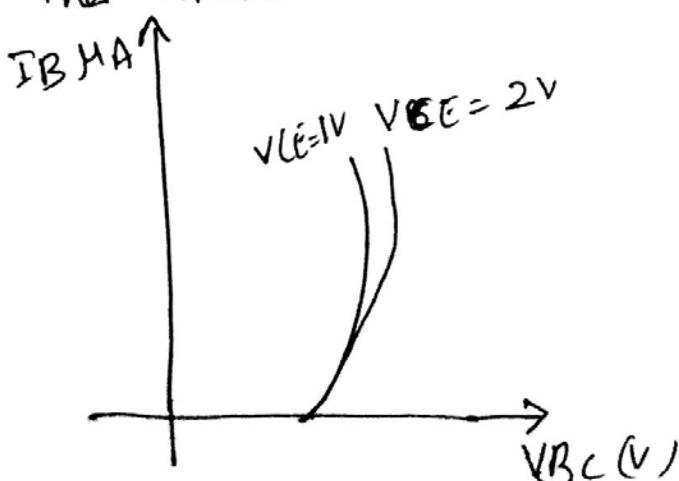
The common collector configuration as shown above fig.
The common collector configuration is used primarily
for impedance matching purposes. Since it has a high
input impedance & low output impedance, opposite
to that of CB or CE.

The common collector circuit configuration with the
load resistance connected from emitter to ground.

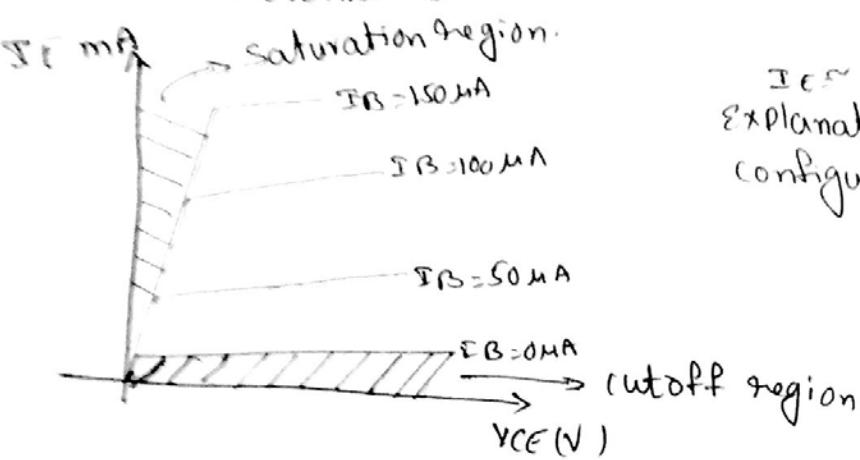


common collector configuration
used for impedance
matching purpose. ch.

The input characteristics



The explanation name as
Common Emitter.



$I_E \approx I_C$ No Name
Explanation on CE
configuration

Current amplification factor:

In c-B configuration current Amplification factor

$$h_{FB} \Rightarrow \alpha = \frac{\Delta I_C}{\Delta I_E}$$

In CE configuration current Amplification factor

$$h_{FE} \Rightarrow \beta = \frac{\Delta I_C}{\Delta I_B}$$

In CC configuration current Amplification factor

$$h_{FC} \Rightarrow r = \frac{\Delta I_E}{\Delta I_B}$$

Comparison of configuration:

	CB	CE	CC
Input resistance	Low (100Ω)	Moderate (750Ω)	High (750Ω)
Output resistance	High ($450 \text{ k}\Omega$)	Moderate ($45\text{k}\Omega$)	Low (25Ω)
Current gain	$1 (\alpha)$	High (β)	High (r)
Voltage gain	About 150	About 500	Less than 1
Phase shift	0 or 360°	180°	0 or 360°
Application	for high freq. circuits	for audio frequency circuits	for impedance matching

Transistor Equations:

$$I_C = \alpha I_E + I_{C0}$$

$$I_C = \alpha I_E + I_{CB0}$$

$$I_C = \beta I_B + I_{CE0}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$I_{CE0} = \frac{I_{CB0}}{1-\alpha}$$

$$\alpha = B \cdot \gamma$$

$$\alpha = \frac{\beta}{\beta+1}$$

$$\gamma = \frac{1}{1-\alpha}$$

$$\gamma = \beta + 1$$

$$I_C = \beta I_B + \underbrace{I_{CE0}}_{\text{neglect}}$$

$$I_C = \beta I_B$$

$$I_E = I_C + I_B$$

$$I_E = \beta I_B + I_B$$

$$I_E = (\beta + 1) I_B$$

Limits of operation .

In the (output) transistor if we increase the Reverse bias voltage at J_C then there are two Possibility

1. Breakdown &
2. Punch through or Reach through.

Breakdown

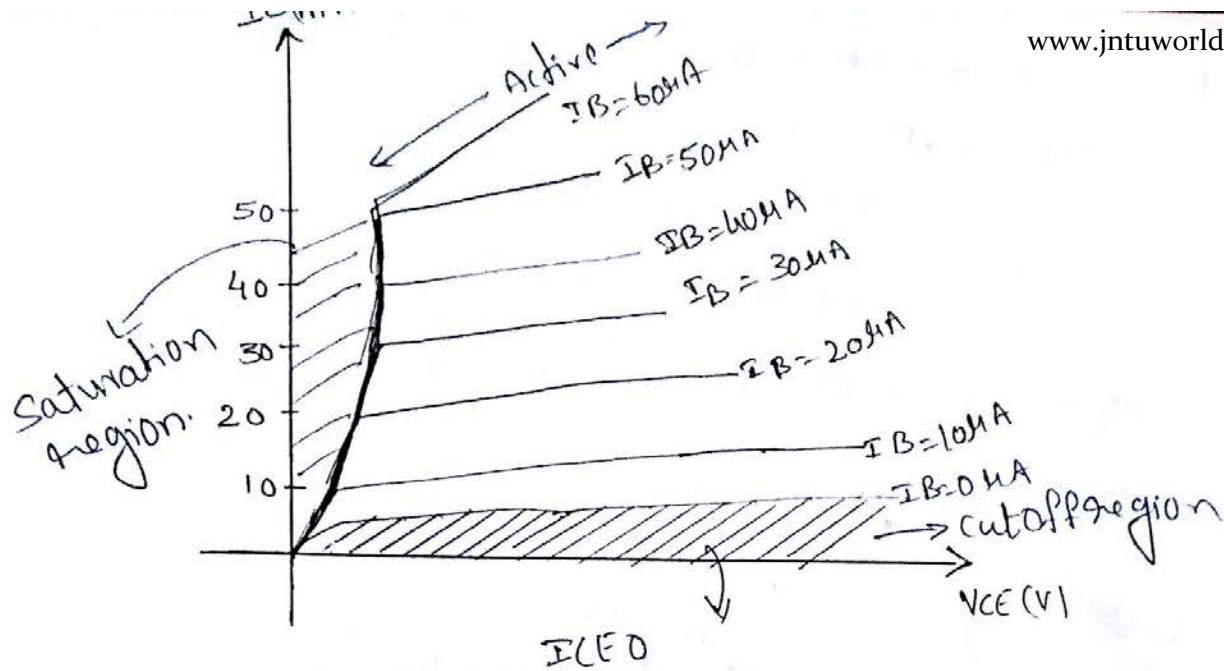
There two broad breakdown occurs,
avalanche breakdown or zener breakdown.

Punch through or Reach through:

If we increase the Reverse bias voltage at J_C region the delection layer of J_C junction increases it will penetrate more in Base than Base width decreases this is known as Base width modulation. If we go on increase the Reverse bias voltage then at particular voltage Base width becomes zero, then it simply behaves a N type or P type material only this is known as Punch through effect or Reach through.

So we have to operate transistor such that it should not enter into Breakdown or punch through effect.

→ For each transistor there is a region of operation on the characteristics that will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion.



The Transistor is wanted to be operated in Active region to act like an amplifier. we have to find what the maximum limits to operate the transistor current I_C in voltage V_{CE} as some will be specified in specification sheet.

The maximum Power dissipation is defined as $P_{max} = V_{CE} \cdot I_C$.

known we have to draw the power dissipation curve for above graph if $P_D = 300\text{mW}$

$$\text{If } I_{Cmax} = 50\text{mA}$$

$$P_{max} = V_{CE} I_C = 300\text{mW}$$

$$V_{CE} \cdot 50\text{mA} = 300\text{mW}$$

$$V_{CE} = 6\text{V}$$

$$Q_1 = (6, 50\text{mA})$$

If $V_{CEmax} = 20\text{V}$ then

$$P_{max} = 20 \cdot I_C = 300\text{mW}$$

$$I_C = 15\text{mA}$$

$$Q_2 (20, 15\text{mA})$$

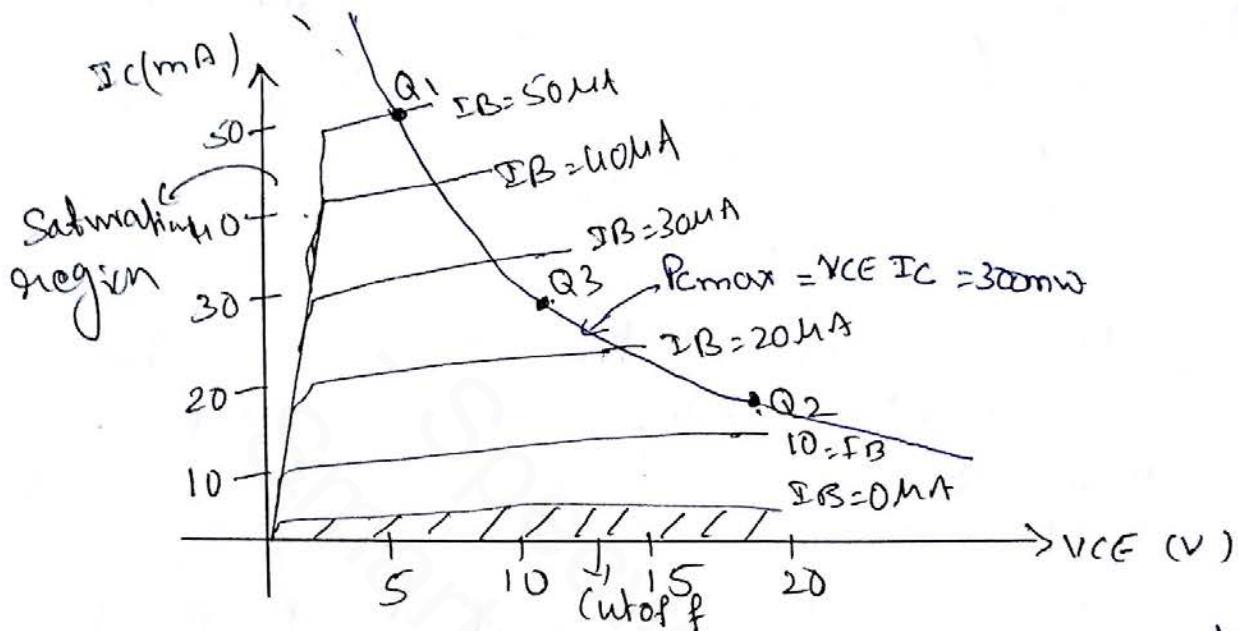
If we choose mid range of I_C ie 25mA then

$$V_{CE}(25\text{mA}) = 300\text{mV}$$

$$V_{CE} = \frac{300\text{mV}}{25\text{mA}} = 12\text{V}$$

$$Q_3 = (12, 25\text{mA})$$

Then Power dissipation curve will be.



If I_C current less than I_{CEO} then it enters in to cutoff region. If I_C current larger than I_{Cmax} or V_{CESat} it enters in to saturation region.

To avoid above problem the transistor should be operated

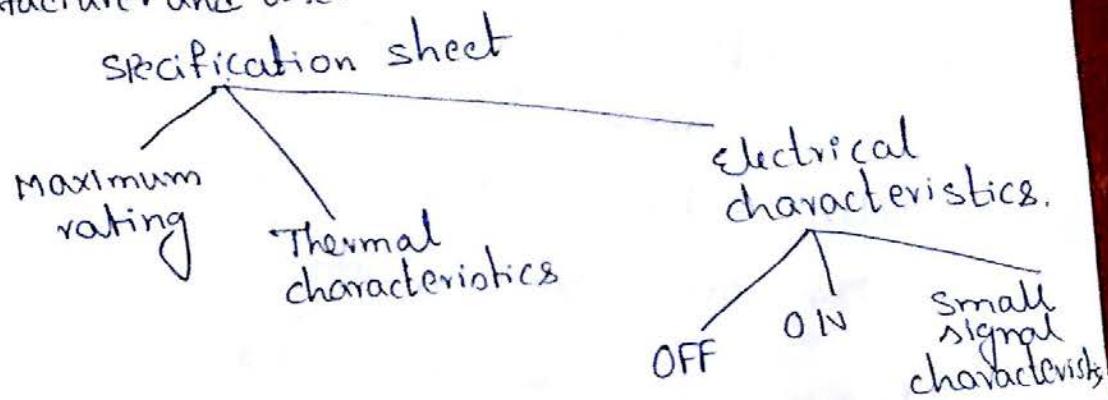
$$I_{CEO} \leq I_C \leq I_{Cmax}$$

$$V_{CESat} \leq V_{CE} \leq V_{CEmax}$$

$$V_{CE} I_C \leq P_{Cmax}$$

Transistor specification sheet:

The specification sheet is the communication link between the manufacturer and user.



Maximum ratings:

Rating	symbol
collector-emitter voltage	V_{CEO}
collector base voltage	V_{CBO}
Emitter base voltage	V_{EBO}
collector current	I_C
Total device dissipation	P_D
$T_A = 25^\circ C$	
Operating & storage junction	$T_j, T_{stg.}$
Temperature range	

Thermal characteristics:

characteristic	symbol
Thermal Resistance, junction to case	$R_{\theta jc}$
Thermal Resistance junction to Ambient	$R_{\theta JA}$

characteristic

OFF characteristic

characteristic

collector - emitter breakdown voltage

collector - base breakdown voltage

Emitter - Base breakdown voltage

collector cutoff current

Emitter cutoff current

ON characteristic.

characteristic

DC current gain

Collector Emitter saturation voltage

Base - Emitter saturation voltage

small signal characteristics.

characteristic

Current - Gain - Bandwidth Product

Output capacitance

Input capacitance

Collector - Base capacitance

Small signal current gain

Current gain - High frequency

Noise Figure

ON characteristics

small signal

symbol

symbol

V_{BR} CEO

V_{BR} CBO

V_{BR} EBO

I_{CBO}

I_{EBO}

symbol

h_{FE}

$V_{CE(sat)}$

$V_{BE(sat)}$

symbol

f_T

C_{obo}

C_{ibo}

C_{cb}

h_{fe}

h_{fc}

N_f

In the previous we discussed in Active region only.

for transistor. The second major application of transistor is for switching applications. When used as an electronic switch i.e if transistor operated in cutoff or saturation they behave like off & ON switches respectively.

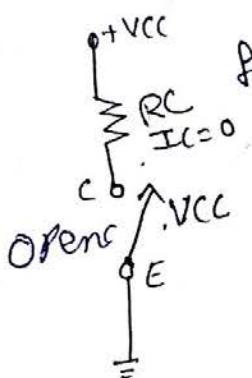
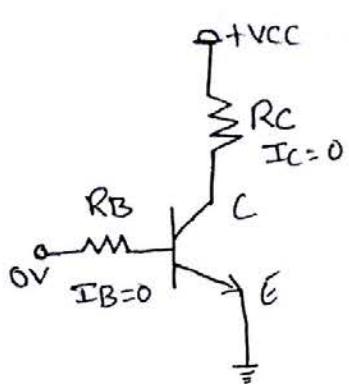
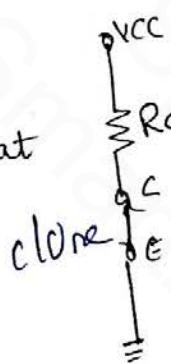
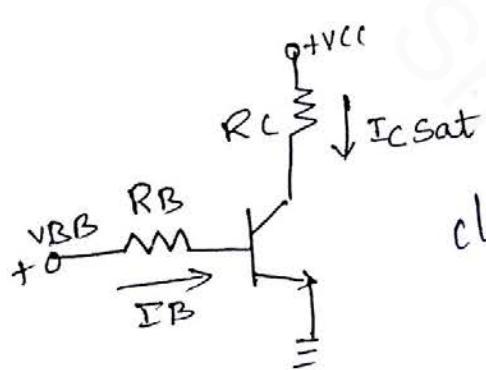


Fig (a) The transistor is in the cutoff region because base-emitter junction is not forward biased. Then the transistor is ideally open between collector & emitter since it is reverse biased. Depletion region is biased more than $R = \infty$ so that opened.

(a) cutoff - open switch.



In fig (b) transistor is in saturation region because base-emitter junction & base-collector junction are forward biased and base current made large

(b) saturation - closed switch.

Enough to cause the collector current to reach its saturation value. Then the transistor is short. Collector-emitter voltage drop across CE is less since shorted ideally $V_{CE} = 0$. in saturation conditions.

Condition in cutoff

A transistor is in the cutoff region when the base-emitter junction is not forward biased. Neglecting leakage current all of the currents are zero, in V_{CE} is equal to V_{CC} .

$$V_{CE(\text{cutoff})} = V_{CC}$$

Conditions in saturation.

When the base-emitter junction is forward biased and there is enough base current to produce a maximum collector current, the transistor is saturated.

The formula for above fig(b) is

$$I_{C\text{ Sat}} = \frac{V_{CC} - V_{CE\text{ Sat}}}{R_C}$$

V_{CE} is small

Or

$$I_{C\text{ Sat}} = \frac{V_{CC}}{R_C}$$

V_{CE} is very small compared to V_{CC} , it can usually be neglected.

The minimum value of base current needed to produce saturation is

$$I_{B\text{ min}} = \frac{I_{C\text{ Sat}}}{\beta_{dc}}$$

I_B should be significantly greater than $I_{B\text{ min}}$ to keep transistor well into saturation.