

UNIT

1

INTRODUCTION TO VLSI DESIGN AND BASIC ELECTRICAL PROPERTIES

Marketed by:



SIA GROUP

PART-A

SHORT QUESTIONS WITH SOLUTIONS

Q1. What is an Integrated circuit?

Ans:

Model Paper-I, Q1(a)

An integrated circuit (IC) is an electronic circuit fabricated on a small semiconductor wafer by building thousands or millions of resistors, capacitors, diodes and transistors on it. ICs are the heart and brains of most circuits.

The integrated circuits are divided into different categories depending on the number of components that are fabricated in the chip. They are,

- (i) Small scale integration (SSI)
- (ii) Medium Scale Integration (MSI)
- (iii) Large Scale Integration (LSI)
- (iv) Very Large Scale Integration (VLSI).

Q2. What is Moore's law?

Ans:

Model Paper-III, Q1(a)

Moore's law is an observation made by Intel cofounder Gordon E. Moore. The law states that the number of transistors that can be positioned on an integrated circuit with little cost increases exponentially. In other words, the transistors that can be positioned on an integrated circuit doubles approximately every two years. The tendency has sustained for more than half a century and is anticipated to continue for another decade and possibly much longer.

Q3. What are the different steps involved in the IC fabrication?

Ans:

The processing steps involved in the fabrication of an integrated circuit are as follows,

1. Wafer preparation
2. Oxidation
3. Photolithography
4. Diffusion
5. Epitaxy
6. Metalization.

WOP | DEM

During a complete fabrication run some of these steps are repeated many times, in different combinations and under different processing conditions.

Q4. Define threshold voltage of a MOS device

Model Paper-III, Q1(b)

Ans:

The minimum amount of gate to source voltage V_g required to produce surface inversion in order to form the conducting channel between the source and the drain is known as the threshold voltage ' V_t '. As long as $V_{gs} < V_t$, no current flows between source and the drain. For $V_{gs} > V_t$, a greater number of minority carriers are pulled to the surface as a result the channel current gets increased.

1.2

Q5. Explain the term figure of merit of a MOS transistor.

Ans:

Figure of merit is a quantity used to characterize the performance of a device comparative to other devices of the similar kind. In engineering, Figure of Merit (FOM) is frequently defined for specific materials or devices to determine their relative usefulness for an application.

MOS transistor figure of merit is denoted as ω_o .

The parameter ω_o indicates the frequency response of MOS transistor. It is defined as,

$$\omega_o = \frac{g_m}{C_{gs}} = \frac{\mu}{L} (V_{gs} - V_t) = \left(\frac{1}{\tau_{rd}} \right)$$

Q6. Draw the circuit diagram of NMOS and CMOS inverter

Ans:

The basic circuit of nMOS inverter is shown in figure (1)

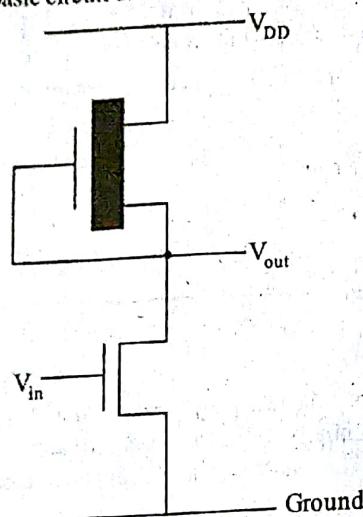


Figure (1).

The basic circuit of CMOS inverter is shown in figure (2)

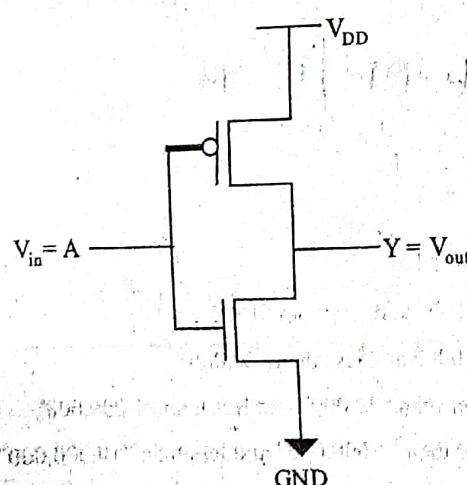
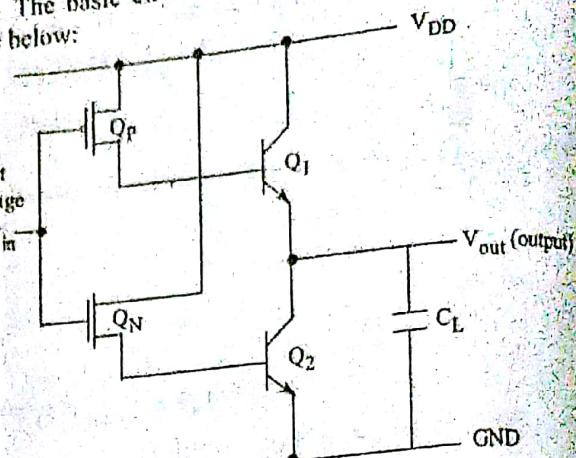


Figure (2)

Q7. Draw the circuit diagram of BiCMOS inverter

Ans:

The basic circuit of BiCMOS inverter is shown in figure below:



Figure

Q8. Write the expression of I_{ds} in terms of V_{ds} for both saturated and non-saturated regions.

Model Paper-II, Q1(b)

Ans:

The expression for I_{ds} in terms of V_{ds} is given by,

$$I_{ds} = C_o \mu \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

(for non-saturated region).

$$I_{ds} = \frac{C_o \mu W}{2L} (V_{gs} - V_t)^2 \text{ (for non-saturated region)}$$

Q9. Write the expression for threshold voltage of a MOSFET.

Ans: The threshold voltage, V_t of a MOSFET expressed as,

$$V_t = \phi_{ms} \frac{Q_B - Q_{ss}}{C_o} + 2\phi_{fN}$$

Where,

Q_B = The charge per unit area in the depletion layer beneath the oxide.

Q_B = Charge density at Si:SiO₂ interface.

C_o = Capacitance per unit gate area.

ϕ_{ms} = Work function difference between gate and silicon.

ϕ_{fN} = Fermi level potential between inverted surface and bulk silicon.

Q10. Write the expression for transconductance of an n-channel enhancement MOSFET.

Model Paper-II, Q1(b)

Ans:

The expression MOSFET is given by,

$$g_m = \beta (V_{gs} - V_t)$$

UNIT

2

VLSI CIRCUIT DESIGN PROCESSES



PART-A

SHORT QUESTIONS WITH SOLUTIONS

Q1: Draw the block diagram of design flow in manufacturing VLSI chip.

Ans:

The block diagram of design flow in manufacturing VLSI chip is shown in figure below.

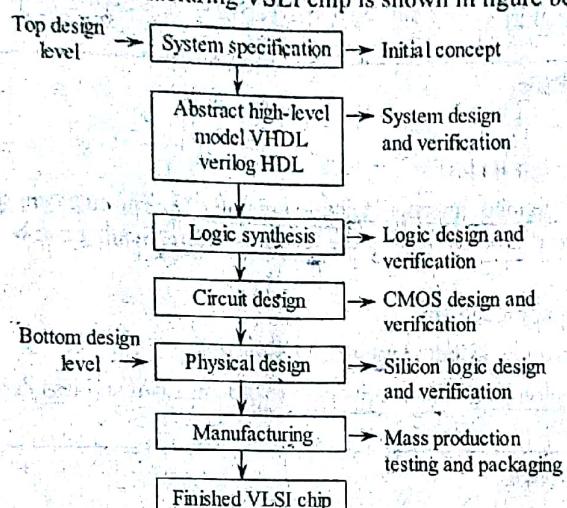


Figure: Major Steps in Design of VLSI Chip

Q2: Why is VLSI design process presented in nMOS only?

Ans:

Model Paper-I, Q1(c)

Due to the good performance, yield and reliability of nMOS over pMOS and bipolar, the fabrication process of nMOS is less expensive than CMOS process. VLSI design process is present in nMOS only.

When power consumption becomes a major factor in the design of a VLSI circuit nMOS is replaced with CMOS. Since, CMOS consumes very little power (negligible).

Q3: What is a stick diagram?

Model Paper-I, Q1(d)

Ans: A stick diagram is a cartoon of chip layout, which helps abstract a model for design of full layout from conventional transistor schematic. Stick diagrams convey the layer information by means of monochrome encoding of the lines so that black and white copies of stick diagrams do not lose the layer information.

Q4. Compare the NMOS and CMOS design styles

Ans:

Model Paper-III, Q1(d)

Comparison between nMOS and CMOS Design Styles

nMOS Design Style	CMOS Design Style
1. In nMOS design style, implant (yellow) and the buried contact (brown) are used.	1. In CMOS design style, absence of depletion mode devices, yellow colour is used to represent p-transistors and wires.

2.	In this, enhance mode transistors are represented without implant and depletion mode transistors are represented with implant.	2.	In this, n-type enhance mode transistors are represented below the demarcation line and p-type enhance mode transistors are represented above the demarcation line.
3.	In this style, all the transistors are arranged randomly.	3.	In this style, n-type transistors are arranged below the demarcation line and p-type transistors are arranged above the demarcation line.
4.	In this style, it is essential to place crosses on the V_{DD} and V_{SS} rails to represent the substrate and p-well connection.	4.	In this style, it is essential to place crosses on the V_{DD} and V_{SS} rails to represent the substrate and p-well connection respectively.

Q5. What are design rules?

Ans:

Model Paper-III, Q1(c)

In VLSI design, as complexity of the process increases, it is difficult for the designers to comprehend the complications of the fabrication process and understand the relations between the different photomasks. Therefore a set of design rules have been defined. They act as interface or communication link between the circuit designer and process engineer in the manufacturing phase. The aim of the design rules is to acquire a circuit with optimum yield in as small area as possible without compromising dependability of the circuit. Further, design rules can be conservative or aggressive, depending on whether yield is desired or performance is desired.

Q6. What are Scalable Design Rules

Ans:

Scalable Design Rules (λ -based Design Rules)

In this approach, all rules are defined in terms of single parameter λ . The rules are so chosen that a design can be easily ported over a cross section of industrial process making the layout portable. Scaling can be easily done by simply changing the value of λ .

The key disadvantages of this approach are,

- (a) Linear scaling is possible only over a limited range of dimensions.
- (b) Scalable design rules are conservative. This results in over dimensioned and less dense design.
- (c) This rule is not used in real life.

Q7. What are Scalable Design Rules

Ans:

Model Paper-II, Q1(b)

Absolute Design Rules (μ -Based Design Rules)

In this approach, the design rules are expressed in absolute dimensions (e.g. $0.75 \mu\text{m}$) and therefore can exploit the features of a given process to a maximum degree. Here, scaling and porting is more demanding and has to be performed manually or using CAD tools. Also, these rules tend to be more complex especially for deep submicron. The fundamental unity in the definition of a set of design rules is the minimum line width. It stands for minimum mask dimension that can be safely transferred to the semiconductor material. Even for same minimum dimension design rules tend to differ from company to company and from process to process.

Q8. What is the need of scaling?

Ans:

Model Paper-II, Q1(c) | April-11, Set-2, Q7

Scaling is required to improve the performance of the MOS circuits. Following are the improvements that can be obtained by scaling.

- (i) More speed and less power consumption
- (ii) Better device characteristics
- (iii) Higher chip density i.e., the number of gates located on the chip is high
- (iv) Less parasitic capacitance
- (v) Low interconnect delays between devices
- (vi) Low chip cost.

UNIT

3

GATE LEVEL DESIGN

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PART-A SHORT QUESTIONS WITH SOLUTIONS

Q1. What is a CMOS logic gate?

Ans:

Model Paper-I, Q1(e)

A CMOS logic gate contains two networks, the Pull-Up Network (PDN) made up of NMOS transistors and the Pull-Up Network (PUN) made up of PMOS transistors. Hence, for the three input gates denoted in figure (a), the PDN conducts for all input combinations that need a low output ($Y = 0$) and then pull the output node down to ground producing a zero voltage to occur at the output, $V_y = 0$. Concurrently, the PUN is OFF, and no direct D.C path dwell in between V_{DD} and ground. The PUN conducts for all input combinations that need a high output ($Y = 1$) and then pull the output node upto V_{DD} , building an output voltage $V_y = V_{DD}$. Concurrently, the PDN is cutoff and no D.C current path exists between V_{DD} and ground.

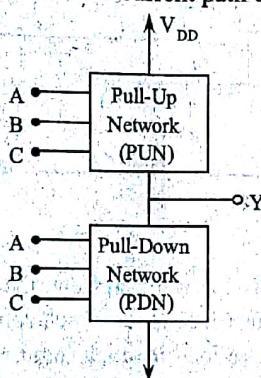


Figure (a): Representation of a Three Input CMOS Logic Gate

Q2. Explain about switch logic.

Ans:

Figure shows a MOS transistor switch built by connecting n-type and p-type transistors in parallel. The switch transmits logic 0 and logic 1 equally well from source to drain. So it is called as a transmission gate. When V_{DD} or V_{SS} is given at the drain, one gets V_{DD} or V_{SS} at the source. However, it needs two transistors and their accompanying biasing. It needs both true and complement form of the gate signal.



Figure: A Complementary Transmission Gate

3.3

Q3. What are the advantages and disadvantages of dynamic logic?

Ans:

Advantages

- ❖ Dynamic logic is twice faster than normal static logic.
- ❖ Attractive for high speed circuits.
- ❖ It uses only the faster N-type transistor.
- ❖ It is amenable to transistor sizing optimization.
- ❖ Widely used in high performance processor.

Disadvantages

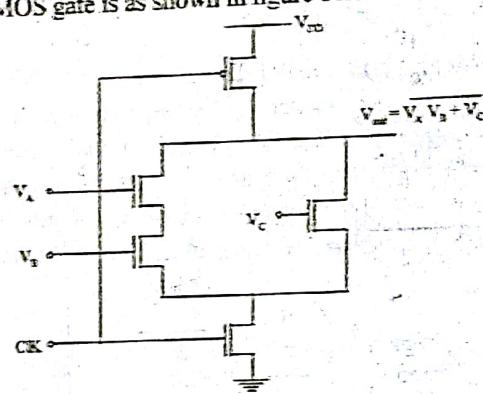
- ❖ Dynamic gates suffers from charge sharing.
- ❖ Dynamic gates are very sensitive to noise. Such as - Capacitive cross talk, Charge sharing, Power supply noise.

Q4. Draw the basic structure of a dynamic CMOS gate

Model Paper-I, Q1(b)

Ans:

The basic structure of a dynamic CMOS gate is as shown in figure below



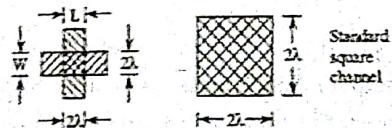
Figure

Q5. Define the standard unit of capacitance.

Model Paper-II, Q1(a)

Ans:

Standard Unit of Capacitance (C_s): Real devices have parasitic elements that are necessary of the device structure. The transistor itself introduces significant gate capacitance, C_g . This capacitance which comes from the parallel plates formed by the polygate and the substrate forms the majority of the capacitive load in small logic circuits. The total gate capacitance is computed by measuring the area of the active region (or $W \times L$) and multiplying the area by the unit capacitance C_s . It is convenient to employ a standard unit of capacitance that can be given a value appropriate to the technology and can also be used in calculations without associating it with an absolute value. The unit is denoted by C_s and is defined the gate-to-channel capacitance of a MOS transistor having $W = L$ = feature size, that is 'standard' square as shown in figure (a).

Figure (a): Standard Square Channel $2\lambda \times 2\lambda$

Q6. What is a Super buffers

Ans:

An inverter when used to drive more significant capacitive loads, gives rise to delay problems that are inevitable. One of the method to overcome these delay problems is super buffer.

A super buffer is a symmetric gate that can deliver or eliminate large currents and switch large capacitive loads speedily than a standard inverter.

There are two types of super buffers,

- (i) Inverting NMOS super buffer
- (ii) Non-Inverting NMOS super buffer.

UNIT-3 (Gate Level Design)

Q7. Write the expression for Rise-time, τ_R and Fall-time, τ_F in the case of CMOS Inverter.

Ans:

Model Paper-III, Q1(f)

The expression for rise time τ_R in the case of CMOS inverter is

$$\tau_R = \frac{3C_L}{\beta_p V_{DD}}$$

The expression for fall time τ_F in the case of CMOS inverter is

$$\tau_F = \frac{3C_L}{\beta_n V_{DD}}$$

Q8. Calculate the gate capacitance value of 5 mm technology minimum size transistor with gate to channel capacitance value is 4×10^{-4} pF/mm².

Ans:

Model Paper-II, Q1(f)

Given that,

Gate to channel capacitance value = 4×10^{-4} pF/ μm^2

and 5 μm technology minimum sized transistor.

For 5 μm MOS circuits

Area/standard square = $5 \mu\text{m} \times 5 \mu\text{m} = 25 \mu\text{m}^2$

Gate to channel capacitance value = 4×10^{-4} pF/ μm^2

Thus, standard gate capacitance value is,

$$\square C_g = 25 \mu\text{m}^2 \times 4 \times 10^{-4} \text{ pF}/\mu\text{m}^2$$

$$\therefore \square C_g = 0.01 \text{ pF}$$

Q9. What is Peripheral Capacitance?

Ans:

Model Paper-I, Q1(f)

The source and drain p-diffusion regions forms junctions with the n-substrate (or well) at well defined and uniform depths. Similarly, the source and drain n-diffusion regions forms junctions with the p-substrate at well defined and uniform depths. Hence, for diffusion regions each diode thus formed will associate a peripheral or side-wall capacitance with it. As a whole the peripheral capacitance, C_p will be in the order of pF/unit length. So, its value will be greater than C_{area} of the diffusion region to substrate.

C_p increases with reduction in source or drain area. Total diffusion capacitance is given by,

$$C_{diff} = C_{area} + C_p$$

However, as the n and p-active regions are formed by impure implants at the surface of the silicon in case of orbit processes, they have negligible depth. Hence, C_p is quite negligible in them.

UNIT

4

DATA PATH SUBSYSTEMS AND ARRAY SUBSYSTEMS

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PART-A SHORT QUESTIONS WITH SOLUTIONS

Q1. What is a shifter?

Ans:

A shifter is most widely used for arithmetic operations. Usually shifting is equivalent to multiplication by powers of two. Shifting is required during floating-point arithmetic. The shift register is one of the simplest shifters that can shift by one position per clock cycle.

Model Paper-I, Q1(g)

Q2. Why is the static 6-transistor cell used for average CMOS system design?

Ans:

The static 6-transistor cell is used for average CMOS system design, because it provides the least amount of detailed circuit design, least amount of process knowledge, it is noise effective and also the current processes are dense enough for allowing large static RAM arrays.

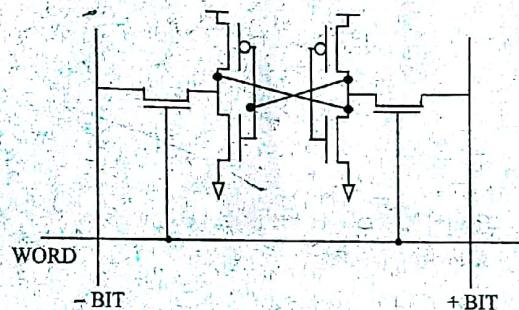


Figure: Static 6-transistor Cell

Q3. Write a short note on Ripple-carry adder

Ans:

The n-bit adder fabricated from n one-bit adders is known as a ripple-carry adder. A ripple-carry adder executes addition operation, which is not completed until the $(n - 1)$ th adder has calculated its S_{n-1} output. The result obtained with the above operation depends on input C_i and so on down the line, so the critical delay path goes from the 0-bit inputs up through the C_i 's to the $(n - 1)$ bit. The most important advantages of this adder is, it is area efficient and easy to design. The drawback of this adder is, it is slow when n is large.

Q4. Write a short note on Full adder.

Ans:

A full adder is the basic adder that computes a one-bit sum and carry from two addends and a carry-in. The sum and carry out equations for the full adder are,

$$S_i = a_i \oplus b_i \oplus c_i$$

$$C_{i+1} = a_i b_i + a_i c_i + b_i c_i$$

Where,

S_i — Sum at the i^{th} stage

C_{i+1} — Carry out of the i^{th} stage



Q5. How can the components of CMOS system design be categorized into the groups?

Ans:

The components of CMOS system design be categorized into following groups. They are,

- (i) Data path operators
- (ii) Memory elements
- (iii) Control structures
- (iv) I/O cells.

Model Paper-III, Q1[1]

After categorizing the groups, the CMOS subsystems that implement those functions are designed.

Q6. What is a datapath? What is its significance in digital processors?

Ans:

Model Paper-I, Q1[1]

Datapath: A datapath is a group of functional units similar to arithmetic logic units or multipliers that carry out data processing operations. The objective of datapath is to provide routes for data to travel among functional units.

Significance of Datapaths in Digital Processors: Datapaths in digital processors,

- (i) Perform arithmetic logical and shift operations
- (ii) Acts as temporary storage of operands.

Model Paper-II, Q1[1]

Q7. Draw the circuit of transistor dynamic RAM core cell.

Ans: The circuit diagram for a one-transistor dynamic RAM core cell is shown in figure below:

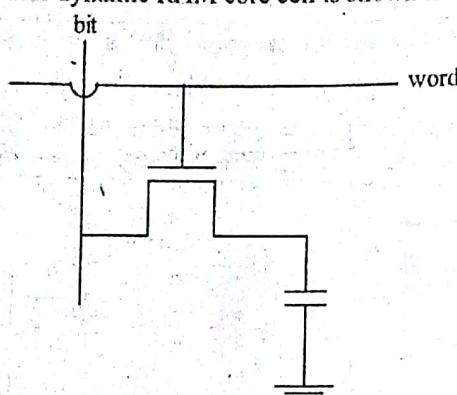


Figure: A One-Transistor Dynamic RAM Core Cell

Q8. What is meant by Read Only Memory(ROM)?

Ans:

Model Paper-III, Q1[1]

A Read Only Memory (ROM) is a non-volatile memory, wherein the state is retained indefinitely even in the absence of power. The ROM cell can be configured using only one transistor per storage bit. Design of a ROM array is carried out as a single-ended NOR array using any structure of NOR gate such as pseudo-nMOS and footless dynamic NOR gate. While precharging the wordline in a dynamic NOR gate, it must be pulled down to low. ROM can be implemented very easily using pseudo-nMOS structure when acceptable amount of DC power is dissipated and required speed is achieved without any timing constraints. In order to reduce the amount of dissipated DC power in multiplexed ROM structure, a pull-up transistor is placed after column multiplexer.

Q9. Explain briefly about programmable ROMs.

Ans:

PROM is a non-volatile ROM, that can be programmed (or) reprogrammed even after its manufacture. The programming and writing speeds of PROM is comparatively slower than the reading speeds of ROMs.

There are about four types of non-volatile memories,

- (i) Programmable ROMs (PROMs)
- (ii) Erasable Programmable ROMs(EPROMs)
- (iii) Electrically Erasable Programmable ROMs (EEPROMs)
- (iv) Flash memories.

UNIT

5

PROGRAMMABLE LOGIC DEVICES AND CMOS TESTING



PART-A SHORT QUESTIONS WITH SOLUTIONS

Q1. Explain the principle of PLA.

Ans:

Programmable Logic Array (PLA)

A programmable Logic Array (PLA) is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a set of programmable OR planes and which can then be conditionally complemented to produce an output. It has 2^N AND gates for N input variables and for M outputs from PLA, there should be M OR gates, each with programmable inputs from all of the AND gates. This layout allows for a large number of logic functions to be synthesized in the sum of products (and sometimes product of sums) canonical forms.

Q2. What are the advantages and disadvantages of PLA's? Explain about the applications of PLA's.

Model Paper-I, Q1(i)

Ans:

Advantages

1. If two or more output functions have a common product term that can be shared by different OR gates the PLA area can be reduced.
2. These offer enhanced flexibility in the design of complex systems.

Disadvantage

The propagation delay of the gate will cause the inverted input to change for a short time after the application of non-inverted signal.

Applications

1. These are used to implement control over a data path.
2. The regular structure of PLA's with programmable AND and OR array's is used in complex systems involving many variables.
3. PLA's are used to perform programmable logic sequencing and finite state machine operations with the registers at input and output.

Q3. Write in short about channelled gate arrays.

Model Paper-II, Q1(i)

Ans:

Channelled Gate Array

A channelled gate array is shown in figure. The important characteristics of this type of masked gate array are,

1. Only a customized interconnect is available.
2. The interconnect uses a predefined space between the rows of base cells.
3. The manufacturing lead time may vary from two days to two weeks.

Q4. Write briefly about channel-less gate arrays with neat sketches.

Ans:

Channel-less Gate Array

The Channel-less gate array is also referred as sea-of-gates (SOG) array or channel-free gate array and is shown in figure. The important characteristics of this type masked gate array are,

5.2

- Only a few of the top mask layers are customized.
- The manufacturing lead time may vary from two days to two weeks.

Q5. What are FPGAs?**Ans:****Field Programmable Gate Arrays (FPGAs)**

A field programmable gate array is a semiconductor device containing programmable logic components called 'logic blocks' and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND and XOR or more complex combinational functions such as decoders or simple mathematical functions. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

Q6. Write the advantages and disadvantages of FPGAs

Model Paper-II, Q10

Ans:**Advantages**

- Shorter time to market.
- Ability to reprogram in the field to fix bugs.
- Lower non-recurring engineering costs.

Disadvantages

- FPGAs are slower compared to ASIC counter parts.
- They cannot handle complex designs.
- Consume more power for any semiconductor process.

Q7. Explain the term observability.

Model Paper-III, Q10

Ans:**Observability**

Observability of any internal node is a degree to which it can be observed that node at output operates correctly. It is very useful to a tester/engineer to measure the output of a gate with in a complex circuit to check its correct operation the main goal of any design engineer is that easy observation of gate outputs. Higher observability indicates the less number of cycles required to measure output node value.

Q8. Explain the term controllability.

Model Paper-II, Q10

Ans:**Controllability**

The controllability is defined as ability of setting a particular logic signal to '0' or '1'. It is used to analyze the difficulty of testing a particular circuit. These value setting can be done by the input pads [IP's]. The main goal of any designer is to design the easily controllable nodes. So it is possible to control easily by using IP's.

Q9. What is ATPG?

Model Paper-I, Q10

Ans:**Automatic Test Pattern Generation (ATPG)**

ATPG is defined as the mechanism which is used in semiconductor electrical testing where the appropriate input patterns check a device for faults which are automatically generated by a program. The vectors are sequentially applied to the device under test and the device response to each set of inputs is compared with the expected response from a good circuit. An 'error' in the response of the device means that it is faulty. The effectiveness of ATPG is measured primarily by the fault coverage achieved and the cost of performing the test.

Q10. What is mean by level sensitive of logic system?**Ans:****Level Sensitive of Logic System**

A logic system is said to be level sensitive if it contains the following rules.

- Steady state response at any input stage is independent of wire delays and circuits.
- The response is also independent of a change in input, either it is one or more than one input. The gate results of all logic system are known as steady state response.

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