

Why we are using electronics in daily norms. why not electrical devices

Electronic Components are more Reliable

Low power dissipation

low cost

low Volume

But more Sophistication and Complexity.

Upto 1950 electronic device technology was dominated by Vacuum tube.

Transistor was invented by William B. Shockley, Walter H. Brattain in 1947.

Integrated circuit → All active and passive Components connecting together with logic.

Integrated circuit was developed by John Bardeen of Bell Laboratories nearly in 1960.

IC generations :- Usually 4

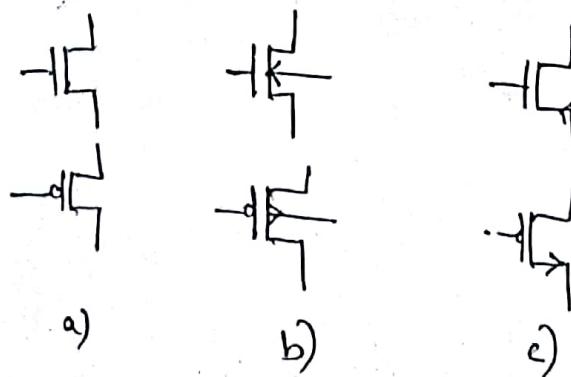
- 1) SSI (Small Scale Integration)
- 2) MSI (Medium Scale Integration)
- 3) LSI (Large Scale Integration)
- 4) VLSI (Very Large Scale Integration)
- 5) ULSI (Ultra large scale Integration)

Year	1947	1950	1961	1966	1971	1980	1990	2000
Technology	Bipolar Transistor	Discrete Components	SST	MST	LST	VLSI	ULSI	ESI
Approximate number of transistors on a chip	1	1	10-100	100-1000	1000-10,000	20,000 - 10,00,000	100,000 - 1,00,00,000	>1,00,00,000
Typical products	-	Function Transistor and diode	Planar devices, logic Gates, flip flops	Counters, Multiplexers Adders	8-bit Microprocessor RAM, ROM	16-bit Special bit MP, Processors Sophisticated peripherals, machines, Smartphones	Virtually anything	

MOS Transistor Theory

Mos transistor acts as a Ideal switch. MOS means Metal Oxide Semiconductor.

Mos transistor Symbols



- a) Indicates the necessary switch logic to build a function.
- b) Indicates if the body (Substrate or well) connection needs to be shown.
- c) Indicates an example of other symbols that may be encountered.

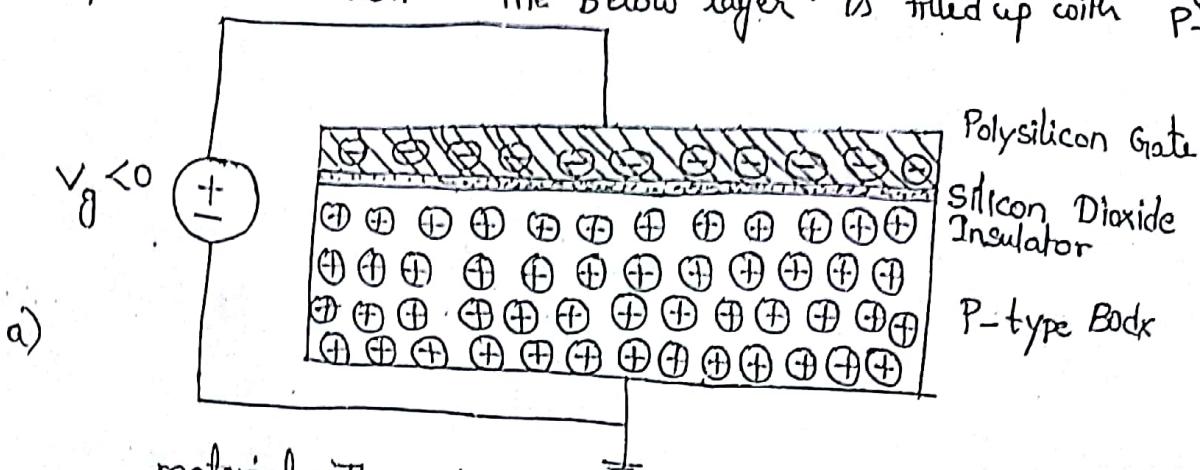
How the mos will operate.

- Mos transistor is a majority carrier device. It has a conduction channel between source and drain. The amount of current will be flows in a conducting channel after applying voltage to the gate.
- Two types of MOSFETs are there.
 - 1) NMOS
 - 2) PMOS

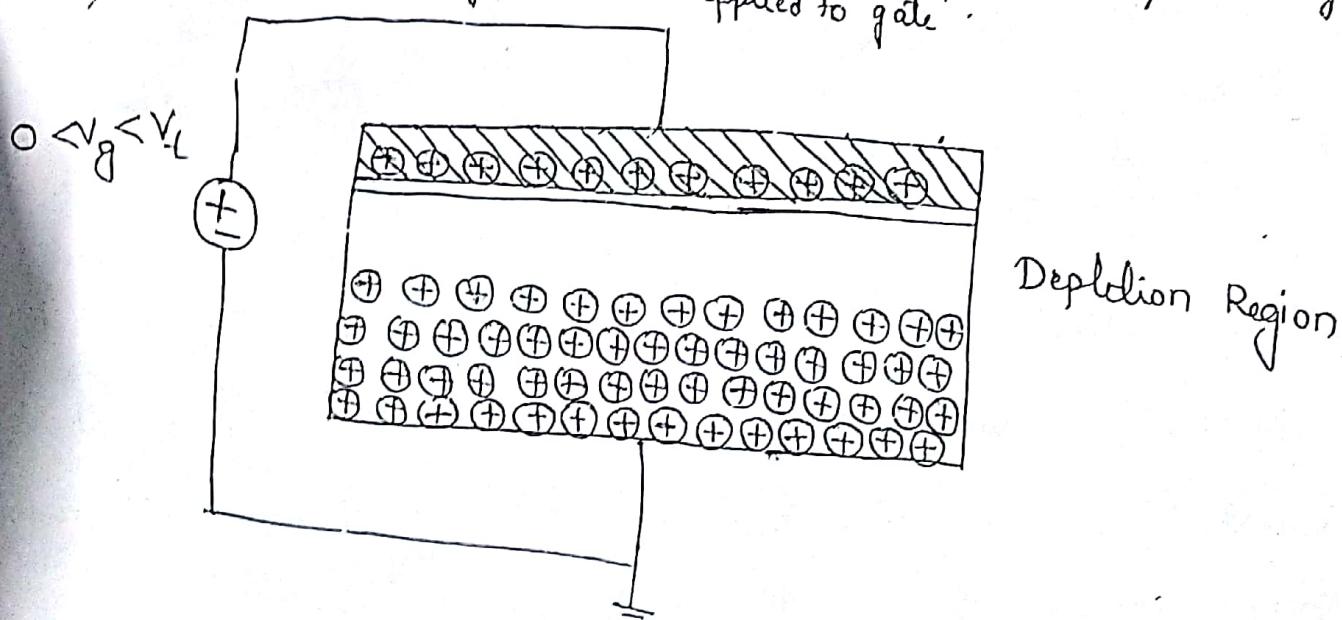
In NMOS, majority carriers are electrons. In PMOS, majority carriers are holes.

MOS Structure

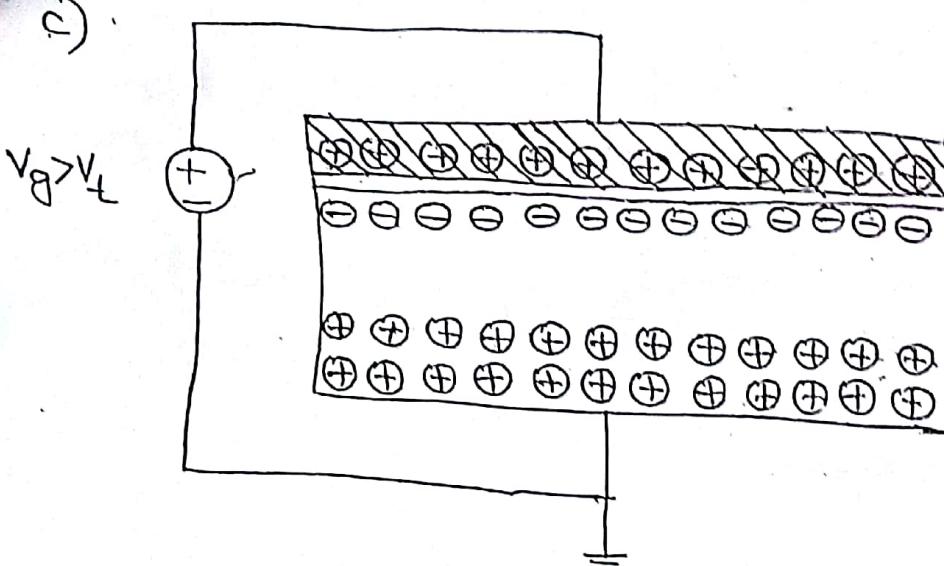
- The top layer is called gate. It is made up of poly Silicon. It is a good conductor.
- The middle layer is a very thin insulating film of Si called gate oxide.
- The bottom layer is called body. The below layer is doped with Silicon. The below layer is filled up with P-type



- b)
- majority carriers are holes. Generally, the body will be grown



The current flows from the gate to the body.



Inversion Region.

Depletion Region.

From figure (a) a negative Voltage is applied to the gate, so there is negative charge on the gate. In body positive negative voltage carriers (electrons) and positively charged carriers (holes) are attracted. This is called accumulation.

From Figure (b) a low positive Voltage is applied to the gate, so positive charge will be there on the gate. The holes in the body are repelled from the region directly beneath the gate, we can call this area as depletion region forming below the gate.

From (c) apply higher potential greater than threshold Voltage V_t is applied. So more positive charge is on the gate. So holes are repelled further and a small number of free electrons in the body are attracted to the region beneath the gate. This forms a layer of

Introduction :-

Why we are using electronics why not electrical devices in daily norms.

Because electronic Components are more

- Reliable
- Low power dissipation
- Low Cost

and is having more Sophistication and Complexity

IC

↓
Integrated Circuit → Having Logic and analog integrated circuit.

Upto 1950 electronic device technology was dominated by Vacuum tube.

Transistor → 1947 by William B. Shockley and Walter H. Brattain

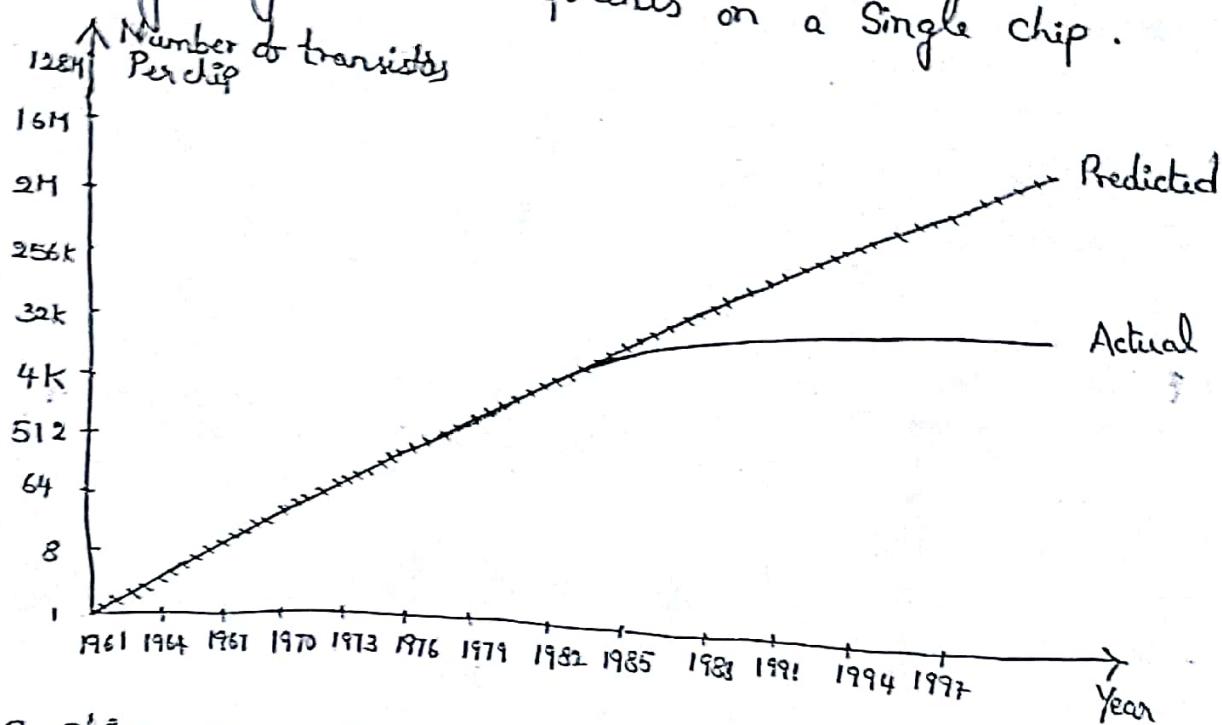
Integrated circuit was developed by John Bardeen of Bell Laboratories nearly in 1960.

IC - 4 generations

- 1) SST (Small Scale Integration)
- 2) MTI (Medium Scale Integration)
- 3) LST (Large Scale Integration)
- 4) VLSI (Very Large Scale Integration)
- 5) ULSI (Ultra Large Scale Integration) (3 million devices on 1 square centimeter)

CMOS

CMOS has become the dominant fabrication process for high performance and low cost. So demand is increasing for integrating more components on a single chip.



RISC chips - 35 million instructions per second.
If we want to increase the throughput rate we have to decrease the micron technology in terms of scaling and processing.

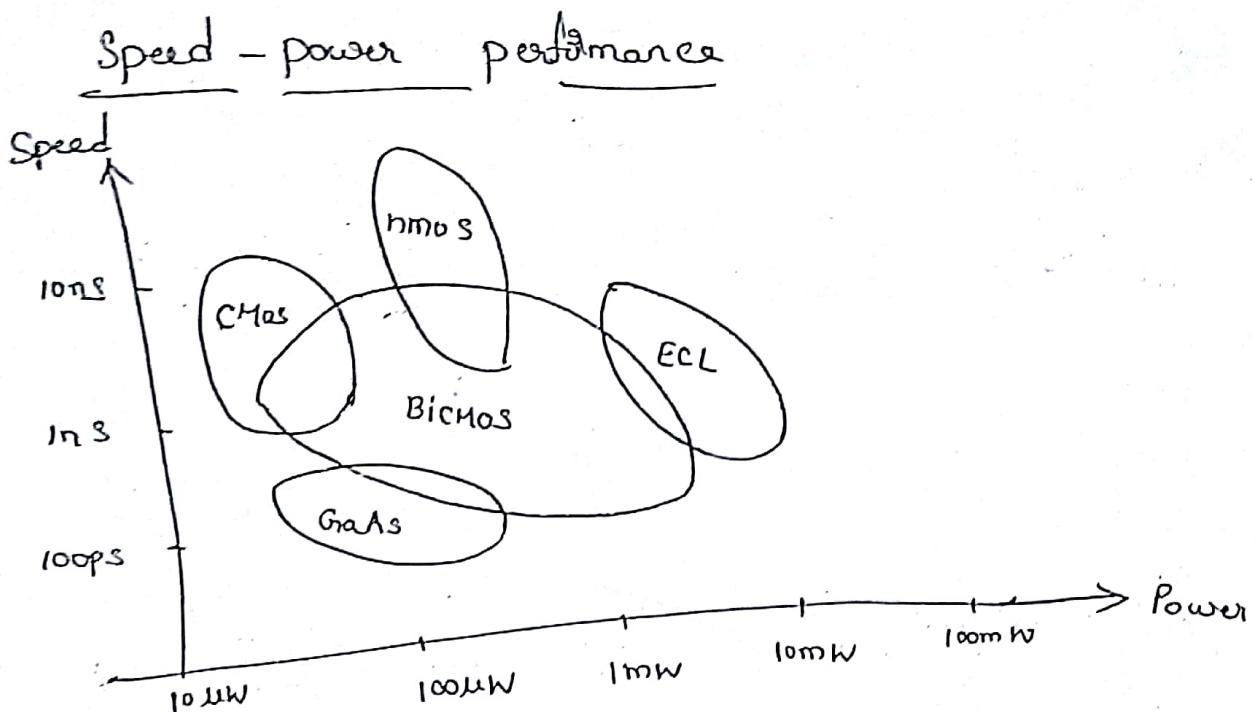
For all generations Si as substrate. Because upto 100 million instructions per second and could effectively do the tripling rate.

For ULSI \rightarrow GaAs used as substrate.

If we include GaAs and Si as substrate will provide the designer with some very exciting possibilities.

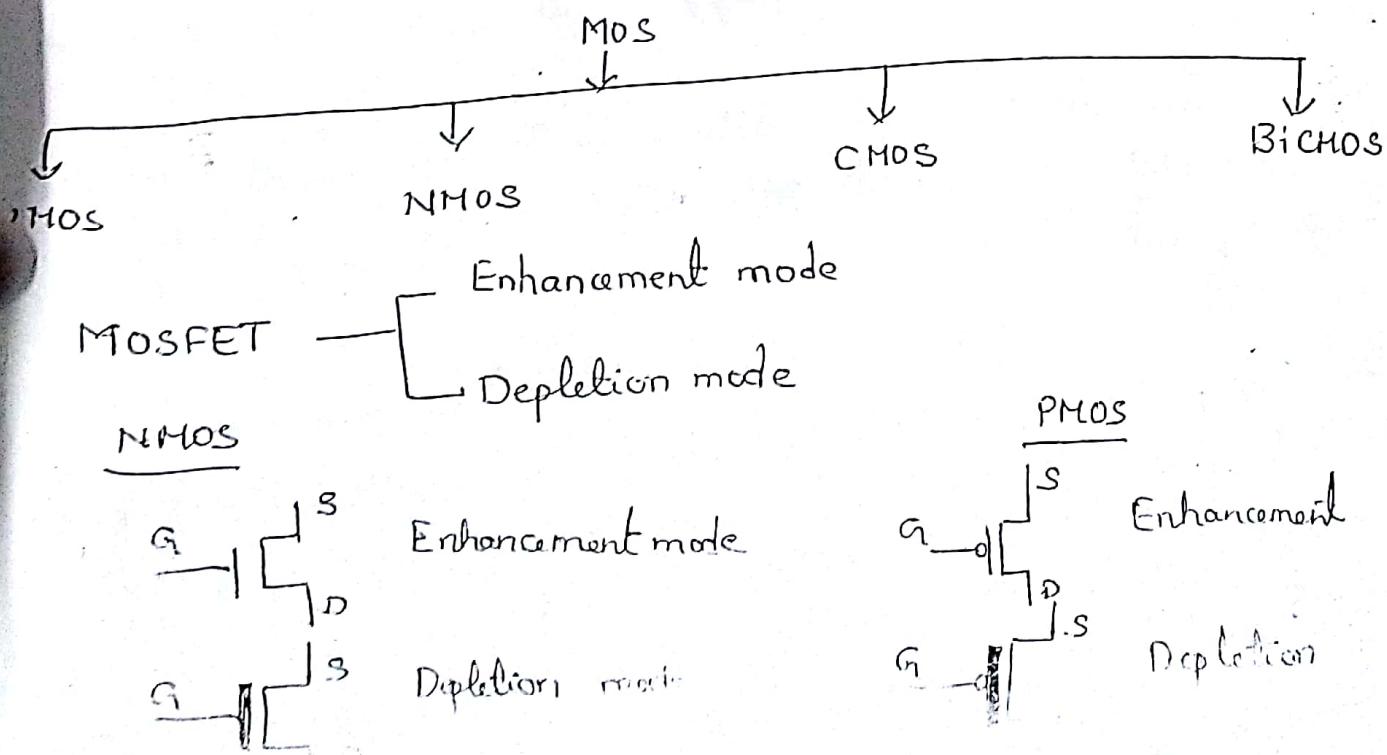
(6)

Different types of technologies are CMOS, GaAs, NMOS, BiCMOS, ECL

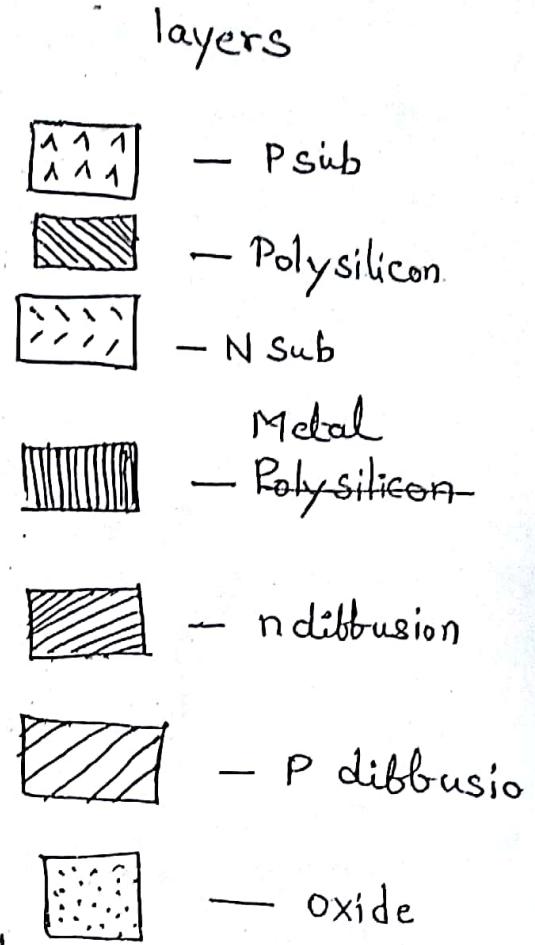
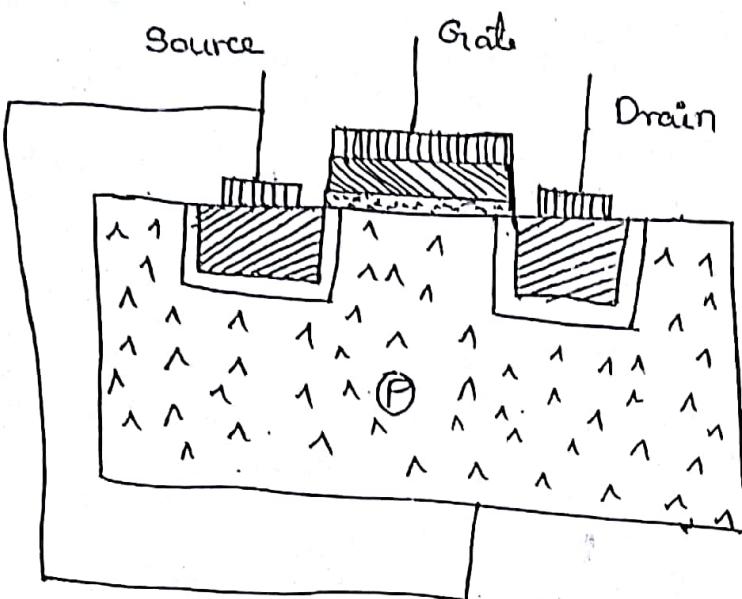


Moores Law :- The number of transistors are doubled in every year . (18 months)

NMOS transistor



NMOS - Enhancement mode



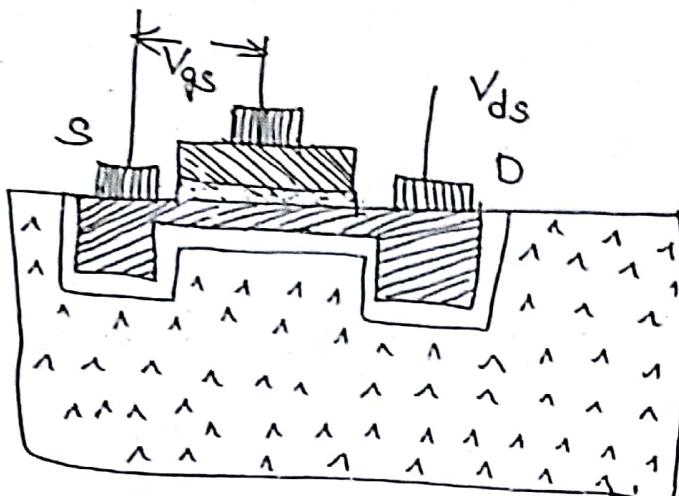
1) Consider rectangular silicon wafer.
for designing NMOS we will consider p type material as substrate.

- 2) Fill up the wafer with F-type Substrate. We know that MOSFET is having three terminal 1) Source 2) Drain
- 3) Gate.
- 4) For making Source and drain n-type impurities are diffused into P-type substrate. And to make the isolation between source and drain Oxide layer has been deposited on the substrate.
- 5) Now Source and Drain are formed. After that to make Gate polysilicon layer is deposited on the surface of Oxide layer. Now Gate has formed.

Now for

How it works

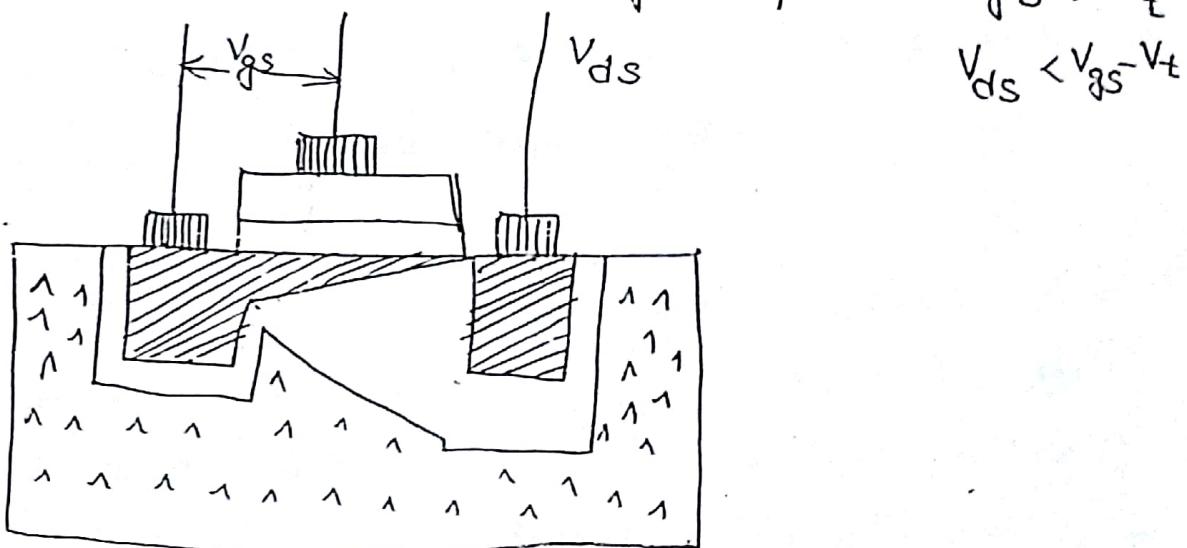
Initially no voltage has been given. In order to establish a channel a minimum voltage level or threshold voltage V_t has been given then channel has established between source and drain as shown in figure. But no current flow through channel ($V_{ds} = 0$)



$$V_{gs} = V_t$$

$$V_{ds} = 0$$

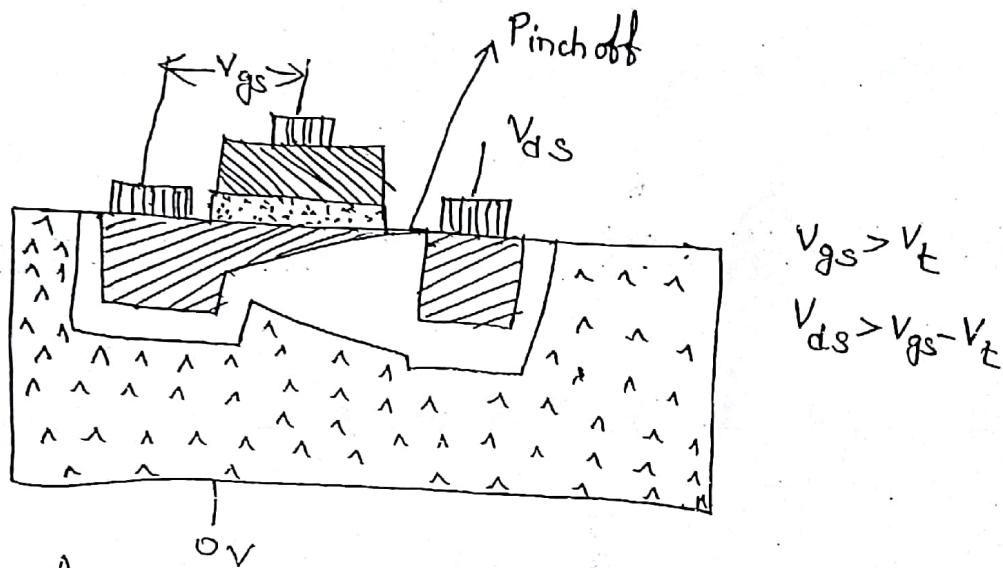
Now apply voltage V_{ds} between drain and source so current conduction takes place through channel from source to drain. And some voltage drop also $V_{gs} > V_t$



there along the channel when the positive gate voltage increases then channel will form and conduction will be there from source to drain. But every region will have their own voltage potential. So the drain

flow from source to drain.

- 8) Now, increase the drain Voltage $V_{ds} > V_{gs} - V_t$ then Voltage drop will be more under the gate insulation layer, so channel will diminish from source end to drain end. This condition we can call as Pinch-off. Even though current will flow from source to drain



The channel will act as constant current source. A, it shows high resistance.

Normally $V_t = 1V$, $V_{DD} = 5V$, $V_t = 0.2V_{DD}$.

All the cases current will flow except $V_{gs} < V_t$.

Basic Electrical properties of MOS and BiCMOS circuits

Drain to Source Current I_{ds} Versus Voltage V_{ds} relationship

- Voltage V_{gs} given to gate to induce a charge in the channel between source and drain.
- The charge induced is dependent on the gate to source voltage V_{gs} . So current I_{ds} is dependent on both V_{gs} and V_{ds} .

The amount of current flow from gate to source to drain is

$$I_{ds} = -I_{sd} = \frac{\text{charge induced in channel } (Q_c)}{\text{Electron transit time } (\tau_e)} \quad (1)$$

$$\therefore \text{Transit time } \tau_{sd} = \frac{\text{Length of channel } L}{\text{Velocity}} \quad (2) \quad \text{v}$$

$$\text{But Velocity } v = \mu E_{ds} \quad (3)$$

where μ = electron & hole mobility

E_{ds} = electric field (drain to source)

$$\text{Substitute (4) in (3)} \quad E_{ds} = \frac{V_{ds}}{L} \quad (4)$$

$$\text{So } v = \frac{\mu V_{ds}}{L} \quad (5)$$

Now Substitute (5) in (2)

$$\tau = \frac{L^2}{\mu v_{ds}} \quad (6)$$

Typical values of μ at room temperature

$$\mu_n = 650 \text{ cm}^2/\text{V sec}$$

$$\mu_p = 240 \text{ cm}^2/\text{V sec}$$

Charge induced in channel due to gate Voltage is due to the voltage difference b/w the gate and the channel V_g . The voltage along the channel varies linearly with distance x from the source due to IR drop in the channel. Assume that the device is not saturated then the average value is $\frac{V_{ds}}{2}$. And the effective gate voltage $V_g = V_{gs} - V_t$ where V_t is the threshold voltage needed to invert the channel charge under the gate and establish the channel.

$$\text{Charge per unit area} = E_g \epsilon_{ins} \epsilon_0$$

$$\text{Induced charge } Q_c = E_g \epsilon_{ins} \epsilon_0 \omega L$$

where E_g = average electric field gate to channel.
 ϵ_{ins} = relative permittivity of insulation b/w gate and channel.

$$\epsilon_0 = \text{Permittivity of free space}$$

$$\epsilon_0 = 8.85 \times 10^{-14} \text{ F cm}^{-1}$$

Now average electric field

$$E_g = (V_{gs} - V_t) - \frac{V_{ds}}{2}$$

where D = Oxide thickness

$$\text{Thus } Q_c = \frac{(V_{gs} - V_t) - \frac{V_{ds}}{2}}{D} \cdot \epsilon_{ins} \epsilon_0 L$$

$$= \frac{\epsilon_{ins} \epsilon_0 \omega L}{D} \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] - (7)$$

Substitute eq (6), (7) in equation (1)

$$I_{ds} = \frac{Q_c}{\tau} = \frac{\epsilon_{ins} \epsilon_0 \omega L \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right]}{\frac{L^2}{\mu V_{ds}}}$$

$$= \frac{\epsilon_{ins} \epsilon_0 \omega}{D L} \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] \mu V_{ds}$$

$$I_{ds} = \frac{\mu \epsilon_0 \epsilon_{ins}}{D} \frac{\omega}{L} \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] V_{ds}$$

$$K = \frac{\mu \epsilon_0 \epsilon_{ins}}{D}$$

$$= K \frac{\omega}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) - (8)$$

$$\beta = K \frac{\omega}{L}$$

$$\text{So } I_{ds} = \beta \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) - (9)$$

And we know that $C_g = \text{Channel Capacitance}$

$$C_g = \frac{\epsilon_{ins} \epsilon_0 \omega L}{D}$$

$$K = \frac{\epsilon_{ins} \epsilon_0 \omega}{D} \frac{L}{\mu} - (i)$$

$$= (ii)$$

Substitute (ii) in (i)

$$C_g = \frac{K}{\mu} (\omega L)$$

Now Substitute k in I_{ds} equation

$$I_{ds} = \frac{\mu C_g}{wL} \cdot \frac{w}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

$$= \frac{\mu C_g}{L^2} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

$$I_{ds} = \frac{\mu C_g}{L^2} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \quad -(10)$$

Sometimes it is convenient to use gate Capacitance per unit area C_0

$$C_g = C_0 w L$$

Substitute $C_g = C_0 w L$ in eq - (10)

$$I_{ds} = \frac{\mu C_0 w}{L^2} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

$$= \frac{\mu C_0 w}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \quad -(11)$$

In Saturation region

Saturation begins when $V_{ds} = V_{gs} - V_t$. Because at this point the IR drop in the channel equals the effective gate to channel voltage at the drain. And assume that the current remains fairly constant as V_{ds} increases further.

$$I_{ds} = k \frac{w}{L} (V_{gs} - V_t)^2$$

$$(a) I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2$$

(b)

$$I_{ds} = \frac{C_0 w}{L} (V_{gs} - V_t)^2 \quad (a) = \underline{C_0 w} \cdot \underline{\frac{w}{L}} (V_{gs} - V_t)^2$$

Mos transistor transconductance g_m and output Conductance g_{ds}

$$g_m = \left. \frac{\delta I_{ds}}{\delta V_{gs}} \right|_{V_{ds}=\text{const}}$$

we know that $I_{ds} = \frac{Q_c}{L}$

$$\delta I_{ds} = \frac{\delta Q_c}{\delta V_{ds}}$$

$$\text{Now } I_{ds} = \frac{L^2}{\mu V_{ds}}$$

$$\delta I_{ds} = \frac{\delta Q_c}{L^2} \mu V_{ds}$$

but we know $\delta Q_c = C_g \delta V_{gs}$

$$\delta I_{ds} = \frac{C_g \delta V_{gs} \mu V_{ds}}{L^2}$$

$$\Rightarrow \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{\mu C_g V_{ds}}{L^2}$$

In saturation $V_{ds} = V_{gs} - V_t$

$$g_m = \frac{\mu C_g}{L^2} (V_{gs} - V_t)$$

but $C_g = \frac{\omega L}{WL}$

$$\begin{aligned}
 f_m &= \frac{\mu \epsilon_0 \text{ Eins} \omega}{D L} (V_{gs} - V_t) \\
 &= \frac{\mu \epsilon_0 \text{ Eins}}{D} \cdot \frac{\omega}{L} (V_{gs} - V_t) \\
 &= K \cdot \frac{\omega}{L} (V_{gs} - V_t) \\
 &= \beta (V_{gs} - V_t)
 \end{aligned}$$

$f_{ds} \Rightarrow$

Mos transistor Figure of merit ω_0

Frequency response may be obtained from the parameter $\omega_0 = \frac{f_m}{C_g} = \frac{\mu}{L^2} (V_{gs} - V_t)$

$$\tau_{ds} = \frac{1}{\omega_0} = \frac{L^2}{\mu} (V_{ds}) = \frac{1}{T_{ds}}$$

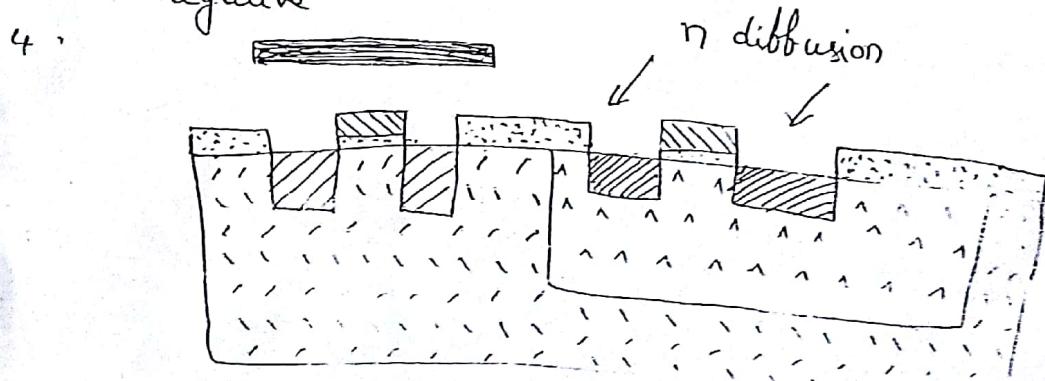
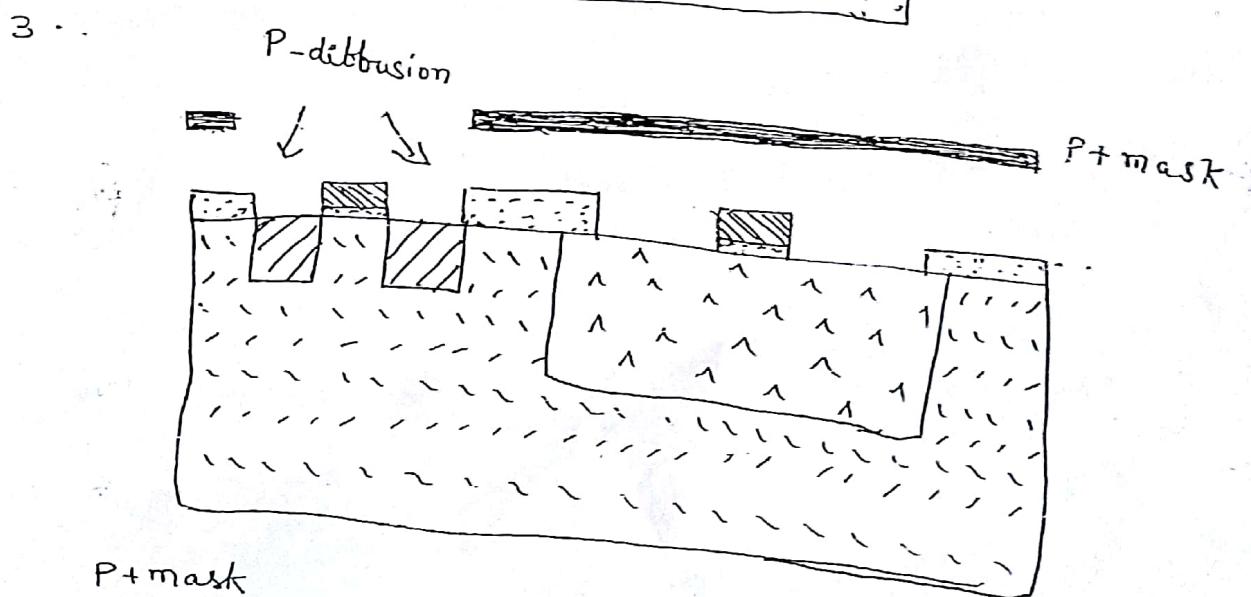
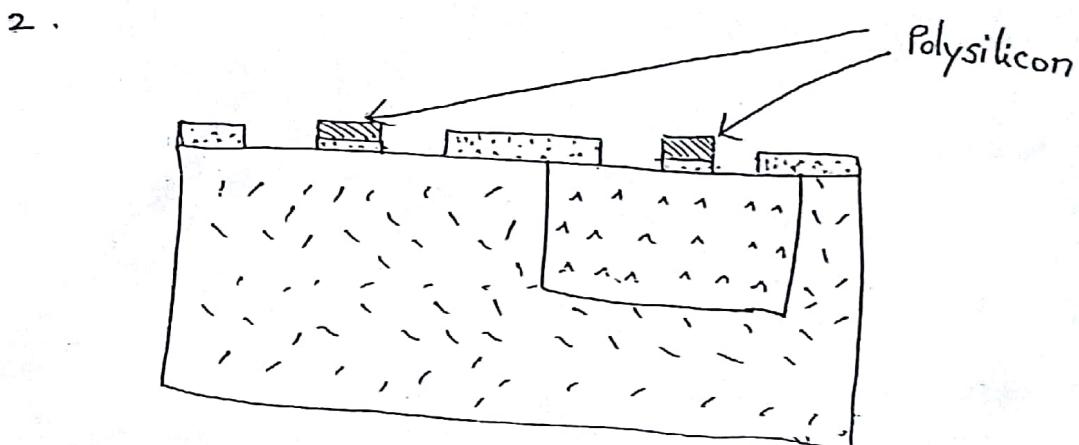
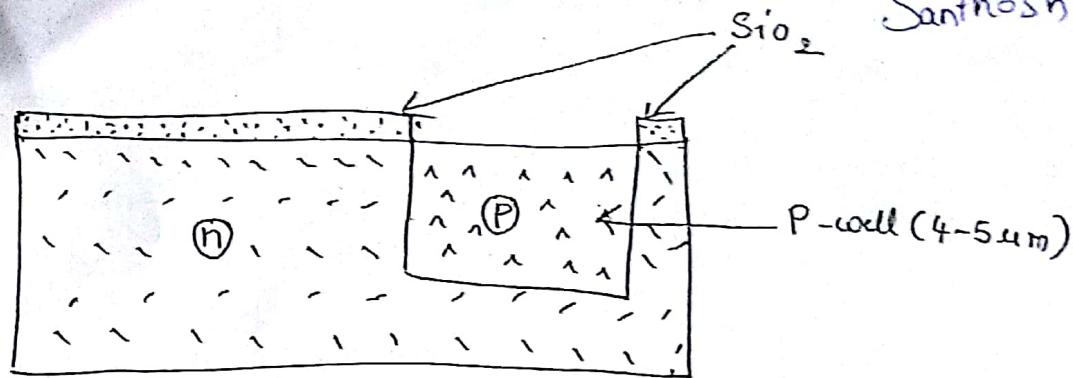
From the above equation switching speed depends on gate voltage above threshold and on carrier mobility and inversely as the square of channel length.

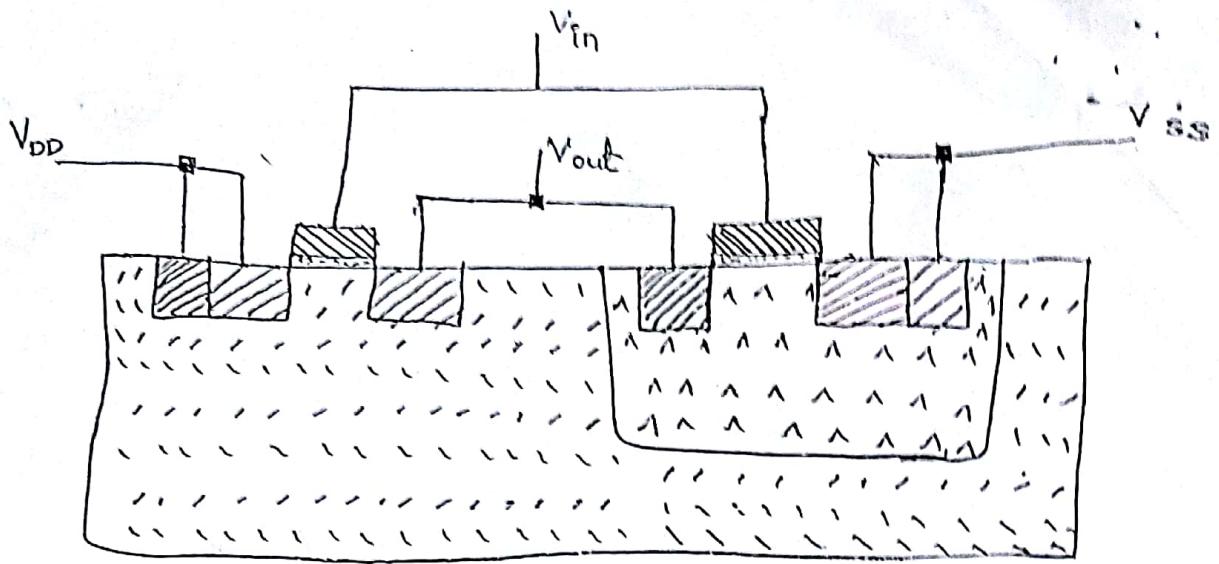
- Note: Normally electron mobility μ_n is larger than 3 times as hole mobility.

P-well Process

UNIT 1 Part ②

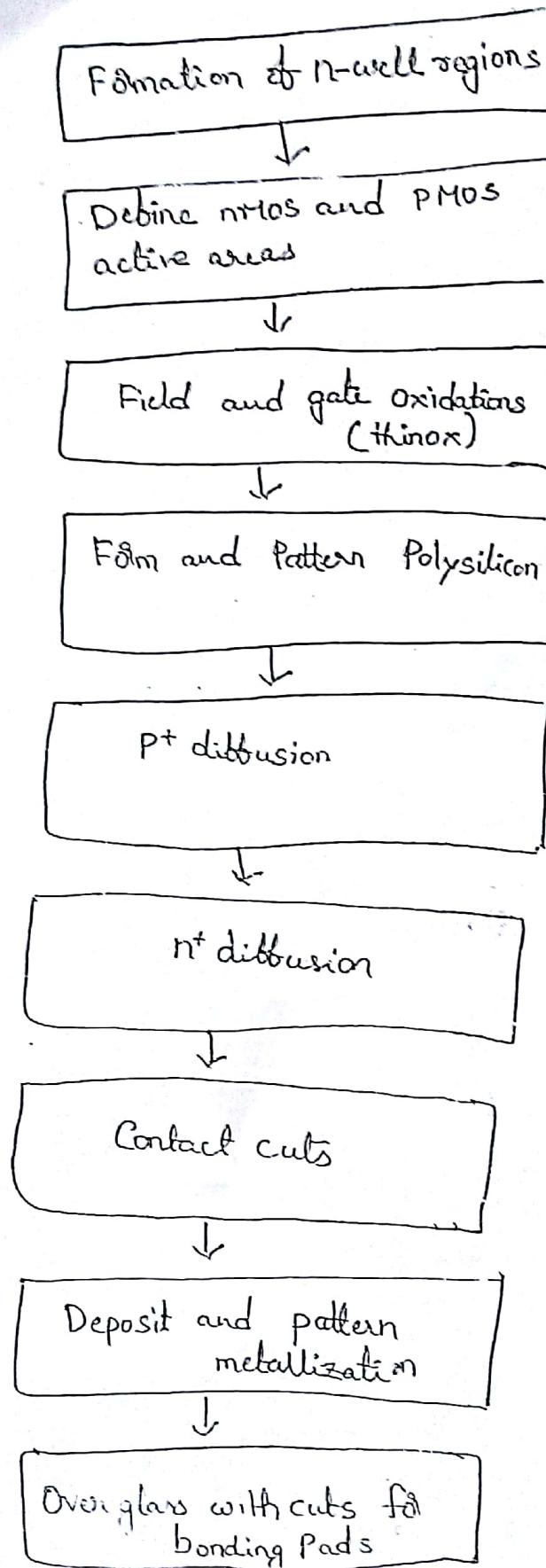
Santhosh Reddy



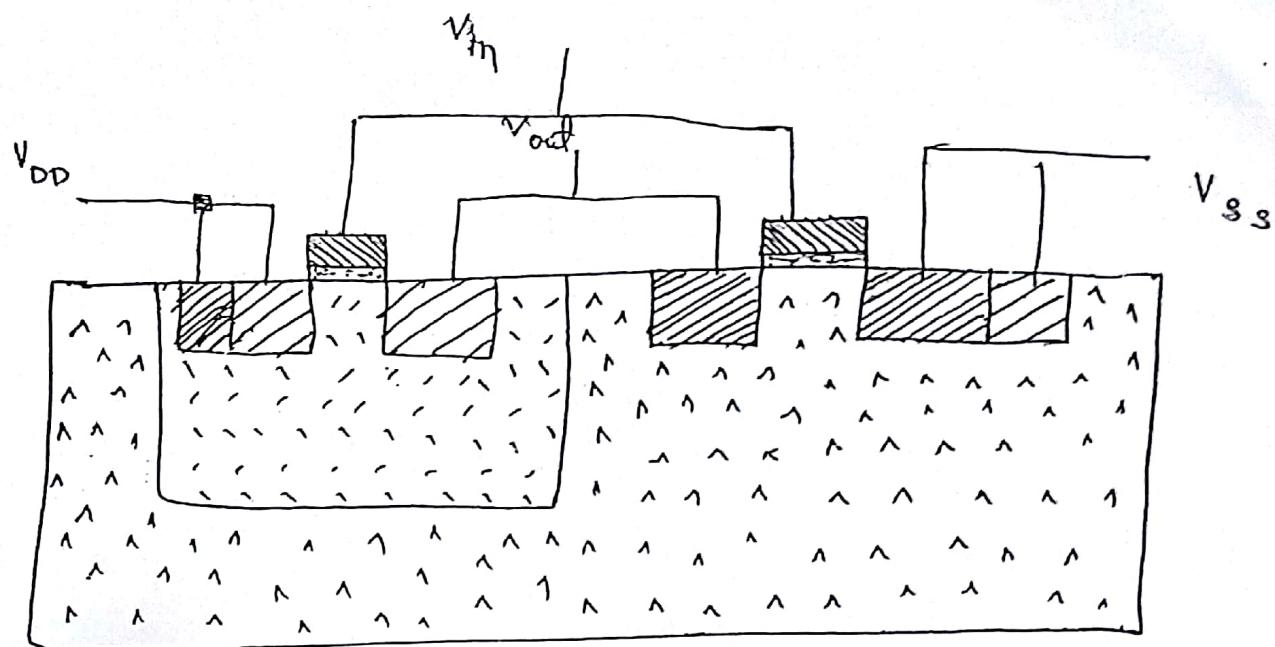


- 1) Define areas where P-well diffusions are to take place
- 2) Define the thin ox regions
- 3) Pattern the polysilicon layer which is deposited after the thin oxide.
- 4) P-plus mask is now used where P-diffusion is to take place.
- 5) P-Plus mask define those areas where n-type diffusion is to take place.
- 6) Contact cuts are not defined.
- 7) Metal layer pattern is defined.
- 8) Overglass passivation \rightarrow needed to define the openings for access to bonding pads.

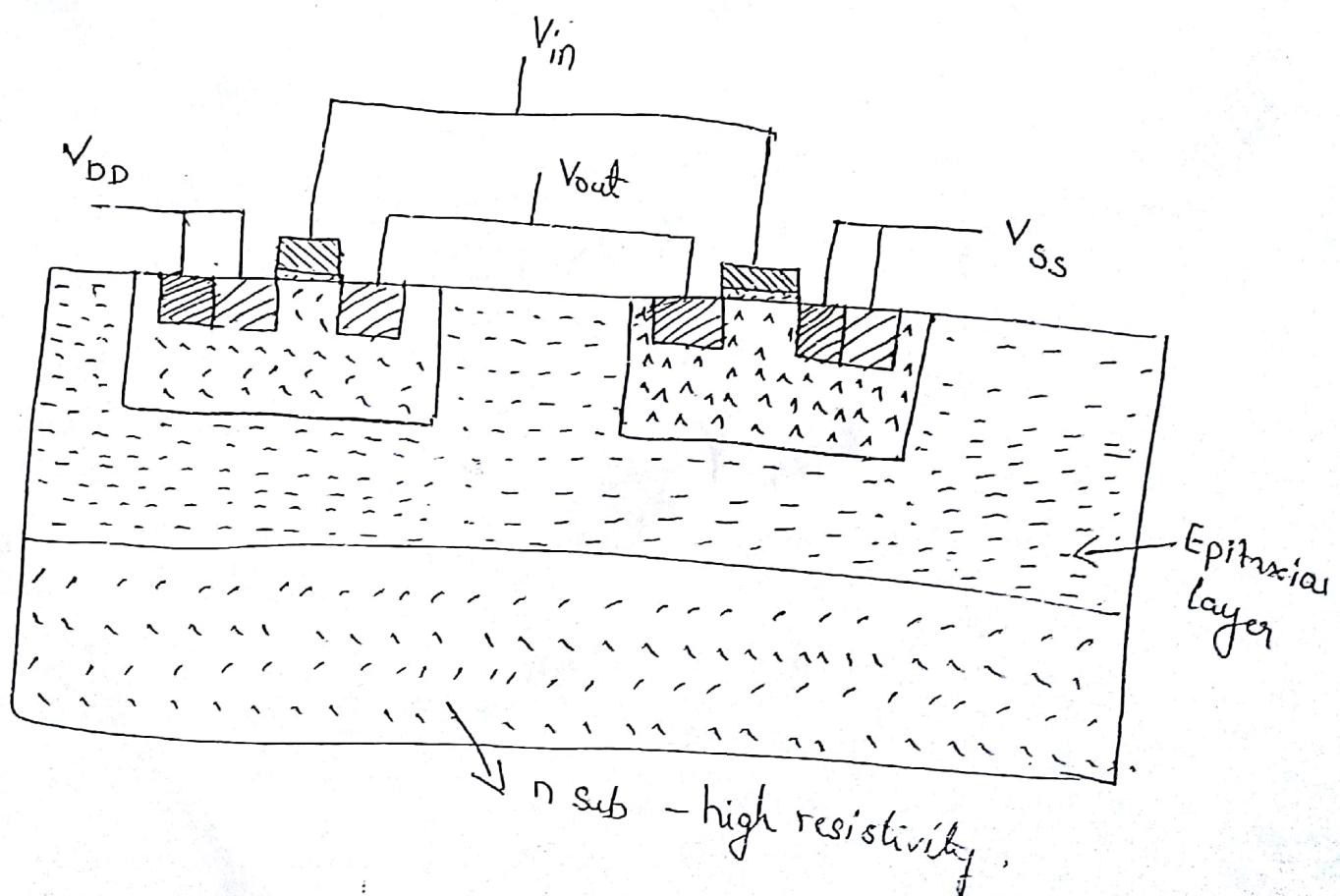
Nwell process



n-well CMOS Inverter



Twin-tub Process



i) A PMOS transistor is operated in the triode region with the following parameters

$$V_{GS} = -4.5V, V_{TP} = -1V, V_{DS} = -2.2V, \omega/L = 95,$$

$\mu_p C_{ox} = 95 \mu A/V^2$. Find its drain current and drain to source resistance.

$$V_{DS} < V_{GS} - V_T, \omega/L = 95, V_{GS} = -4.5V, \mu_p C_{ox} = 95 \mu$$

$$V_{TP} = -1V, V_{DS} = -2.2V$$

$$I_{DS} = \mu_p C_{ox} \frac{W}{L} \left((V_{GS} - V_{TP}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$= 95 \times 10^{-6} \times 95 \left[(-4.5 + 1)(-2.2) - \frac{(-2.2)^2}{2} \right]$$

$$I_{DS} = 47.65 \text{ mA}$$

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{-2.2}{47.65 \text{ mA}} = \frac{2.2}{47.65 \times 10^{-3}}$$

$$= 46.16 \Omega$$

2) Find g_m and r_{DS} for an n-channel transist with $V_{GS} = 1.2V$, $V_{TN} = 0.8V$, $\omega/L = 10$, $\mu_n C_{ox} = 92 \mu A/V^2$ and $V_{DS} = V_{DD} + 0.5V$. The output impedance constant $= 95.3 \times 10^{-3} V^{-1}$

$$V_{GS} = 1.2V$$

$$V_{DS} = V_{eff} + 0.5$$

$$V_{Th} = 0.8V$$

$$V_{eff} = V_{GS} - V_{Th}$$

$$W/L = 10$$

$$= 1.2 - 0.8 = 0.4$$

$$\mu_n C_{ox} = 92 \text{ mA/V}^2$$

$$\text{O/P impedance } \lambda = 95.3 \times 10^{-3} \text{ V}^{-1} \quad \therefore V_{DS} = 0.4 + 0.5 = 0.9$$

$$V_{DS} > V_{GS} - V_{Th}$$

$$g_m = \frac{C_{mu}}{L^2} V_{DS} = \frac{\mu C_{ox} \omega L}{L^2} V_{DS}$$
$$= \mu_n C_{ox} \frac{\omega}{L} V_{DS} = 92 \times 10^{-6} \times 10 \times 0..$$

$$r_{DS} = \frac{1}{\lambda I_{DS}} = 82.8 \text{ m}\Omega$$

$$I_{DS} = \frac{\mu n C_{ox}}{2} \frac{\omega}{L} (V_{GS} - V_{Th})^2$$

$$= \frac{92 \times 10^{-6}}{2} (10) (0.4)^2$$

$$= 7.36 \times 10^{-5} \text{ A}$$

$$r_{DS} = \frac{1}{\lambda I_{DS}} = \frac{1}{95.3 \times 10^{-3} \times 7.36}$$

$$= 142.57 \text{ k}\Omega$$

3) An nmos transistor is operated in the triode region with the following parameters $V_{gs} = 4V$, $V_{tn} = 1V$, $V_{ds} = 2V$, $w/L = 100$, $\mu_nC_{ox} = -90 \mu A/V^2$. Find its drain current and drain to source resistance.

It is given that nmos transistor is operating in the triode region i.e $V_{ds} < V_{gs} - V_t$

$$V_{gs} = 4V$$

$$w/L = 100$$

$$V_{tn} = 1V$$

$$V_{ds} = 2V$$

$$\mu_nC_{ox} = -90 \mu A/V^2$$

$$\begin{aligned} I_{ds} &= \mu_nC_{ox} \frac{w}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \\ &= 90 \times 10^{-6} \times 100 \left[(3)(2) - \frac{2^2}{2} \right] \\ &= 36 \text{ mA} \end{aligned}$$

$$R_{ds} = \frac{V_{ds}}{I_{ds}} = \frac{2V}{36 \times 10^{-3}} = 55.56 \Omega$$

4) NMOS transistor is operated in the active region with the following parameters $V_{gs} = 3.9V$, $V_{tn} = 1V$, $w/L = 100$, $\mu_nC_{ox} = 90 \mu A/V^2$

NMOS transistor is operating in active region

$$V_{tn} = 1V, \mu_n C_{ox} = 90 \mu A/V^2$$

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{\omega}{L} (V_{gs} - V_{tn})^2$$

$$= \frac{90}{2} \times 100 (3.9 - 1)^2 \times 10^{-6} = 37.8 \text{ mA}$$

$$R_{ds} = \frac{V_{ds}}{I_d} = \frac{V_{gs} - V_t}{I_d} = \frac{3.9 - 1}{37.8 \times 10^{-3}} = 76.71 \Omega$$

5) An nmos transistor is operating in the Saturation region with the following parameters.

$$V_{gs} = 5V \quad \omega/L = 110$$

$$V_{tn} = 1.2V \quad \mu_n C_{ox} = 110 \mu A/V^2$$

$$g_m = \frac{g \mu_n (V_{ds})}{L^2}$$

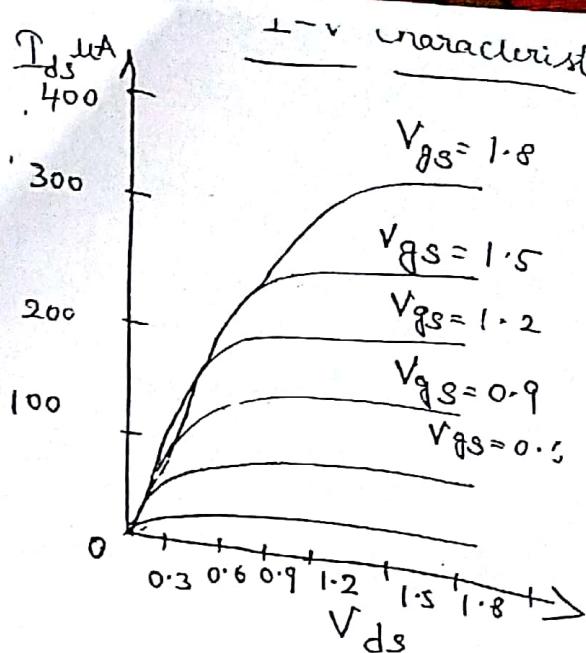
$$\text{So } V_{ds} = V_{gs} - V_{tn}, \quad C_g = C_{ox} \omega L$$

$$= \frac{C_{ox} \omega \mu_n}{L^2} (V_{gs} - V_{tn})$$

$$= \mu_n C_{ox} \frac{\omega}{L} (V_{gs} - V_{tn})$$

$$= 110 \times 10^{-6} \times 110 (5 - 1.2)$$

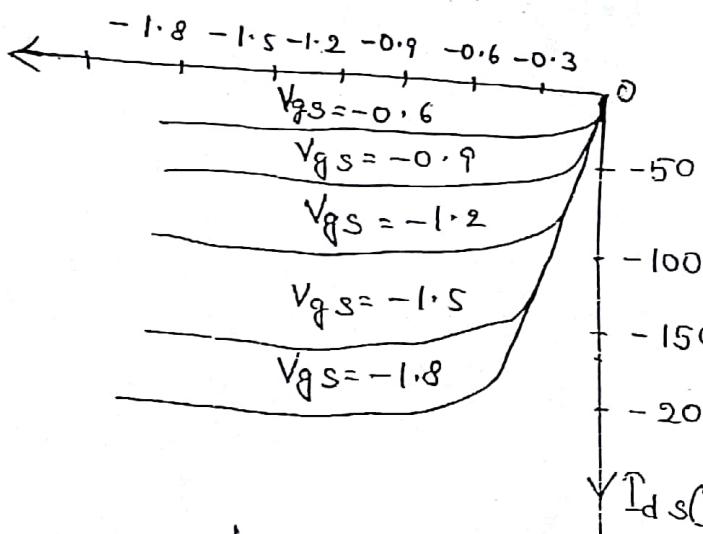
$$= 4.578 \text{ nA}$$



I-V characteristics for NMOS

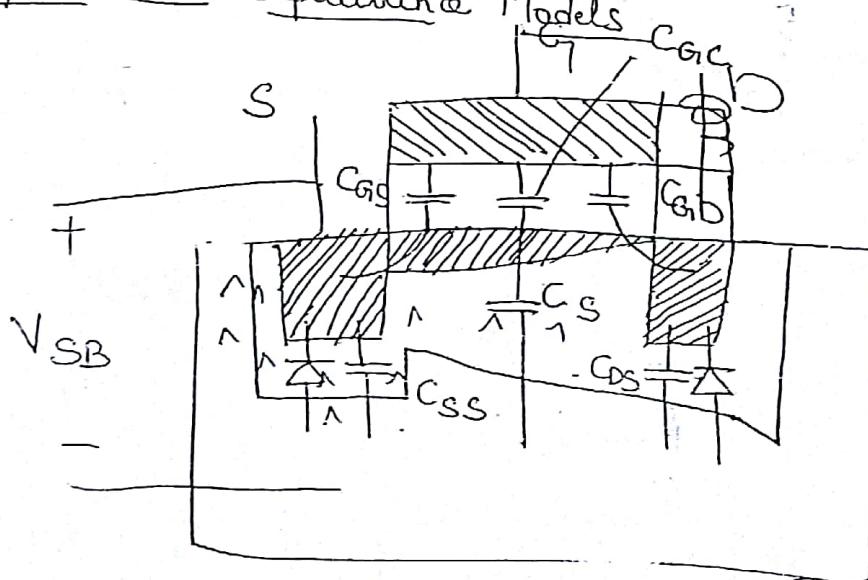
- 1) The current is zero below threshold Voltage V_t .
- 2) For higher gate Voltages Current increases linearly with V_{ds} .
- 3) As V_{ds} reaches the saturation Point $V_{gs}-V_t$ current rolls off eventually becomes independent of V_{ds} when the transistor is saturated.

PMOS



- 1) PMOS transistor behave in the same way but with the signs reversed.
- 2) The I-V characteristics are in the third quadrant.

Simple MOS Capacitance Models



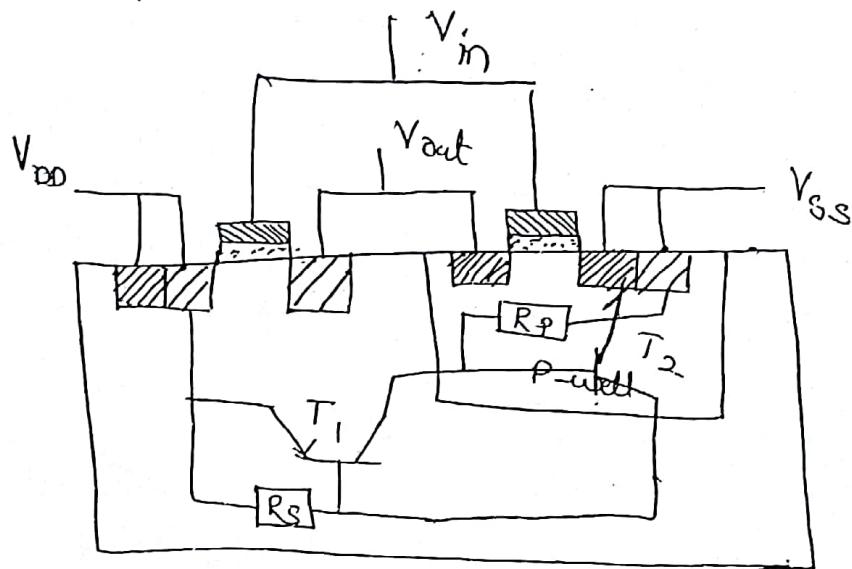
C_{GC} = gate to channel cap

C_{GS} = gate to source capacitance

C_{GD} = gate to drain capacitance.

Latch up

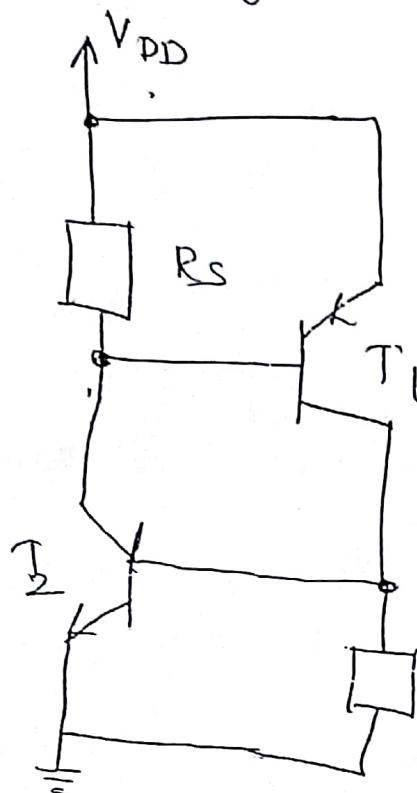
P-well



- 1) Latch up occurs because of Large number of Junctions.
- 2) Latch up is a Condition in which the parasitic Components give rise to the establishment of low resistance conducting paths between V_{DD} and V_{SS} because of formation of transistors and diodes.
- 3) Latches may be induced by glitches on the supply rails.
- 4) Here, in the above circuit the transistors

between V_{DD} and V_{SS} .

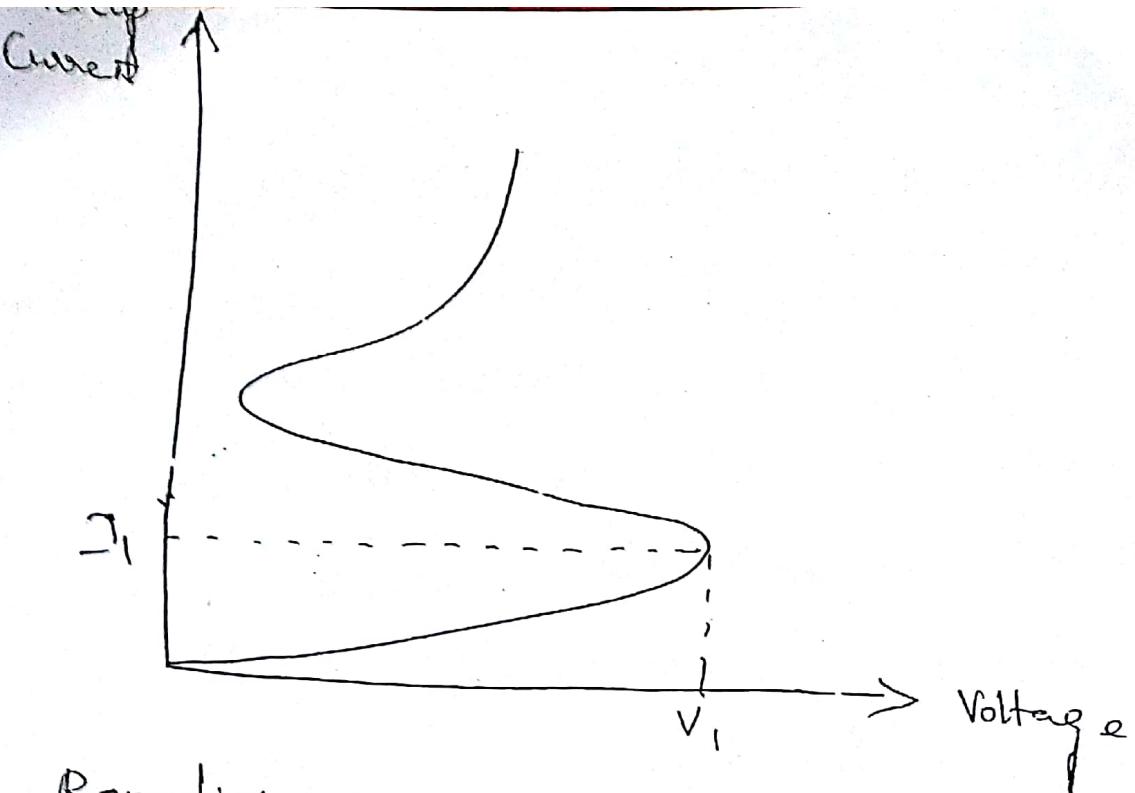
- 5) If sufficient substrate current flows to generate enough voltage across R_s to turn on transistor T_1 , this will draw current through R_p and in p-well also if the voltage across R_p sufficient T_2 will also turn on.
- 6) It establishes a low resistance path between the supply rails.



Latch up circuit model.

7) with no injected carrier the parasitic transistors exhibit high resistance.

8) Once it is latched up, this condition will be maintained until the latch up current drops below I_1 .



Remedies

- 1) Increase substrate doping levels with a consequent drop in the value of R_s .
- 2) Reduce R_p by control of fabrication parameters.
- 3) Introduction of guard rings on V_{dd} and V_{ss} .

Aspects of MOS Transistor threshold Voltage V_t

The gate structure of a MOS transistor consists electrical off charges stored in the dielectric layers and at the surface to surface interfaces as well as in the substrate itself.

For enhancement mode MOS transistor we need to give positive voltage to make the transistor ON.

For depletion mode MOS transistor (-ve) Voltage to neutralize the charge stored.

Switching an enhancement mode MOS transistor from the OFF to the ON state consists in applying sufficient gate voltage to neutralize these charges and enable the underlying silicon to undergo an inversion due to the electric field from the gate.

Switching a depletion mode nMOS transistor from ON to the off state consists in applying enough Voltage to the gate to add to the stored charge and invert the n-implant region to 'p'.

The threshold Voltage V_t may be expressed as

$$V_t = Q_{ms} \frac{Q_s - Q_{ss}}{C_o} + 2Q_{fn}$$

Threshold voltage

$$V_t = \phi_{ms} - \frac{Q_B - Q_{ss}}{C_0} + 2\phi_{FN}$$

Q_B = charge / unit area in depletion layer
beneath the contact.

Q_{ss} = charge density at Si: SiO₂ interface

C_0 = capacitance per unit gate area.

ϕ_{ms} = work function diff. b/w gate Si

ϕ_{FN} = Fermi level potential b/w channel & bulk

$$\Rightarrow Q_B = \sqrt{2\epsilon_0 \epsilon_s q N_i (2\phi_{FN} + V_{SB})} \quad C/cm^2$$

$$\phi_{FN} = \frac{kT}{q} \ln \frac{N}{n_i} \text{ volt.}$$

$$Q_{ss} = (1.5 \times 10^{-8}) \times 10^{-8} \text{ C/m}^2.$$

$$V_{SB} =$$

$$q = 1.6 \times 10^{-19}$$

N = impurity constant N_A or N_D .

$$\epsilon_s = 11.7$$

n_i = intrinsic e⁻ constant $1.6 \times 10^{10} / \text{cm}^3$ at 300K

$$k = \text{Boltzmann} \quad 1.4 \times 10^{-23} \text{ J/K.}$$

Body effect

$$V_t = V_t(0) + \left[\frac{D}{\epsilon_m \epsilon_0} \right] \sqrt{2 \epsilon_0 \epsilon_s Q_N (V_{SB})^{1/2}}$$

$$= V_t(0) + \gamma (V_{SB})^{1/2}$$

$$\gamma = \sqrt{\frac{2 \epsilon_s F}{C_0}}$$

$$\gamma = \sqrt{\frac{2 \epsilon_s F}{C_0}}$$

h_{my} (e)

$$V_{SB} = 0$$

$$V_t = 0.2 V_{DD}$$

$$V_{SB} = 5V$$

$$V_t = 0.3 V_{DD}$$

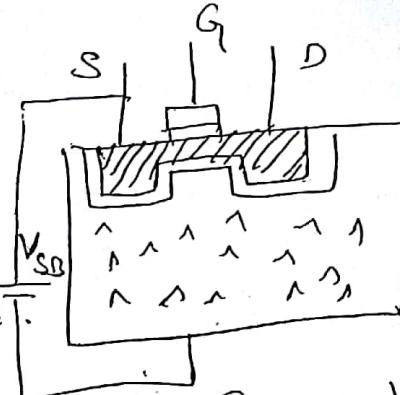
h_{my} D

$$V_{SB} = 0$$

$$V_{tD} = -0.7 V_{DD}$$

$$V_{SB} = 5$$

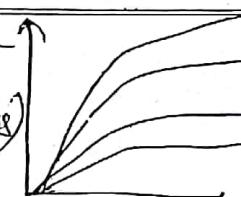
$$V_{tD} = -0.6 V_{DD}$$



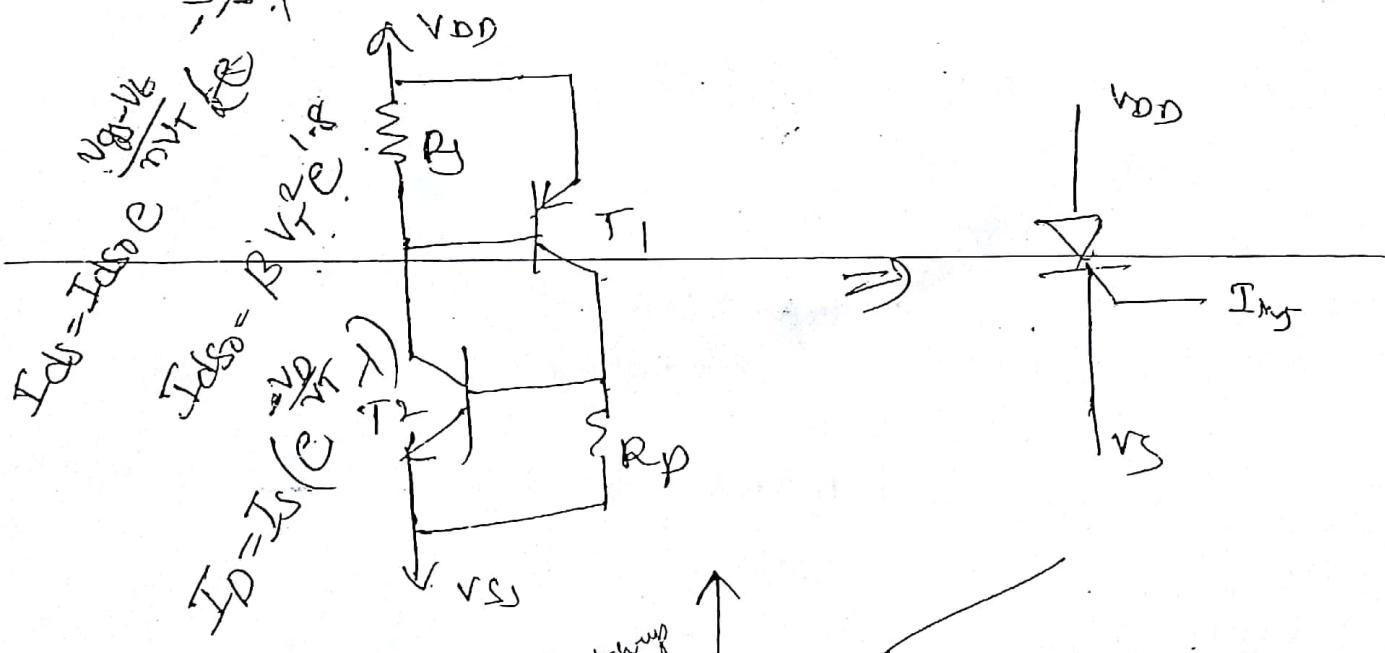
Increase V_{SB} cause
channel to be depleted
more and threshold V_t
raises.

Channel length modulation

$$I_{DS} = \frac{B}{2} (V_{GS} - V_t)^2 \cdot (1 + \gamma V_{DS})$$



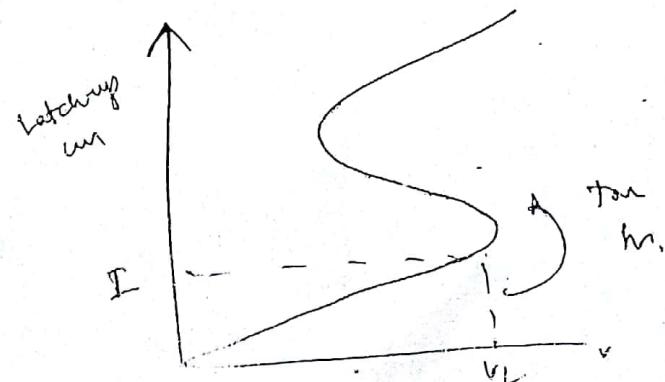
Latch-up



R_p → Sub-doping

R_p , R_s - fab. param

good rings



* Subthreshold Conduction :-

- The ideal transistor model assumes current only flows from source to drain when $V_{GS} > V_T$.
- In real transistors, some current will flow even below threshold voltage.
- The current does not abruptly cut off below threshold voltage, but rather drops off exponentially.
- This conduction is also known as leakage. It is undesirable.
- The subthreshold conduction or leakage current is denoted by

$$I_{DS} = I_{DS0} e^{\frac{V_{GS}-V_T}{nV_T}} \left(1 - e^{-\frac{V_D}{V_T}} \right)^{10PA}$$

where,

$$I_{DS0} = \beta V_T^{1.8} e^{1.8} = \text{at the current at threshold.}$$

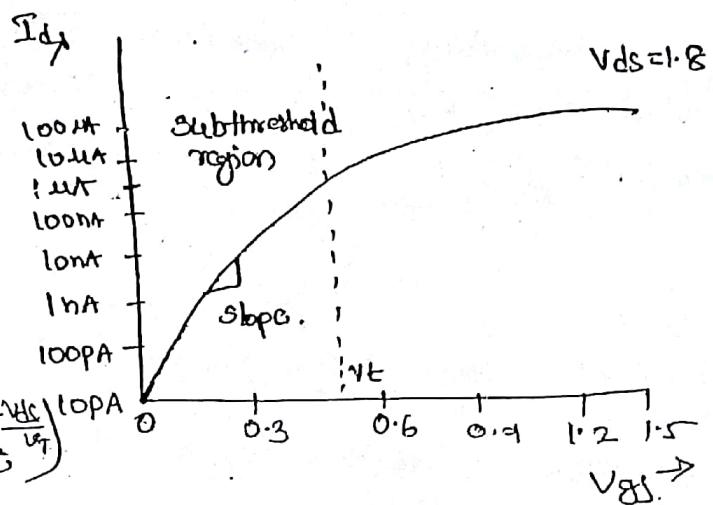
where $\beta^{1.8}$ = device geometry value.

n = is process dependent term, range (1.4-1.5) for CMOS.

V_T = Thermal voltage.

* Junction Leakage :-

- In the construction of MOS devices, many P-N junctions are formed. For example, P-N diodes between diffusion and substrate, diffusions between wells and P-N junction b/w well and substrate. All these diodes should be reverse biased. Practically, reverse bias diodes still conduct a small amount of current I_J called junction leakage.



$$\therefore I_D = I_S \left(e^{\frac{V_D}{V_T}} - 1 \right)$$

I_D = diode current

I_S = reverse saturation current

V_D = diode voltage [ex: $-V_{SB}$ or V_{DB}]

V_T = thermal voltage.

Tunneling:-

According to quantum mechanics, there is some probability that carriers will tunnel through the gate oxide.

This results in gate leakage current flowing into the gate.

Channel Length Modulation:-

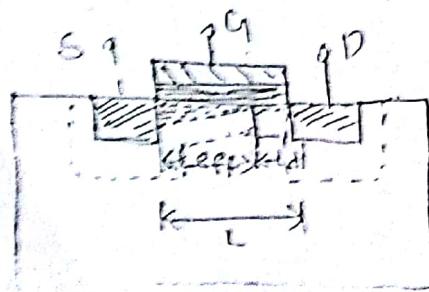
In the saturation region, the current I_D is independent of V_{DS} , this makes transistor a perfect current source.

The depletion region at drain side with a width L_d increases with reverse biased voltage. This depletion region effectively shortens the channel length to

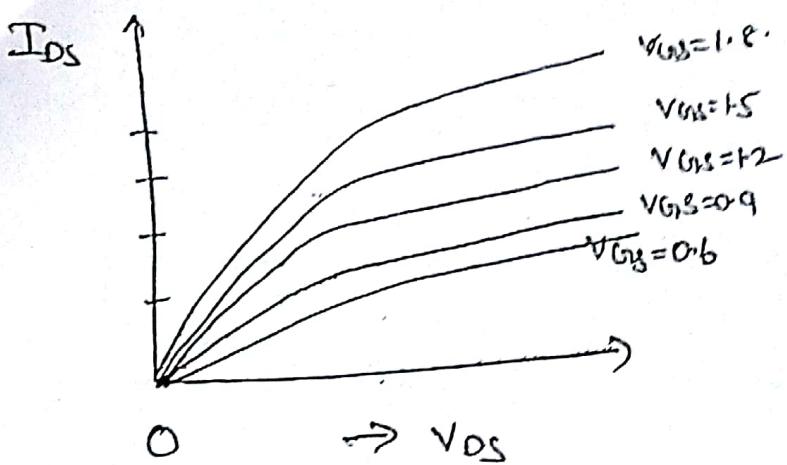
$$L_{eff} = L - L_d$$

↓ ↓ →

actual length of channel. length of depletion region.



⇒ The shorter channel length results in higher I_D current and it also increases with V_{DS} in saturation region.



Now, the I_{DS} in saturation region is given by:

$$I_{DS} = \frac{B}{2} (V_{GS} - V_t)^2 \cdot (1 + \lambda V_{DS})$$

where, λ is channel length modulation factor.

- As channel length gets shorter, the effect of channel length modulation becomes more significant.

Comparison between CMOS and Bipolar technologies

CMOS technology

- Low static power dissipation
- High input impedance
(low drive current)
- Scalable threshold voltage
- High noise margin
- High packing density
- High delay sensitivity to load
- Low output drive current
- Low g_m
- Bidirectional capability
- Ideal switching device

Bipolar technology

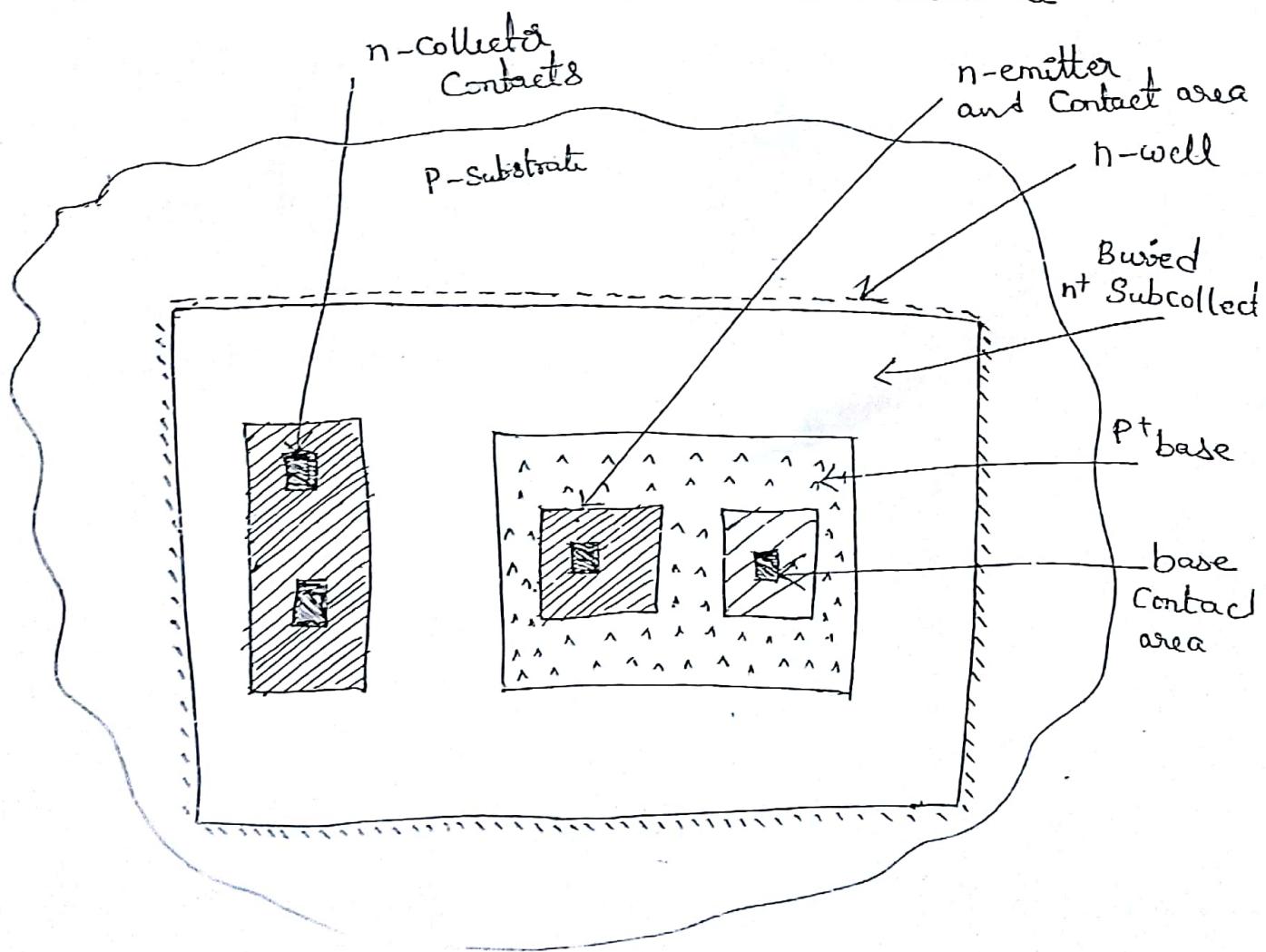
- High power dissipation
- Low input impedance
(high drive current)
- Fixed threshold voltage
- Low voltage swing logic
- Low packing density
- Low delay sensitivity to load
- High output drive current
- High g_m
- Essentially unidirectional

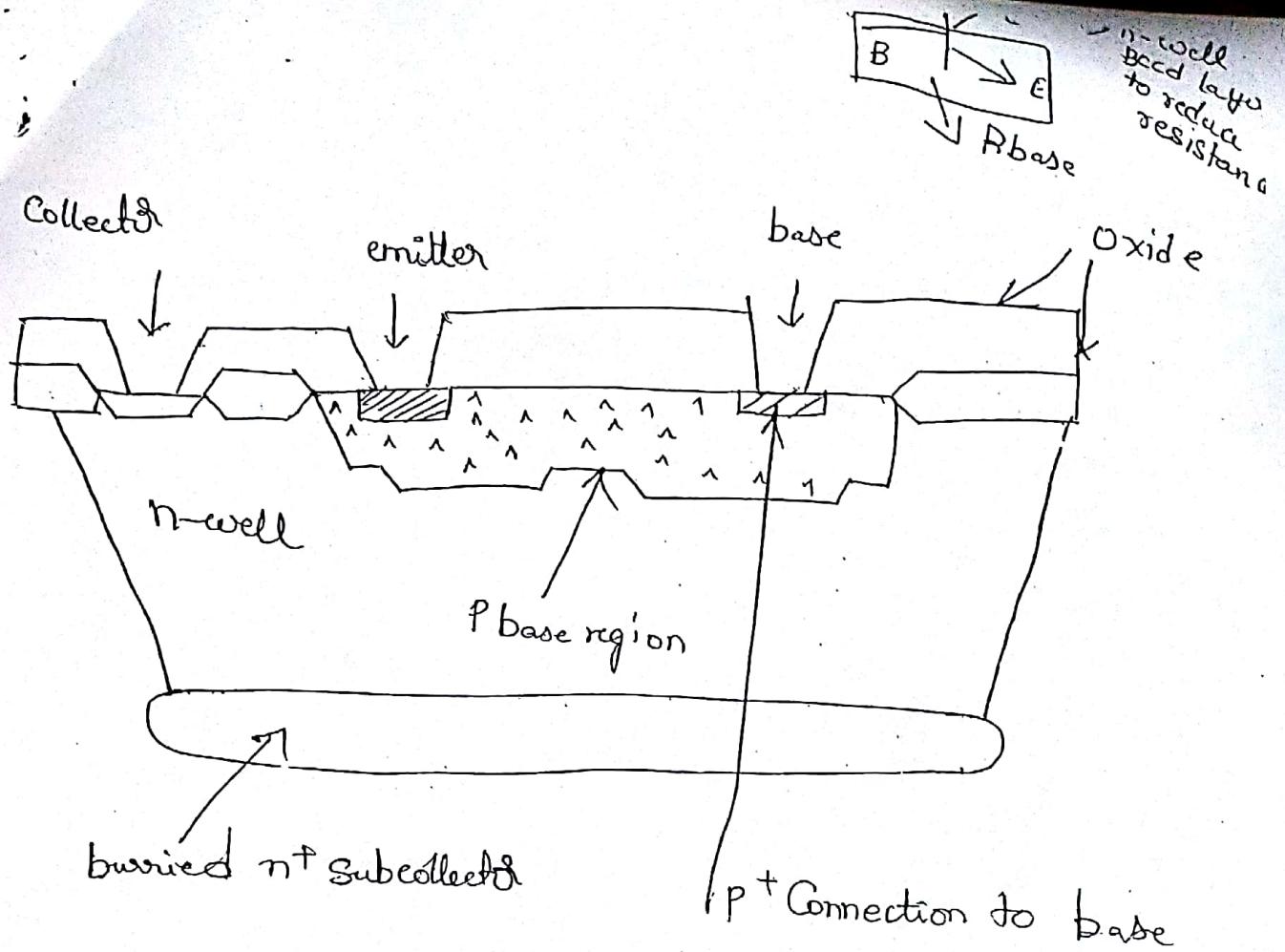
BICMOS fabrication process

One disadvantage of p-well and n-well CMOS processing that parasitic bipolar transistors are formed.

- Add additional layers - n^+ subcollector and p^+ base layer
- npn transistor is formed in an n-well and the additional p^+ base region is located in the well to form the p-base region of the transistor

Second additional layer, the buried n^+ subcollector (BCCD) is added to reduce the n-well resistance.





MOS transistor figure of Merit ω_0

$$\omega_0 = \frac{g_m}{C_g} = \frac{\mu}{L^2} (V_{gs} - V_t) = \frac{1}{T_{sd}}$$

This shows that switching speed depends on gate Voltage above threshold and on carrier mobility and inversely as the square of channel length.