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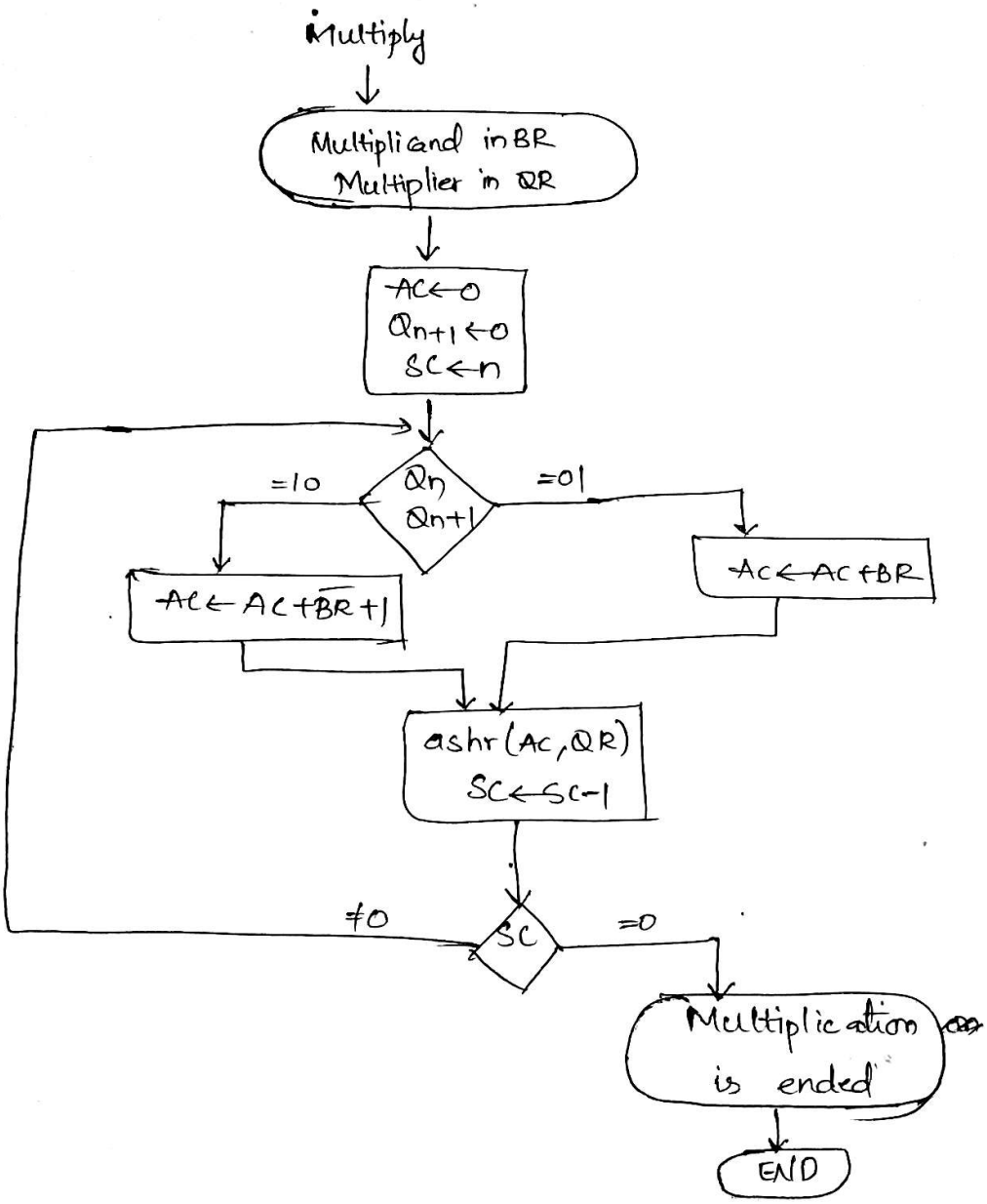
ECE-C
15B81A04D8

CAO ASSIGNMENT

1. **Booth Algorithm with an Example:**

Algorithm used for Multiplying Signed 2's Complement numbers, it is called Booth Multiplication Algorithm.



BR → Multiplicand in Signed 2's Complement

QR → Multiplier in Signed 2's Complement

BR & QR includes Sign bits. Result in AC & QR.

Example: $(-9) \times (-13)$

Multiplicand → −9

BR = 2's complement of −9

BR = 10111

$\overline{BR}+1 = 01001$

Multiplier → −13

QR = 2's Complement

QR = 10011

SC = n (no. of bits in Mu

SC = 101 = 5.

Qn Qn+1		AC	QR	Qn+1	SC
	Initial	00000	10011	0	101
10	Subtract BR ashr (AC, QR)	00000 01001 01001 00100	11001	1	100
11	ashr(AC,QR)	00010	01100	1	011
01	add(AC+BR)	10111 00010 11001			
	ashr(AC,QR)	11100	10110	0	010
00	ashr(AC,QR)	11110	01011	0	001
10	AC+$\overline{BR}$+1	01001 11110 1 00111 Discard			
	ashr	00011	10101	1	000.

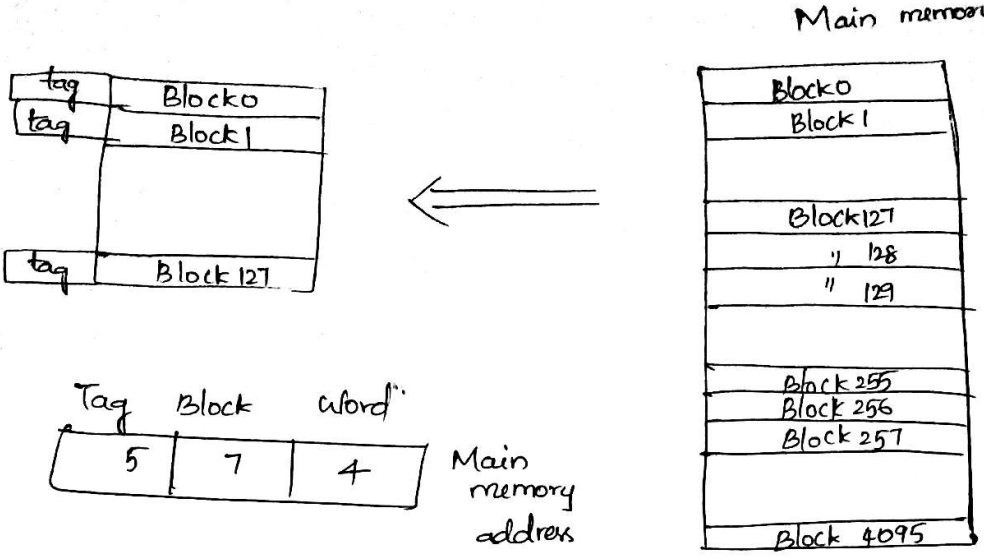
Result → AC, QR

$\Rightarrow 0001110101 \Rightarrow (117)_{10}$.

$\Rightarrow (-9) \times (-13) = +117$

...ous Mapping Techniques in Cache Memories.

...ect Mapping:



Here, each block contains 16 words.

Total no. of words = 4096 × 16 = 2^{16} locations = 64k locations

16 address bits are required to access 64k locations.

Cache contains 128 blocks

∴ No. of words = 128 × 16 = 2048 words = 2k words

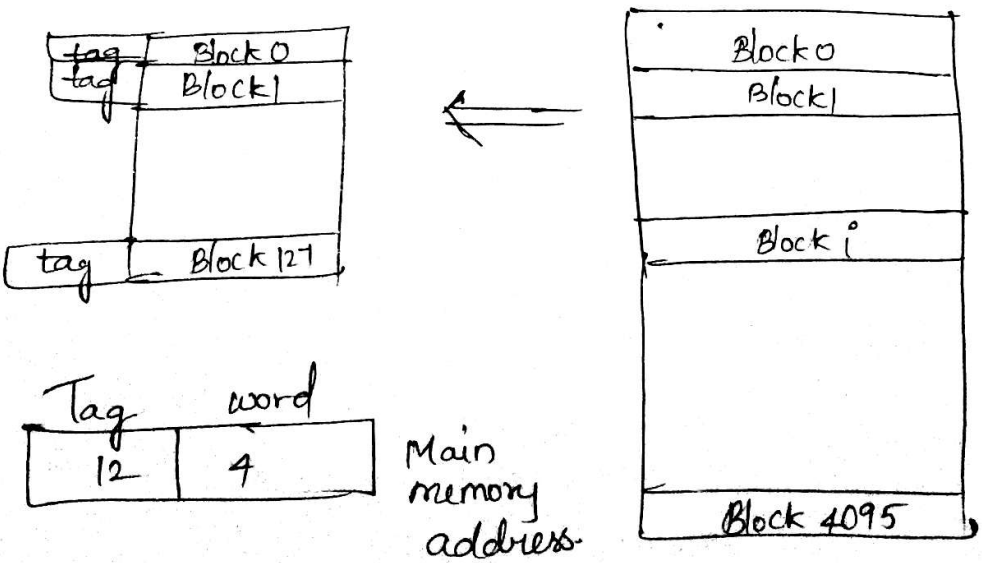
Block 0 of main memory is placed in block 1 of Cache.

Block 1 " " " " " " 2 " "

Block " 127 " " " " " " 128 " "

Block j of main memory is placed in block (j % 128) of Cache.

Associative Mapping:



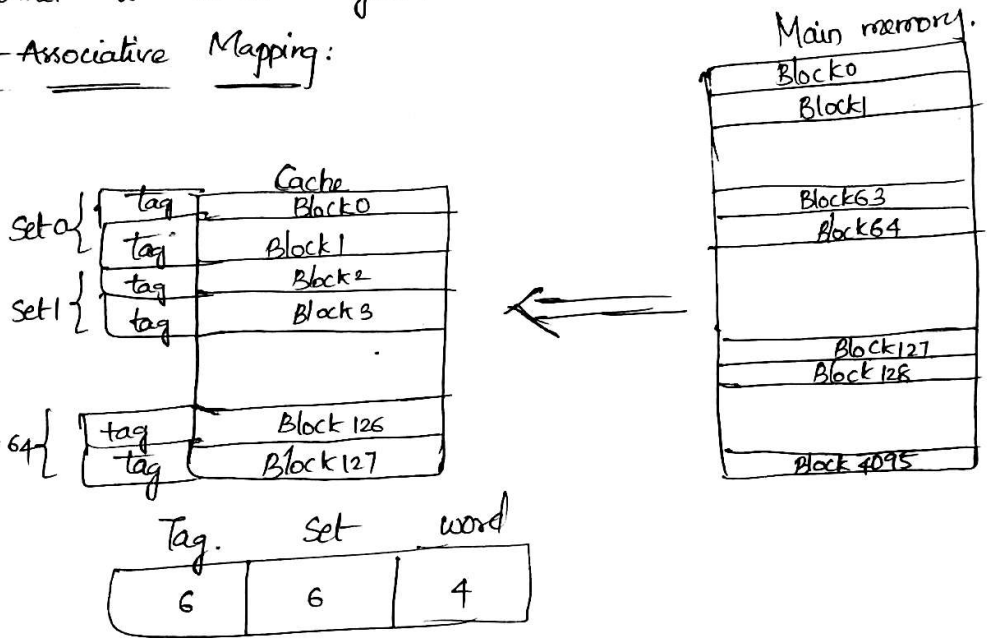
Main memory address.

Any block of main memory can be placed in any b... Cache memory. Word is the data stored in a location.

Block is to be brought into Cache memory, one block of ... memory should be removed when the Cache is full. Algorithms ... decide which block of Cache is to be replaced, when the Cache ... full are called Replacement algorithms. One of the algorithm LRU (least Recently Used block) which is accessed long back.

Another is oldest algorithm. where oldest block is removed.

Set-Associative Mapping:



In Cache memory, some no. of blocks are taken as a set. Here, two blocks are taken as a set.

128 blocks = 64 sets.

Block 0, 64, 128, ... 4032 of main memory are placed in set 0 of Cache Memory. If the tag bit of a set matches with tag bit of Main memory, address is the required word. that set contains two blocks.

Ex: if set 0, Block 0 (or) Block 1 are in set 0, if tag bits in set 0 matches with tag bits in Main memory, then word required is present.

briefly Different modes of Transfer.

data is transferred from i/p device to memory & from memory o/p device with (or) without CPU.

with Processor, i/p to processor, processor to memory.
memory to processor, processor to o/p device is transferred.

Without Processor, directly transferred b/w I/O & memory

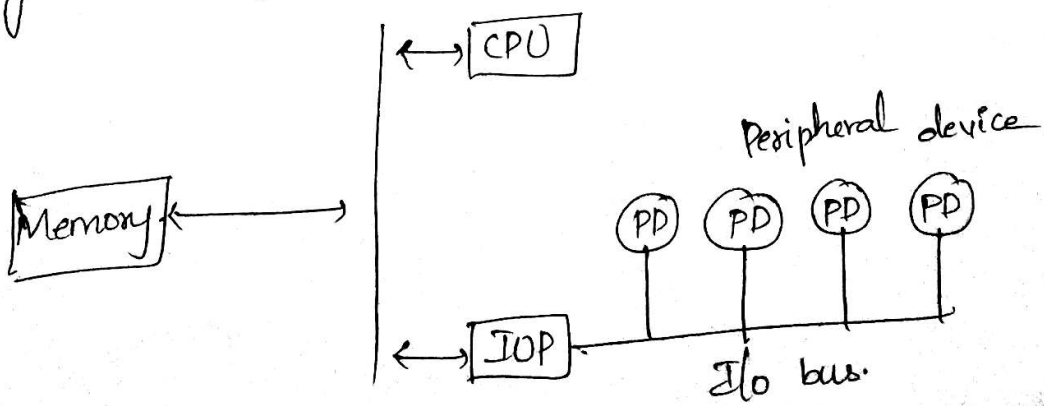
3 modes of Transfer:

1. Programmed I/O: through CPU.
If CPU is fast device & I/O is slow device, CPU should continously check whether the device is ready to transfer data or not. By this, CPU time is wasted and not efficiently used.

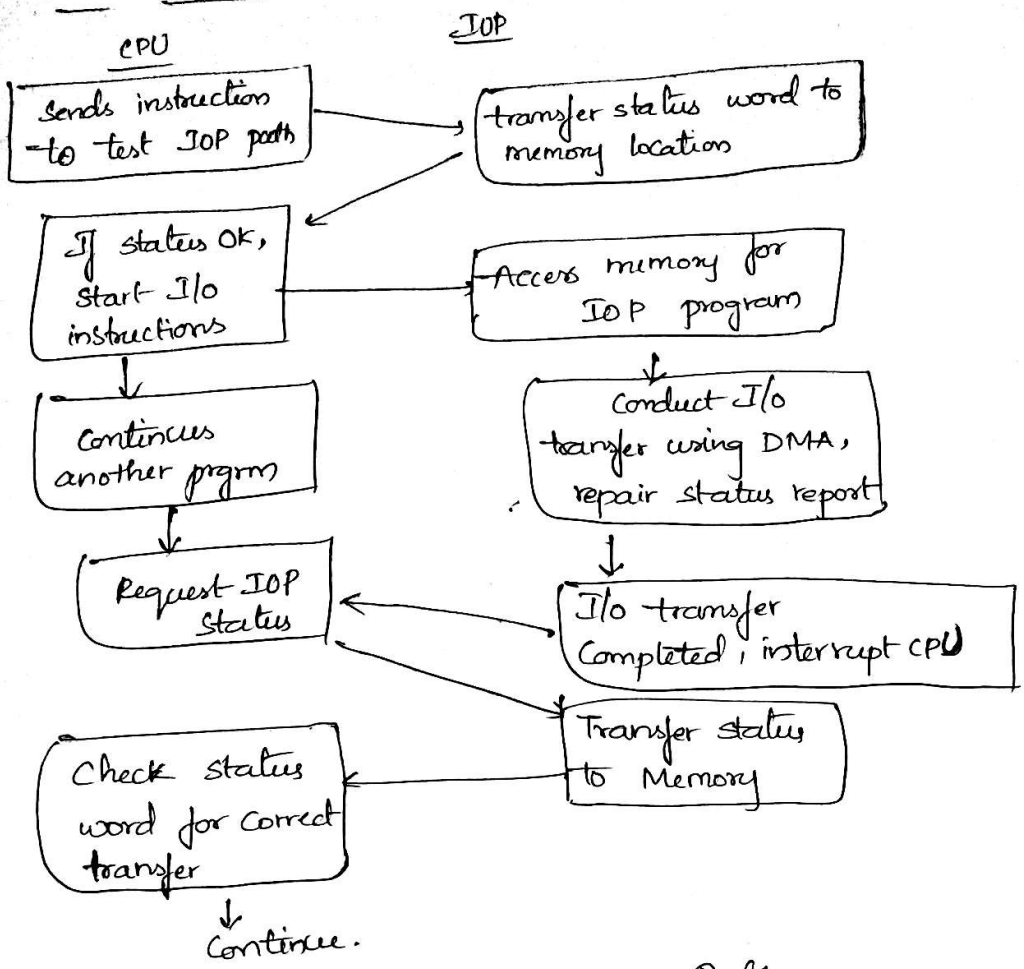
2. Interrupted initiated I/O: To overcome this interrupt initiated I/O is used in which we are using interrupt facility where the interface interrupts CPU whenever device is ready to perform data transfer. Meanwhile, CPU can be used to execute another program. Then, CPU need not Continously check whether device is ready or not.

3. DMA → Direct Memory Access: Directly transfering data b/w I/O & memory without Processor.

4. Explain Input Output Processor:
Purpose of IO processor is to perform data transfer b/w Memory and peripheral devices i.e., I/O devices. when No IOP, CPU tranfers data from memory to IO device.



CPU-IOP Communication:



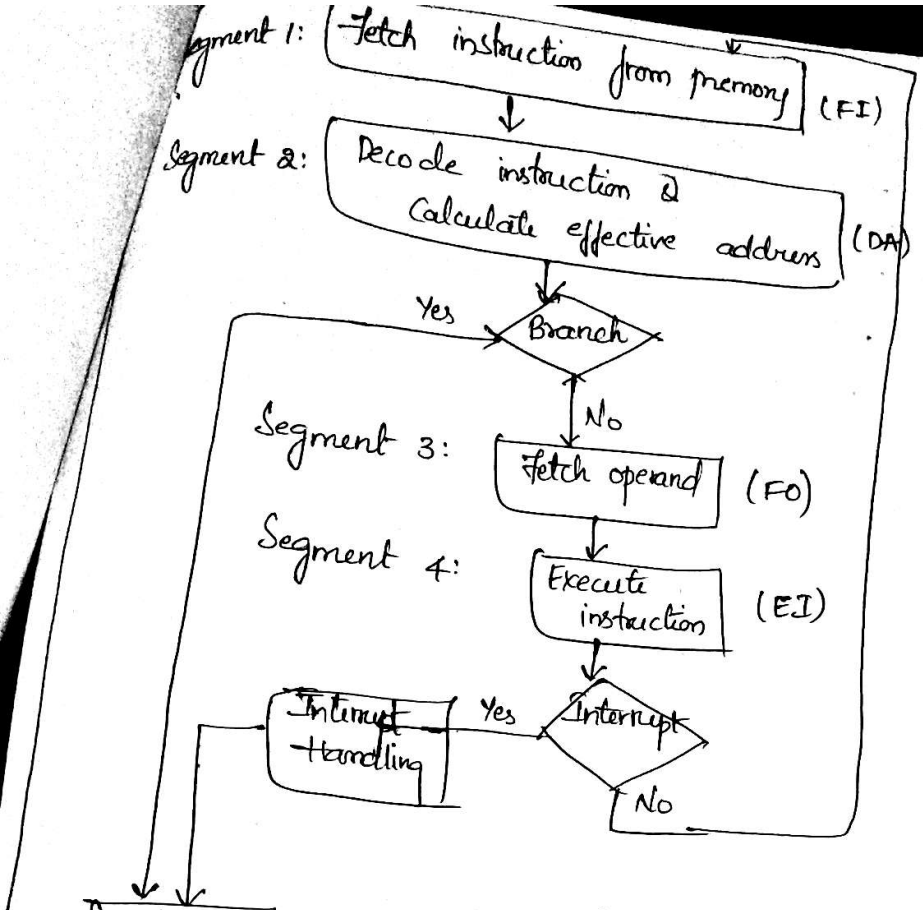
5. Explain 4-Segment Instruction Pipeline.

Used to process multiple instructions simultaneously.

1. Fetch instruction from Memory.
2. Decode instruction
3. Calculate Effective Address
4. Fetch operands from memory
5. Execute the instruction
6. Store result in proper place.

These 6 steps are divided in to 4 Segments and

Flow chart for 4-Segment Instruction pipeline is;



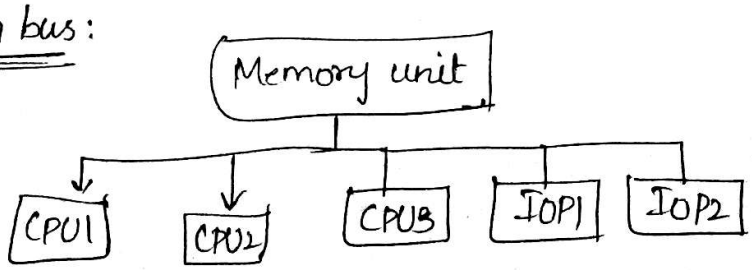
Here, Branching is done for step-3.

then,

Step	1	2	3	4	5	6	7	8	9	10	11	12	13
Instruction 1	FI	DA	FO	EI									
2		FI	DA	FO	EI								
3			FI	DA	FO	EI							
4				FI	-	-	FI	DA	FO	EI			
5					-	-	-	FI	DA	FO	EI		
6									FI	DA	FO	EI	
7										FI	DA	FO	EI

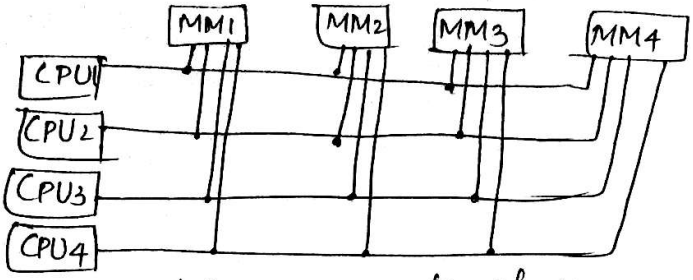
. Different InterConnection Structures in Multiprocessor System? Explain them.

e shared, Common bus:



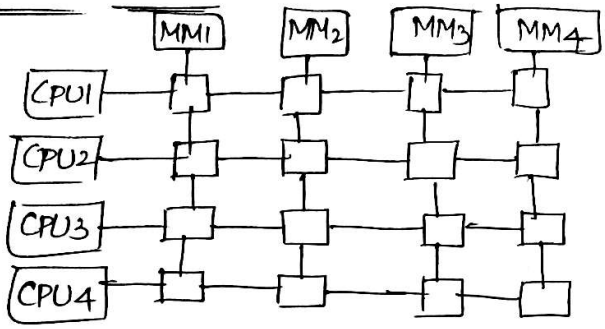
ingle bus b/w processor & Memory. when one uses Memory, other has to wait.

Multiport Memory:



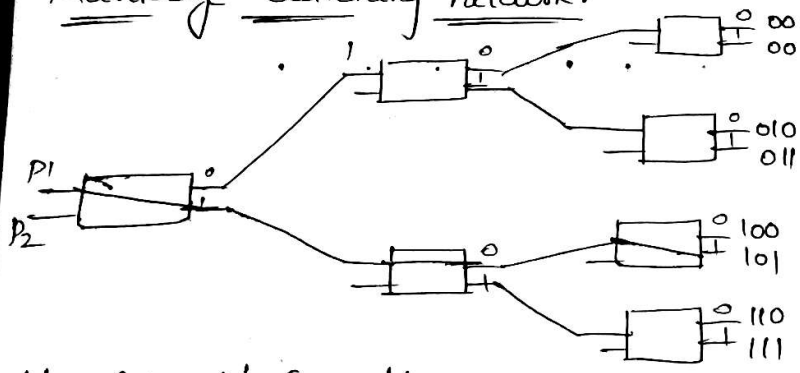
Memory Modules are parts of memory units. It Contains multiple port and each port Connected to ~~each~~ one processor.

Crossbar Switch:



Here, Single port is a Memory module. Switches are used to eshtablish the path b/w CPU and Memory module. All switches along the path should be on for transfer to take place.

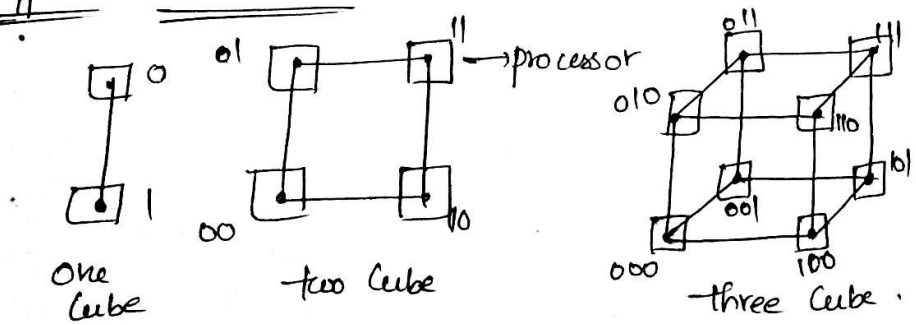
Multistage Switching network:



Addrees of memory Modules.

P_1, P_2 Indicates processors as i/ps and 0 & 1 as o/p's. The Connection is to be eshtablished b/w processor and Memory module. Here, 101 → is Connected.

HyperCube interConnection:



One Cube — two Cube — three Cube.

It is loosely coupled (or) distributed memory multiprocessor System.

For 1 Cube, 2^1 nodes, for 2 Cube, 2^2 nodes.

///ly for n Cube, 2^n nodes. for n cube, we interConnect 2^n processors.

-The Successive 2 nodes differ by only 1 bit.