REVIEW QUESTIONS FOR 2nd MID EXAM [3,4, 5]

Short Questions:

1. What is the difference between Static and Dynamic RAM?
2. Define Hit & Miss in cache.
3. What is a virtual Memory?
4. Differentiate Isolated and memory mapped I/O.
5. What is the difference between a vectored and a Non-vectored Interrupt?
6. Give the Flynn's classification of computers.
7. What is Pipelining? How does it increase the speed of computers?
8. What is delayed load and delayed branch in RISC pipeline?
9. What are the characteristics of a multiprocessor?
10. Differentiate tightly and loosely coupled multiprocessors.
11. Define a normalized floating point number.
12. What is Booth's algorithm?
13. Give the three ways of representing negative fixed point binary numbers?
14. What is meant by memory access time?
15. What is locality of Reference?
16. What is a pipeline hazard?
17. Define crossbar switch?
18. What is the basic component of a multistage network?
19. Define cache coherence?
20. Define Multicomputer and Multiprocessors?

Long Questions:

1. What are the different mapping techniques used in Cache memories. Explain in detail.
2. Explain how address translation is achieved using TLB (Translation look-aside buffer)
3. What are the different modes of data transfer? What is Interrupt-Initiated I/O? Explain
4. Explain about the DMA mode of data transfer.
5. What is an IOP. Explain about CPU-IOP communication.
6. Explain about Arithmetic Pipeline.
7. Explain about four segment Instruction pipeline?
8. Briefly explain RISC pipeline. How NOP instruction is used to resolve conflicts in pipeline.
9. What are the different pipeline conflicts? Explain
10. Briefly explain about Array Processors.
11. Write short notes on vector processing. Mention some applications of vector processors.
12. Explain about the different Interconnection structures used in multiprocessor environment.
13. Explain Cache coherence problem and solutions to it.
14. Explain step by step process of multiplying +15 with -13 using Booths algorithm.
15. Explain 4 bit by 3 bit array multiplier with neat diagram.
16. Give the algorithm for performing restoring division with example.

17. Give the algorithm for performing non-restoring division. With example.
18. What is virtual Memory ? Explain paging mechanism with diagram.
19. List and explain various categories of computers in Flynn's classification.
20. Explain about PCI bus
21. Explain about IEEE 488 bus?

A computer system uses pipeline technique to process computer instructions. Assume the time it takes to process an operation in each segment is equal to t_p=20ns. Assume this pipeline has k=4 segments and exceeds n=100 instructions in sequence. Answer the following (CO6)

i) How long time to execute 100 instructions does this computer take with this pipeline. $(k+n-1)t_p = (4+99) \times 20 = 2060$ ns.

ii) How long time does it take with non-pipeline(T_{np}) $= nt_n = nkt_p$ $(t_n = kt_p)$ $= 100 \times 4 \times 20 = 8000$ ns

iii) What is speed up? $= \frac{8000}{2060} = 3.88$

A computer system uses pipeline technique to process computer instructions: Assume the time it takes to process an operation in each segment is equal to t_p=20ns. Assume this pipeline has k=4 segments and exceeds n=100 instructions in sequence. Answer the following (CO6)

iv) How long time to execute 100 instructions does this computer take with this pipeline.

v) How long time does it take with non-pipeline(T_{np})

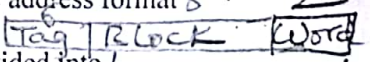
vi) What is speed up?

(Or)

22. Construct a diagram for a 8x8 omega switching network. Show the switch setting required to connect Processor 3 to MM 1?

2. A digital computer has a memory unit of 64k x 16 and a cache memory of 1k words. The cache uses direct mapping with a block size of four words(CO5)

a) How many bits are there in the tag,index,block & word field of the address format



b) How many bits are there in each word of a cache ,how are they divided into functions ? Include a valid bit.? →

index = 10 bit
cache address = 16 bit address
= 23 bits in each word of cache

c) How many blocks can the cache accommodate?

b) $\frac{1K}{4} = 256$

23. Explain in detail about Input-Output Processor (IOP).

$2^{16} = 64K$
$2^8 = 256$ block
$2^{10} = 1K$