MPMC Assignment-II

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(1) What happens when Gate=1 in TMOD Register. (8051)

Mode control Register: (TMOD), (SFR address-89H)

The mode control register TMOD of 8051 allows gating control over the timers, selects each timer for either timer or counter operation and sets one of the four modes of operation of the timers or counters. The

D7	D6	D5	D4	D3	D2	D1	D0
Gate 1	C/T_1	M1	M0	Gate 0	C/T_0	M1	M0
Timer/counter 1				Timer/counter 0			

Fig Bit definitions of 8051 TMOD Register.

The upper nibble of the TMOD Register is used for programming Timer 1 configuration while the lower nibble is used for programming Timer 0 configuration.

If a Gate bit is '1' the respective timer or counter will have the Gate function activated. $\overline{INT0}$ will act as input for Timer/Counter 0 while $\overline{INT1}$ will act as gate input for Timer/Counter 1. If the gate bit is '1', the respective timer or counter will count up only if the $\overline{INT0}$ or $\overline{INT1}$

(for T0 or T1) is high. If INT pin goes high then the counting will be withhold till the $\overline{INT}$ pin goes high. The hardware way of starting and stopping the timer by an external source is achieved by making GATE = 1 in the TMOD Register.

(2) Operation Command Words (in 8259) (OCW2 & OCW3)

Once 8254A is initialised using the ~~previously discussed~~ command words for initialisation, it is ready for the normal function i.e. for accepting the interrupts but 8259A has its own ways of handling the received interrupts called as modes of operation. These modes of operation can be selected by programming i.e. writing three internal registers called as operation command word registers. The data written into them (bit pattern) is called as operation command words. In these operation command words OCW1, OCW2, OCW3, every bit corresponds to some operational feature of the mode selected, except for the few bits those are either '1' or zero.

In OCW2, the three bits R_2, R_1, R_0, SL and EOI control the end of interrupt, the rotate mode and their combinations as shown in fig(b). The three bits L_2, L_1 and L_0

In OCW2 determine the interrupt level to be selected for operation, if the SL bit is active, ie. '1'. The details of OCW2 are shown in Fig. 6.18(b)

A_0	D7	D6	D5	D4	D3	D2	D1	D0
1	R	SL	EOI	0	0	L2	L1	L0

End of Interrupt	0	0	1	Non specific EOI command
	0	1	1	Specific EOI command
Automatic Rotation.	1	0	1	Rotate on nonspecific EOI command
	1	0	0	Rotate in automatic EOI mode (set)
	0	0	0	Rotate in automatic EOI (clear)
Specific Rotation.	1	1	1	Rotate on specific EOI command
	1	1	0	Set priority command*
	0	1	0	No operation.

* In this mode L0-L2 are used.

Fig. 6.18. (b)

In operation command word 3 (OCW3), if the ESMM bit i.e. Enable Special Mask mode bit is set to '1', the SMM bit is enabled to select or mask the special mask mode. When ESMM bit is '0', the SMM bit is neglected. If the SMM bit, ie. Special Mask Mode bit is '1', the 8259A will enter special mask mode provided ESMM = 1

If ESMM = 1 and SMM = 0, the 8259A will return to

the normal mask mode. The details of bits of OCW3 are given in Fig. 6.18(c) along with their bit definitions.