

UNIT IV

DIGITAL INTEGRATED CIRCUITS

→ Diff. Logic families, TTL

↳ Standard, Totem pole op.

collector Schottky, Transistor

TTL

CMOS → CMOS NAND, CMOS NOR, open drain

and ~~open~~ - state Op.

IEE manufacturing - TTL with CMOS, CMOS with TTL

combinational IC's - DeMorgan, Inverter, Adder,

Subtraction, Max, Comparator, etc.

Digital Fundamentals - Floyd and Jain

or

Digital Design by Makhrely

Logic Family

A group of compatible IC's with the

same logic levels and supply voltages

which perform various logic functions and

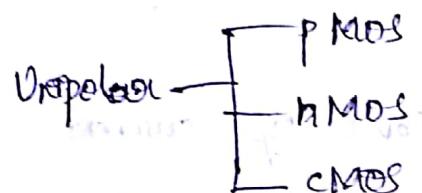
are fabricated as per the specific circuit

configurations is called a logic family. They are classified as

Bipolar logic family and Unipolar logic family.

→ Bipolar " uses bipolar devices like diodes & transistors

→ Unipolar " uses unipolar devices like MOSFETs.



Bipolar

Saturated

RTL

DTL

HTL

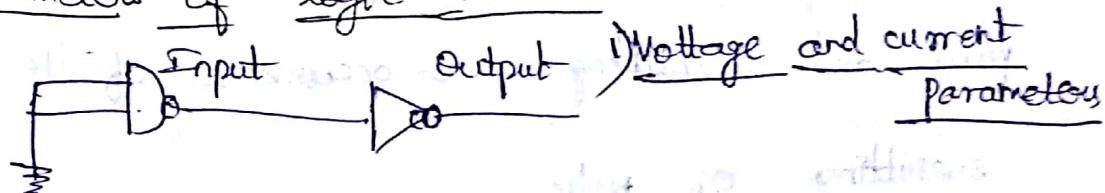
DETL

TTL
ECL or ECL

Unsaturation

Schottky TTL ECL

Parameters of logic families:



There are two types of V and I levels

Parameters for logic families.

They are
 V_{IH} - High level ϕ /voltage (logic-1)
 V_{IL} - Low " " " " (logic-0)

V_{OH} - High " " " " "

V_{OL} - Low " " " " "

Similarly, there are 4-current parameters.

I_{IH} - High level ϕ /current

I_{IL} - Low " " " "

I_{OH} - High level ϕ /current

I_{OL} - Low " " " "

⇒ Fan-out (loading factor)

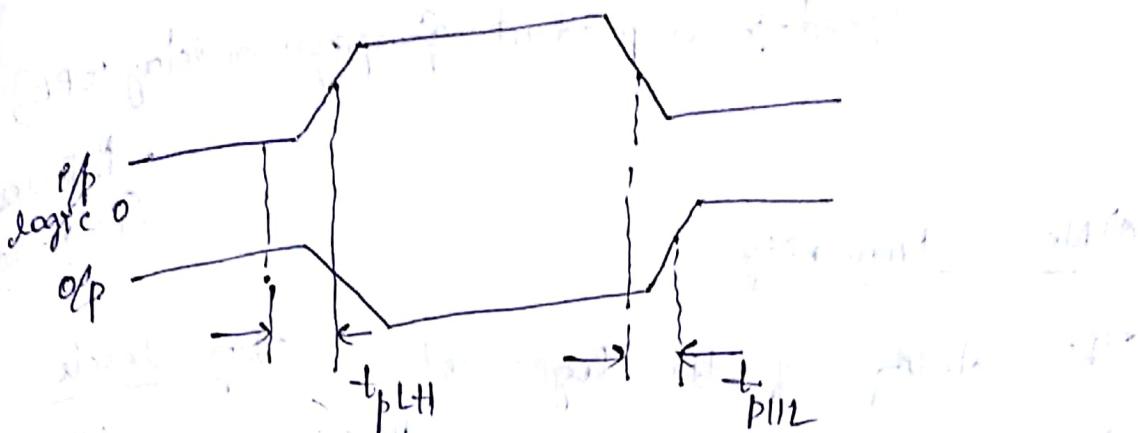
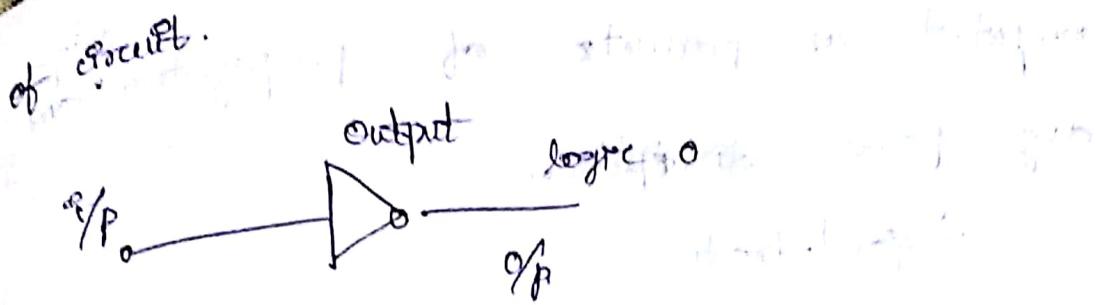
The maximum no. of similar gates which the given gate can drive is fan out.

→ High fanout is advantage.

⇒ Propagation delay (speed of the operation)

It is the propagation delay of the gate is the time interval b/w the application of the ϕ pulse and resulting occurrence of the resulting ϕ pulse.

It limits the speed of operation. The shorter the propagation delay, higher the speed



$$\text{Propagation delay} = \frac{t_{pLH} + t_{pHL}}{2}$$

4) Power dissipation!

The ~~greater~~ amount of power dissipated by any

circuit is determined by the avg. supply current

I_{cc} i.e obtained from the power supply V_{cc} .

$$\therefore \text{Power dissipation} = V_{cc} \times I_{cc}$$

$$P.D = V_{cc} \times I_{cc}$$

$$I_{cc} \text{ avg} = \frac{I_{ccH} + I_{ccL}}{2}$$

5) Figure of Merit: (speed, power product)

For any digital IC, it is desirable to have shorter propagation delays (higher speed) and

lower value of power dissipation. It is

computed as product of propagation delay and avg. power dissipation

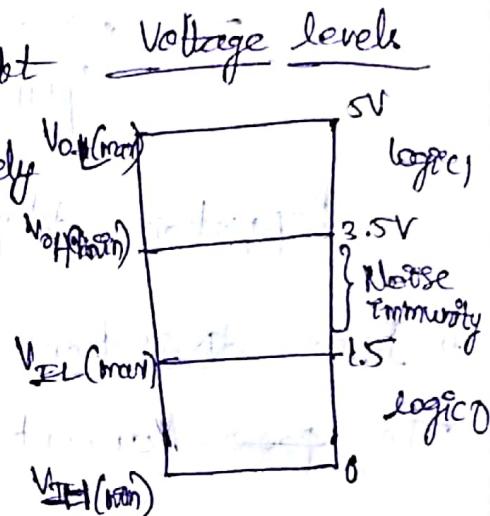
Speed Product

$$\therefore \text{Speed-power product} = (\text{propagation delay} \times \text{PD})$$

P. Joules
(Microjoules)

b) Noise Immunity:

The ability of the logic circuit to tolerate noise and effectively prevent the changes in the output is termed as noise immunity.



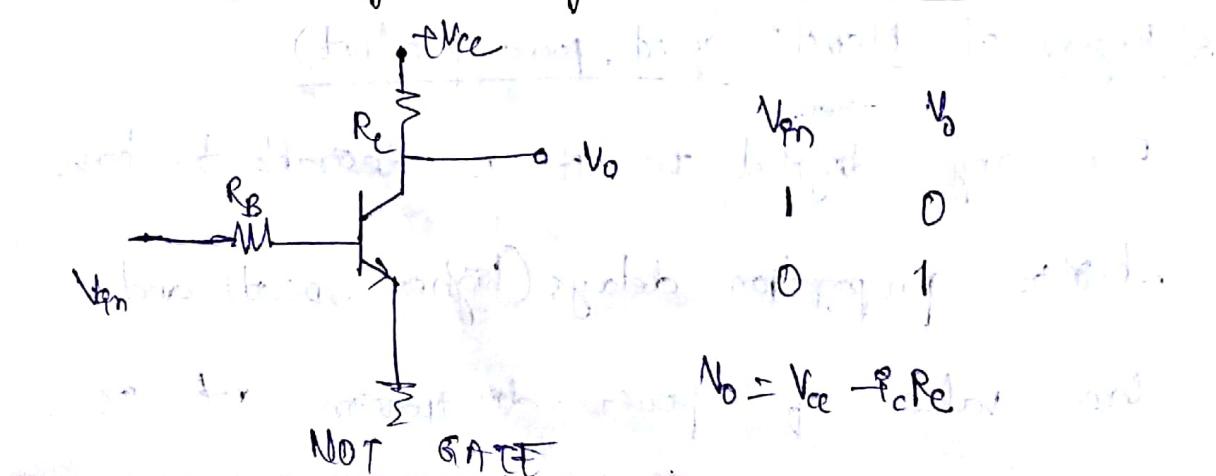
It is measured in terms of noise margin.

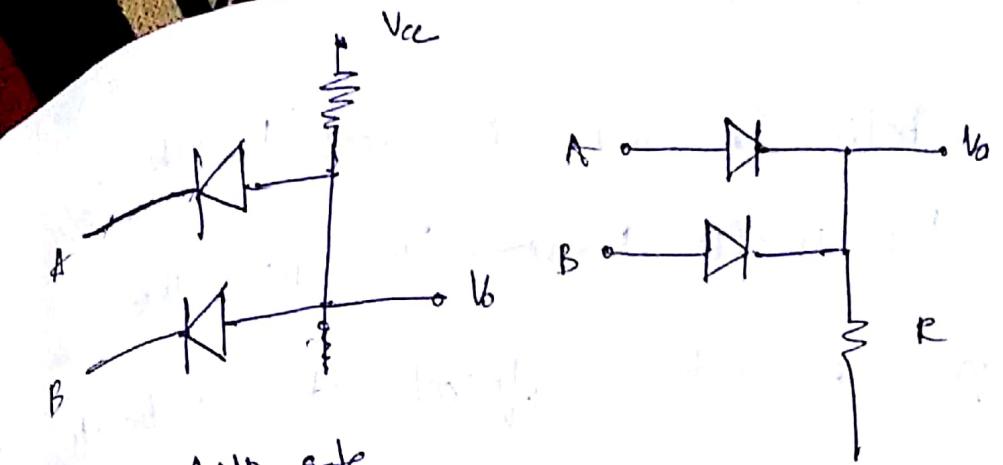
$$\text{High state Noise margin} = V_{OH} - V_{ON}$$

$$\text{Low state Noise margin} = V_{OL} - V_{ON}$$

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Logical gates using electronic devices:



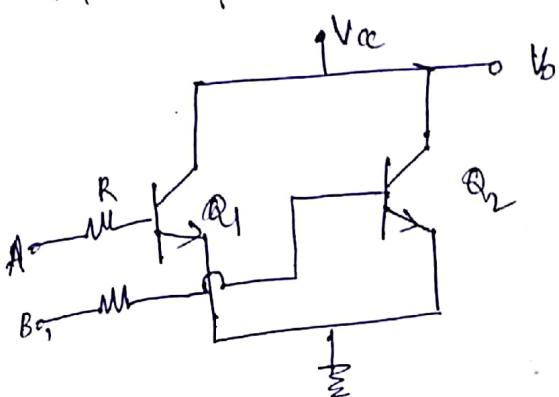


AND gate

A	B	V _o
0	0	0
0	1	0
1	0	0
1	1	1

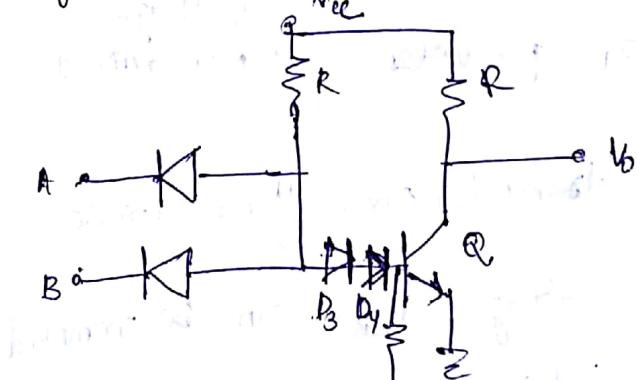
OR gate

A	B	V _o
0	0	0
0	1	1
1	0	1
1	1	1



RTL NOR gate

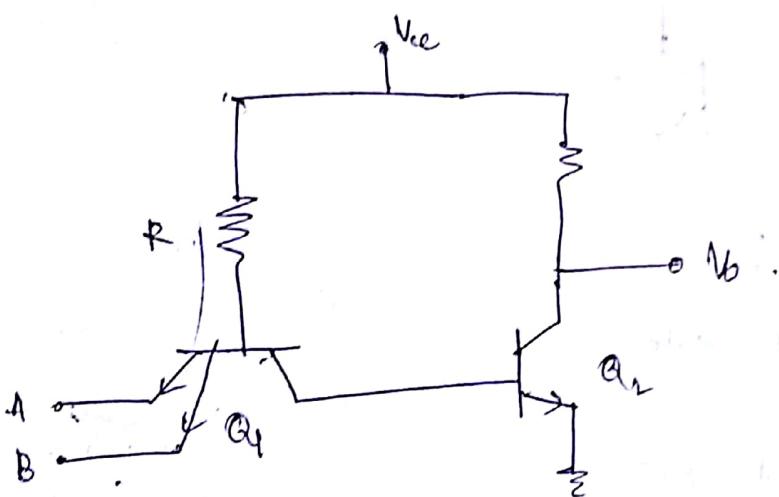
Design a NAND gate:



A	B	Q	V _o
0	0	off	1
0	1	off	1
1	0	off	1
1	1	on	0

When both A and B are '1', the V_{ce} flows towards the transistor Q_1 , but the voltage is not sufficient to make the transistor ON, hence, the diodes $D_3 \& D_2$ are added to decrease the voltage at the base of the transistor.

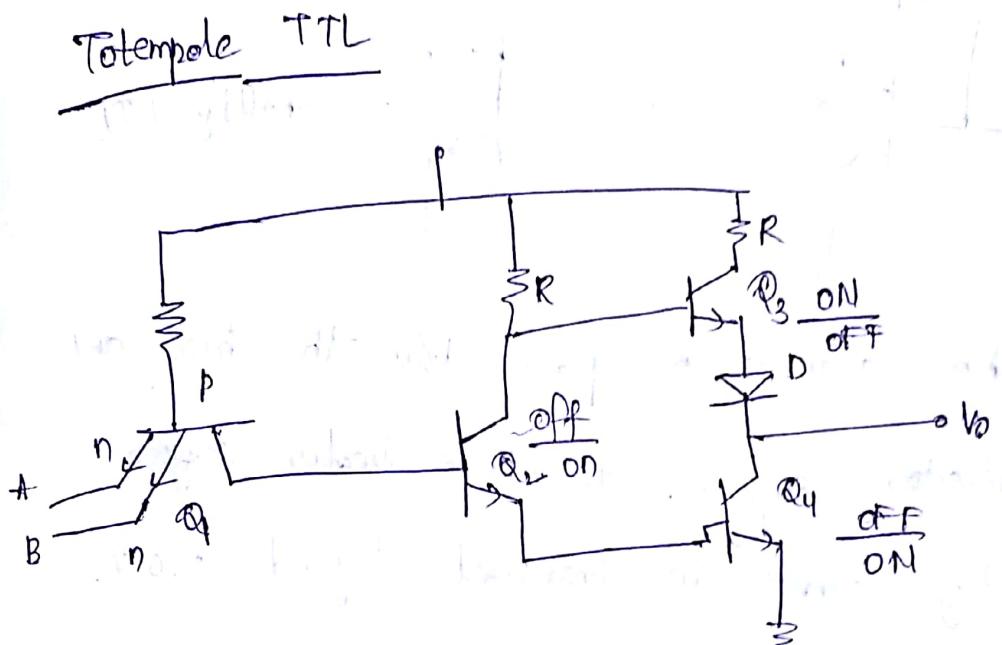
Simple TTL gate:



The transistor Q_1 provides the required voltage for logic 1 of transistor Q_2 . Hence diode D_3 & its base voltage V_{BB} can be removed.

A	B	Q_1	Q_2	V_b
0	0	ON	OFF	1
0	1	ON	OFF	1
1	0	ON	OFF	1
1	1	OFF	ON	0

When both A & B are '1' and one transistor Q₁ is off and Q₂ is ON. All the V_{cc} power supply will be flowing towards Q₂ ground, which increases the sink current. Hence, to eliminate this problem Totempole TTL is used.



Truth Table:

A	B	Q ₁	Q ₂	Q ₃	Q ₄	V ₀
0	0	on	off	on	off	1
0	1	on	off	on	off	1
1	0	on	off	on	off	1
1	1	off	on	off	on	0

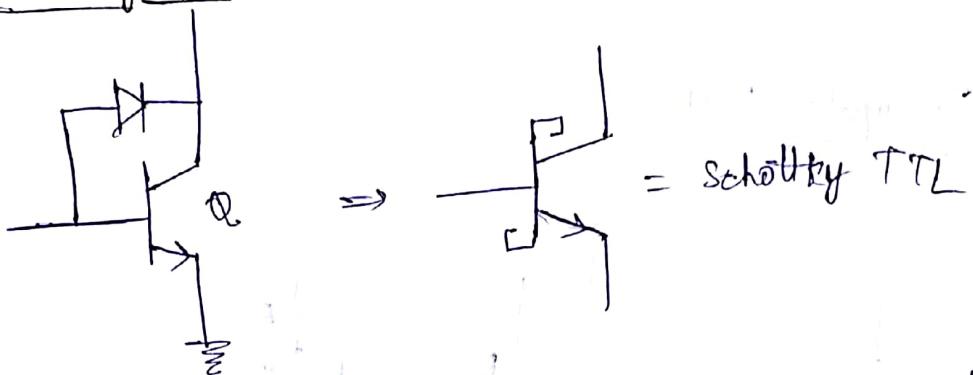
When A=B=0, Q₁=ON, Q₂=OFF, Q₃=ON, Q₄=OFF

$$V_0 = 1$$

When $A=B=1$, Q_1 -off, Q_2 -ON, Q_3 -off and Q_4 =ON.

but the turn-off time taken by the Q_3 transistor to off state is more than to change from ON state. Hence, for a short duration, Q_3 diode Q_4 is ON.

Schottky TTL:

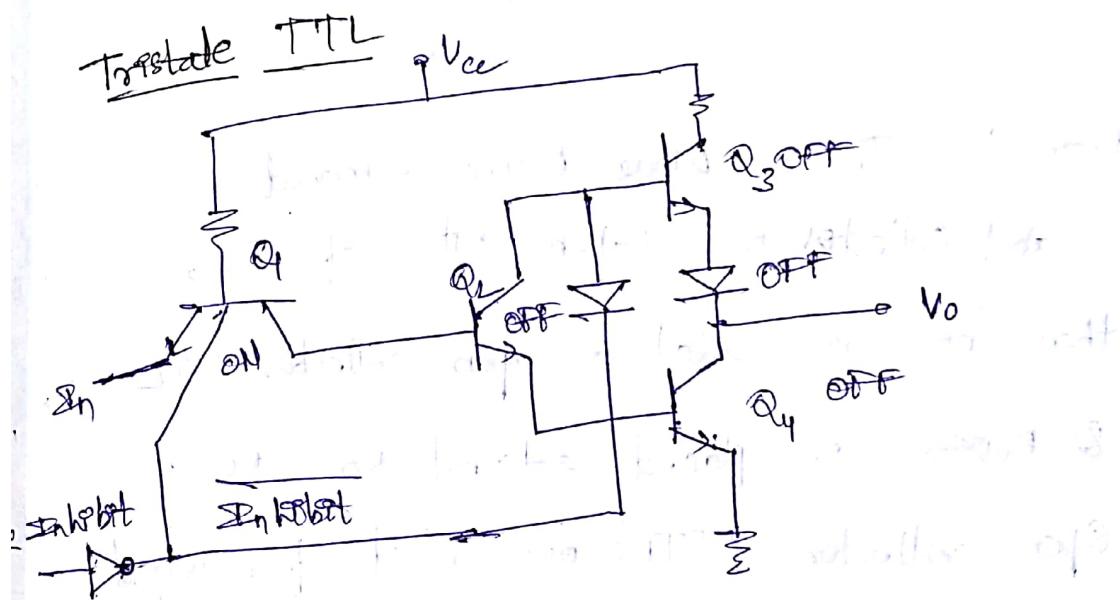
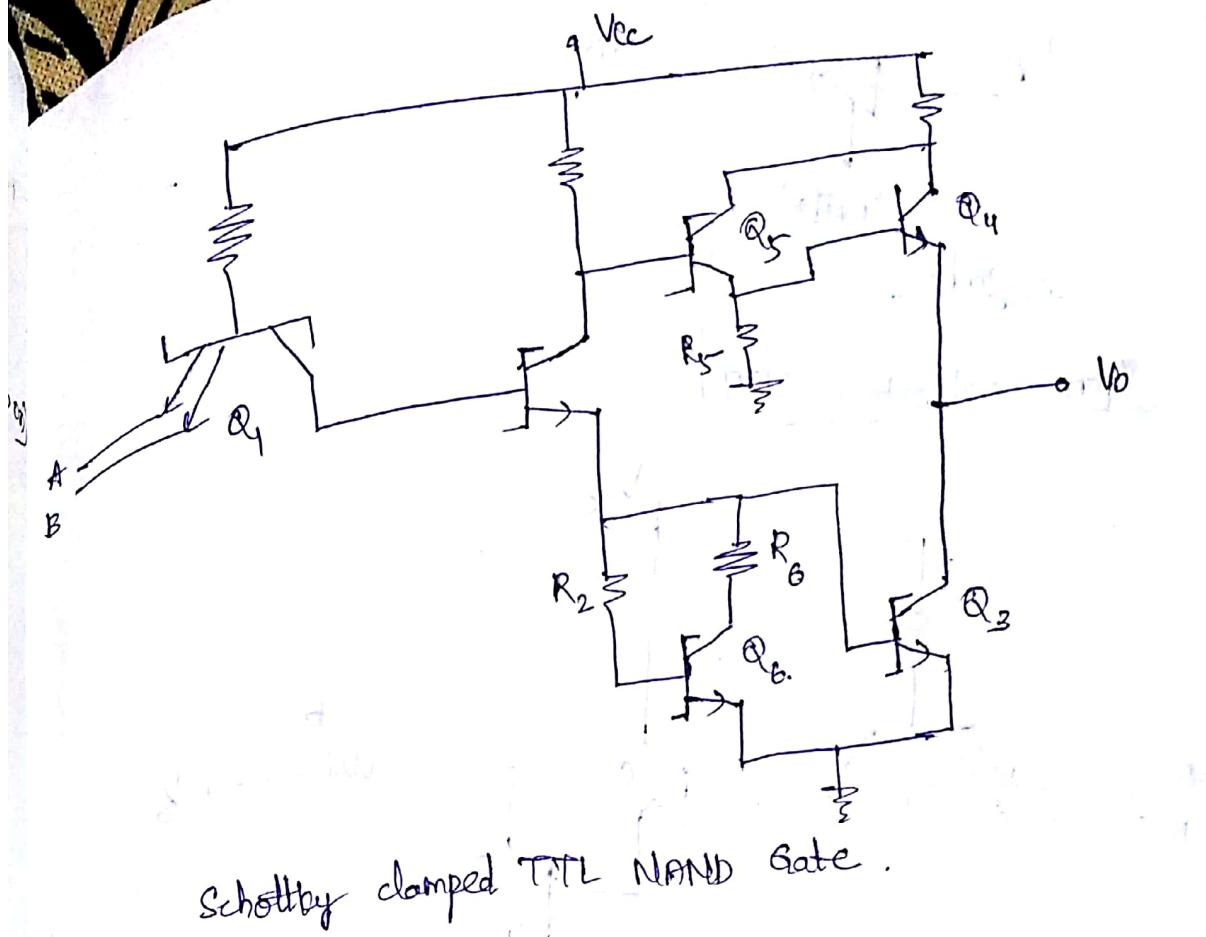


When a diode is placed b/w the base and collector region, the base-collector region

voltage cannot be increased beyond 0.6 V.

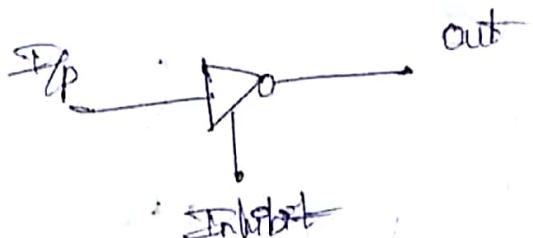
Hence, the transistor is only in active region.

By making the transistor to operate only in active region, the storage time can be reduced and hence the propagation delay can be reduced.



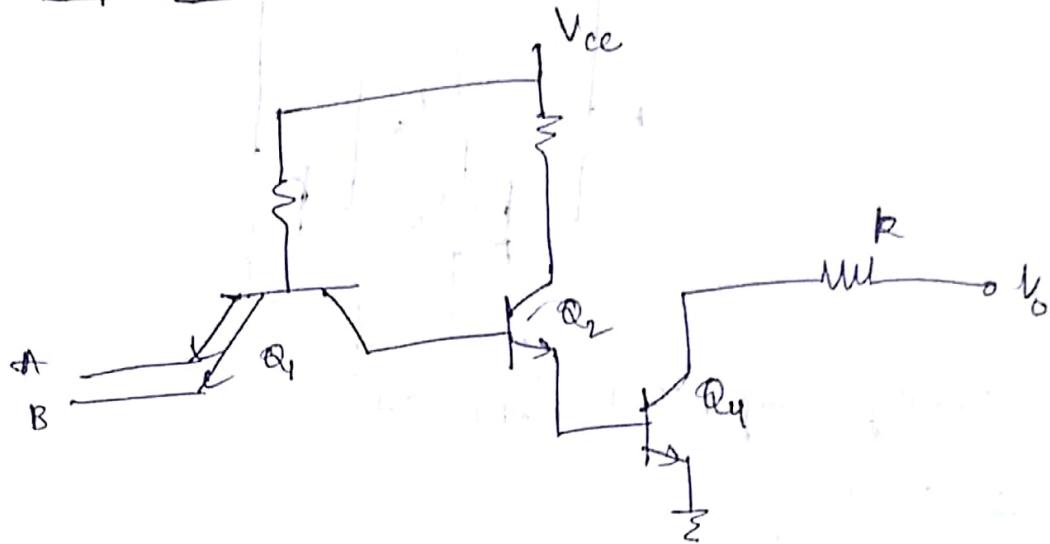
Truth Table:

Inhibit	I _{in}	V ₀
0	0	1
0	1	0
1	0 X	H _{H-Z}
1	1	0



Symbol.

Open collector TTL



Transistor T₃ & Diode D are removed

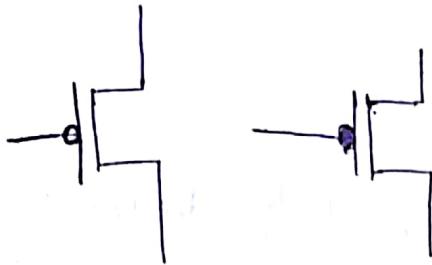
and collector is taken out of Fe_3 ,

then it is called as open collector TTL

& Resistor is placed external to E.

Open collector TTL's are used for wired connections & wired-AND logics.

CMOS:



pMOS

nMOS

for logic 1-low

logic 0-high

(Not gate)

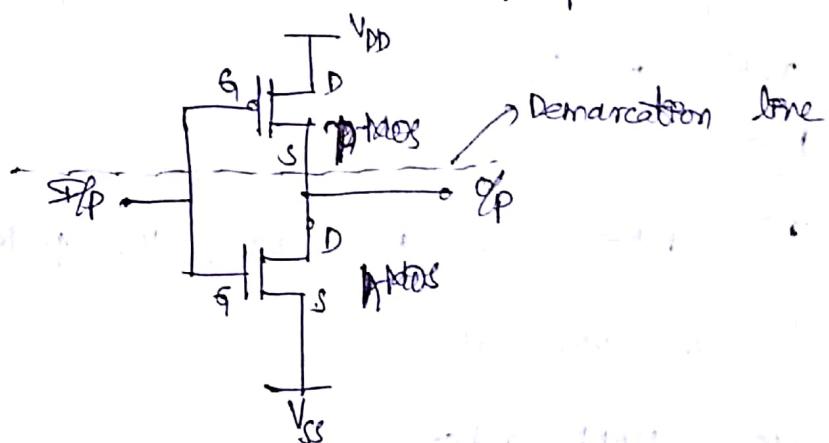
for logic 1 - high

logic 0-low

(Buffer gate)

→ Advantage of n-MOS over p-MOS is, the mobility of e^- 's is $>$ holes

→ CMOS is a combination of pMOS and nMOS



D/P	pMOS	NMOS	O/P
0	ON	OFF	H
1	OFF	ON	L

over TTL

Advantage of CMOS is, there will be no leakage current (If O/P = 1 \Rightarrow O/P = 0)

AND

For AND N-MOS - series

OR N-MOS - parallel

→ PMOS and n-MOS are separated by demarcation line

→ PMOS acts as pullup resistors or and called as pullup resistors (They are preferred in DC as it occupies less space).

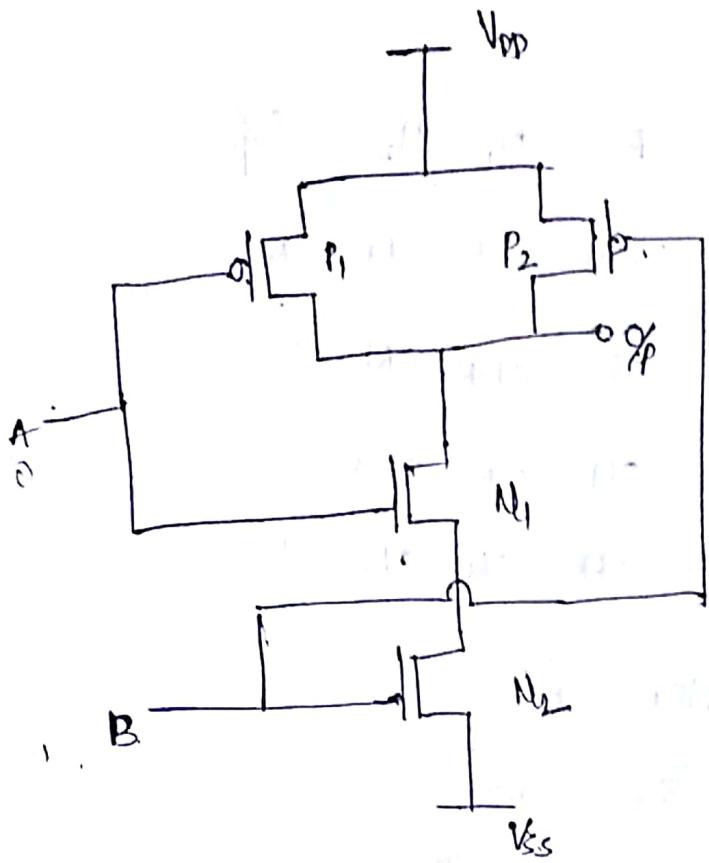
To perform AND operation, two n-MOS should be placed in series & for OR operation,

n-MOS in parallel.

Note:

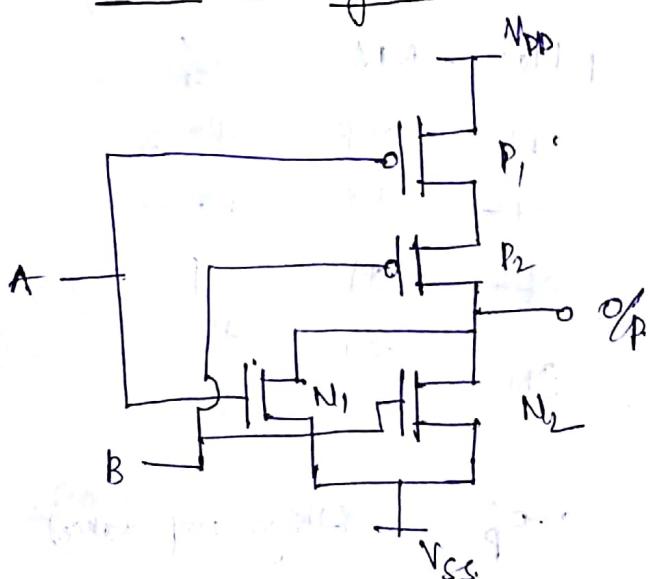
If n-MOS are in series, then PMOS in parallel & vice versa.

CMOS NAND gate:



A	B	P ₁	P ₂	N ₁	N ₂	O/p
0	0	ON	ON	OFF	OFF	H
0	1	ON	OFF	OFF	ON	H
1	0	OFF	ON	ON	OFF	H
1	1	OFF	OFF	ON	ON	L

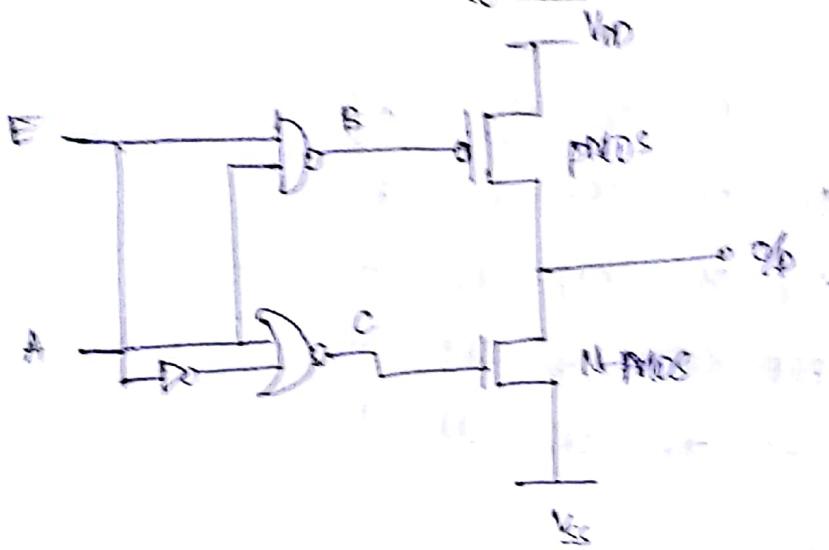
CMOS NOR gate:



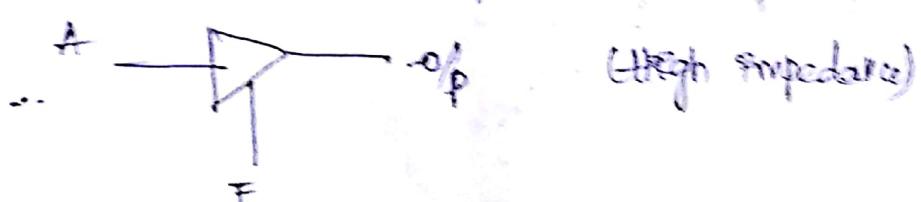
A	B	S	R	N_1	N_2	O/p
0	0	ON	ON	OFF	OFF	H
0	1	ON	OFF	OFF	ON	L
1	0	OFF	ON	ON	OFF	L
1	1	OFF	OFF	ON	ON	L

'Nor gate'

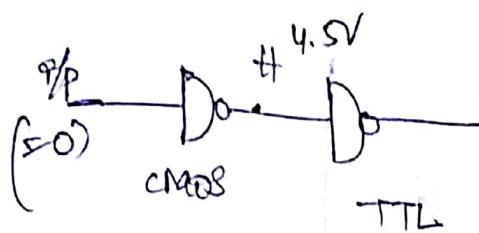
Inverter buffer gate



E	A	B	C	P-MOS	N-MOS	O/p
0	0	1	0	OFF	OFF	H-L
0	1	1	0	OFF	OFF	H-L
1	0	1	1	OFF	ON	L
1	1	0	0	ON	OFF	H



CMOS Driving TTL



If the CMOS op₁ is in high state, then it acts as a source resistor and can drive TTL cts. If the op₁ of the CMOS is in low state, then it acts as current sink. Hence, if the CMOS is of TLC & HCT, it can drive maximum of one TTL gate. Other CMOS series cannot drive any gate in the low state.

Code converters:

Binary, Octal, Hexadecimal

Decimal

BCD

Ex: $(25)_{10}$

$$= (11001)_2 \quad (0010\ 0101) \rightarrow \text{BCD}$$

① Design a logic circuit to convert 3-bit binary to gray code

Sols → Truth Table

→ K-map simplification

→ Logic diagram

D. Truth Table

Binary			Binary		
B_3	B_2	B_1	s_3	s_{12}	s_1
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

G_3

		G_3			
		B_3	B_2	B_1	
B_3	B_2	00	01	11	10
		0	1	1	1

$$G_3 = B_3$$

G_{12}

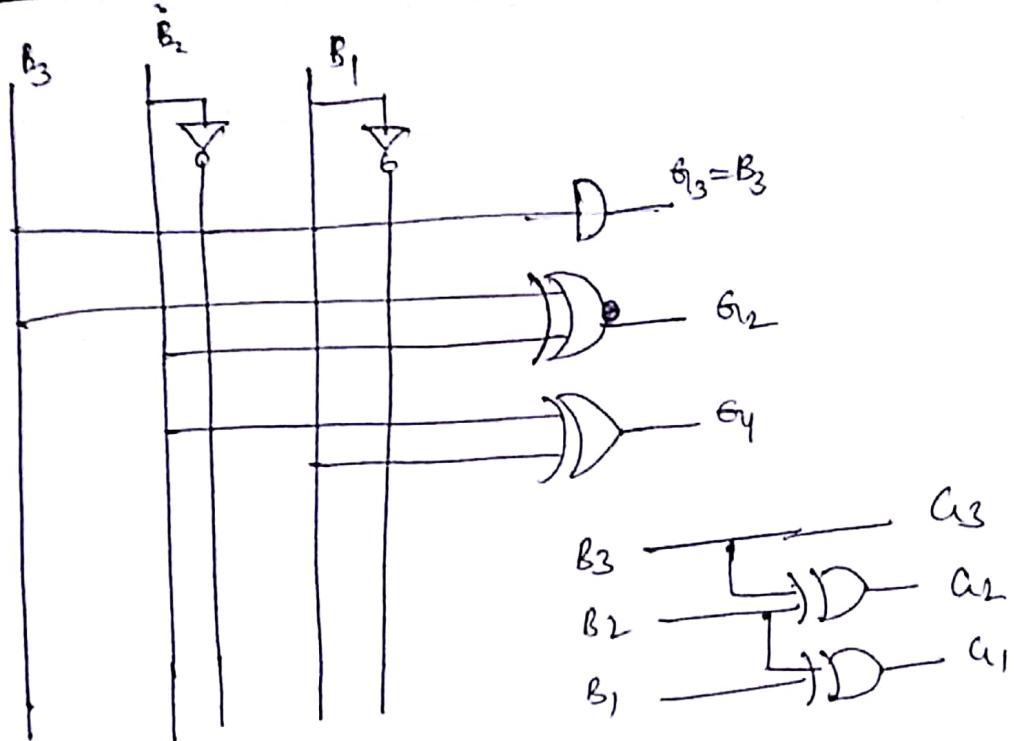
		G_{12}			
		B_3	B_2	B_1	
B_3	B_2	00	01	11	10
		0	0	1	1

$$\begin{aligned} G_{12} &= \overline{B}_3 B_2 + B_3 \overline{B}_2 \\ &= B_3 \oplus B_2 \end{aligned}$$

G_1

		G_1			
		B_3	B_2	B_1	
B_3	B_2	00	01	11	10
		0	1	0	1

$$\begin{aligned} G_1 &= \overline{B}_2 B_1 + B_2 \overline{B}_1 \\ &= B_1 \oplus B_2 \end{aligned}$$

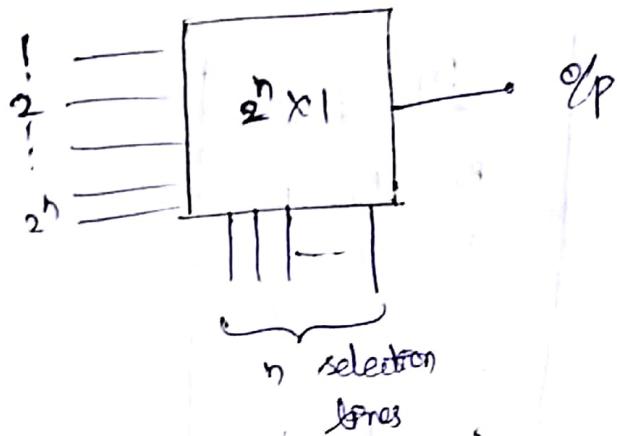


② Design a logic circuit for a 3bit gray to binary converter:

<u>Sole</u>	<u>Gray</u>	<u>Binary</u>
	$G_3 \quad G_2 \quad G_1$	$B_3 \quad B_2 \quad B_1$
	0 0 0	0 0 0
	0 0 1	0 0 1
	0 1 1	0 1 0
	0 1 0	0 1 1
	1 1 0	1 0 0
	1 1 1	1 0 1
	1 0 1	1 1 0
	1 0 0	1 1 1

$$B_3 = G_3$$

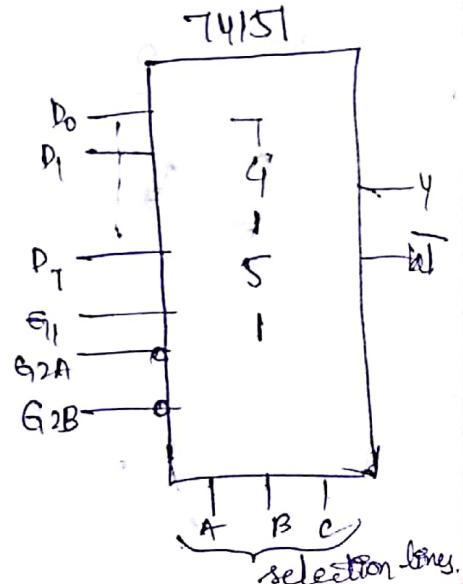
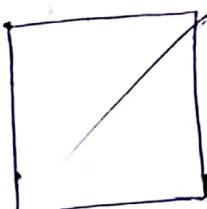
Multiplexer



n selection
lines

74151 is used as IC which is used

as a 8×1 MUX



① Design a full adder using IC 74151

Truth Table

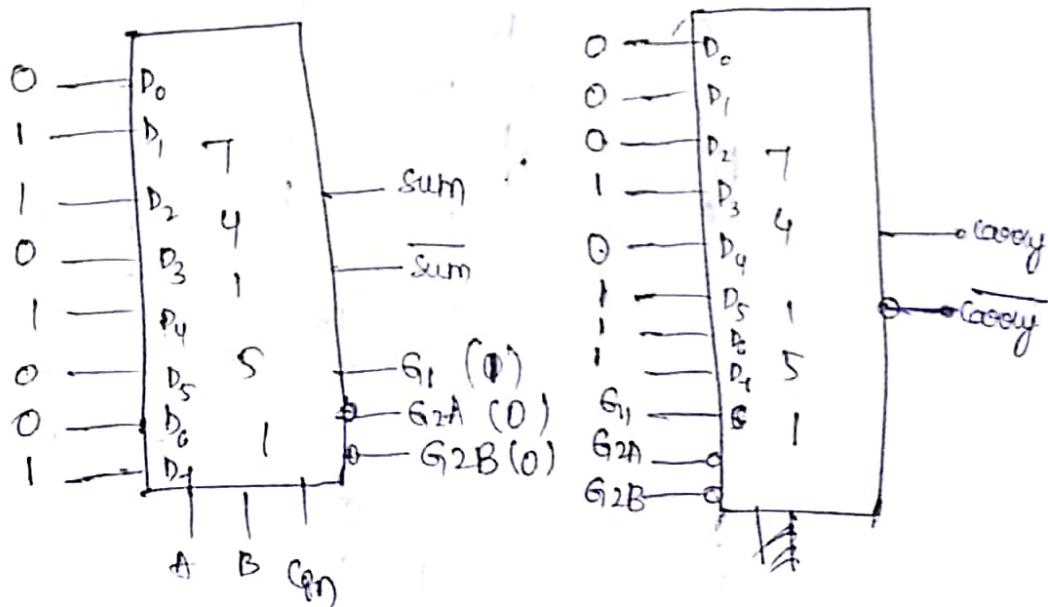
A	B	C _{in} (Carry)	sum	carry (out)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

• A → B_{in}

		00	01	11	10
		0	1	0	1
0		0	1	0	1
1		1	0	1	0

$$\text{Sum} = A\bar{B}\bar{C}_{in} + \bar{A}\bar{B}C_{in} + A\bar{B}C_{in} + \bar{A}B\bar{C}_{in}$$

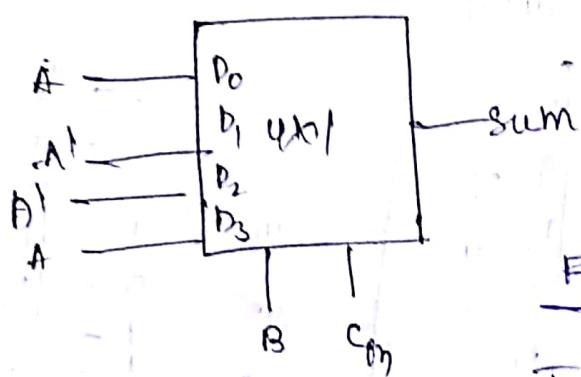
= 74151



② Design a full adder using 4N NOR

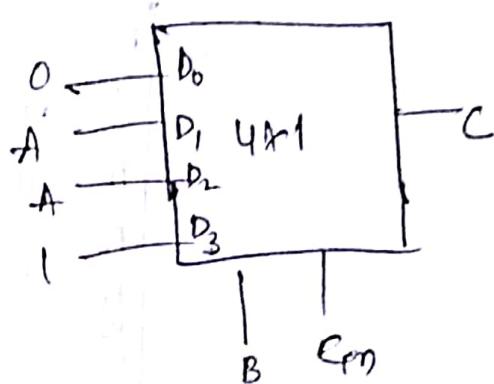
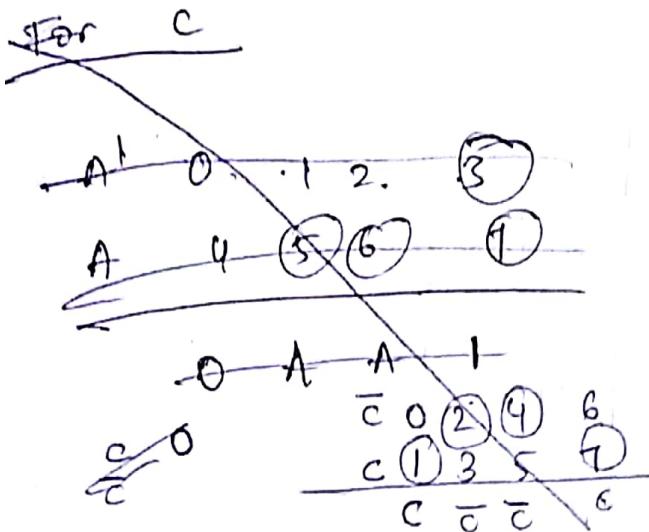
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\begin{array}{r}
 A^1 \quad 0 \quad 1 \quad 2 \quad 3 \\
 A \quad 4 \quad 5 \quad 6 \quad 7 \\
 \hline
 A \quad A^1 \quad A^1 \quad A
 \end{array}$$

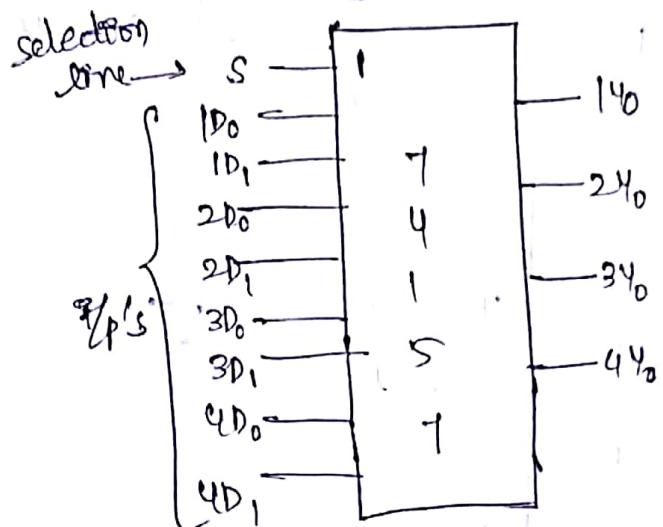


For C

$$\begin{array}{r}
 A \quad 0 \quad 1 \quad 2 \quad 3 \\
 A \quad 4 \quad 5 \quad 6 \quad 7 \\
 \hline
 0 \quad 0 \quad 1 \quad 0 \quad 1 \\
 0 \quad 1 \quad 0 \quad 1 \quad 0 \\
 1 \quad 0 \quad 1 \quad 0 \quad 1 \\
 1 \quad 1 \quad 1 \quad 1 \quad 1 \\
 \hline
 0 \quad A \quad A \quad 1
 \end{array}$$



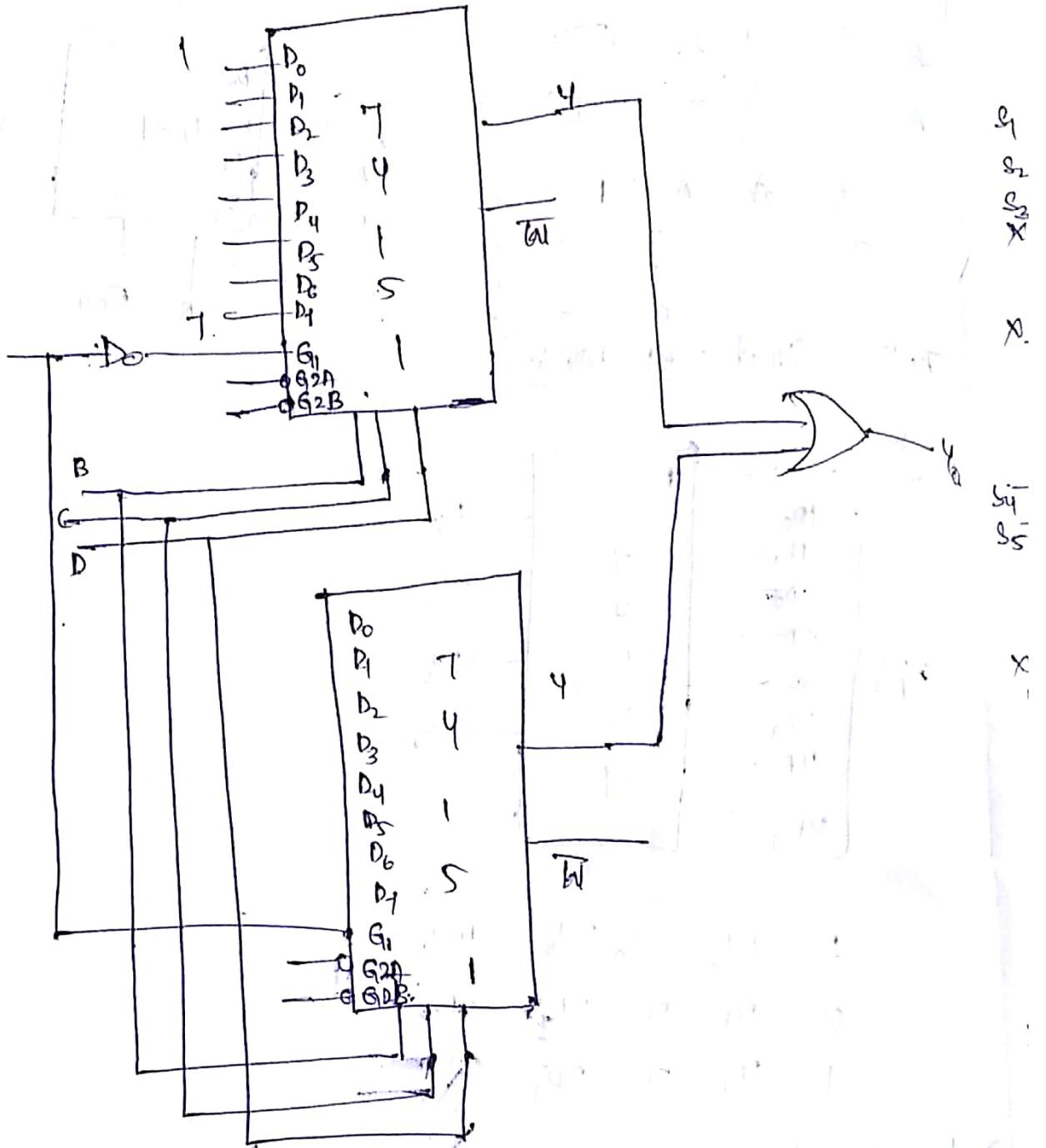
74151 Quad 2x1 MUX



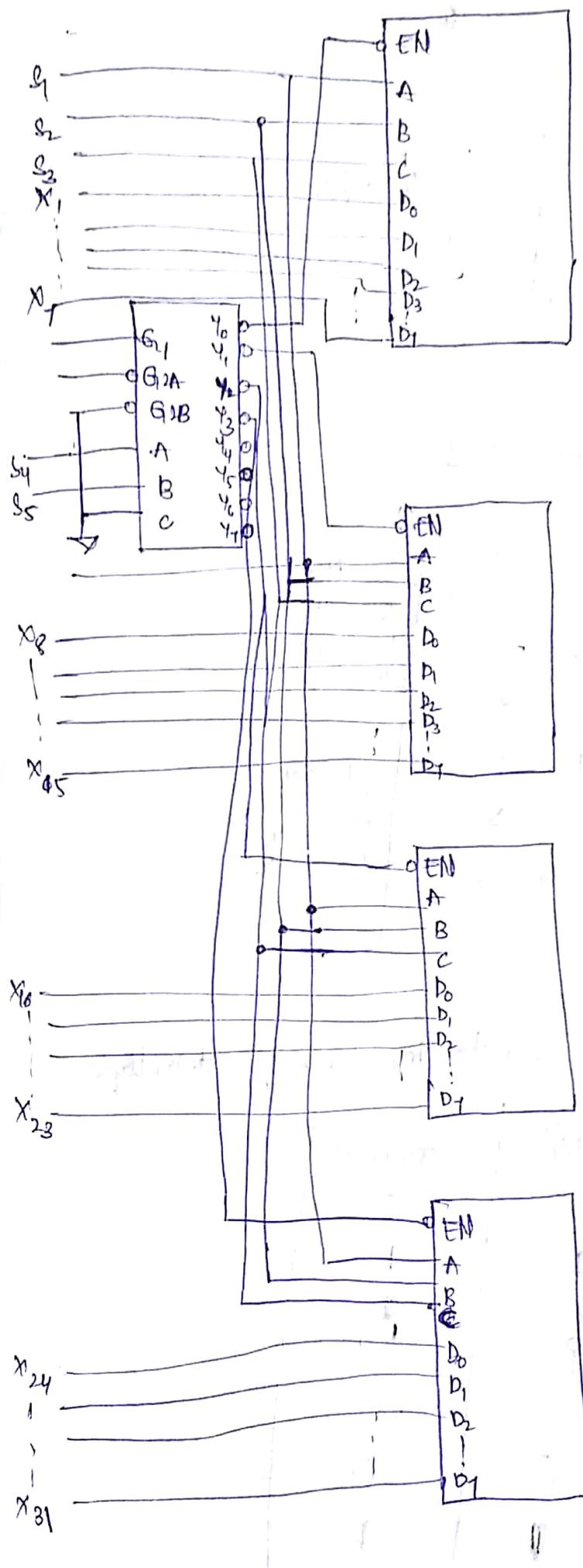
S	1D ₀	2D ₀	3D ₀	4D ₀
0	1D ₀	2D ₀	3D ₀	4D ₀
1	1D ₁	2D ₁	3D ₁	4D ₁

② Design 16x1 MUX using 2x74151

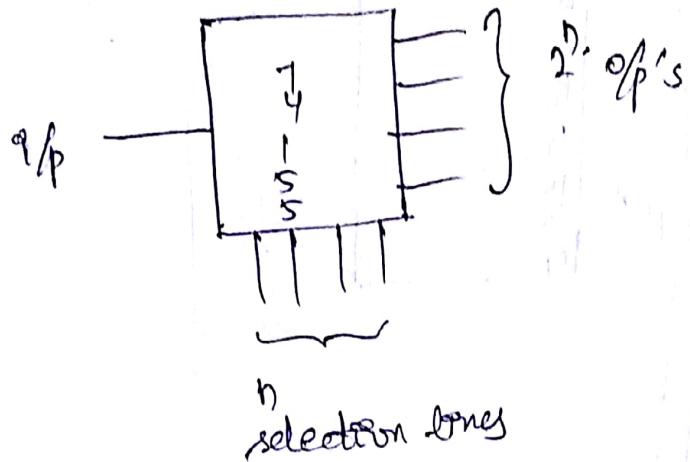
Sol: 16x1 MUX using 8x1 MUX
 ↓
 4 select ; ↓
 ; 3 select



② Design a 32x1 RAM using 74181 & 74188
 ⚡ select
 $(8 \times 1 \text{ RAM})$ \downarrow $(3 \times 8 \text{ decoded})$
 ⚡ select



DEMUX: (DE74155) - (DE74155)



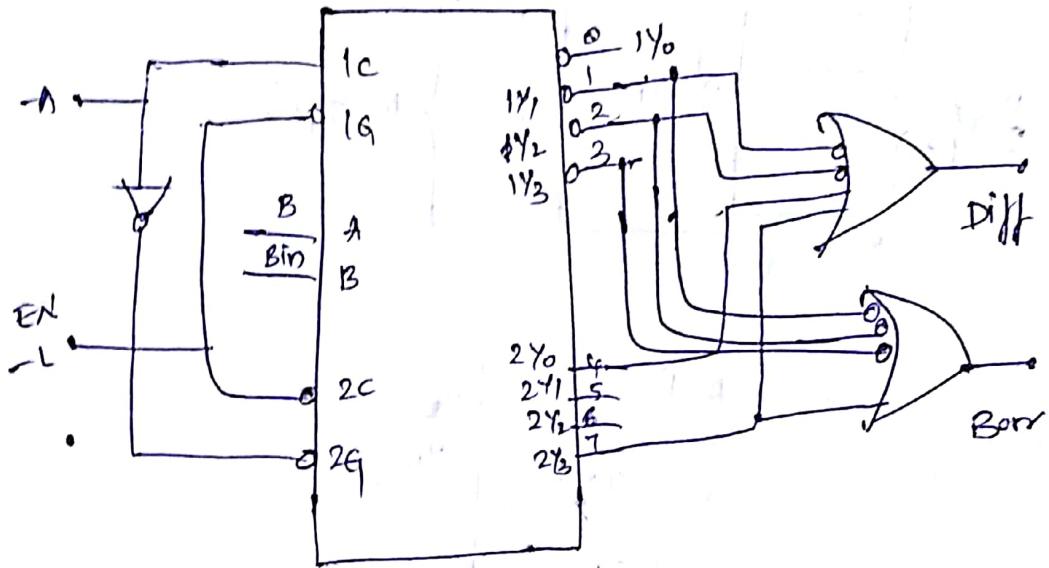
1		1c			7	$^{14}_0$
2	0	1G	7		6	$^{14}_1$
13		A	4		5	$^{14}_2$
3		B	1		4	$^{14}_3$
15	0	2C	5		9	$^{24}_0$
		2G	5		10	$^{24}_1$
					M	$^{24}_2$
					12	$^{24}_3$

Design a full subtractor using demultiplexer

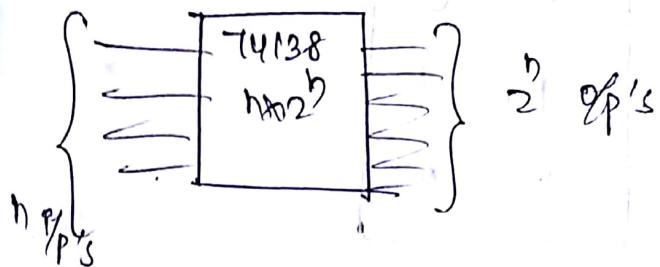
A	B	C	diff	borrow
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
1	0	0	0	0
1	1	0	0	0
1	1	1	0	1

$$diff = \neg A \oplus BC \oplus C$$

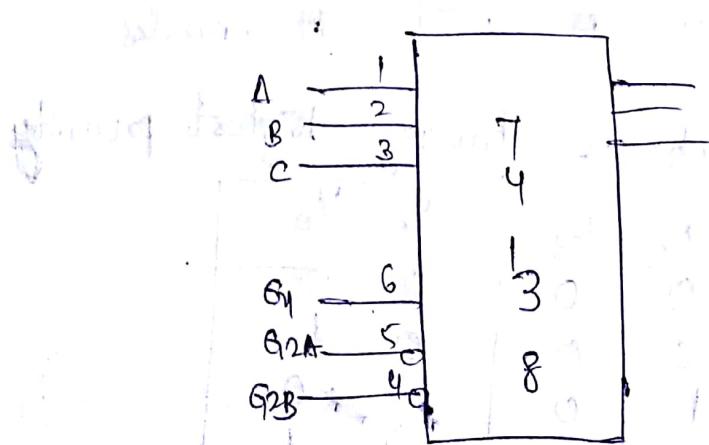
$$\text{borrow} = \neg \bar{A}B + \bar{B}C + AC$$



Decoder

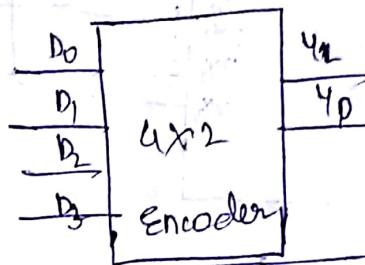
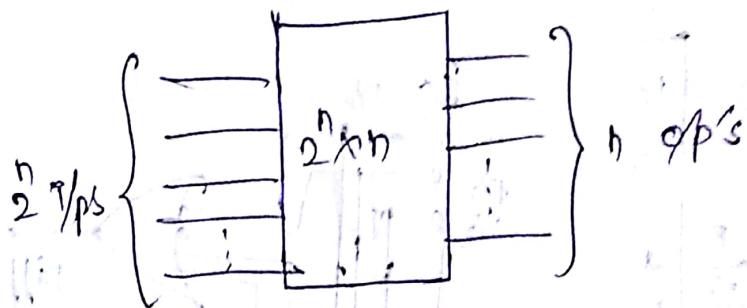


Design a 4x16 decoder using 3x8 decoders.



13/10/17

Encoder

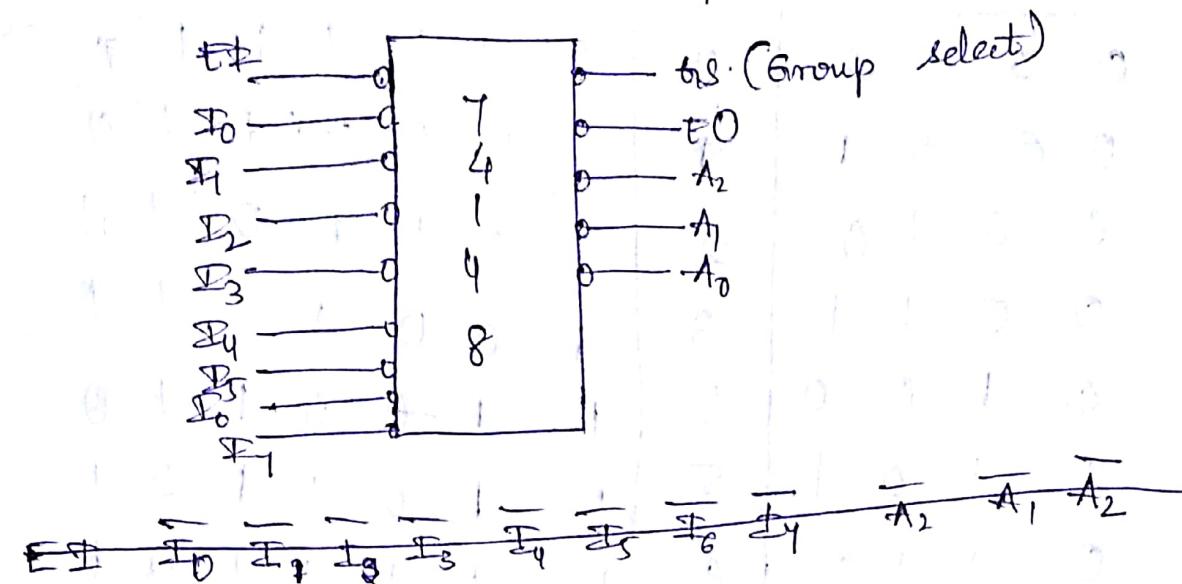


D_0	D_1	D_2	D_3	Y_1	Y_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1
0	0	0	0	x	x

Priority encoder: If more than 1 I/p is high, priority encoder is used. It encodes the I/p which is having highest priority.

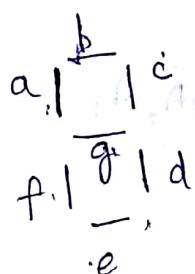
E	I_0	I_1	I_2	I_3	Y_1	Y_0
0	1	0	0	0	0	0
0	x	1	0	0	0	1
0	x	x	1	0	1	0
0	x	x	x	1	1	1

74148 is used as priority encoder.



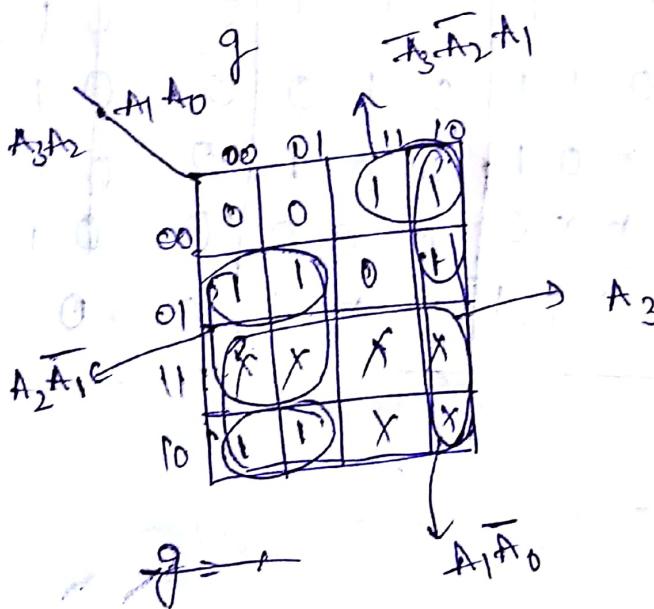
E_1	\overline{D}_0	\overline{D}_1	\overline{D}_2	\overline{D}_3	\overline{D}_4	\overline{D}_5	\overline{A}_2	\overline{A}_1	\overline{A}_0	GS	EO
0	0	1	1	1	1	1	1	1	1	1	01
0	x	0	0	0	0	0	1	1	0	0	01
0	x	x	0	1	1	1	1	0	1	0	01
0	x	x	x	0	1	1	1	0	0	0	01
0	x	x	x	x	0	1	0	1	1	0	01
0	x	x	x	x	x	0	0	1	1	0	01
0	x	x	x	x	x	x	0	1	0	0	01
0	1	1	1	1	1	1	x	x	0	0	0

7-segment display:



A_3	A_2	A_1	A_0	Decimal	f	f	e	d	c	b	a
0	0	0	0	0	0	1	1	1	1	1	r
0	0	0	1	1	0	0	0	0	1	1	0
0	0	1	0	2	1	0	1	1	0	1	1
0	0	1	1	3	1	0	0	1	1	1	1
0	1	0	0	4	1	1	0	0	1	1	0
0	1	0	1	5	1	1	0	1	1	0	1
0	1	1	0	6	1	1	1	0	1	0	1
0	1	1	1	7	0	0	0	0	1	1	1
1	0	0	0	8	1	1	1	1	1	1	1
1	0	0	1	9	1	1	0	1	1	1	1

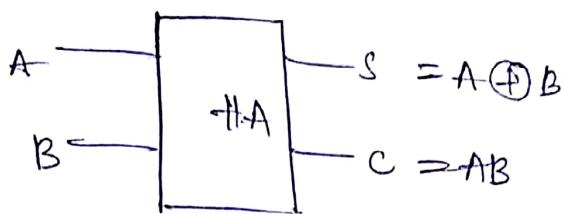
B-map



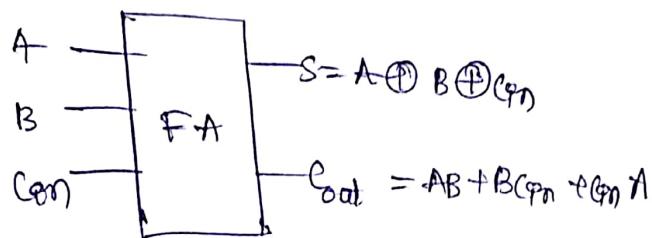
$$f = A_1 \bar{A}_0 + A_2 \bar{A}_1 + A_3 + \bar{A}_3 \bar{A}_2 A_1$$

Adder:

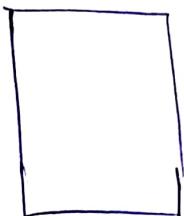
Half adder



Full adder



Subtractor:



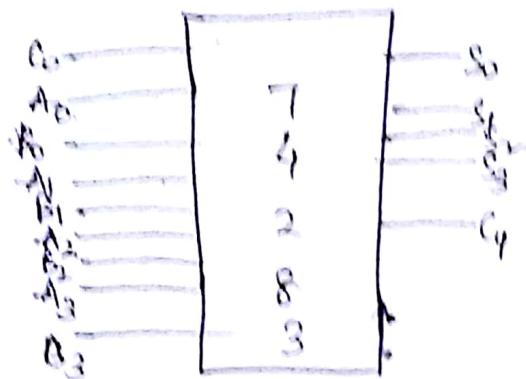
Method of subtraction by addition of two's complement

Method of subtraction by borrowing and adding

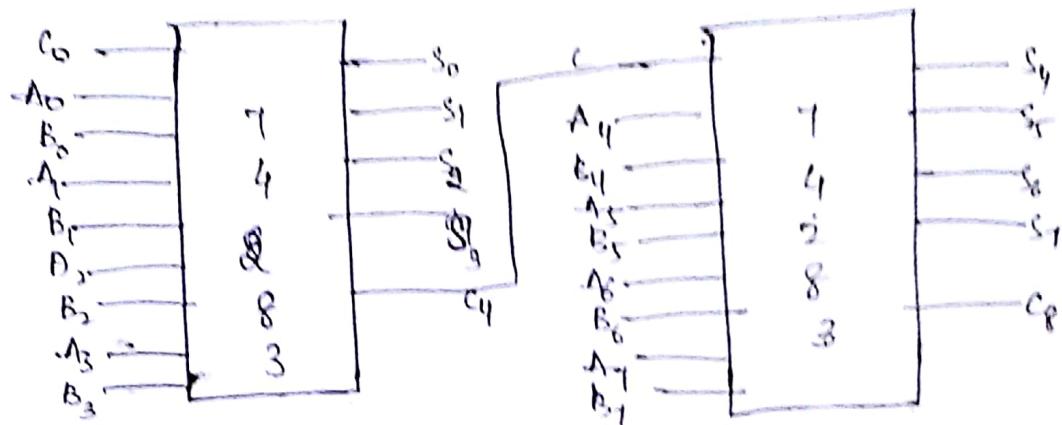


The ~~IC~~ 74283 is used to perform parallel adder to perform 4 bit addition.

4-bit Parallel Adder:



Design a 8-bit adder:



Comparator:

Design a 2-bit comparator:

