8/8/18

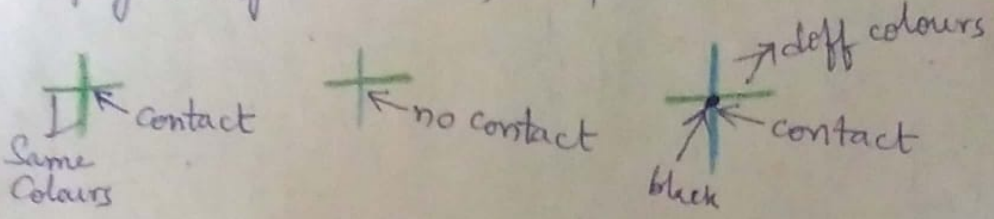
UNIT - 3

Metal layer – blue (power supply, i/p & o/p lines)

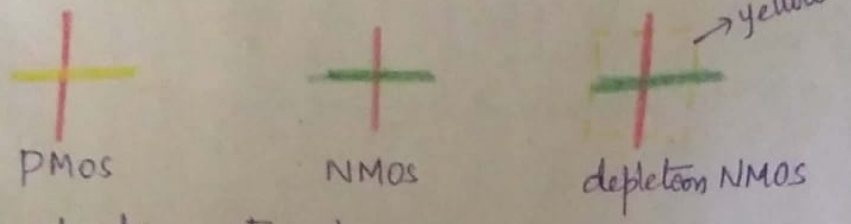
p-diffusion layer - yellow

n-diffusion layer – green

polysilicon (gate connection) - red



→ If diffusion crosses polysi, it is a transistor.



Steps to draw stick diagram:

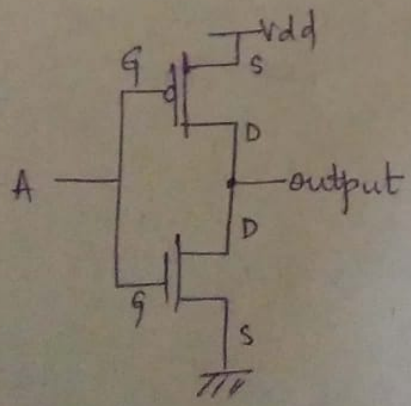
1) Draw power supply lines (in blue)

2) Draw demarkation line with brown colour

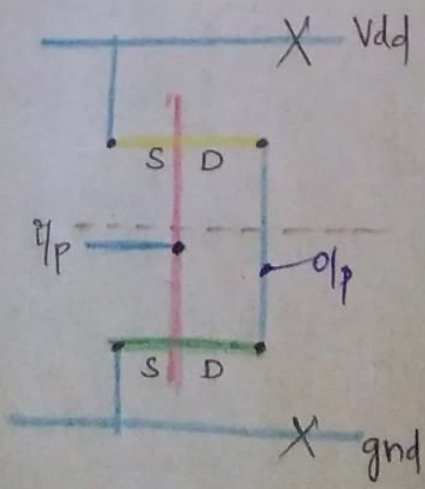
3) X for power supply connection (well contact & substrate contact)

CMOS Inverter:

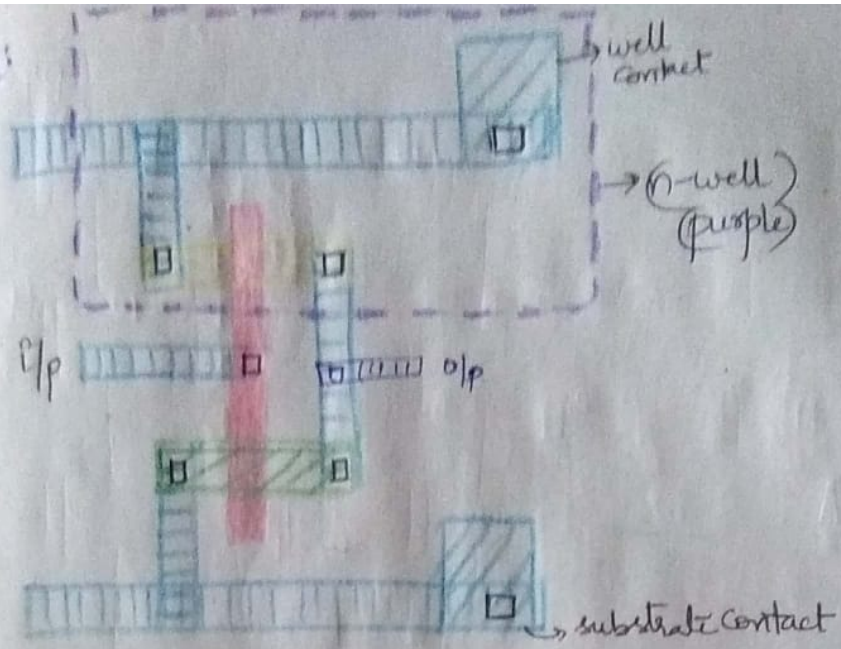
Schematic:



Stick Diagram:

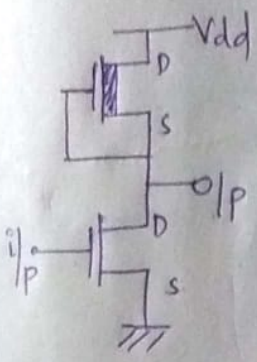


Layout:

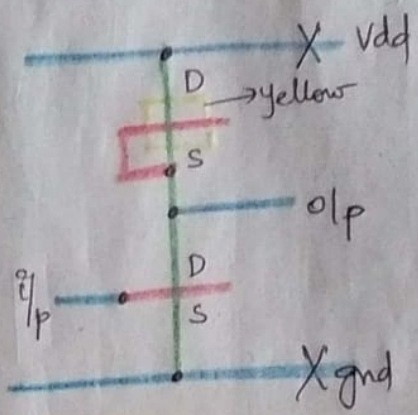


NMOS Inverter:

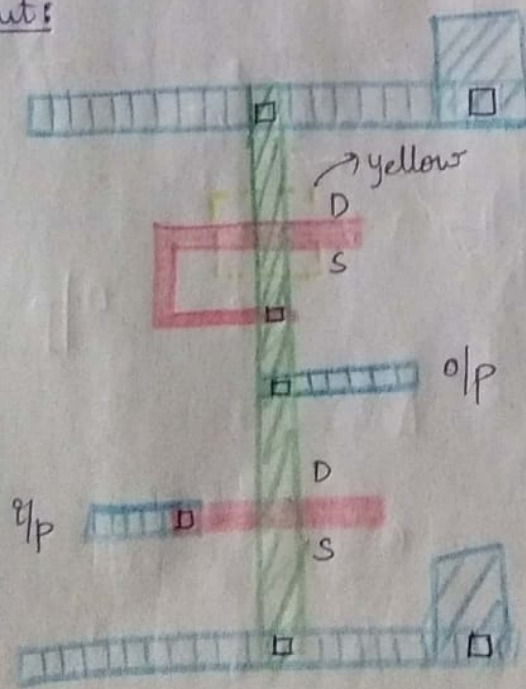
Schematic:



Stick Diagram:



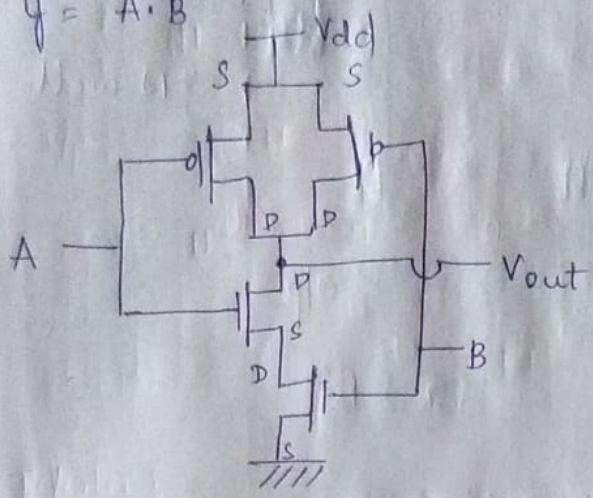
Layout:



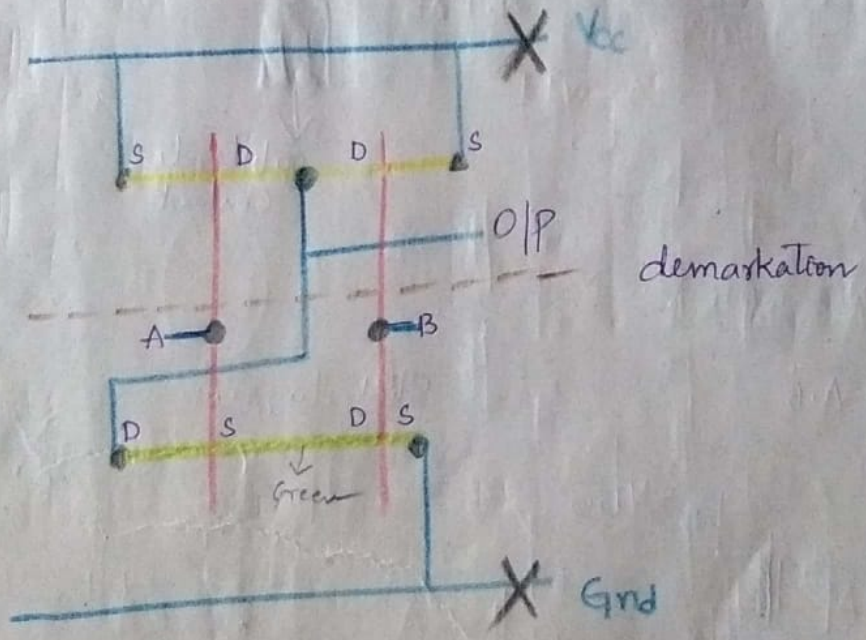
9/8/18

CMOS NAND GATE :

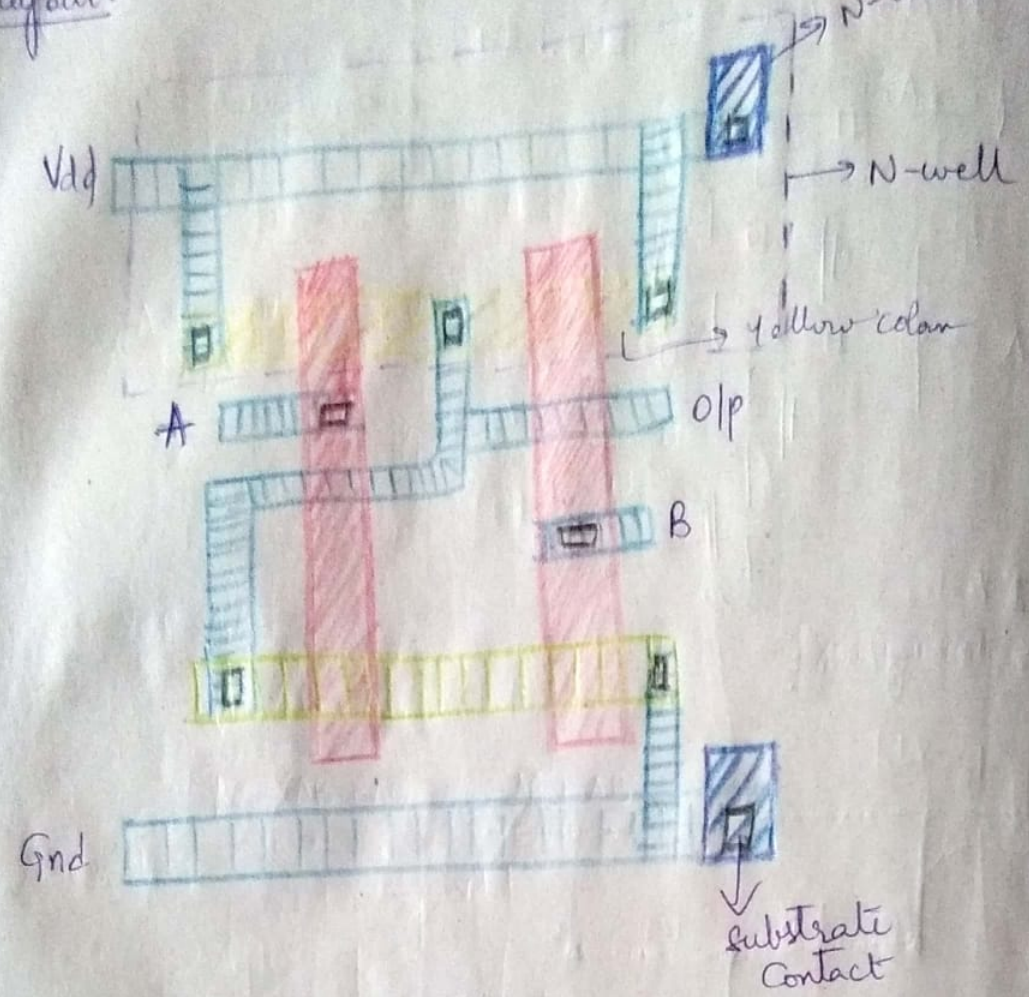
$Y = \overline{A \cdot B}$



Stick Diagram:

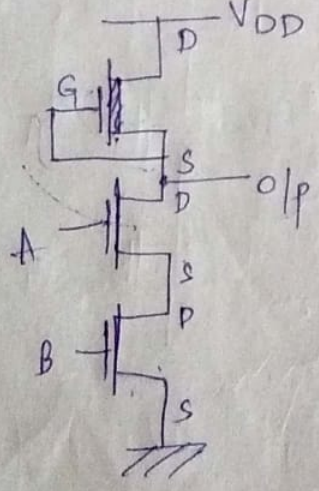


Layout:

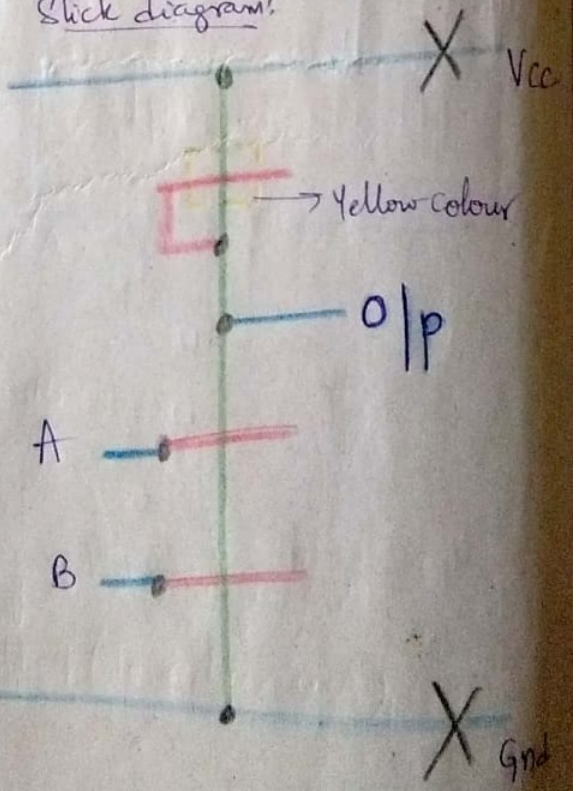


NMOS NAND GATE:

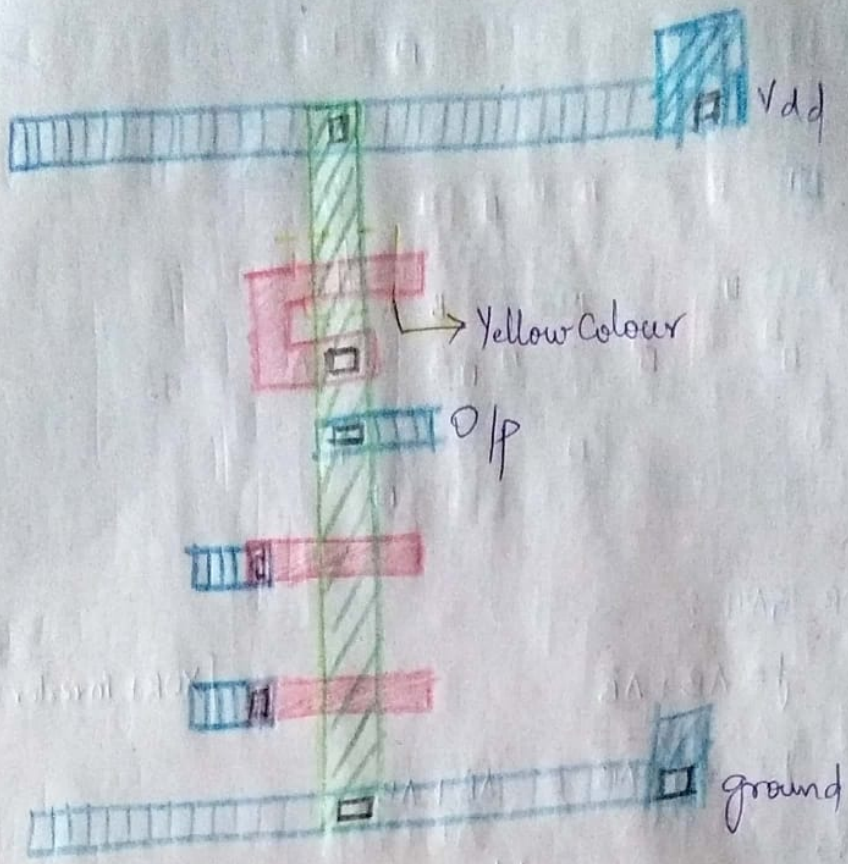
$y = \overline{A \cdot B}$



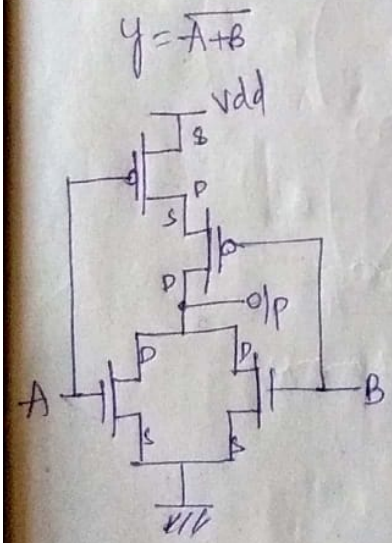
Stick diagram:



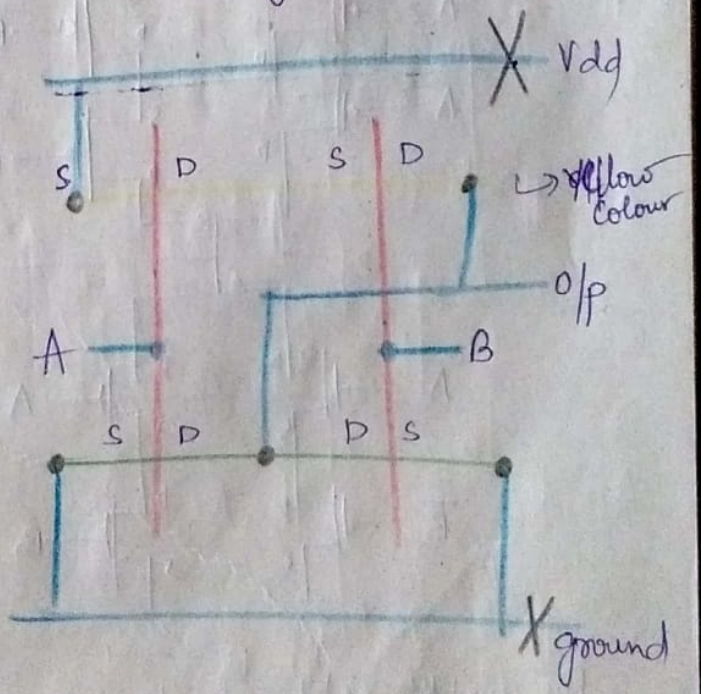
Layout:



CMOS NOR gate:

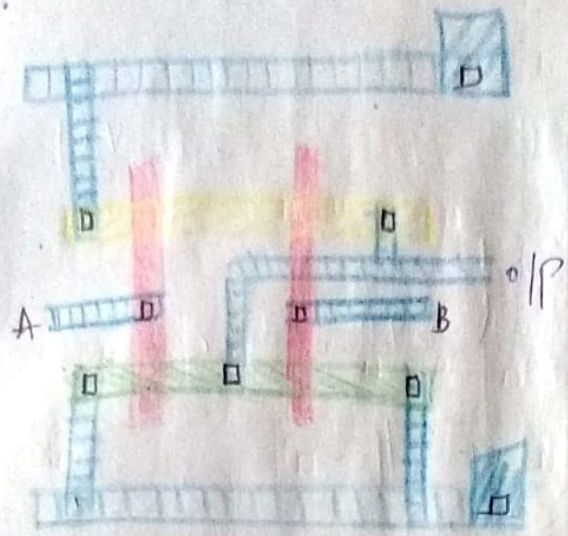


Stick Diagram:



red – polysilicon
green – N-MOS
yellow – P-MOS
blue – metal
black – contact cut

Layout:



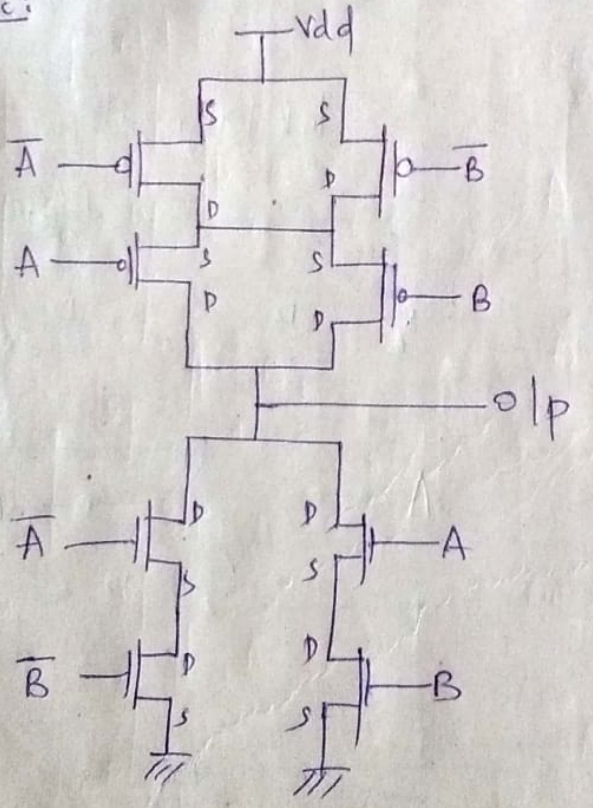
CMOS XOR GATE:

XOR + inverter = XNOR

$$Y = \bar{A}B + A\bar{B}$$

$$\bar{Y} = \overline{\bar{A}B + A\bar{B}} = \overline{\bar{A}\bar{B} + AB}$$

Schematic:



For complete ckts, for drawing stick diagram, we follow Euler's path method (to reduce area)

→ In Euler's method,

each transistor is a branch

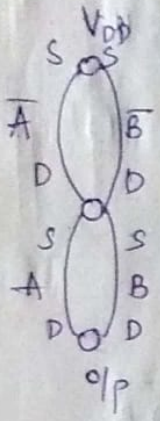
each connection is a node.

→ We need to choose a path such that (there are no repeated loops, branchs)

→ Both PMOS & NMOS should have same path.

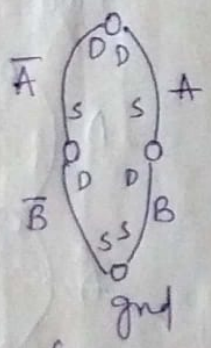
Euler's path :

For PMOS



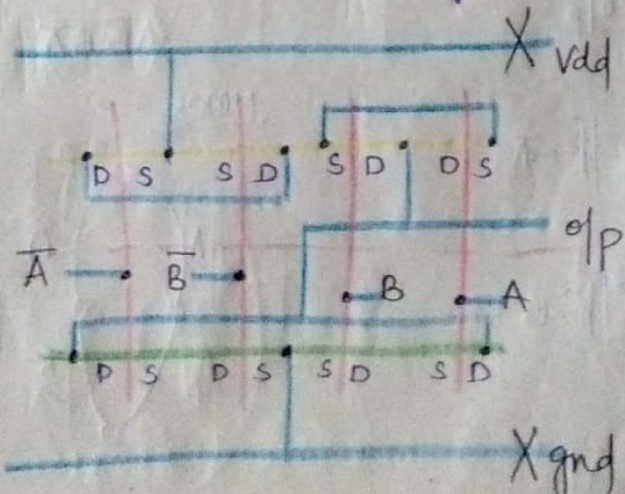
$\overline{A}\,\overline{B}BA$

For NMOS

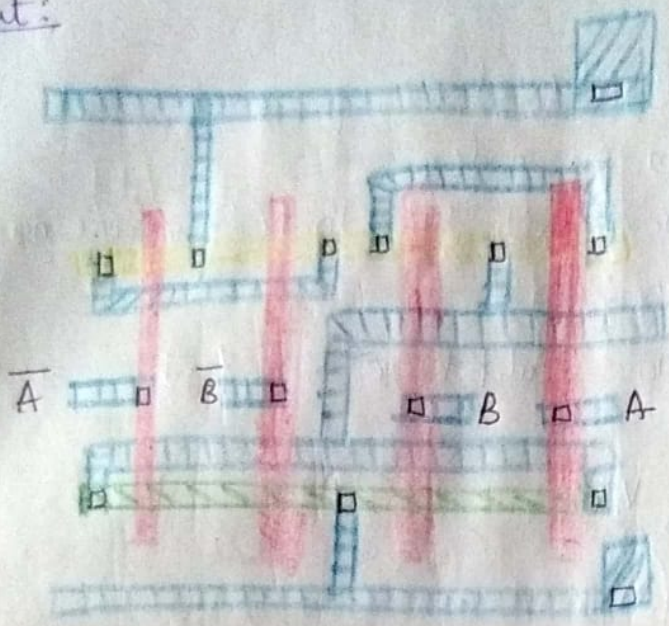


$\overline{A}\,\overline{B}BA$

Stick Diagram : (Draw according to path)



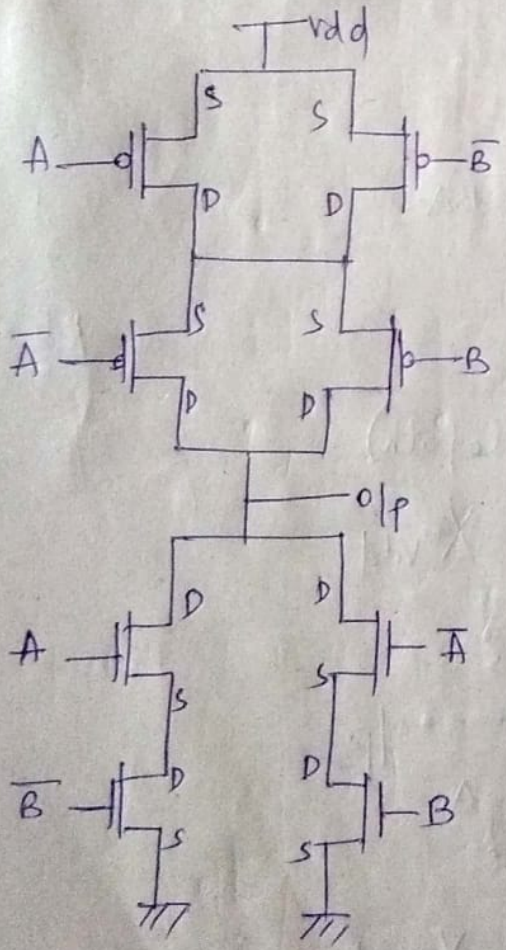
Layout:



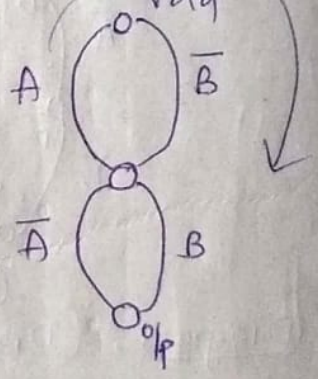
CMOS XNOR gate:

$$y = \bar{A}\bar{B} + AB$$

$$y = \overline{\bar{A}\bar{B} + AB} = \overline{A\bar{B} + \bar{A}B}$$

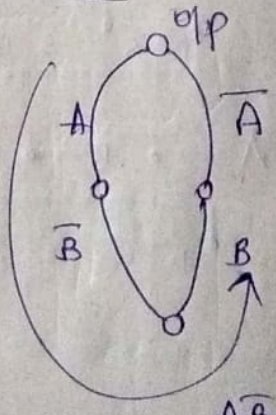


PMOS



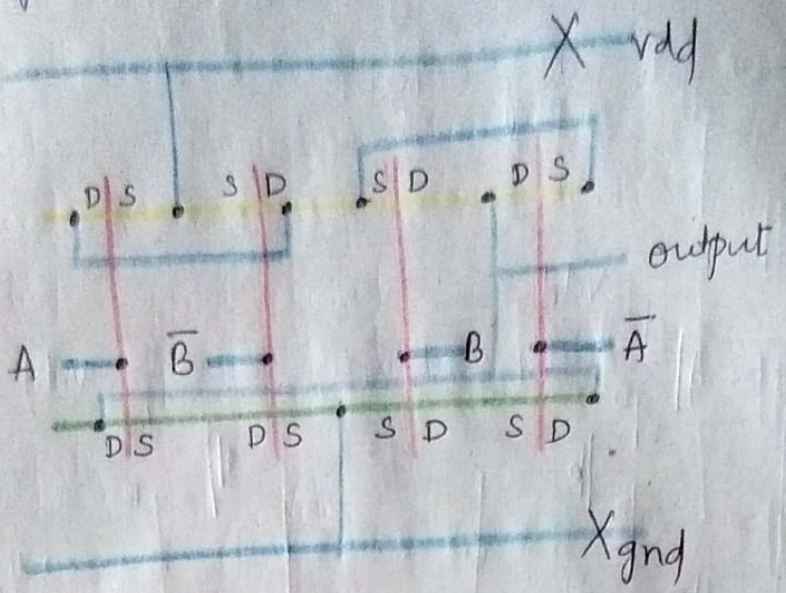
$A\bar{B}\,B\bar{A}$

NMOS



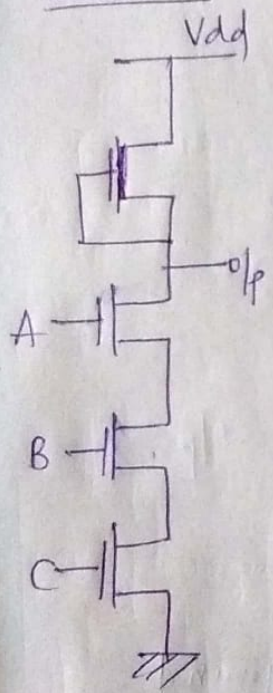
$A\bar{B}\,B\,A$

Stick Diagram:

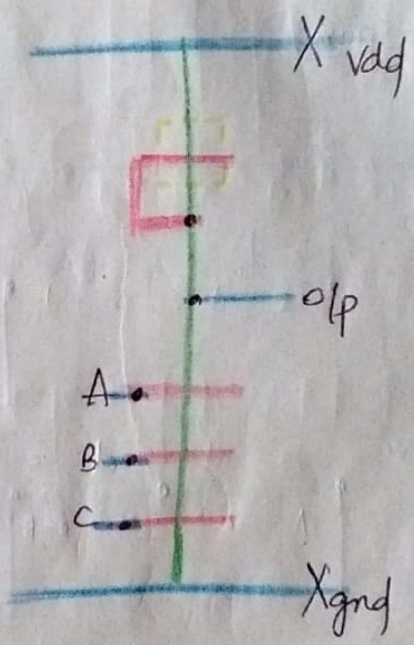


3-input NAND gate using NMOS design style:

Schematic:



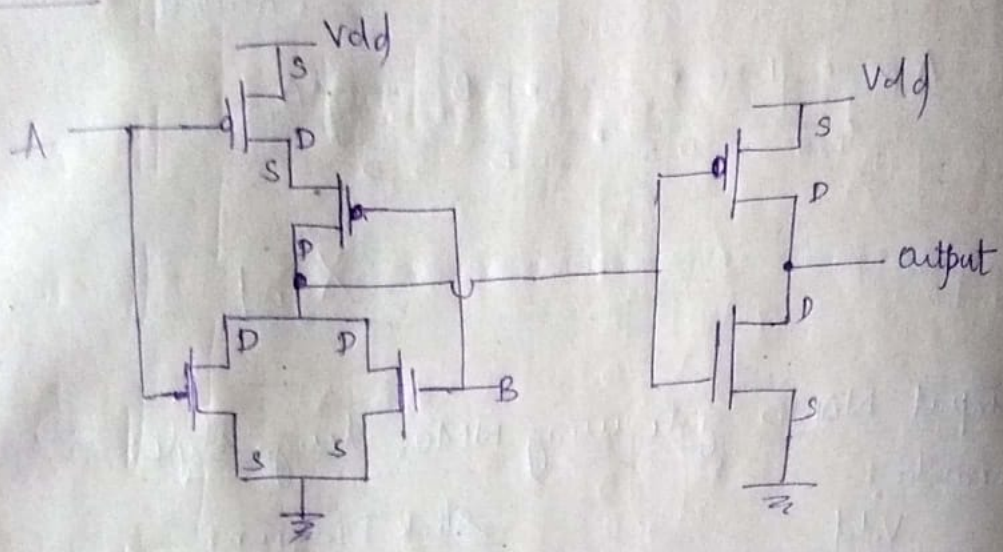
Stick Diagram:



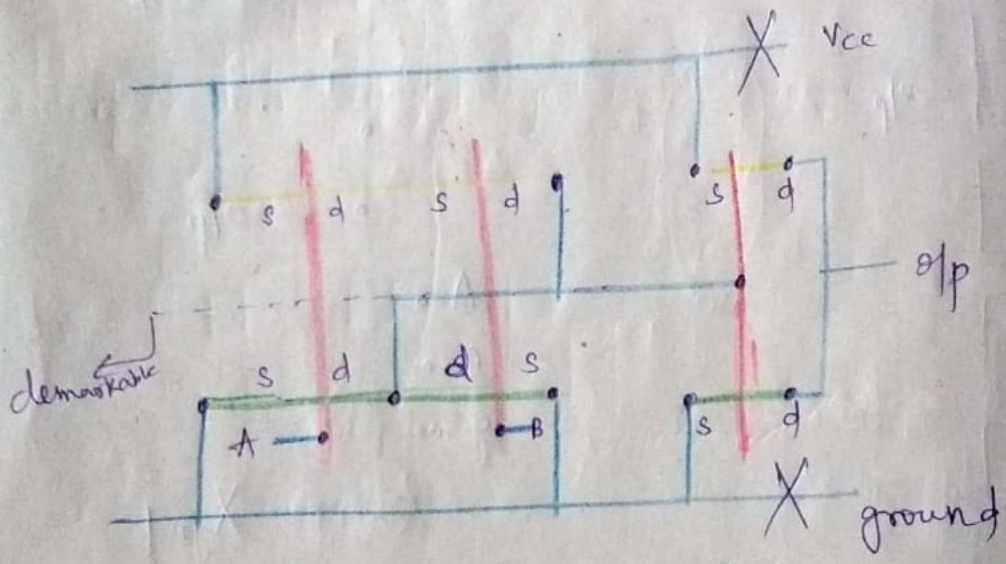
18/8/18

2-Input OR gate using Cmos:

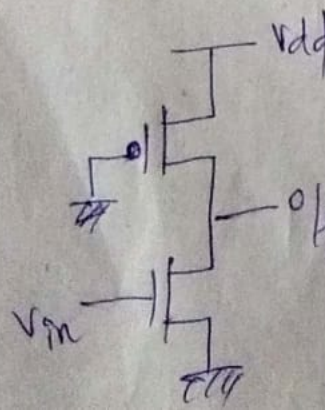
Schematic:

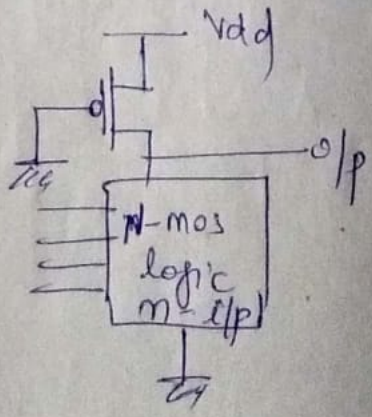


Stick Diagram:

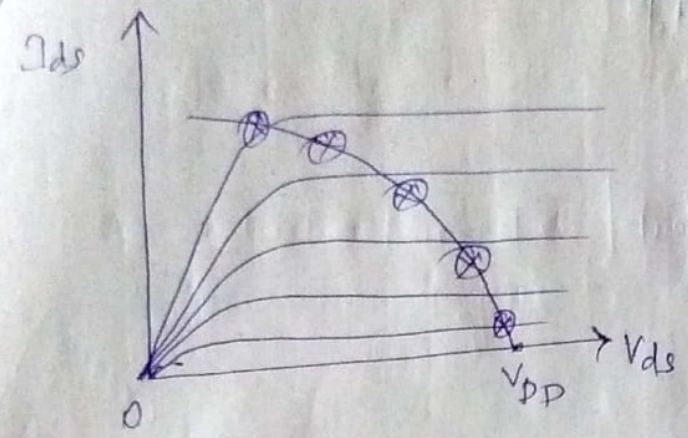


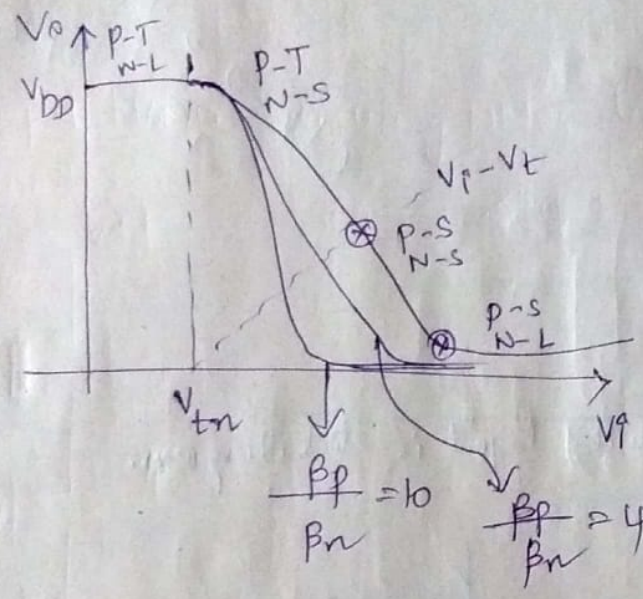
Pseudo N-MOS logic:



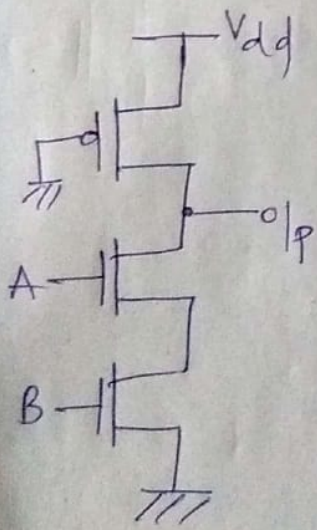


In order to overcome delay & area we use pseudo-NMOS logic. There will be static power dissipation.





Pseudo logic - NAND gate:



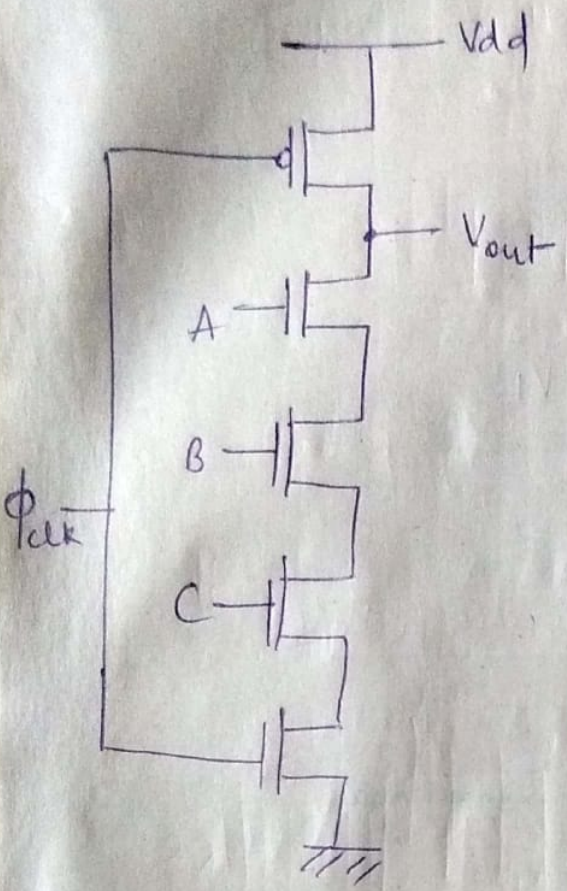
Pseudo NMOS logic

→ no. of transistors / area ↓

→ gate capacitance ↓

→ delay ↓

Q) Implement 3 input NAND gate using dynamic CMOS logic



CLK=0 → pre charge phase
=1 → evaluation phase

→ Interface b/w circuit & layout is stick diagram.