

Q.4 MOS Transistor figure of merit ω_0

frequency response may be obtained from the parameter $\omega_0 = \frac{g_m}{C_g} = \frac{\mu}{L^2} (V_{gs} - V_t) = \frac{1}{T_{sd}}$

T_{sd} = transit time

Switching speed depends on gate voltage above threshold and on carrier mobility and inversely as the square of channel length.

normally electron mobility μ_n is larger than that 3 times as hole mobility.

$$\mu_n = 650 \text{ cm}^2/\text{V sec}$$

$$\mu_p = 240 \text{ cm}^2/\text{V sec}$$

but bulk mobilities

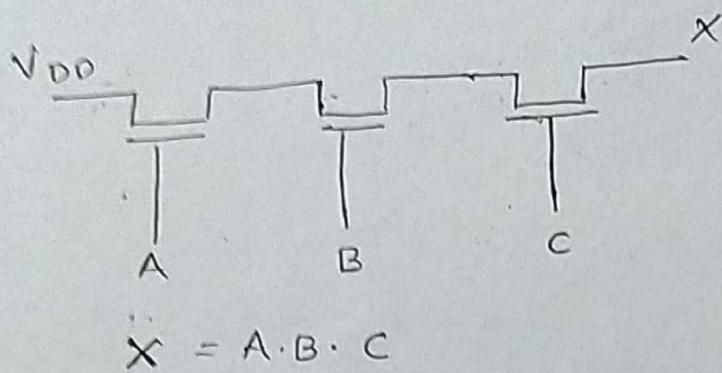
$$\mu_n = 1250 \text{ cm}^2/\text{V sec}$$

$$\mu_p = 480 \text{ cm}^2/\text{V sec}$$

$$\frac{\mu_s}{\mu} = 0.5 \quad (\mu_s = \text{surface mobility})$$

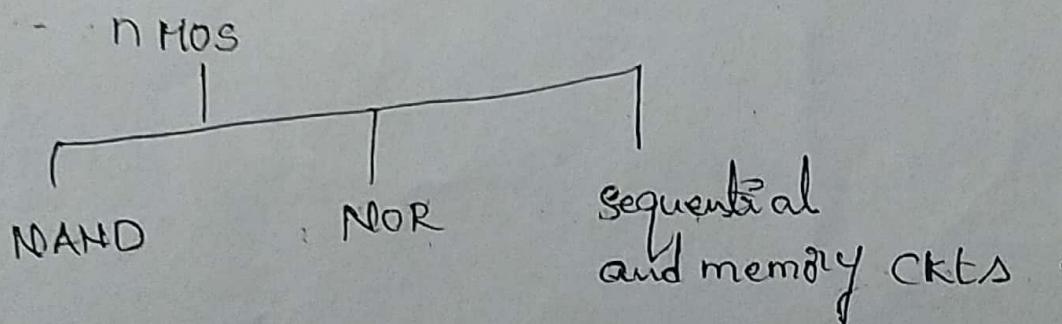
$\mu = \text{bulk mobility}$

2.5 The pass transistor



These mos transistors to be used as switches in series with lines carrying logic levels. This application of the MOS device is called the pass transistor.

2.6 The nMOS inverter

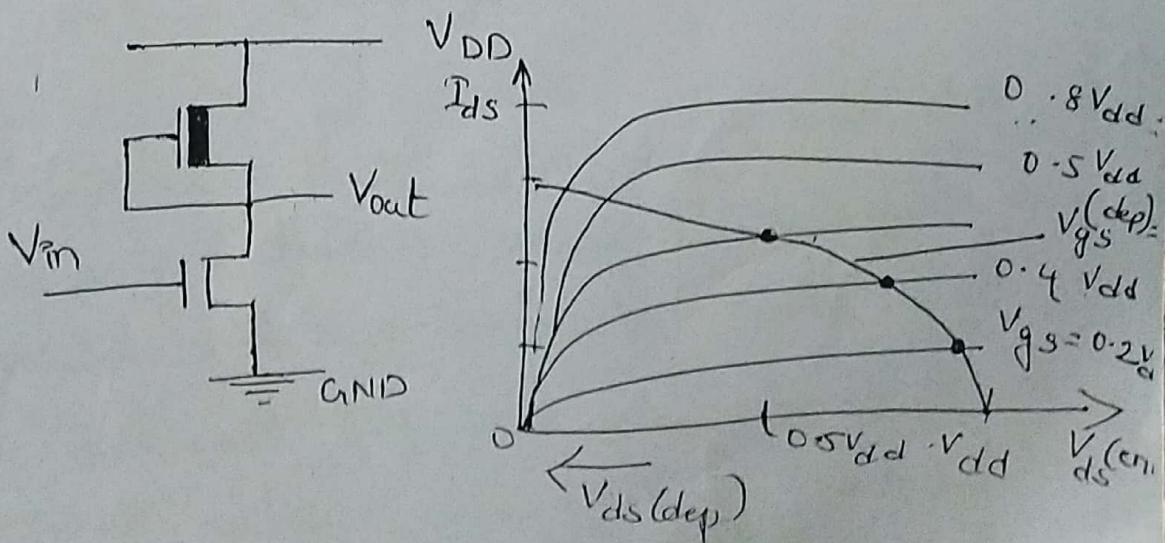


The basic inverter ckt requires a transistor with source connected to ground and a load resistor connected from the drain to the positive supply rail V_{DD}. The output is taken from the drain and the ip applied b/w gate and ground.

Normally every transistor is having internal

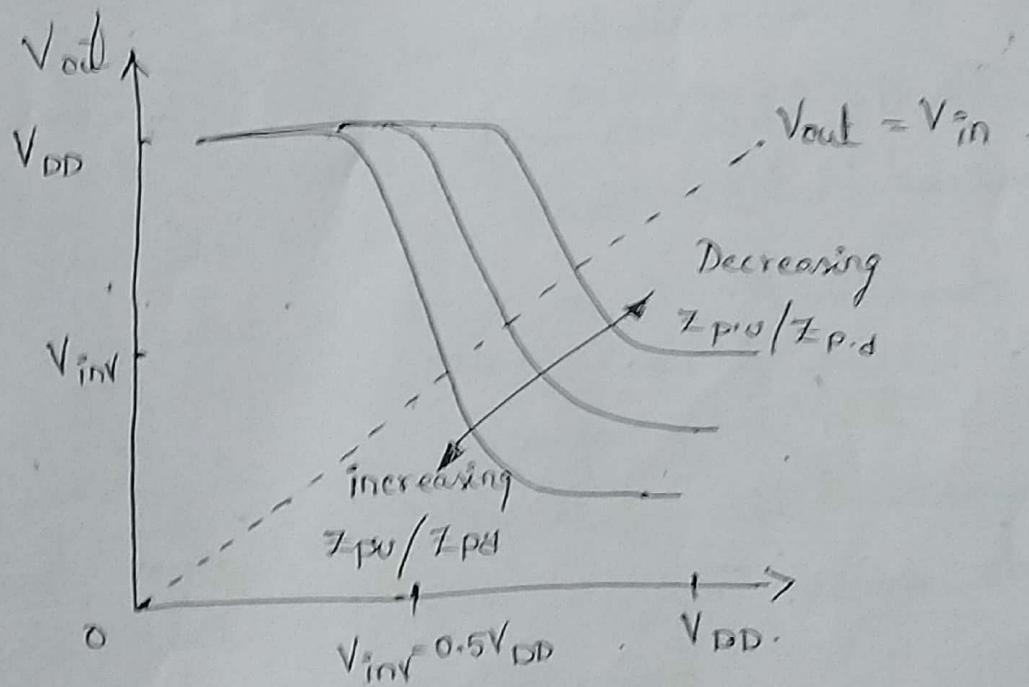
parasitic resistance and capacitances. So if we take PMOS which is larger than the NMOS by 3 times so obviously the internal parasitic resistors are occupy more area. So to overcome this problem depletion mode transistors as the load then

- 1) With no current drawn from the op, the currents I_{ds} for both transistors must be equal.
- 2) For the depletion mode transistor, the gate is connected to the source so it is always on and only the characteristic curve $V_{gs} = 0$ is relevant.
- 3) In this configuration the depletion mode device is called the pull-up (P.U) and the enhancement mode device the pull-down (P.D) transistor.



4) To obtain the Inverter transfer characteristic we superimpose the $V_{GS} = 0$ depletion mode characteristic curve on the family of curves for the enhancement mode device, we will note the voltage across the enhancement mode device corresponds to minimum voltage across the depletion mode transistors.

5) The points of intersection of curves give points on the transfer characteristic.



6) Note that as V_{in} ($= V_{GS}$ P.d. transistors) exceeds the P.d. threshold voltage current begins to flow. The output voltage thus decreases and the subsequent increase in V_{in} will cause the P.d. transistor to come out of saturation and become resistive. The P.u. transistor is

Initially resistive as the P.d transistor turns on.

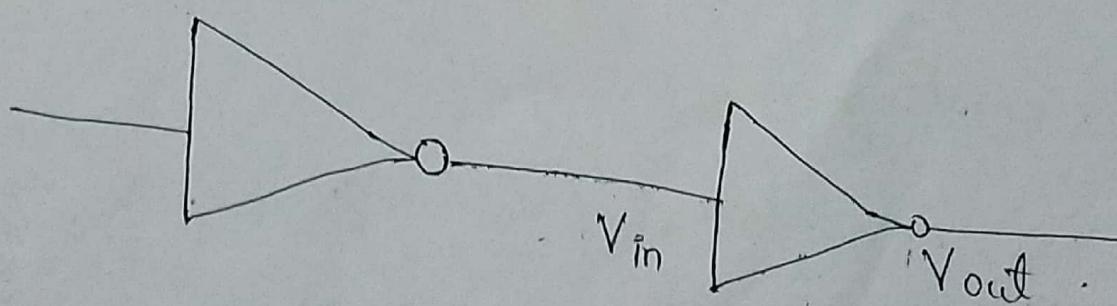
7) During transition, the slope of the transfer characteristic determines the gain.

$$\text{Gain} = \frac{\delta V_{\text{out}}}{\delta V_{\text{in}}}$$

8) The point at which $V_{\text{out}} = V_{\text{in}}$ is denoted as V_{inv} and it will be noted that the transfer characteristic and V_{inv} can be shifted by variation of the ratio of pull-up to pull-down resistances.

$Z_{\text{p.u}}/Z_{\text{p.d}}$ Z is the ratio of w, L .

2.7) Determination of Pull-up to pull-down ratio ($Z_{\text{p.u}}/Z_{\text{p.d}}$) for an nMOS inverter driven by another



Consider the depletion mode transistor for which $V_{gs} = 0$ under all conditions, and assume that

in order to cascade inverters with out degradation of levels we are aiming to meet the requirement

$$V_{in} = V_{out} = V_{inv}$$

for equal margins around the inverter threshold, we set $V_{inv} = 0.5V_{DD}$. At this point both transistors are in saturation

$$I_{ds} = k \frac{\omega}{L} \left(\frac{(V_{gs} - V_t)^2}{2} \right)$$

in depletion mode

$$\begin{aligned} I_{ds} &= k \frac{\omega}{L} \left(\frac{(-V_t)^2}{2} \right) \quad \because V_{gs} = 0 \\ &= k \frac{\omega_{p.u}}{L_{p.u}} \left(\frac{V_{td}^2}{2} \right) \quad -(1) \end{aligned}$$

in enhancement mode

$$I_{ds} = k \frac{\omega_{p.d}}{L_{p.d}} \left(\frac{V_{inv} - V_t}{2} \right)^2 \quad , \because V_{gs} = V_{inv} \quad -(2)$$

equating (1), (2)

$$k \frac{\omega_{p.u}}{L_{p.u}} \left(\frac{V_{td}^2}{2} \right) = k \frac{\omega_{p.d}}{L_{p.d}} \left(\frac{V_{inv} - V_t}{2} \right)^2$$

$$Z_{p.d} = \frac{L_{p.d}}{\omega_{p.d}} ; \quad Z_{p.u} = \frac{L_{p.u}}{\omega_{p.u}}$$

$$\frac{1}{Z_{p.d}} \left(\frac{V_{td}^2}{2} \right) = \frac{1}{Z_{p.u}} \left(\frac{(V_{inv} - V_t)^2}{2} \right)$$

$$\frac{Z_{p.u}}{Z_{p.d}} = \frac{(V_{inv} - V_t)^2}{V_{td}^2}$$

$$\frac{V_{inv} - V_t}{V_{td}} = \sqrt{\frac{Z_{p.u}}{Z_{p.d}}} \quad \left\{ \begin{array}{l} \frac{V_{td}}{V_{inv} - V_t} = \sqrt{\frac{Z_{p.d}}{Z_{p.u}}} \\ V_{td} = (V_{inv} - V_t) \cdot \sqrt{\frac{Z_{p.d}}{Z_{p.u}}} \end{array} \right.$$

$$V_{inv} - V_t = \cancel{\frac{V_{td}}{Z_{p.d}}}$$

$$V_{td} \sqrt{\frac{Z_{p.u}}{Z_{p.d}}}$$

$$V_{inv} - V_t = V_{td} \sqrt{\frac{Z_{p.u}}{Z_{p.d}}}$$

$$V_{inv} = V_t + \frac{V_{td}}{\sqrt{\frac{Z_{p.d}}{Z_{p.u}}}}$$

$$= V_t + \frac{V_{td}}{\sqrt{\frac{Z_{p.d}}{Z_{p.u}}}}$$

$$V_t = 0.2 V_{DD}, \quad V_{td} = -0.6 V_{DD}$$

$$V_{inv} = 0.5 V_{DD}$$

$$0.5 V_{DD} = 0.2 + \frac{0.6}{\sqrt{\frac{Z_{p.u}}{Z_{p.d}}}}$$

$$0.5 - 0.2 = 0.6$$

$$\sqrt{\frac{Z_{p.u}}{Z_{p.d}}}$$

$$0.3 = \frac{0.6}{\sqrt{\frac{Z_{p.u}}{Z_{p.d}}}}$$

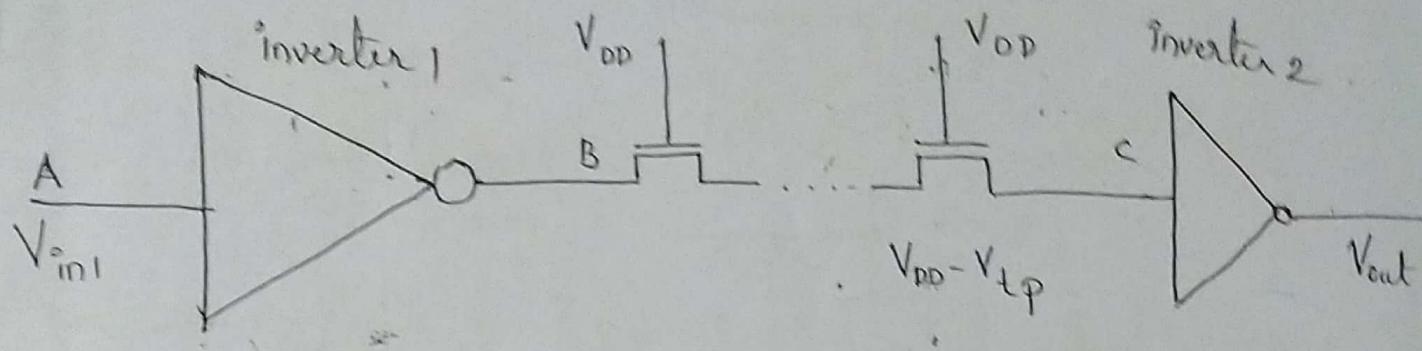
$$\sqrt{\frac{Z_{p.u}}{Z_{p.d}}} = 2$$

$$\frac{Z_{p.u}}{Z_{p.d}} = 4/1$$

2.8 Pull-up to pull-down ratio for an nMOS inverter driven through one or more pass transistors

The i/p to inverter 2 comes from the o/p of inverter 1 but passes through one or more pN MOS pass transistors used as switches

Connection of pass transistors in series will degrade the logic 1 level into inverter 2 so that the o/p will not be a proper logic 0 level.



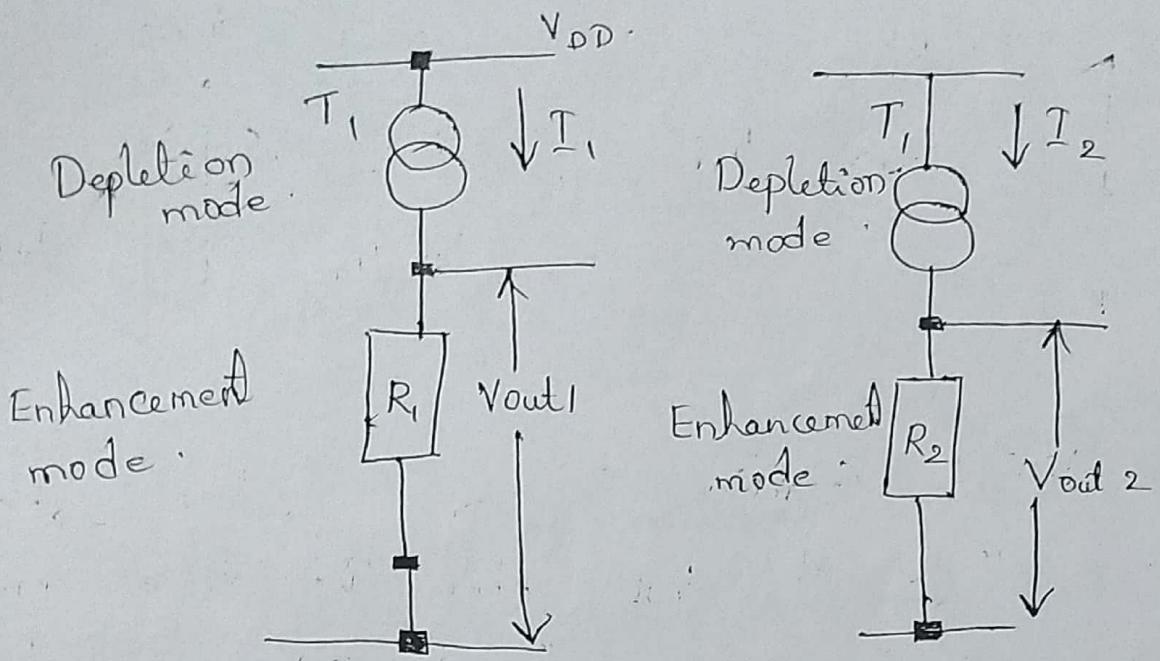
The Critical Condition is when point A is at 0V and B is thus at V_{DD} , but the Voltage into inverter 2 at point C is now reduced from V_{DD} by the threshold voltage of the series pass transistor.

with all pass transistor gates connected to V_{DD} there is a loss of V_{tp} , however many are connected in series. Since no static current flows through them and there can be no voltage drop in the channels. Therefore the i/p voltage at inverter 2 is

$$V_{in2} = V_{DD} - V_{tp}$$

where V_{tp} = threshold voltage of pass transistor.

Consider inverter 1 with input at V_{DD} then the p-d transistors with a low voltage across it. So it is in saturation. The p-n transistors T_1 and T_2 is conducting but region represented by R , is in resistive



For the P. d. transistors

$$I_{ds} = K \frac{W_{P.d}}{L_{P.d}} \left((V_{DD} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

$$\therefore R_1 = \frac{V_{ds}}{I_1} = \frac{1}{K} \frac{L_{P.d}}{W_{P.d}} \left(\frac{1}{V_{DD} - V_T - \frac{V_{ds}}{2}} \right)$$

Note that V_{ds} is small and $\frac{V_{ds}}{2}$ can be ignored.

$$R_1 = \frac{1}{K} \frac{L_{P.d}}{W_{P.d}} \left(\frac{1}{V_{DD} - V_T} \right)$$

Now, for depletion mode P. n in saturation with $V_{gs} = 0$

$$I_1 = I_{ds} = K \frac{W_{P.a.}}{L_n} \left(\frac{-V_{td}}{2} \right)^2$$

The product

$$I_1 R_1 = V_{out,1}$$

$$V_{out,1} = I_1 R_1 = \frac{Z_{p.d.1}}{Z_{p.u.1}} \left(\frac{1}{V_{DD} - V_t} \right) \left(\frac{V_{td}}{2} \right)^2$$

Consider inverter 2 when $i_P = V_{DD} - V_{tp}$.

$$R_2 = \frac{1}{K} Z_{p.d.2} \frac{1}{(V_{DD} - V_{tp}) - V_t}$$

$$I_2 = K \cdot \frac{1}{Z_{p.u.2}} \frac{\left(-V_{td} \right)^2}{2}$$

$$V_{out,2} = I_2 R_2 = \frac{Z_{p.d.2}}{Z_{p.u.2}} \left(\frac{1}{V_{DD} - V_{tp} - V_t} \right) \frac{V_t}{2}$$

$$I_1 R_1 = I_2 R_2$$

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} = \frac{Z_{p.u.1}}{Z_{p.d.1}} \frac{(V_{DD} - V_t)}{(V_{DD} - V_{tp} - V_t)}$$

Taking typical Values

$$V_t = 0.2 V_{DD}, \quad V_{tp} = 0.3 V_{DD}$$

$$\frac{Z_{P.U.2}}{Z_{P.D.2}} = \frac{Z_{P.U.1}}{Z_{P.D.1}} \cdot \frac{0.8}{0.5}$$

↳

$$\frac{Z_{P.U.2}}{Z_{P.D.2}} = 2 \frac{Z_{P.U.1}}{Z_{P.D.1}} = \frac{8}{1}$$

Summarizing for an nMOS inverter.

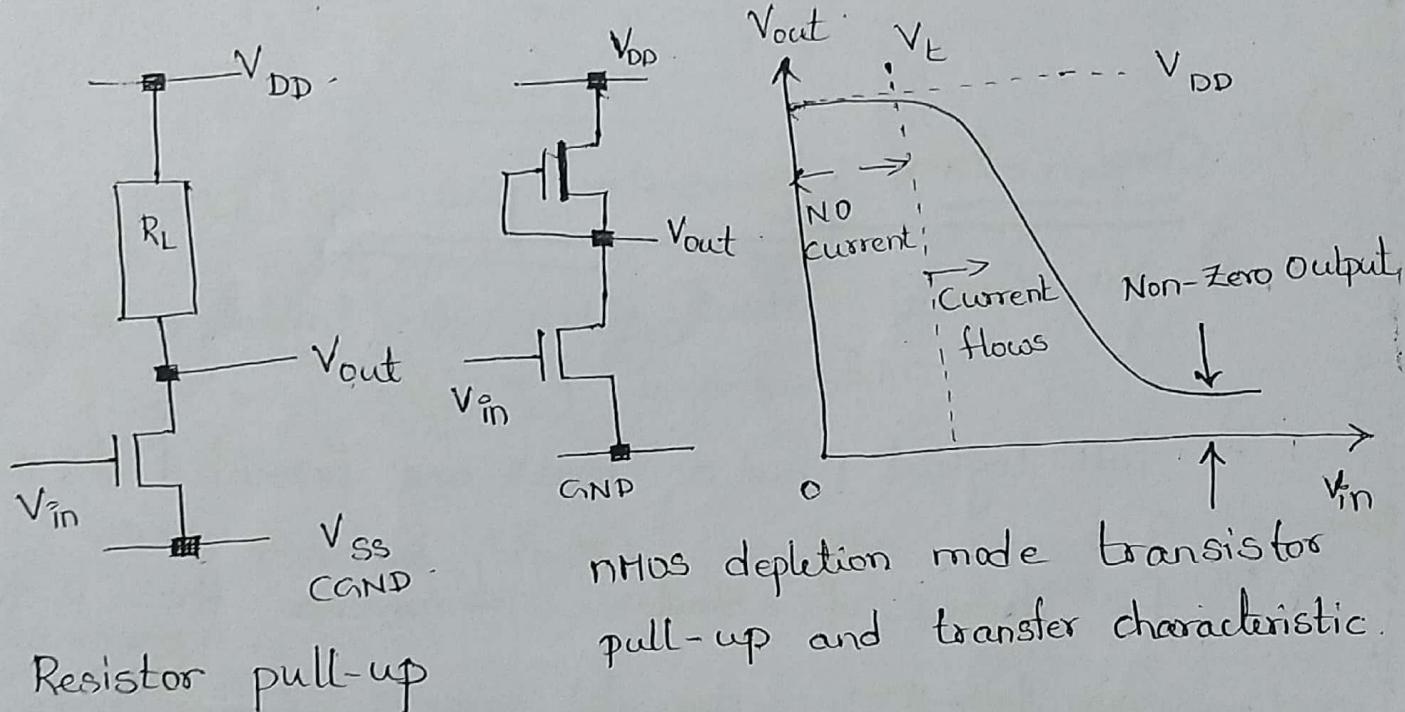
- An inverter driven directly from the o/p of another should have a $Z_{P.U.}/Z_{P.D.}$ ratio of $\geq 4/1$.
- An inverter driven through one or more pass transistors should have a $Z_{P.U.}/Z_{P.D.}$ ratio of $\geq 8/1$.

2.9 Alternative forms of pull-up

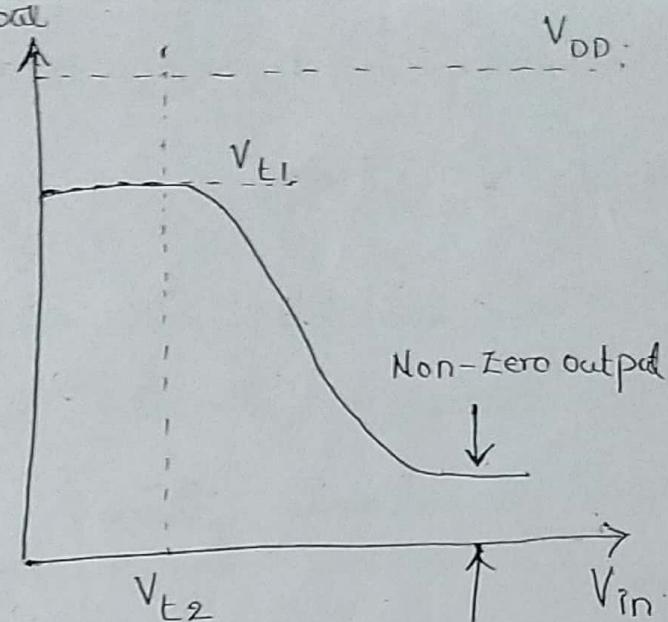
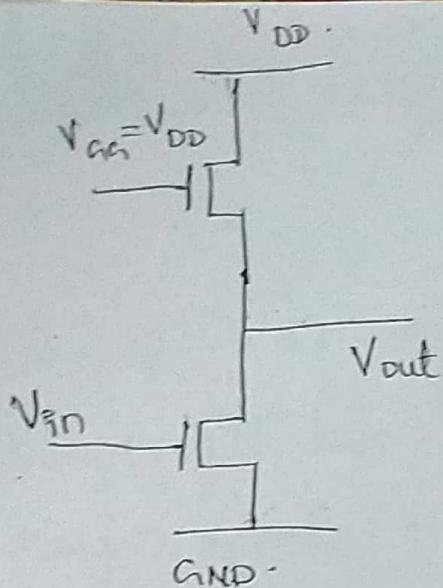
Up to now we have assumed that the inverter circuit has a depletion mode pull-up transistor as its load. There are at least four possible arrangements

- 1) Load Resistance R_L :- This arrangement is not often used because of the large space requirement of resistors produced in a silicon substrate.
- 2) nMOS depletion mode transistor pull-up :-
 a) Dissipation is high since rail to rail current flows when $V_{in} = \text{logical 1}$.

- b) Switching of o/p from 1 to 0 begins when V_{in} exceeds V_t of P.d
- c) when switching the output from 1 to 0, the p.u device is non-saturated initially and this presents lower resistance through which to charge capacitive loads.

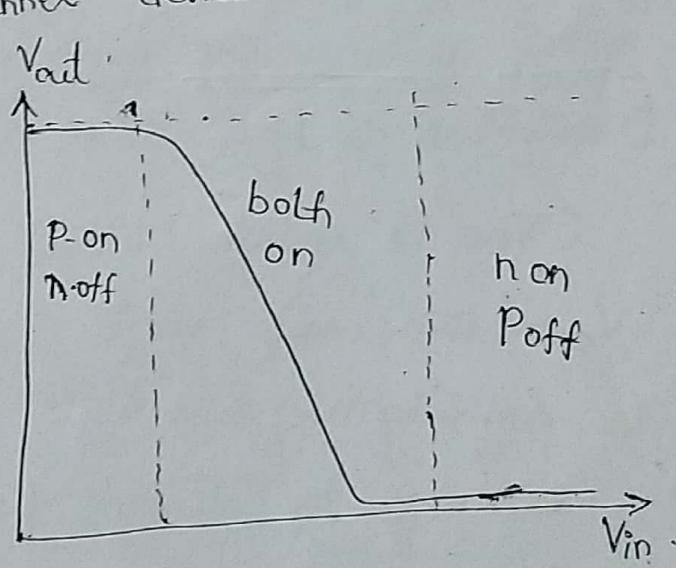
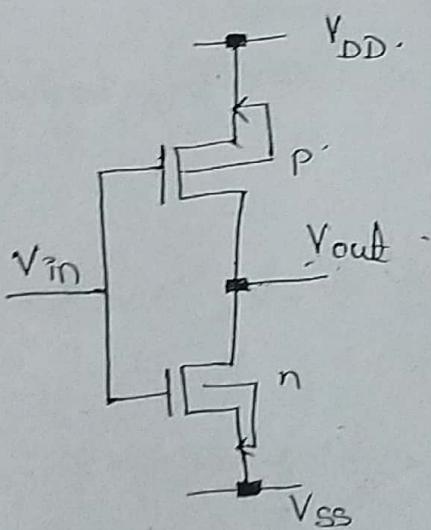


- 3) nMOS enhancement mode pull-up
- Dissipation is high since current flows when V_{in} = logical 1 (V_{aa} is returned to V_{DD})
 - V_{out} can never reach V_{DD} (logical 1) if $V_{aa} = V_{DD}$ as is normally the case.
 - V_{aa} may be derived from a switching source, for example one phase of a clock, so that dissipation can be greatly reduced.
 - If V_{aa} is higher than V_{DD} then an extra supply rail is required.



4) Complementary transistor pull-up (CMOS)

- No current flow either for logical 0 or for logical 1 inputs.
- full logical 1 and 0 levels are presented at the output
- For devices of similar dimensions the p-channel is slower than the n-channel device



The CMOS Inverter

$$I_{ds} = K \frac{w}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \quad \text{in the resistive region}$$

$$I_{ds} = K \frac{w}{L} \frac{(V_{gs} - V_t)^2}{2} \quad \text{in saturation region.}$$

K = technology dependent parameter.

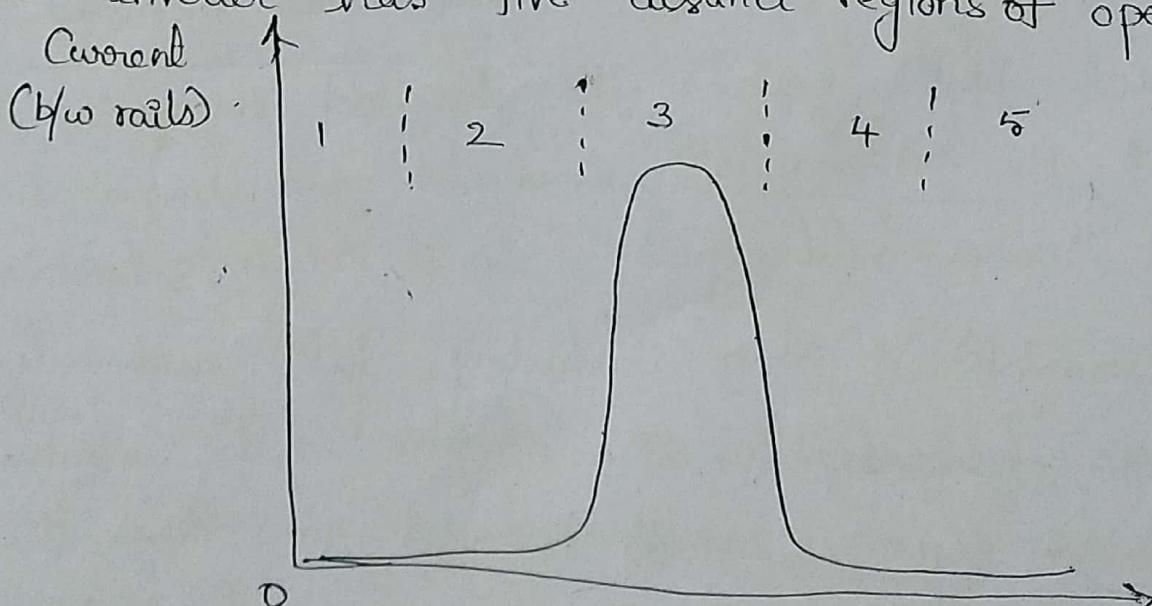
$$K = \frac{\epsilon_{ins} \epsilon_0 \mu}{D}$$

$$\beta = K \frac{w}{L}$$

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2 \quad \text{in saturation.}$$

where w_n, L_n, w_p, L_p are the n and p transistor dimensions.

CMOS inverter has five distinct regions of operation.



β may be applied to both NMOS and PMOS transistors as follows

$$\beta_n = \frac{\epsilon_{ins} \epsilon_0 U_n}{D} \frac{\omega_n}{L_n}$$

$$\beta_p = \frac{\epsilon_{ins} \epsilon_0 U_p}{D} \frac{\omega_p}{L_p}$$

In region 1 for which $V_{in} = \text{logic 0}$, we have the p-transistor fully turned on while the n-transistor is fully turned off. Thus no current flows through the inverter and the o/p is directly connected to V_{DD} through the p-transistor. A good logic 1 output is thus present at the output.

In region 5 $V_{in} = \text{logic 1}$, the n-transistor is fully on while the p-transistor is fully off. Again, no current flows and a good logic 0 appears at the o/p.

In region 2 the input Voltage has increased to a level which just exceeds the threshold Voltage of the n-transistor. The n-transistor conducts and has a large Voltage b/w source and drain. So it is in saturation. The p-transistor is also conducting but with only a small Voltage across it, it operates in the unsaturated resistive region. A small current now flows through the inverter from V_{DD} to V_{SS} .

Region 4 is similar to region 2 but with the roles of the P- and n transistors reversed. The current magnitudes in 2,4 regions are small and most of the energy consumed in switching from one state to the other is due to large current. Region 3 is the region in which the inverter exhibits gain and both transistors are in saturation.

The currents in each device must be the same since the transistors are in series.

$$I_{dsp} = -I_{dsn}$$

$$I_{dsp} = \frac{\beta_p}{2} (V_{in} - V_{DD} - V_{tp})^2$$

and

$$I_{dsn} = \frac{\beta_n}{2} (V_{in} - V_{tn})^2$$

we can express V_{in} in terms of the β ratio and the other circuit voltages and currents.

$$V_{in} = \frac{V_{DD} + V_{tp} + V_{tn} (\beta_n / \beta_p)^{1/2}}{1 + (\beta_n / \beta_p)^{1/2}}$$

Since both transistors are in saturation they act as current sources so that the equivalent circuit in this region is two current sources in series b/w V_{DD} and V_{SS} .

if $\beta_n = \beta_p$ and $V_{tn} = -V_{tp}$

then $V_{in} = 0.5 V_{DD}$

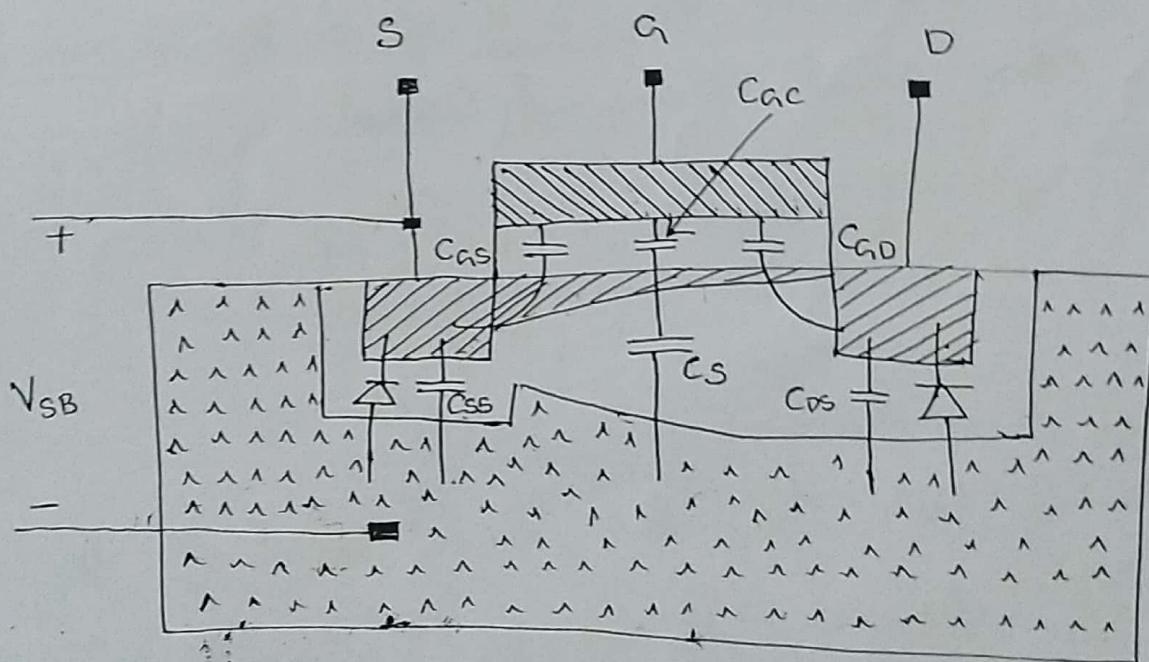
$V_{in} = V_{out} = 0.5 V_{DD}$

for $\beta_n = \beta_p$ $\frac{W_P W_P}{L_P} = \frac{W_n W_n}{L_n}$

but the mobilities are unequal and thus it is necessary for the width to length ratio of the P-device to be two to three times that of the n-device.

$$\frac{W_P}{L_P} = 2.5 \frac{W_n}{L_n}$$

MOS transistor circuit model



C_{GC} = gate to channel capacitance

C_{GS} = gate to source capacitance

C_{GD} = gate to drain capacitance

C_{SS} = source to substrate capacitance

C_{DS} = drain to substrate capacitance

C_{CS} = channel to substrate capacitance.

2.12 Some characteristics of npn bipolar transistors

Transconductance g_m - bipolar

The transconductance of a bipolar transistor is commonly presented as $g_m = I_c / \frac{kT}{qV}$

I_c = collector current

qV = electron charge

k = Boltzmann's constant

T = temperature °K

The expression can be rewritten in the form

$$g_m \propto A_E e^{V_{be}(q/kT)}$$

where V_{be} is the base to emitter voltage

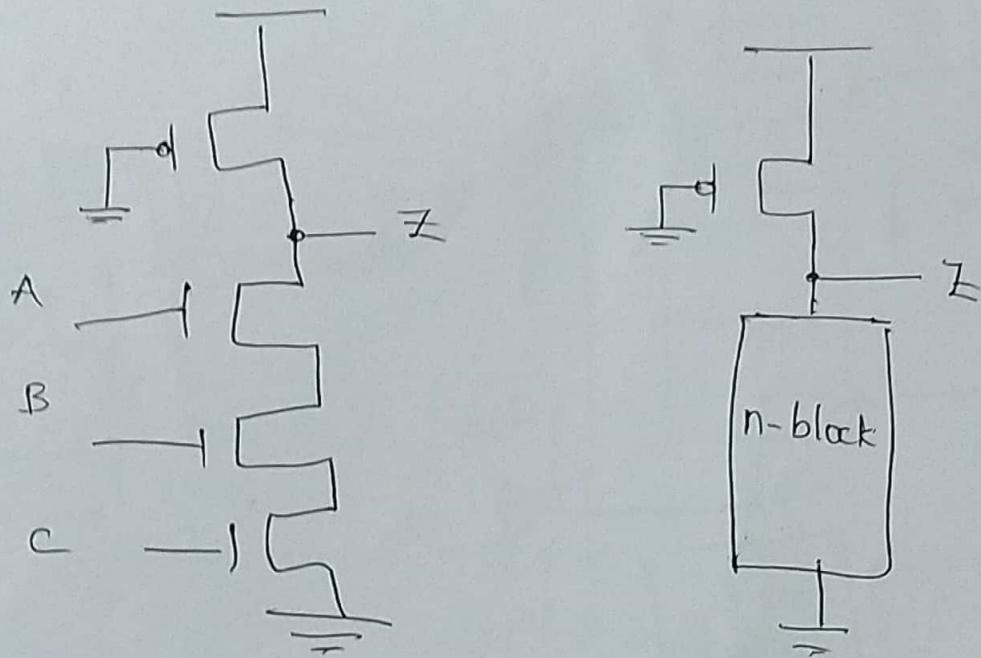
and A_E is the emitter area.

Other forms of CMOS

1) Pseudo-nMOS logic.

with three input nand

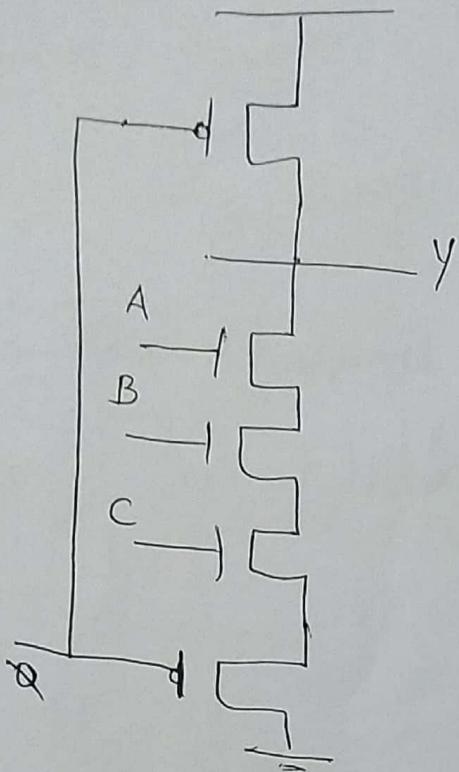
like depletion mode pull up transistors with a P-transistor with gate connected to V_{SS}



For this type of Pseudo-nMOS logic the Z.P.u/Z.P.d ratio is 3/1.

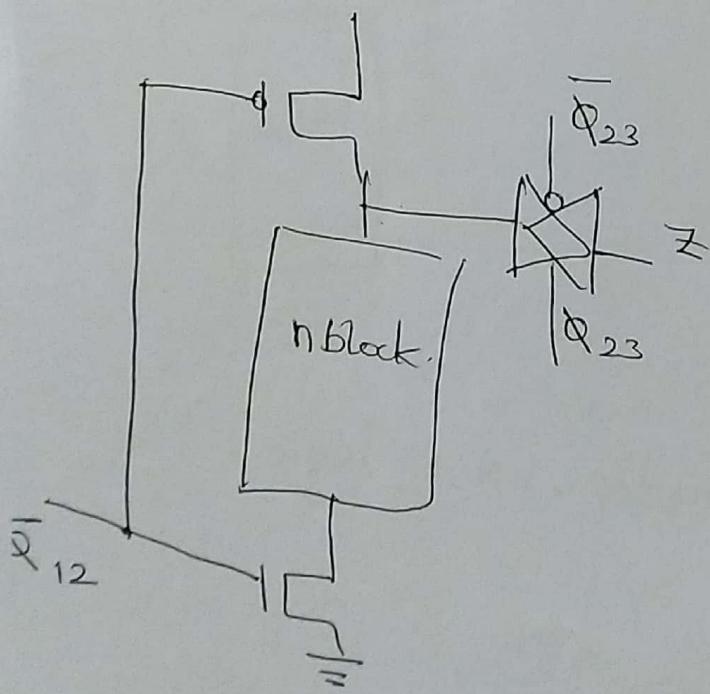
2) Dynamic

- 1) Charge sharing may be a problem
- 2) delays more.



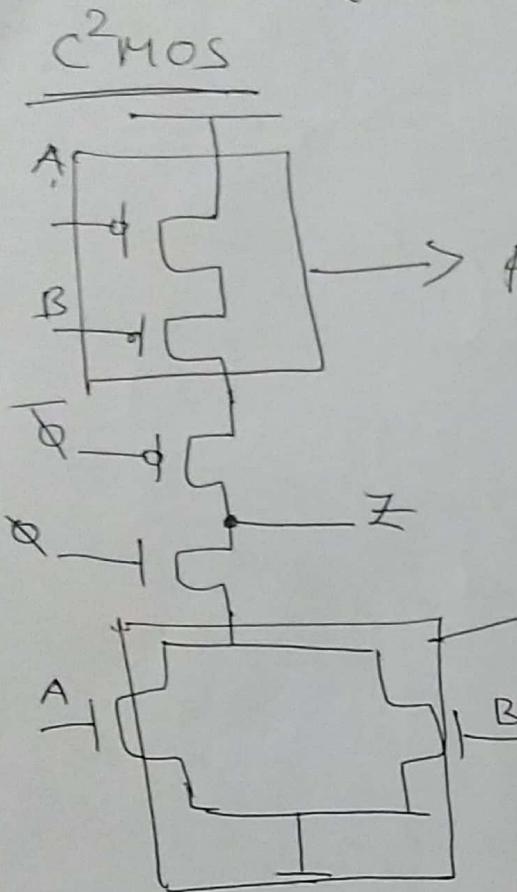
Single phase structures cannot be cascaded.

Better to use four phase clock

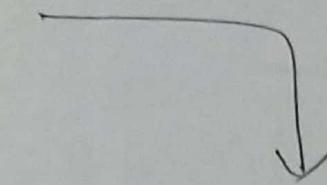


CMOS domino

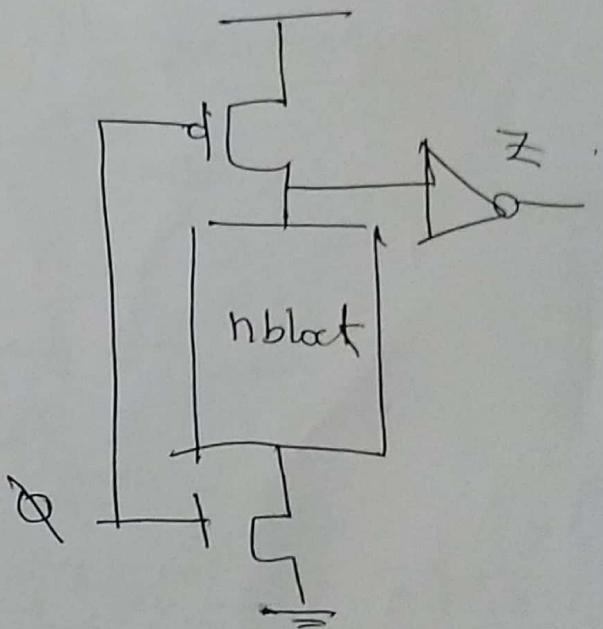
use only single phase



C²MOS

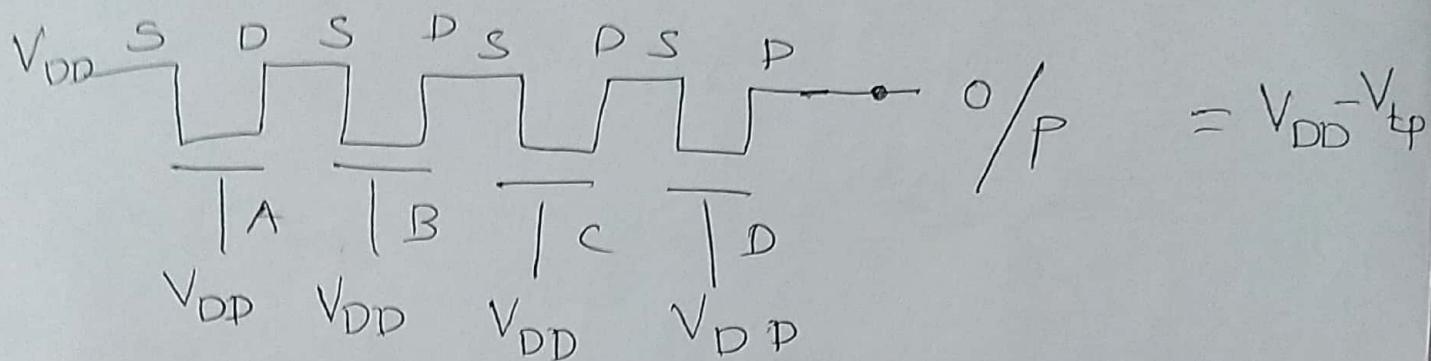


CMOS domino

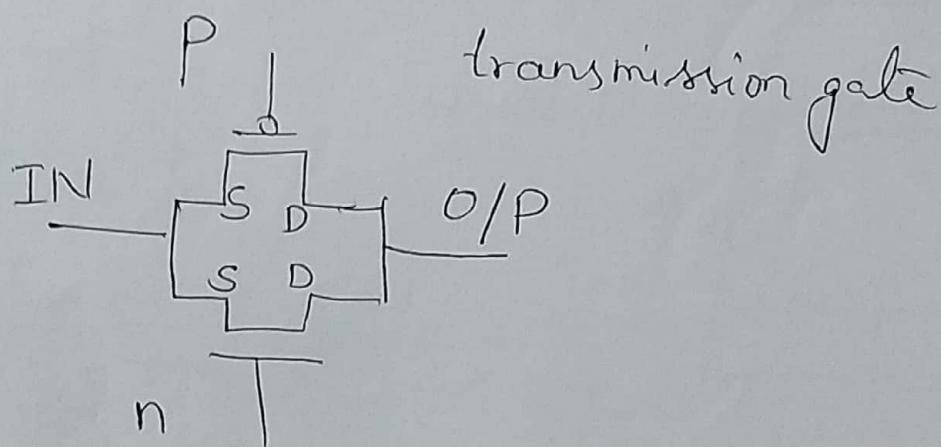


- 1) Parasitics are small
- 2) Small area
- 3) Charge distribution may be prob
- 4) free of glitches.

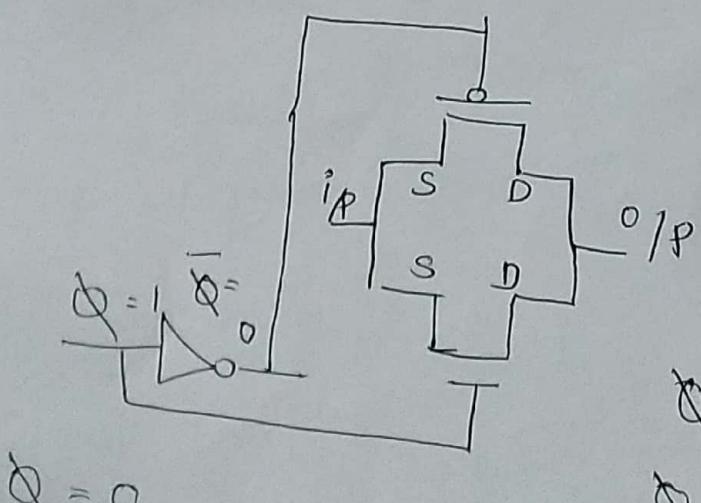
Pass transistors



Transmission logic



logic



$Q = 0$,

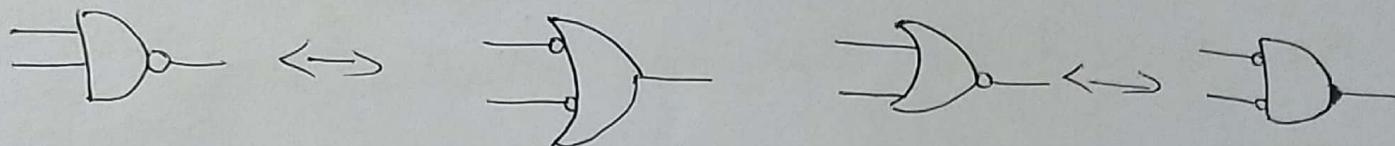
$Q = 1, \bar{Q} = 0$ $O/P = i_P$.
 $Q = 0, \bar{Q} = 1$ $O/P = \bar{i}_P$.
 Both will be off $O/P = \text{Z}$.

Static CMOS

DeMorgan's law

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

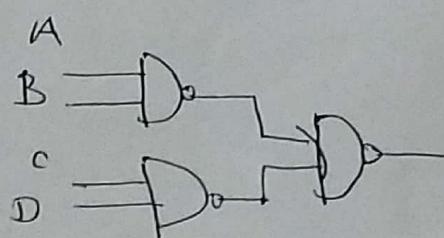
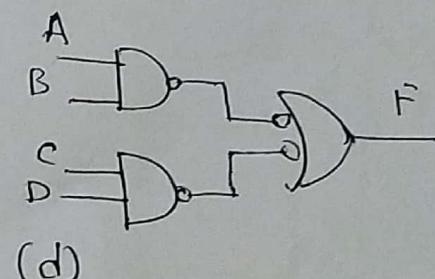
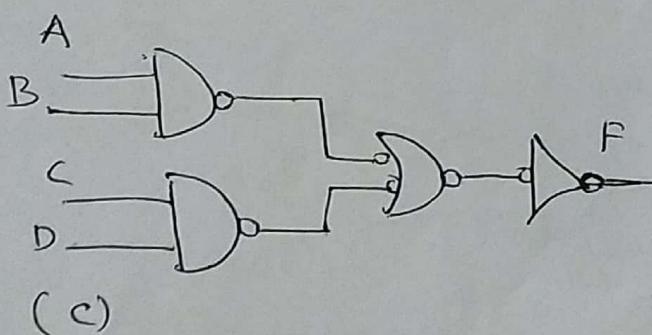
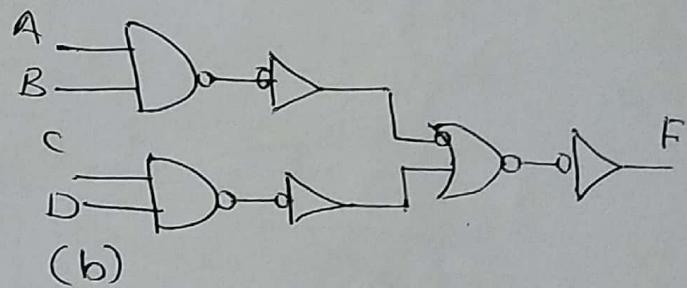
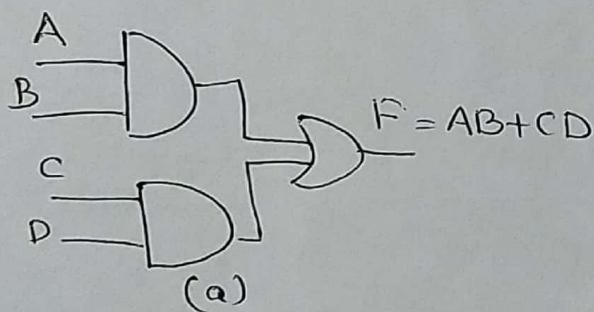
$$\overline{A+B} = \overline{A} \cdot \overline{B}$$



Switching between these representations is easy to do on a white board and is often called bubble pushing.

- 1) Design a circuit to compute $F = AB + CD$ using NANDS

$$F = AB + CD$$



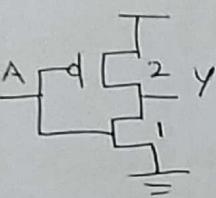
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logical effort :- Logical effort of each input is the ratio of the input capacitance of that input to the input capacitance of the inverter.

- The parasitic delay is crudely estimated from the total diffusion capacitance on the output node by summing the sizes of the transistors attached to the output.

Unit Inverter

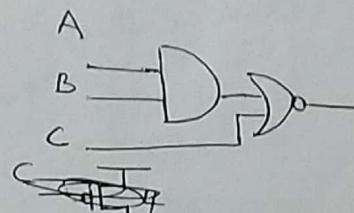
$$Y = \overline{A}$$



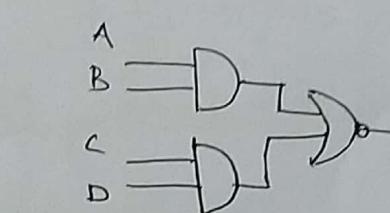
$$g_A = 3/3$$

$$P = 3/3$$

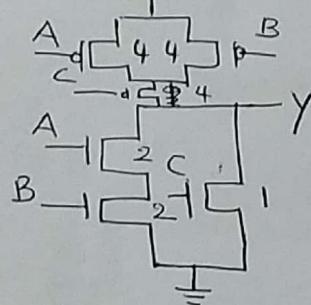
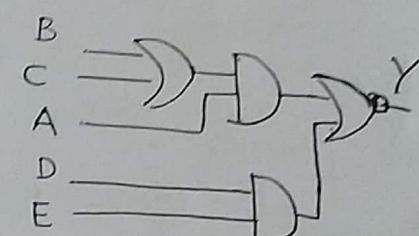
$$Y = \overline{A \cdot B + C}$$



$$Y = \overline{A \cdot B + C \cdot D}$$



$$Y = \overline{A \cdot (B + C) + D \cdot E}$$

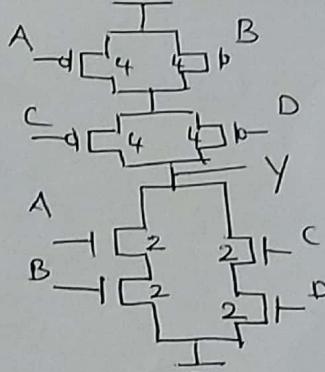


$$g_A = 6/3$$

$$g_B = 6/3$$

$$g_C = 5/3$$

$$P = 7/3$$



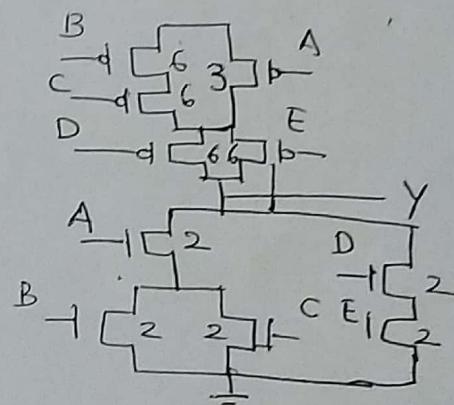
$$g_A = 6/3$$

$$g_B = 6/3$$

$$g_C = 6/3$$

$$g_D = 6/3$$

$$P = 12/3$$



$$g_A = 5/3$$

$$g_B = 8/3$$

$$g_C = 8/3$$

$$g_D = 8/3$$

$$g_E = 8/3$$

$$P = 16/3$$