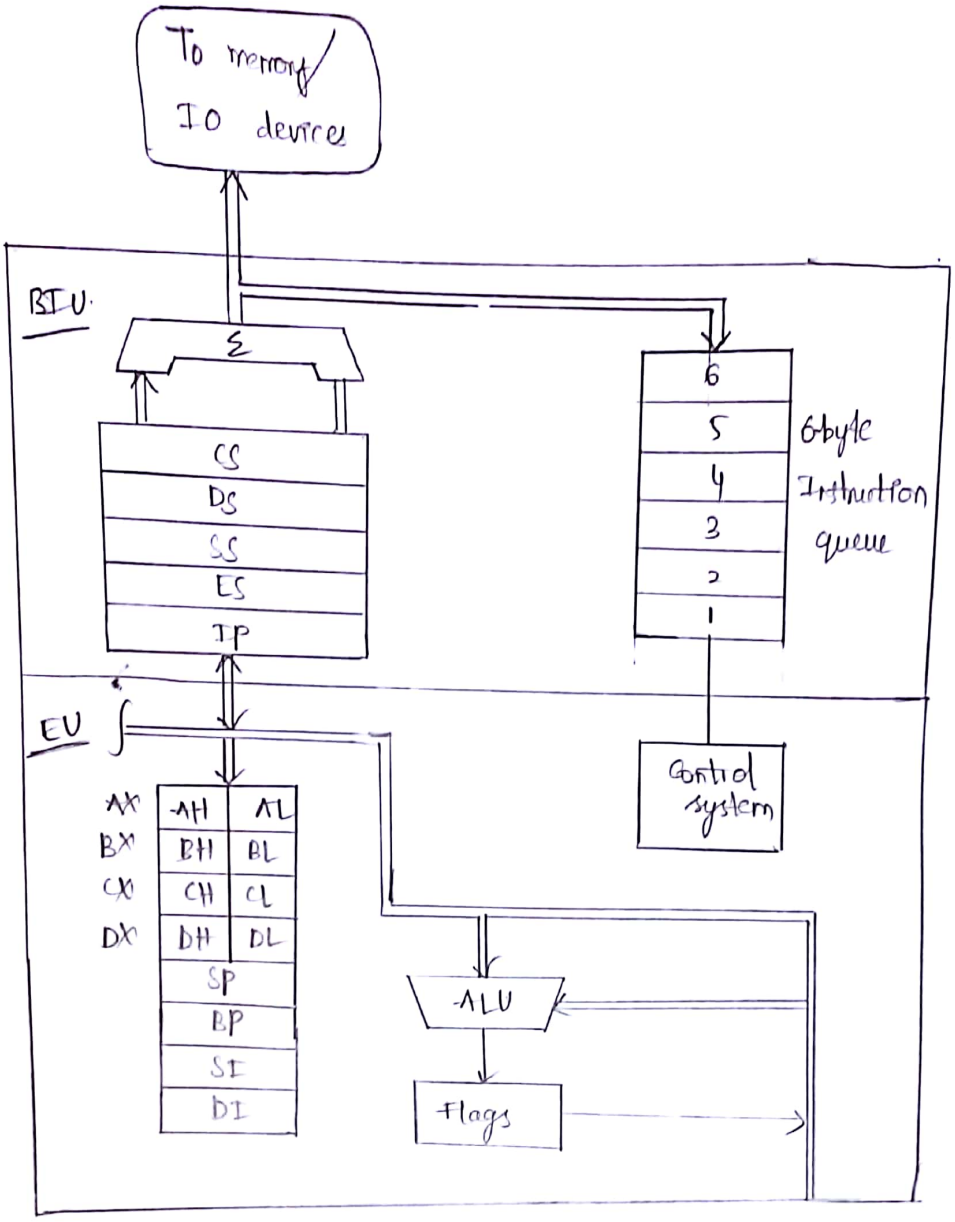


8086 Architecture

8086 Architecture:

→ Architecture is divided into 2 units

1) Bus interface unit (BIU)
2) Execution unit (EU)

Out of 14 registers, 5 are present in BIU and 9 are present in EU.

Functions of BIU:

→ It generates 20-bit physical address using summer.
→ It gives the interface to the memory / IO devices.
→ It reads/writes the data to the memory (or) from the memory.
→ It also sends addresses to memory (or) IO ports
→ Other blocks present are 6-byte Instruction queue
→ It fetches the 6 bytes of next instruction.
→ It is decoded by the control system.

Execution Unit (EU)

→ The next instruction is decoded by control system.
→ Pipelining is used in this unit
→ It decodes instruction and performs arithmetic (+, −, *) and logical operations (AND/OR/NOT, shift, Rotate)
→ updates the flag register.

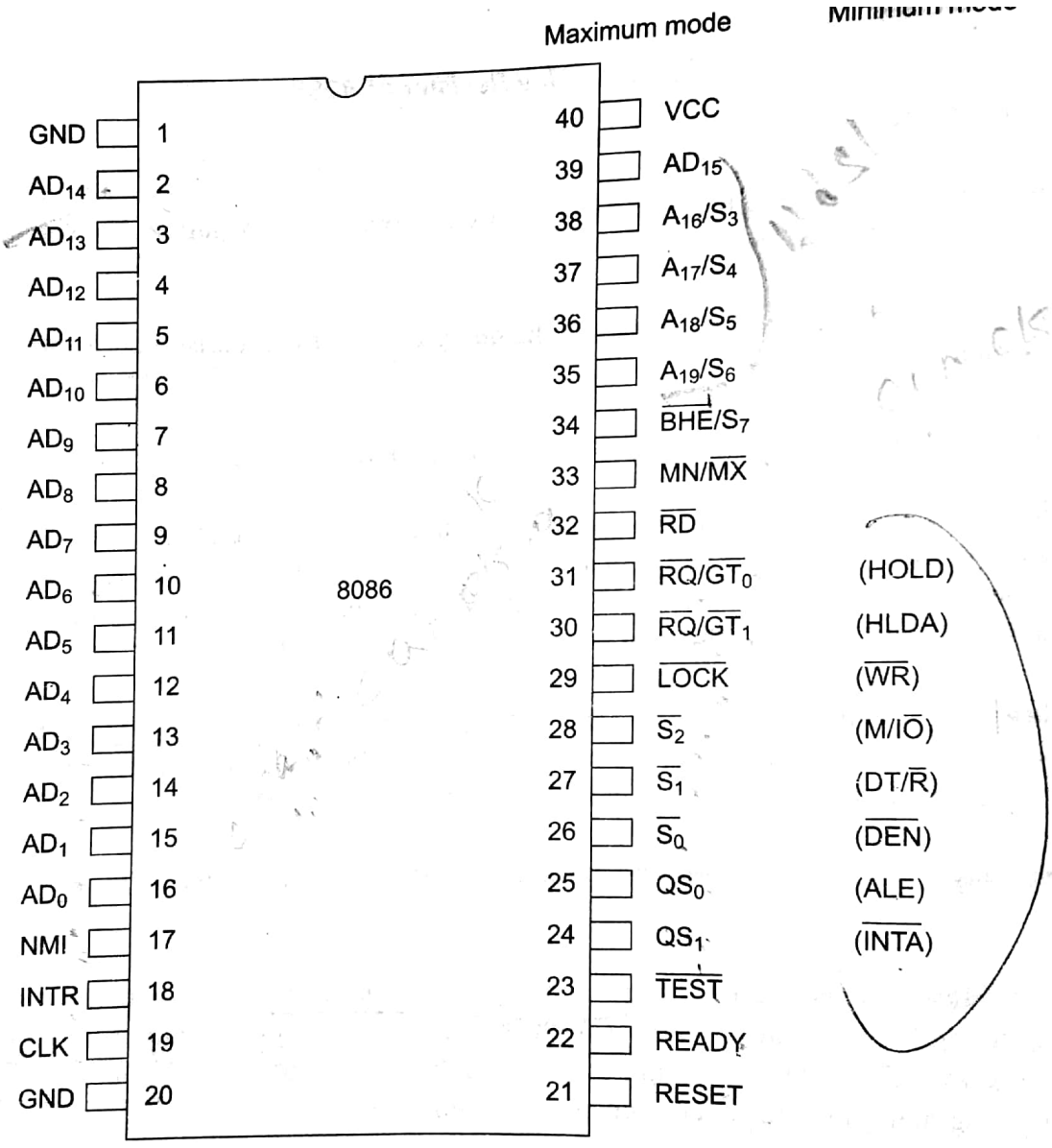


Fig. 1.5 *Pin Configuration of 8086*

The following signal descriptions are common for both the minimum and maximum

is dropped by the requesting master, the HLDA is dropped by the processor at the trailing edge of the r clock, as shown in Fig. 1.14 (c). The other conditions have already been discussed in the signal descripti section for the HOLD and HLDA signals.

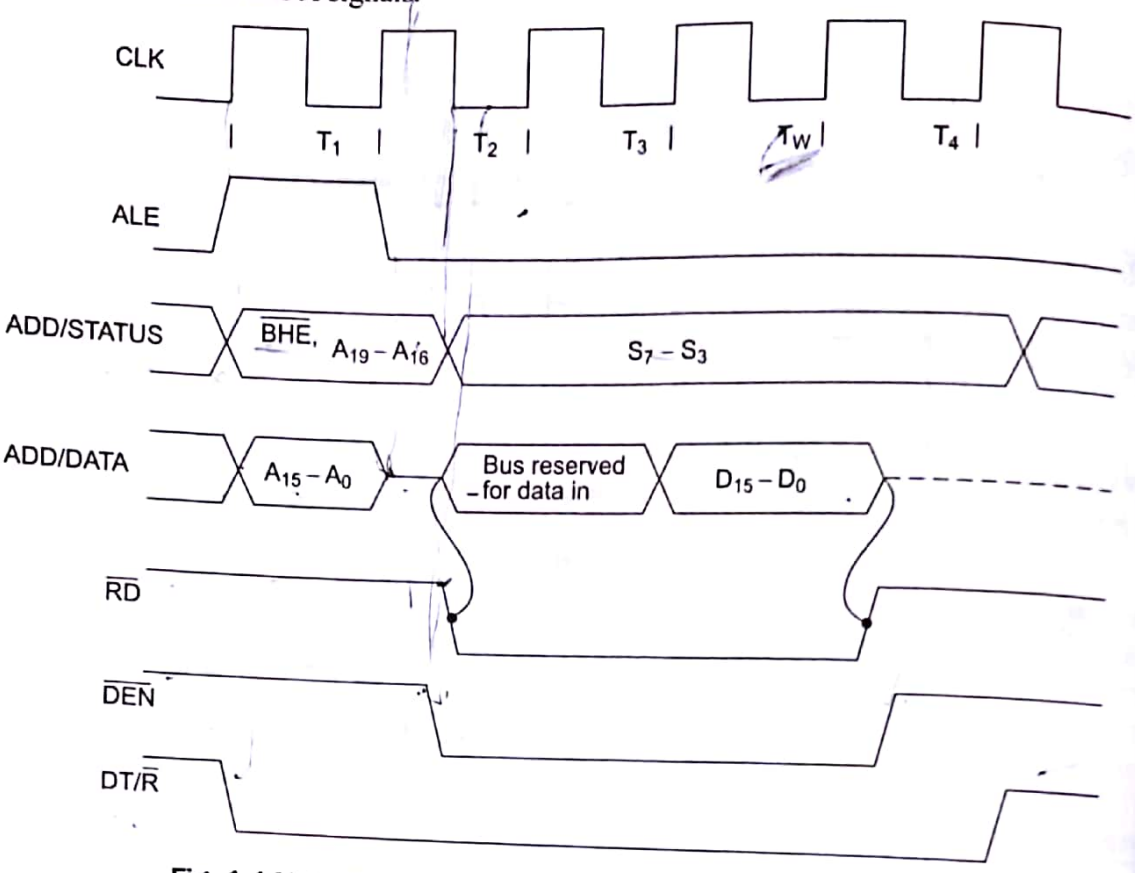


Fig. 1.14(a) *Read Cycle Timing Diagram for Minimum Mode*

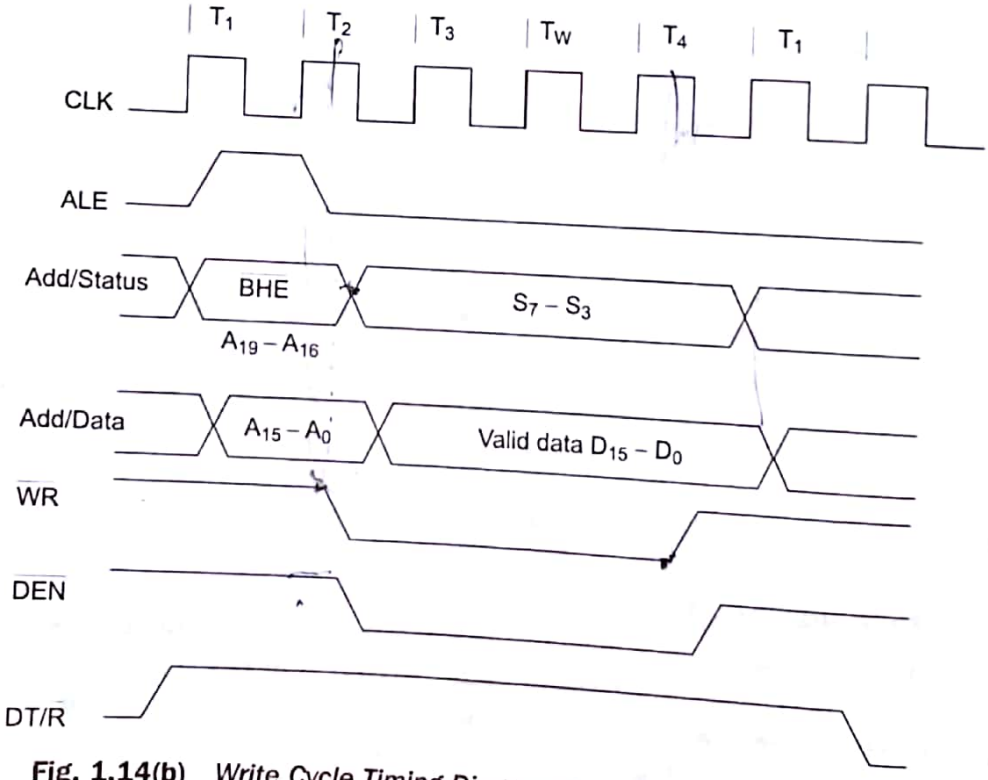


Fig. 1.14(b) *Write Cycle Timing Diagram for Minimum Mode Operation*

The basic functions of the bus controller chip IC8288, is to derive control signals like $\overline{RD}$ and $\overline{WR}$ (for memory and I/O devices), $\overline{DEN}$, DT/$\overline{R}$, ALE, etc. using the information made available by the processor on the status lines. The bus controller chip has input lines $\overline{S}_2$, $\overline{S}_1$ and $\overline{S}_0$ and CLK, which are driven by the CPU. It derives the outputs ALE, DEN, DT/$\overline{R}$, $\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$ and $\overline{AIOWC}$. The $\overline{AEN}$, IOB and CEN pins are specially useful for multiprocessor systems. $\overline{AEN}$ and IOB are generally grounded. CEN pin is usually tied to +5V. The significance of the MCE/$\overline{PDEN}$ output depends upon the status of the IOB pin. If IOB is grounded, it acts as master cascade enable to control cascaded 8259A, else it acts as peripheral data enable used in the multiple bus configurations. $\overline{INTA}$ pin is used to issue two interrupt acknowledge pulses to the interrupt controller or to an interrupting device.

$\overline{IORC}$, $\overline{IOWC}$ are I/O read command and I/O write command signals respectively. These signals enable an IO interface to read or write the data from or to the addressed port. The $\overline{MRDC}$, $\overline{MWTC}$ are memory read command and memory write command signals respectively and may be used as memory read and write signals. All these command signals instruct the memory to accept or send data to or from the bus. For both of these write command signals, the advanced signals namely $\overline{AIOWC}$ and $\overline{AMWTC}$ are available. They also serve the same purpose, but are activated one clock cycle earlier than the $\overline{IOWC}$ and $\overline{MWTC}$ signals, respectively. The maximum mode system is shown in Fig. 1.15.

The maximum mode system timing diagrams are also divided in two portions as read (input) and write (output) timing diagrams. The address/data and address/status timings are similar to the minimum mode. ALE is asserted in T_1, just like minimum mode. The only difference lies in the status signals used and the available control and advanced command signals. Figure 1.16 (a) shows the maximum mode timings for the read operation while the Fig. 1.16 (b) shows the same for the write operation. The CS Logic block represents chip select logic and the 'e' and 'O' suffixes indicate even and odd address memory bank.

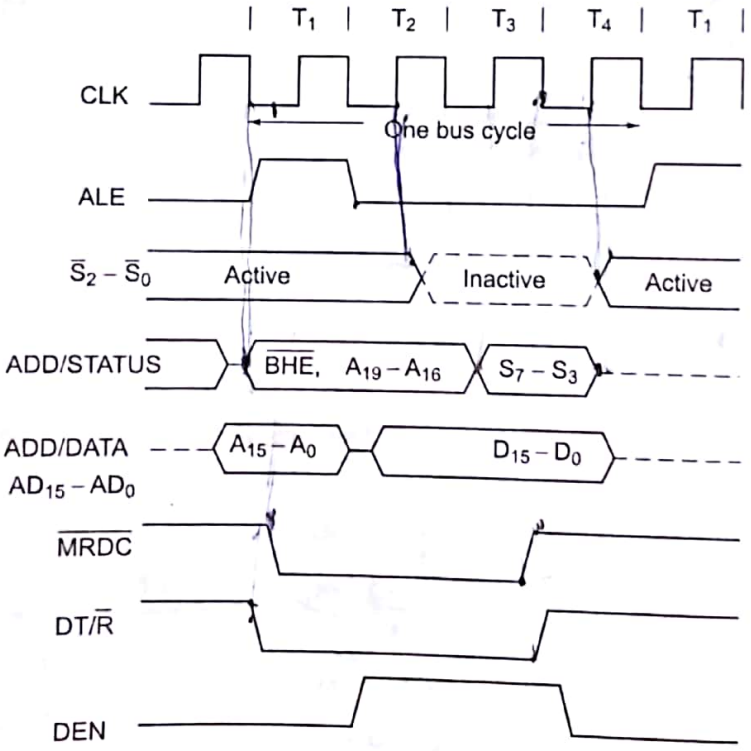


Fig. 1.16 (a) *Memory Read Timing in Maximum Mode*

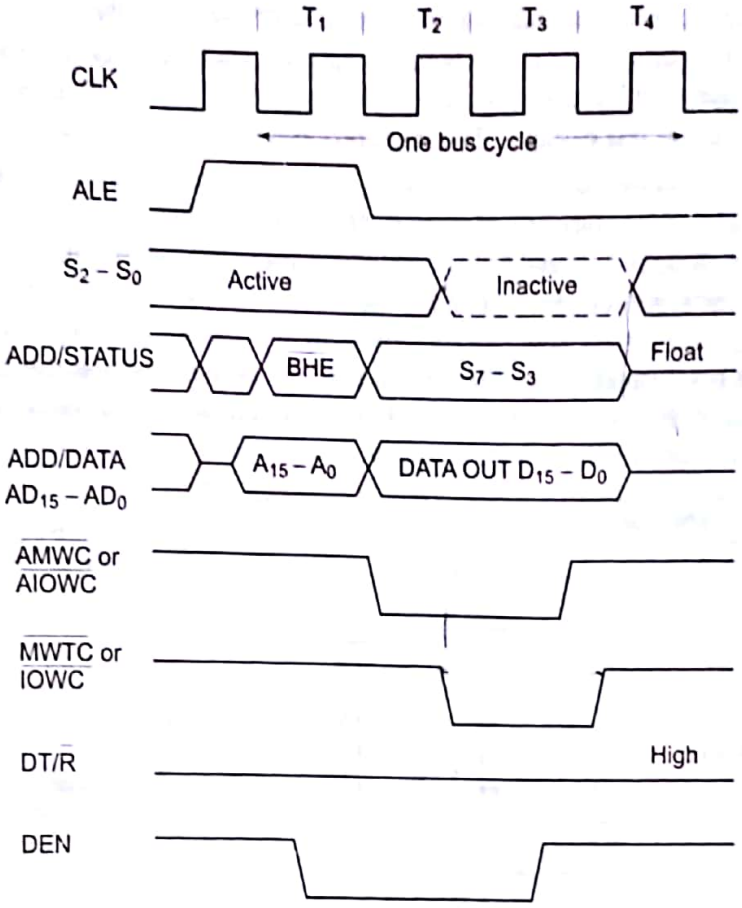


Fig. 1.16(b) *Memory Write Timing in Maximum Mode*

1.9.1 Timings for $\overline{RQ}/\overline{GT}$ Signals

The request/grant response sequence contains a series of three pulses as shown in the timing diagram Fig.1.16 (c). The request/grant pins are checked at each rising pulse of clock input. When a request is detected and if the conditions discussed in pin diagram section of this chapter for valid HOLD request are satisfied, the processor issues a grant pulse over the $\overline{RQ}/\overline{GT}_0$ pin immediately during the T_4 (current) or T_1 (next) state. When the requesting master receives this pulse, it accepts the control of the bus. The requesting master uses the bus till it requires. When it is ready to relinquish the bus, it sends a release pulse to the processor (host) using the $\overline{RQ}/\overline{GT}$ pin. This sequence is shown in Fig. 1.16 (c).

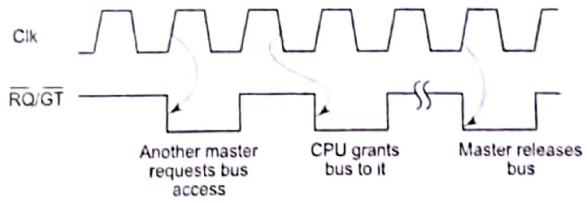
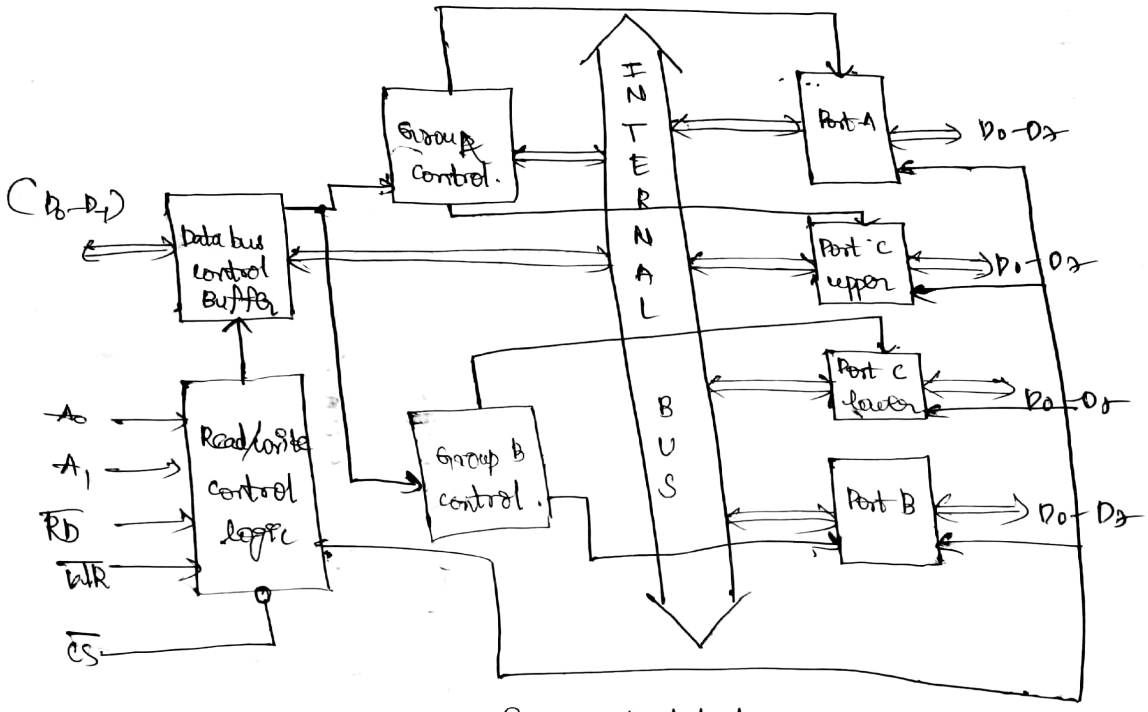


Fig. 1.16 (c) *$\overline{RQ}/\overline{GT}$ Timings in Maximum Mode*

1.10 THE PROCESSOR 8088

The launching of the processor 8086 is seen as a remarkable step in the development of high speed computing machines. Before the introduction of 8086, most of the circuits required for the different applications in computing and industrial control fields were already designed around the 8-bit processor 8085. The 8086 imparted



8255 Architecture.

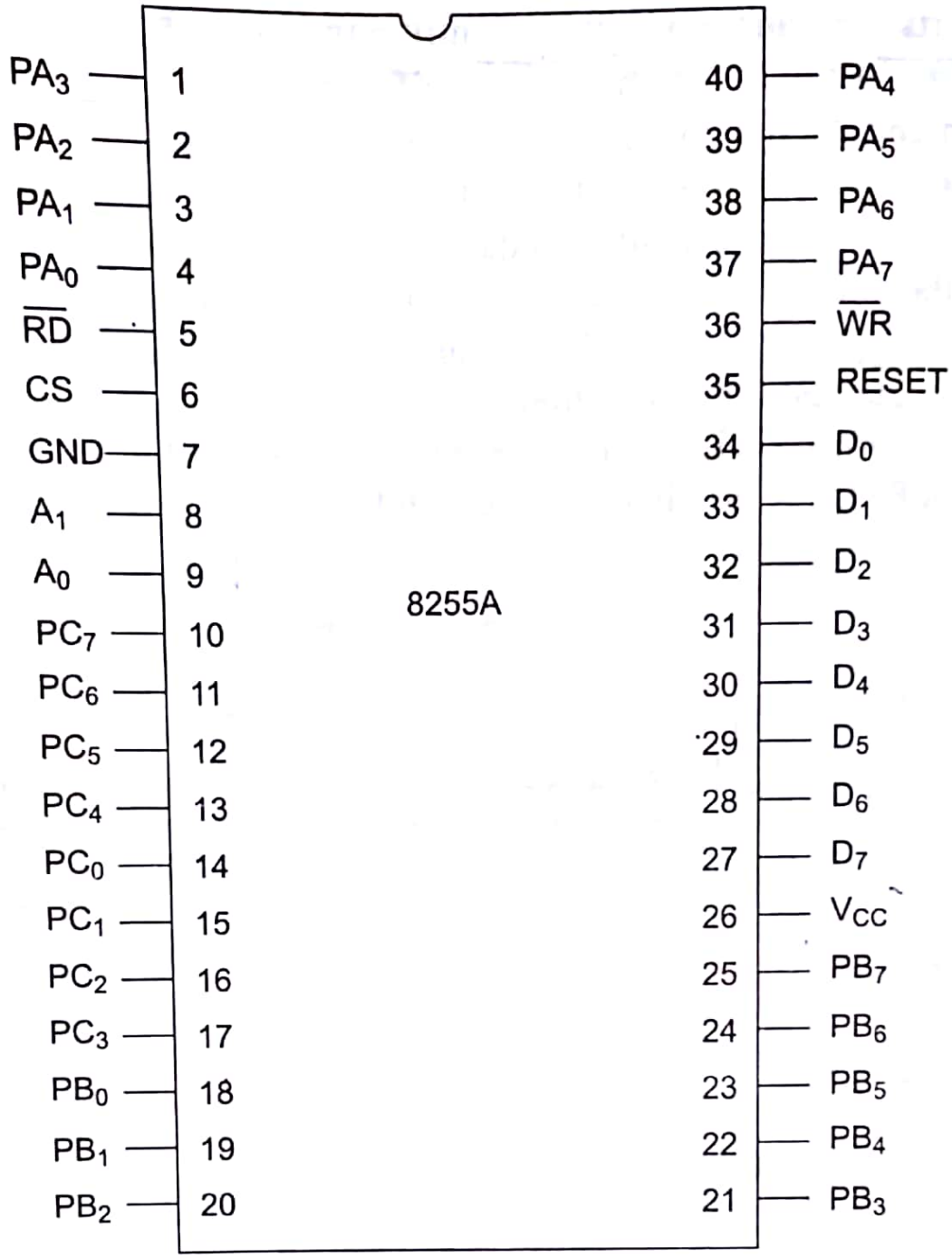


Fig. 5.17(b) *8255A Pin Configuration*

is the input line driven by the microprocessor and should be low to indicate read operation

6.2.1 Architecture and Signal Descriptions of 8259A

The architectural block diagram of 8259A is shown in Fig. 6.12. The functional explanation of each block is given in the following text in brief:

Interrupt Request Register (IRR) The interrupts at IRQ input lines are handled by Interrupt Request Register internally. IRR stores all the interrupt requests in it in order to serve them one by one on the priority basis.

In-Service Register (ISR) This stores all the interrupt requests those are being served, i.e. ISR keeps a track of the requests being served.

Priority Resolver This unit determines the priorities of the interrupt requests appearing simultaneously. The highest priority is selected and stored into the corresponding bit of ISR during $\overline{INTA}$ pulse. The IR_0 has the highest priority while the IR_7 has the lowest one, normally in fixed priority mode. The priorities however may be altered by programming the 8259A in rotating priority mode.

Interrupt Mask Register (IMR) This register stores the bits required to mask the interrupt inputs. IMR operates on IRR at the direction of the Priority Resolver.

Interrupt Control Logic This block manages the interrupt and the interrupt acknowledge signals to be sent to the CPU for serving one of the eight interrupt requests. This also accepts the interrupt acknowledge (INTA) signal from CPU that causes the 8259A to release vector address on to the data bus.

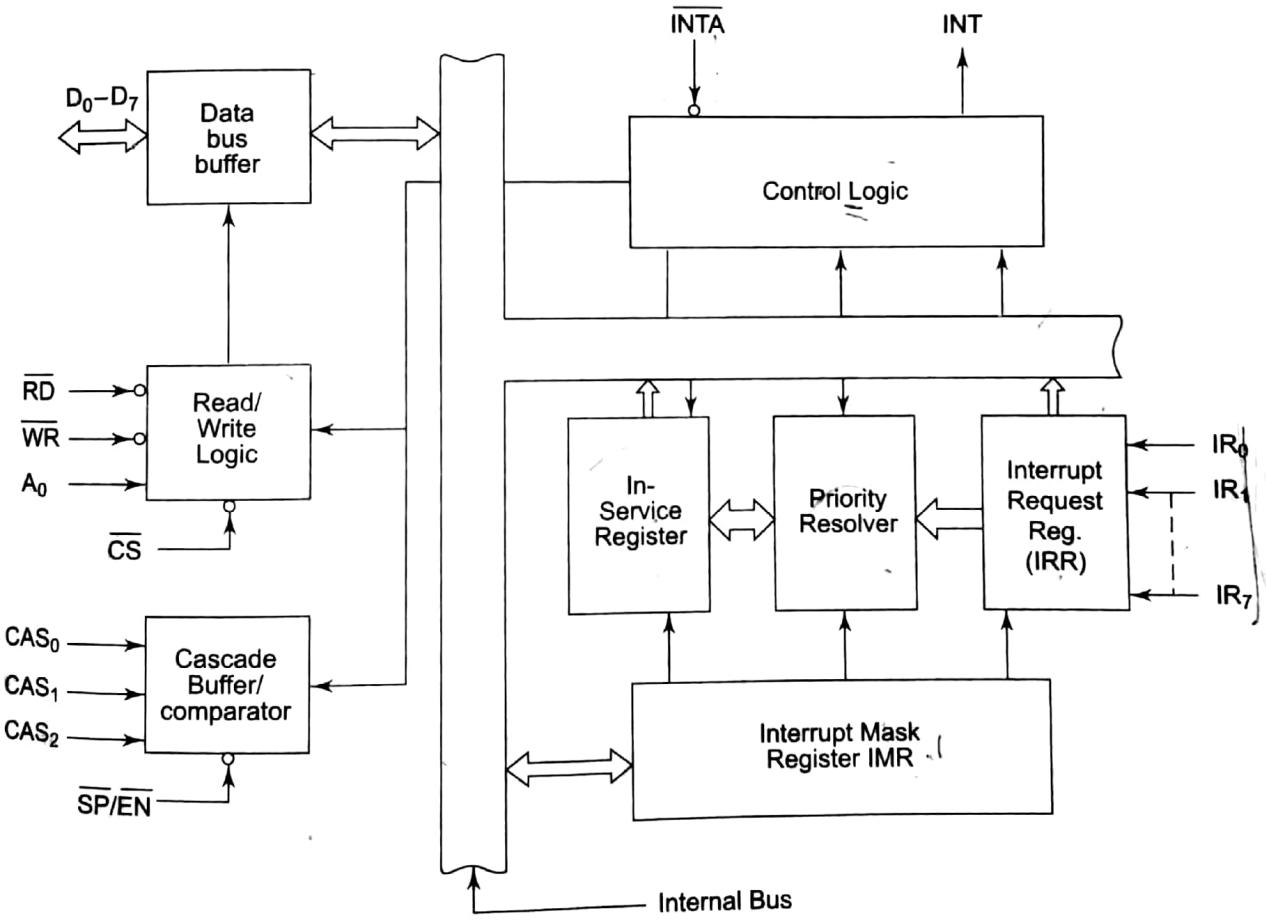


Fig. 6.12 *8259A Block Diagram*

Data Bus Buffer This tristate bidirectional buffer interfaces internal 8259A bus to the microprocessor system data bus. Control words, status and vector information pass through data buffer during read or write operations.

Read/Write Control Logic This circuit accepts and decodes commands from the CPU. This block also allows the status of the 8259A to be transferred on to the data bus.

Cascade Buffer/Comparator This block stores and compares the IDs of all the 8259As used in the system. The three I/O pins CAS0-2 are outputs when the 8259A is used as a master. The same pins act as inputs when the 8259A is in the slave mode. The 8259A in the master mode, sends the ID of the interrupting slave device on these lines. The slave thus selected, will send its pre-programmed vector address on the data bus during the next $\overline{\text{INTA}}$ pulse.

Figure 6.13 shows the pin configuration of 8259A, followed by their functional description of each of the signals in brief.

CS This is an active-low chip select signal for enabling $\overline{\text{RD}}$ and $\overline{\text{WR}}$ operations of 8259A. $\overline{\text{INTA}}$ function is independent of $\overline{\text{CS}}$.

$\overline{\text{WR}}$ This pin is an active-low write enable input to 8259A. This enables it to accept command words from CPU.

$\overline{\text{RD}}$ This is an active-low read enable input to 8259A. A low on this line enables 8259A to release status onto the data bus of CPU.

D_7–D_0 These pins form a bidirectional data bus that carries 8-bit data either to control word or from status word registers. This also carries interrupt vector information.

CAS_0–CAS_2 Cascade Lines A single 8259A provides eight vectored interrupts. If more interrupts are required, the 8259A is used in the cascade mode in which a master 8259A along with eight slaves 8259A can provide up to 64 vectored interrupt lines. These three lines act as select lines for addressing the slaves 8259A.

$\overline{\text{PS}}/\overline{\text{EN}}$ This pin is a dual purpose pin. When the chip is used in buffered mode, it can be used as a buffer enable to control buffer transreceivers. If this is not used in buffered mode then the pin is used as input to designate whether the chip is used as a master ($\overline{\text{SP}} = 1$) or a slave ($\overline{\text{EN}} = 0$).

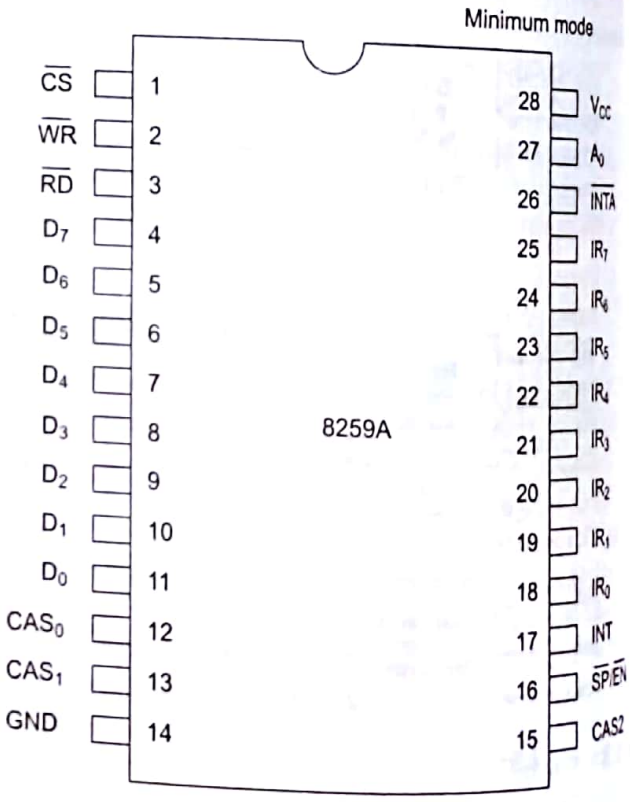
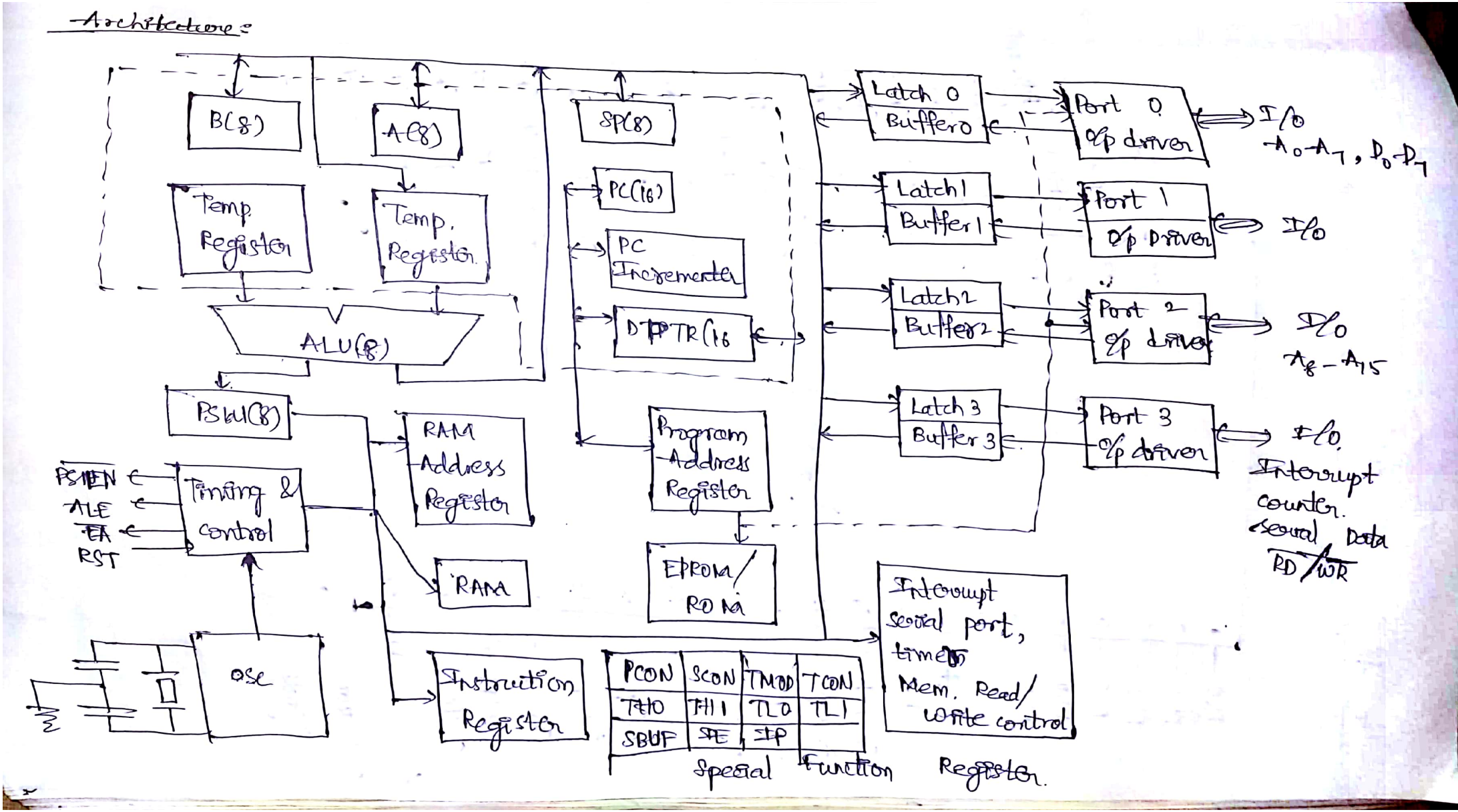


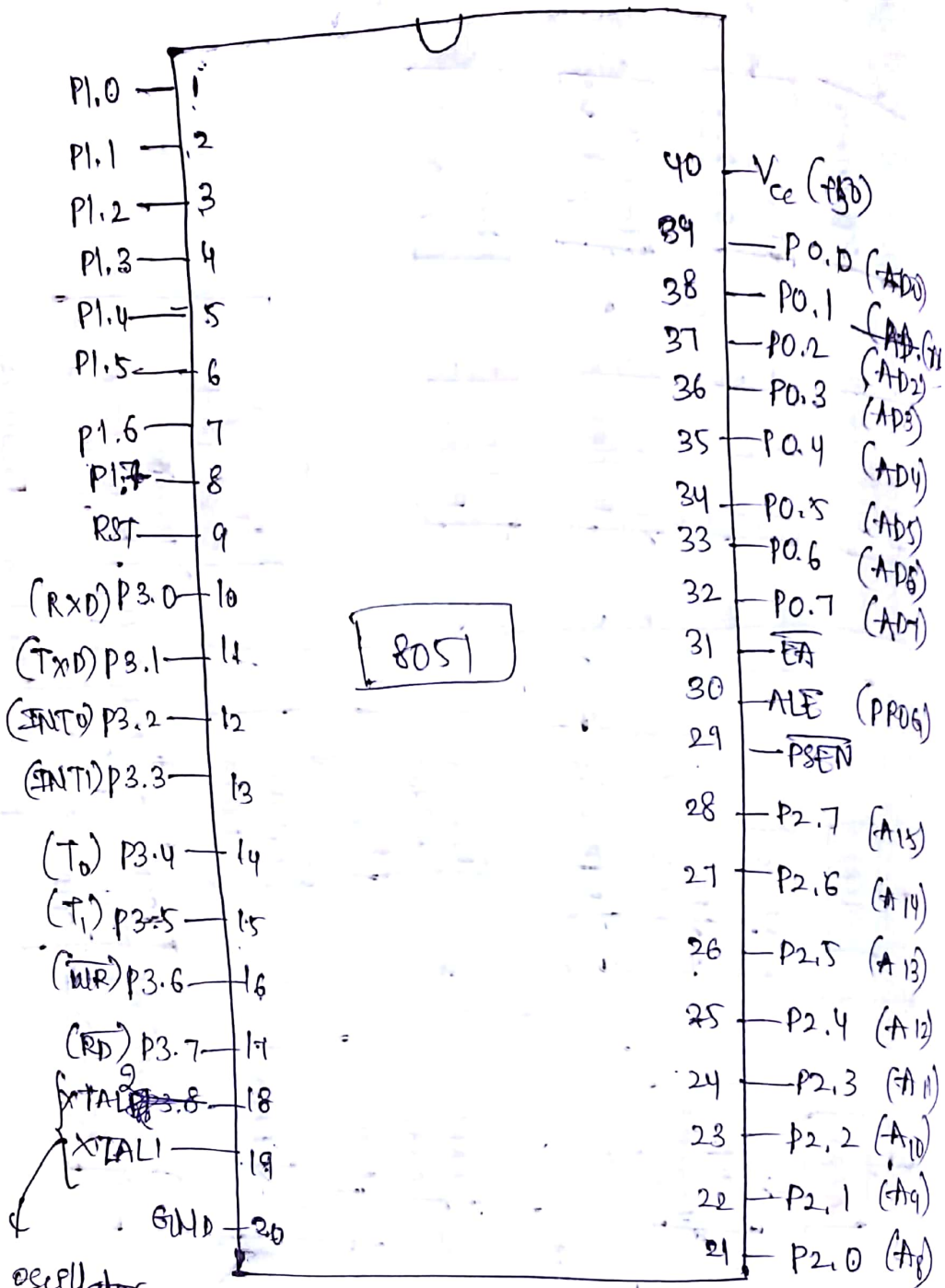
Fig. 6.13 *8259 Pin Diagram*

INT This pin goes high whenever a valid interrupt request is asserted. This is used to interrupt the CPU and is connected to the interrupt input of CPU.

Architecture :



Pin diagram of 8051



oscillator signals.

Special Function Registers (SFR's)

*A - E0H

*B - F0H

* PSW - D0H

DPH - 83H

DPL - 82H

* P0 - 80H

* P1 - 90H

* P2 - A0H

* P3 - B0H

* IP - B8H

* IE - A8H

TMOD - 89H

TCON - 88H

TH0 - 8CH
TL0 - 8AH
} Timer 0

TH1 - 8DH
TL1 - 8BH
} Timer 1

SCON - 98H serial control

SBUF - 99H - Serial Buffer

PCON - 87H power control.

* → indicates bit addressable (each and every bit can be controlled