– INT1 ——— Low Priority.

→ 8259 – PIC (Priority Interrupt Controller)

(8 - 64) I/O devices

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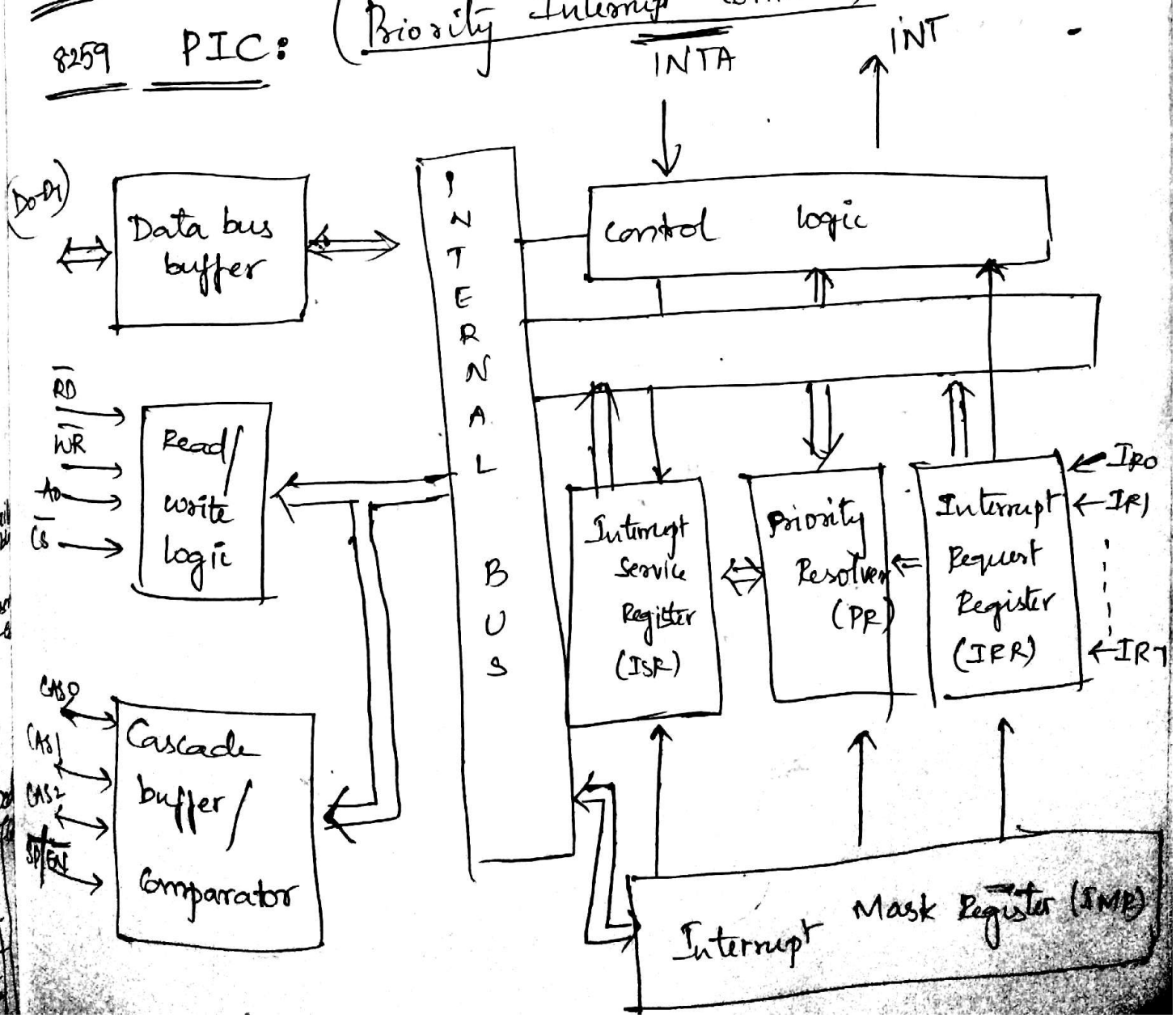
8259 PIC: (Priority Interrupt Controller)



→ IRR, ISR, PR, IMR are 8-bit registers.

→ IR levels — IR0 to IR7

→ IRR gives interrupt request level which requests the service.

if i/p is connected to IR0, IR1 & o/p to IR7,

	IR7	6	5	4	3	2	1	0
then	1	0	0	0	0	0	1	1

→ PR - if one I/o device requests the service, PR is not used.

- if more than one I/o devices requests the service, PR decides which has the higher priority.

→ ISR - It gives the level which is currently being serviced by 8086.

if 1000 0000 ⇒ IR7 is currently served by the 8086

~~0000 00~~

→ only one bit is '1' at a time

→ IMR — To mask the particular IR level

Two Command lines

ICW (4) OCW (3)

→ IMR is programmed in OCW - operational command

→ After 8086

→ Data

→ Read

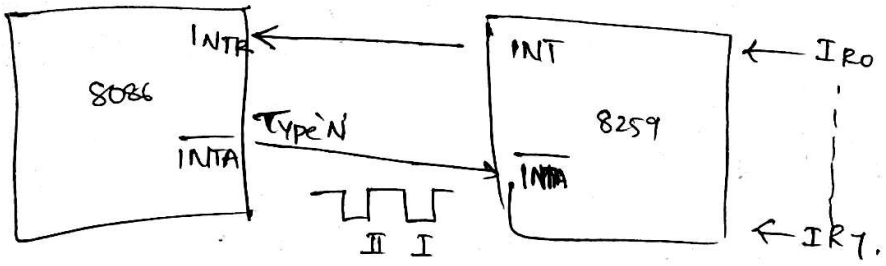
→ Casc

During

→ when

→ Def

→ After setting the priority, IR (request) is sent to 8086 from 8259 through INT &.
then 8086 sends INTA (acknowledge) to 8259



→ Data bus buffer → Sends data b/w 8086 & 8259
& also used to check the status of 8086.

→ Read/Write logic → $\overline{CS}=0$.

→ Cascade buffer / comparator → 3 I/o Cascade lines
CAS0, CAS1, CAS2
i/p's.

$\overline{SP}/\overline{EN}$ = Active low

$\overline{SP}=0$ ⇒ slave mode is enabled. (single mode)
$\overline{EN}=0$ ⇒ 8259 is operated in Master mode. (Cascade mode)

→ 8259 is interrupted with 8086 from 8 devices upto 64 devices.

During I (1st clk cycle):
→ when it is servicing, particular ISR bit is '1' & Corresponding IRR bit is '0'.

During II clk cycle:
→ it gives the type of interrupt in 8086.

→ Default; IR0 — high priority & IR7 — low priority.

Modes for Priority:

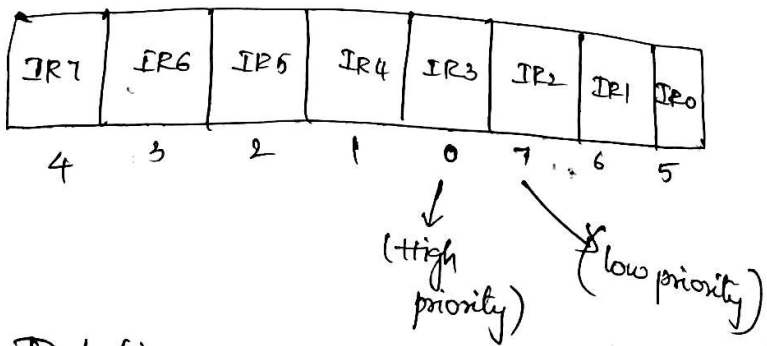
1. Fully Nested mode (or) Default mode:

IR0 – high priority
⋮
IR7 – low priority

2. Specific Rotation mode:

Any one of the IR level can be specified by assigning the low priority. Hence, the priorities of other IR levels get fixed in cyclic order.

Ex: If low priority is assigned to IR2, other priorities are as shown below (i.e., cyclic order).



3. Automatic Rotation mode:

If IR4 → low priority
IR3
IR2
IR1
IR0
IR7
IR6
IR5 → high priority.

4. Special Fully Nested

Master mode

8086 ← 8259 – Master

each Slave have

Here; IR

Ex:

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8259 PIC:

→End of Interrupt

1. Non-Specific E

it will reset of ISR.

2. Specific EOI

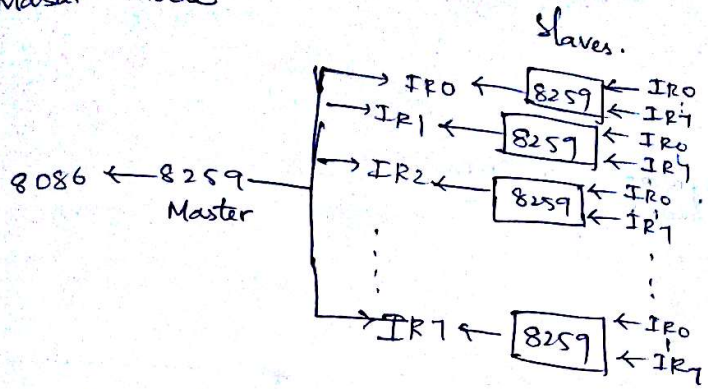
level can be this command specify the I

3. Automatic

8259 will

4. Special Fully Nested mode (default mode):

Master mode



each Slave have again 8 IR levels.

Here; IR0 — H.P (high priority)
IR7 — L.P (low priority)

Ex:

Slaves

IR1 ← IR3 (I priority)
IR6 (II ")

IR3 ← IR0 (III ")

IR7 ← IR4 (IV ")

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8259 PIC:

→End of Interrupt (EOI) Command: EOI resets the set bit in ISR after the interrupt is served.

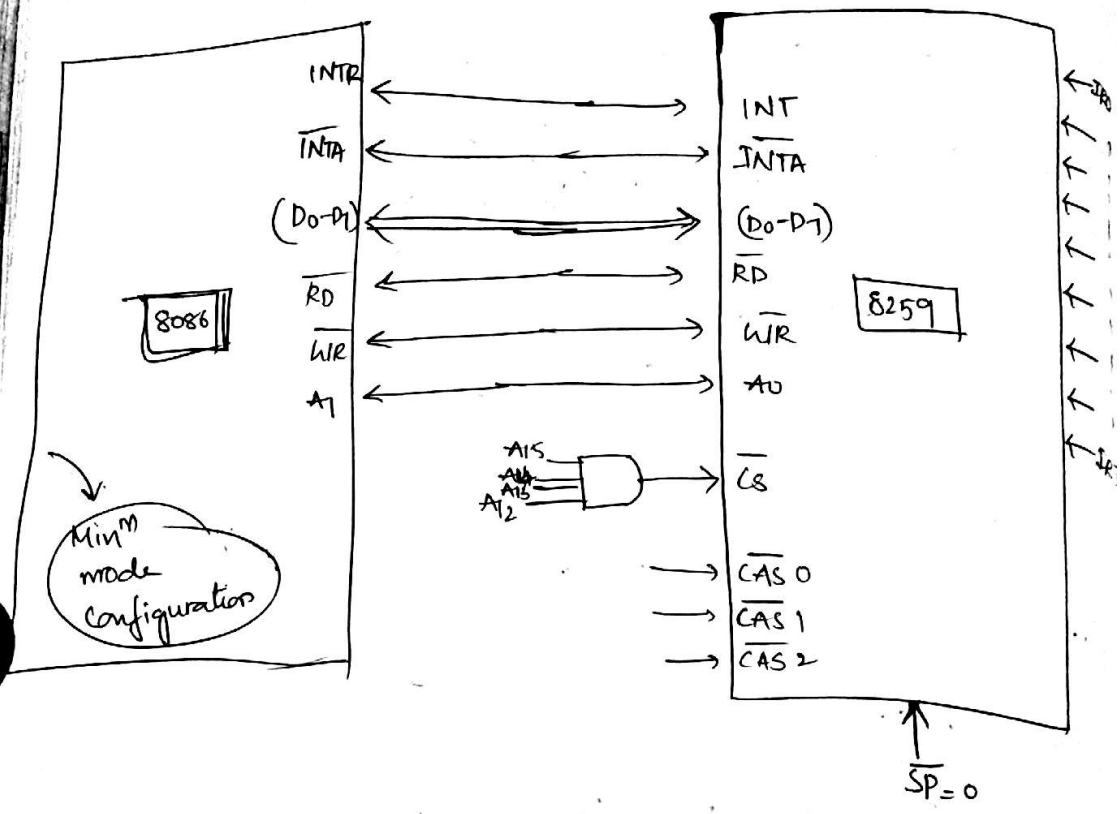
1. Non-Specific EOI: when 8259 receives this command it will reset the high priority IR level setbit of ISR.

2. Specific EOI: 8259 have 8 IR levels, each IR level can be specified by 3-bit address. when this command is given to 8259, it will specify the specified IR level of ISR

3. Automatic EOI: In response to first INTA pulse 8259 will set the corresponding IR level of ISR

and in response to 2nd $\overline{INTA}$ pulse, 8259 will reset the corresponding set bit of ISR by giving this command.

8259 Interfacing to 8086:



Command words: (CW) (7)

- Initialization Command words (ICW) (4)
  - ICW1
  - 2
  - 3
  - 4
- Operational Command words (OCW) (3)
  - OCW1
  - 2
  - 3

2 to 4 ICW are written (required) to initialize 8259 (i.e) to act as i/p & o/p)

ICW1:

7	6	5	4	3	2	1	0
x	x	x	1	LTM	x	SNGL	ICW4

if ICW4 is required → 1
not " → 0.

SNGL – single mode → 1 (only 1 8259 as slave mode)
Cascade mode → 0 (master mode)

LTM – level Triggered → 1
edge " → 0

ICW2:

T7	T6	T5	T4	T3	0	0	0

Interrupt Vector Address.

ICW3: → slave
→ Master

slave

0	0	0	0	0	ID2	ID1	ID0

Identification number.
of slaves

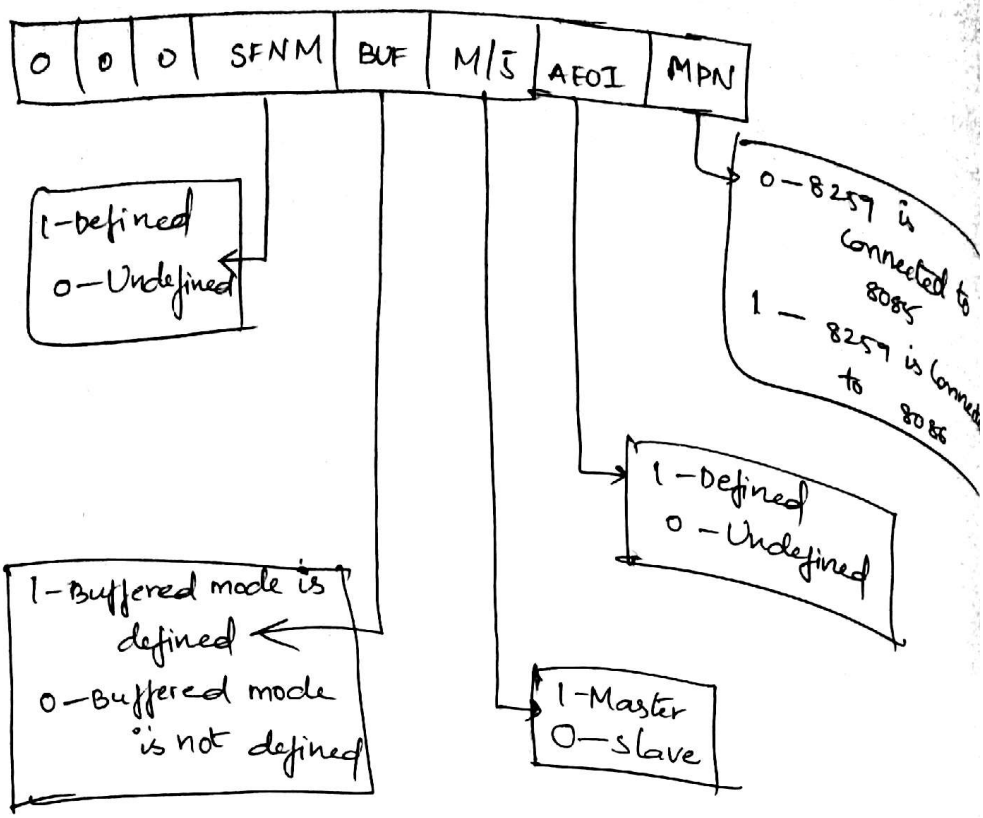
Master

SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

if all bits are '1', all slaves are connected

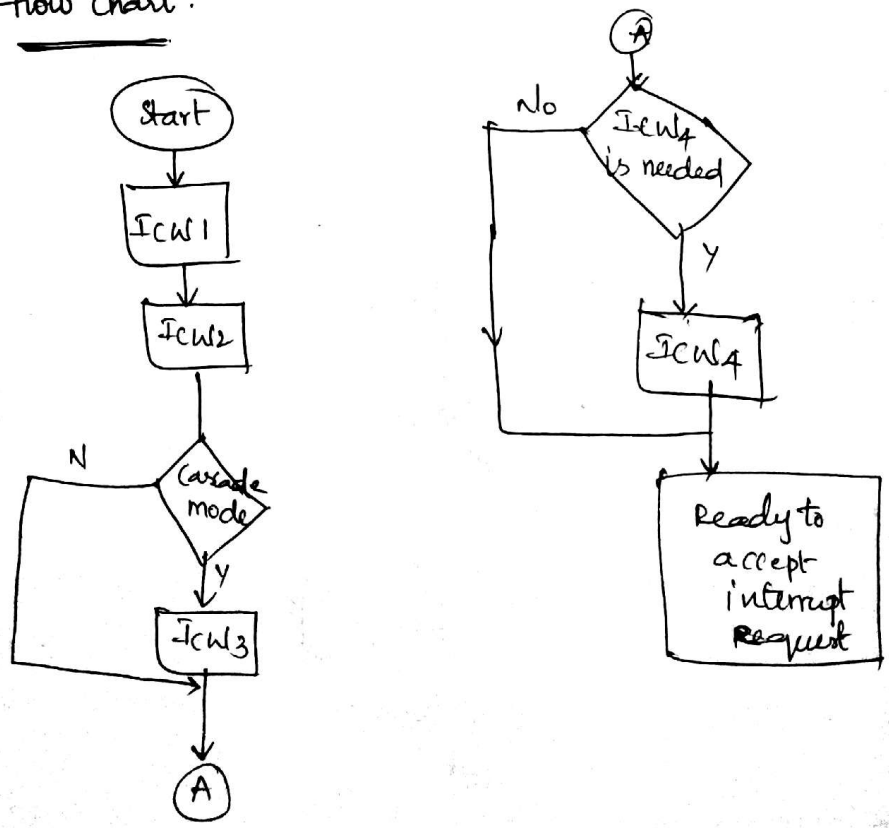
SL0 → 1 → slave 0 is connected
→ 0 → " " not "
⇒ SLn → 1 → slave n is connected
→ 0 → slave n is not connected.

ICW4:



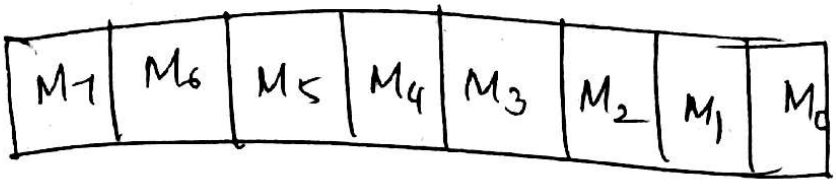
→ if 8259 is operated in cascade (master) mode, AEOI is required.

Flow chart:



OCW1:

It is programmed to mask the particular IR level



$M_7 \rightarrow 1 \rightarrow IR7$ is masked

$0 \rightarrow IR7$ is not masked.

$Mn \rightarrow 1 \rightarrow IRn$ is masked

$0 \rightarrow IRn$ is not masked.

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DMA Controller (8257)