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What happens when Gate = 1 in TMOD Register. (8051)

Mode control Regrester: (TMOD), (SFR address-89-H)

The mode control regrester TMOD of 8057 allows gating control even the timos, selects each timer for either timer or counter operation and sets one of the four modes of operation of the timers or counters. The

D7	D6'	pz	Dч	D 3	D2	bι	Do	
Sate 1	YT1	MI	Mo	hate o	CATO	М	Mo	

Timer/counters Timery counters

Try Bit definitions of 8051 Thop Register.

The upper whole of the TMOD Register is used for programming Timer 1 configuration while the lower mibble is used for programming timero configuration.

If a Bate both is '1' the nespective times or counter will have the Bate function activated. Into will act as Enput for Timer/Counter o colole INTI coll act as gate input for Temer/counter 1. If the gate but 98 1', the respective timer or counter will count up only of the INTO or INTI

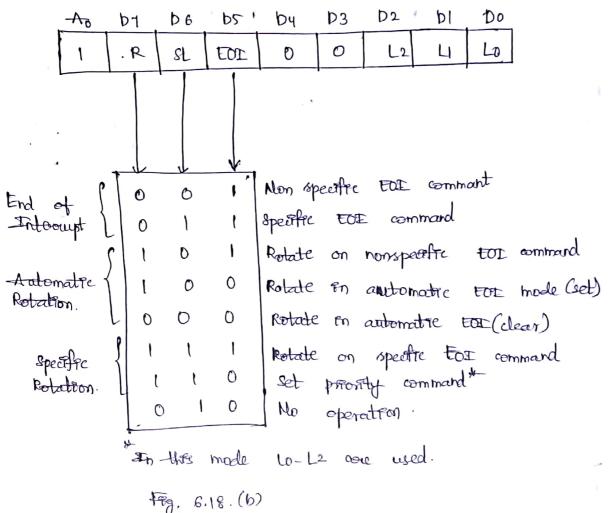
(For to or Ti) 98 hagh. It INT prin goes trigh low the counting will be withhold till the INT prin goes high. The hardware way of strating and stopping the times by an external source 93 activered by making GATE = 1 80 the TMOD Regrister.

Once 8259A & grotralised using the previously discussed

comments words for restratisation, it is nearly for its hormal function i.e. for accepting the intocupts but 82591 has the cun ways of handling the received intocupts called as modes of operation. These meter of operation can be selected by programming i.e. uniting three intound registors called as eperation command usered registors. The data unitten into them (bit pattorn) is called as operation command words. In those operation command coords. In those operation command coords occuls, occuls, every bit corresponds to some operational feature of the mode selected, except for the few bits those one either it or 3000.

In Debt och 2, the thouse bots, Mig. R, SL and EOST control the end of antesoupt, the notate mode and their combinations as shown in fig. b). The thouse bots L, L, and Ln Scanned by CamScanner

m och 2 detoimme the entompt level to be selected for operation, of the SL bit 95 active, ie.'1'. The details of och 2 agre shown on Fig. 6.18(b)



In operation command world 3 (occurs), the ESMM bit i.e.

Enable special Mast mode bit is set to "," the SMM bit

95 enabled to select or mask the special mask mode. When

ESMM bit is "o", the SMM bit is replected. If the SMM bit,

i.e. special Mask Mode bit is ", the 8259th will enter

special mask mode provided ESMM =1

THE ESMM=1 and SMM=0, the 8259th will section to

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-the normal mask mode. The details of bits of oeld3 core tog. 6.18(c) along with their bit defenitions. **D6** DC Dd Dy **b3** D2 D1 Do EMM SMM kk RIS No action. 0 1-Pall command No action 0 Reset Special Mask-s 0- No poll 0 Read IRR on Command spead Mask nent RD pube Read IRR on kent RD pulse