Analysis of Small-signal Transistor Amplifiers

On completion of this chapter you should be able to predict the behaviour of given transistor amplifier circuits by using equations and/or equivalent circuits that represent the transistor's a.c. parameters.

1 Reasons for Adopting this Technique

The gains of an amplifier circuit may be obtained by drawing the load lines on the plotted output characteristics. However, for a number of reasons, this is not a truly practical method.

(a) Manufacturers do not provide graphs or data to enable the characteristics to be plotted.
(b) Even if such data were available, the process would be very time consuming.
(c) Obtaining results from plotted graphs is not always very accurate—much depends upon the skill and interpretation of the individual concerned.

For these reasons an alternative method, which involves the use of equations and/or simple network analysis, is preferred. This method involves the use of the transistor parameters, the data for which is provided by manufacturers. This information is most commonly obtained from component catalogues produced by suppliers such as Radio Spares and Maplin Electronics.

2 BJT Parameters

You should already be familiar with the d.c. parameters such as input resistance (R_{IN}), output resistance (R_{OUT}), and current gain (h_{FE}), and their relationship to the transistor's output characteristics. In addition, an a.c. amplifier circuit may be redrawn in terms of the appearance of the circuit to a.c. signals. This is illustrated in Fig. 1.

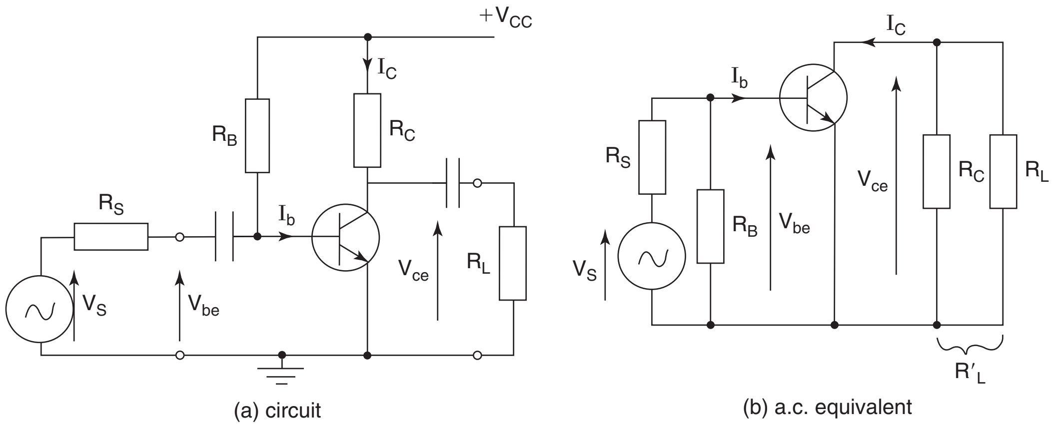

Fig. 1

The a.c. equivalent circuit of Fig. 1(b) is useful in that the current flow paths of the a.c. signal and the effective a.c. load can be appreciated, but in order to analyse the complete amplifier circuit the load lines would still need to be drawn on the characteristics. What is required is a simple network representation of the transistor itself, which can then be inserted into Fig. l(b) in place of the transistor symbol.

There are a variety of transistor parameters that may be used in this way. Amongst these are Z-parameters, Y-parameters, hybrid π parameters, and h-parameters. For the analysis of small-signal audio frequency amplifiers the use of h-parameters is the most convenient, and will be the method adopted here.

Provided that the transistor is correctly biased and the input signal is sufficiently small so as to cause excursions of currents and voltages that remain within the linear portions of the characteristics, then the transistor itself may be considered as a simple four-terminal network as shown in Fig. 2.

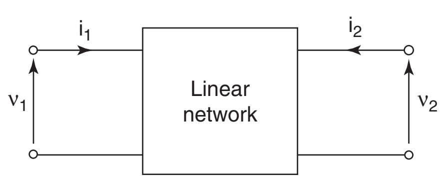

Fig. 2

The relationships between the four quantities of a linear network can be expressed by a number of equations, two of which are:

$$v_1 = Ai_1 + Bv_2 \;..................[1]$$
$$i_2 = Ci_1 + Dv_2 \;..................[2]$$

Examination of the units involved in these two equations reveals that A must be an impedance (ohm), B and C are dimensionless (ratios), and D must be an admittance (siemen). Since there is a mixture or hybrid of units involved, they are known as the hybrid or h-parameters, having the following symbols:

$$\text{A} = h_i \text{ ohm}; \quad \text{B} = h_r; \quad \text{C} = h_f; \quad \text{D} = h_o \text{ siemen}$$

If the transistor is conected in common emitter configuration the two equations would be written as follows

$$v_1 = h_{ie}i_1 + h_{re}v_2$$
$$i_2 = h_{fe}i_1 + h_{oe}v_2$$

If the transistor is connected in common base configuration then the parameters would be h_{ib}, h_{rb}, h_{fb} and h_{ob} respectively.

The h-parameters are defined as follows:

$\boldsymbol{h_i}$**:** is the input impedance with the output short-circuited to a.c.

Thus, $h_i = \dfrac{v_1}{i_1}$ ohm

$\boldsymbol{h_r}$**:** is the reverse voltage feedback ratio with the input open-circuited to a.c.

Thus, $h_r = \dfrac{v_1}{v_2}$

$\boldsymbol{h_o}$**:** is the output admittance with the input open-circuited to a.c.

Thus, $h_0 = \dfrac{i_2}{v_2}$ siemen

$\boldsymbol{h_f}$**:** is the forward current gain with the output short-circuited to a.c.

Thus, $h_f = \dfrac{i_2}{i_1}$

Notes:

1. In modern transistors h_r is very small ($<10^{-4}$) so this parameter will be ignored.
2. Just as conductance $G = 1/R$ siemen, so admittance, $Y = 1/Z$ siemen.
3. The h-parameters will vary with temperature, ageing and frequency. For the analysis at this level we shall consider that they remain constant.
4. Since the transistor is a current-operated device it is convenient to represent its collector circuit as a current generator with its 'internal' impedance ($1/h_o$) in parallel.

Considering the amplifier circuit of Fig. 1, the complete h-parameter equivalent circuit would be as shown in Fig. 3.

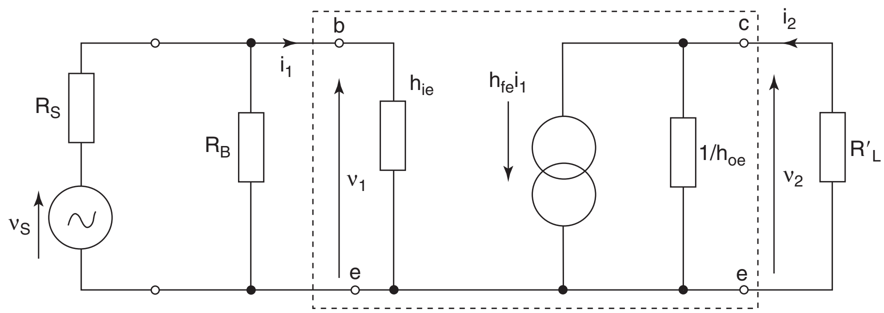

Fig. 3

For practical purposes it may be assumed that the h-parameters will have the same numerical values as their d.c. counterparts

$$\text{i.e. } h_i = R_{IN}; \quad h_f = h_F; \quad 1/h_o = R_{OUT}$$

3 h-parameter Equations

Ignoring h_r the original two equations may be written as:

$$v_1 = h_i i_1 \ldots\ldots\ldots\ldots[1]$$
$$i_2 = h_f i_1 + h_o v_2 \ldots\ldots\ldots\ldots[2]$$

and using these equations the following results can be obtained.

$$\text{Amplifier current gain, } A_i = \frac{h_f}{1 + h_o R'_L} \tag{1}$$

$$\text{Amplifier voltage gain, } A_v = \frac{h_f R'_L}{h_i(1 + h_o R'_L)} = \frac{A_i R'_L}{h_i} \tag{2}$$

Thus, knowing the values for a transistor's h-parameters, the prediction of amplifier gains can simply be obtained by either using the above equations or by simple network analysis using the h-parameter equivalent circuit.

Worked Example 1

Q **For the amplifier circuit of Fig. 4, (a) sketch the h-parameter equivalent circuit and, (b) determine the amplifier current and voltage gains using (i) network analysis, and (ii) h-parameter equations.**

The h-parameters are $h_{ie} = 1.5\,\text{k}\Omega$; $h_{fe} = 90$; $h_{oe} = 50\,\mu\text{S}$

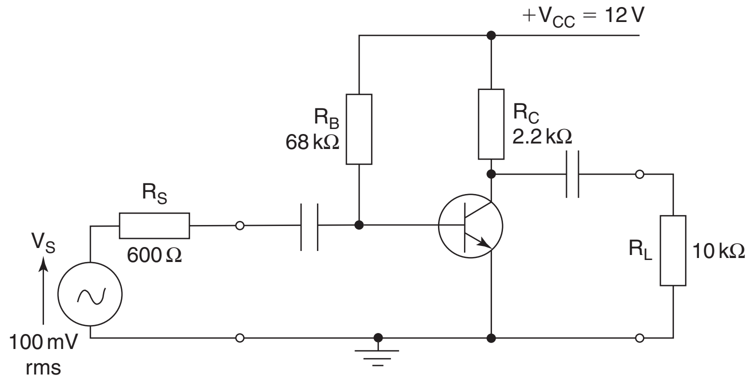

Fig. 4

A

$h_{ie} = 1.5\,\text{k}\Omega$; $h_{fe} = 90$; $h_{oe} = 50 \times 10^{-6}$ S

(a) The h-parameter circuit will be as shown in Fig. 5.

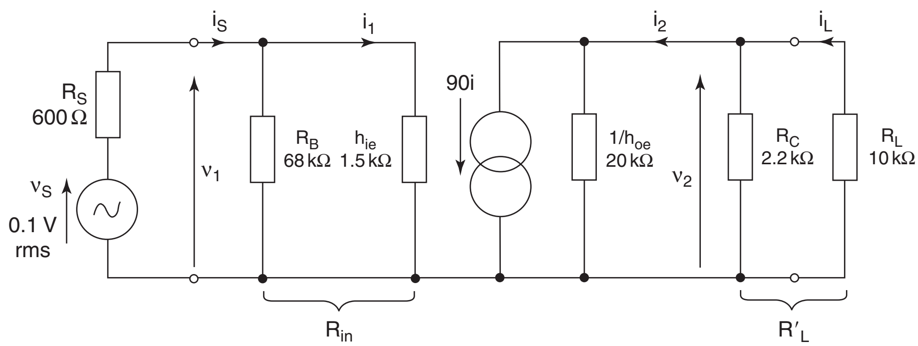

Fig. 5

(i) $1/h_{oe} = \dfrac{10^{-6}}{50} = 20\,\text{k}\Omega$; $R_L' = \dfrac{R_C R_L}{R_C + R_L}$ ohm $= \dfrac{2.2 \times 10}{2.2 + 10}$ kΩ $= 1.8$ kΩ

Input circuit: $R_{in} = \dfrac{h_{ie} R_B}{h_{ie} + R_B} = \dfrac{68 \times 1.5}{68 + 1.5} = 1.47\,\text{k}\Omega$

Using potential divider technique:

$$v_1 = \frac{R_{in}}{R_s + R_{in}} \times v_s \text{ volt} = \frac{1.47}{1.47 + 0.6} \times 0.1 \text{ V}$$

$$v_1 = 71 \text{ mV}$$

$$i_1 = \frac{v_1}{h_{ie}} = \frac{71 \times 10^{-3}}{1.5 \times 10^3} \text{ amp} = 47.3\,\mu\text{A}$$

Output circuit: $90 i_1 = 90 \times 47.3 \times 10^{-6} = 4.26$ mA

Using current divider technique:

$$i_2 = \frac{1/h_{oe}}{1/h_{oe} + R_L'} \times 90 i_1 \text{ amp} = \frac{20}{20 + 1.8} \times 4.26$$

$$i_2 = 3.91 \text{ mA}$$

$$v_2 = i_2 R_L' \text{ volt} = 4 \times 10^{-3} \times 1.8 \times 10^3$$
$$v_2 = 7.2 \text{ V}$$
$$A_i = \frac{i_2}{i_1} = \frac{3.91 \times 10^{-3}}{47.3 \times 10^{-6}} = 82.7 \textbf{ Ans}$$
$$A_v = \frac{v_2}{v_1} = \frac{7.04}{71 \times 10^{-3}} = 99 \textbf{ Ans}$$

(ii)
$$A_i = \frac{h_{fe}}{1 + h_{oe}R_L'} = \frac{90}{1 + (50 \times 10^{-6} \times 1800)}$$
$$A_i = \frac{90}{1.09} = 82.6 \textbf{ Ans}$$
$$A_v = \frac{A_i R_L'}{h_{ie}} = \frac{82.6 \times 1.8}{1.5}$$
$$A_v = 99 \textbf{ Ans}$$

Thus, allowing for the cumulation of rounding errors in part (i), the results from the equations agree with those from the network analysis.

The actual current that will flow in the load of the previous example will not in fact be i_2, but only a fraction of that, and is shown in Fig. 5 as i_L. Thus the power delivered to the external load will be less than the maximum possible. This problem may be minimised by the use of a matching transformer connected between the load and the amplifier circuit output terminals.

Worked Example 2

Q **The transistor used in the circuit of Fig. 6 has the following h-parameters $h_{ie} = 2\,\text{k}\Omega$; $h_{oe} = 60\,\mu\text{S}$; $h_{fe} = 100$. Calculate (a) the amplifier current gain, (b) the actual power delivered to the external load, and (c) the turns ratio required for a matching transformer in order to maximise the power delivered to the load.**

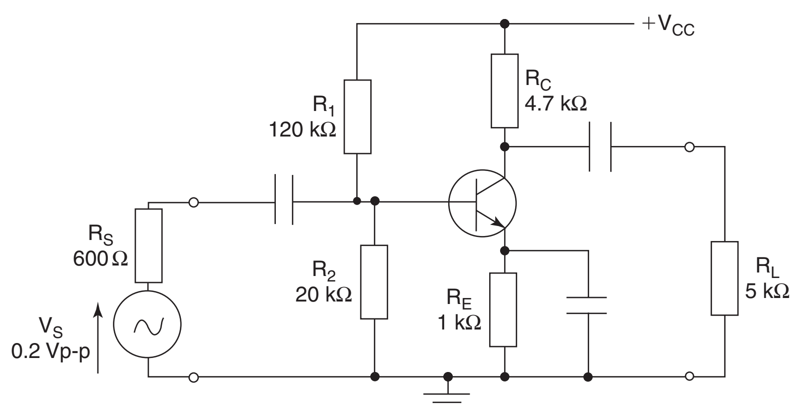

Fig. 6

A

$$h_{ie} = 2\,\text{k}\Omega;\ h_{oe} = 60 \times 10^{-6}\,\text{S};\ h_{fe} = 100$$

(a) The h-parameter equivalent circuit is shown in Fig. 7.

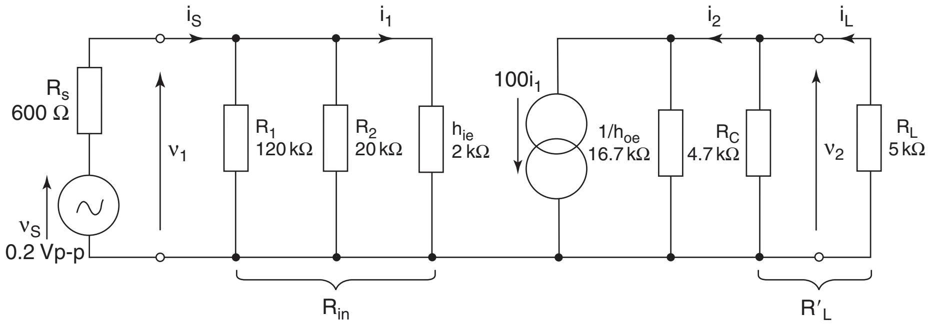

Fig. 7

Input circuit: $\dfrac{1}{R_{in}} = \dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{h_{ie}}$ siemen $= \dfrac{1}{120} + \dfrac{1}{20} + \dfrac{1}{2}$ mS

$$\frac{1}{R_{in}} = \frac{1+6+60}{120} = \frac{67}{120}\text{ mS}$$

so, $R_{in} = 1.79$ kΩ

$$v_1 = \frac{R_{in}}{R_s + R_{in}} \times v_s = \frac{1.79}{0.6 + 1.79} \times 200\text{ mV pk-pk}$$

$$v_1 = 150\text{ mV pk-pk}$$

$$i_1 = \frac{v_1}{h_{ie}}\text{ amp} = \frac{0.15}{2000} = 75\ \mu\text{A pk-pk}$$

Output circuit: $R'_L = \dfrac{R_C R_L}{R_C + R_L} = \dfrac{4.7 \times 5}{4.7 + 5}$ kΩ

$$R'_L = 2.42\text{ k}\Omega$$

$$100i_1 = 7.5\text{ mA pk-pk}$$

$$i_2 = \frac{1/h_{oe}}{1/h_{oe} + R'_L} \times 100i_1 = \frac{16.7}{16.7 + 2.42} \times 7.5\text{ mA pk-pk}$$

$$i_2 = 6.55\text{ mA pk-pk}$$

$$A_i = \frac{i_2}{i_1} = \frac{6.55 \times 10^{-3}}{75 \times 10^{-6}}$$

$A_i = 87.3$ **Ans**

Check: $A_i = \dfrac{h_{fe}}{1 + h_{oe}R'_L} = \dfrac{100}{1 + (60 \times 10^{-6} \times 2420)} = 87.3$

(b) $i_L = \dfrac{R_C}{R_C + R_L} \times i_2 = \dfrac{4.7}{9.7} \times 6.55$ mA pk-pk

$i_L = 3.17$ mA pk-pk

$P_L = I_L^2 R_L$ watt, where I_L is the **r.m.s.** value

so, $I_L = \dfrac{i_L}{2\sqrt{2}} = \dfrac{3.17}{2\sqrt{2}}$ mA $= 1.12$ mA

$$P_L = (1.12 \times 10^{-3})^2 \times 5000$$

$$P_L = 6.3 \text{ mW } \textbf{Ans}$$

(c) For maximum power transfer, R_L must match the parallel combination of $1/h_{oe}$ and R_c—call this R_p.

$$R_p = \frac{16.7 \times 4.7}{16.7 + 4.7} \text{ k}\Omega = 3.67 \text{ k}\Omega$$

$$R_p = \frac{N_p^2}{N_s} R_L \text{ ohm}$$

$$\text{so, } \frac{N_p}{N_s} = \sqrt{\frac{R_p}{R_L}} = \sqrt{\frac{3.67}{5}}$$

$$\frac{N_p}{N_s} = 0.856 : 1 \textbf{ Ans}$$

4 FET Parameters and Equivalent Circuits

Since a FET has an extremely high input impedance then its input circuit may be represented simply as an open circuit. Also, being a voltage operated device it is convenient to represent the output circuit as a voltage source with the internal resistance (r_{ds}) in series with it. The small-signal equivalent circuit will therefore be as shown in Fig. 8. The FET parameters r_{ds} and g_m should already be familiar to you.

From Fig. 8: $V_o = \dfrac{R_L'}{R_L' + r_{ds}} \times g_m r_{ds} V_i$ volt

$$\frac{V_o}{V_i} = A_v = \frac{g_m r_{ds} R_L'}{R_L' + r_{ds}} \tag{3}$$

but in practice, $r_{ds} \gg R_L'$, so

$$\frac{V_o}{V_i} = \frac{g_m r_{ds} R_L'}{r_{ds}}$$

$$\text{and, } A_v = g_m R_L' \tag{4}$$

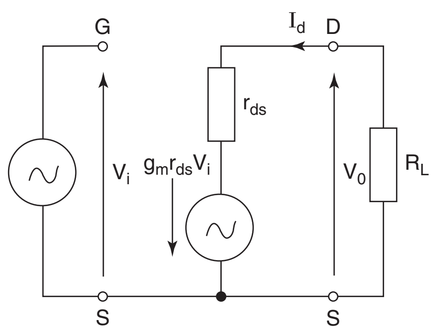

Fig. 8

Worked Example 3

Q **The FET used in the amplifier circuit of Fig. 9 has parameter values of $r_{ds} = 80\,\text{k}\Omega$ and $g_m = 4\,\text{mS}$. Calculate (a) the amplifier voltage gain, and (b) the effective input resistance of the amplifier circuit.**

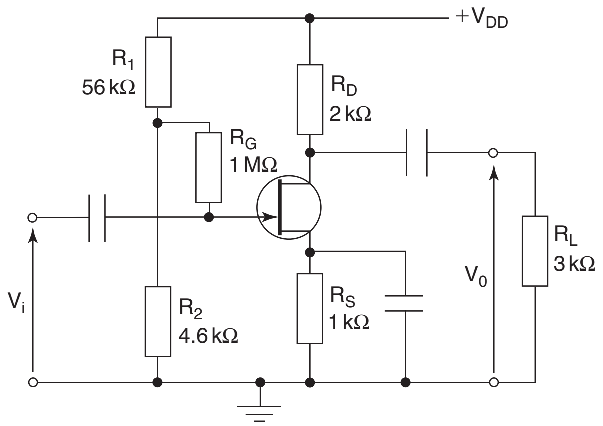

Fig. 9

A

$$r_{ds} = 80 \times 10^3\,\Omega;\ g_m = 4 \times 10^{-3}\,\text{S};\ R_L = 3\,\text{k}\Omega$$

(a) For this circuit, the effective a.c. load, $R_L' = \dfrac{R_D R_L}{R_D + R_L}$ ohm $= \dfrac{3 \times 2}{5}$ kΩ

$$R_L' = 1.2\ \text{k}\Omega$$

and since $r_{ds} \gg R_L'$, then equation (4) may be used

$$\text{so, } A_v = g_m R_L' = 4 \times 10^{-3} \times 1.2 \times 10^3$$

$A_v = 4.8$ **Ans**

In order to check the validity of using the approximation of equation (4), we can also calculate the gain using equation (3) and compare the two answers.

$$\text{Thus, } A_v = \frac{g_m r_{ds} R_L'}{r_{ds} + R_L'} = \frac{4 \times 10^{-3} \times 80 \times 10^3 \times 1.2 \times 10^3}{80 \times 10^3 + 1.2 \times 10^3} = \frac{384\ 000}{81\ 200}$$

$A_v = 4.73$, which confirms the validity of equation (4)

Note that a FET amplifier provides very much less voltage gain than a comparable BJT amplifier.

(b) Looking in at the input terminals, for a.c. signals, the gate resistor R_G is in series with the parallel combination of R_1 and R_2, as shown in Fig. 10.

$$R_{in} = R_G + \frac{R_1 R_2}{R_1 + R_2}\ \text{ohm} = 10^6 + \frac{56 \times 4.7}{60.7}$$

$R_{in} = 1.0043\ \text{M}\Omega$ **Ans** (say 1 MΩ)

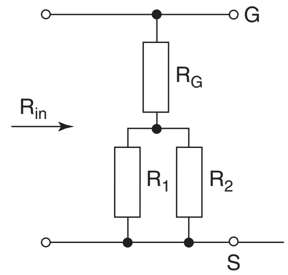

Fig. 10

Thus, the inherently high input resistance of the FET is preserved in the amplifier circuit by the inclusion of R_G.

5 Practical Implications

It should be borne in mind that when designing an amplifier circuit, the results of the equations as shown in this chapter give **only theoretical** answers. If an amplifier circuit thus analysed is then constructed and tested, the actual gain figures achieved may well be different to those predicted. There are a number of reasons for this: the resistors will have actual values depending upon how close to tolerance they are, and the transistor parameters cannot be guaranteed to be exactly those quoted by the manufacturer. Indeed, manufacturers recognise this by quoting minimum, maximum and typical values for such parameters as h_f. In calculations the typical value is normally used. Thus the mathematical analysis should be considered as only the first step in the design process, and component values will then need to be adjusted in the light of practical tests.

Summary of Equations

BJT amplifier: Current gain, $$A_i = \frac{h_f}{1 + h_o R_L'}$$

Voltage gain, $$A_v = \frac{A_i R_L'}{h_i}$$

Power gain, $$A_p = A_i A_v$$

FET amplifier: Approx. voltage gain, $$A_v = g_m R_L'$$

or, more accurately, $$A_v = \frac{g_m r_{ds} R_L'}{r_{ds} + R_L'}$$

Assignment Questions

1 The h-parameters for the transistor used in the circuit of Fig. 11 are $h_{fe} = 250$, $h_{ie} = 5\,\text{k}\Omega$, and $h_{oe} = 40\,\mu\text{S}$.

(a) sketch the h-parameter equivalent circuit and hence, or otherwise,

(b) calculate the amplifier current, voltage and power gains.

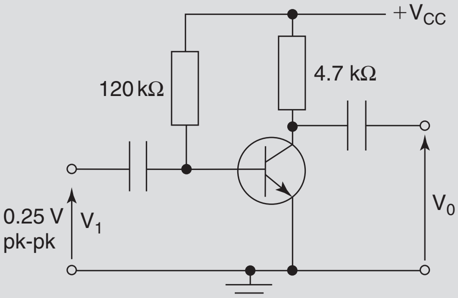

Fig. 11

2 The circuit of Fig. 11 is now reconnected so that the transistor is connected in common base configuration. If the common base parameters h_{ib} and h_{ob} are $100\,\Omega$ and $20\,\mu\text{S}$ respectively,

(a) sketch the equivalent circuit, and

(b) calculate the amplifier current, voltage and power gains.

3 Figure 12 shows a simply biased common source FET amplifier, where the transistor parameters are $g_m = 3\,\text{mS}$, and $r_{ds} = 75\,\text{k}\Omega$. Calculate the amplifier voltage gain.

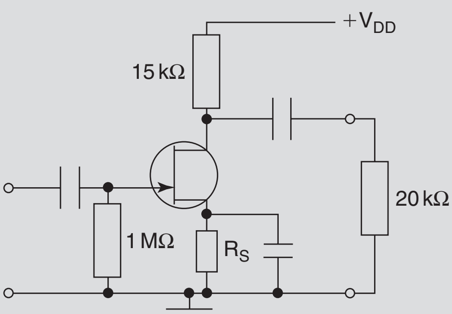

Fig. 12

4 The transistor of the amplifier circuit shown in Fig. 13 has the following parameters: $h_{ie} = 2.5\,\text{k}\Omega$, $h_{fe} = 120$, and $h_{oe} = 100\,\mu\text{S}$. Sketch the equivalent circuit and determine the amplifier current and voltage gains, and the power dissipated in the external $7.5\,\text{k}\Omega$ load.

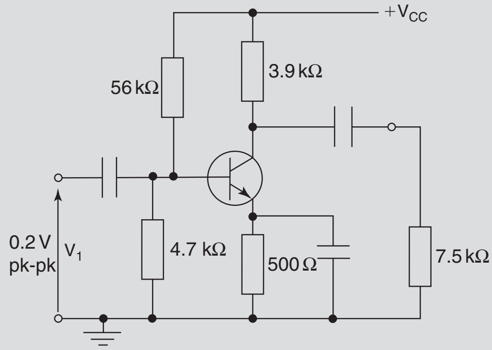

Fig. 13

5 The parameters for the FET in Fig. 14 are $r_{ds} = 85\,\text{k}\Omega$ and $g_m = 4.1\,\text{mS}$.

(a) calculate the amplifier voltage gain, and

(b) the power dissipated in the external $15\,\text{k}\Omega$ load.

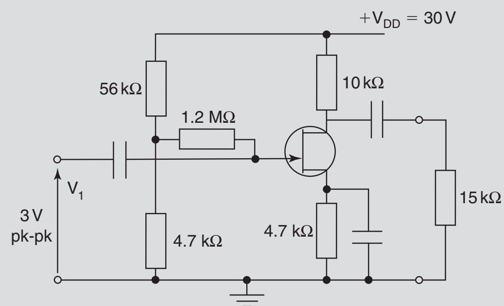

Fig. 14

6 For the two equivalent circuits shown in Figs. 15(a) and (b), sketch the amplifier circuits that they represent, showing component values, and also identify the values for the transistor parameters in each case.

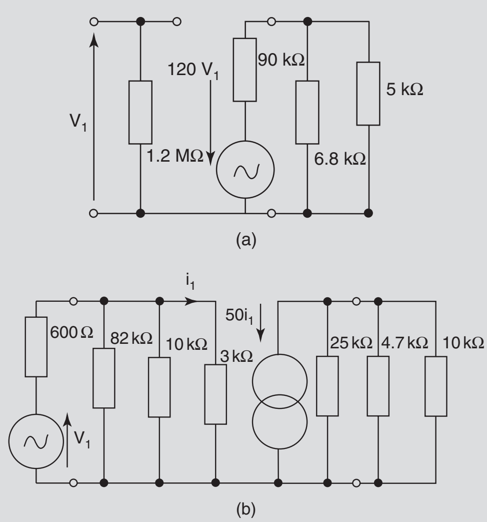

Fig. 15

Supplementary Worked Example 1

Q **Calculate the minimum value of h_{fe} required for the transistor in Fig. 16 in order that a power of 3.5 mW is dissipated in the 10 kΩ load resistor. The values for h_{ie} and h_{oe} are 4 kΩ and 50 μS respectively.**

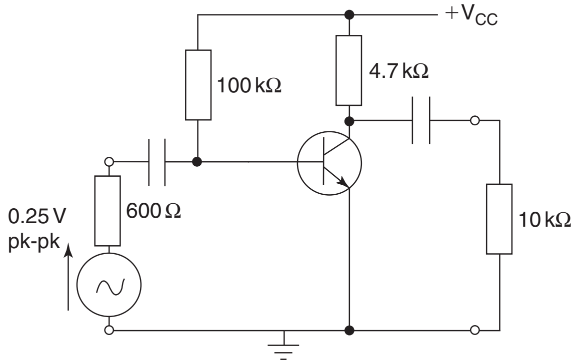

Fig.16

A

The h-parameter equivalent circuit is shown in Fig. 17. Since $R_B \gg h_{ie}$ then the shunting effect of R_B will be negligible, and it has therefore been omitted from the calculation.

$h_{ie} = 4000\,\Omega$; $h_{oe} = 50 \times 10^{-6}$ S; $V_i = 0.25$ V pk-pk; $P_o = 3.5 \times 10^{-3}$ W

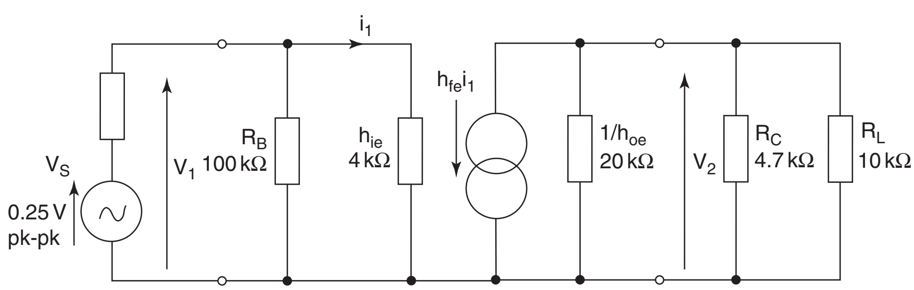

Fig. 17

$$P_0 = \frac{V_2^2}{R_L} \text{ watt so } V_2 = \sqrt{P_0 R_L} \text{ volt} = \sqrt{3.5 \times 10^{-3} \times 10^4}$$

$$V_2 = 5.916 \text{ V}$$

$$V_1 = \frac{h_{ie}}{h_{ie} + R_s} \times V_s \text{ volt pk-pk} = \frac{4}{4.6} \times 0.25$$

$$V_1 = 0.217\text{V pk-pk}$$

$$\text{so, } V_1 = \frac{0.217}{2\sqrt{2}} = 76.8\text{mV r.m.s.}$$

$$\text{Voltage gain required, } A_v = \frac{V_2}{V_1} = \frac{5.916}{0.768}$$

$$A_v = 77$$

$$A_v = \frac{h_{fe}R_L'}{h_{ie}(1 + h_{oe}R_L')} \text{ where } R_L' = \frac{1/h_{oe} \times R_L}{1/h_{oe} + R_L} = \frac{47}{14.7} = 3.2\ \text{k}\Omega$$

$$\text{so, } h_{fe} = \frac{A_v\{h_{ie}(1 + h_{oe}R_L')\}}{R_L'} = \frac{77\{4(1 + 50 \times 10^{-6} \times 3.2 \times 10^3)\}}{3.2}$$

$$h_{ie} = 112 \ \textbf{Ans}$$

Supplementary Worked Example 2

Q **The FET in the circuit of Fig. 18 has $r_{ds} = 50\,\text{k}\Omega$ and $g_m = 5\,\text{mS}$. Determine the value of the output voltage, V_2, and the power developed in the 25 kΩ load.**

A

$r_{ds} = 50 \times 10^3\,\Omega$; $g_m = 5 \times 10^{-3}$ S

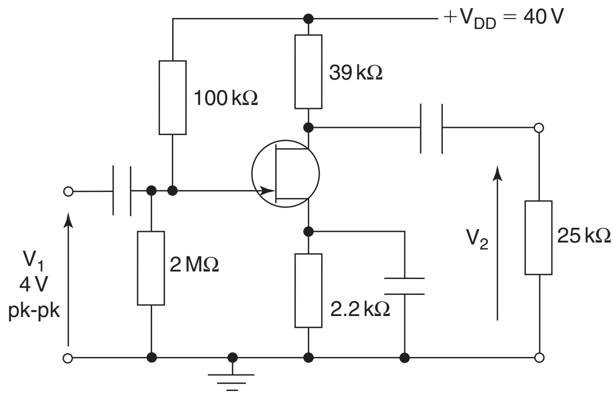

Fig. 18

$$R_L' = \frac{R_D R_L}{R_D + R_L} \text{ ohm} = \frac{25 \times 3.9}{25 + 3.9} = 15.2\ \text{k}\Omega$$

Now, since r_{ds} is NOT $\gg R_L'$, then the approximate equation for voltage gain should not be used, hence

$$A_v = \frac{g_m r_{ds} R_L'}{r_{ds} + R_L'} = \frac{1.5 \times 10^{-3} \times 50 \times 10^3 \times 15.2 \times 10^3}{65.2}$$

$$A_v = 17.48$$

$$\text{Thus, } V_2 = 17.48 \times 4 \text{ V pk-pk} = 70 \text{ V pk-pk}$$

$$\text{so, } V_2 = 24.75 \text{ V } \textbf{Ans}$$

$$P_0 = \frac{V_2^2}{R_L} \text{ watt} = \frac{24.75^2}{25 \times 10^3}$$

$$P_0 = 0.2 \text{ mW } \textbf{Ans}$$

Note that had the approximate equation $A_v = g_m R_L'$ been used in this case an error of about 22% would have resulted in the value for A_v. This would be an unacceptably large error.

The approximate form of the equation should be used only when r_{ds} is **at least** 10 times larger than R_L'.

Answers to Assignment Questions

1 **(b)** $A_i = 210$; $A_v = 197$; $A_p = 41\ 370$
2 **(b)** $A_i = 0.91$; $A_v = 42.8$; $A_p = 39$
3 25.7
4 $A_i = 95.5$; $A_v = 98.1$; $P_o = 6.5\,\mathrm{mW}$
5 $A_v = 24.6$; $P_o = 45.4\,\mathrm{mW}$