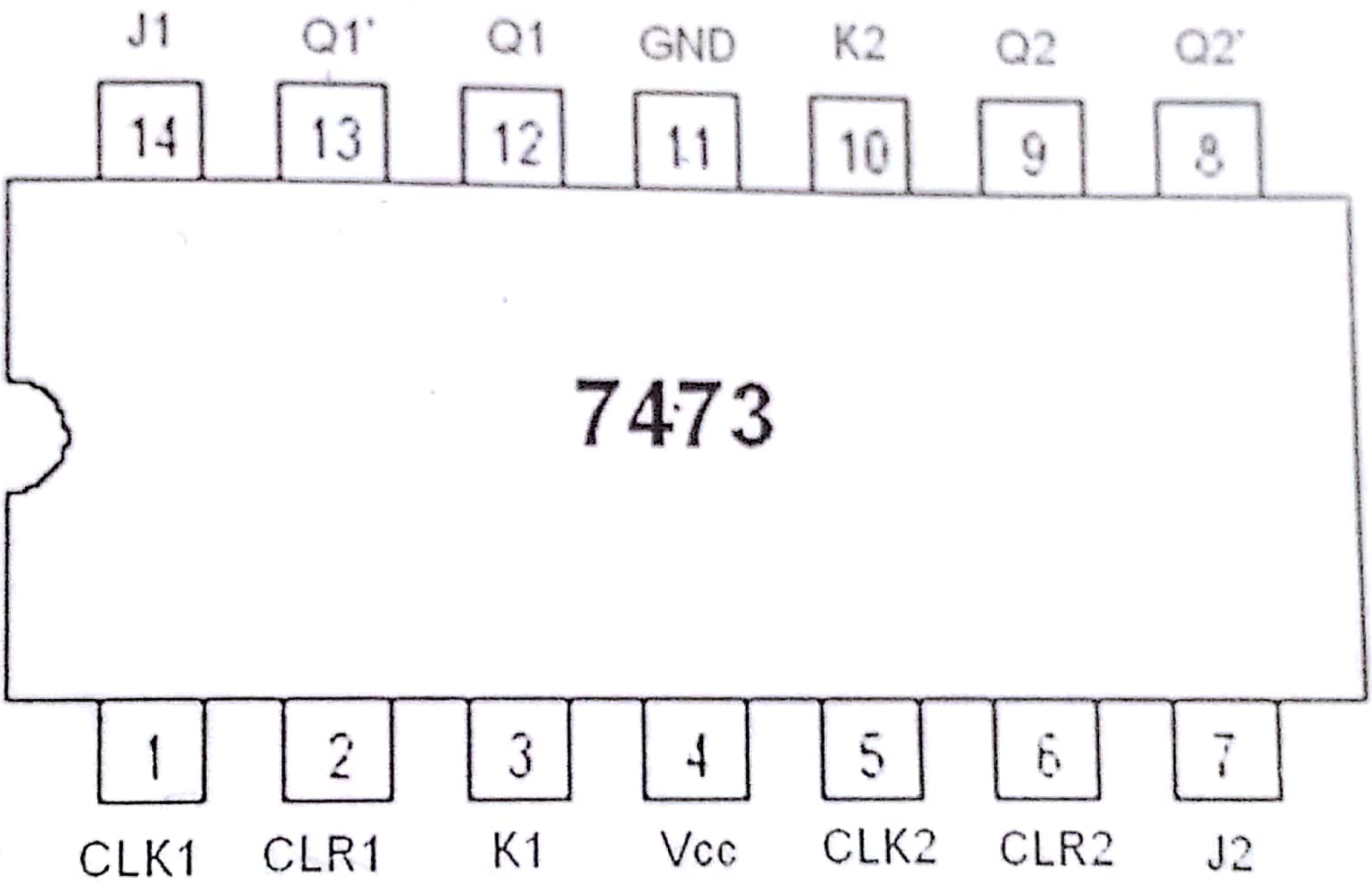
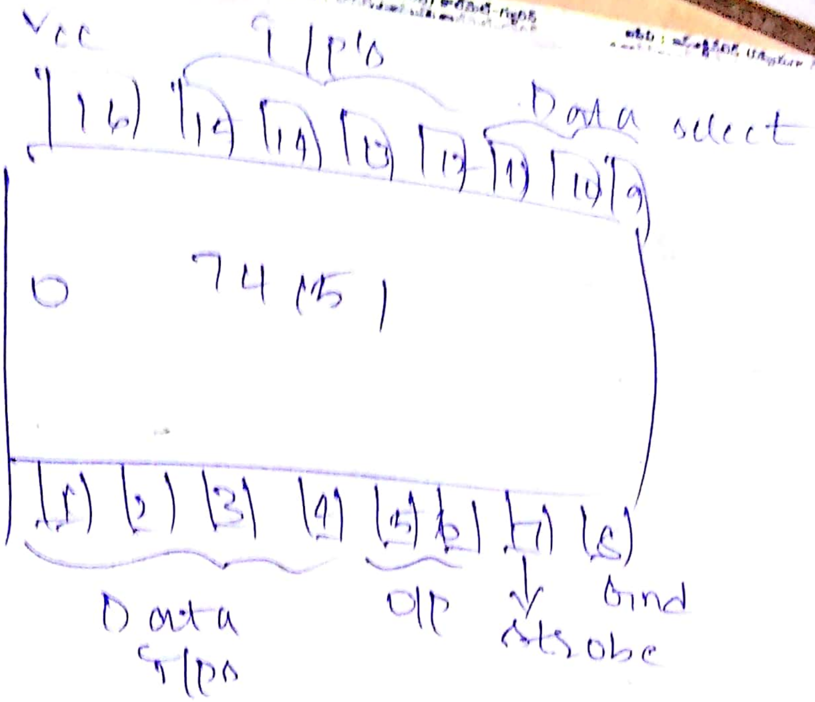
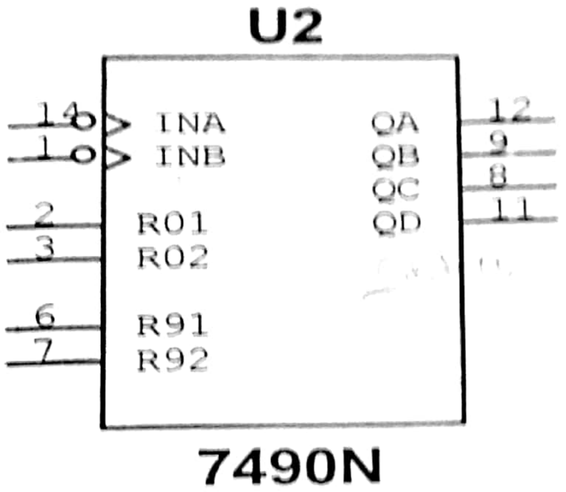

J1
Q1'
Q1
GND
K2
Q2
Q2'
14
13
12
11
10
9
8
7473
1
2
3
4
5
6
7
CLK1
CLR1
K1
Vcc
CLK2
CLR2
J2




~~CMOS~~ ~~TTL~~

**Linearity** :- A system is said to be linear if the changes in i/p measurement are proportional to the changes in o/p measurement.

CIRCUIT :



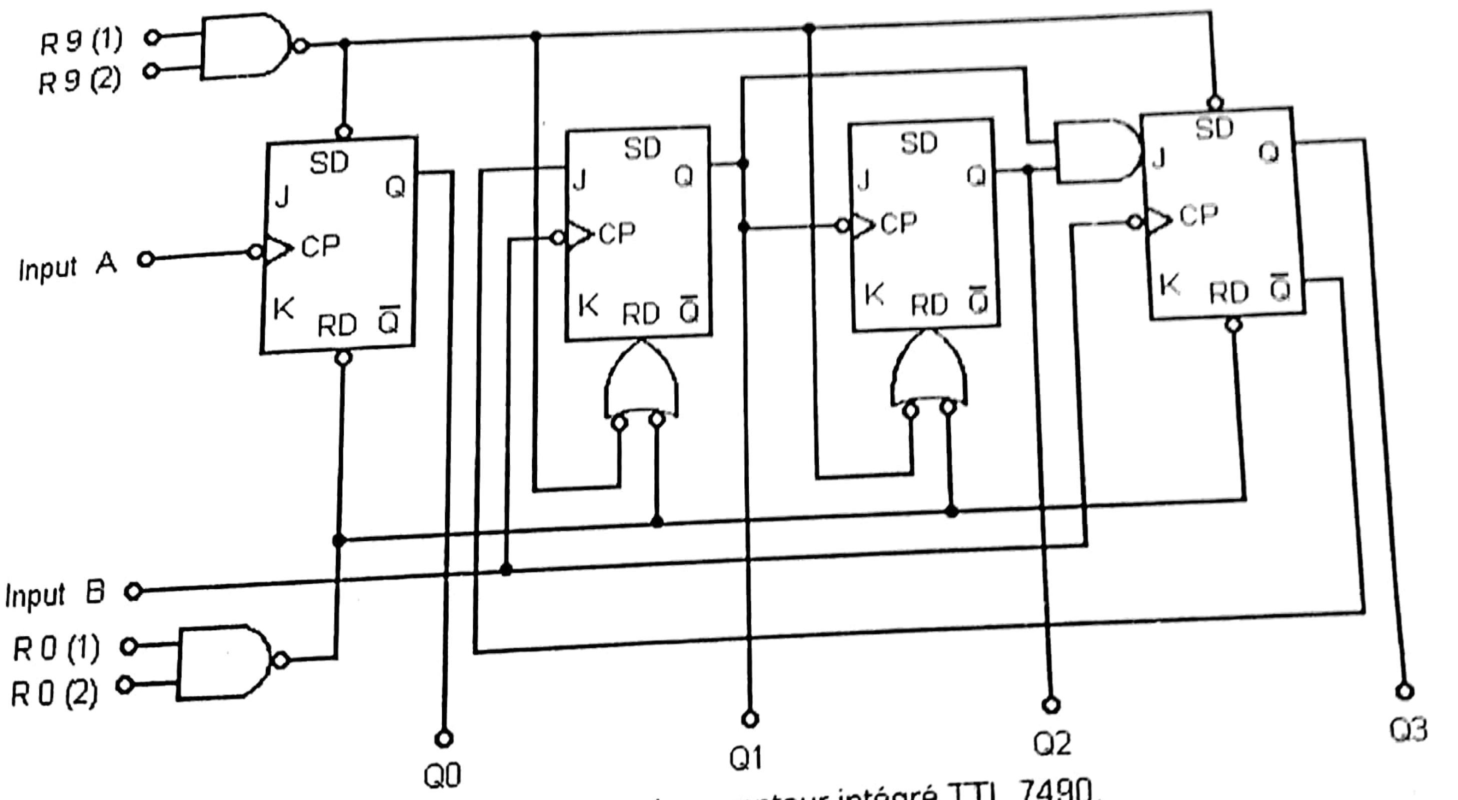
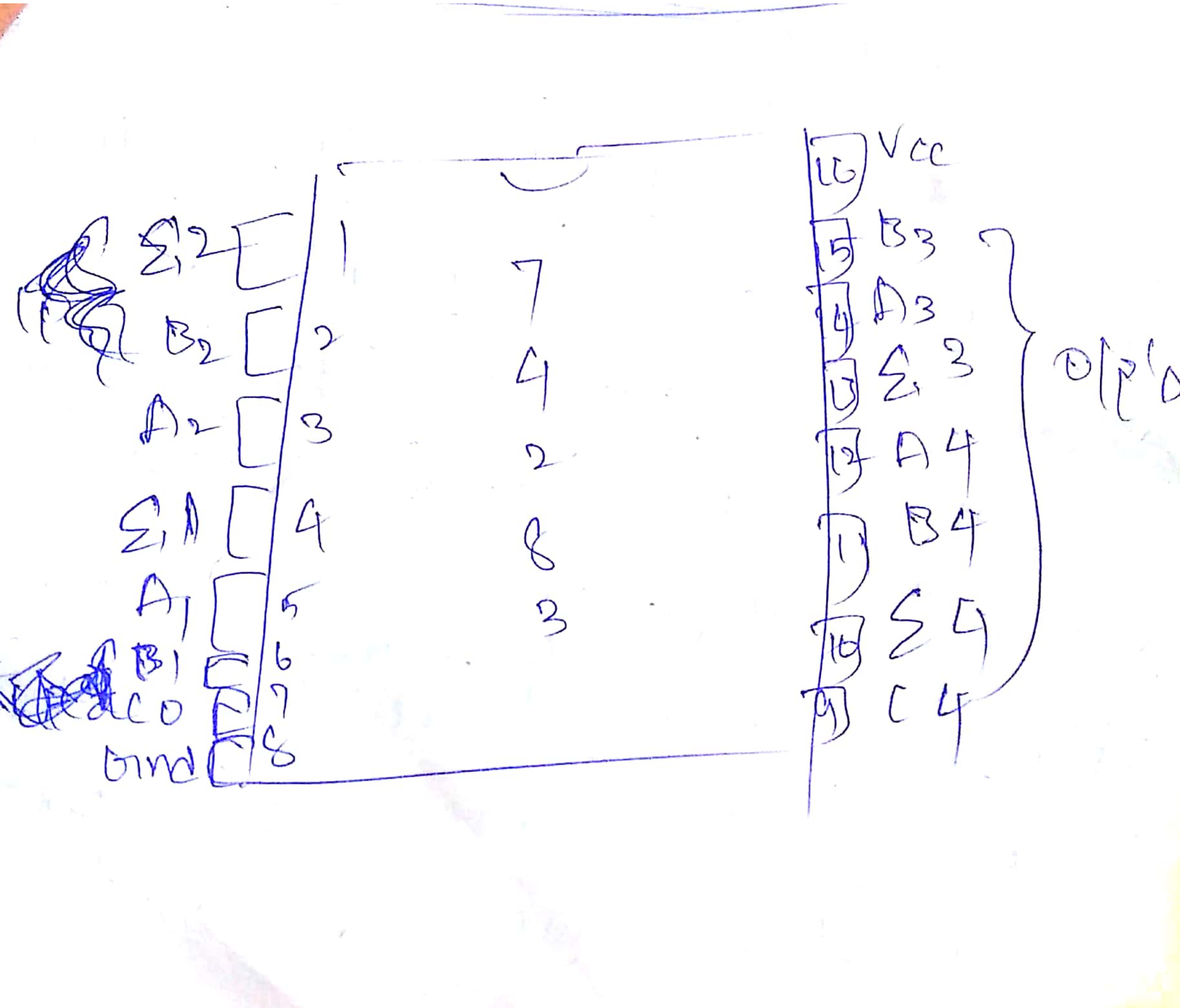




Fig. 37. - Schéma du compteur intégré TTL 7490.


7483
Σ2
B2
A2
Σ1
A1
B1
C0
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
Vcc
B3
A3
Σ3
A4
B4
Σ4
C4
O/P's

$V_O$ = O/P ...

The resolution takes care of changes in the input.

Accuracy:

It is a comparison of actual output voltage with expected output. It is expressed in percentage. Ideally, the accuracy of DAC should be, at worst $\pm \frac{1}{2}$ of its LSB. If the full scale O/P voltage is 10.2 V then for an 8-bit DAC accuracy can be given as

$$\text{Accuracy} = \frac{V_{O\,FS}}{(2^n-1) \times 2}$$

$$= \frac{10.2}{255 \times 2} = 20\ mV$$

... monotonicity of ...

A DAC (Digital to Analog converter) accepts an n-bit binary input word $b_1, b_2, b_3 \ldots b_n$ in binary and produce an analog signal proportional to it. Fig. shows circuit symbol and input - output characteristics of a 4 bit DAC. There are four digital inputs, indicating 4-bit DAC. Each digital input requires an electrical signal representing either a logic 1 or a logic 0. The $b_n$ is the least significant bit, LSB, whereas $b_1$ is the most significant bit, MSB.

Performance Parameters of DAC :-

The various performance parameters of DAC are,

1. Resolution :

Resolution is defined in two ways.

i) Resolution is the number of different analog output values that can be provided by a DAC. For an n-bit DAC

$$\text{resolution} = 2^n$$

ii) Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n-bit DAC it can be given as

$$\text{resolution} = \frac{V_{OFS}}{2^n - 1}$$

where $V_{OFS}$ = full scale output voltage

For an 8-bit DAC resolution can be given as

$$\text{Resolution} = 2^n = 2^8$$
$$= 256$$

If the full scale o/p voltage is 10.2 V then by second definition the resolution for an 8-bit DAC can be given as

$$\text{resolution} = \frac{V_{OFS}}{2^n - 1}$$

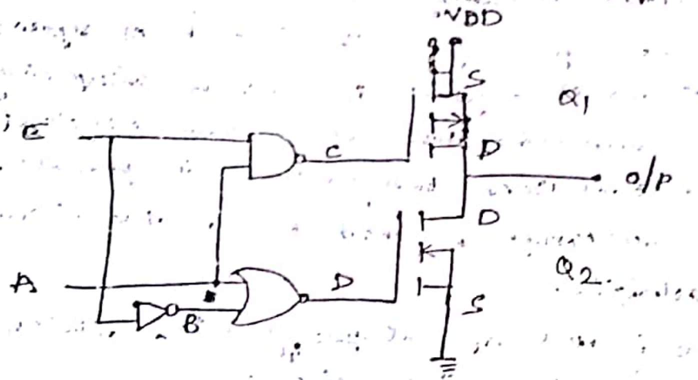
$$= \frac{10.2}{2^8 - 1} = \frac{10.2}{255} = 40 \text{ mV/LSB}$$

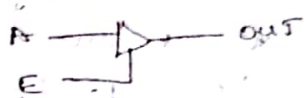
we say that i/p change of 1 LSB causes o/p to change by 40 mV.

are High
d be
cut-off ; k
connected

## Three State outputs :

A circuit diagram for a CMOS three state buffer is shown




To simplify the diagram, NAND, NOR and inverter functions are shown in functional rather than in MOS form.

when Enable input is High, depending on A value the circuit behave as a buffer.

| E | A | B | C | D | $Q_1$ | $Q_2$ | o/p |
|---|---|---|---|---|---|---|---|
| H | L | L | H | H | OFF | ON | L |
| H | H | L | L | L | ON | OFF | H |
| L | L | H | H | L | OFF | OFF | Hi-Z |
| L | H | H | H | L | OFF | OFF | Hi-Z |

when Enable input is LOW, both outputs MOSFET's are Off and the output is in the Hi-Z state.

**CMOS compared to TTL:**

- CMOS components are typically more expensive than TTL equivalents. However, CMOS technology is usually less expensive on a system level due to CMOS chips being smaller and requiring less regulation.
- CMOS circuits do not draw as much power as TTL circuits while at rest. However, CMOS power consumption increases faster with higher clock speeds than TTL does. Lower current draw requires less power supply distribution, therefore causing a simpler and cheaper design.
- Due to longer rise and fall times, the transmission of digital signals becomes simpler and less expensive with CMOS chips.
- CMOS components are more susceptible to damage from electrostatic discharge than TTL components.