unit - 1

P-n junction Diode.

Qualitative Theory of the p-n junction:

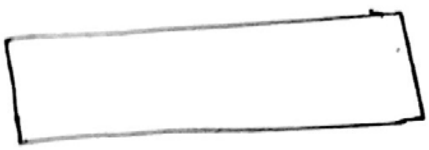
If donor impurities are introduced in to one side and acceptors in to the otherside of a single crystal of a semiconductor, say germanium, a p-n junction is formed. In the fig(a), The donor ion is indicated schematically by a plus sign because, after this impurity atom "donates" an electron, It becomes a positive ion. The acceptor ion is indicated by a minus sign because, after this atom accepts an electron, it becomes a negative ion. Initially There are nominally only p-type carriers to the left of the Junction and only n type carrier to the right. Because there is a density gradient across the junction, holes will diffuse to the right across the junction and electrons to the left

Therefore anet negative charge is Established on the p-side and a net positive charge is established on the N side (As aresult junction formed) This net negative on the Pside Prevents futher diffusion of electrons In to the Pside. similarly the net positive charge on the NSide repels the holes crossing from Pside to Nside.

Thus a potential barrier is setup near the junction which prevents further movement of charge carries. An Electric field across the depletion layer an electrostatic

Potential difference is established between P and N regions, which is called as potential barrier or junction barrier.
The Potential barrier varies with doping levels and temperature 0.3V for Germanium & 0.72 V for silicon.

1. Intrinsic material Ge or Si

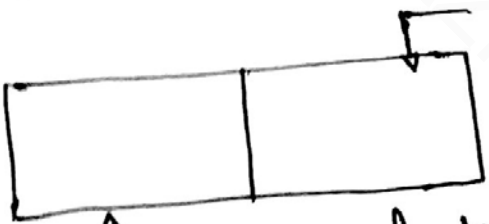


→ Germanium semiconductor.

2. Add Pentavalent atoms to form N type, Add trivalent atoms to form P type.

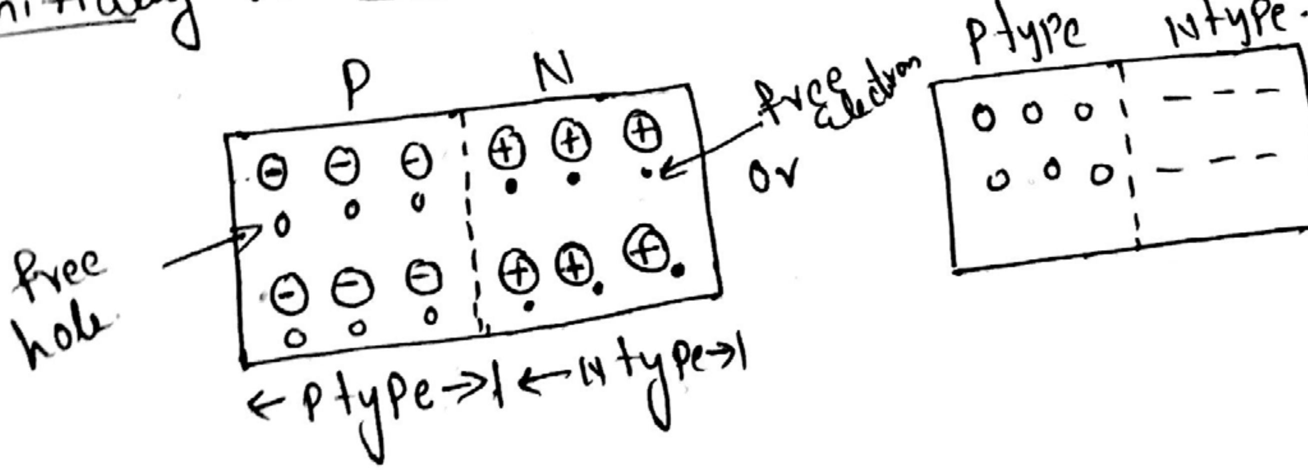
Pentavalent impurities → arsenic, antimony, Phosphorous
Trivalent impurities → Aluminium or born.

(Add) doping of pentavalent

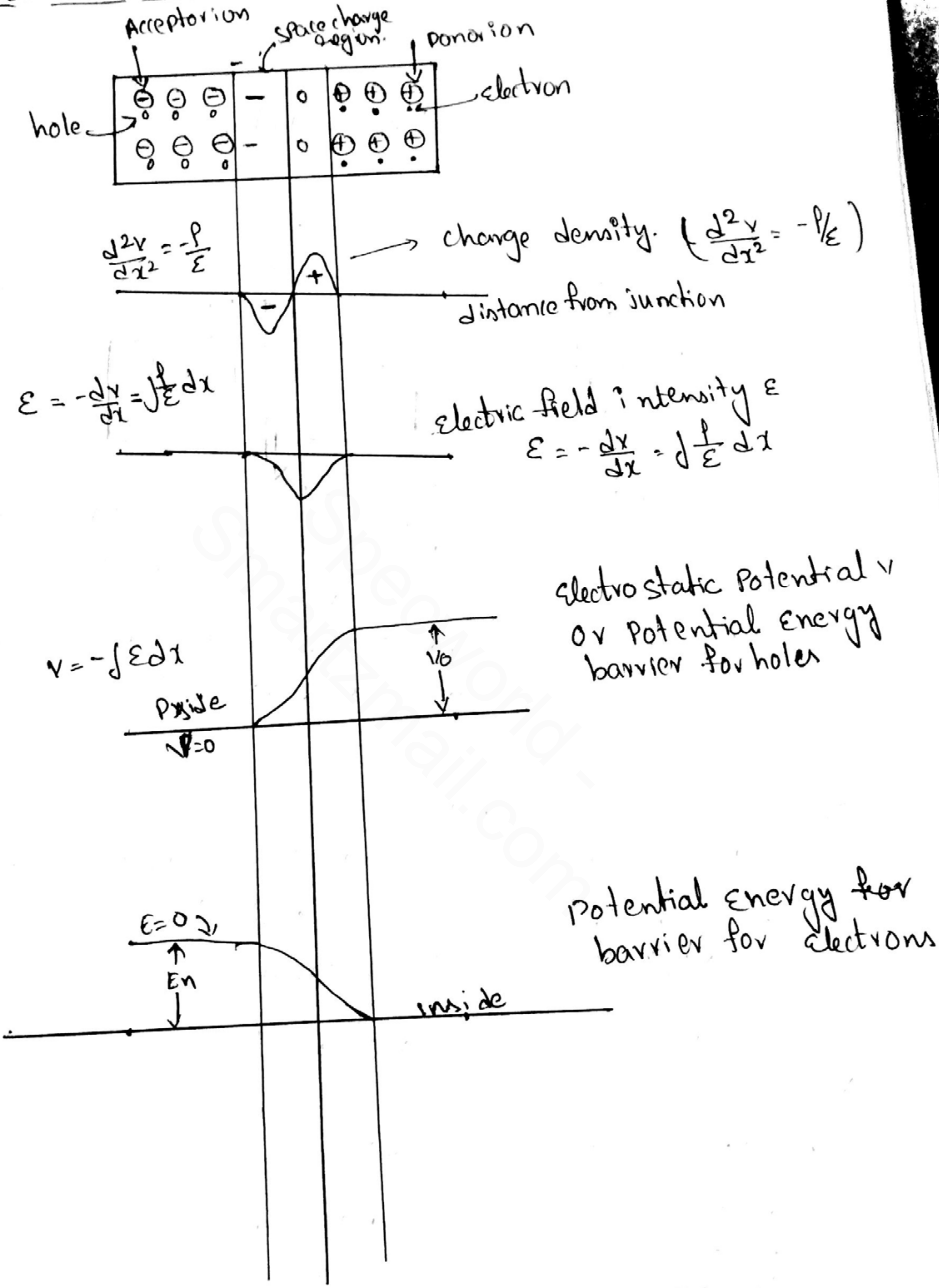


↑ doping of trivalent

Initially or Before diffusion:



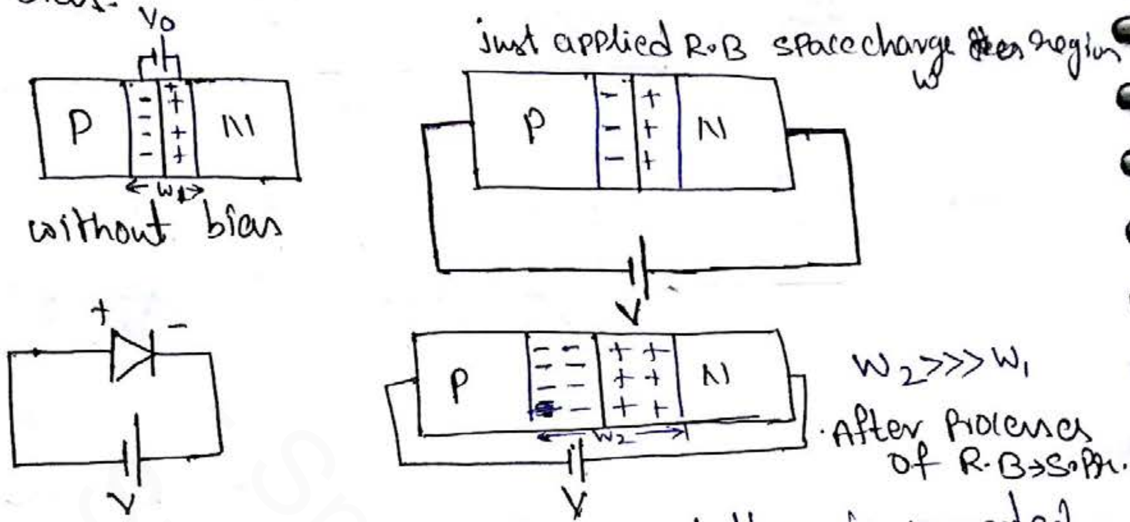
After diffusion or junction (p-n).



P-N Junction as a Diode:

The essential electrical characteristic of a p-n junction is that it constitutes a diode which permits the easy flow of current in one direction but restrains the flow in the opposite direction.

Reverse bias:



when the negative terminal of the battery is connected to the P side of the junction and positive terminal to the n side.

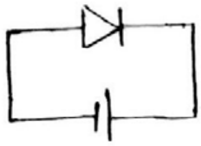
operation in Reverse bias:

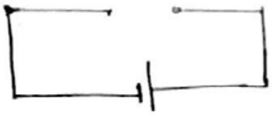
The polarity of connection is such as to cause both the holes in the P type and the electrons in the n type to move away from the junction.

consequently the regions of negative charge density is spread to the left of the junction, and positive charge density region is spread to the right. so the width of the depletion region increases. so no current through majority carriers.

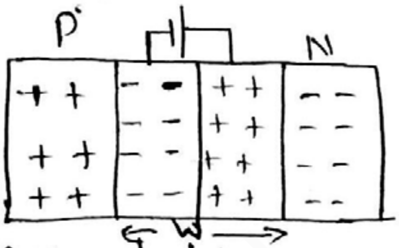
so in Reverse bias only minority carrier current [In Ptype electrons are miniority carriers and holes are the minority carriers in ntype].

From above discussion we can conclude that P-N junction in reverse bias does not flow majority carrier current I=0. so it acts like a open ckt

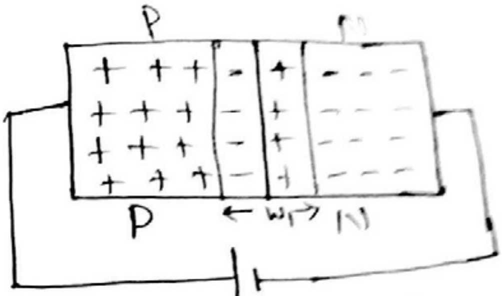




Forward bias.



without bias.



After applying forward bias.

$W >> W_1$ or $W_1 << W$.

when positive terminal of the battery is connected to the P type and negative terminal of the battery is connected to the N type of the P-N junction diode, the bias is known as forward bias.

operation of forward bias:

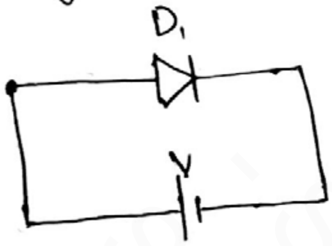
under the forward bias condition, the applied positive terminal potential repels the holes in P type region, so holes moves towards junction.

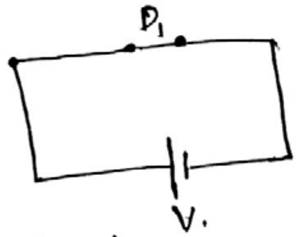
And the applied negative potential repels the electrons in the N type region, and electrons moves towards the junction.

The applied External field more than the internal potential barrier ~~and~~ acts as an opposition to the internal barrier potential and disturbs the equilibrium. So the internal potential barrier disappears. Hence for a forward bias the holes cross the junction from the p-type to the n-type, and electrons cross the junction in opposite direction.

These majority carriers can then travel around the closed circuit and a relatively large current will flow.

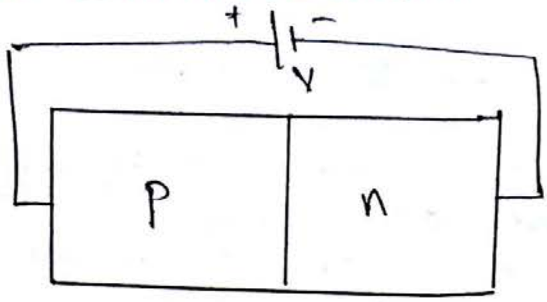
So diode in forward bias majority carrier current flow (large amount). The Diode acts like a short ckt.

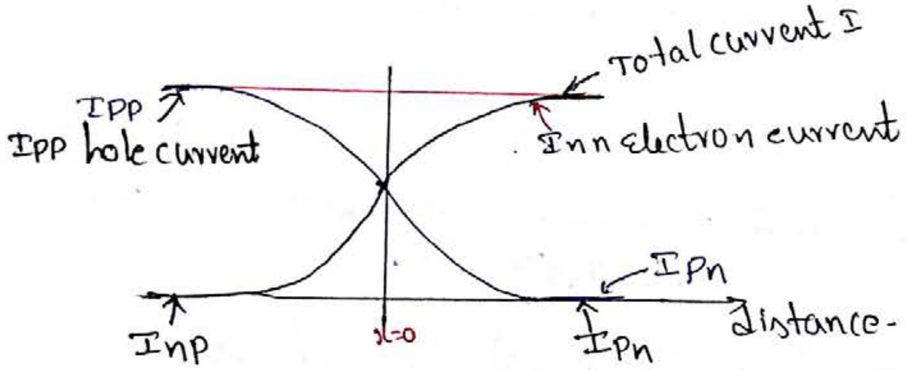




In forward bias of diode both majority & miniority carrier current.

Diode current Equation:





The current components in a p-n diode:

when forward bias is applied to a diode holes are injected in to n side and Electrons in to the p side. The number of these injected minority carriers falls off Exponentially with distance from the junction as shown in fig.

Since the diffusion current of minority carriers is Proportional to the concentration gradient, This current must also varry exponentially with distance.

There are two minority currents I_{pn} and I_{np}. Electrons crossing The junction at $x=0$ from right to left, constitute a current in the same direction as holes crossing the junction from left to right.

Hence the total current I at $x=0$ is

$I = I_{np}(0) + I_{pn}(0)$ miniority current at junction.

Since current is the same throught out series circuit I is Independent of x.

so majority carrier current can be given as

$$I_{pp}(x) = I - I_{np}(x)$$

$$I_{nn}(x) = I - I_{pn}(x) \quad — ②$$

As the holes approach the junction some of them recombine with electrons, which are injected in to the p side from the n side. The I_{pp} at the junction enters to n side and becomes the hole diffusion current I_{pn}.

lly for I_{nn}.

Hence in forward biased p-n diode the current enters the p side as a hole current and leaves the n side as an electron current of the same magnitude.

Quantitative Theory of the p-n diode currents

we have to derive expression of total current as a function of applied voltage.

If forward bias applied to the diode holes are injected from the p side in to the n material. The concentration P_n of holes in the n side is increased above the its thermal equilibrium value P_{no}.

$$P_n(x) = P_{no} + P_n(0)\, e^{-x/L_P} \quad — ③$$

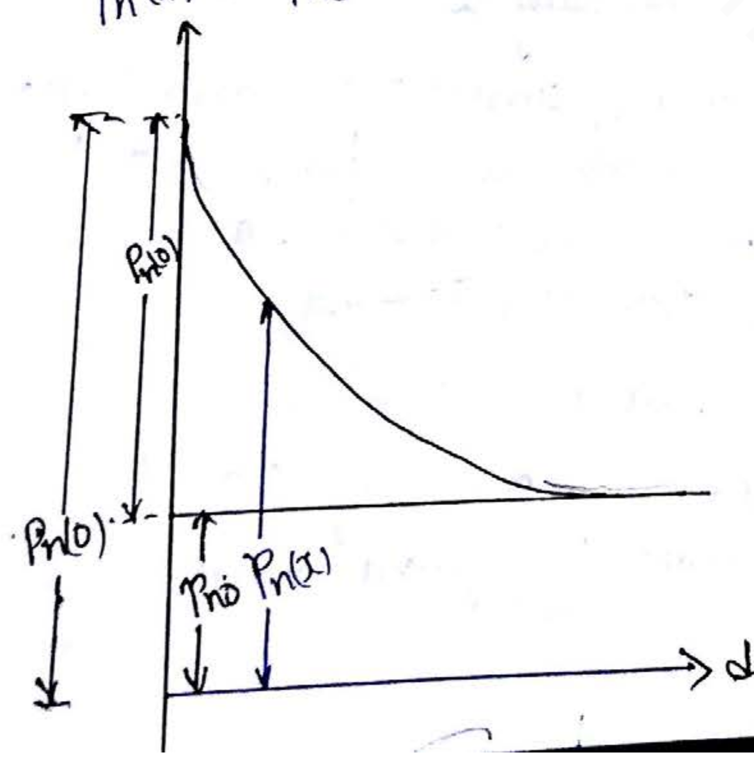


fig. Concentration.

where the parameter L_p is called the diffusion length for holes in the n material and the injected or excess concentration at $x=0$ is

$$P_n(0) \cdot e^{-x/L_P} = P_n(x) - P_{n0}$$

$$P_n(0)\, e^{-x/L_P} = P_n(x) - P_{n0} \; \cancel{\text{at } x=0}.$$

At $x=0$

$$P_n(0)\, e^{-0/L_P} = P_n(0) - P_{n0}$$

$$P_n(0) = P_n(0) - P_{n0} \Rightarrow P_n(0) = P_n(0) - P_{n0} \quad -④$$

Since in the n-type material the hole current is due to diffusion is given as

$$I_{Pn}(x) = -A \cdot e \cdot D_p \cdot \frac{dP_n(x)}{dx} \quad -⑤$$

$$J_{Pn} = -q \cdot D_p \frac{dp}{dx}$$

$$J_{Pn}(x) = -q \cdot D_p \cdot \frac{dP_n(x)}{dx}$$

hole current in inside

$$\therefore J = I/A$$

$$I_{Pn}(x) = -A \cdot e \cdot D_p \cdot \frac{dP_n(x)}{dx}.$$

From continuity equation

$$P_n(x) = P_{n0} + P_n(0) \cdot e^{-x/L_P}.$$

Thermal equilibrium value (at room temperature). so it is a small value when compared to $P_n(0) \cdot e^{-x/L_P}$ is applied. it is occured at when forward voltage is applied.

So $P_n(0) \cdot e^{-x/L_P} > P_{n0}$

$$P_n(x) \cong P_n(0) \cdot e^{-x/L_P} \quad -⑥$$

from ⑤ $$I_{Pn}(x) = -A \cdot e \cdot D_p \cdot \frac{d}{dx}\left(P_n(0) \cdot e^{-x/L_P}\right)$$

$$= -A \cdot e \cdot D_p\, P_n(0) \cdot e^{-x/L_P} \times \frac{d}{dx}\left(\frac{-x}{L_P}\right)$$

$$\boxed{I_{Pn}(x) = \frac{A \cdot e \cdot D_p\, P_n(0) \cdot e^{-x/L_P}}{L_p}} \quad -⑦$$

$$I_{Pn}(0) = \frac{A \cdot e \cdot D_p P_n(0) \cdot e^{-0/L_P}}{L_p}$$

$$\Rightarrow I_{Pn}(0) = \frac{A \cdot e \cdot D_p \cdot P_n(0)}{L_p}$$

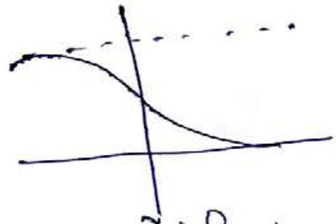
In Eq. (7) the $I_{Pn}(0)$ is dependent on voltage since the $P_n(0)$ is injected concentration implicitly is a function of voltage.

Law of junction.

If the hole concentration at the edges of the space charge region are P_p and P_n in the p type and n type materials respectively and if the barrier potential across this depletion layer is V_B then

$$P_p = P_n \cdot e^{V_B/V_T} \quad — (8)$$

This is the Boltzman relationship of kinetic gas theory.



Exponential decrement

In case of openckt p-n junction

$P_p = P_{Po}$ $\quad P_n = P_{no}$

$V_B = V_0 \rightarrow$ openckt potential barrier value

If the junction is biased barrier voltage V_B is decreased.

$V_B = V_0 - V \rightarrow$ applied potential.

In case of open ckt p-n junction

$P_o = P_{P0}$ $\quad P_n = P_{n0}$ $\quad V_B = V_0$ — openckt potential barrier value.

If the junction is baised, barrier voltage V_B is decreased

$V_B = V_0 - V \rightarrow$ applied potential.

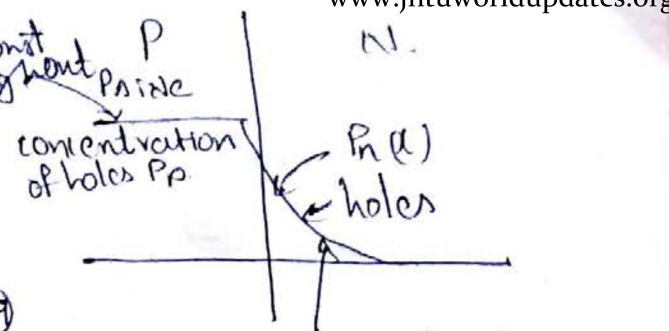
So $P_p = P_{P0}$

$\because P_n = P_n(x)$ at $x = 0$

From Eq.

$$P_p = P_n e^{V_B/V_T}$$

$$P_{p_0} = P_{n(0)} e^{(V_0 - V)/V_T} \quad \text{— (9)}$$



Exponential decrement in nside for hole since minority.

For thermal Equilibrium, assume that barrier voltage V_0 is not there.

$$P_n(0) = P_{n0} e^{V/V_T}$$

This boundary condition is called the law of junction.

If $V>0$ the hole concentration $P_n(0)$ at the junction is greater than the thermal Equilibrium value P_{n0}.

If no equilibrium

$$P_n(0) = \underline{P_{n0} e^{V/V_T}} - P_{n0} \quad \text{— from fig (a)}$$

$\because P_{n0} e^{V/V_T} - P_n(x)$ consentration

$$P_n(0) = P_{n0} e^{V/V_T} - P_{n0}$$

$$P_n(0) = P_{n0} (e^{V/V_T} - 1) \quad \text{— (10)}$$

Forward current

from Eq. (7)

$$I_{Pn}(x) = \frac{A e D_p P_n(0) \cdot e^{-x/L_p}}{L_p} \Rightarrow I_{Pn}(0) = \frac{A e \cdot D_p \cdot P_n(0)}{L_p} \quad \text{substitute 10.}$$

$$I_{Pn}(0) = \frac{A \cdot e \cdot D_p \cdot P_{n0} (e^{V/V_T} - 1)}{L_p} \quad \text{— (11)}$$

Illy for electron current

$$I_{nP}(0) = \frac{A e D_n \cdot n_{P0} (e^{V/V_T} - 1)}{L_n} \quad \text{— (12)}$$

from (1)

$$I = I_{np}(0) + I_{pn}(0)$$

from (11) & (12)

$$I = \frac{A e D_n n_{p0}}{L_n}\left(e^{V/V_T}-1\right) + \frac{A e D_p n_{n0}\left(e^{V/V_T}-1\right)}{L_p}$$

$$= \left(e^{V/V_T}-1\right) I_0$$

$\frac{A e D_n n_{p0}}{L_n}$ - diffusion electron current

$$I = I_0\left(e^{V/V_T}-1\right)$$

Reverse saturation current:

$$I_0 = \frac{A e D_n n_{p0}}{L_n} + \frac{A e D_p P_{n0}}{L_p}$$

$$= Ae\left(\frac{D_n n_{p0}}{L_n} + \frac{D_p P_{n0}}{L_p}\right)$$

$$= Ae\left[\frac{D_n n_{p0}}{L_n} + \frac{D_p P_{n0}}{L_p}\right]$$

$$= Ae\left[\frac{D_n n_i^2}{L_n N_A} + \frac{D_p \cdot n_i^2}{L_p N_D}\right]$$

$$= Ae\left[\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\right] n_i^2$$

mass action law

$np = n_i^2$

In p type

$P = n_i^2/n$

$N_A = n_i^2/N_D$

$n = n_i^2/P$

$N_D = n_i^2/N_A$

Where $n_i^2 = A_0 T^3 e^{-E_{G0}/KT} = A_0 T^3 e^{-\frac{V_{G0}}{KT}}$

Total current

$$I = I_0\left(e^{V/V_T}-1\right)$$

Through out derivation we neglected carrier generation & recombination in the space charge region.

$$\boxed{I = I_0\left(e^{V/nV_T}-1\right)}$$

$\eta = 1$ for Ge large currents

$\eta = 2$ for Si

$$V_T = \frac{T}{11,600}$$

k = Boltzman const 1.38066×10^{-23} J/k

q = charge of Electron 1.602×10^{-19} C

Volt-Ampere characteristics:

As we know that diode equation

$$\boxed{I = I_0 (e^{V/nV_T} - 1)}$$

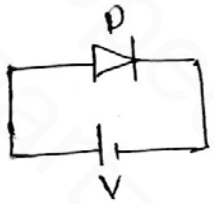
A positive value of I means that current flows from P to the n side. The diode is forward biased if V is positive indicating that the P side of the junction is positive with respect to n side. The symbol n is unity for germanium and is approximately 2 for silicon.

The symbol V_T stands for the volt equivalent of temperature

$$V_T = T/11,600.$$

At room temperature $T = 300 k$ $V_T = 0.026 V = 26 mV$.

Forward bias:



Under the forward bias condition, the applied positive terminal potential repels the holes in P-type region, so the holes move towards junction. (N type - electrons repels by -ve terminal)

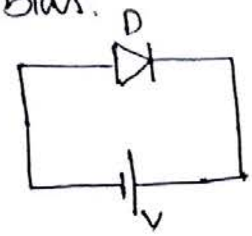
And the applied external field more than than the internal barrier potential, acts as an opposition to the internal potential barrier and disturbs the equilibrium. So internal barrier disappears.

Hence for forward bias, the holes cross the junction from the P type to the N type, and electrons cross the junction in opposite direction.

$$\boxed{I = I_0 (e^{V/nV_T} - 1)} \quad -①$$

from above equation diode current changes exponentially with the applied voltage.

Reverse bias:



The Polarity of connection will cause both the holes in the p-type and the electrons in the N-type to move away from the junction.

consequently the region of negative charge density is spread to left of the junction, and positive charge density region is spread to the right. so width of the depletion region increases. so no current through majority carriers.

In p-type electrons are minority carriers, holes are the minority carriers in N-type. The minority carrier will wander over the junction.

The wandering occurs due to energy is applied externally absorbing that energy they cannot be static in nature. so they get in to motion. so that the electrons and holes of minority carriers wander over the regions.

This results a small amount of current of the diode known as reverse saturation current. This is represented by I_0.

Any how in reverse bias majority carrier current will not be there only minority current will flow.

If Reverse voltage is increased, the current is maintained as const. since minority carrier current will be there in Reverse bias

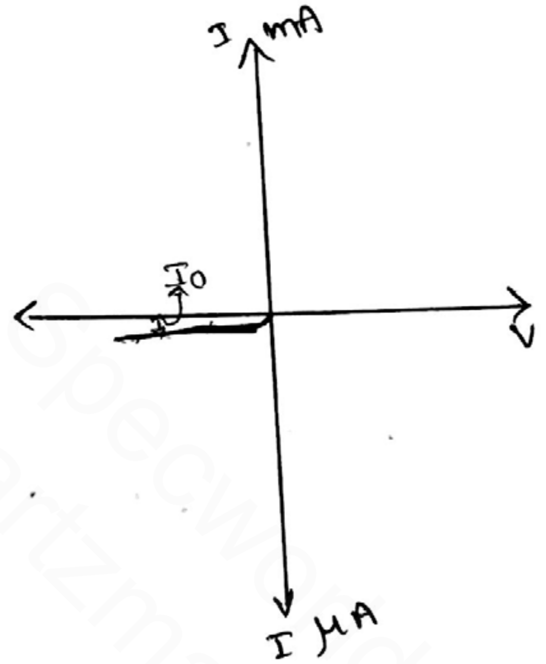
Reverse saturation current is independent of the applied Reverse voltage.

According to equation

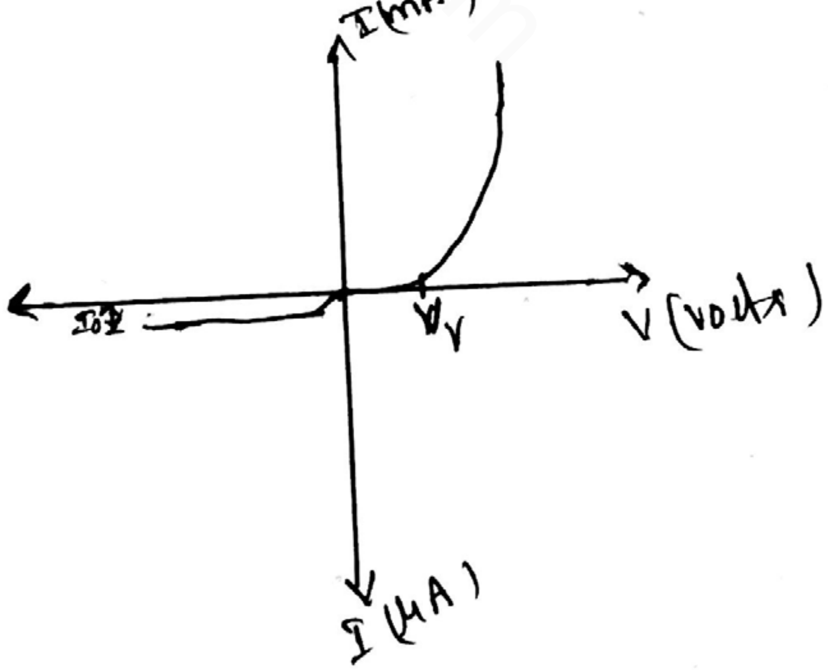
$$I = I_0 \left(e^{V/nV_T} - 1\right)$$

$V \Rightarrow -V \Rightarrow$ so $I \cong -I_0$.

$V = -V$ so that $I \cong -I_0$.



Volt amper characteristics



Temparature dependence of VI characteristic:

The rise in temparature increases the generation of Electron-hole pairs in semiconductors and increase their conductivity. As a result the current through the P-N junction diode increases with temparature as given by the diode current Equation.

$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

The reverse saturation current I_0 of diode increases approximately 7 Percent/°c for both germanium and silicon. Since $(1.07)^{10} \cong 2$, reverse saturation current approximately doubles for every 10°c rise in temperature. Hence if the temparature is increased at fixed voltage, the current I increases. $I_{02} = I_{01} \times 2^{(T_2 - T_1)/10}$. $I_{01} \rightarrow$ at T_1, $I_{02} \rightarrow$ at T_2

To bring the current I to its original value, the voltage V has to be reduced. i.e

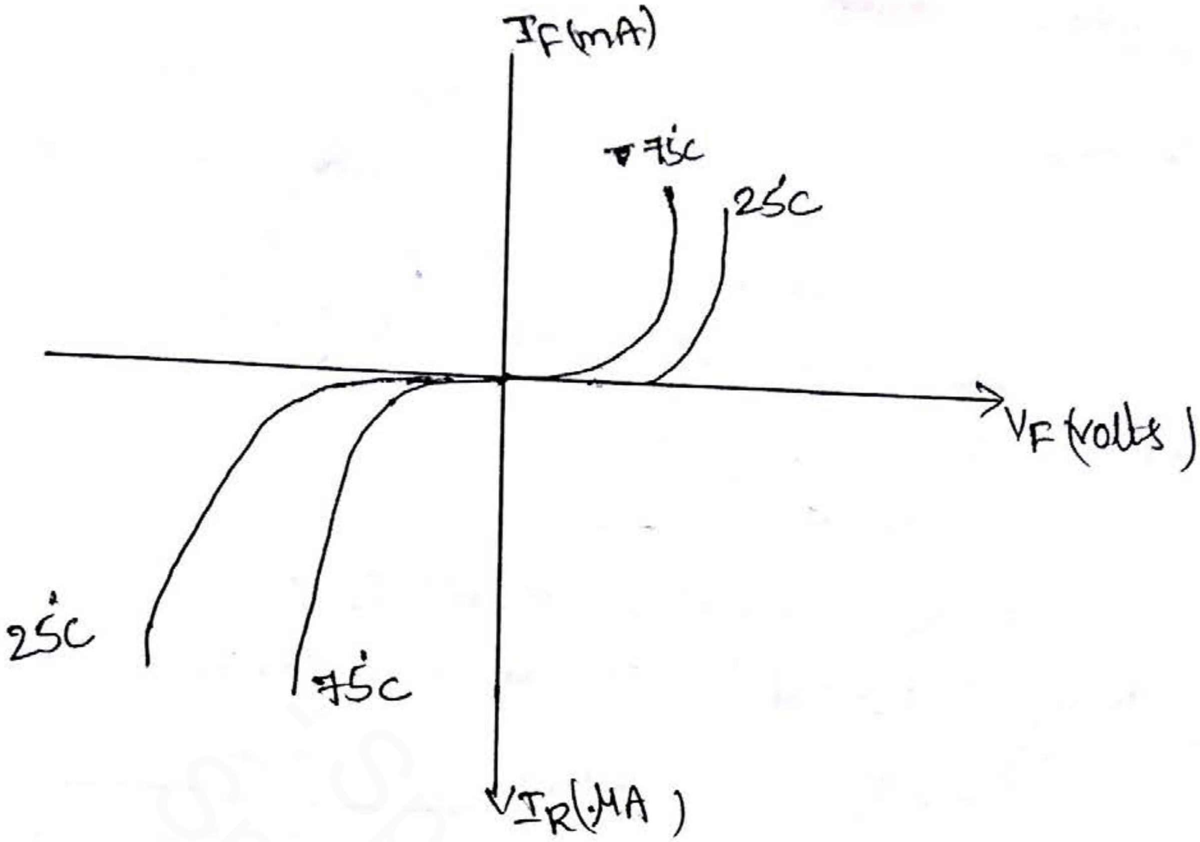
$$\frac{dV}{dT} \cong -2.5\ mV/°c.$$

In order to maintain the current I to a constant value.

At room temparature at 300°k the value of barrier voltage or cutin voltage is about 0.3V for germanium & 0.7V for Silicon.

The barrier voltage is temparature dependent & it is decreased by 2mV/°c for both germanium & silicon.

Mostly we use silicon diodes since a germanium diode can be used up to maximum of 75°c and a silicon diode to maximum of 175°c.



ie The operating temparature of silicon is 175°C & germanium is 75°C.

Cutin voltage $\propto \frac{1}{\text{Temparature}}$

Breakdown voltage $\propto \frac{1}{\text{Temparature}}$.

Cutin voltage & Breakdown voltages are inversly proportional to the Temparature.

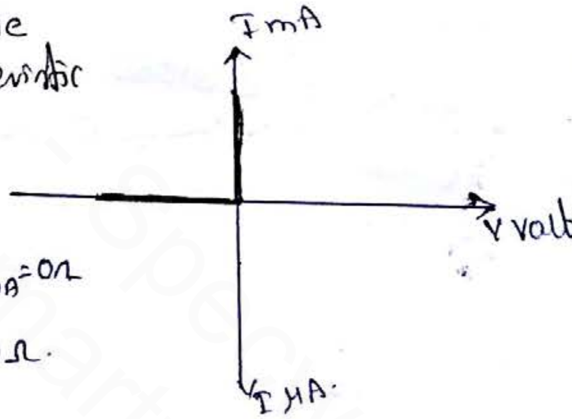
Ideal versus Practical diode

The Ideal diode permits flow of current in one direction and restricts flow of current in another direction.

Ideally the semiconductor diode is to behave like a closed switch in the forward bias region, the resistance of the diode should be 0 Ω.

Ideally in reverse region should be ∞ Ω to represent as open ckt.

Ideal diode
V-I Characteristic



$R_f = 0\ \Omega$
$R_r = \infty\ \Omega$

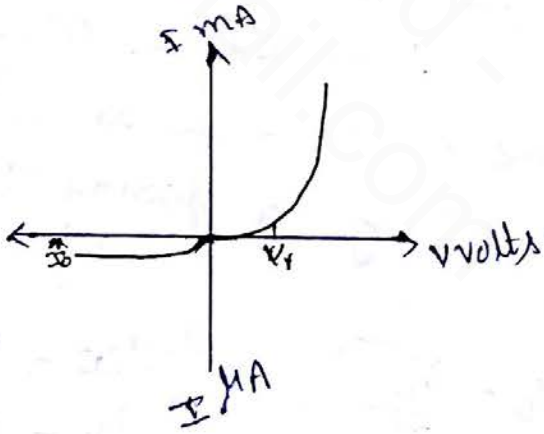
Suppose $R_F = \frac{V_D}{I_D} = \frac{0}{5mA} = 0\Omega$

$R_R = \frac{V_D}{I_D} = \frac{20V}{0\,mA} = \infty\Omega$.

$R_f \rightarrow$ forward bias resistance

$R_r \rightarrow$ reverse bias resistance.

Practical V-I characteristic.



$R_f \neq 0\ \Omega$
$R_r \neq \infty\ \Omega$

Practically after the cutin voltage only the current flows through diode, so that

$R_f \neq 0;$

In Reverse bias also miniory carrier current will flow practically so that

Ideal versus Practical Resistance levels.

Ideal: In Ideal diode the resistance levels is going to mainted as constant due to linear shape

$R_F = 0\,\Omega \qquad R_R = \infty\,\Omega$

Practical Resistance levels.

In Practical diode the resistance levels are going to to be changed due to nonlinear shape of the characteristic curve.

As the operating point of a diode moves from one region to another resistance of the diode will also change due to the nonlinear shape of the characteristic curve.

DC or Static Resistance:

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve will not change with time.

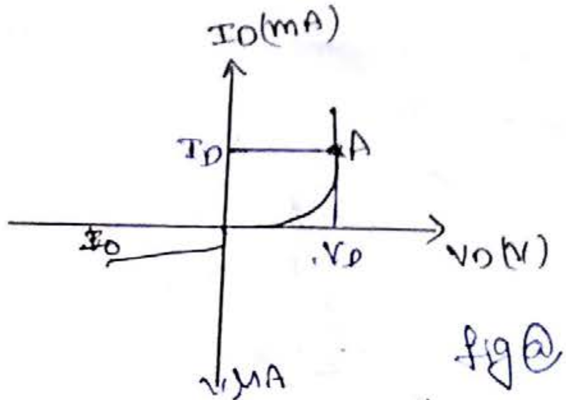
The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D.

$$\boxed{R_D = \frac{V_D}{I_D}}$$

V_D - DC voltage or at P.P V
I_D - DC current or at P.P I

V_D = DC voltage or at a Particular Point voltage
I_D = DC current or at a Particular point current.

In general ~~the~~ the higher the current through a diode, the lower is the DC resistance level



$$R_D = \frac{V_D}{I_D}$$

fig (a)

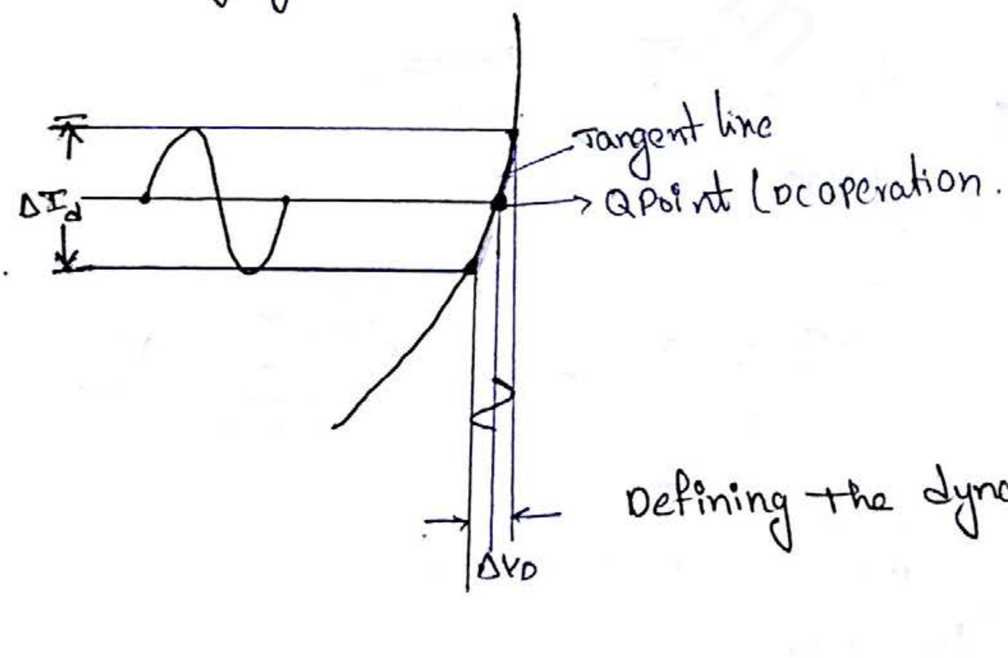
Determining the DC resistance of a diode at a Particular Point.

Ac or Dynamic Resistance :

The sinusoidal input is applied the situation will change completly. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus define a specific change in current and voltage as shown in fig (b)

Quiescent – Q Point

with no applied varying signal, the point of operation would be a point in fig (b) determined by applied dc voltage level. Q is derived from the word quiescent which means still or unvarying



Defining the dynamic or ac resistance

A straight line drawn tangent to the curve through the QPoint as shown in fig (1)

Dynamic or ac resistance for the region of diode is

$$\boxed{r_d = \frac{\Delta V_d}{\Delta I_d}}$$

The effort should be made to keep the change in voltage and current as small as possible and equidistant to either side of the QPoint.

In general, the lower the QPoint of operation smaller current or lower voltage, the higher is the ac resistance.

$$r_d = \frac{\Delta V_d}{\Delta I_d} \quad ; \quad I = I_0 (e^{V/nV_T} - 1) \qquad \begin{aligned} n &= 1 \text{ for Ge} \\ &= 2 \text{ for Si} \end{aligned}$$

The derivation of a function at a point is equal to the slope of the tangent line drawn at that point.

$$I = I_0 (e^{V/nV_T} - 1)$$

$$\frac{dI}{dV_0} = I_0 \cdot e^{V/nV_T} \cdot \frac{d}{dV} \frac{V}{nT} - 0$$

$$= \frac{I_0 \cdot e^{V/nV_T}}{nV_T}$$

$$= \frac{I_0 e^{V/nV_T} - I_0 + I_0}{nV_T} = \frac{I_0 (e^{V/nV_T} - 1) + I_0}{nV_T}$$

$$= \frac{I + I_0}{nV_T} = \frac{I}{nV_T}$$

$$\boxed{\frac{dV}{dI} = \frac{nV_T}{I}} \qquad r_f = \frac{nV_T}{I}$$

$$\boxed{r_d = \frac{nV_T}{I_D}}$$

$n = 1$ & $V_T \cong 26mV$

$$\boxed{r_d = \frac{26mV}{I_D}}$$

The dynamic resistance can be found simply by substituting the Quiescent value of the diode current in to the Equation.

All resistance levels determined above defined for p-n junction and do not include the resistance of the semiconductor material itself called body resistance

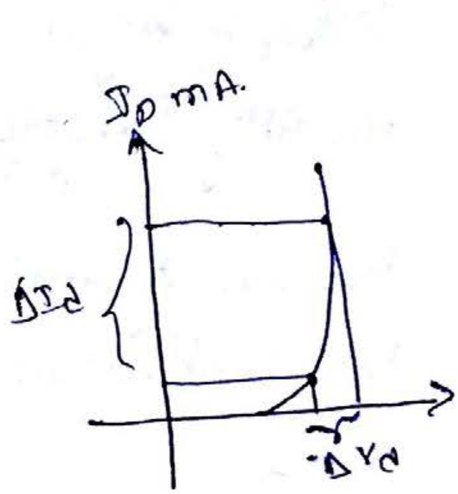
$$r_d' = \frac{26mV}{I_D} + r_B.$$

Average AC resistance

Average AC resistance is defined as the resistance

The Average AC resistance is defined as the two determined by a straight line drawn between the two intersections established by the maximum and minimum values of input voltage.

$$r_{av} = \frac{\Delta V_d}{\Delta I_d}\bigg|_{pt\ to\ pt.}$$



Transition capacitance or Space charge or Depletion region capacitance

As we know that when junction is reversebias majority carriers to move away from junction (Attraction b/n ptype to - ve ntype to +) Hence the thickness of the space charge layer at the junction increases with reverse voltage increased.

$$C_T = \left| \frac{dQ}{dV} \right| \quad -①$$

∵ C_T or W is not constant it varries voltage (reverse) so we taken dQ/dv

$$i = \frac{dQ}{dt}$$

$$i = C_T \cdot \frac{dv}{dt}$$ → from this Equation we can say that i current is depending on C_T also

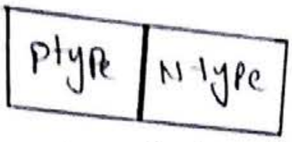
If we use diode or transistor as an circuit element then it is important to know C_T.

C_T is known as transition region, space charge, barrier depletion region capacitance.

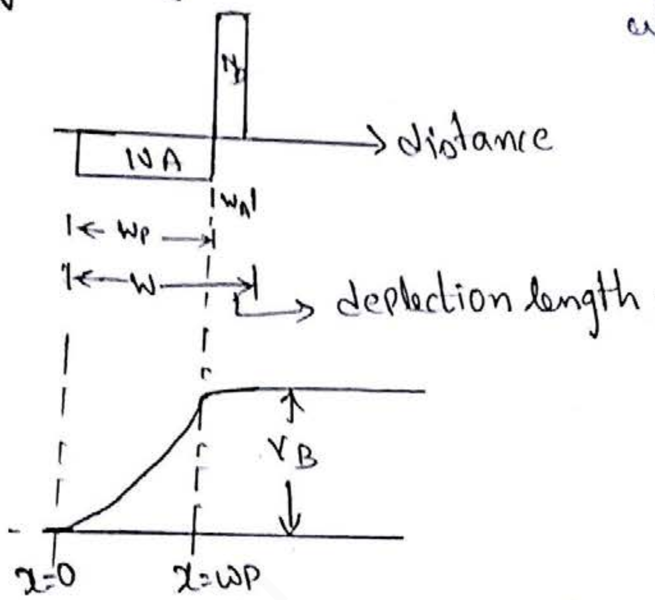
An Alloy junction:

A junction is fabricated by placing trivalent indium against ntype of Germanium and heating the combination to a high temparature, for short time.

since some of the indium dissolves into the germanium the Ntype Germanium is changed to the ptype at the junction (small area) such junction is called as alloy, or fusion junction.



charge density at Junction.



Before heating

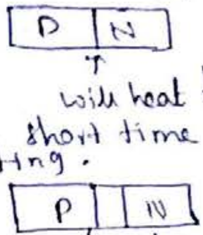


fig. charge density and potential variation at a fusion p-n junction

From graph

$$e \cdot N_A \cdot W_P = e N_D \cdot W_n$$

(NA is less, Wp is large so $N_A W_P$=const
ND is more, Wn is smal → $N_D \cdot W_n$ = const)

If $N_A << N_D$ then $W_P >> W_n$

∵ $N_D >> N_A$ the potential V_B only (i.e only for electrons)

The relationship between potential and charge density by Poisions equation,

$$\frac{d^2V}{dx^2} = \frac{eN_A}{\varepsilon} \quad \text{—②}$$

$\varepsilon_0 \to$ permittivity of free space
ε – permittivity of semiconductor
$\varepsilon_r = \frac{\varepsilon}{\varepsilon_0}$ ε_r is relative permittivity

from fig of potential

$x = W_P \longrightarrow V = V_B$

$$\frac{dV}{dx^2} = \int \frac{eN_A}{\varepsilon}.$$

integrate Eq. ② double times

$$d^2V = \int \frac{eN_A}{\varepsilon} \cdot dx^2$$

$$\iint d^2V = \iint \frac{eN_A}{\varepsilon} dx^2$$

$$\int dV = \int \frac{eN_A}{\varepsilon} \cdot x \cdot dx$$

$$V = \frac{eN_A}{\varepsilon} \cdot \frac{x^2}{2} = \frac{eN_A \cdot x^2}{2\varepsilon}$$

at $x = W_p$; $V = V_B$

$$V_B = \frac{eN_A}{\varepsilon} \frac{W_p^2}{2} \qquad W_p \cong W$$

$$V_B = \frac{eN_A}{2\varepsilon} \cdot W^2 \text{ --- ③} \Rightarrow W^2 = \frac{V_B \cdot 2\varepsilon}{eN_A}$$

$$\boxed{W^2 = \frac{2\varepsilon \cdot V_B}{eN_A}} \text{ --- ④}$$

$$\iint d^2V = \iint \cdot d \cdot dV = \int \int d \cdot dV = \int dV = V.$$

If we consider contact Potential V_0 then

$V_B = V_0 - V \rightarrow$ Reverse bias voltage.

$$W^2 = \frac{2\varepsilon \cdot V_B}{eN_A} \qquad W \propto \sqrt{V_B}$$

from ⓐ (leftside)

$$Q = N_A \cdot e \cdot W \cdot A$$

The transition capacitance C_T given by

$$C_T = \frac{dQ}{dV}$$

$$= \frac{d\, N_A \cdot e \cdot W \cdot A}{dV} \text{ ---}$$

$$= N_A \cdot e \cdot A \frac{dW}{dV} \text{ --- ⑤}$$

$J = nev$ → velocity

$I = nev \cdot A$

$= ne \cdot \frac{W}{t} \cdot A$

$D = S \times t$

$S = D/t$

$D = W$

$I = ne \frac{W}{t} \cdot A$

$\because I = Q/t$

$Q = neW \cdot A$

If concentration $n \cong N_A$

$Q = N_A \cdot e \cdot W \cdot A$ → ⓐ

from (3)

$$V_B = \frac{eNA}{2\varepsilon} W^2$$

$$\frac{dV}{dW} = \frac{eNA}{2\varepsilon} \cdot 2 \cdot W$$

$$\frac{dV}{dW} = \frac{eNA \cdot W}{\varepsilon} \Rightarrow \frac{dW}{dV} = \frac{\varepsilon}{eNA \cdot W} \quad (6)$$

Substitute (6) in (5)

$$C_T = NA \cdot e \cdot A \cdot \frac{\varepsilon}{eNA \cdot W} = \frac{\varepsilon A}{W} = \boxed{C_T = \frac{\varepsilon A}{W}}$$

where A is the Area of junction.
W is the depletion length
ε is the Permittivity $\quad \varepsilon_r = \frac{\varepsilon}{\varepsilon_0} \Rightarrow \varepsilon = \varepsilon_r$.

$$W = \left[\frac{2\varepsilon_0 \varepsilon_r (V_0 - V)}{e} \left(\frac{NA + ND}{NA \cdot ND} \right) \right]^{1/2}$$

Diffusion capacitance or storage capacitance:

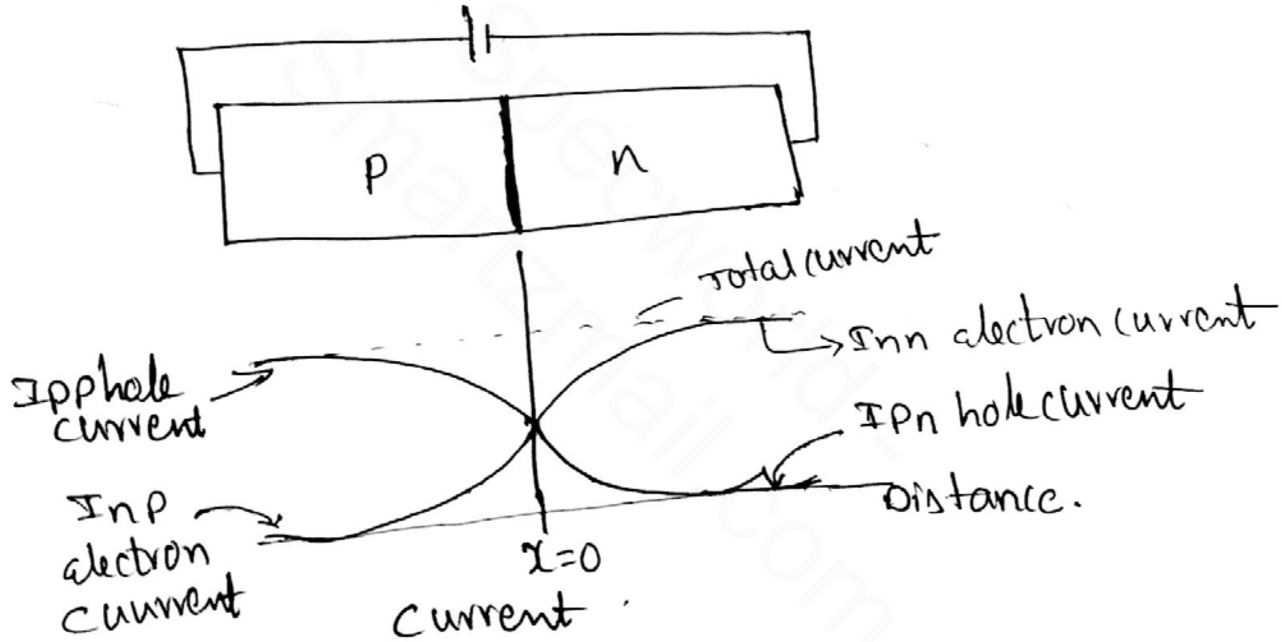
This capacitance comes in to picture when diode in forward bias

<u>origin of capacitance</u>: (How it comes)

If the bias is forward, the potential barrier at the junction is lowered and holes from the pside enter to nside.
Similarly electron from nside to pside.

<u>Derivation</u>:

$$Q = \int_0^\infty Ae\,P_n(0) \cdot e^{-x/L_P} \cdot dx \quad -①$$



$$C_D = \frac{dQ}{dV}$$

$$Q = \int_0^\infty Ae\,P_n(0) \cdot e^{-x/L_P} \cdot dx$$

$$= Ae\,P_n(0) \int_0^\infty e^{-x/L_P} \cdot dx$$

$$= Ae\,P_n(0) \left[\frac{e^{-x/L_P}}{-1/L_P} \right]_0^\infty$$

$$= Ae\,P_n(0)\left[\frac{e^{-x/LP}}{-1/LP}\right]_0^{\infty}$$

$$= \left[A\,e\,P_n(0)\cdot\frac{e^{-\infty/LP}}{-1/LP}\right] - \left[\frac{Ae\,P_n(0)\cdot e^{-0/LP}}{-1/LP}\right]$$

If $\int f(x)\,dx = g(x)$ then

$\int f(ax+b)\cdot dx = \frac{1}{a}g(ax+b)+c$

$e^{-\infty} = 1/e^{\infty} = \frac{1}{\infty} = 0$

$e^{-0} \simeq 1$

$$= 0 + \frac{Ae\,P_n(0)\cdot 1}{1/LP} = Ae\,P_n(0)\cdot LP.$$

Diffusion current given by

$$J = -q\cdot D_p\frac{dp}{dx} = -eD_p\cdot\frac{dp}{dx}.$$

$$Q = Ae\,P_n(0)\cdot L_p \text{ — } (2)$$

$$C_D = \frac{d}{dV}\,A\,e\,P_n(0)\cdot L_p.$$

$$C_D = Ae\,L_p\cdot\frac{d}{dV}(P_n(0))$$

The hole current I is given by $I_{P_n}(x)$. (refer the refference ine2)

$$I_{P_n}(x) = \frac{Ae\,D_p\,P_n(0)\cdot e^{-x/LP}}{LP.}$$

$$\text{at } x=0 \Rightarrow I_{P_n}(0) = \frac{Ae\,D_p\,P_n(0)\cdot e^{-0/LP}}{L_p}$$

$$\because I_{P_n}(0) \simeq I$$

$$I = \frac{Ae\,D_p\,P_n(0)}{LP.}$$

$$P_n(0) = \frac{I \cdot L_p}{A_e \cdot D_p}$$

Differentiate w.r.t V $\frac{dP_n(0)}{dV}$ – find

$$\frac{dP_n(0)}{dV} = \frac{L_p}{A_e D_p} \cdot \frac{dI}{dV} \quad \text{— (4)}$$

$$I = I_0 \left(e^{V/nV_T} - 1\right)$$

$$\frac{dI}{dV} = I_0 e^{V/nV_T} \cdot \frac{d}{dV} \frac{V}{nV_T} - 0$$

$$= I_0 \left(e^{V/nV_T}\right) \cdot \frac{1}{nV_T} \times 1$$

$$= \frac{I_0 \cdot e^{V/nV_T}}{nV_T}$$

$$= \frac{I_0 e^{V/nV_T} - I_0 + I_0}{nV_T}$$

$$= \frac{I_0 \left(e^{V/nV_T} - 1\right) + I_0}{nV_T}$$

$$= \frac{I_0 \left(e^{V/nV_T} - 1\right) + I_0}{nV_T}$$

$$= \frac{I + I_0}{nV_T} \simeq \frac{I}{nV_T}$$

$\frac{dI}{dV} = g$ = conductance

$g = I/V$

small change $g = \frac{dI}{dV}$

so g is conductance

$r = 1/g$.

$$\frac{dI}{dV} = \frac{I}{nV_T} \quad \text{— (5)}$$

substitute (5) in (4)

$$\frac{dP_n(0)}{dx} = \frac{L_p}{A_e D_p} \cdot \frac{I}{nV_T} \quad \text{— (6)}$$

$$C_D = \frac{dQ}{dV} = \frac{d}{dV} A_e P_n(0) \cdot L_p = A_e L_p \cdot \frac{dP_n(0)}{dV}.$$

$$C_D = A_e L_p \frac{dP_n(0)}{dV} \quad \text{— (7)}$$

Substitute (6) in (7)

$$C_D = A e L_p \times \frac{L_p}{A e D_p} \cdot \frac{I}{n V_T}$$

$$= \frac{L_p^2}{D_p} \cdot \frac{I}{n V_T}$$

$$= \tau \cdot \frac{I}{n V_T}$$

$$\boxed{C_D = \frac{I \cdot \tau}{n V_T} \qquad V_T = \frac{T}{11{,}600}}$$

Note: C_D is much larger than C_T.

For reference uc (1)

The Thermal agitation produces new electron hole pair as these undergoes recombination process (combining of electrons and holes). And the time before the recombination process is known as (carrier) lifetime or carrier lifetime or mean life time. It is denoted by τ $\boxed{\tau = \frac{L_p^2}{D_p}}$

For reference uc : 2 :

Diffusion current density given as by holes.

$$J = -e D_p \cdot \frac{dp}{dx}$$

$$J = -e D_p \cdot \frac{dP_n(x)}{dx} \quad \because J = I/A$$

$$I = -e \cdot D_p \cdot \frac{dP_n(x)}{dx} \times A$$

$$I_{P_n}(x) = -e \cdot D_p \left(\frac{d}{dx} P_n(x)\right) A.$$

$$I_{P_n}(x) = -A \cdot e \cdot D_p \frac{dp}{dx} = -A \cdot e \cdot D_p \frac{d P_n(x)}{dx}$$

By continuity Eq. $\quad \because P_n(x) = P_{n0} + P_n(0) \cdot e^{-x/L_p}.$

$$P_n(x) \simeq P_n(0) \cdot e^{-x/L_p}$$

$$I_{P_n}(x) \Rightarrow -A \cdot e \cdot D_p \frac{d P_n(0)}{dx} e^{-x/L_p}$$

$$I_{P_n}(x) = -A \cdot e \cdot D_p P_n(0) \cdot \frac{d}{dx} e^{-x/L_p}.$$

$$I_{pn}(x) = -A \cdot e \cdot D_p P_n(0) \cdot e^{-x/L_p} \times \frac{d}{dx}\left(\frac{-x}{L_p}\right)$$

$$I_{pn}(x) = -A e \cdot D_p P_n(0) \cdot e^{-x/L_p}\left(-1/L_p\right)$$

$$I_{pn}(x) = \frac{A \cdot e \cdot D_p P_n(0) \cdot e^{-x/L_p}}{L_p}$$

$$I_{pn}(0) = \frac{A e D_p P_n(0) \cdot e^{-0/L_p}}{L_p}$$

$$I_{pn}(0) = \frac{A \cdot e \cdot D_p \cdot P_n(0)}{L_p} \cdot 1 \quad — (9)$$

This (9) Equation is used in diffusion capacitance derivation for hole current I

Diode Equivalent circuits:

The equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severly affecting the actual behavior of the system.

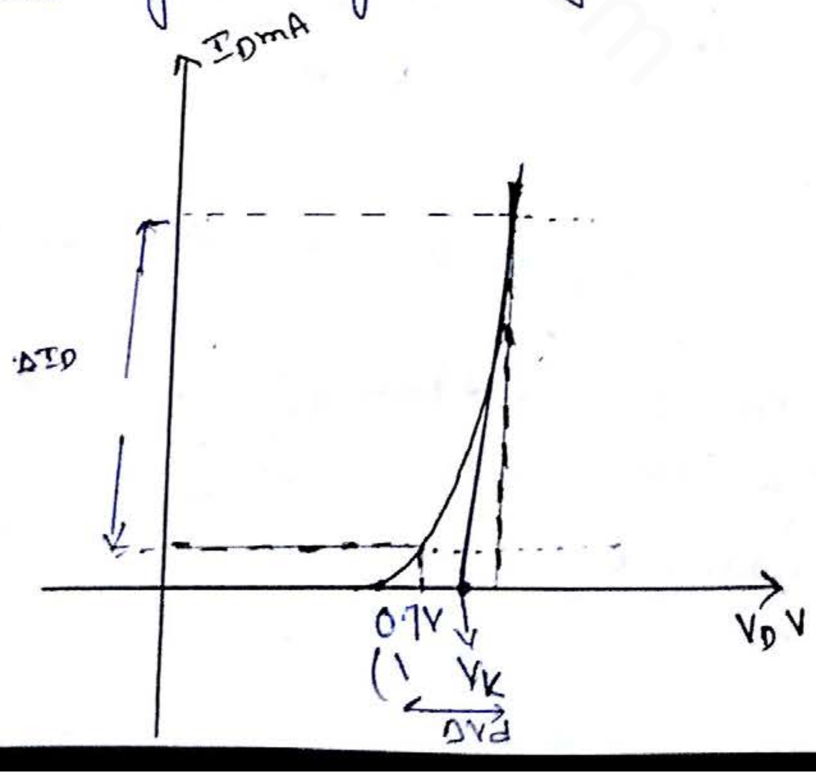
An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device or system in a particular operating region.

Diode equivalent circuits can be discussed under three techniques

1. Piecewise linear equivalent circuit
2. Simplified equivalent circuit
3. Ideal equivalent circuit.

Piecewise linear equivalent circuit:

In this technique an equivalent circuit for a diode is to approximated the characteristics of the device by a straight line segments.

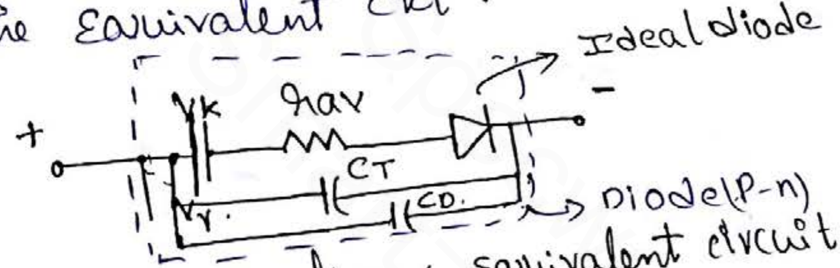


$r_{av} = \frac{\Delta V_d}{\Delta I_D} \Big|_{pt\ to\ pt}$.

The average resistance is considered since through out the curve the resistance will be approximately constant.

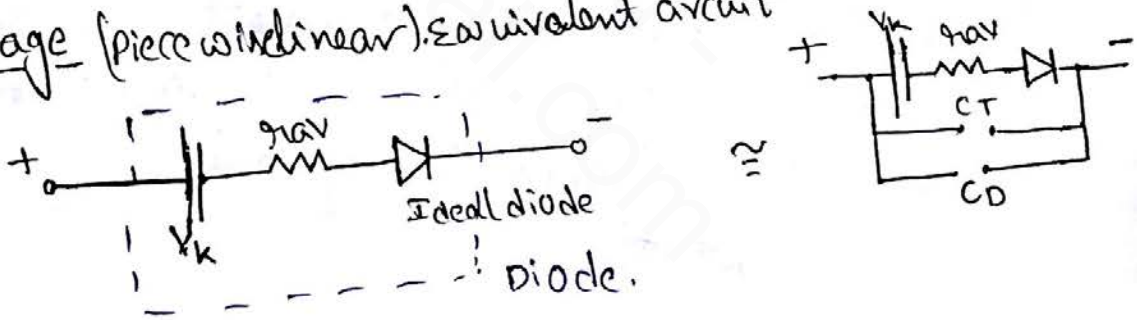
The Ideal diode is indicated in equivalent ckt to represent that there is only one direction of conduction through the device, and reverse bias condition will result the open ckt state of the device.

Since a silicon semiconductor diode does not reach the conduction state untill cutin voltage reaches to 0.7v in forward bias. so a battery V_K opposing the ~~condition~~ conduction direction should be there in the Equivalent ckt.



Piecewise linear Equivalent circuit.

DC voltage (piecewiselinear) Equivalent circuit.



DC voltage $f=0$;

In reverse bias region we have transition or depletion region capacitance(C_T).

where as in the forward bias region we have diffusion C_D or storage capacitance. $C_T = \varepsilon A/d$.

forward bias $\rightarrow$ C_D — diffusion capacitance

Reverse bias — C_T — transition capacitance.

As we that for DC voltage $\underline{f=0}$ in capacitance

$X = \frac{1}{j2\pi fc} = \frac{1}{j\omega c}$.

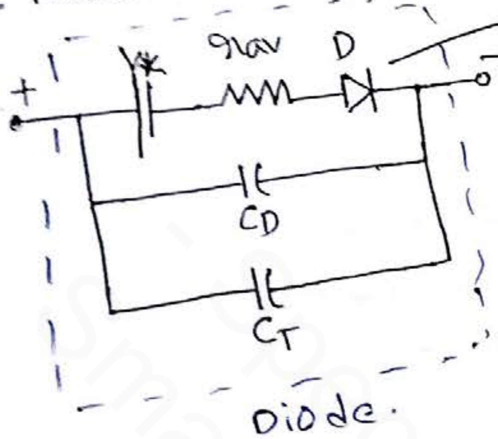
$\underline{DC}$ $\underline{f=0}$ $X_c = \frac{1}{j2\pi(0) \cdot C}$ $X_c = \infty$

So the capacitance will not come in to picture for the diode when DC voltage is applied.

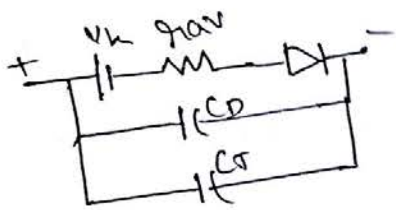
AC voltage piecewise linear - Equivalent ckt.

→ Ideal diode (R=0 → F.B, R=∞ → R.B)

AC i/p applied



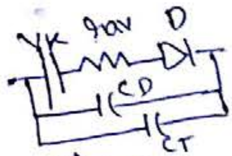
Diode.



for AC voltage $f \neq 0$

$X_c = \frac{1}{j2\pi fc}$ = Some value will be there.

<u>lower frequency value</u> $f \neq 0$ & $f \neq \infty$



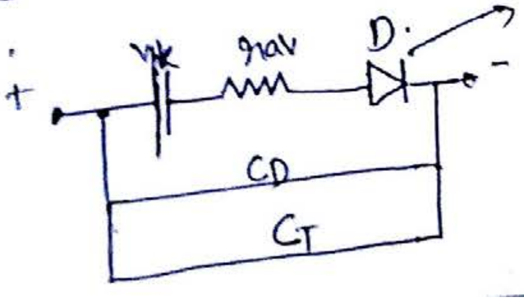
$X_c = \frac{1}{j2\pi fc}$ = some value will be there.

<u>Higher frequency value $f \neq 0$ & $f = \infty$</u>

$X_c = \frac{1}{2\pi(\infty) \cdot C} = \frac{1}{\infty} = 0$.

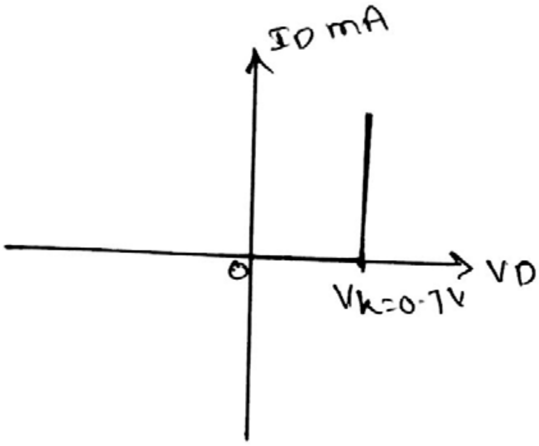
X_c act has a short circuit at higher frequency values.

→ Ideal Diode.



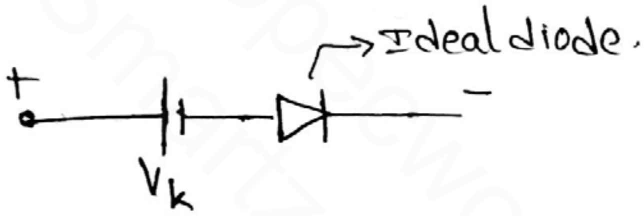
Simplified Equivalent circuit:

If the elements of the network are large when compared to diode elements then the elements of the diode can be ignored.



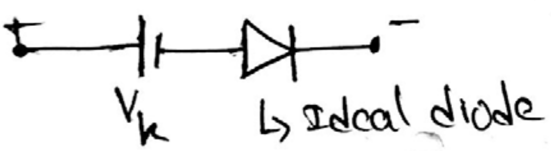
$r_{av} = 0\,\Omega$.

DC voltage – Simplified Equivalent circuit.



$R_{network} >> r_{av}$

AC voltage – simplified Equivalent circuit.



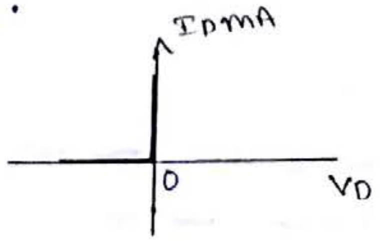
$R_{network} >> r_{av}$

$C_{network} >>> C_D$ & C_T

r_{avg} & C_D, C_T are ignored when the network values are greater than C_D, C_T & r_{avg}.

Ideal Equivalent circuit:

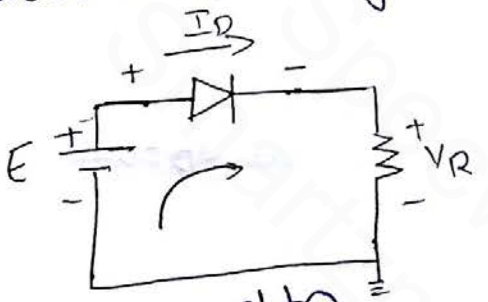
The Ideal Equivalent circuit is for the Ideal diode.



Ideal Equivalent circuit for both AC & DC voltage.

Load line Analysis:

Loadline analysis is used to describe the analysis of a diode circuit using its actual characteristics.



ckt@

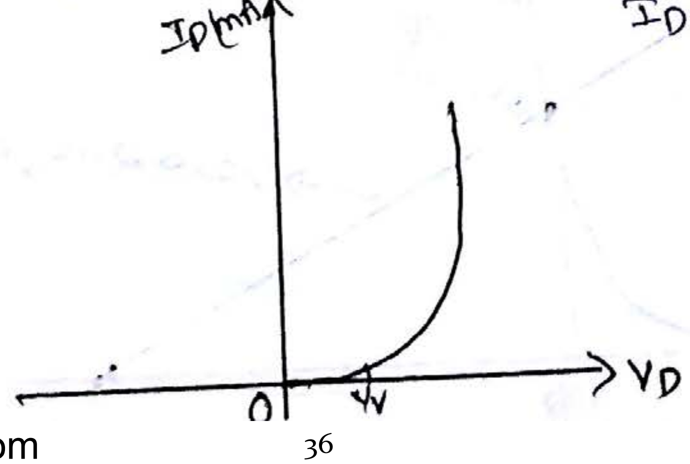
Load line Analysis is done in two steps.

1> draw the curve for actual characteristics.

2> Draw a straight line is called a load line. by using Kirchoff's voltage law.

Draw the actual characteristics of curve by using a diode Equation

$$I_D = I_0\left(e^{V/nV_T} - 1\right). \quad -① \qquad I_D = I_0\left(e^{V_D/nV_T} - 1\right)$$



By using kirchhoffs voltage law for above ckt(a),

we get

$$+E - V_D - V_R = 0$$

$$E = V_D + I_D \cdot R. \quad -②$$

The two variables in Eq.② V_D & I_D are the same as the diode axis variables as in Eq.①. so we can plot both on the same figure.

we have to find where the load line touches the x-axis and y-axis.

<u>X-axis</u> <u>touches</u> <u>at</u> when $I_D = 0A$.

$$E = V_D + I_D \cdot R \quad \text{from②}$$

If we set $I_D = 0V$ & slove for V_D, we have the magnitude of V_D on the horizontal axis.

$$E = V_D + (0A) R$$

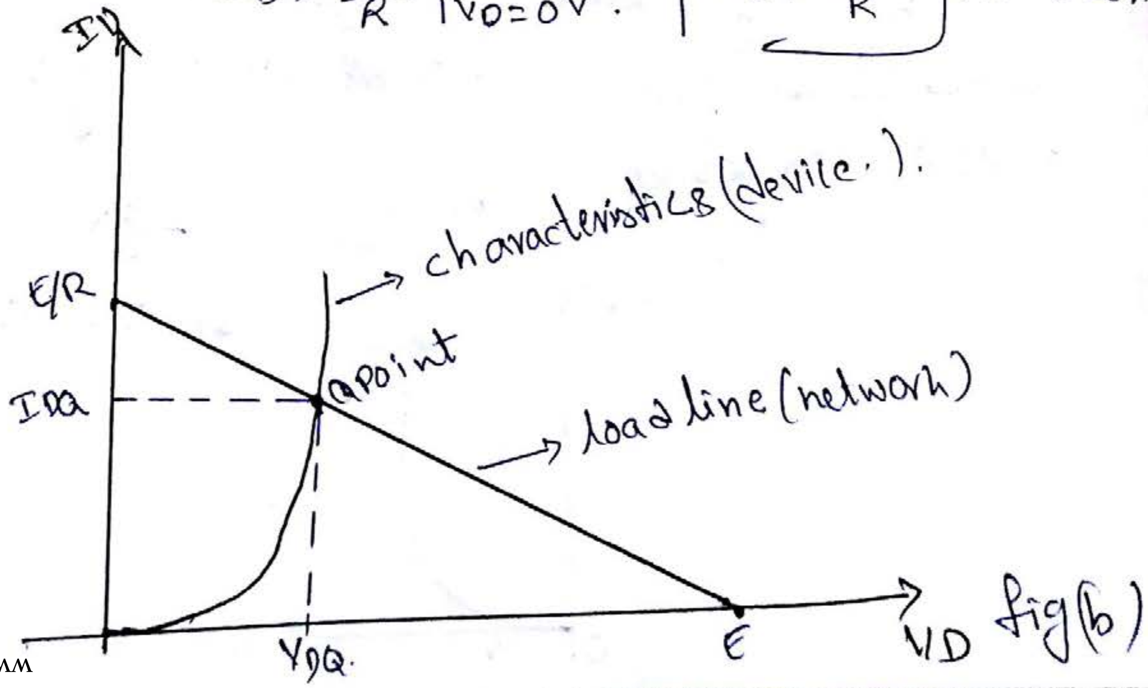
$$E = V_D + 0. \quad \boxed{V_D = E} \text{ at } I_D = 0A.$$

Y-axis touches at when $V_D = 0 \cdot A$.

$$E = V_D + I_D \cdot R$$

$$= 0 + I_D \cdot R$$

$$I_D = \frac{E}{R}\Big|_{V_D = 0V}. \quad \boxed{I_D = \frac{E}{R}} \text{ at } V_D = 0A$$



change the level of R (the load) and the intersection on the vertical axis will change.

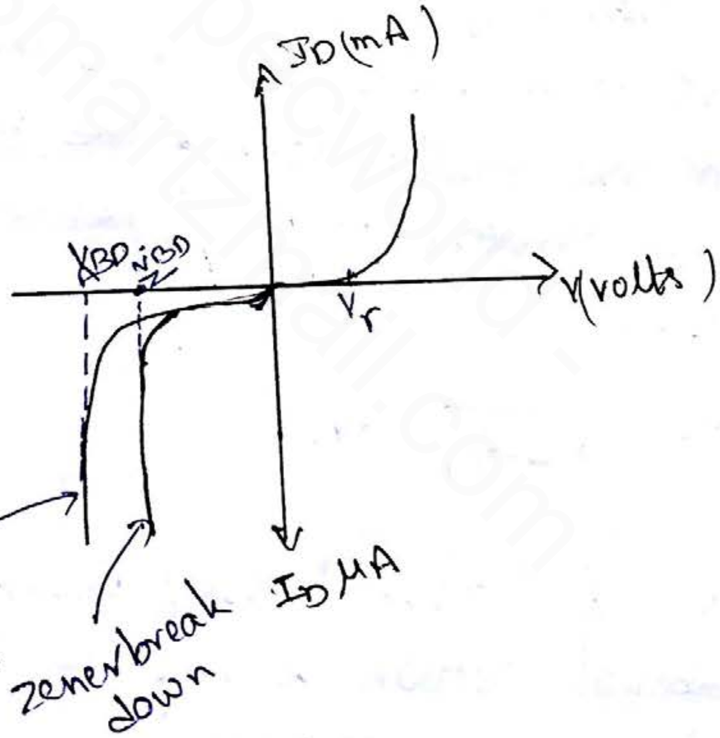
The result will be change in the slope of the load line and a different point of intersection between the load line and the device characteristics.

The point of intersection of load line w device characteristics point is known as Q point.

Breakdown mechanisms in semiconductor Diodes.

The diode Equation Predicts that under reverse bias condition a small constant current i.e saturation current I_0, flows due to minority carriers, which is independent of the magnitude of the bias voltage. But it is not true entirely true for Practical diodes.

There is a sudden increase in reverse current due to some sort of breakdown, when the reverse bias voltage approaches a particular value called breakdown voltage or Peak inverse voltage V_{BD}.



In semiconductor Diodes there are two types of breakdown

1. Avalanche breakdown.
2. zener breakdown.

Avalanche breakdown.

Thermally generated minority carriers cross the deplection region ω acquire sufficient kinetic energy from the applied Potential. As a result the velocity of these carriers increases, these electrons disturb covalent bonds by colliding with immobile ions and create new electron-hole pairs.

These new carriers again acquire sufficient Energy from the field and collide with other immobile ions by disturbing the covalent bonds there by generating further electron hole pairs.

This Processes is going on multiplication of avalanche charge carriers with in short time. so this Proleses is called Avalanche multiplication. The multiplication effect of free carriers may be represented by following equation.

$$M = \frac{1}{1-\left(V/V_{BD}\right)^n}$$

M = carrier multiplication factor (which is the ratio of total number of electrons leaving the deplection region to the number entering the region.)

V = applied reverse voltage.

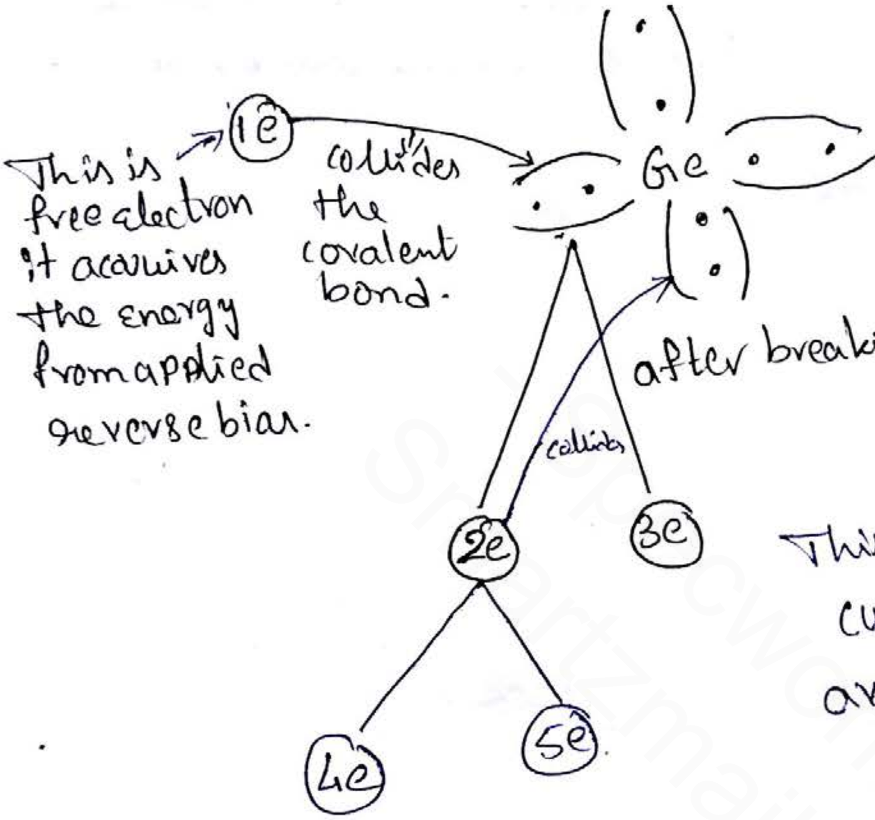
V_{BD} = reverse break down voltage

n = emperical const. which depends on the lattice material ω the carrier type. for N-type silicon $n \simeq 4$ ω for ptype $n \simeq 2$.

This Processes results of flow of large amount of current at small change of value of reverse bias voltage.

The avalanche breakdown occurs at the voltage > 6v.

Picture diagram of Avalanche Processes.



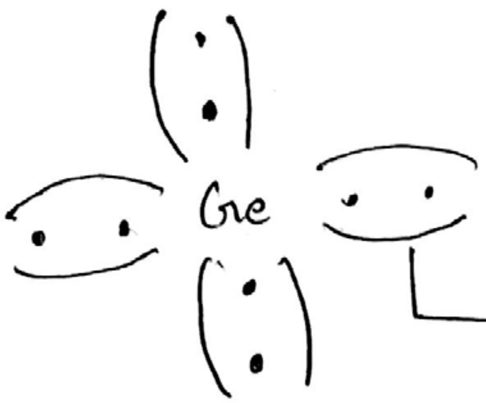
This Process is cumulative so known as avalanche multiplication.

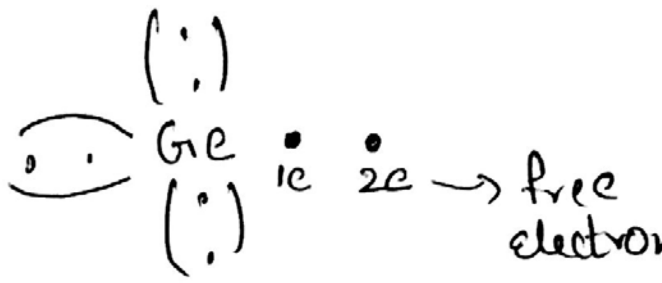
zener break down:

If initally available carriers donot gain enough energy to distrub the covalent bonds. Then it initiate breakdown through direct rupture of the covalent bonds, because of presence of a strong electric field. under this conditions breakdown is reffered as the zener breakdown. so then new electron hole pairs are created, by this increase in reverse current.

This breakdown occurs at the below (6v) voltage < 6v

Picture diagram of zener breakdown voltage:





rupture of covalent bonds due to pressure will be more.

Zener Diode characteristics:

when the reverse voltage reaches breakdown voltage in normal PN junction diode, the current through the junction and the power dissipated at the junction will be high. such an operation is destructive and diode gets damaged.

Some of the diodes can be designed with adequate power dissipation capabilities to operate in the breakdown region. one of such diodes is known as zenerdiode.

The zener diode is heavily doped than the ordinary diode. (zener→1: 10^5 ; P-n →1: 10^6)
for 10^5 intrinsic material 1 atom impurity is added.
If doping level changes characteristics of diode will change.

The breakdown voltage depends on the doping level.

$$V_B \text{ (Break down voltage)} \propto \frac{1}{\text{doping}}$$

$$W \text{ (depletion layer width)} \propto \frac{1}{\text{doping}}$$

It is clear that the breakdown voltage for a particular diode can be controlled during manufacture by altering the doping levels in the junction.

zener diode operate as a P-n junction diode in the forward bias. The zener diode characteristics are mainly observed in the reverse bias.

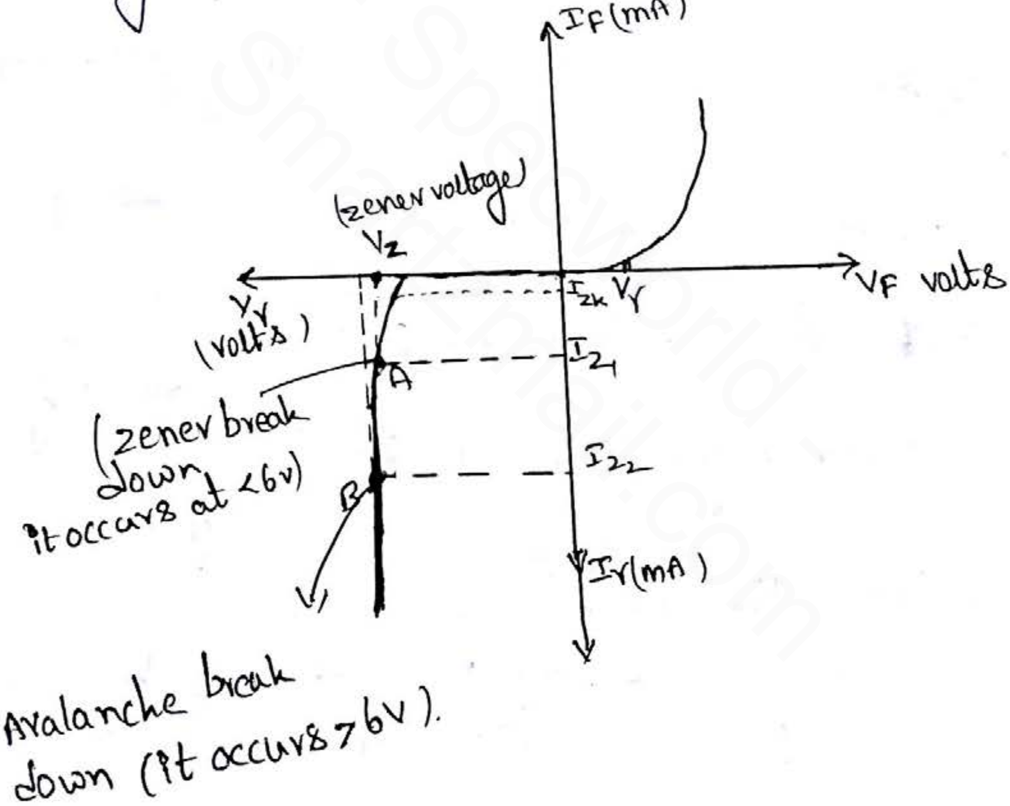
Zener diode characteristics in reverse bias:

In reverse bias condition, zener diode will have two breakdown regions

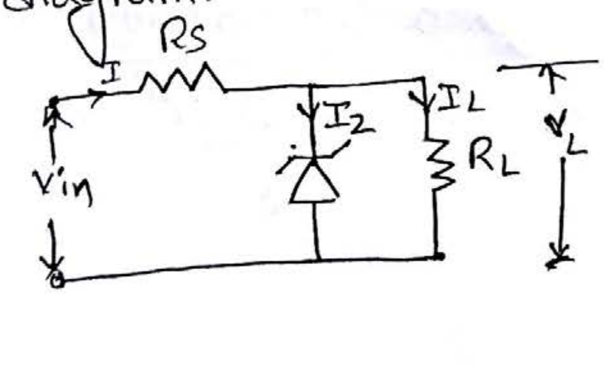
1. Zener breakdown (it occurs <6V)
2. Avalance breakdown (it occurs >6V).

Due to these two breakdowns there will be sudden increment of currents for small change in voltage. If small change of voltage can be treated as a constant voltage.

So. zener diode can be treated as a voltage regulator.



ckt diagram.



$I = I_Z + I_L$

$V_L = I_L \cdot R_L$

$V_Z = I_Z \cdot R_Z$

R_Z — zener resistance

zener diode is conducting then

$$V_L = V_Z = V_{Br}$$

$I_L \cdot R_L = I_Z \cdot R_Z$ — since in parallel the voltage are same

$$\frac{I_L}{I_Z} = \frac{R_Z}{R_L}$$