Computer Architecture & Organization

II mid Review questions.

Short answer question

1) Define Hit & Miss in cache memory.
2) What is a virtual Memory?
3) Differentiate tightly and loosely coupled multiprocessors.
4) Define crossbar switch?
5) What is a pipeline hazard?
6) Define cache coherence?
7) Differentiate Isolated and memory mapped I/O.
8) Define Multicomputer and Multiprocessors?
9) What is a pipeline hazard?
10) What is locality of Reference?
11) What is the difference between Static and Dynamic RAM?
12) What is the difference between a vectored and a Non-vectored Interrupt?
13) What is delayed load and delayed branch in RISC pipeline?
14) What is the basic component of a multistage network?
15) Define a normalized floating point number.

Easy type:

1) Give the algorithm for performing restoring division with example.
2) A digital computer has a memory unit of 64kx16 and a cache memory of 1k words. The cache uses direct mapping with a block size of four words
    a) How many bits are there in the tag,index,block & word field of the address format

b) How many bits are there in each word of a cache, how are they divided into functions? Include a valid bit?

c) How many blocks can the cache accommodate?

3) Explain about the DMA mode of data transfer.

4) Explain in detail about Input-Output Processor (IOP).

5) Write short notes on vector processing. Mention some applications of vector processors.

6) Explain about the different Interconnection structures used in multiprocessor environment.

7) Explain step by step process of multiplying +15 with -13 using Booths algorithm.

16) What are the different mapping techniques used in Cache memories. Explain any one of them in detail with example.

17) What are the different modes of data transfer? Explain Interrupt-Initiated I/O?

18) A) Explain about PCI bus?

B) Explain about IEEE 488 bus?

15. A computer system uses pipeline technique to process computer instructions. Assume the time it takes to process an operation in each segment is equal to t_p=20ns. Assume this pipeline has k=4 segments and exceeds n=100 instructions in sequence. Answer the following

i) How long time to execute 100 instructions does this computer take with this pipeline.

ii) How long time does it take with non-pipeline(T_{np})

iii) What is speed up?

16. Construct a diagram for a 8x8 omega switching network. Show the switch setting required connecting Processor 3 to MM 1?

17. Briefly explain about Array Processors.

18. Explain Cache coherence problem and solutions to it.

19. Briefly explain RISC pipeline. How NOP instruction is used to resolve conflicts in pipeline.

20. Explain how address translation is achieved using TLB (Translation look-aside

buffer)