**Department/Program:** CIS / Information Technology

**Course Code:** CIS 236 **Course Title:** Computer Organization and Architecture

**Credits: 3 Lecture Hours:** 3

**Lab/Studio Hours:** None **Clinical/Fieldwork Hours:** None

**Prerequisites:** MA 101 and CIS 160 or CIS 165

**Semester Offered:** Spring (Evening)

**Special Facilities/Equipment:**

Hardware: WinTel Platform PC or lab top.

Software:

Storage Media: At least 1 GB Flash Drive for saving homework and projects.

**ADDITIONAL TIME REQUIREMENTS**:

All homework assignments are completed out of class time. Students, who don’t have a computer or don’t have the version of the operating system and software, can use the open lab to complete homework assignments.

**REQUIRED TEXTBOOK/MATERIALS**:

**Textbooks:** **“Computer Organization and Architecture: Designing for Performance”**; 9th Edition; William Stallings; Prentice Hall; 2013. ISBN-13: 978013607373413.

**Reference:** “**Introduction to Computing Systems, From Bits & Gates to C & Beyond”;** Yale N. Patt & Sanjay J. Patel, McGraw Hill, 2004.

**Catalog Course Description:**

This course provides the students with a clear, comprehensive presentation of the organization and architecture of modern-day computers, emphasizing both fundamental principles and the critical role of performance in driving computer design. The course will highlight the system three major components: processor, memory, and I/O. Furthermore, each major component is decomposed into its major sub-components. Included topics are (data representation, digital logic design, control unit, registers, ALU, instructions, data paths, memory hierarchy, I/O devices, instruction set architecture, and addressing modes). Throughout, aspects of the system are viewed from the points of view of both architecture and organization.

**COURSE LEARNING OUTCOMES**:

Upon completion of this course, students will be able to:

1. Transform problems expressed by humans as binary strings in a machine code.
2. Describe how computers are constructed out of a set of functional units
3. Describe how these functional units operate, interact and communicate
4. Explain the factors that affect computer performance.
5. Demonstrate an understanding the effect of memory and I/O subsystems on the overall system performance.
6. Simulate computations as actually performed at the machine level

**General Education Outcomes (if applicable**)

N/A

**EVALUATION CRITERIA:**

To assess the above student outcomes, students will be given homework, quizzes, and exams. In addition, students have to demonstrate a satisfactory level of knowledge and skills in:

1. Machine data representations and digital logic
2. Hardware functional units’ capabilities and limitations.
3. Effect of one subsystem on another subsystem performance.
4. Various bus structures.
5. Interconnectivity of the modern system components.
6. CPU functional units.
7. Multicore CPU architecture

**RESOURCE BIBLIOGRAPHY:**

* **The Essentials of Computer Organization and Architecture (Third Edition)**, linda Null and Julia lobur, jones & Bartlett, 2012.
* **Software Organization and Design: *The Hardware/Software Interface*, (Fourth Edition)**, David A. Patterson & John L. Hennessy, Morgan Kaufmann Publishers (Elsevier Inc.), 2009
* [**Computer Architecture, 5th Edition: A Quantitative Approach**](http://www.elsevierdirect.com/product.jsp?isbn=9780123838728)  
  Hennessy and Patterson, Morgan Kaufmann Publishers,2012.
* [**Computer Architecture and Organization: An Integrated Approach**](http://www.wiley.com/WileyCDA/WileyTitle/productCd-EHEP000661.html)**,** Miles J. Murdocca, Vincent P. Heuring, Wiley, 2007
* **Structured Computer Organization (5th Edition)**, Andrew S. Tannenbaum, Pearson Prentice Hall, 2006.

**ACADEMIC REGULATIONS AND POLICIES**:

For Information regarding any of the following, please refer to the PCCC student Handbook and the PCCC Academic Bulletin:

* PCCC’s Academic Integrity Code
* Student Conduct Code
* Student Grade Appeal Process
* Writing Intensive Requirements
* Information Literacy Requirements
* Panther Alert: The College will announce delayed openings, closings, and other emergency situations through the Panther Alert System. Students are encouraged to sign up for the Panther Alert Notification. Students can sign up once they log into their Campus Cruiser Portal account through the PCCC website at www.pccc.edu.
* Cell Phone Policy: Use of cellular telephones, audible pagers, or other forms of audible electronic devices is prohibited in all academic learning environments (including but not limited to, laboratories, testing centers, classroom, library, learning centers, theater, and so forth) unless previously approved by the instructor or other authorized administrator.

**NOTIFICATION FOR STUDENTS WITH DISABILITIES:**

If you have a disability, and believe you need accommodations in this class, please contact the Office of Disabilities Services (ODS)

at 973-684-6395, or email [ods@pccc.edu](mailto:ods@pccc.edu), to make an appointment.

You should do so as soon as possible at the start of each semester.

If you require testing accommodations, you must remind me (the instructor) one week in advance of each test.

**LATE HOMEWORK POLICY:**

* Any homework that is late will lose 15% of its value for every week that its late

**MAKE-UP EXAM POLICY:**

* Make-up exams will be permitted only under extenuating circumstances and only with prior notification and original documentation.
* Exams cannot be made-up after the exam date has passed.
* The instructor reserves the right to create alternate make-up exams

**GRADING STANDARD**:

Students will be graded on the basis of testing and an evaluation of projects assigned by the instructor.

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| --- | --- |
| **Activity** | **Contribution** |
| Homework (every chapter) | 30% |
| Tests/ Quizzes | 35% |
| Final Exam | 30% |
| Attendance/Activities/Etc. | 5% |

|  |  |  |  |
| --- | --- | --- | --- |
| **Grading Scale** | | | |
| 95+ | A | 76-79 | C+ |
| 90-94 | A- | 70-75 | C |
| 87-89 | B+ | 60-69 | D |
| 84-86 | B | < 60 | F |
| 80-83 | B- |  |  |

**COURSE CONTENT:**

**Student Preparation for Each Class:**

* Read the text chapters assigned per the schedule.
* Review objectives from the chapters.

**LECTURE SCHEDULE**

**WEEK TOPIC Chapter**

1 **Introduction:** 9 + 11

##### Review - Syllabus and requirements

##### Review – Number systems and Digital Logic

##### 2 Review - Organization and Architecture, Structure and Function 1

3 **Computer Evolution and Performance:** 2

##### A Brief History of Computers, Designing for Performance,

##### The Evolution of the Intel x86 Architecture,

##### Embedded Systems and the ARM, Performance Assessment,

##### Recommended Reading and Web Sites

4 **A Top-Level View of Computer Function and Interconnection:** 3

##### Computer Components, Computer Function,

##### Interconnection Structures, Bus Interconnection,

##### PCI, A Timing Diagrams

##### 5(Test 1) **Cache Memory:** 4

##### Computer Memory System Overview,

##### Cache Memory Principles, Elements of Cache Design,

Pentium 4 Cache Organization, ARM Cache Organization.

6 **Internal Memory Technology:** 5

##### Semiconductor Main Memory, Error Correction,

##### Advanced DRAM Organization.

# 7 External Memory: 6

##### Magnetic Disks, RAID, Optical Memory, Magnetic Tape.

# 8(Test 2) Input/Output: 7

##### External Devices, I/O Modules, Programmed I/O,

##### Interrupt-Driven I/O

Direct Memory Access, I/O Channels and Processors,

##### The External Interface: FireWire and Infiniband

##### 9 **Operating System Support:** 8

##### Operating System Overview,

##### Scheduling, Memory Management

##### Pentium Memory Management, ARM Memory Management

**WEEK TOPIC Chapter**

**10(Test 3)** **Computer Arithmetic:** 10

##### The Arithmetic and Logic Unit (ALU)

##### Integer Representation, Integer Arithmetic

11 Floating-Point Representation, Floating-Point Arithmetic. 10

11 **Instruction Sets: Characteristics and Functions:** 12

Machine Instruction Characteristics,

12 Types of Operands, Intel x86 and ARM Data Types, 12

Types of Operations, Intel x86 and ARM Operation Types

12 **Instruction Sets: Addressing Modes and Formats:** 13

##### Addressing, x86 and ARM Addressing Modes,

13 Instruction Formats, x86 and ARM Instruction Formats, 13

##### Assembly Language.

**13(Test 4)** **Processor Structure and Function:** 14

##### Processor Organization, Register Organization,

##### The Instruction Cycle, Instruction Pipelining,

14 The x86 Processor Family, The ARM Processor 14

##### Addressing, x86 and ARM Addressing Modes.

Review

15 **Final Exam**

**CHANGES TO THE SYLLABUS:**

The instructor reserves the right to make changes to this syllabus. In the event that changes become necessary, students will be notified during the following scheduled class.