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MANIPAL INSTITUTE OF TECHNOLOGY
BENGALURU
(A constituent unit of MAHE, Manipal)

QUIZ
IV SEMESTER (CSE / CSE-CS),
EMBEDDED SYSTEM (CSE_2253/IT_2253)
SET - C

Max Marks: 10 **Duration: 30 minutes**

Student's Name	RUTVIK AVINASH BARBHAI
Reg No./ SECTION	225805222 / section - A
Student Signature	RutBar:

1. Which register is used as the pointer in PC relative addressing mode?
   a. R12
   b. R13
   c. R14
   d. R15

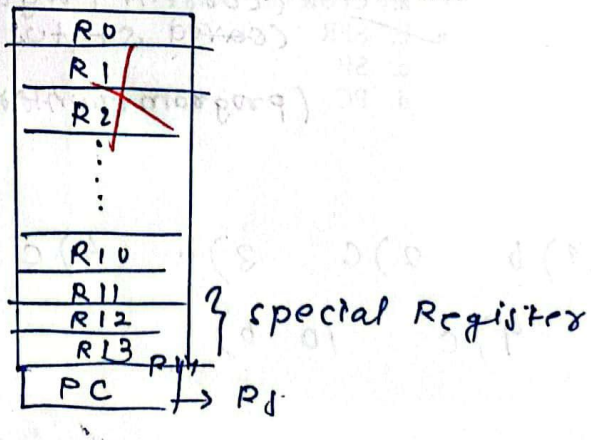
2. When the processor is executing in ARM state, then all instructions are _____ wide.
   a. 8bits
   b. 16bits
   c. 32bits
   d. 64bits

3. Which one of the following architecture has fewer number instructions?
   a. RISC (Reduced instructions set Architecture)
   b. CISC (complex instruction set Architecture)
   c. Both a and b
   d. None of the above

4. In PC Relative addressing, the address of the operand is calculated as:
   a. The sum of the base register and the offset
   b. The difference between the program counter and the operand address
   c. The sum of the program counter and the offset
   d. The difference between the base register and the operand address

   PC +

5. In ARM's Advanced Indexed Addressing Mode, which registers is typically used as the base register?
   a. R0
   b. R15 (PC)
   c. R7 (SP) (special purpose Reg)
   d. Any general-purpose register



Load Register

R8 [R9, R10] R8 [R9+R10]

6. In the ARM assembly code snippet below:
   LDR R8, [R9, R10]
   What does the instruction load into register R8, and which addressing mode is used?
   a. The value at the address [R9 + R10], Indexed addressing
   b. The value at the address [R9 - R10], Indexed addressing
   c. The value at the address [R9] + R10, Offset addressing
   d. An immediate value, Immediate Addressing

7. Write instructions to load value 0x95 into location with address 0x20.
   a. MOV R1,#0x20
      MOV R2,#0x95
      LDRB R2,[R1]
   b. MOV R1,#0x20
      MOV R2,#0x95
      LDR R2,R1
   c. MOV R1,#0x20
      MOV R2,#0x95
      STRB R2,[R1]
   d. MOV R1,#0x20
      MOV R2,#0x95
      STRB R2,R1

R1 → 0x95 0x20
R2 → 0x95

R1	0x20
R2	0x95

R2 | value | address |
|---|---|
| | 0x95 | 0x20 |

8. Show the status of the Z flag after the execution of the following program:
   MOV R2,#4
   MOV R3,#2
   MOV R4,#4
   SUBS R5,R2,R3
   SUBS R5,R2,R4

   a. Z=4
   b. Z=0
   c. Z=1
   d. Z=2

Reg	value
R2	4
R3	2
R4	4

R5, R2, R3
R5 → R2 − R3
R5 → 4 − 2 = 2 Z = 0
R5 → 4 − 4 = 0 Z = 1

Z Flag → zero.
Zero Flag is set to 1 Z = 1

9. A given ARM chip has the following address assignments. Calculate the space and the amount of memory given to the address range of 0x00100000 – 0x00100FFF for EEPROM
   a. 16K bytes
   b. 32K bytes
   c. 4K bytes
   d. 128K bytes

0x 00100000
0x 00100FFF

4095 + 1 = 4096

  00100FFF
− 00100000
  00000FFF

10. The flag register in the ARM is called the _____.
    a. CPSR (current program status register)
    b. SFR (saved status Flag Register
    c. SP
    d. PC (program counter)