Assignment – I

MANIPAL INSTITUTE OF TECHNOLOGY

BENGALURU

(A constituent unit of MAHE, Manipal)

Programme Name & Branch: **B.Tech – CSE /AI/Cyber Security**

Course Name & Code: Computer Organization and Architecture & CSE_ 2151/IT_2151

General instruction(s):

- Missing data if any may be assumed suitably.

1. Write a RISC program to find the factorial of a number
2. Write a ALP to find the sum of negative and odd integers between 1 and a given number. Write its equivalent RTD. Draw the Wilkes Design Architecture for the same. Also, write its equivalent Vector Code.
3. Perform the signed multiplication using Booth Multiplication for the following numbers:

   i) 20 x -13 ii) -12 x -11
4. A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

   a)Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

   b) When a program is executed, the processor reads data sequentially from the following word addresses: 1126, 1330, 1126, 2180, 1208, 1330

   All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss, if the cache is organized as a 2-way set-associative cache that uses the LRU replacement algorithm

5. A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

   a)Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

   b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176

   All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss, if the cache is organized as a 2-way set-associative cache that uses the LRU replacement algorithm