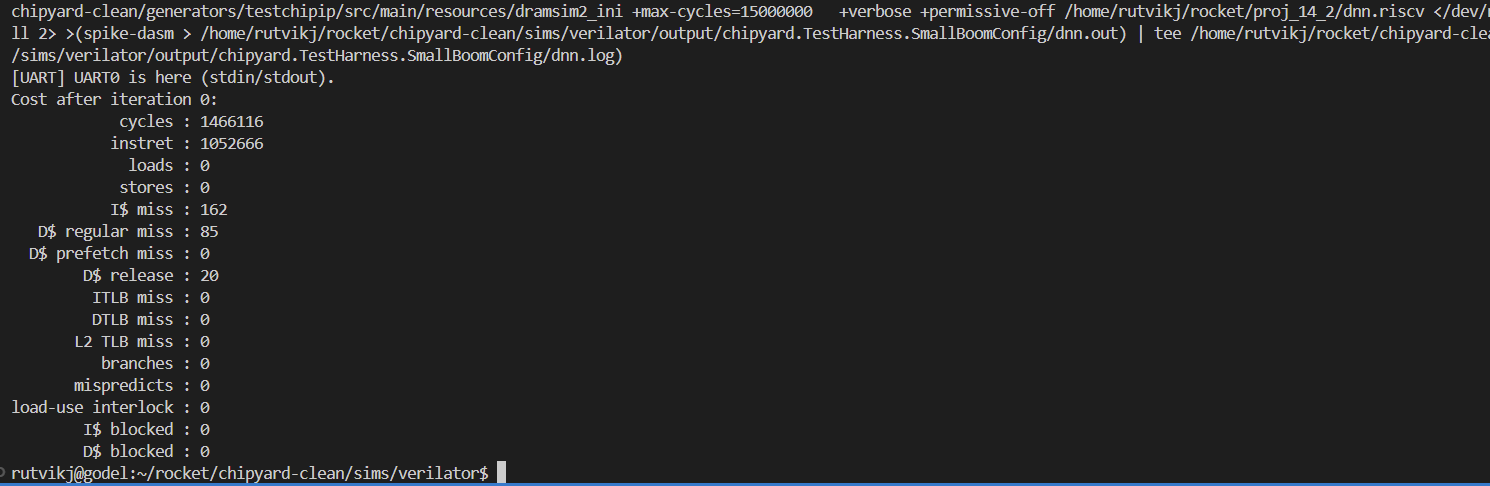
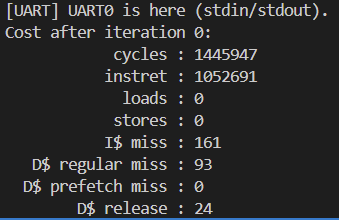
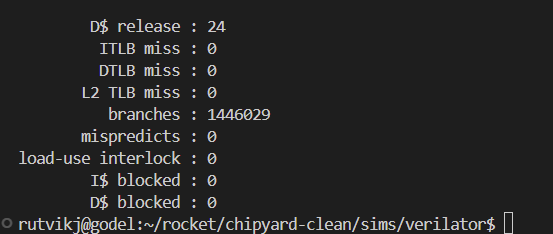
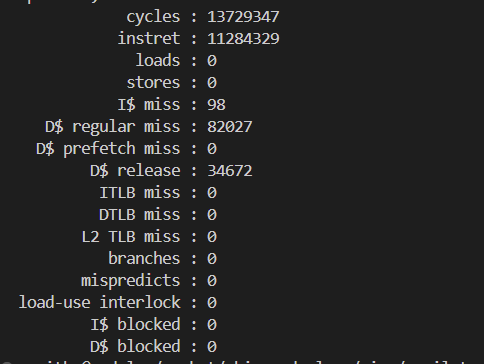
Dnn.c:  






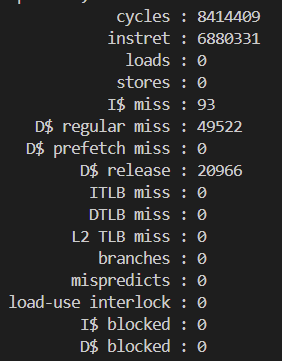
With TAGE BPD (dnn.c)



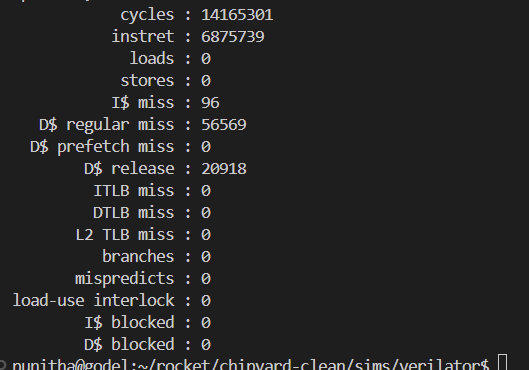
With Pseudo LRU and L1 prefetching (dnn.c)

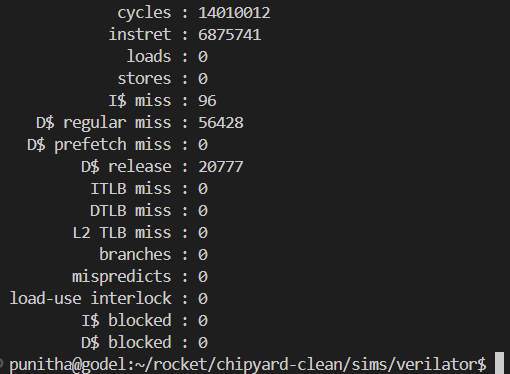


2 booms and a tage:

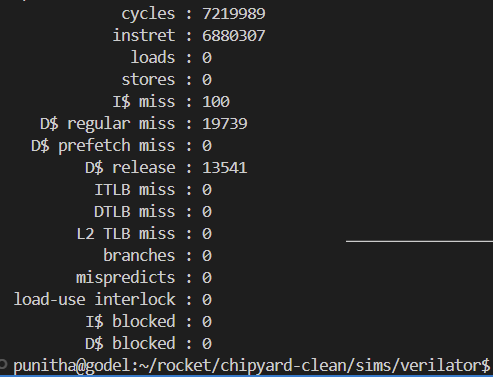


Just small boom:

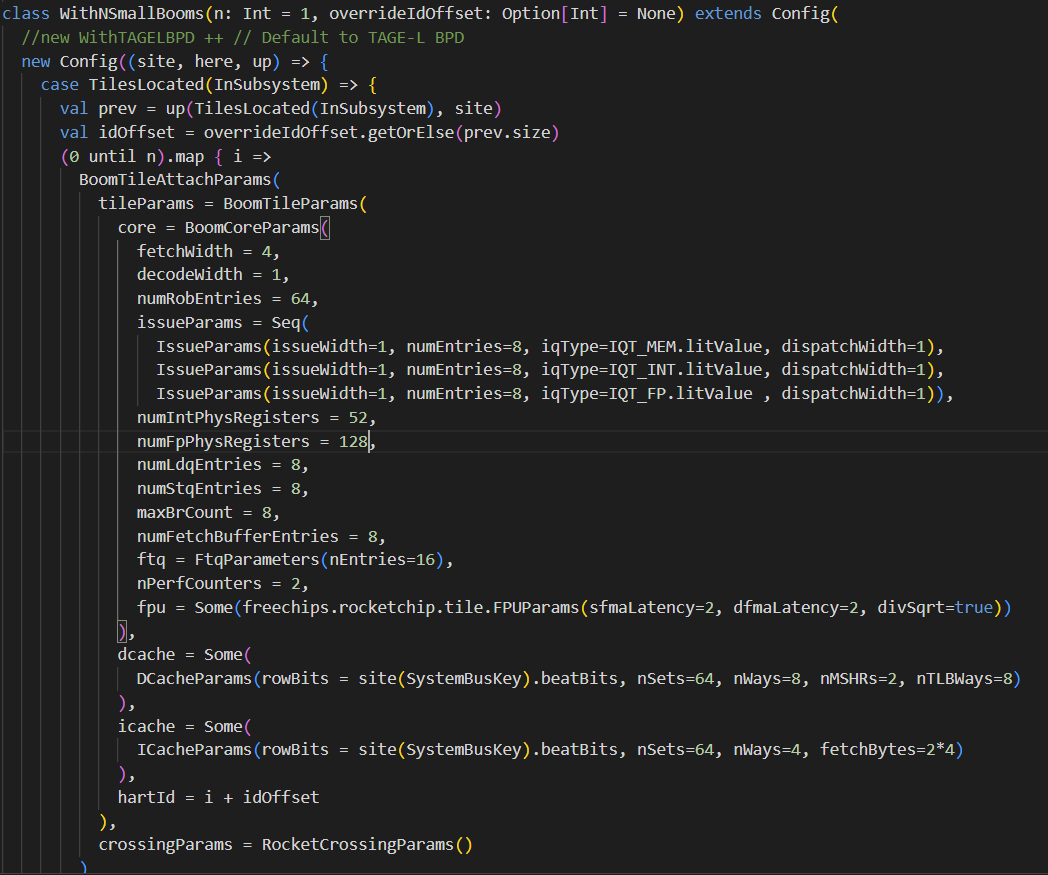


Fpu latency reduced and attempted 2 units for FMA:  


Decodewidth = 1 and numofRoB enteries = 64; LRU replacement policy and TAGE; Dcache =64; ways=8:

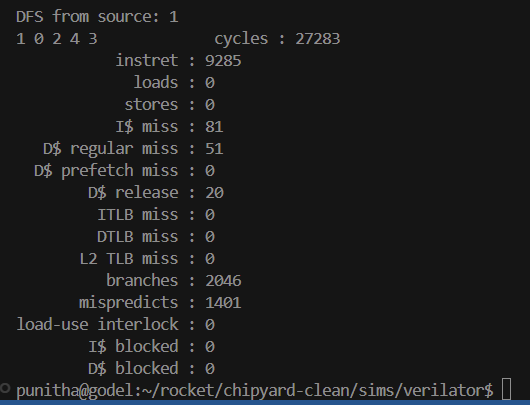


Final + fpphyregisters = 128

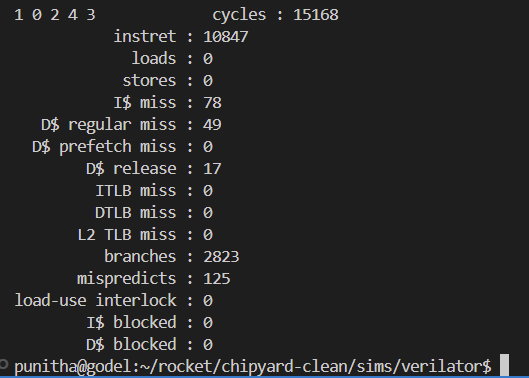
Final set up:  


Dfs.c:

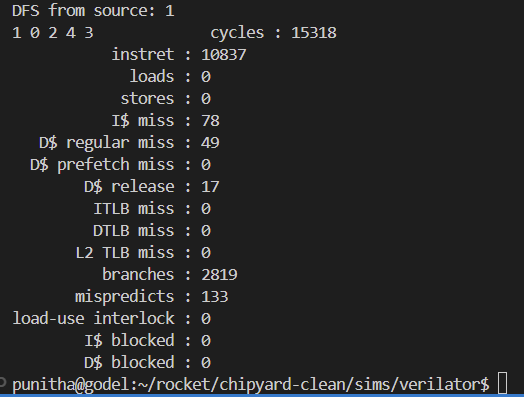
Just small boom:



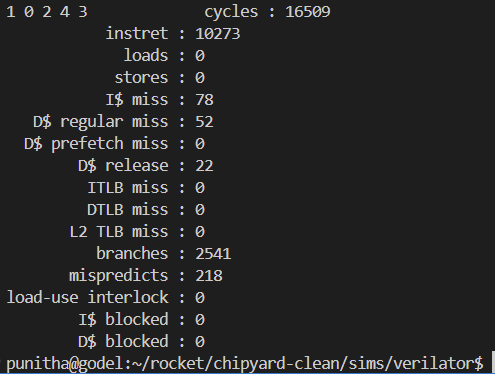
Tage + small boom:



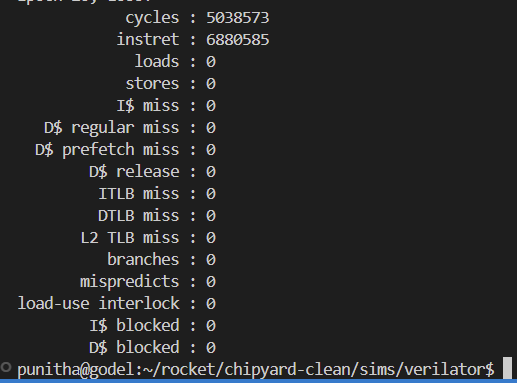
2 BPD + small boom:



Alpha (tourney) + small boom:

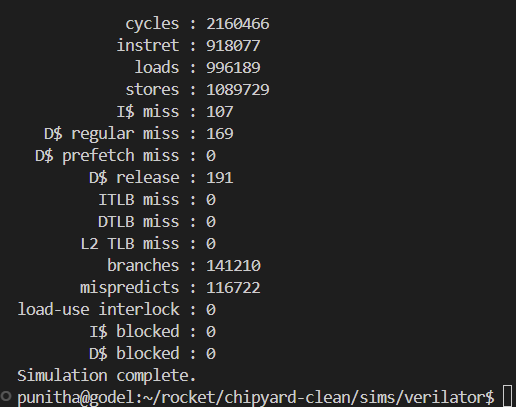


Dnn.c on Large boom:

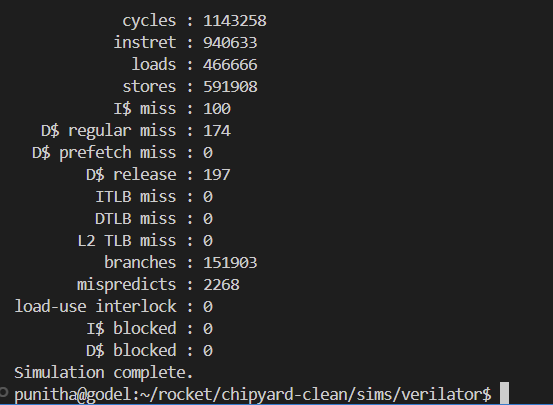


Heat.c:

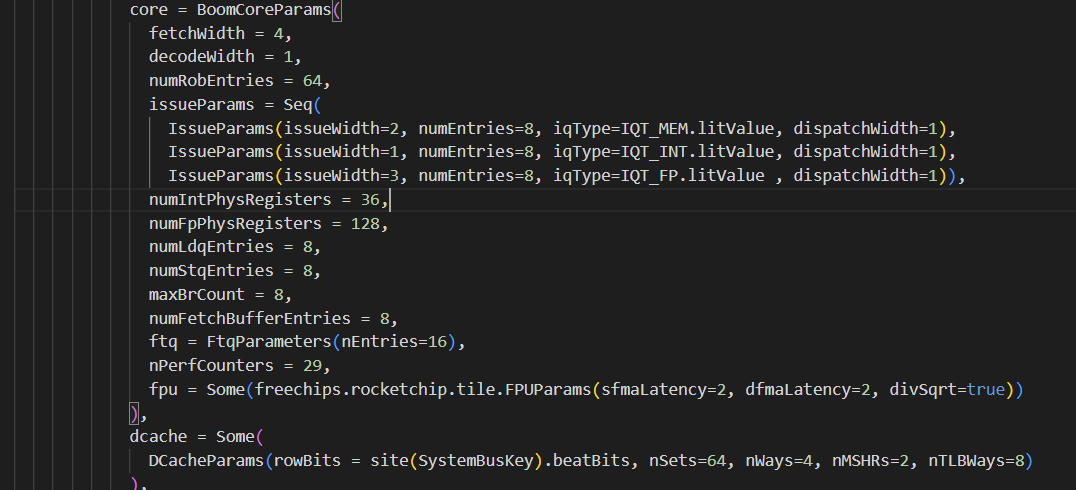
Baseline small boom:



Optimized:



Setup:



MSHR = 4

