FIGURE 2-3: PIC16F877/876 REGISTER FILE MAP

	Address I		Address		Address 1	Addre		
Indirect addr. (*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180	
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181	
PCL	02h	PCL	82h	PCL	102h	PCL	182	
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	18	
FSR	04h	FSR	84h	FSR	104h	FSR	18	
PORTA	05h	TRISA	85h		105h		18	
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	18	
PORTC	07h	TRISC	87h		107h		18	
PORTD ⁽¹⁾	08h	TRISD ⁽¹⁾	88h		108h		18	
PORTE ⁽¹⁾	09h	TRISE ⁽¹⁾	89h		109h		18	
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18	
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18	
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18	
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18	
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved ⁽²⁾	18	
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved ⁽²⁾	18	
T1CON	10h		90h		110h		19	
TMR2	11h	SSPCON2	91h		111h		19	
T2CON	12h	PR2	92h		112h		19	
SSPBUF	13h	SSPADD	93h		113h		19	
SSPCON	14h	SSPSTAT	94h		114h		19	
CCPR1L	15h	301 31741	95h		115h		19	
CCPR1H	16h		96h		116h		19	
CCP1CON	17h		97h	General	117h	General	19	
RCSTA	18h	TXSTA	98h	Purpose	118h	Purpose	19	
TXREG	19h	SPBRG	99h	Register 16 Bytes	119h	Register 16 Bytes	19	
RCREG	1Ah	OI DIXO	9Ah	10 Dytes	11Ah	To Dytes	19	
CCPR2L	1Bh		9Bh		11Bh		19	
CCPR2H	1Ch		9Ch		11Ch		19	
CCP2CON	1Dh				11Dh		19	
ADRESH	1Eh	ADRESL	9Dh 9Eh		11Eh		19 19	
	1Fh				11Fh		19	
ADCON0		ADCON1	9Fh					
	20h		A0h		120h		1A	
General		General		General		General		
Purpose Register		Purpose Register		Purpose Register		Purpose Register		
_		80 Bytes		80 Bytes		80 Bytes	4 -	
96 Bytes			EFh		16Fh		1E	
		accesses	F0h	accesses	170h	accesses	1F	
	フロト	70h-7Fh	C C h	70h-7Fh	17Fh	70h - 7Fh	1F	
Bank 0	7Fh	Bank 1	FFh	Bank 2	1 1/711	Bank 3	IF	
Darin 0						•		

2: These registers are reserved, maintain these registers clear.

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1. The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral features section.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 0											
00h ⁽³⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	27
01h	TMR0	Timer0 Mo	Timer0 Module Register								47
02h ⁽³⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	26
03h ⁽³⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	18
04h ⁽³⁾	FSR	Indirect Da	ata Memory /	Address Poir	iter					xxxx xxxx	27
05h	PORTA	_	_	PORTA Da	ta Latch whei	n written: POF	RTA pins whe	n read		0x 0000	29
06h	PORTB	PORTB Da	ata Latch wh	en written: P	ORTB pins w	hen read				xxxx xxxx	31
07h	PORTC	PORTC Da	ata Latch wh	en written: P	ORTC pins v	vhen read				xxxx xxxx	33
08h ⁽⁴⁾	PORTD	PORTD D	ata Latch wh	en written: P	ORTD pins v	vhen read				xxxx xxxx	35
09h ⁽⁴⁾	PORTE	_	_	_	_	_	RE2	RE1	RE0	xxx	36
0Ah ^(1,3)	PCLATH	_	-	_	Write Buffer	for the upper	5 bits of the I	Program Cou	unter	0 0000	26
0Bh ⁽³⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	20
0Ch	PIR1	PSPIF ⁽³⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	22
0Dh	PIR2	_	(5)	_	EEIF	BCLIF	_	_	CCP2IF	-r-0 00	24
0Eh	TMR1L	Holding re	Holding register for the Least Significant Byte of the 16-bit TMR1 Register								
0Fh	TMR1H	Holding re	gister for the	Most Signifi	cant Byte of t	the 16-bit TMI	R1 Register			xxxx xxxx	52
10h	T1CON	_	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	51
11h	TMR2	Timer2 Mo	dule Registe	er						0000 0000	55
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	55
13h	SSPBUF	Synchrono	us Serial Po	rt Receive B	uffer/Transm	it Register				xxxx xxxx	70, 73
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	67
15h	CCPR1L	Capture/C	Capture/Compare/PWM Register1 (LSB)								57
16h	CCPR1H	Capture/C	Capture/Compare/PWM Register1 (MSB)								57
17h	CCP1CON	_	_	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	58
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	96
19h	TXREG	USART Tra	USART Transmit Data Register								99
1Ah	RCREG	USART Re	eceive Data	Register						0000 0000	101
1Bh	CCPR2L	Capture/C	ompare/PWI	M Register2	(LSB)					xxxx xxxx	57
1Ch	CCPR2H	Capture/C	Capture/Compare/PWM Register2 (MSB)								57
1Dh	CCP2CON	_	_	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	58
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	116
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	_	ADON	0000 00-0	111

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.

Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

- 2: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.
- 3: These registers can be addressed from any bank.
- 4: PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.
- 5: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

PIC16F87X

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 1											
80h ⁽³⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)									27
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	19
82h ⁽³⁾	PCL	Program C	Program Counter (PC) Least Significant Byte								
83h ⁽³⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	18
84h ⁽³⁾	FSR	Indirect Da	ata Memory A	Address Poir	nter					xxxx xxxx	27
85h	TRISA	_	_	PORTA Da	ta Direction R	legister				11 1111	29
86h	TRISB	PORTB Da	ata Direction	Register						1111 1111	31
87h	TRISC	PORTC Da	ata Direction	Register						1111 1111	33
88h ⁽⁴⁾	TRISD	PORTD D	ata Direction	Register						1111 1111	35
89h ⁽⁴⁾	TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE Data	Direction B	its	0000 -111	37
8Ah ^(1,3)	PCLATH	_	_	_	Write Buffer	for the uppe	r 5 bits of the I	Program Cou	ınter	0 0000	26
8Bh ⁽³⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	20
8Ch	PIE1	PSPIE ⁽²⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	21
8Dh	PIE2	_	(5)	_	EEIE	BCLIE	_	_	CCP2IE	-r-0 00	23
8Eh	PCON	_	_	_	_	_	_	POR	BOR	qq	25
8Fh	_	Unimpleme	ented							_	_
90h	_	Unimpleme	ented							_	_
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	68
92h	PR2	Timer2 Pe	riod Register							1111 1111	55
93h	SSPADD	Synchrono	Synchronous Serial Port (I ² C mode) Address Register								
94h	SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	66
95h	_	Unimpleme	Unimplemented								
96h	_	Unimpleme	Unimplemented								_
97h	_	Unimpleme	ented							_	_
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	95
99h	SPBRG	Baud Rate	Generator F	Register						0000 0000	97
9Ah	_	Unimpleme	ented							_	_
9Bh	_	Unimpleme	ented							_	_
9Ch	_	Unimpleme	ented							_	_
9Dh	_	Unimpleme	ented							_	_
9Eh	ADRESL	A/D Result	t Register Lo	w Byte						xxxx xxxx	116
9Fh	ADCON1	ADFM	_		_	PCFG3	PCFG2	PCFG1	PCFG0	0 0000	112

- Legend: x = unknown, u = unchanged, q = value depends on condition, = unimplemented, read as '0', r = reserved.

 Shaded locations are unimplemented, read as '0'.

 Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

 2: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.

 - These registers can be addressed from any bank.
 PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.
 PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 2											
100h ⁽³⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)									27
101h	TMR0	Timer0 Module Register									47
102h ⁽³⁾	PCL	Program Counter's (PC) Least Significant Byte									26
103h ⁽³⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	18
104h ⁽³⁾	FSR	Indirect Da	ata Memory A	Address Poir	iter					xxxx xxxx	27
105h	_	Unimpleme	ented							_	_
106h	PORTB	PORTB Da	ata Latch wh	en written: P	ORTB pins w	hen read				xxxx xxxx	31
107h	_	Unimpleme	ented							_	_
108h	_	Unimpleme	ented							_	_
109h	_	Unimpleme	ented							_	_
10Ah ^(1,3)	PCLATH	_	_	_	Write Buffer	for the upper	r 5 bits of the I	Program Cou	ınter	0 0000	26
10Bh ⁽³⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	20
10Ch	EEDATA	EEPROM Data Register Low Byte									41
10Dh	EEADR	EEPROM Address Register Low Byte									41
10Eh	EEDATH	EEPROM Data Register High Byte								xxxx xxxx	41
10Fh	EEADRH	— — EEPROM Address Register High Byte								xxxx xxxx	41
Bank 3											
180h ⁽³⁾	INDF	Addressing	this location	n uses conte	nts of FSR to	address data	a memory (no	t a physical r	egister)	0000 0000	27
181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	19
182h ⁽³⁾	PCL	Program C	ounter (PC)	Least Signi	ficant Byte					0000 0000	26
183h ⁽³⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	18
184h ⁽³⁾	FSR	Indirect Da	ata Memory A	Address Poir	iter		•	•	•	xxxx xxxx	27
185h	_	Unimpleme	ented							_	_
186h	TRISB	PORTB Data Direction Register								1111 1111	31
187h	_	Unimpleme	Unimplemented								_
188h	_	Unimplemented								_	_
189h	_	Unimplemented								_	_
18Ah ^(1,3)	PCLATH	— — Write Buffer for the upper 5 bits of the Program Counter								0 0000	26
18Bh ⁽³⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	20
18Ch	EECON1	EEPGD	_	_	_	WRERR	WREN	WR	RD	x x000	41, 42
18Dh	EECON2	EEPROM Control Register2 (not a physical register)									41
18Eh	_	Reserved maintain clear								0000 0000	_
18Fh	_	Reserved maintain clear								0000 0000	_

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
 Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.

- 3: These registers can be addressed from any bank.
 4: PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.
- **5:** PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.