Essentials of ICT
ICT1113

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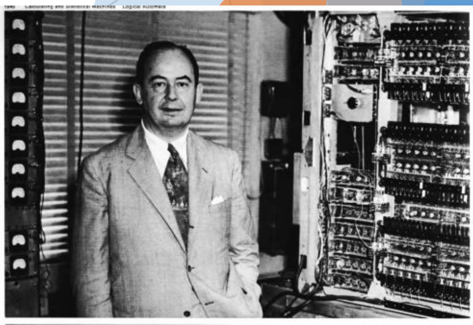
Lecture 03
Computer Architecture &
System Unit

Learning Objectives

- After successfully completing this chapter, you should be able to:
  - State the concepts of Von Neumann Architecture
  - Explain the difference between hardware and software approaches
  - Explain the operations of instruction cycle
  - Describe the three types of system bus

Von Neumann Architecture

- Most of the contemporary computer designs are based on concepts developed by John von Neumann
- It is based on **three key concepts:**
  - Data and instructions are stored in a single read-write memory
  - The contents of this memory are addressable by location, without regard to the type of data contained there
  - Execution occurs in a sequential fashion from one instruction to the next

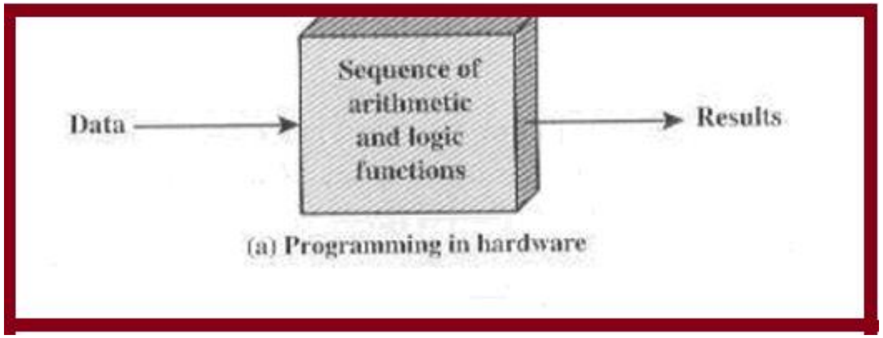


What is a Hardwired Program?

- A set of basic logic components can be combined in a way to store binary data and perform arithmetic and logical operations on that data
- The process of connecting these components produces a program in the **form of hardware**.
- This resulting program is called a hardwired program

Hardware and Software Approaches

- Hardware Approach



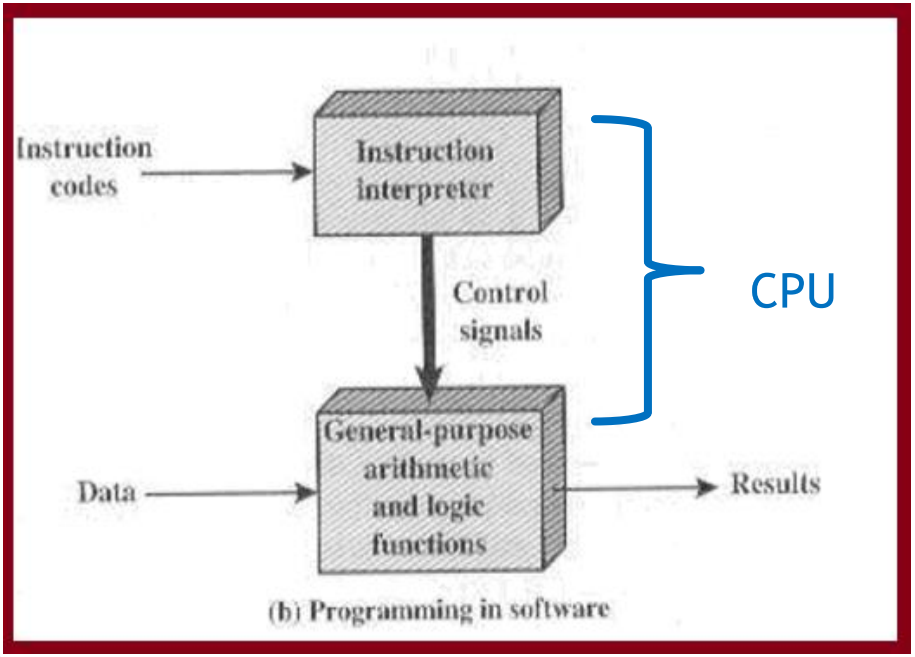
(a) Programming in hardware

✓ Special Purpose Configuration.

✓ Input → Data.

✓ Perform a specific function.

- Software Approach



(b) Programming in software

✓ General Purpose Configuration.

✓ Input → Data + Control Signals.

✓ Perform various functions depending on control signals.

✓ No need to rewrite the hardware for each new program.

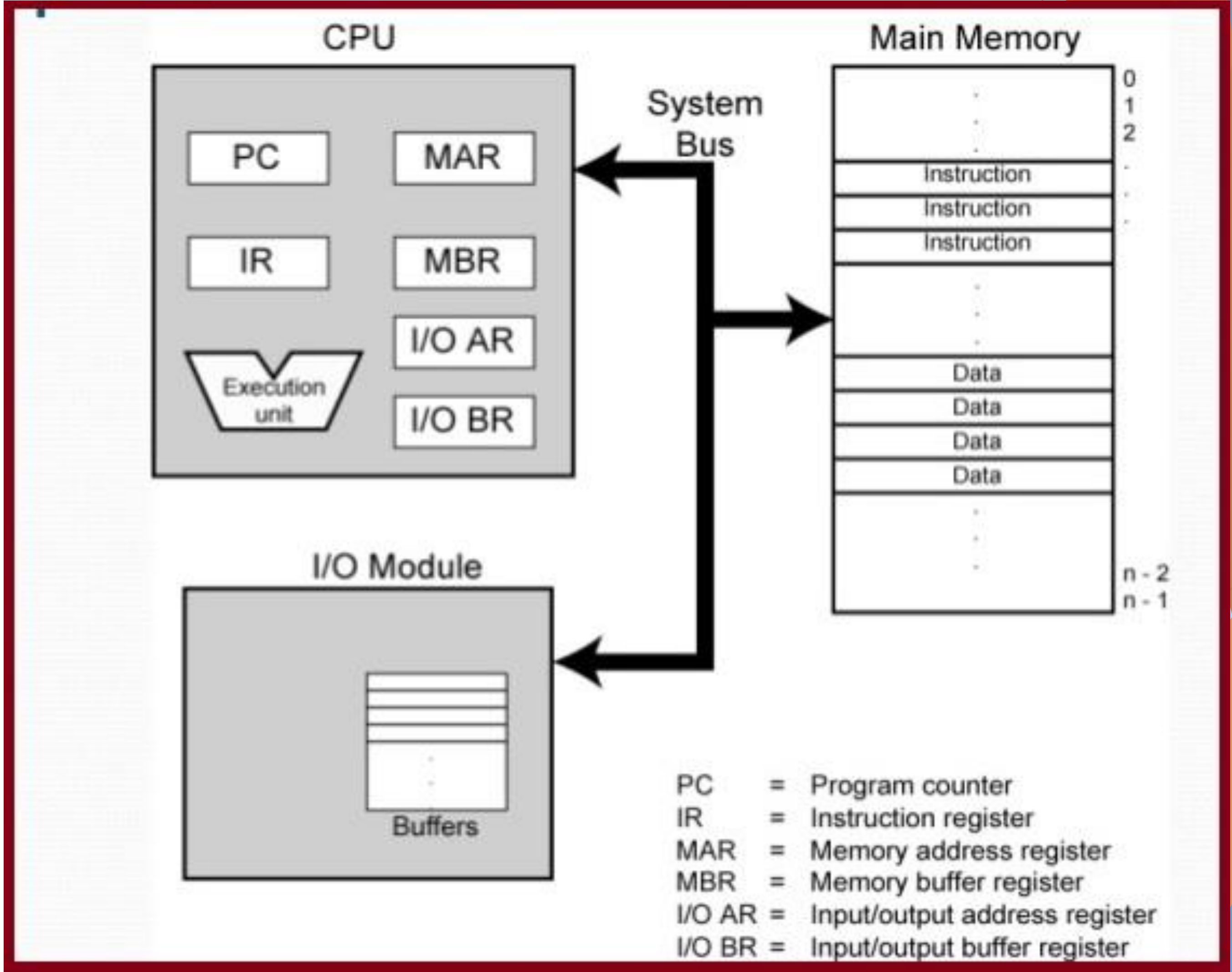
✓ A sequence of instuction codes are called software.

Other Computer Components

- **I/O component** is used for accepting data and instruction in some form and converting them into an internal form of signals usable by the system, and for reporting results in the form of an output module
- **Memory** module (main memory) is a place both data and instructions are stored temporarily

Computer Components: Top Level View

- CPU + Memory + I/O Module



PC	=	Program counter
IR	=	Instruction register
MAR	=	Memory address register
MBR	=	Memory buffer register
I/O AR	=	Input/output address register
I/O BR	=	Input/output buffer register

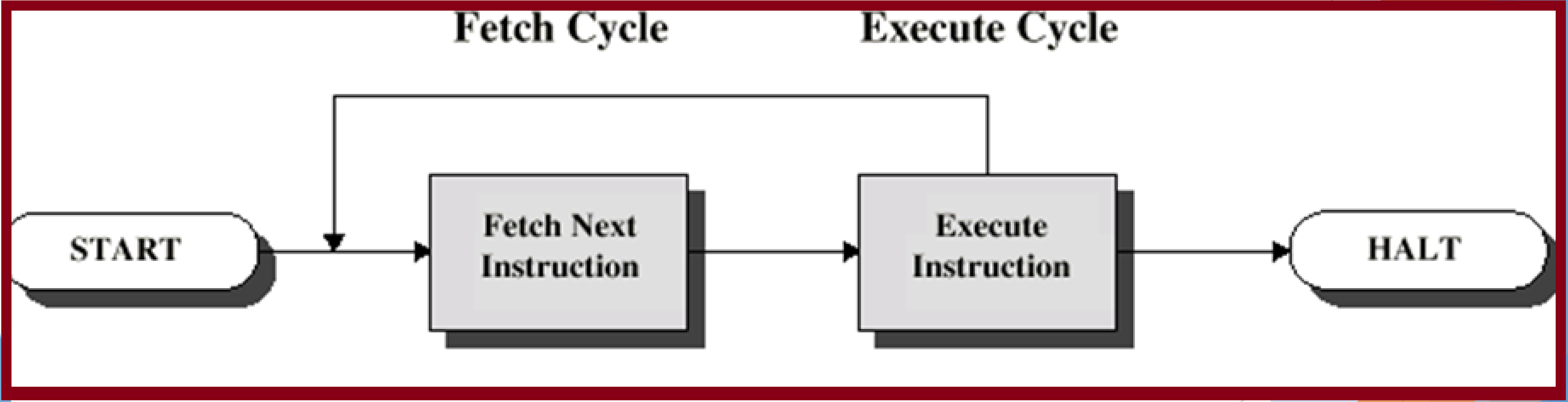
- The CPU exchanges data with memory. For this purpose, it typically makes use of two internal registers:
    - **Memory address register (MAR)** - specifies the address in memory for the next read or write
    - **Memory buffer register (MBR)** - contains the data to be written into memory or receives the data read from memory
- Similarly,
    - **I/O address register (I/OAR) -** specifies a particular I/O device
    - **I/O buffer register (I/OBR) -** uses for the exchange of data between an I/O module and the CPU

Computer Function

- The basic function of a computer is to execute a program, which consists of a set of instructions stored in memory
- The instruction is in the form of a binary code that specifies what action the CPU is to take.
- Processing required for a single instruction is called an **Instruction cycle**

Instruction Cycle

- Two steps:
  - Fetch
  - Execute



Fetch Cycle

- Program Counter (PC) holds address of next instruction to fetch
- Processor fetches(reads) instruction from memory location pointed to by PC
- Increment PC by 1
  - Unless told otherwise
- The fetched instruction is loaded into Instruction Register (IR)
- The instruction contains bits that specify the action the processor is to take
- Processor interprets instruction and performs required actions

Execute Cycle

- The processor actions fall into four categories
- **Processor-memory**
  - data transfer between CPU and main memory
- **Processor - I/O**
  - Data transfer between CPU and I/O module
- **Data processing**
  - Some arithmetic or logical operation on data
- **Control**
  - Alteration of sequence of operations
  - e.g:- jump
- An instruction’s execution may involve a combination of these actions

CPU

- main components of a computer
  - CPU , Memory, I/O devices, System interconnection (system bus)
- CPU is the most interesting and most complex component
- fundamental operation
  - execute programs
- program
  - a sequence of stored instructions
- program execution
  - **instruction execution**

CPU Operation

CPU must :

- Fetch instruction
  - CPU **reads** an instruction from memory
- Interpret instruction
  - instruction is **decoded** to determine what action is required
- Fetch data
  - execution of an instruction may require **reading data from memory or I/O** module
- Process data
  - execution of an instruction may require **performing some arithmetic or logical operation** on data
- Write data

CPU components

- **main components** of the CPU :
  - **Arithmetic and Logic Unit (ALU)**

ALU does the actual computation or processing of data

  - **Control unit**

Controls the movement of data and instruction into and out of the CPU and controls the operation of the ALU

  - **Registers**

Store instructions and data temporarily while an instruction is being executed

  - **Internal CPU interconnections**

CPU Internal Structure

- Internal CPU interconnections

- **Data transfer path** - Internal CPU bus transfer data between the various registers and the ALU

- **Logic control path -** hardware that tells the data path what to do, in terms of switching, operation selection, data movement between ALU components

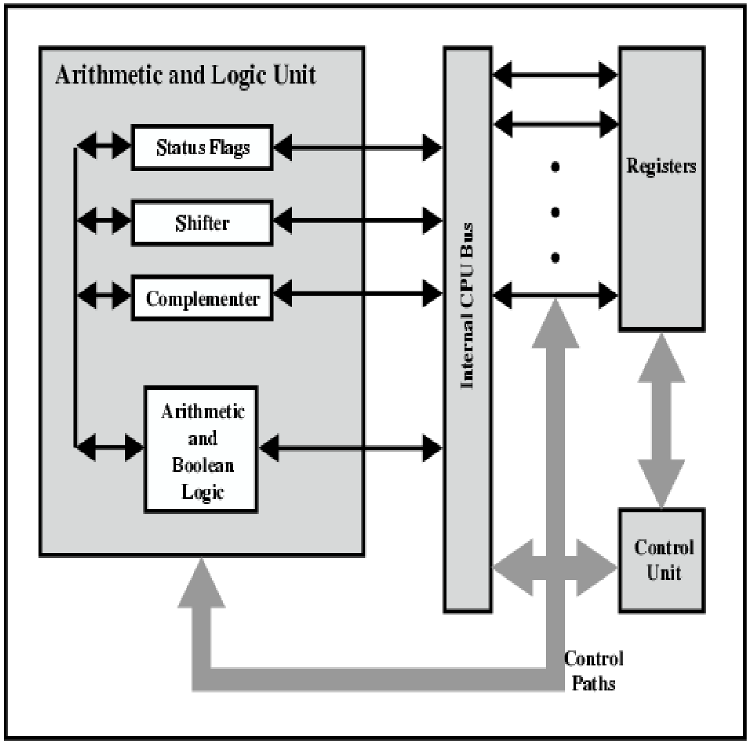


Figure 12.2 Internal Structure of the CPU

Arithmetic and Logic Unit

- Performs arithmetic and logical operations on data
  - Integer arithmetic operations (addition, subtraction, multiplication, division)
  - logic operations (AND,NOT,OR, XOR)
  - Left or right shift
- ALU loads data from input registers
- Control Unit tells the ALU what operation to perform on that data
- ALU stores its result into an output register
- ALU may also set flags as the result of an operation

Control Unit

- Controls the entire operation of the computer
- Maintains order and directs the operation of the entire system
- Controls the data flow between CPU and peripherals (including memory)
- Provides status, control and timing signals that memory and I/O devices require
- Sends suitable control signals to other components to perform necessary steps to execute the instruction

Register Organization

- set of registers → faster, smaller and more expensive
- registers in the CPU can be categorized into two groups:
  - User-visible registers
  - Control and status registers
- **User-visible registers:**

enables the machine - or assembly-language programmer to minimize main memory reference by optimizing use of registers(Ex: General Purpose Registers, Data Registers, Address Registers ,Condition Codes)

- **Control and status registers:**

these are used by the control unit to control the operation of the CPU (Ex: PC, IR..)

- No clear separation
  - E.g: on some machines the PC is user visible (Pentium)

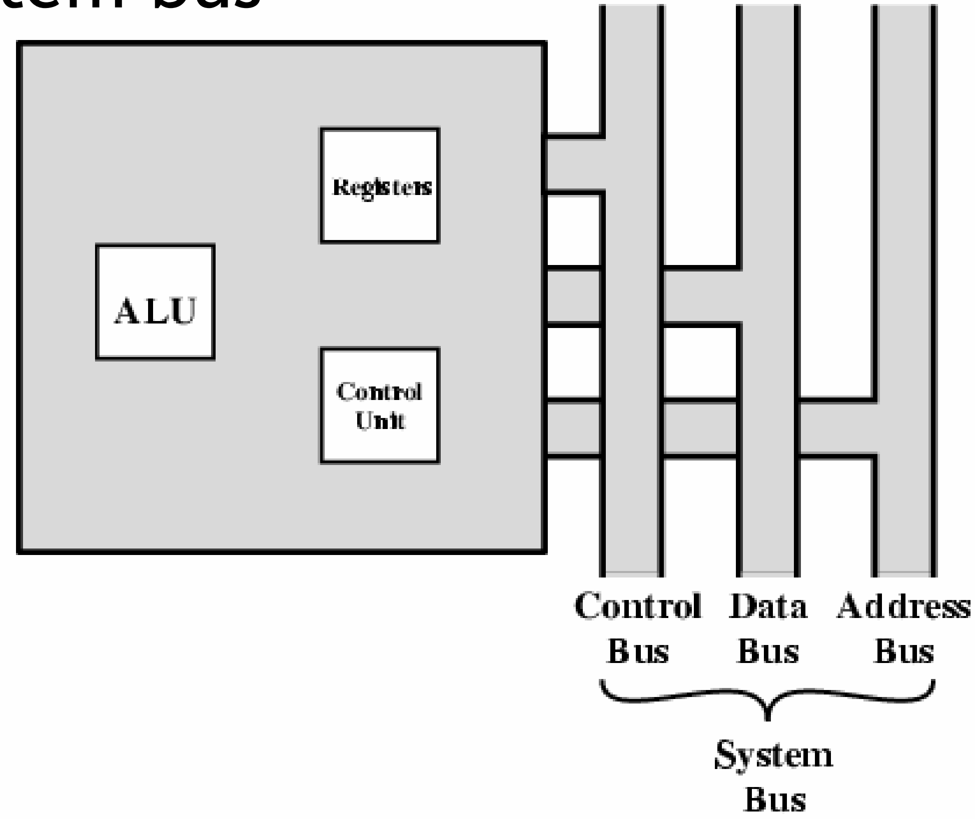
Control and Status Registers

- Employed to control the operation of the CPU
- four registers are essential to instruction execution:
  - **Program counter (PC)**
    - Contains the address of an instruction to be fetched
  - **Instruction register (IR)**
    - Contains the most recently fetched instruction
  - **Memory address registers (MAR)**
    - Contains the address of a location in memory
  - **Memory buffer register (MBR)**
    - Contains a word of data to be written to memory or the word most recently read

CPU With System Bus

- System bus

CPU is connected to the rest of the system through system bus



System Bus

- Connects major computer components.(Processor, I/O, Memory)
- Computer interconnection structures are based on one or more system buses.
- Classified into three functional groups (based on the functions of lines)
  - Data Bus
  - Address Bus
  - Control Bus
- In addition there may be power distribution lines also

Data Bus

- Carries data among system modules.
  - Remember that there is no difference between “data” and “instruction” at this level
- Width = Number of Lines
  - 8, 16, 32, 64 or more lines
  - One bit per line at one time
- Ex:-
  - The data bus is 32 bits wide (32 lines) and each instruction is 64 bits long. Then the processor must access the memory module twice during each instruction cycle.

Address bus

- Identify the source or destination of data
  - e.g. CPU needs to read an instruction (data) from a given location in memory.Puts the address of desired data on the address line.
- Width = Maximum memory capacity of system

  n-bit width address bus: 2^n addressable words
- Unidirectional

Control Bus

- Control the access to and the use of the data and address lines.
- Control signals transmit both command and timing information among system modules.
  - Timing Signals – Validity of data and addresses.
  - Command Signals – Operations to be performed.

Questions ???