C335
Computer Structures

Final Exam Review

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Coverage

- About 80% of the questions will be from what we learned since last mid-term exam
- The rest questions will be from what learned before.

Pipelined Datapath Design

- Single cycle, multiple cycle, vs. Pipelining
  - CPU performance – some calculations
- Pipelining
  - The laundry analogy
  - Throughput vs. latency
- Pipeline hazards
  - Data, structure, control
  - What are the causes?
  - How to “fix” them?

Memory hierarchies

- Memory hierarchy
  - Motivations: why we use cache?
  - Why cache help?
- Cache design
  - Direct-mapped cache
    - The “TIO” cache mnemonic
    - How it works
    - Block size tradeoffs
    - Sources of cache misses
  - Fully associative cache
  - N-way set associative cache
  - Cache block replacement policy
  - Cache write policy

Input/Output

- Important metrics of I/O devices
  - Dependability, diversity, and others
- How CPU directs the I/O devices
  - Standard I/O
  - Memory-mapped I/O, how?
- How the I/O device com. with CPU
  - Polling-based, how?
  - Interrupt-driven, how?
- I/O performance measure
- Types of buses