

## C335 Homework #6 Solution

### Part I (9 points)

Assume that X consists of 2 bits,  $x_1$  and  $x_0$ , and Y consists of 2 bits,  $y_1$  and  $y_0$ . Write logic functions that are true if and only if

- (A)  $X < Y$ , where X and Y are thought of as unsigned binary numbers
- (B)  $X < Y$ , where X and Y are thought of as signed (two's complement) numbers
- (C)  $X = Y$

$x_1$	$x_0$	$y_1$	$y_0$	F(A)	F(B)	F(C)
0	0	0	0	0	0	1
0	0	0	1	1	1	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	0
0	1	0	1	0	0	1
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	0	1	1	1	1	0
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	0	0
1	1	1	1	0	0	1

$$F(A) = x_1'x_0'y_1'y_0 + x_1'x_0'y_1y_0' + x_1'x_0'y_1y_0 + x_1'x_0y_1y_0' + x_1'x_0y_1y_0 + x_1x_0'y_1y_0 \\ (= x_1'x_0'y_0 + x_1'y_1 + x_0'y_1y_0)$$

$$F(B) = x_1'x_0'y_1'y_0 + x_1x_0'y_1'y_0' + x_1x_0'y_1'y_0 + x_1x_0'y_1y_0 + x_1x_0y_1'y_0' + x_1x_0y_1'y_0' \\ (= x_1'x_0'y_0 + x_1y_1' + x_0'y_1'y_0)$$

$$F(C) = x_1'x_0'y_1'y_0' + x_1'x_0y_1'y_0 + x_1x_0'y_1y_0' + x_1x_0y_1y_0$$

## Part II (12 points)

Describe the effect that a single stuck-at-0 fault (i.e., regardless of what it should be, the signal is always 0) would have for the signals shown below, in the single-cycle datapath (shown in the figure in Part IV). Which instructions (R-type, lw, sw, or beq), if any, will not work correctly? Explain why.

Consider each of the following faults separately:

- A) RegWrite = 0
- B) ALUOp0 = 0
- C) ALUOp1 = 0
- D) Branch = 0
- E) MemRead = 0
- F) MemWrite = 0

A) RegWrite = 0: All R-format instructions, in addition to lw, will not work because these instructions will not be able to write their results to the register file.

B) ALUOp0 = 0: beq instruction will not work correctly.

C) ALUOp1 = 0: R-format instructions will not work correctly.

D) Branch (or PCSrc) = 0: beq will not execute correctly. The branch instruction will always be not taken even when it should be taken.

E) MemRead = 0: lw will not execute correctly because it will not be able to read data from memory.

F) MemWrite = 0: sw will not work correctly because it will not be able to write to the data memory.

### Part III (12 points)

This exercise is similar to Part II, but this time consider stuck-at-1 faults. Describe the effect that a single stuck-at-1 fault (i.e., regardless of what it should be, the signal is always 1) would have for the signals shown below, in the single-cycle datapath (shown in the figure in Part IV). Which instructions (R-type, lw, sw, or beq), if any, will not work correctly? Explain why.

Consider each of the following faults separately:

- A) RegWrite = 1
- B) ALUop0 = 1
- C) ALUop1 = 1
- D) Branch = 1
- E) MemRead = 1
- F) MemWrite = 1

A) RegWrite = 1: sw and beq should not write results to the register file. sw (beq) will overwrite a random register with either the store address (branch target) or random data from the memory data read port.

B) ALUop0 = 1: lw, sw, and R format instructions will not work correctly.

C) ALUop1 = 1: lw, sw, and beq will not work correctly.

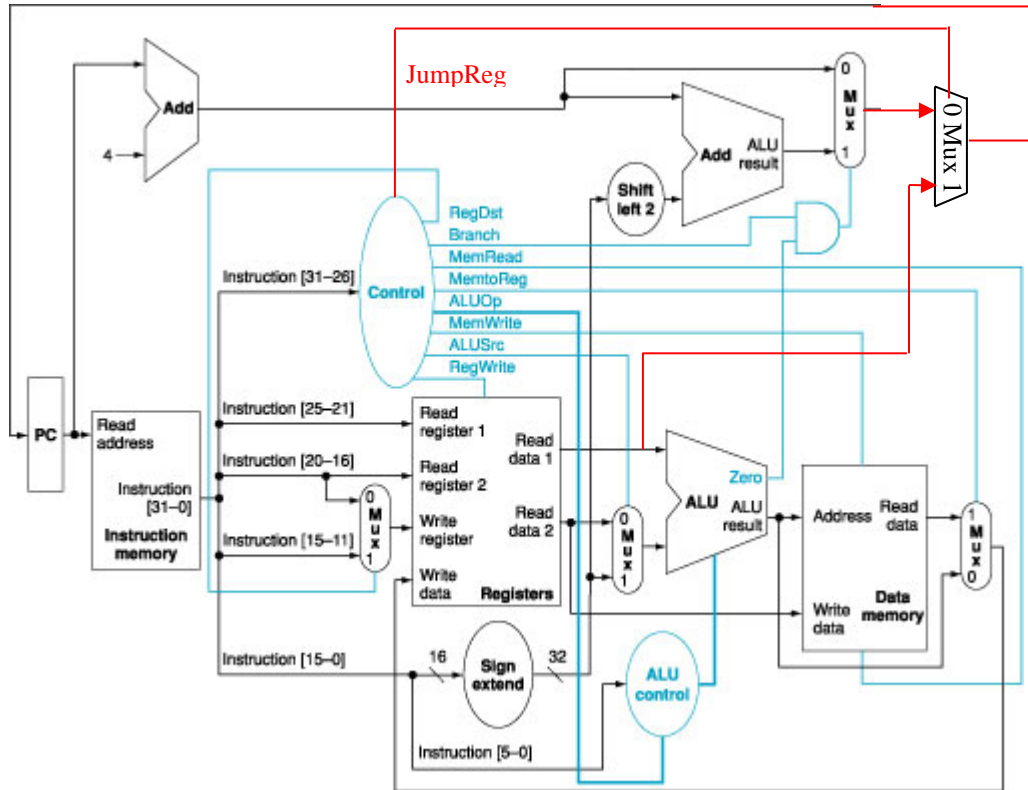
D) Branch = 1: Instructions other than branches (beq) will not work correctly if the ALU Zero signal is raised. An R-format instruction that produces zero output will branch to a random address determined by its least significant 16 bits.

E) MemRead = 1: All instructions will work correctly (data memory is always read, but memory data is never written to the register file except in the case of lw.). However, unnecessary memory reading may cause some other potential problems which we should avoid.

F) MemWrite = 1: Only sw will work correctly. The rest of instructions will store their results in the data memory, while they should not.

## Part IV (7 points)

We wish to add the instructions jr (jump register) to the single-cycle datapath described in the lectures. Add any necessary datapaths and control signals to the single-cycle datapath shown in the Figure below.



Instr	RegDst	ALUSrc	MemReg	RegWr	MemRd	MemWr	Branch	ALUOp	JumpReg
jr	X	X	X	0	0	0	X	XX	1