C335 Homework #1 Solutions

Part I (4 points)

Textbook, pp 54-55, Exercises 1.2. Please fill your answers into the following table.

	Match which of the eight ideas?
a.	Performance via Pipelining
b.	Dependability via Redundancy
c.	Performance via Prediction
d.	Make the Common Case Fast
e.	Hierarchy of Memories
f.	Performance via Parallelism
g.	Design for Moore's Law
h.	Use Abstraction to Simplify Design

Part II (9 points)

Consider three different processors P1, P2, and P3 executing the same instruction set with the clock rates and CPIs given in the following table.

Processor	Clock Rate	CPI
P1	2 GHz	1.5
P2	1.5 GHz	1.0
P3	3 GHz	2.5

(1) Which processor has the highest performance?

$$\text{performance of P1 (instructions/sec)} = 2 \times 10^9 / 1.5 = 1.33 \times 10^9$$
$$\text{performance of P2 (instructions/sec)} = 1.5 \times 10^9 / 1.0 = 1.5 \times 10^9$$
$$\text{performance of P3 (instructions/sec)} = 3 \times 10^9 / 2.5 = 1.2 \times 10^9$$

(2) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

$$\text{cycles(P1)} = 10 \times 2 \times 10^9 = 20 \times 10^9 \text{ s}$$
$$\text{cycles(P2)} = 10 \times 1.5 \times 10^9 = 15 \times 10^9 \text{ s}$$
$$\text{cycles(P3)} = 10 \times 3 \times 10^9 = 30 \times 10^9 \text{ s}$$

$$\text{time} = (\text{No. instr.} \times \text{CPI})/\text{clock rate, then No. instructions} = \text{No. cycles/CPI}$$

$$\text{instructions(P1)} = 20 \times 10^9 / 1.5 = 13.33 \times 10^9$$
$$\text{instructions(P2)} = 15 \times 10^9 / 1 = 15 \times 10^9$$
$$\text{instructions(P3)} = 30 \times 10^9 / 2.5 = 12 \times 10^9$$

(3) We are trying to reduce the time by 30% but this leads to an increase of 20% in CPI. What clock rate should we have to get this time reduction?

$$\text{CPI} = \text{CPI} \times 1.2, \text{ then CPI(P1)} = 1.8, \text{CPI(P2)} = 1.2, \text{CPI(P3)} = 3$$

$$f = \text{No. instr.} \times \text{CPI/time, then}$$

$$f(\text{P1}) = 13.33 \times 10^9 \times 1.8/7 = 3.42 \text{ GHz}$$
$$f(\text{P2}) = 15 \times 10^9 \times 1.2/7 = 2.57 \text{ GHz}$$
$$f(\text{P3}) = 12 \times 10^9 \times 3/7 = 5.14 \text{ GHz}$$

Part III (9 points)
Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.5 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

(1) Given a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C and 20% class D, which implementation is faster?

CPU exec. time (P1) = 10^6 * (.10*1+.20*2+.50*3+.20*4) / (1.5 * 10^9) = 0.00187s = 1.87e-3s
CPU exec. time (P2) = 10^6 * (.10*2+.20*2+.50*2+.20*2) / (2.0 * 10^9) = 0.001s = 1.00e-3s

(2) What is the global CPI for each implementation?

CPI (P1) = .10*1+.20*2+.50*3+.20*4 = 2.8
CPI (P2) = .10*2+.20*2+.50*2+.20*2 -= 2.0

(3) Find the clock cycles required in both cases.

Clock Cycles (P1) = 10^6 * (.10*1+.20*2+.50*3+.20*4) = 2.8e+6
Clock Cycles (P2) = 10^6 * (.10*2+.20*2+.50*2+.20*2) = 2.0e+6

Part IV (8 points)
Assume you are in a company that will market a certain IC chip. The fixed costs, including R&D, fabrication and equipments, and so on, add up to $500,000. The cost per wafer is $6000, and each wafer can be diced into 2000 dies. The die yield is 50%. Finally, the dies are packaged and tested, with a cost of $14 per chip. The test yield is 50%; only those that pass the test will be sold to customers. If the retail price is 50% more than the cost, at least how many chips have to be sold to break even? **Show your steps**

Cost per Chip = (6000 + 2000*50%*14) / (2000*50%*50%) = 20000/400 = 40

Price = 40 * (1 + 50%) = 60

If we need to sell n chips, then 500,000 + 40*n = 60 * n, so n = 25,000