CS 6290 High Performance Computer Architecture

Lab 2 Report

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1.0 Default Configuration

The traces are run using default configuration.

MSHR Size : 4	Cache Size : 512KB	Type : 4 way set associative
D-cache latency : 5 cycles	DRAM Row Buffer Hit latency : 100 cycles	DRAM Row Buffer Miss latency : 200 cycles
DRAM_BANK_NUM : 4	DRAM_PAGE_SIZE : 2KB	

The results of the execution are as follows.

Memory Intensive Trace	**Non Memory Intensive Trace**
Total instruction: 10057019	Total instruction: 7583269
Total cycles: 35893678	Total cycles: 30307751
IPC: 0.280189	IPC: 0.250209
Total I-cache miss: 0	Total I-cache miss: 0
Total D-cache miss: 15693	Total D-cache miss: 3225
Total D-cache hit: 3626739	Total D-cache hit: 3876379
Total data hazard: 883472	Total data hazard: 488849
Total control hazard : 2050615	Total control hazard : 1705561
Total DRAM ROW BUFFER Hit: 942	Total DRAM ROW BUFFER Hit: 905
Total DRAM ROW BUFFER Miss: 12833	Total DRAM ROW BUFFER Miss: 527
Total Store-load forwarding: 18	Total Store-load forwarding: 15

2.0 Different Cache Sizes

Now, we vary cache size and analyze the results

2.1 Memory intensive trace

Cache Size : 128K	**Cache Size : 512K**
Total instruction: 10057019	Total instruction: 10057019
Total cycles: 35894697	Total cycles: 35893678
IPC: 0.280181	IPC: 0.280189
Total I-cache miss: 0	Total I-cache miss: 0
Total D-cache miss: 15739	Total D-cache miss: 15693
Total D-cache hit: 3626693	Total D-cache hit: 3626739
Total data hazard: 884498	Total data hazard: 883472
Total control hazard : 2050615	Total control hazard : 2050615
Total DRAM ROW BUFFER Hit: 945	Total DRAM ROW BUFFER Hit: 942
Total DRAM ROW BUFFER Miss: 12864	Total DRAM ROW BUFFER Miss: 12833
Total Store-load forwarding: 18	Total Store-load forwarding: 18

Cache Size : 1024K	**Cache Size 2048K**
Total instruction: 10057019 Total cycles: 35890513 IPC: 0.280214 Total I-cache miss: 0 Total D-cache miss: 15550 Total D-cache hit: 3626882 Total data hazard: 880708 Total control hazard : 2050615 Total DRAM ROW BUFFER Hit: 920 Total DRAM ROW BUFFER Miss: 12779 Total Store-load forwarding: 16	Total instruction: 10057019 Total cycles: 35890483 IPC: 0.280214 Total I-cache miss: 0 Total D-cache miss: 15549 Total D-cache hit: 3626883 Total data hazard: 880708 Total control hazard : 2050615 Total DRAM ROW BUFFER Hit: 920 Total DRAM ROW BUFFER Miss: 12778 Total Store-load forwarding: 16

We can draw following inferences from the results obtained above.

1. Increase in D-cache size results in more number of hits. But this behavior can be seen till increase in cache sizes up to 1MB. After that, increasing the cache size does not affect the cache hits. This is because of the fact that the application has utilized all the caching that it needs and the misses it gets are the compulsory misses, which can not be avoided.
2. The total number of DRAM accesses (hits + misses) also gets reduced by 110. This is 0.81% decrease in number of memory accesses.
3. As we get more number of cache hits and less number of memory accesses, the number of cycles required to complete the execution decreases. As a result, we get improved performance (higher IPC value). It can be seen that we can save 4214 cycles by changing the cache size from 128K to 2MB.
4. It can be observed that replacing 128K cache by 1MB cache results in 0.01% increased IPC. But the subsequent increases in cache size do not affect IPC greatly.

2.2 Non memory intensive trace

Cache Size : 128K	**Cache Size : 512K**
Total instruction: 7583269 Total cycles: 30309803 IPC: 0.250192 Total I-cache miss: 0 Total D-cache miss: 3275 Total D-cache hit: 3876329 Total data hazard: 490917 Total control hazard : 1705561 Total DRAM ROW BUFFER Hit: 917 Total DRAM ROW BUFFER Miss: 535 Total Store-load forwarding: 17	Total instruction: 7583269 Total cycles: 30307751 IPC: 0.250209 Total I-cache miss: 0 Total D-cache miss: 3225 Total D-cache hit: 3876379 Total data hazard: 488849 Total control hazard : 1705561 Total DRAM ROW BUFFER Hit: 905 Total DRAM ROW BUFFER Miss: 527 Total Store-load forwarding: 15
Cache Size : 1024K	**Cache Size 2048K**
Total instruction: 7583269 Total cycles: 30307751 IPC: 0.250209	Total instruction: 7583269 Total cycles: 30307751 IPC: 0.250209

Total I-cache miss: 0 Total D-cache miss: 3225 Total D-cache hit: 3876379 Total data hazard: 488849 Total control hazard : 1705561 Total DRAM ROW BUFFER Hit: 905 Total DRAM ROW BUFFER Miss: 527 Total Store-load forwarding: 15	Total I-cache miss: 0 Total D-cache miss: 3225 Total D-cache hit: 3876379 Total data hazard: 488849 Total control hazard : 1705561 Total DRAM ROW BUFFER Hit: 905 Total DRAM ROW BUFFER Miss: 527 Total Store-load forwarding: 15

It is evident that non-memory intensive programs gain very little by increases in cache size. The current execution shows that, this program was able to benefit from increase in cache size from 128K to 512K only. There is no improvement in IPC after cache size of 512K. The performance increase obtained is mere 0.006% as opposed to 0.01% in memory intensive trace.

3.0 Different Cache Associativity

Now we vary the cache associativity and observe the results.

3.1 Memory intensive trace

Associativity : 1 way Total instruction: 10057019 Total cycles: 35903716 IPC: 0.280111 Total I-cache miss: 0 Total D-cache miss: 130802 Total D-cache hit: 3511630 Total data hazard: 893592 Total control hazard : 2050615 Total DRAM ROW BUFFER Hit: 958 Total DRAM ROW BUFFER Miss: 127587 Total Store-load forwarding: 35	**Associativity : 2 way** Total instruction: 10057019 Total cycles: 35896780 IPC: 0.280165 Total I-cache miss: 0 Total D-cache miss: 134699 Total D-cache hit: 3507733 Total data hazard: 886418 Total control hazard : 2050615 Total DRAM ROW BUFFER Hit: 989 Total DRAM ROW BUFFER Miss: 131607 Total Store-load forwarding: 38
Associativity : 4 way Total instruction: 10057019 Total cycles: 35893678 IPC: 0.280189 Total I-cache miss: 0 Total D-cache miss: 15693 Total D-cache hit: 3626739 Total data hazard: 883472 Total control hazard : 2050615 Total DRAM ROW BUFFER Hit: 942 Total DRAM ROW BUFFER Miss: 12833 Total Store-load forwarding: 18	**Associativity : 8way** Total instruction: 10057019 Total cycles: 35893678 IPC: 0.280189 Total I-cache miss: 0 Total D-cache miss: 15715 Total D-cache hit: 3626717 Total data hazard: 883472 Total control hazard : 2050615 Total DRAM ROW BUFFER Hit: 942 Total DRAM ROW BUFFER Miss: 12855 Total Store-load forwarding: 18
Associativity : 16 way Total instruction: 10057019 Total cycles: 35893678	

IPC: 0.280189 Total I-cache miss: 0 Total D-cache miss: 15715 Total D-cache hit: 3626717 Total data hazard: 883472 Total control hazard : 2050615 Total DRAM ROW BUFFER Hit: 942 Total DRAM ROW BUFFER Miss: 12855 Total Store-load forwarding: 18	

Increasing cache associativity also increases the hit rate and decreases number of accesses to the memory. This phenomenon can be observed when we increase the associativity from direct mapped cache to 4-way set associative cache. Further increases in associativity do not contribute performance increase. This could be due to the fact that, the 4 way set associative cache is sufficient for this application and the address space it uses is small enough so that the application does not need more that 4 lines per set. The performance gained (increase in IPC) by changing the associativity from 1 to 4 results in 0.02% increase.

3.2 Non memory intensive trace

Associativity : 1 way Total instruction: 7583269 Total cycles: 30319369 IPC: 0.250113 Total I-cache miss: 0 Total D-cache miss: 3630 Total D-cache hit: 3875974 Total data hazard: 500418 Total control hazard : 1705561 Total DRAM ROW BUFFER Hit: 953 Total DRAM ROW BUFFER Miss: 643 Total Store-load forwarding: 20	**Associativity : 2 way** Total instruction: 7583269 Total cycles: 30308697 IPC: 0.250201 Total I-cache miss: 0 Total D-cache miss: 3252 Total D-cache hit: 3876352 Total data hazard: 489808 Total control hazard : 1705561 Total DRAM ROW BUFFER Hit: 913 Total DRAM ROW BUFFER Miss: 531 Total Store-load forwarding: 17
Associativity : 4 way Total instruction: 7583269 Total cycles: 30307751 IPC: 0.250209 Total I-cache miss: 0 Total D-cache miss: 3225 Total D-cache hit: 3876379 Total data hazard: 488849 Total control hazard : 1705561 Total DRAM ROW BUFFER Hit: 905 Total DRAM ROW BUFFER Miss: 527 Total Store-load forwarding: 15	**Associativity : 8way** Total instruction: 7583269 Total cycles: 30307751 IPC: 0.250209 Total I-cache miss: 0 Total D-cache miss: 3225 Total D-cache hit: 3876379 Total data hazard: 488849 Total control hazard : 1705561 Total DRAM ROW BUFFER Hit: 905 Total DRAM ROW BUFFER Miss: 527 Total Store-load forwarding: 15
Associativity : 16 way Total instruction: 7583269 Total cycles: 30307751	

IPC: 0.250209 Total I-cache miss: 0 Total D-cache miss: 3225 Total D-cache hit: 3876379 Total data hazard: 488849 Total control hazard : 1705561 Total DRAM ROW BUFFER Hit: 905 Total DRAM ROW BUFFER Miss: 527 Total Store-load forwarding: 15	

Non-memory intensive application also achieves performance gain of 0.03% changing the cache type from directly mapped to 4-way set associative.

Thus, from these observations, it seems that it is beneficial to use a 512KB, 4-way set associative cache in order to get maximum performance from the given memory intensive and non-intensive applications.

4.0 All Combinations of Available Configurations

Now, let us confirm this, by analyzing the IPC values, by varying both cache size and associativity and find a best possible match.

Memory Intensive	Non-memory-intensive
Cache Size : 128 Associativity : 1 IPC: 0.279992	Cache Size : 128 Associativity : 1 IPC: 0.250088
Cache Size : 128 Associativity : 2 IPC: 0.280082	Cache Size : 128 Associativity : 2 IPC: 0.25018
Cache Size : 128 Associativity : 4 IPC: 0.280181	Cache Size : 128 Associativity : 4 IPC: 0.250192
Cache Size : 128 Associativity : 8 IPC: 0.280189	Cache Size : 128 Associativity : 8 IPC: 0.250209
Cache Size : 128 Associativity : 16 IPC: 0.280189	Cache Size : 128 Associativity : 16 IPC: 0.250209
Cache Size : 512 Associativity : 1 IPC: 0.280111	**Cache Size : 512 Associativity : 1** **IPC: 0.250113 <BEST SUITED>**
Cache Size : 512 Associativity : 2 IPC: 0.280165	Cache Size : 512 Associativity : 2 IPC: 0.250201
Cache Size : 512 Associativity : 4 **IPC: 0.280189 <OPTIMAL>**	**Cache Size : 512 Associativity : 4** **IPC: 0.250209 <OPTIMAL>**

Cache Size : 512 Associativity : 8 IPC: 0.280189	Cache Size : 512 Associativity : 8 IPC: 0.250209
Cache Size : 512 Associativity : 16 IPC: 0.280189	Cache Size : 512 Associativity : 16 IPC: 0.250209
Cache Size : 1024 Associativity : 1 IPC: 0.280149	Cache Size : 1024 Associativity : 1 IPC: 0.250151
Cache Size : 1024 Associativity : 2 IPC: 0.280203	Cache Size : 1024 Associativity : 2 IPC: 0.250205
Cache Size : 1024 Associativity : 4 **IPC: 0.280214 <BEST SUITED>**	Cache Size : 1024 Associativity : 4 IPC: 0.250209
Cache Size : 1024 Associativity : 8 IPC: 0.280214	Cache Size : 1024 Associativity : 8 IPC: 0.250209
Cache Size : 1024 Associativity : 16 IPC: 0.280214	Cache Size : 1024 Associativity : 16 IPC: 0.250209
Cache Size : 2048 Associativity : 1 IPC: 0.280163	Cache Size : 2048 Associativity : 1 IPC: 0.250151
Cache Size : 2048 Associativity : 2 IPC: 0.280214	Cache Size : 2048 Associativity : 2 IPC: 0.250209
Cache Size : 2048 Associativity : 4 IPC: 0.280214	Cache Size : 2048 Associativity : 4 IPC: 0.250209
Cache Size : 2048 Associativity : 8 IPC: 0.280214	Cache Size : 2048 Associativity : 8 IPC: 0.250209
Cache Size : 2048 Associativity : 16 IPC: 0.280214	Cache Size : 2048 Associativity : 16 IPC: 0.250209

From these results, it can be said that 1MB 4-way associative cache is best suited for memory intensive application while 512K direct mapped cache is good for non-memory intensive trace.
But as we have to run these applications on same computer, we will require an optimal cache that will try to balance the applications and maximize the performance for both of them at the same time. Thus, a 512K 4-way set associative cache will be optimal for the chosen machine and it should be chosen as the working set. This confirms the initial observation.