CS 6290 High Performance Computer Architecture

Lab 3 Report

G-share Branch Predictor and TLB

Name : Raghavendra Vinayak Belapure
T-Square Account Name : rbelapure3

1.0 G-share Branch Predictor

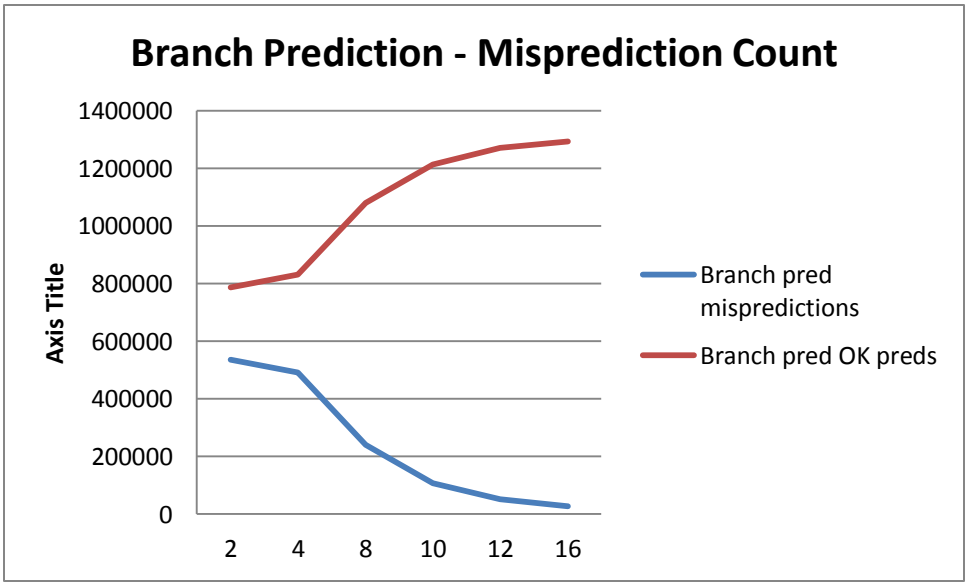
The aim is to vary the g-share history length from 2 to 16 and measure the branch predictor accuracy. The values used for the other parameters are as follows.

MSHR Size : 4	Cache Size : 512KB	Type : 4 way set associative
D-cache latency : 5 cycles	DRAM Row Buffer Hit latency : 100	DRAM Row Buffer Miss latency : 200
DRAM_BANK_NUM : 4	DRAM_PAGE_SIZE : 2KB	

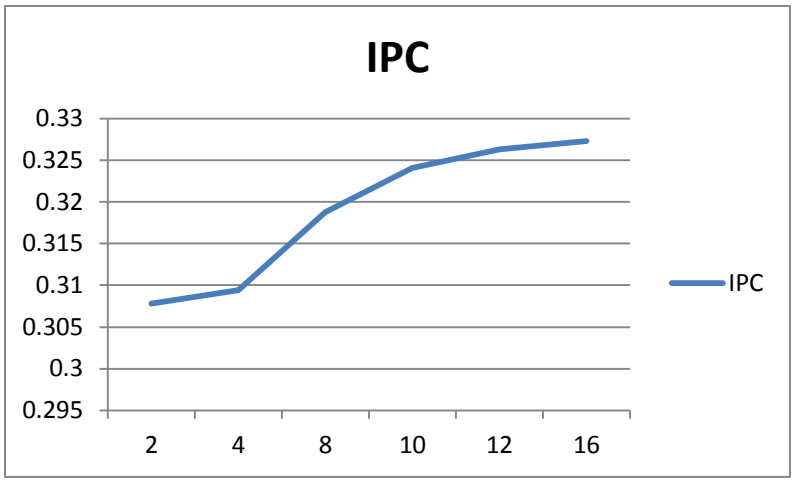
The results obtained for test1.pzip by varying the history length are as follows.

History Length	2	4	8	10	12	16
Total Cycles	25542174	25407684	24662558	24260594	24092611	24022630
IPC	0.307802	0.30943	0.31878	0.324061	0.326321	0.327271
Branch pred mispredictions	535550	490321	241040	107191	50706	27402
Branch pred OK preds	785261	830490	1079771	1213620	1270105	1293409

The graphs are plotted for Branch prediction-misprediction counts vs. History length and IPC vs. History length. These graphs are shown below.



The graph shows that the number of mis-predictions reduce drastically when the history length is increased. Changing the value of history length from 2 to 16 improves the branch prediction accuracy from 59.45% to 97.92%. This is due to the fact that as G-share is a history based predictor, the prediction accuracy increases when the amount of history



available is large. This increase in branch predictor accuracy results in less number of branches being mis-predicted, which in turn cause less pipeline flushes. As a result, the IPC improves. This is evident from the IPC vs. History length plot shown below. Improvement in IPC is 6.32%.

Similarly, we present the values for accurate predictions and IPC for remaining three cases as well.

Results for test2.pzip:

History Length	2	4	8	10	12	16
IPC	0.330064	0.331357	0.335605	0.336804	0.337231	0.337493
OK preds	547639	560839	604200	616056	620242	622815

IPC improvement: 2.25% Prediction accuracy (2): 83.37% Prediction accuracy (16):94.81%

Results for test3.pzip:

History Length	2	4	8	10	12	16
IPC	0.338252	0.33996	0.343901	0.344976	0.345476	0.345791
OK preds	770846	795329	851596	866553	873466	877805

IPC improvement: 2.22% Prediction accuracy (2): 83.38% Prediction accuracy (16):94.95%

Results for test4.pzip:

History Length	2	4	8	10	12	16
IPC	0.308213	0.309631	0.319312	0.324573	0.326697	0.327621
OK preds	1488178	1562577	2051733	2304332	2405170	2448170

IPC improvement: 6.29% Prediction accuracy (2): 59.74% Prediction accuracy (16):98.28%

In case 1 and 4, it can be seen that, as the size of history increases, considerable improvement in IPC can be seen because of the tremendous improvement in accuracy of branch prediction. In case of traces 2 and 3, it can be inferred that the branches in these cases can be predicted accurately even if very little history is available. Thus, these traces can possibly include loops with very large counter. As the increase in prediction accuracy is not that large as compared to trace 1 and 4, the improvement in IPC is also marginal.

2.0 Varying TLB Size (Page size = 4K)

We now vary the size of TLB and report TLB hit rate, IPC and number of memory accesses. Initially we start with a TLB with only one entry and then we gradually increase it till 16 entries. Number of memory accesses is equal to number of cache misses.

Results for test1.pzip

TLB Size	1	4	16
TLB Hit Rate	75.92%	94.32%	99.62%
IPC	0.30134	0.326321	0.334311
Memory accesses	7057	7192	7203

Results for test2.pzip

TLB Size	1	4	16
TLB Hit Rate	43.77%	85.55%	97.03%
IPC	0.29311	0.337231	0.3518
Memory accesses	52181	52441	52453

Results for test3.pzip

TLB Size	1	4	16
TLB Hit Rate	37.50%	86.59%	96.32%
IPC	0.293043	0.345476	0.3582
Memory accesses	52248	52510	52526

Results for test4.pzip

TLB Size	1	4	16
TLB Hit Rate	73.30%	93.10%	99.36%
IPC	0.300077	0.326697	0.33613
Memory accesses	7559	7705	7720

As we increase the number of entries in TLB, it is able to cache more translations. This is evident from the fact that TLB Hit rate increases as we increase the TLB size. This results in lesser requests being forwarded to cache and memory which helps in reducing the number of cycles. As a result, the IPC is improved. On the other hand, another interesting observation can be made. As we introduce TLB, the dcache is now shared by the PTE entries as well as the actual data entries. As a result, the space for each of them is insufficient in cache and as a result, it is causing thrashing in the cache. Thus, we get higher number of cache misses.

3.0 Changing the Page Table Size

We now run similar experiments as that of section 2.0 by changing the virtual page size from 4K to 8K. The results are shown below.

Results for test1.pzip:

TLB Size	Page Size = 4K	Page Size = 8K
1	Total instruction: 7861921 Total cycles: 26089901 IPC: 0.30134 Total I-cache miss: 0 Total D-cache miss: 7057 Total D-cache hit: 3365500 Total data hazard: 1578895 Total control hazard : 1320811 Total DRAM ROW BUFFER Hit: 2089 Total DRAM ROW BUFFER Miss: 940 Total Store-load forwarding: 24 Total Branch Predictor Mispredictions: 50706 Total Branch Predictor OK predictions: 1270105 Total DTLB Hit: 2063809 Total DTLB Miss: 654374	Total instruction: 7861921 Total cycles: 26086500 IPC: 0.301379 Total I-cache miss: 0 Total D-cache miss: 7050 Total D-cache hit: 3365048 Total data hazard: 1578701 Total control hazard : 1320811 Total DRAM ROW BUFFER Hit: 2088 Total DRAM ROW BUFFER Miss: 934 Total Store-load forwarding: 24 Total Branch Predictor Mispredictions: 50706 Total Branch Predictor OK predictions: 1270105 Total DTLB Hit: 2064266 Total DTLB Miss: 653916
4	Total instruction: 7861921 Total cycles: 24092611 IPC: 0.326321 Total I-cache miss: 0 Total D-cache miss: 7192 Total D-cache hit: 2865329 Total data hazard: 1536278 Total control hazard : 1320811 Total DRAM ROW BUFFER Hit: 2089 Total DRAM ROW BUFFER Miss: 940 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 50706 Total Branch Predictor OK predictions: 1270105 Total DTLB Hit: 2563845 Total DTLB Miss: 154338	Total instruction: 7861921 Total cycles: 24046019 IPC: 0.326953 Total I-cache miss: 0 Total D-cache miss: 7182 Total D-cache hit: 2854086 Total data hazard: 1525965 Total control hazard : 1320811 Total DRAM ROW BUFFER Hit: 2088 Total DRAM ROW BUFFER Miss: 934 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 50706 Total Branch Predictor OK predictions: 1270105 Total DTLB Hit: 2575096 Total DTLB Miss: 143086
16	Total instruction: 7861921 Total cycles: 23516824 IPC: 0.334311 Total I-cache miss: 0 Total D-cache miss: 7203 Total D-cache hit: 2721309 Total data hazard: 1499843 Total control hazard : 1320811 Total DRAM ROW BUFFER Hit: 2089 Total DRAM ROW BUFFER Miss: 940 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 50706 Total Branch Predictor OK predictions: 1270105 Total DTLB Hit: 2707854 Total DTLB Miss: 10329	Total instruction: 7861921 Total cycles: 23478579 IPC: 0.334855 Total I-cache miss: 0 Total D-cache miss: 7194 Total D-cache hit: 2712156 Total data hazard: 1496035 Total control hazard : 1320811 Total DRAM ROW BUFFER Hit: 2088 Total DRAM ROW BUFFER Miss: 934 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 50706 Total Branch Predictor OK predictions: 1270105 Total DTLB Hit: 2717014 Total DTLB Miss: 1168

Results for test2.pzip:

TLB Size	Page Size = 4K	Page Size = 8K
1	Total instruction: 3354758 Total cycles: 11445374 IPC: 0.29311 Total I-cache miss: 0 Total D-cache miss: 52181 Total D-cache hit: 1350296 Total data hazard: 637653 Total control hazard : 656859 Total DRAM ROW BUFFER Hit: 6105 Total DRAM ROW BUFFER Miss: 1097 Total Store-load forwarding: 21 Total Branch Predictor Mispredictions: 36617 Total Branch Predictor OK predictions: 620242 Total DTLB Hit: 393009 Total DTLB Miss: 504734	Total instruction: 3354758 Total cycles: 11320594 IPC: 0.296341 Total I-cache miss: 0 Total D-cache miss: 52167 Total D-cache hit: 1319670 Total data hazard: 637539 Total control hazard : 656859 Total DRAM ROW BUFFER Hit: 6107 Total DRAM ROW BUFFER Miss: 1085 Total Store-load forwarding: 20 Total Branch Predictor Mispredictions: 36617 Total Branch Predictor OK predictions: 620242 Total DTLB Hit: 423649 Total DTLB Miss: 474094
4	Total instruction: 3354758 Total cycles: 9535988 IPC: 0.3518 Total I-cache miss: 0 Total D-cache miss: 52453 Total D-cache hit: 871933 Total data hazard: 630563 Total control hazard : 656859 Total DRAM ROW BUFFER Hit: 6105 Total DRAM ROW BUFFER Miss: 1097 Total Store-load forwarding: 29 Total Branch Predictor Mispredictions: 36617 Total Branch Predictor OK predictions: 620242 Total DTLB Hit: 871100 Total DTLB Miss: 26643	Total instruction: 3354758 Total cycles: 9833228 IPC: 0.341165 Total I-cache miss: 0 Total D-cache miss: 52427 Total D-cache hit: 946862 Total data hazard: 632539 Total control hazard : 656859 Total DRAM ROW BUFFER Hit: 6107 Total DRAM ROW BUFFER Miss: 1085 Total Store-load forwarding: 27 Total Branch Predictor Mispredictions: 36617 Total Branch Predictor OK predictions: 620242 Total DTLB Hit: 796197 Total DTLB Miss: 101546
16	Total instruction: 3354758 Total cycles: 9947954 IPC: 0.337231 Total I-cache miss: 0 Total D-cache miss: 52441 Total D-cache hit: 974984 Total data hazard: 632660 Total control hazard : 656859 Total DRAM ROW BUFFER Hit: 6105 Total DRAM ROW BUFFER Miss: 1097 Total Store-load forwarding: 25 Total Branch Predictor Mispredictions: 36617 Total Branch Predictor OK predictions: 620242 Total DTLB Hit: 768061 Total DTLB Miss: 129682	Total instruction: 3354758 Total cycles: 9451692 IPC: 0.354937 Total I-cache miss: 0 Total D-cache miss: 52436 Total D-cache hit: 851434 Total data hazard: 630319 Total control hazard : 656859 Total DRAM ROW BUFFER Hit: 6107 Total DRAM ROW BUFFER Miss: 1085 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 36617 Total Branch Predictor OK predictions: 620242 Total DTLB Hit: 891616 Total DTLB Miss: 6127

Results for test3.pzip:

TLB Size	Page Size = 4K	Page Size = 8K
1	Total instruction: 4951261 Total cycles: 16896027 IPC: 0.293043 Total I-cache miss: 0 Total D-cache miss: 52248 Total D-cache hit: 2072718	Total instruction: 4951261 Total cycles: 16712625 IPC: 0.296259 Total I-cache miss: 0 Total D-cache miss: 52140 Total D-cache hit: 2027491

	Total data hazard: 675273 Total control hazard : 924487 Total DRAM ROW BUFFER Hit: 6117 Total DRAM ROW BUFFER Miss: 1088 Total Store-load forwarding: 20 Total Branch Predictor Mispredictions: 51021 Total Branch Predictor OK predictions: 873466 Total DTLB Hit: 490504 Total DTLB Miss: 817187	Total data hazard: 675049 Total control hazard : 924487 Total DRAM ROW BUFFER Hit: 6116 Total DRAM ROW BUFFER Miss: 1076 Total Store-load forwarding: 20 Total Branch Predictor Mispredictions: 51021 Total Branch Predictor OK predictions: 873466 Total DTLB Hit: 535749 Total DTLB Miss: 771941
4	Total instruction: 4951261 Total cycles: 14331694 IPC: 0.345476 Total I-cache miss: 0 Total D-cache miss: 52510 Total D-cache hit: 1430613 Total data hazard: 670475 Total control hazard : 924487 Total DRAM ROW BUFFER Hit: 6117 Total DRAM ROW BUFFER Miss: 1088 Total Store-load forwarding: 24 Total Branch Predictor Mispredictions: 51021 Total Branch Predictor OK predictions: 873466 Total DTLB Hit: 1132355 Total DTLB Miss: 175336	Total instruction: 4951261 Total cycles: 14195327 IPC: 0.348795 Total I-cache miss: 0 Total D-cache miss: 52395 Total D-cache hit: 1397140 Total data hazard: 670414 Total control hazard : 924487 Total DRAM ROW BUFFER Hit: 6116 Total DRAM ROW BUFFER Miss: 1076 Total Store-load forwarding: 27 Total Branch Predictor Mispredictions: 51021 Total Branch Predictor OK predictions: 873466 Total DTLB Hit: 1165845 Total DTLB Miss: 141845
16	Total instruction: 4951261 Total cycles: 13822600 IPC: 0.3582 Total I-cache miss: 0 Total D-cache miss: 52526 Total D-cache hit: 1303276 Total data hazard: 668418 Total control hazard : 924487 Total DRAM ROW BUFFER Hit: 6117 Total DRAM ROW BUFFER Miss: 1088 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 51021 Total Branch Predictor OK predictions: 873466 Total DTLB Hit: 1259680 Total DTLB Miss: 48011	Total instruction: 4951261 Total cycles: 13712612 IPC: 0.361074 Total I-cache miss: 0 Total D-cache miss: 52402 Total D-cache hit: 1276415 Total data hazard: 668266 Total control hazard : 924487 Total DRAM ROW BUFFER Hit: 6116 Total DRAM ROW BUFFER Miss: 1076 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 51021 Total Branch Predictor OK predictions: 873466 Total DTLB Hit: 1286563 Total DTLB Miss: 21127

Results for test4.pzip:

TLB Size	Page Size = 4K	Page Size = 8K
1	Total instruction: 14949126 Total cycles: 49817632 IPC: 0.300077 Total I-cache miss: 0 Total D-cache miss: 7559 Total D-cache hit: 6491804 Total data hazard: 2812665 Total control hazard : 2490792 Total DRAM ROW BUFFER Hit: 2132 Total DRAM ROW BUFFER Miss: 1152 Total Store-load forwarding: 24 Total Branch Predictor Mispredictions: 85622 Total Branch Predictor OK predictions: 2405170 Total DTLB Hit: 3760473	Total instruction: 14949126 Total cycles: 49461173 IPC: 0.30224 Total I-cache miss: 0 Total D-cache miss: 7518 Total D-cache hit: 6403069 Total data hazard: 2783058 Total control hazard : 2490792 Total DRAM ROW BUFFER Hit: 2128 Total DRAM ROW BUFFER Miss: 1147 Total Store-load forwarding: 24 Total Branch Predictor Mispredictions: 85622 Total Branch Predictor OK predictions: 2405170 Total DTLB Hit: 3849217

	Total DTLB Miss: 1369430	Total DTLB Miss: 1280685
4	Total instruction: 14949126 Total cycles: 45758387 IPC: 0.326697 Total I-cache miss: 0 Total D-cache miss: 7705 Total D-cache hit: 5476147 Total data hazard: 2715099 Total control hazard : 2490792 Total DRAM ROW BUFFER Hit: 2132 Total DRAM ROW BUFFER Miss: 1152 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 85622 Total Branch Predictor OK predictions: 2405170 Total DTLB Hit: 4775988 Total DTLB Miss: 353915	Total instruction: 14949126 Total cycles: 45543172 IPC: 0.328241 Total I-cache miss: 0 Total D-cache miss: 7663 Total D-cache hit: 5422788 Total data hazard: 2710533 Total control hazard : 2490792 Total DRAM ROW BUFFER Hit: 2128 Total DRAM ROW BUFFER Miss: 1147 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 85622 Total Branch Predictor OK predictions: 2405170 Total DTLB Hit: 4829353 Total DTLB Miss: 300549
16	Total instruction: 14949126 Total cycles: 44474230 IPC: 0.33613 Total I-cache miss: 0 Total D-cache miss: 7720 Total D-cache hit: 5155038 Total data hazard: 2646942 Total control hazard : 2490792 Total DRAM ROW BUFFER Hit: 2132 Total DRAM ROW BUFFER Miss: 1152 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 85622 Total Branch Predictor OK predictions: 2405170 Total DTLB Hit: 5097086 Total DTLB Miss: 32817	Total instruction: 14949126 Total cycles: 44355039 IPC: 0.337033 Total I-cache miss: 0 Total D-cache miss: 7678 Total D-cache hit: 5125688 Total data hazard: 2632385 Total control hazard : 2490792 Total DRAM ROW BUFFER Hit: 2128 Total DRAM ROW BUFFER Miss: 1147 Total Store-load forwarding: 28 Total Branch Predictor Mispredictions: 85622 Total Branch Predictor OK predictions: 2405170 Total DTLB Hit: 5126438 Total DTLB Miss: 3464

Thus, following observations can be made from these results.

1. As TLB is a cache for VPN to PFN translations, increasing the TLB size will result in more number of entries getting stored in the TLB. This results in improvement on TLB hit rate. As a result, the number of memory accesses that are required, get reduced. We can observe that the TLB hit rate can go up to 99% when TLB size is increased.
2. Increasing the page size will cause the number of bits allocated for VPN to shrink. This causes the number of TLB hits to increase as more TLB entries can be stored.