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Core Facts

Provided with Core	
Documentation	Data Sheet
Design File Formats	Encrypted VHDL
Constraints Files	Reference design ucf
Verification	
Reference Designs & Application Notes	Reference Design for the ZedBoard™ from Avnet Electronics Marketing
Additional Items	SW support integrated with Linux and Microsoft® Windows® Embedded Compact drivers for graphics logicBRICKS IP cores
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 All Programmable SoC, 7 series and Spartan®-6 FPGAs
- Provides twelve independent clock outputs that can be configured by generic parameters:
  - Six outputs can be dynamically configured through register interface during operation
  - Six outputs can be configured by generic parameters only
- Input clock frequency range*:
  - Spartan-6: 19 – 540 MHz
  - 7 series: 19 – 1066
- Output clocks frequency range*:
  - Spartan-6: 3.125 – 400 MHz
  - 7 series: 6.25 – 741 MHz
- Configurable ARM® AMBA® AXI4-Lite and CoreConnect™ PLBv46 compliant registers interface
- Software support for Linux and Microsoft® Windows® Embedded Compact operating systems
- Available for Xilinx Vivado® IP Integrator and ISE® Platform Studio

** Depending on the used device's speed grade*

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	LCs	Slices[1] (FFs/ LUTs)	IOB[2]	CMT (PLLs (MMCMs)/ DCMs)	BRAM	MULT/ DSP48/E	GTx	Design Tools
Zynq™-7000[3] (XC7Z020-3)	1990	311 (814/543)	2	(2/0)	0	0	N/A	ISE® 14.7
Spartan®-6 (XC6SLX150T-3)	1818	284 (734/496)	2	(2/0)	0	0	N/A	ISE® 14.7

Notes:
1) Assuming the following configuration: AXI4-Lite registers interface, Dynamic Reconfiguration Parameters Module (DRP) generated.
2) Assuming register interface, as well as status signals and generated clock outputs are connected internally.
3) The same implementation statistics apply to the Xilinx 7 series All Programmable FPGAs.

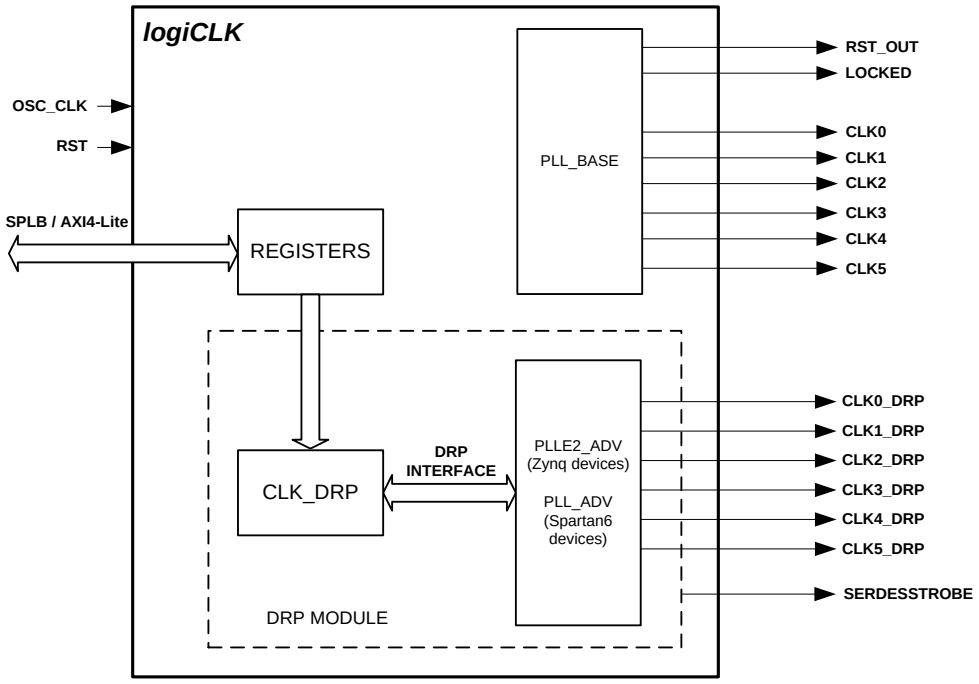

Figure 1: logiCLK Architecture

General Description

The logiCLK Programmable Clock Generator IP core from the Xylon logicBRICKS IP core library is optimized for Xilinx Zynq-7000 AP SoC and Spartan-6 and 7 series All Programmable FPGAs, and designed to provide frequency synthesis, clock network deskew and jitter reduction. Input and output frequency ranges are restricted by PLL, MMCM and Clock Buffer switching characteristics of the specific Xilinx All Programmable device.

The logiCLK clock generator IP core has twelve independent and fully configurable clock outputs. While six clock outputs can be fixed by generic parameters prior to the implementation, the other six clock outputs can be either fixed by generics or dynamically reconfigured in a working device. The Dynamic Reconfiguration Port (DRP) interface gives system designers the ability to change the clock frequency and other clock parameters while the design is running by mean of a set of memory-mapped PLL configuration and status registers (Fg. 1).

The ability to dynamically change the clock signals during the operation is an important feature for some SoC applications. For example, the logiCLK IP core enables precise clock adjustments necessary for driving display output with different resolutions, which would be otherwise impossible without an external programmable Phase-Locked Loop (PLL) device.

Xylon uses the logiCLK IP core in free and pre-verified Graphics Processing Unit (GPU) reference designs prepared for popular Xilinx Zynq-7000 AP SoC based development kits. Please visit Xylon web site to see the full list of logicBRICKS reference designs:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

Xylon's software drivers for graphics logicBRICKS IP cores, such as the logiCVC-ML display controller IP core, include support for the logiCLK Programmable Clock Generator IP core and enable its easy use with the Linux and Microsoft Windows Embedded Compact operating systems.

Functional Description

The Figure 1 presents internal logiCLK architecture. The logiCLK functional blocks are Dynamic Reconfiguration Parameters module and Registers.

Dynamic Reconfiguration Parameters module

Dynamic Reconfiguration Parameters module is an optional IP core's module that provides six output clocks (CLK_DRP) defined by a set of re-configurable parameters. It is designed in accordance to the Xilinx Application Note XAPP888: "MMCM and PLL Dynamic Reconfiguration" for 7 series FPGAs and to Xilinx Application Note XAPP879: "PLL Dynamic Reconfiguration" for Spartan-6 FPGAs.

Registers

The CPU has access to logiCLK's registers through the PLBv4.6 or AXI4-Lite bus.

Core Modifications

The core is supplied in encrypted VHDL format compatible with Xilinx Vivado IP Integrator and ISE Platform Studio implementation tools. Many logiCLK configuration parameters are selectable prior to VHDL synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logiCLK VHDL configuration parameters

Parameter	Description
C_REGS_INTERFACE	Defines registers interface: PLBv46 or AXI4-Lite
C_OSC_CLK_FREQ_HZ	Oscillator frequency
C_RST_POLARITY	Reverts the polarity of input RST signal
C_CLK_MULTIPLY[1)]	Specifies the multiplication value for all CLK clock outputs
C_CLK0_DIVIDE - C_CLK5_DIVIDE[1)]	Specifies the divide value for clock outputs 0 to 5
C_USE_CLK_DRP[1)]	When set enables the DRP module
C_USE_VLINK_CLK	When set clk0_drp is output from BUFIO for 7 series FPGAs or BUFPLL for Spartan 6 FPGAs
C_DRP_CLKFBOUT_PHASE[1, 2)]	Specifies the phase offset in degrees of the clock feedback output
C_DRP_BANDWIDTH[1, 2)]	Specifies the PLL programming algorithm affecting the jitter, phase margin and other characteristics of the PLL
C_DRP_CLKFBOUT_MULT[1, 2)]	Specifies the multiplication value for all CLK_DRP clock outputs
C_DRP_DIVCLK_DIVIDE[1, 2)]	Specifies the divide ratio for all clock outputs with respect to the input clock
C_DRP_CLKOUT0_DIVIDE- C_DRP_CLKOUT5_DIVIDE[1, 2)]	Specifies the amount to divide the associated CLK_DRP clock output if a different frequency is desired
C_DRP_CLKOUT0_PHASE- C_DRP_CLKOUT5_PHASE[1, 2)]	Specifies the phase offset in degrees of the clock feedback output
C_DRP_CLKOUT0_DUTY- C_DRP_CLKOUT5_DUTY[1, 2)]	Specifies the Duty Cycle for CLK_DRP clock outputs in percentage

Notes:

1. Refer to Xilinx 7 series or Spartan-6 FPGA Libraries Guide for HDL Designs.
2. These parameters are used to configure CLK_DRP outputs if dynamic reconfiguration enable bit in control register is cleared, or if dynamic reconfiguration enable bit in control register set and data address is "0".

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
OSC_CLK	Input	Oscillator clock input
RST	Input	Global synchronous set/reset input
RST_OUT	Output	Synchronous set/reset output
LOCKED	Output	An output from the PLL that indicates when the PLL has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range
SERDESSTROBE	Output	BUFPLL output
Register Interface		
PLBv46 Slave Interface	Bus	Refer to Xilinx-IBM Core connect specification
AXI4-Lite Interface	Bus	Refer to AMBA AXI version 4 specification from ARM
Clock Output Signals		
CLK0_DRP - CLK5_DRP	Output	User configurable (DRP) clock outputs (if C_USE_CLK_DRP = 1)
CLK0-5	Output	User configurable clock outputs

Verification Methods

The logiCLK is fully supported by the Xilinx Vivado and ISE Design Suites. This tight integration tremendously shortens IP integration and verification. A full logiCLK implementation does not require any particular skills beyond general Xilinx tools knowledge. This IP core has been successfully validated in different designs.

Software drivers

Xylon Linux Framebuffer driver includes the software support for the logiCLK IP core. For more information, please get the Linux Framebuffer User's Manual:

URL: http://www.logicbricks.com/Documentation/Datasheets/SW/Xylon-Linux-FrameBuffer.pdf

Xylon logiDISP driver for Microsoft Windows Embedded Compact includes the software support for the logiCLK IP core. For more information, please visit:

URL: http://www.logicbricks.com/Products/Xylon-Windows-Embedded-Display.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

logiREF-ZGPU-ZED Reference Design – evaluate 2D and 3D logicBRICKS graphics on the ZedBoard from Avnet Electronics Marketing with connected PC monitor. Deliverables include complete software support for Linux OS, from the basic FrameBuffer up to the full 3D graphics. Configurable IP cores enable customization of the evaluation hardware, which can be also used with other popular operating systems. This design uses the logiCLK Programmable Clock Generator IP core to support different display resolutions.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Zynq-AP-SoC-ZedBoard.aspx

To check a full list of Xylon reference designs please visit the web:

URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.00.	06.09.2012.	Initial Xylon release.
1.01.	28.03.2013.	Support for Spartan 6 FPGA families.
1.02.	20.09.2013.	Document version changed according to HW.
1.2.	08.12.2014.	New versioning scheme introduced for Vivado packaged IP core.