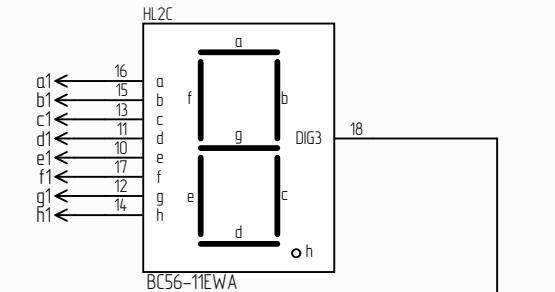
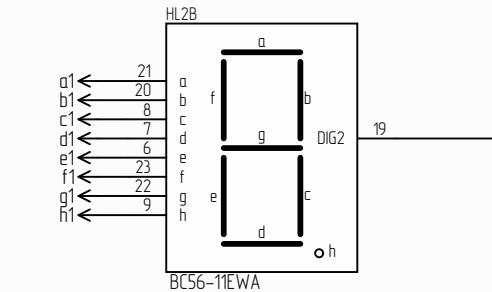
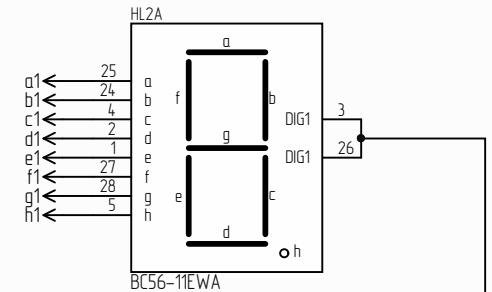
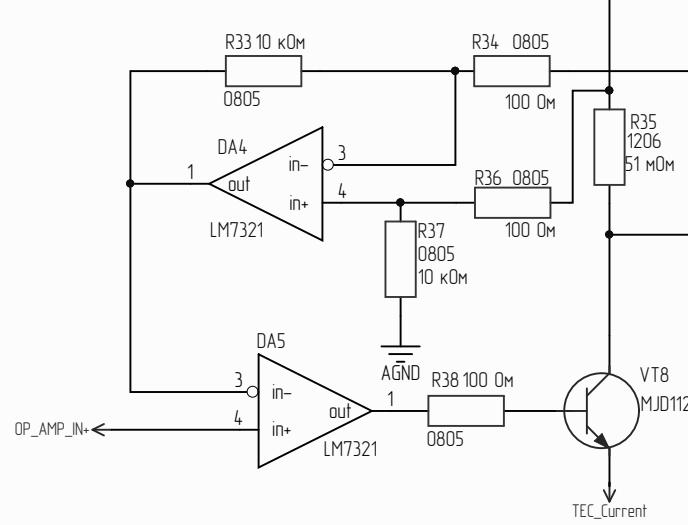
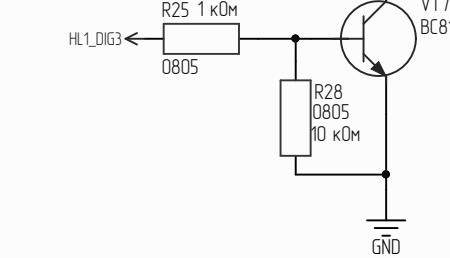
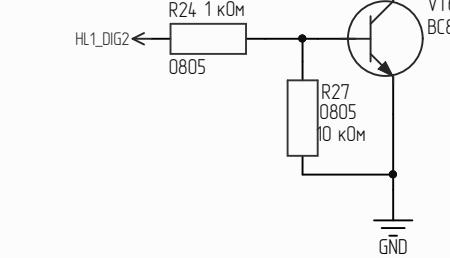
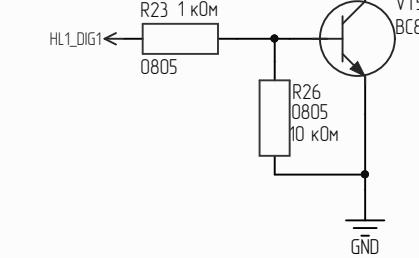
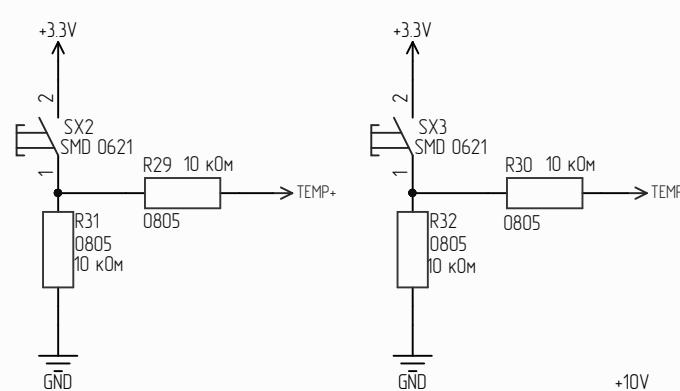
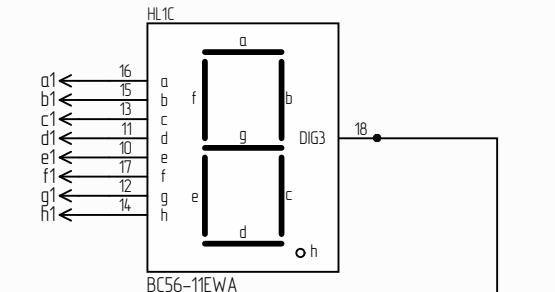
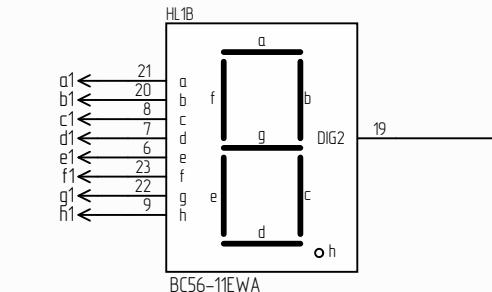
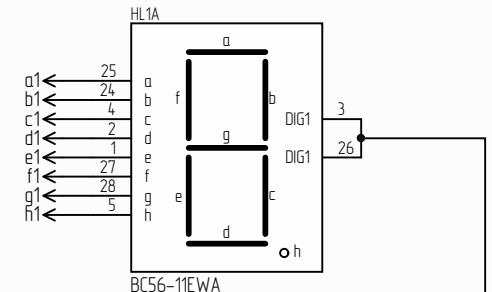
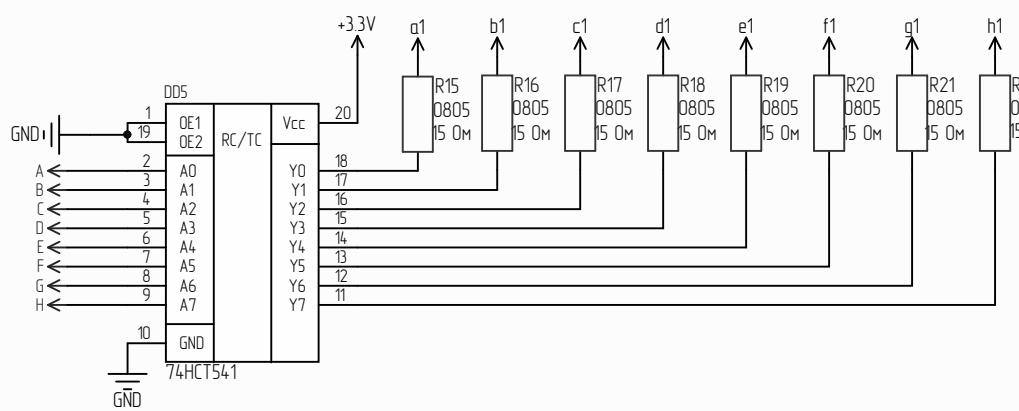


ЛЭТИ.120337.001 ЗЗ

					ЛЭТИ.120337.001 Э3			
Изм.	Лист	№ докум.	Подп.	Дата	Схема управления модулем Пельтье	Лит.	Масса	Масштаб
Разраб.	Ли							1:1
Проф.	Герасимов							
Т.контр.						Лист 1	Листов 1	
Н.контр.	Кострин							
Утв.	Герасимов							
						СПБГЭТУ «ЛЭТИ»		

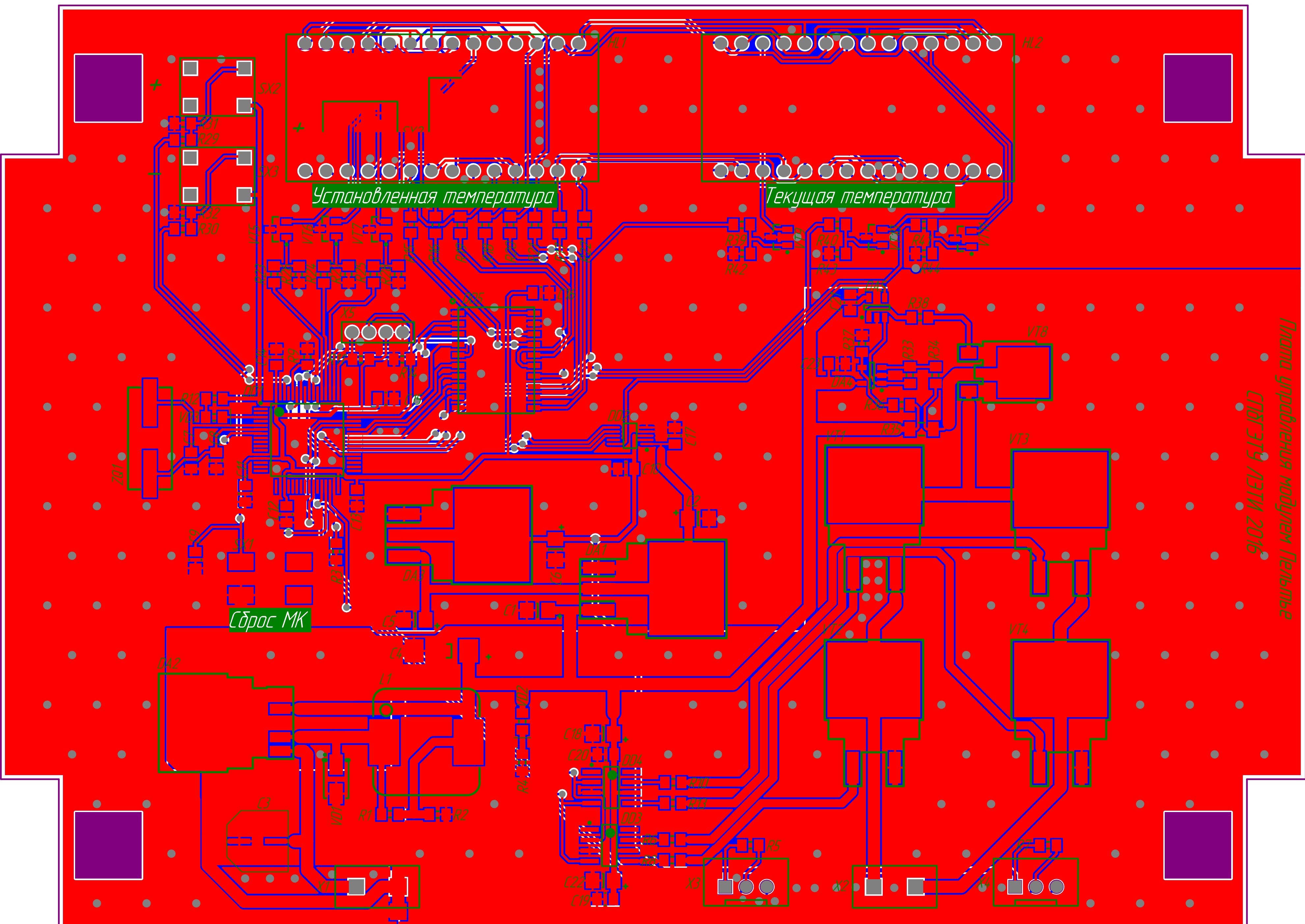
ATN.120337.001 33

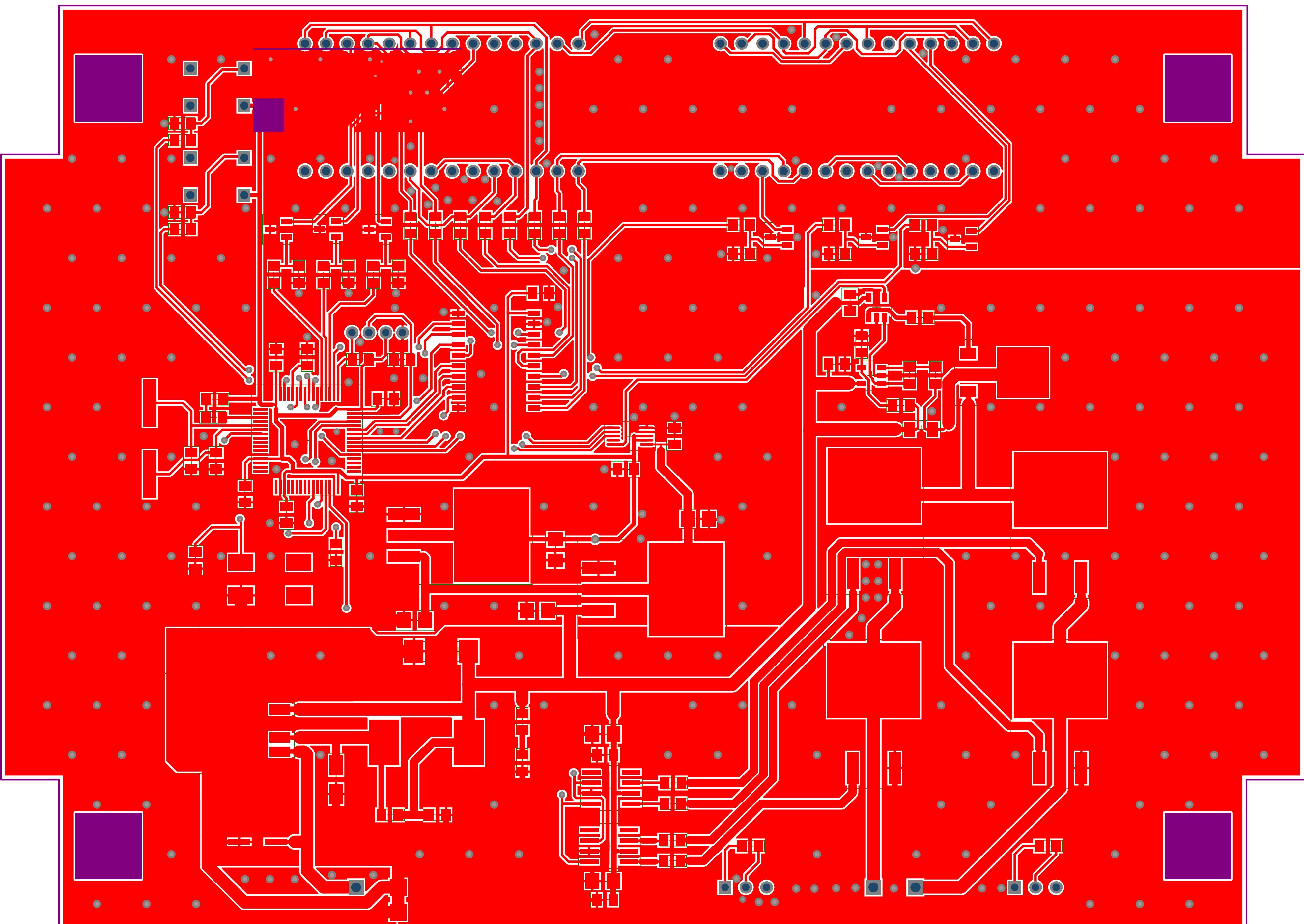


Инф. № по делу.	Подп. и дата	Взам. инф. №	Инф. № изыск.	Подп. и дата

Designator	Comment	value	Quantity
C1, C2, C6	танталовый конденсатор	10 мкФ 10В	3
C3	алюм. конденсатор	100 мкФ 35 В	1
C4	алюм. конденсатор	220 мкФ 10 В	1
C5	танталовый конденсатор	10 мкФ 10В	1
C7, C8	керамический 0805	20 пФ	2
C9, C10, C11, C12, C13, C14, C15, C16, C17, C19, C20, C21, C23	керамический 0805	0.1 мкФ	13
C18, C22	танталовый SMD A	0.47 мкФ 25В	2
DA1	микросхема	LM1086-5.0	1
DA2	микросхема	LM2596-ADJ	1
DA3	микросхема	LM1086-3.3	1
DA4, DA5	операционный усилитель	LM7321	2
DD1	микросхема	STM32F103RET6	1
DD2	микросхема	AD5693R	1
DD3	микросхема	MAX4426	1
DD4	микросхема	MAX4427	1
DD5	микросхема	74HCT541	1
HL1, HL2	7-сегментный индикатор	BC56-11EWA	2
L1	дроессель	47 мГн	1
R1	0805	7.5 кОм	1
R2, R23, R24, R25, R39, R40, R41	0805	1 кОм	7
R3, R9, R11, R14, R26, R27, R28, R29, R30, R31, R32, R33, R37, R42, R43, R44	0805	10 кОм	16
R4	0805	620 Ом	1
R5, R7	0805	4.7 кОм	2
R6, R8, R10, R13	0805	10 Ом	4
R12	0805	300 Ом	1
R15, R16, R17, R18, R19, R20, R21, R22	0805	15 Ом	8
R34, R36, R38	0805	100 Ом	3
R35	1206	51 мОм	1
SX1	кнопка тактовая	TC-0102	1
SX2, SX3	кнопка тактовая	SMD 0621	2
VD1	диод Шоттки	STPS1L30A	1
VD2, VD3	светодиод 0805	BL-LS0805PGC	2
VT1, VT2, VT3, VT4	N-канальный МОП транзистор	IRF540S	4
VT5, VT6, VT7, VT9, VT10, VT11	биполярный транзистор	BC817	6
VT8	биполярный транзистор	MJD112	1
X1, X2	клеммник	EK508V-02P	2
X3, X4	вилка на плату	PW10-3M	2
X5	вилка на плату	PLS-4 2.54	1
ZQ1	кварцевый резонатор	8 МГц	1

Плата управления модулем пельмель
СБРГЭТУ /ЛЭМ/ 2016





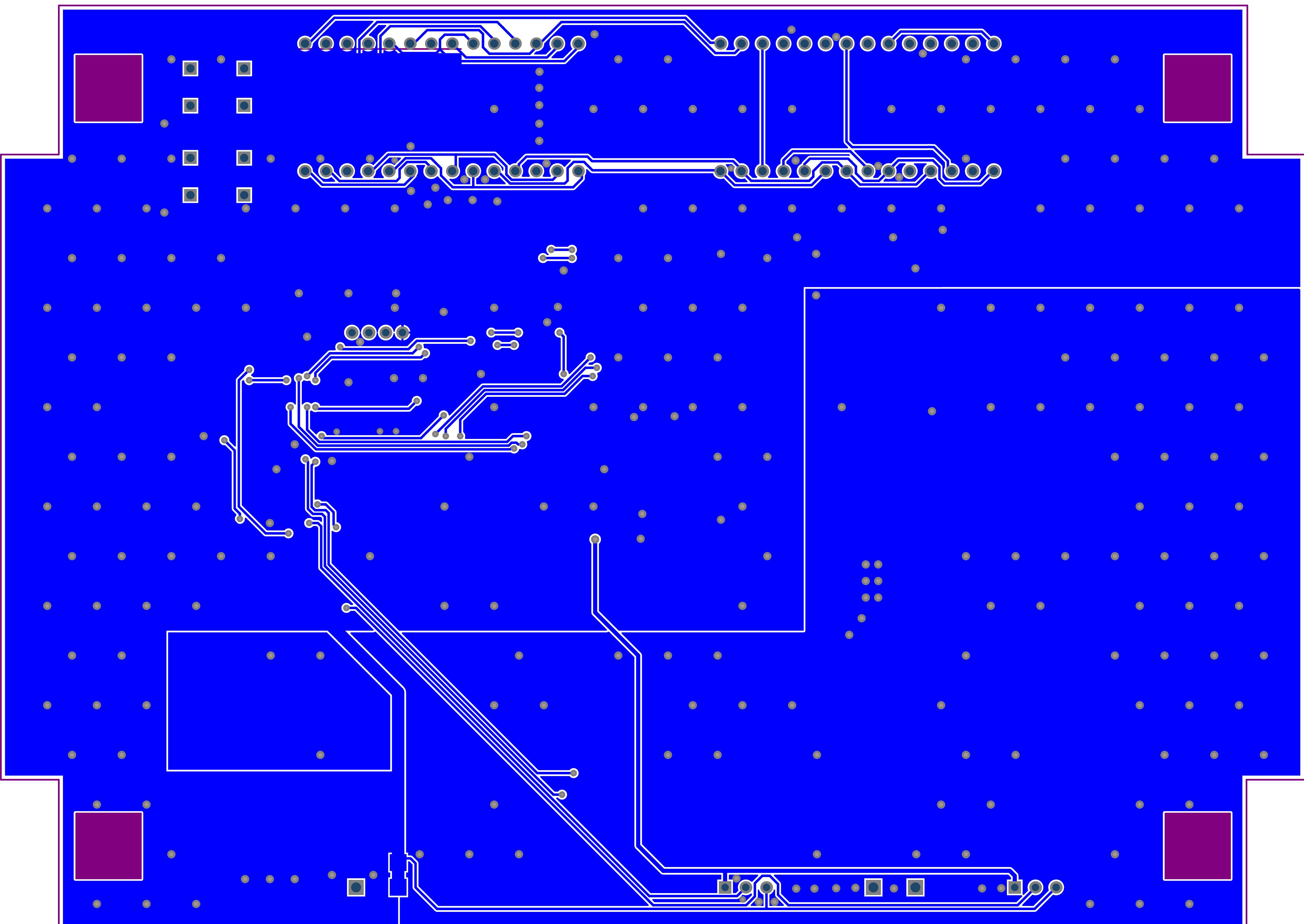
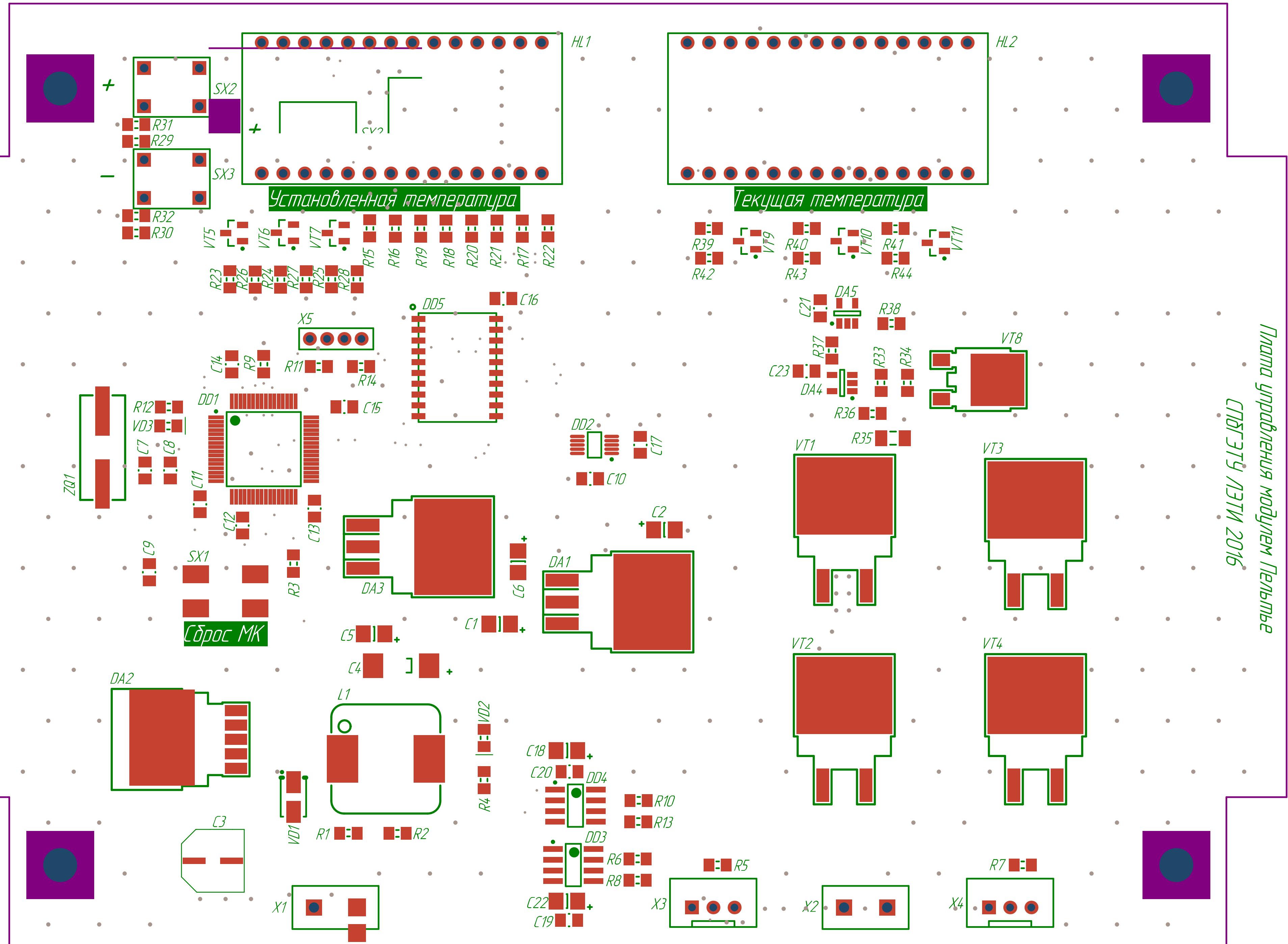
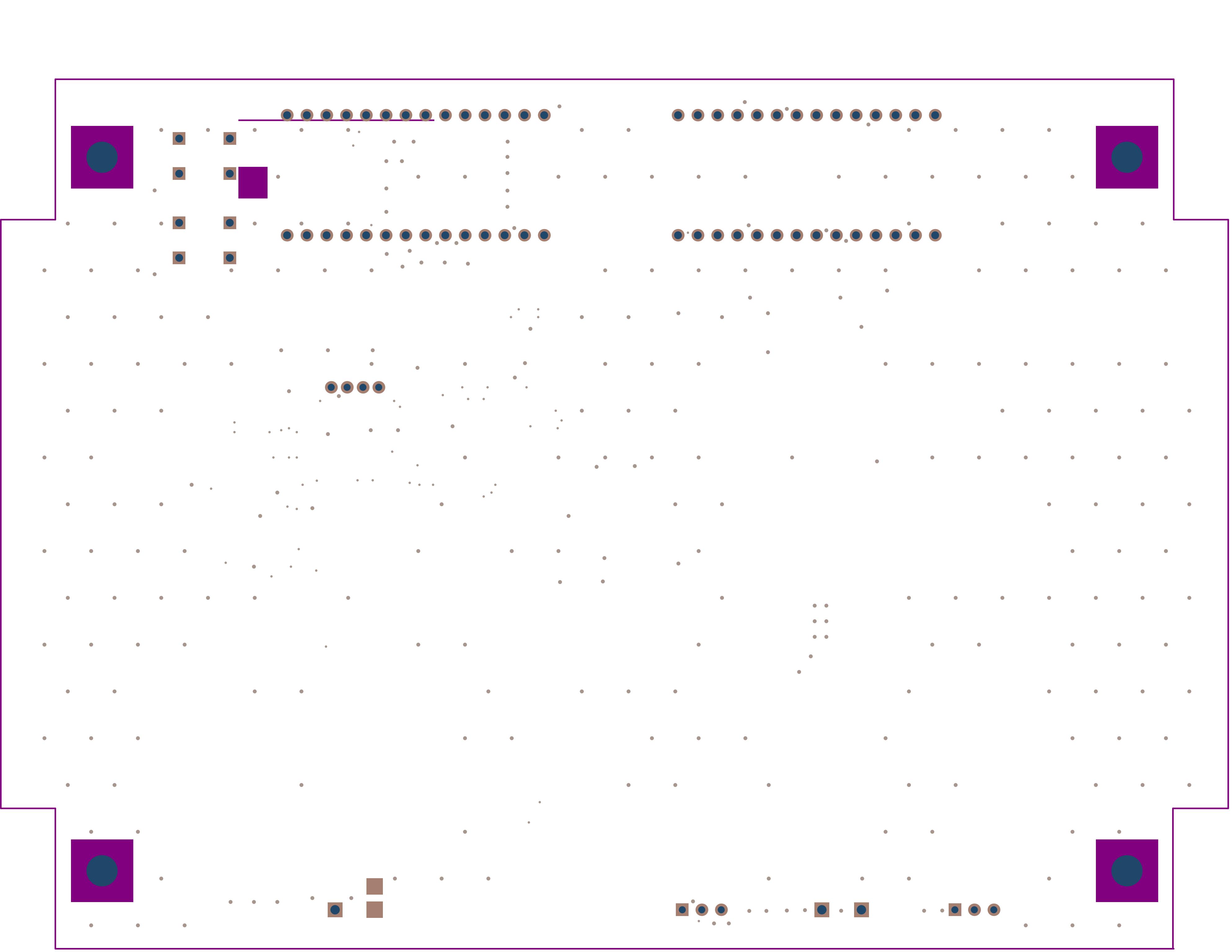


Схема модуля температуры

Чтобы открыть щиток в паяльной маске





Design Rules Verification Report

Filename : C:\Users\estam\Google Диск\MDP\MDP_Peltier.PcbDoc

Warnings 0
Rule Violations 6

Warnings	
Total	0

Rule Violations	
Routing Via (MinHoleWidth=0.5mm) (MaxHoleWidth=99mm) (PreferredHoleWidth=0.5mm) (MinWidth=1mm)	6
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mm) (All)	0
Silk to Silk (Clearance=0.254mm) (Disabled)(All),(All)	0
Silk To Solder Mask (Clearance=0.05mm) (IsPad),(IsText)	0
Minimum Solder Mask Sliver (Gap=0.05mm) (All),(All)	0
Hole To Hole Clearance (Gap=0.15mm) (All),(All)	0
Height Constraint (Min=0mm) (Max =25.4mm) (Prefered=12.7mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max =99mm) (All)	0
Minimum Annular Ring (Minimum=0.2mm) (IsPad)	0
Minimum Annular Ring (Minimum=0.15mm) (IsVia)	0
Un-Routed Net Constraint (All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Routing Via (MinHoleWidth=0.3mm) (Max HoleWidth=0.3mm) (PreferredHoleWidth=0.3mm) (MinWidth=0.8mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Width Constraint (Min=0.15mm) (Max =3mm) (Preferred=0.254mm) (All)	0
Width Constraint (Min=1mm) (Max =3mm) (Preferred=1.5mm) (Disabled)(InNetClass('PWR'))	0
Clearance Constraint (Gap=0.15mm) (All),(All)	0
Clearance Constraint (Gap=0.2mm) (InPolygon),(All)	0
Clearance Constraint (Gap=3mm) (Disabled)(IsPad and not PadIsPlated),(All)	0
Clearance Constraint (Gap=0.508mm) (IsStitchingVia and InNet('GND')),((IsVia and (Not IsStitchingVia)) Or IsPad)	0
Silk primitive without silk layer	0
Total	6

Routing Via (MinHoleWidth=0.5mm) (MaxHoleWidth=99mm) (PreferredHoleWidth=0.5mm) (MinWidth=1mm) (MaxWidth=
Routing Via Style: Via (76.625mm,-97.95mm) from Top Layer to Bottom Layer Actual Size : 0.8mm Actual Hole Size : 0.3mmr
Routing Via Style: Via (34.75mm,-41.425mm) from Top Layer to Bottom Layer Actual Size : 0.8mm Actual Hole Size : 0.3mm
Routing Via Style: Via (32.8mm,-41.425mm) from Top Layer to Bottom Layer Actual Size : 0.8mm Actual Hole Size : 0.3mm
Routing Via Style: Via (27.575mm,-41.475mm) from Top Layer to Bottom Layer Actual Size : 0.8mm Actual Hole Size : 0.3mm
Routing Via Style: Via (34.575mm,-8.7mm) from Top Layer to Bottom Layer Actual Size : 0.8mm Actual Hole Size : 0.3mm
Routing Via Style: Via (75.225mm,-9.675mm) from Top Layer to Bottom Layer Actual Size : 0.8mm Actual Hole Size : 0.3mmr

