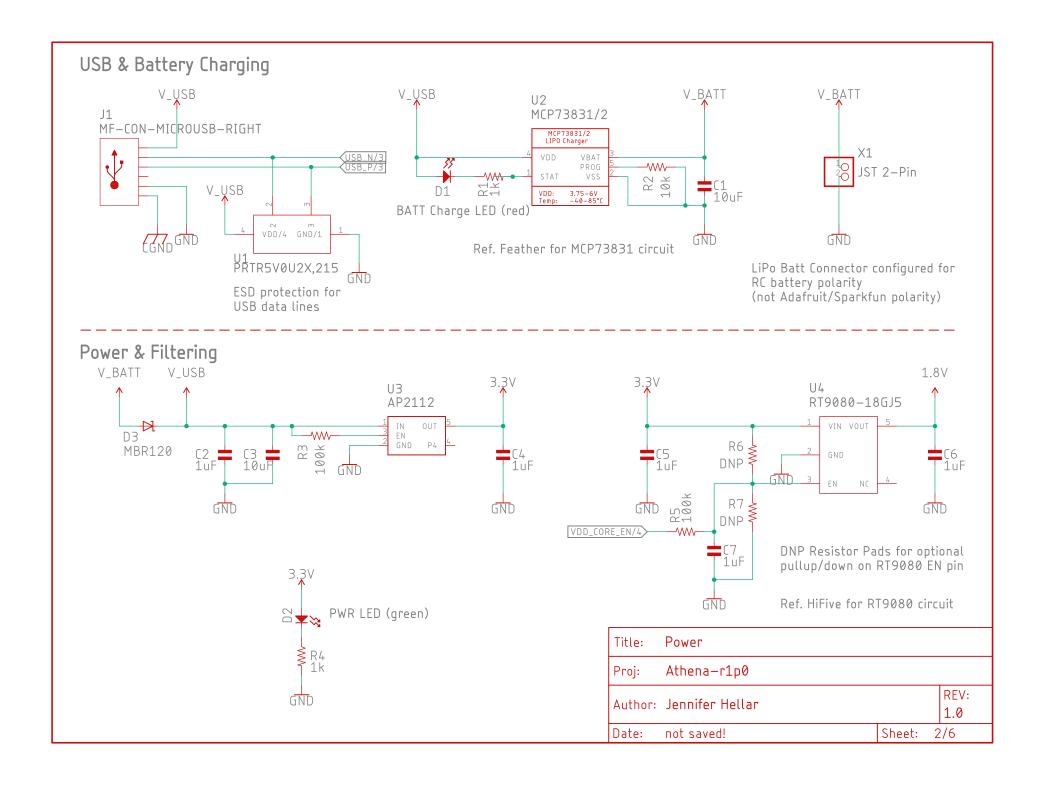
# Athena Design Rev. 1.0 Schematic RVR Lab, Rice University, Houston TX

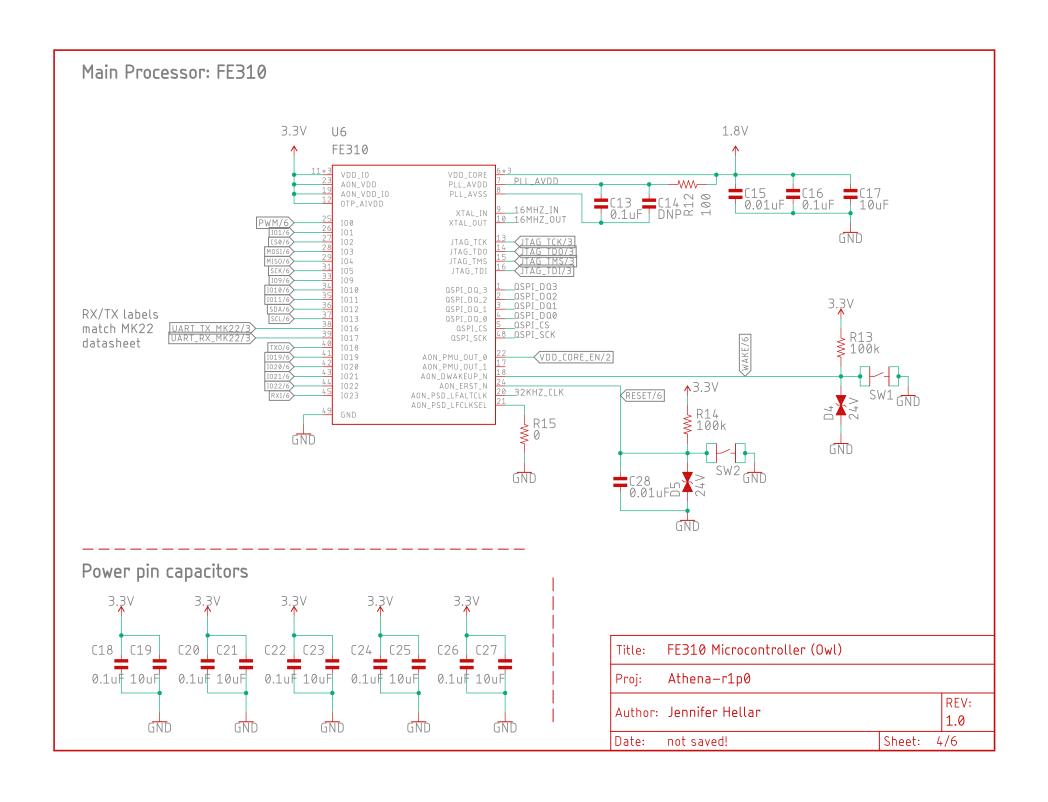
The first RISC-V development board at Rice University, featuring the SiFive FE310 microprocessor, Athena is a prototyping and experimental platform for education and research at Rice. It is intended to be used in undergraduate lab courses and in VIP projects, therefore the design focus is on debug capability and I/O access.

#### May 18, 2022

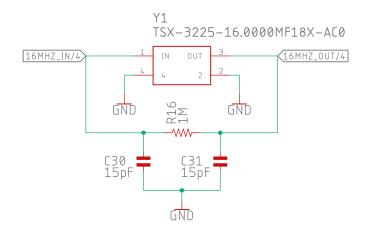
Sheet	Description
1	Cover Page
2	Power: USB, Charging, Voltage Regulators
3	Debug Control: MK22 Processor
4	Main Processor: SiFive FE310, the RISC—V MCU
5	Peripherals: Oscillators, Flash Memory
6	I/O Headers: mikroBus—Compatible, GPIO, and Power; Mechanical



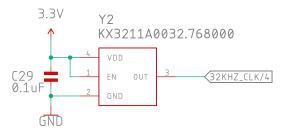
#### MK22 Processor (USB/JTAG/UART controller) 3.3V U5 MK22FN128VLH10 B0 B1 B2 B3 VBATT VREFH PTB0/LLWU\_P5 VDDA PTB1 PTB2 VDD РТВЗ USBVDD UART\_RX\_MK22/4 UART\_TX\_MK22/4 RX/TX\_MK22 labels consistent NC8 PTB16 D -PTB17 USB\_N with MK22 datasheet PTB18 D+ GND USB\_P PTB19 PTE0/VLKOUT32K JTAG\_TD0/4 PTE1/LLWU\_P0 PTC0 PTC1/LLWU\_P6 ADC0\_DP0/ADC1\_DP3 PTC2 ADC0\_DM0/ADC1\_DM3 PTC3/LLWU\_P7 ADC1\_DP0/ADC0\_DP3 PTC4/LLWU\_P8 PTC5/LLWU\_P9 ADC1\_DM0/ADC0\_DM3 VREF OUT PTC6/LLWU\_P10 DAC0\_OUT PTC7 PTC8 DBG\_SWDCLK PTA0 PTC9 3.31 PTA1 PTC10 PTA2 PTC11/LLWU\_P11 PTA3 R9 100 PTA4/LLWU\_P3 PTD0/LLWU\_P12 PTD1 PTA5 -WW JTAG\_TDI/4 3.3V PTA12 PTD2/LLWU\_P13 PTA13/LLWU\_P4 PTD3 PTA18 PTD4/LLWU\_P14 PTA19 PTD5 JTAG TCK/4 R8 — |-| |-| JTAG\_TMS/4 PTD6/LLWU\_P15 ₹ 100k PTD7 10 10 XTAL32 VSSA EXTAL32 VREFL RESET/4 DBG\_RESET) RESET\_B GND Ref. HiFive for MK22 circuit J2 6pin Tag-Connect, MK22 Debug J2 TC2030-IDC-NL MK22 Controller (Nest) Title: DBG\_SWDCLK DBG\_SWO Ргој: Athena-r1p0 REV: GND Author: Jennifer Hellar 1.0 Date: Sheet: 3/6 not saved!



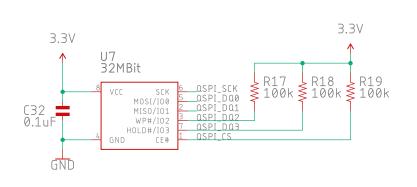
### 16MHz TSX-3225 Oscillator



### 32kHz KX3211 Oscillator



# 32MBit Flash Memory



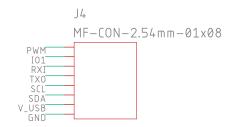
Ref. to HiFive for Flash circuit Prod: IS25LP032D-JBLE

Title:	Oscillators and Memory (Owl)		
Ргој:	Athena-r1p0		
Author:	Jennifer Hellar		REV: 1.0
Date:	not saved!	Sheet:	5/6

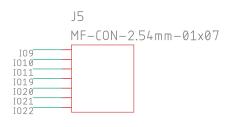
# mikroBus Left Header



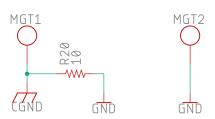
# mikroBus Right Header



# GPIO Header



# Mechanical & Grounds



Title:	I/O Headers (Owl)			
Ргој:	Athena-r1p0			
Author:	Jennifer Hellar			REV: 1.0
Date:	not saved!	Sheet:	6	5/6