Athena Design Rev. 1.0 Schematic

RVR Lab, Rice University, Houston TX

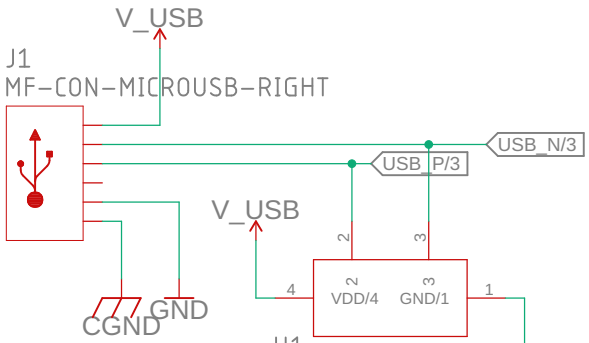
The first RISC-V development board at Rice University, featuring the SiFive FE310 microprocessor, Athena is a prototyping and experimental platform for education and research at Rice. It is intended to be used in undergraduate lab courses and in VIP projects, therefore the design focus is on debug capability and I/O access.

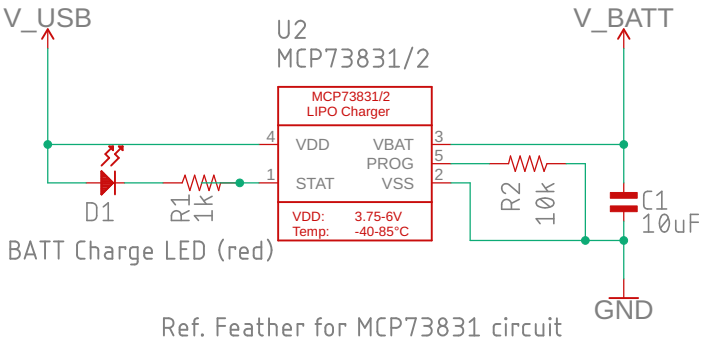
Aug. 5, 2021

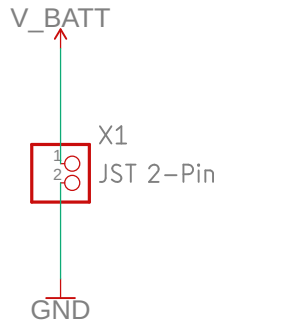
Sheet	Description
1	Cover Page
2	Power: USB, Charging, Voltage Regulators
3	Debug Control: MK22 Processor
4	Debug Headers: MK22 Tag, FE310 Tag, MK22->FE310 Bridge
5	Main Processor: SiFive FE310, the RISC-V MCU
6	Peripherals: Oscillators, Flash Memory
7	I/O Headers: mikroBus-Compatible, GPIO, and Power; Mechanical

Designed in EAGLE 9.6.2.

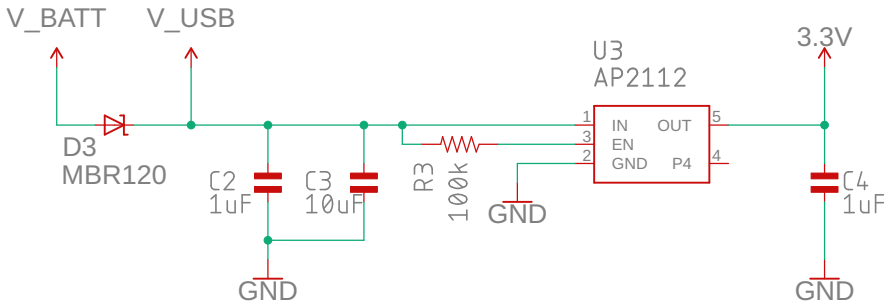
USB & Battery Charging

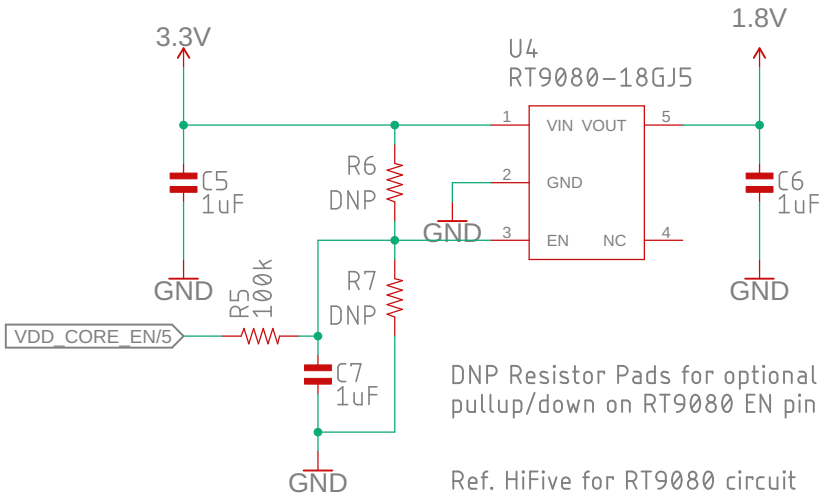


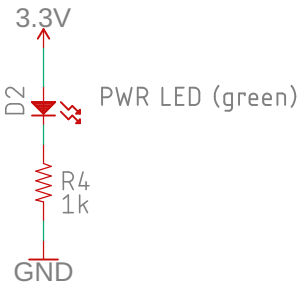




Power & Filtering

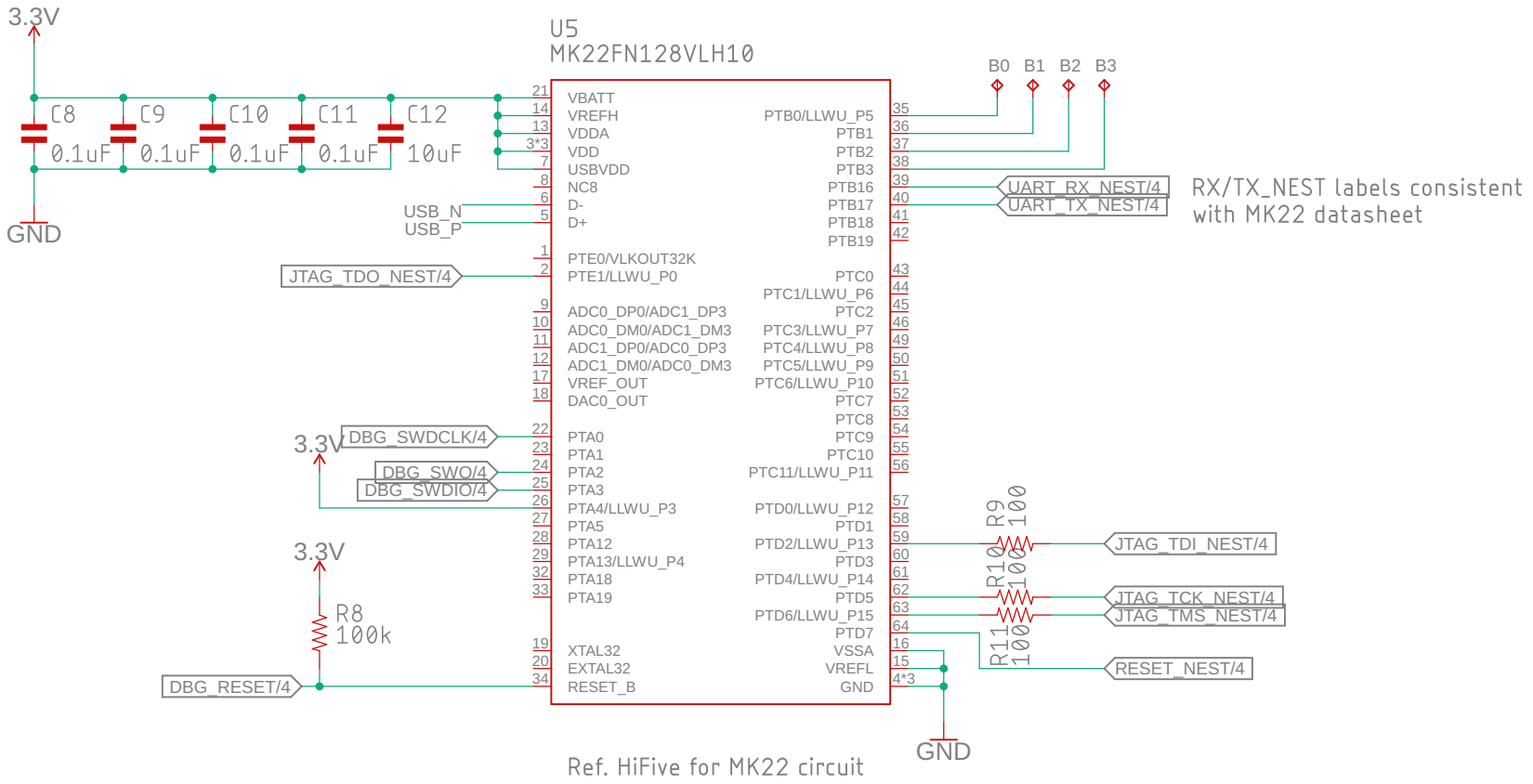






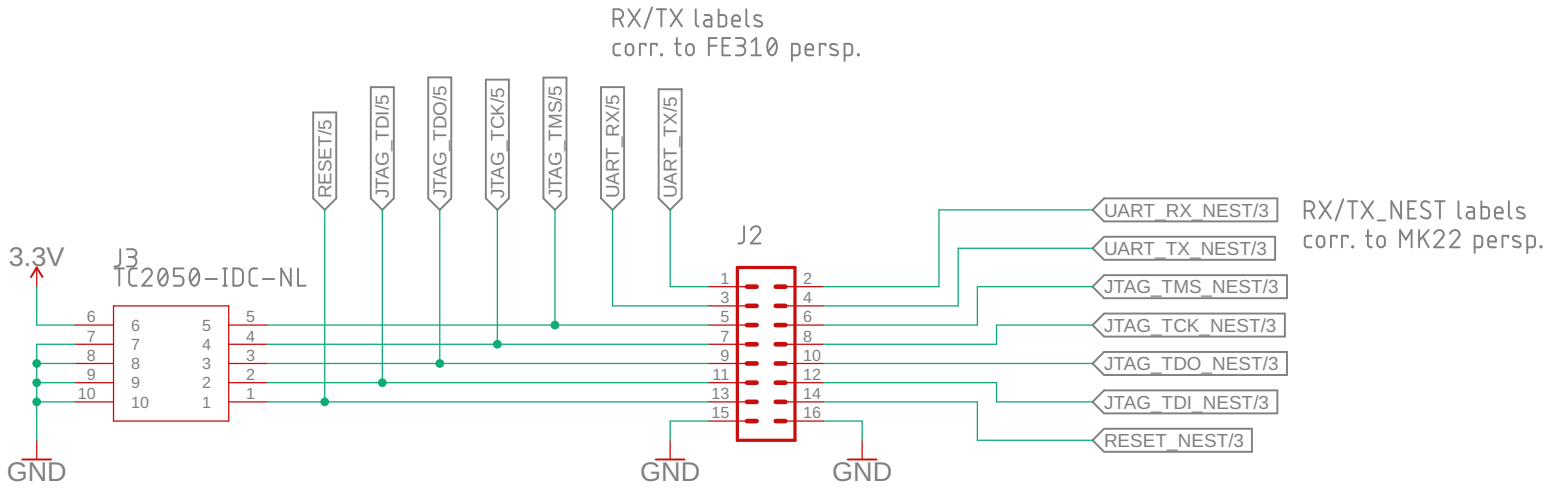
Title:	Power		
Proj:	Athena-r1p0		
Author:	Jennifer Hellar	REV:	1.0
Date:	8/5/2021 7:44 PM	Sheet:	2/7

MK22 Processor (USB/JTAG/UART controller)

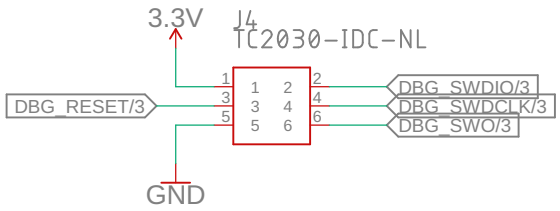


Title:	MK22 Controller (Nest)		
Proj:	Athena-r1p0		
Author:	Jennifer Hellar		REV: 1.0
Date:	8/5/2021 7:44 PM	Sheet:	3/7

J2 Bridge for on/off-board FE310 Debug,
J3 10pin Tag-Connect for on-board FE310 Debug



J4 6pin Tag-Connect, MK22 Debug



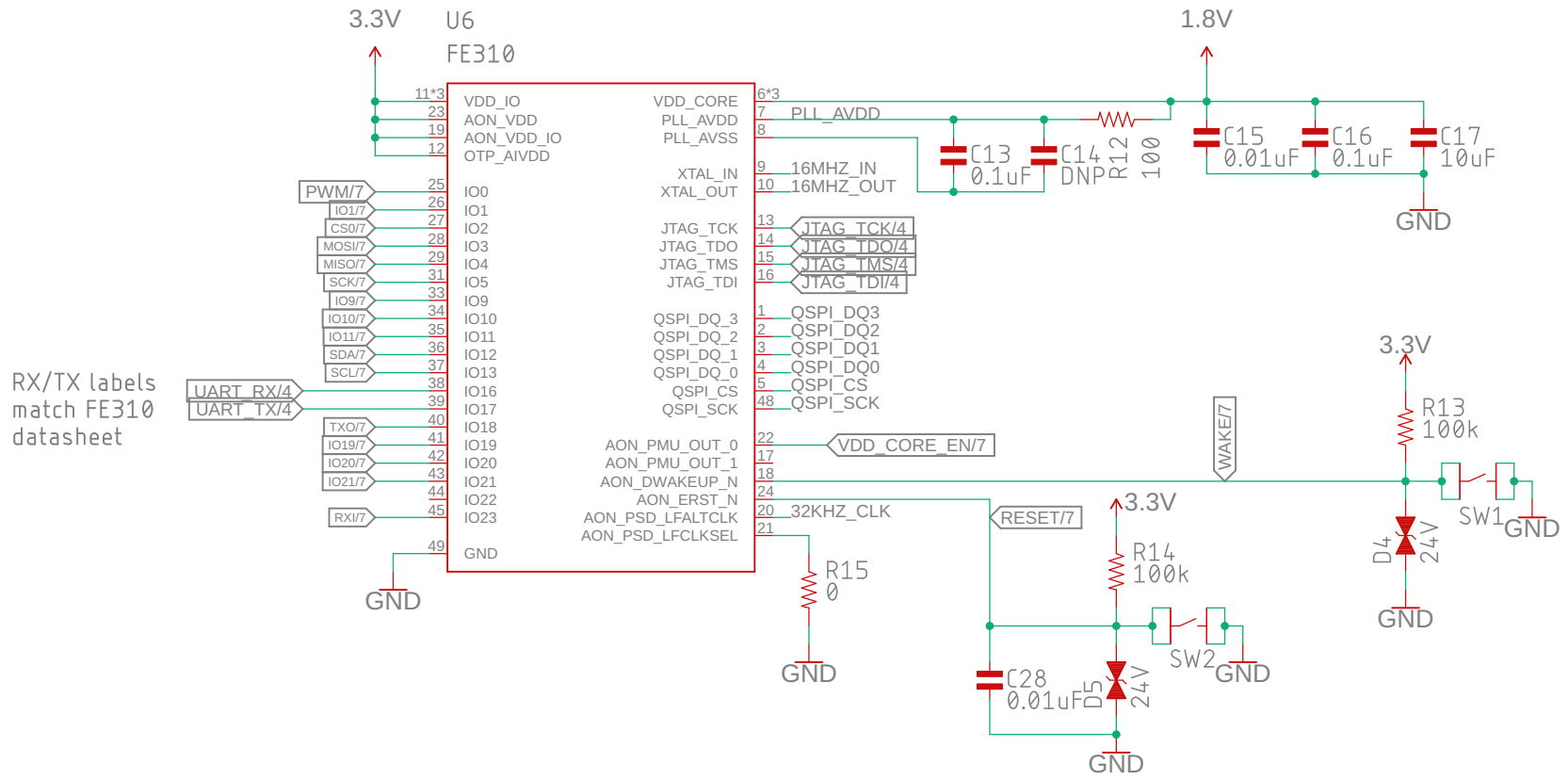
J2 Bridge connector notes

Default: Closed (1->2, 3->4, ..., 15->16) to program/debug on-board (Athena) FE310.

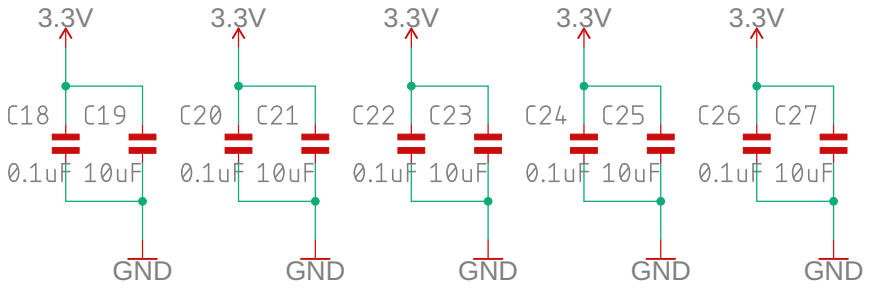
Open and access NEST-side pins to program/debug off-board FE310 using Athena MK22 controller.

Title:	Bridge and Debug Headers	
Proj:	Athena-r1p0	
Author:	Jennifer Hellar	REV: 1.0
Date:	8/5/2021 7:44 PM	Sheet: 4/7

Main Processor: FE310

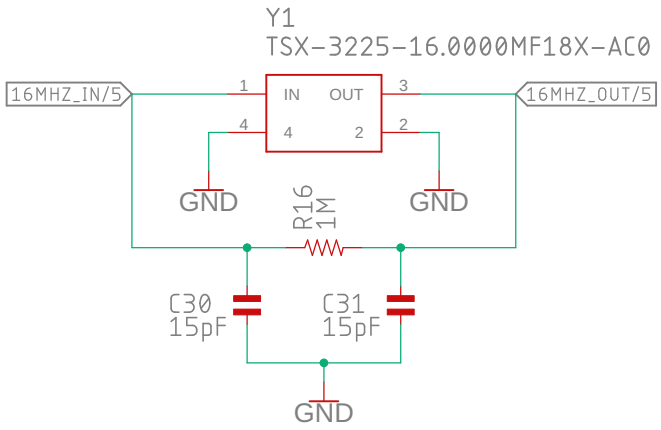


Power pin capacitors

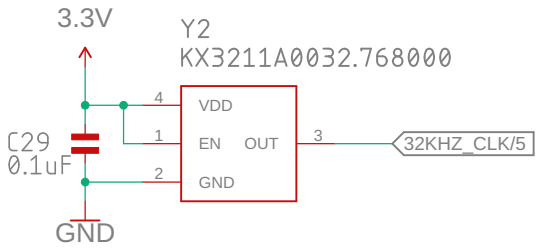


Title:	FE310 Microcontroller (Owl)		
Proj:	Athena-r1p0		
Author:	Jennifer Hellar	REV:	1.0
Date:	8/5/2021 7:44 PM	Sheet:	5/7

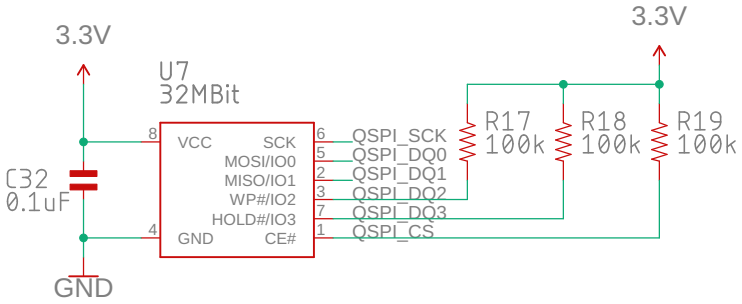
16MHz TSX-3225 Oscillator



32kHz KX3211 Oscillator



32MBit Flash Memory

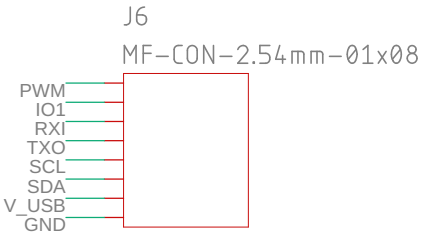


Ref. to HiFive for Flash circuit
Prod: IS25LP032D-JBLE

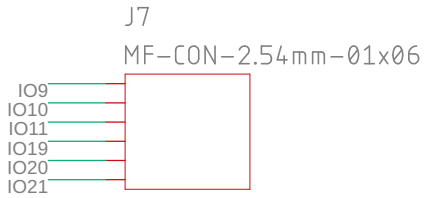
Title:	Oscillators and Memory (Owl)		
Proj:	Athena-r1p0		
Author:	Jennifer Hellar		REV: 1.0
Date:	8/5/2021 7:44 PM	Sheet:	6/7

mikroBus Left Header

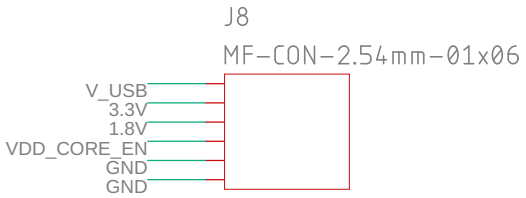
mikroBus Right Header



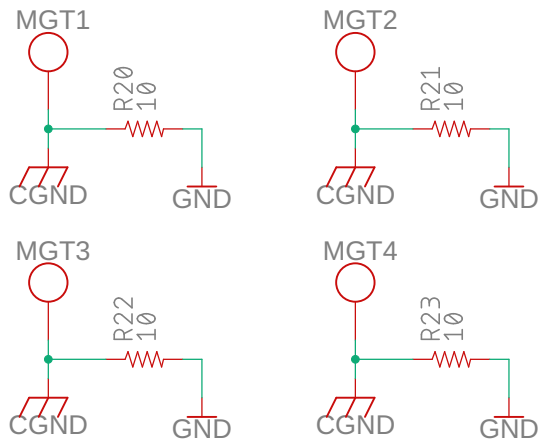
GPIO Header



Power Header



Mechanical & Grounds



Title:	I/O Headers (Owl)	
Proj:	Athena-r1p0	
Author:	Jennifer Hellar	REV: 1.0
Date:	8/5/2021 7:44 PM	Sheet: 7/7