

Athena Design Rev. 1.0 Schematic

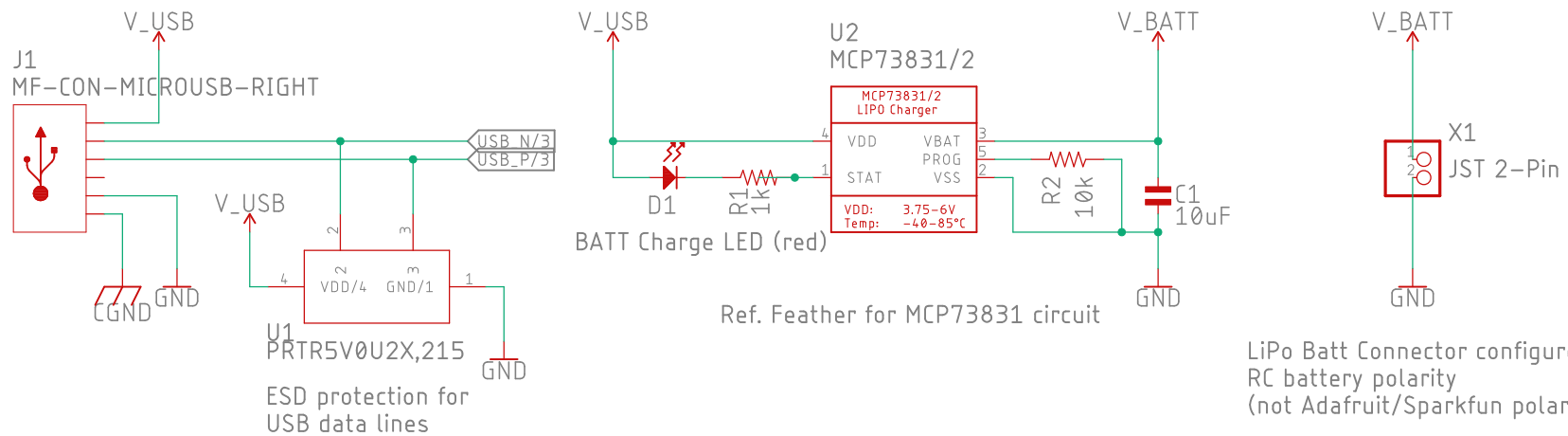
RVR Lab, Rice University, Houston TX

The first RISC-V development board at Rice University, featuring the SiFive FE310 microprocessor, Athena is a prototyping and experimental platform for education and research at Rice. It is intended to be used in undergraduate lab courses and in VIP projects, therefore the design focus is on debug capability and I/O access.

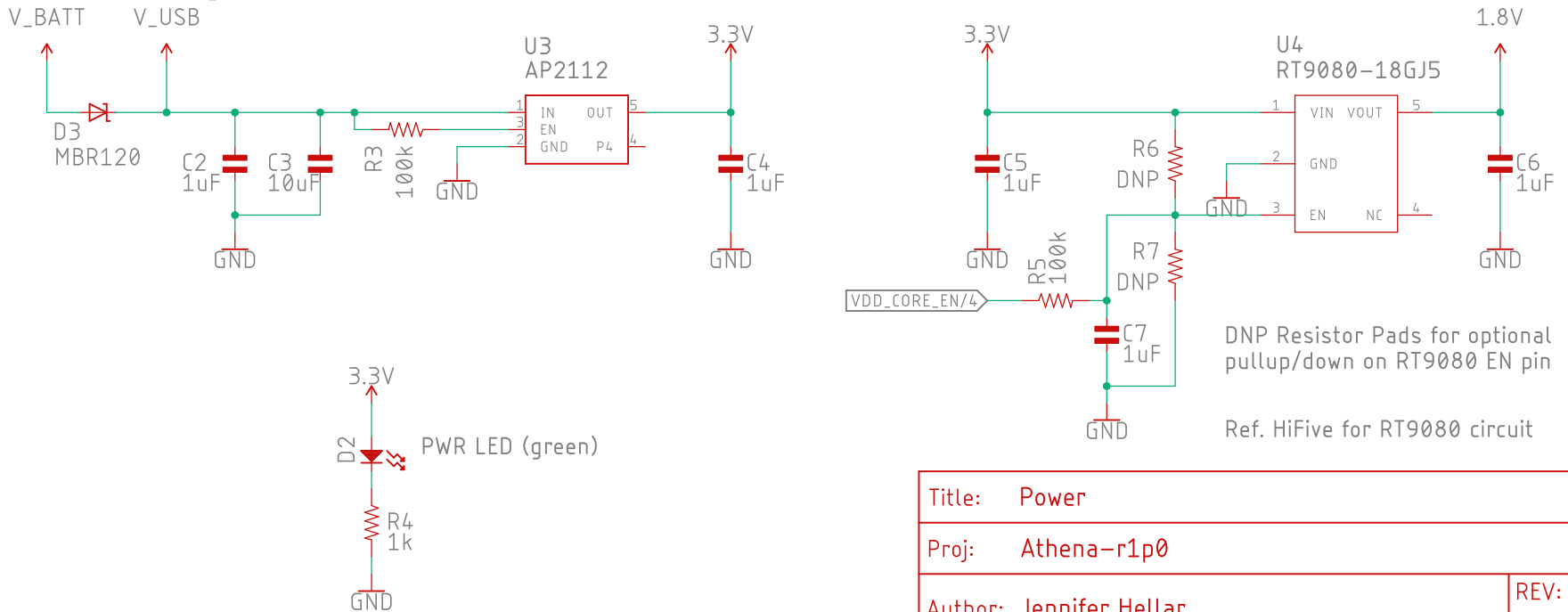
May 18, 2022

Sheet	Description
1	Cover Page
2	Power: USB, Charging, Voltage Regulators
3	Debug Control: MK22 Processor
4	Main Processor: SiFive FE310, the RISC-V MCU
5	Peripherals: Oscillators, Flash Memory
6	I/O Headers: mikroBus-Compatible, GPIO, and Power; Mechanical

USB & Battery Charging



Power & Filtering



Title: Power

Proj: Athena-r1p0

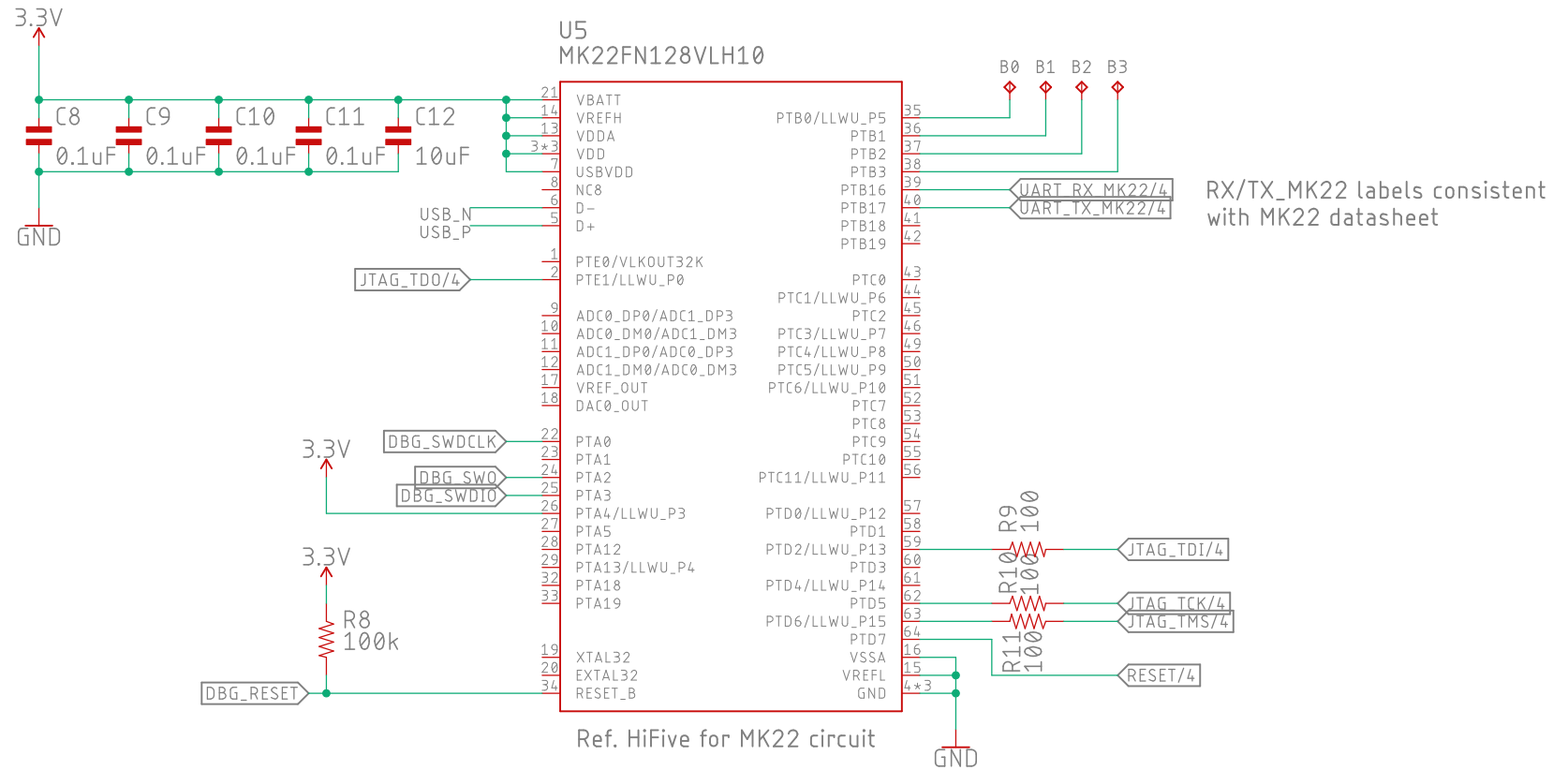
Author: Jennifer Hellar

REV:
1.0

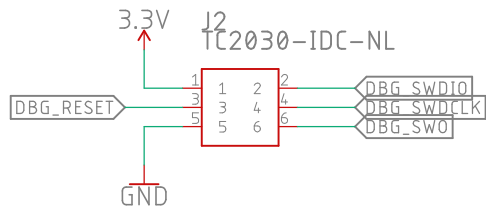
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Sheet: 2/6

MK22 Processor (USB/JTAG/UART controller)

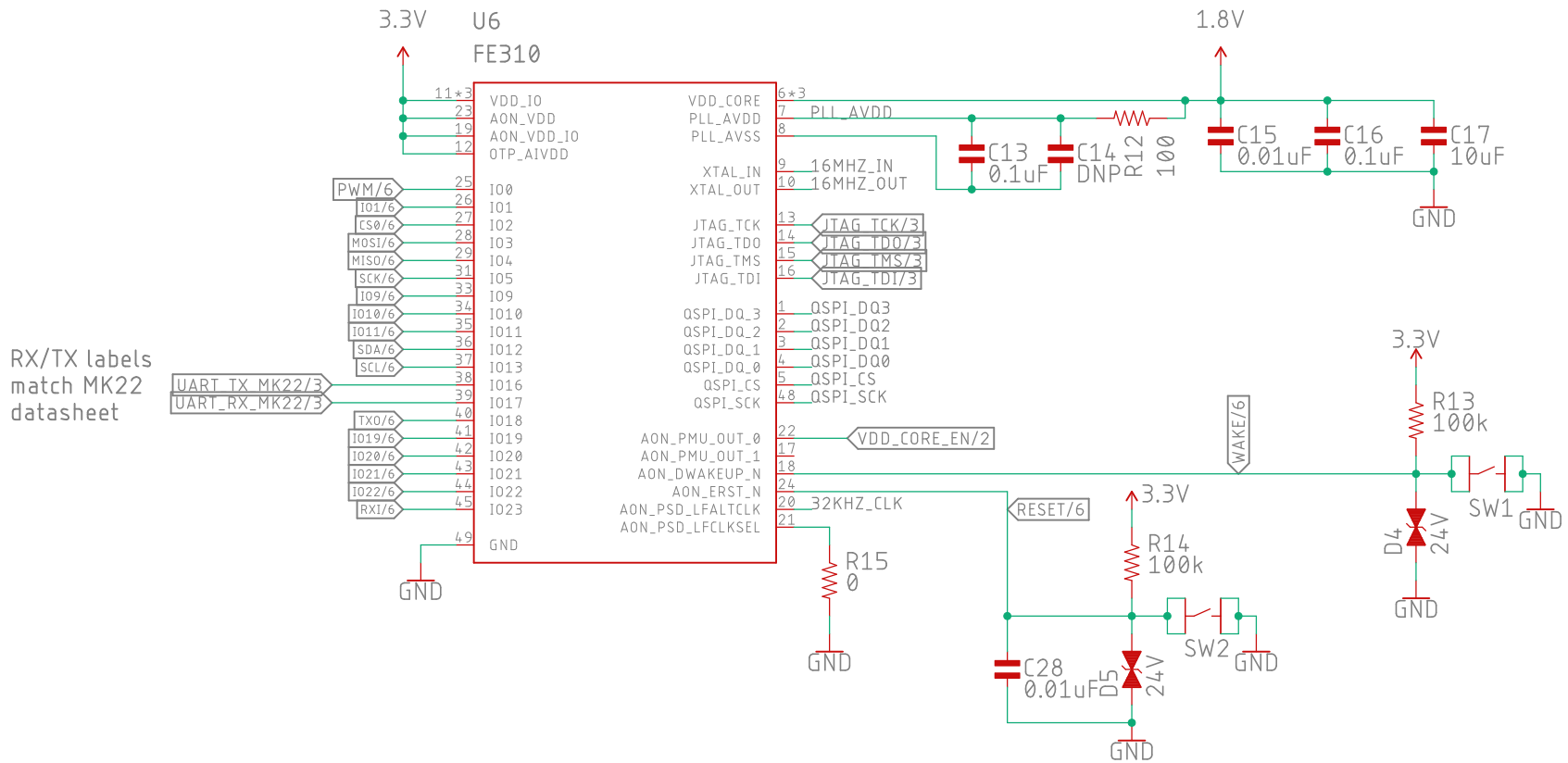


J2 6pin Tag-Connect, MK22 Debug

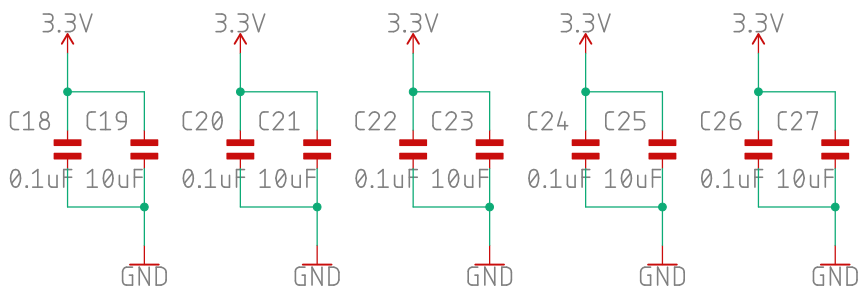


Title:	MK22 Controller (Nest)		
Proj:	Athena-r1p0		
Author:	Jennifer Hellar		REV: 1.0
Date:	not saved!	Sheet:	3/6

Main Processor: FE310

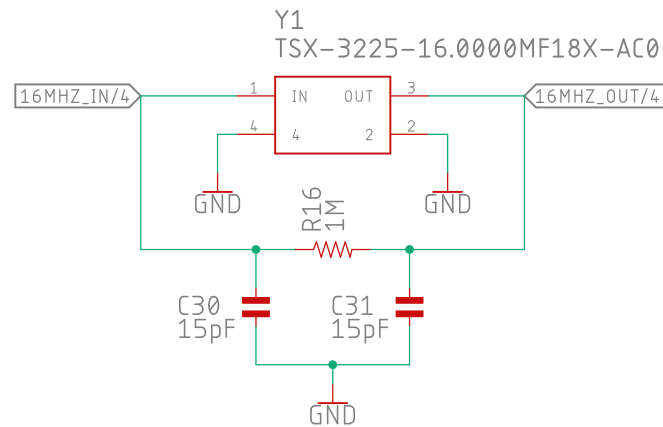


Power pin capacitors

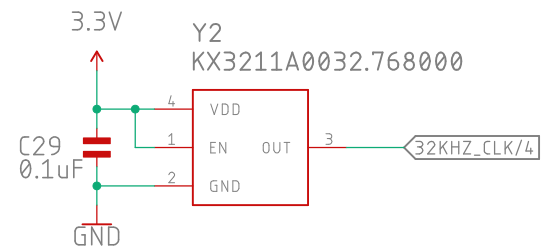


Title: FE310 Microcontroller (Owl)	
Proj: Athena-r1p0	
Author: Jennifer Hellar	REV: 1.0
Date: not saved!	Sheet: 4/6

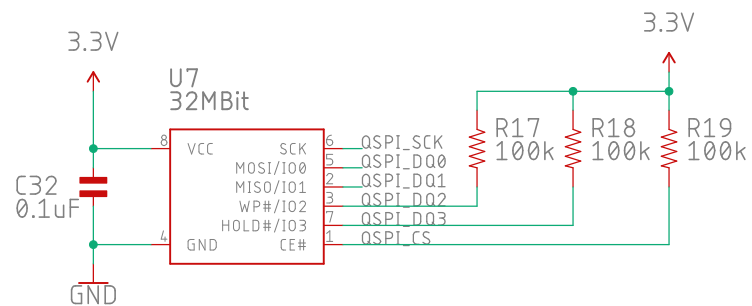
16MHz TSX-3225 Oscillator



32kHz KX3211 Oscillator



32MBit Flash Memory



Ref. to HiFive for Flash circuit
Prod: IS25LP032D-JBLE

Title: Oscillators and Memory (Owl)

Proj: Athena-r1p0

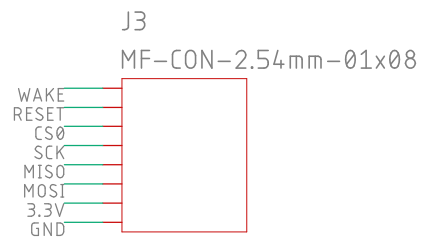
Author: Jennifer Hellar

REV:
1.0

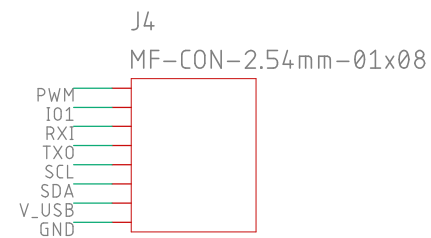
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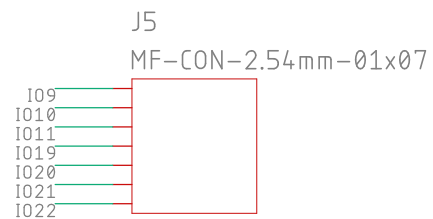
mikroBus Left Header



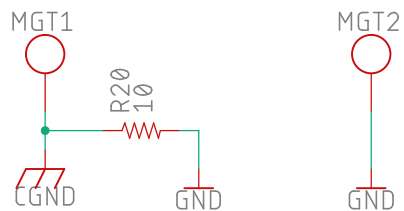
mikroBus Right Header



GPIO Header



Mechanical & Grounds



Title: I/O Headers (Owl)

Proj: Athena-r1p0

Author: Jennifer Hellar

REV:
1.0

Date: not saved!

Sheet: 6/6