# Athena Design Rev. A1 Schematic RVR Lab, Rice University, Houston TX

The first RISC-V development board at Rice University, featuring the SiFive FE310 microprocessor, Athena is a prototyping and experimental platform for education and research at Rice. It is intended to be used in undergraduate lab courses and in VIP projects, therefore the design focus is on debug capability and I/O access.

### July 25, 2022

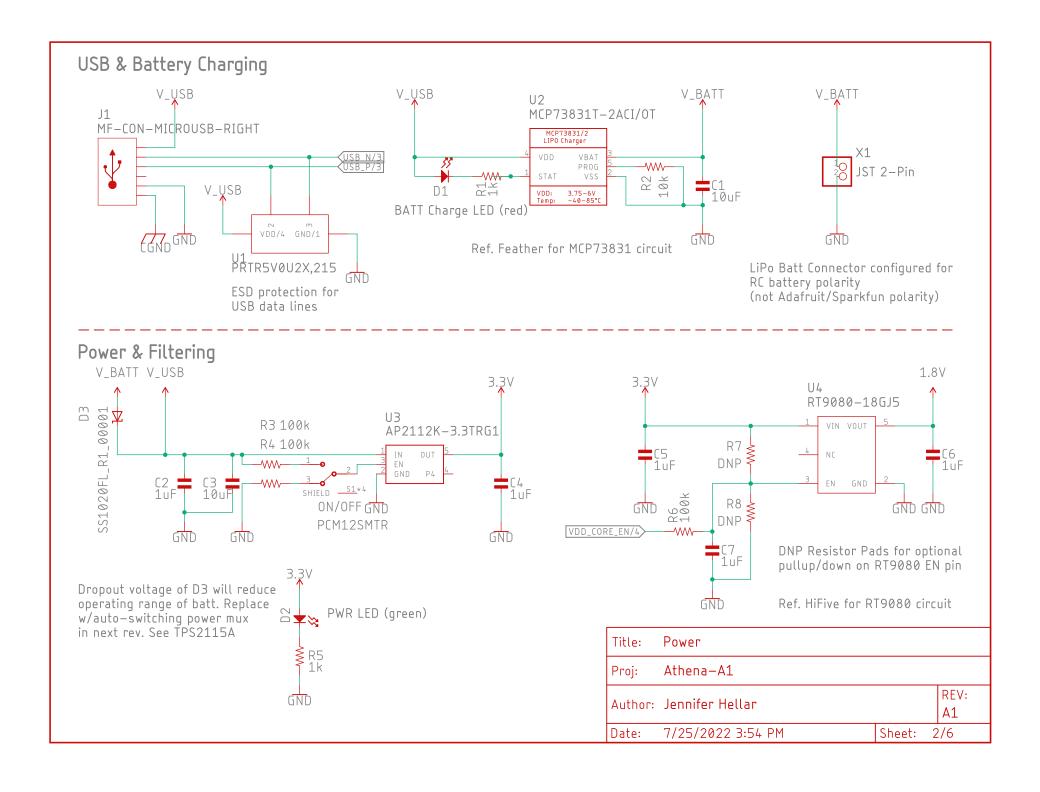
| Sheet | Description   |
|-------|---|
| 1     | Cover Page  |
| 2     | Power: USB, Charging, Voltage Regulators                      |
| 3     | Debug Control: MK22 Processor                                 |
| 4     | Main Processor: SiFive FE310, the RISC—V MCU                  |
| 5     | Peripherals: Oscillators, Flash Memory                        |
| 6     | I/O Headers: mikroBus—Compatible, GPIO, and Power; Mechanical |

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Designed in EAGLE 9.6.2.



#### MK22 Processor (USB/JTAG/UART controller) 3.3V U5 MK22FN128VLH10 0 1 2 3 VBATT VREFH PTB0/LLWU\_P5 VDDA PTB1 PTB2 VDD USBVDD PTB3 UART\_RX\_MK22/4 UART\_TX\_MK22/4 RX/TX\_MK22 labels consistent NC8 PTB16 D -PTB17 USB\_N with MK22 datasheet PTB18 D+ GND USB\_P PTB19 PTE0/VLKOUT32K JTAG\_TD0/4 PTE1/LLWU\_P0 PTC0 PTC1/LLWU\_P6 ADC0\_DP0/ADC1\_DP3 PTC2 ADC0\_DM0/ADC1\_DM3 PTC3/LLWU\_P7 ADC1\_DP0/ADC0\_DP3 PTC4/LLWU\_P8 ADC1\_DM0/ADC0\_DM3 PTC5/LLWU\_P9 VREF OUT PTC6/LLWU\_P10 DAC0\_OUT PTC7 PTC8 DBG\_SWDCLK PTA0 PTC9 3.31 PTA1 PTC10 PTA2 PTC11/LLWU\_P11 PTA3 PTA4/LLWU\_P3 PTD0/LLWU\_P12 100 PTD1 PTA5 PTD2/LLWU\_P13 JTAG\_TDI/4 3.3V PTA12 PTD3 PTA13/LLWU\_P4 PTA18 PTD4/LLWU\_P14 PTD5 JTAG TCK/4 JTAG TMS/4 RESET/4 PTA19 R9 PTD6/LLWU\_P15 ₹100k PTD7 XTAL32 VSSA EXTAL32 VREFL DBG\_RESET) RESET\_B GND Ref. HiFive for MK22 circuit J2 6pin Tag-Connect, MK22 Debug J2 TC2030-IDC-NL MK22 Controller (Nest) Title: DBG\_SWDCLK DBG\_SWO Athena-A1 Proj: REV: GND Author: Jennifer Hellar

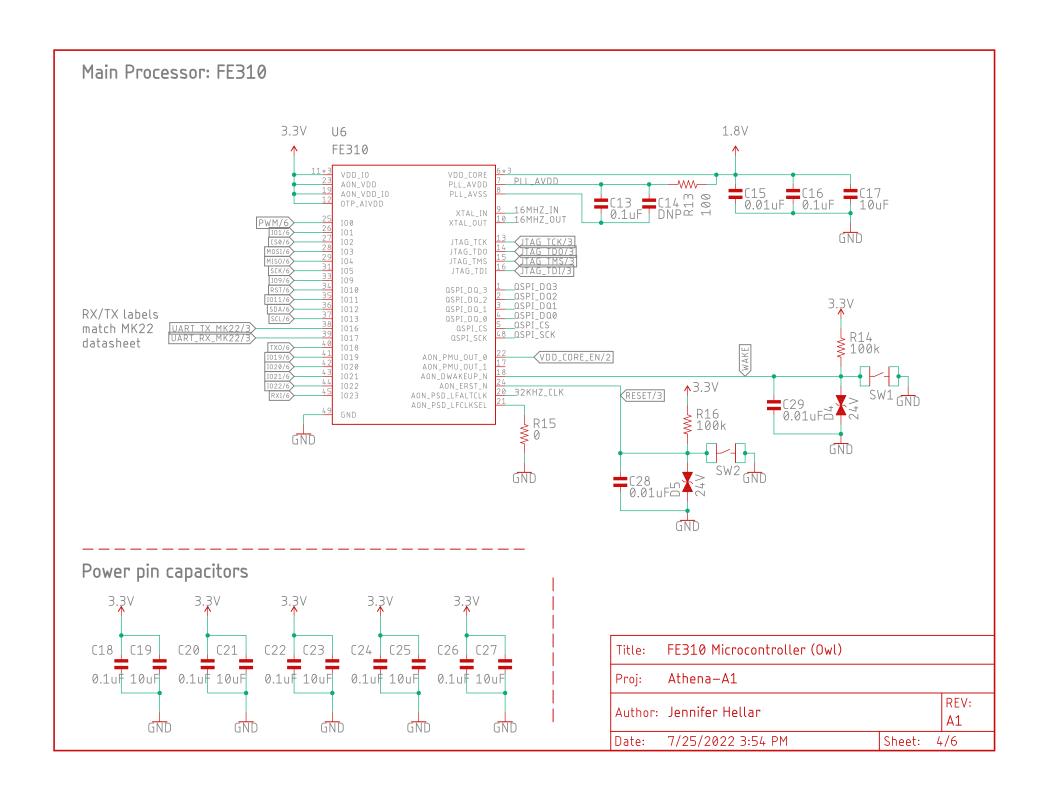
**A1** 

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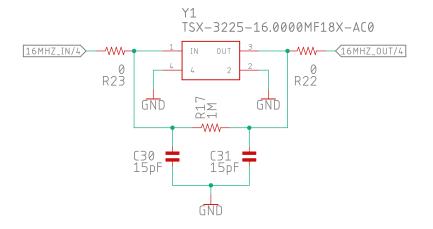
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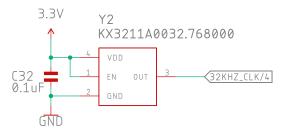
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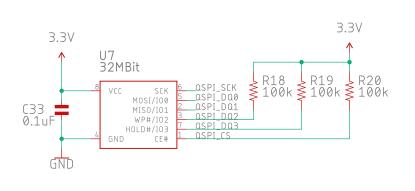
# 16MHz TSX-3225 Crystal



## 32kHz KX3211 Oscillator



# 32MBit Flash Memory



Ref. to HiFive for Flash circuit

Prod: IS25LP032D-JBLE

Title: Oscillators and Memory (Owl)

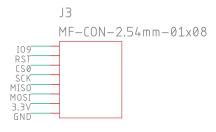
Proj: Athena—A1

Author: Jennifer Hellar

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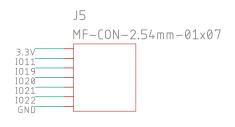
# mikroBus Left Header



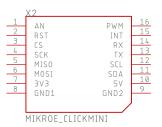
# mikroBus Right Header



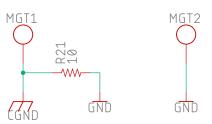
# GPIO Header



Top—left pin of mikroBus std is an analog input. FE310 has no internal ADC, so this is GPIO instead. Recommend adding an I2C ADC chip (e.g. ADC121C027) in next rev.



## Mechanical & Grounds



Title: I/O Headers (Owl)

Proj: Athena—A1

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REV:

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