

Athena Design Rev. A1 Schematic

RVR Lab, Rice University, Houston TX

The first RISC–V development board at Rice University, featuring the SiFive FE310 microprocessor, Athena is a prototyping and experimental platform for education and research at Rice. It is intended to be used in undergraduate lab courses and in VIP projects, therefore the design focus is on debug capability and I/O access.

July 25, 2022

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3	Debug Control: MK22 Processor
4	Main Processor: SiFive FE310, the RISC–V MCU
5	Peripherals: Oscillators, Flash Memory
6	I/O Headers: mikroBus–Compatible, GPIO, and Power; Mechanical

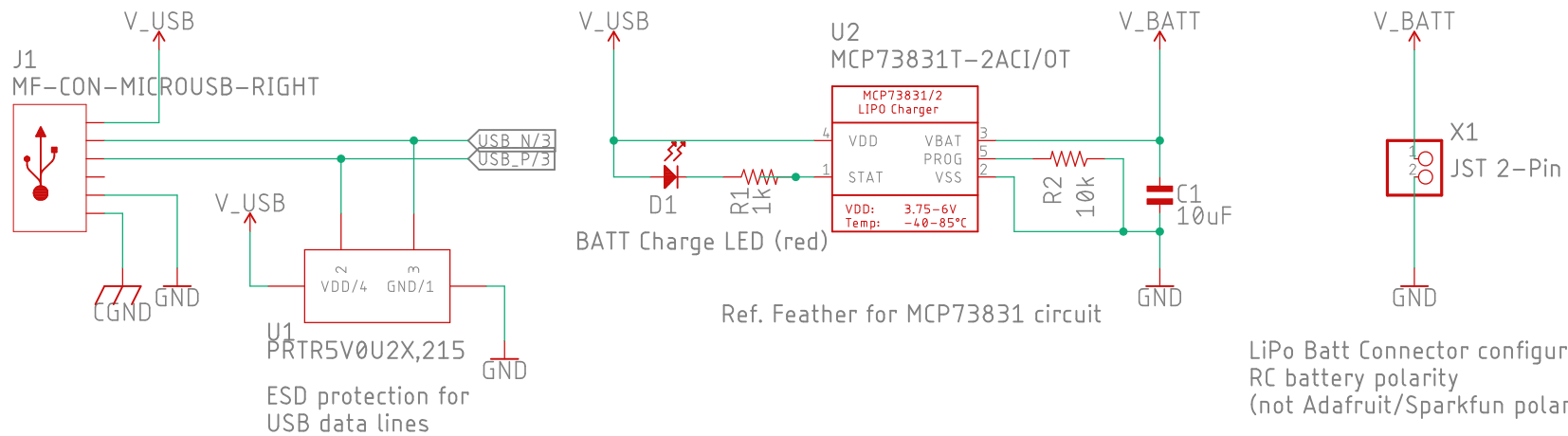
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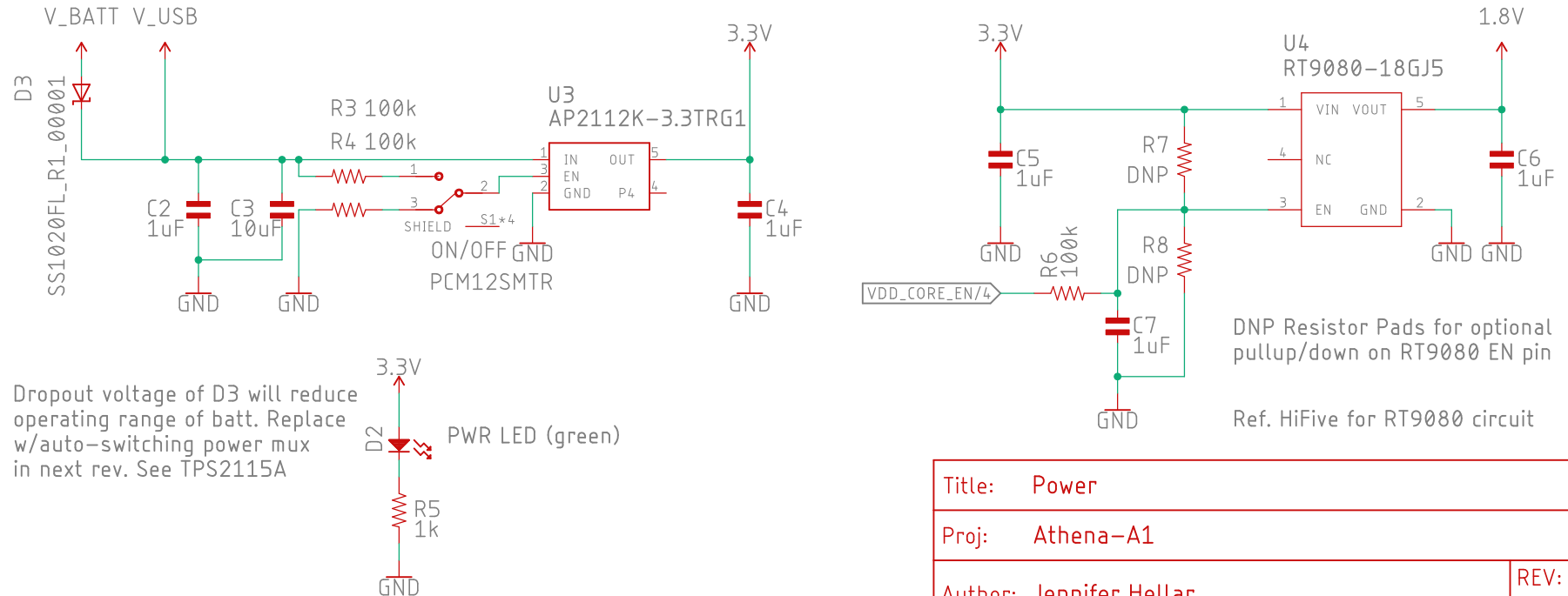
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Designed in EAGLE 9.6.2.

USB & Battery Charging



Power & Filtering



Title: Power

Proj: Athena-A1

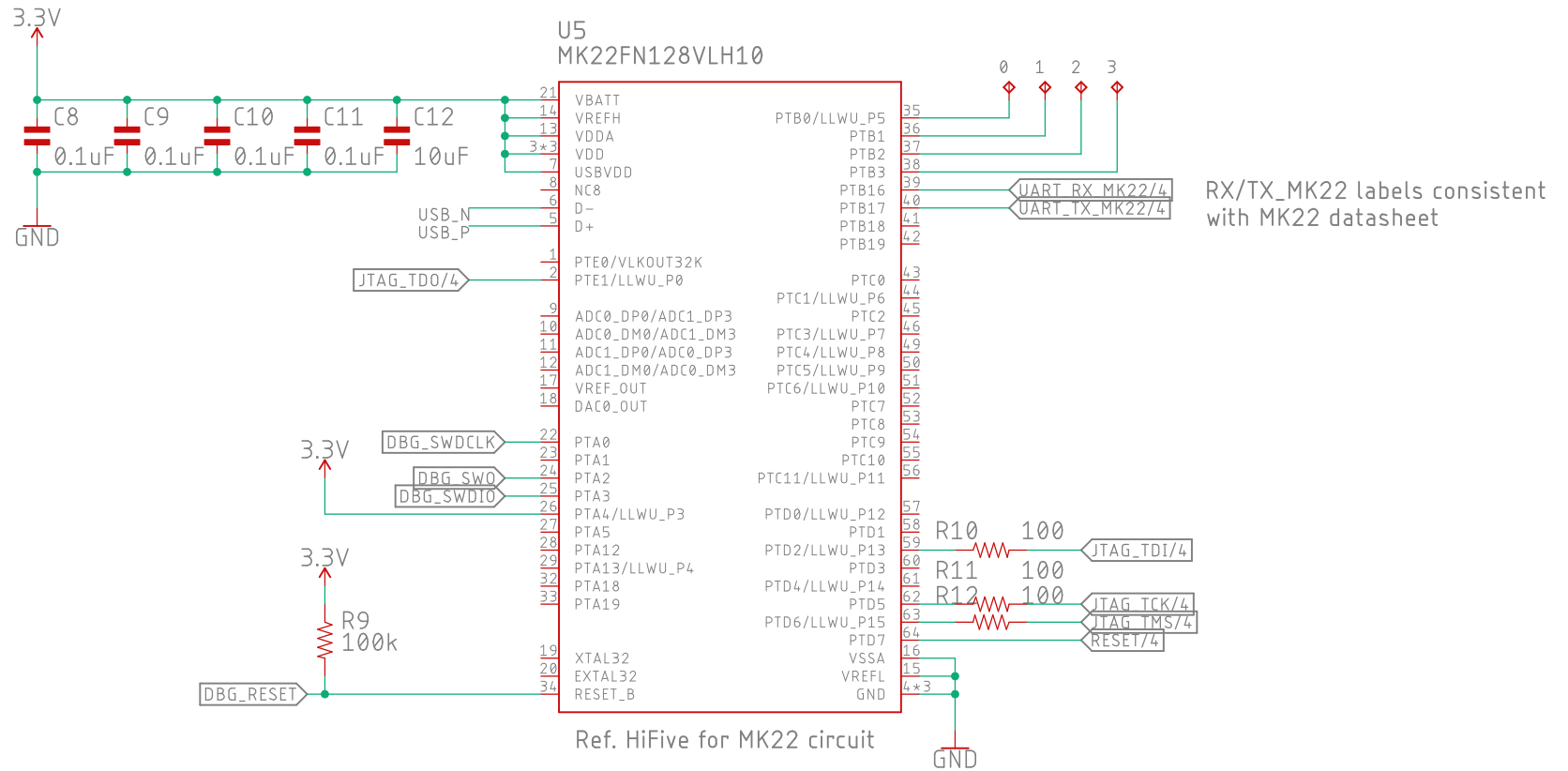
Author: Jennifer Hellar

REV:
A1

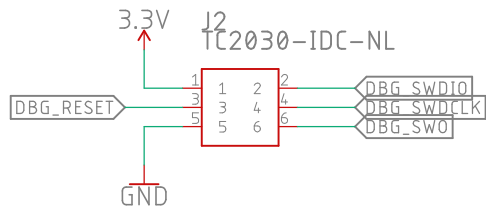
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MK22 Processor (USB/JTAG/UART controller)

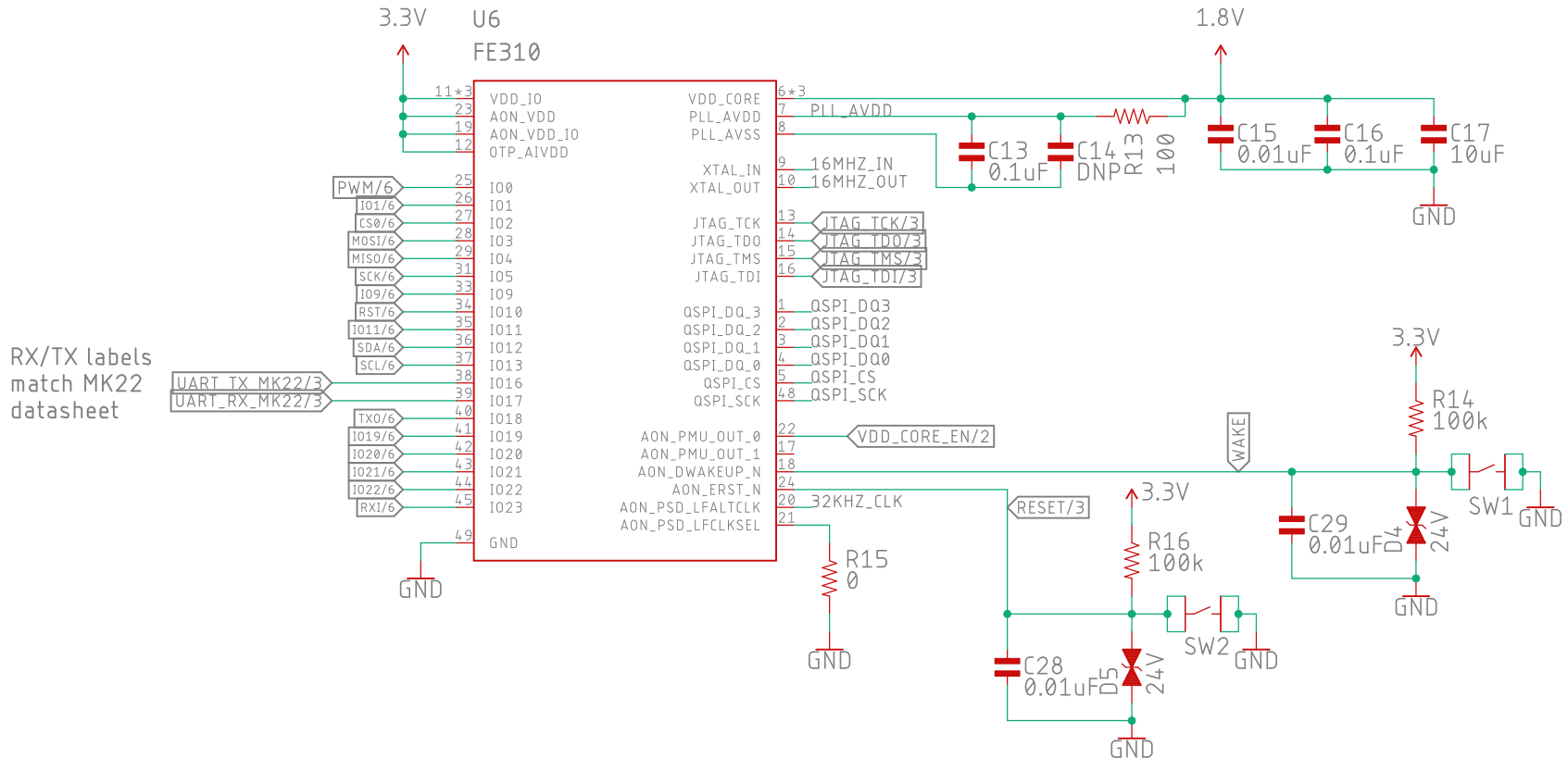


J2 6pin Tag-Connect, MK22 Debug

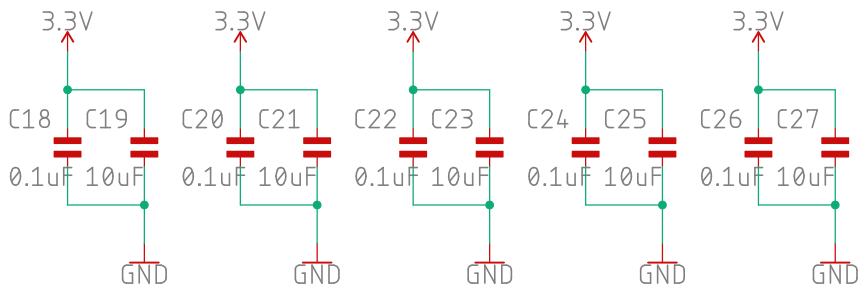


Title: MK22 Controller (Nest)	
Proj: Athena-A1	
Author: Jennifer Hellar	REV: A1
Date: 7/25/2022 3:54 PM	Sheet: 3/6

Main Processor: FE310

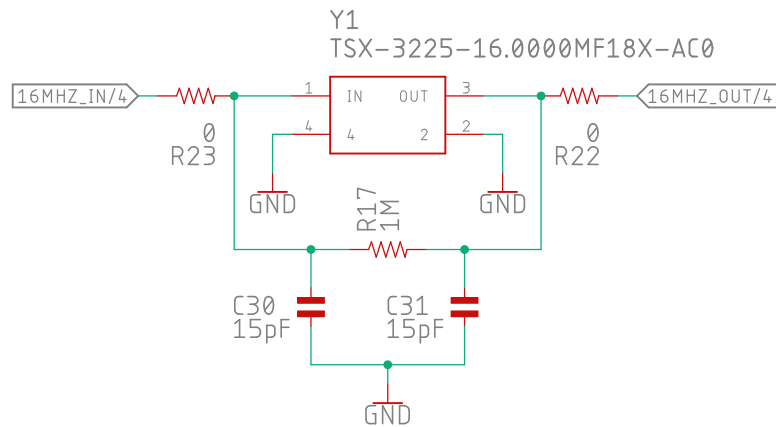


Power pin capacitors

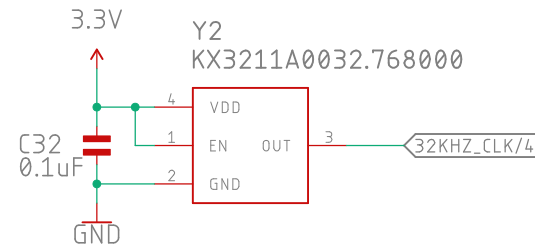


Title: FE310 Microcontroller (Owl)	
Proj: Athena-A1	
Author: Jennifer Hellar	REV: A1
Date: 7/25/2022 3:54 PM	Sheet: 4/6

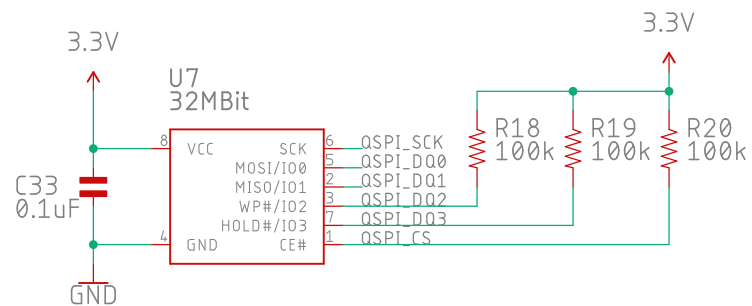
16MHz TSX-3225 Crystal



32kHz KX3211 Oscillator



32MBit Flash Memory



Ref. to HiFive for Flash circuit
Prod: IS25LP032D-JBLE

Title: Oscillators and Memory (Owl)

Proj: Athena-A1

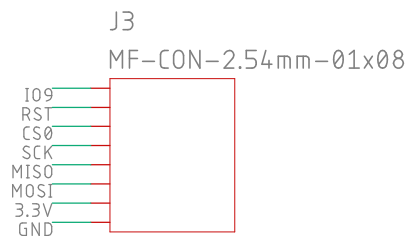
Author: Jennifer Hellar

REV:
A1

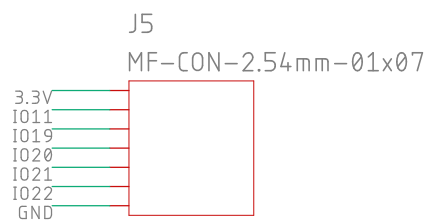
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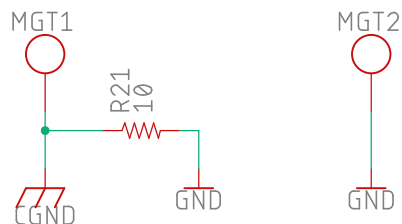
mikroBus Left Header



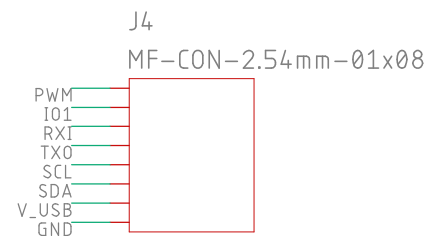
GPIO Header



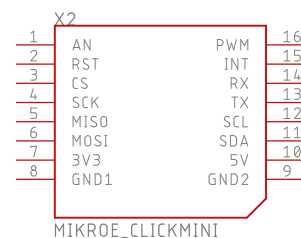
Mechanical & Grounds



mikroBus Right Header



Top-left pin of mikroBus std is an analog input. FE310 has no internal ADC, so this is GPIO instead. Recommend adding an I2C ADC chip (e.g. ADC121C027) in next rev.



Title: I/O Headers (Owl)

Proj: Athena-A1

Author: Jennifer Hellar

REV:
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