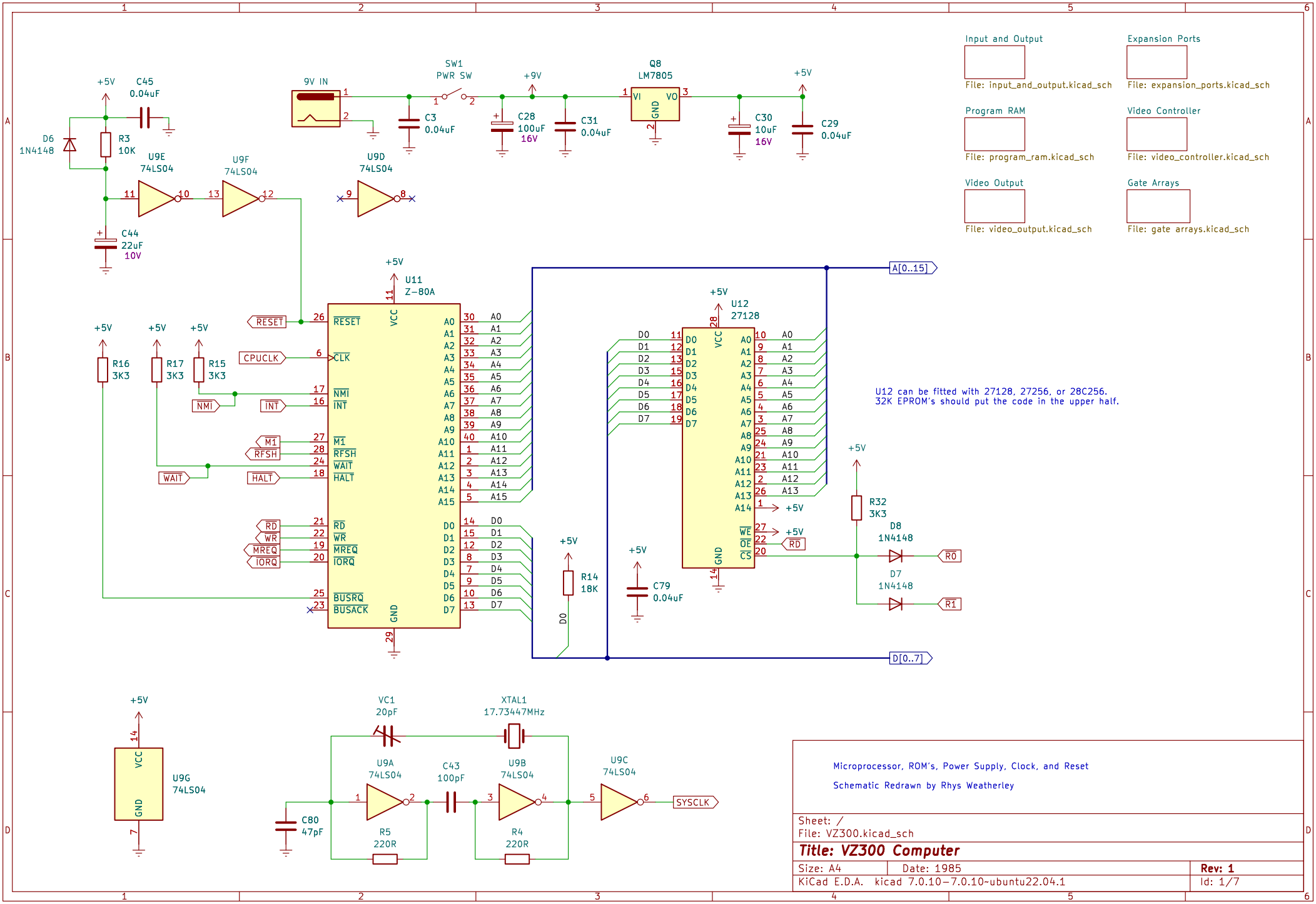
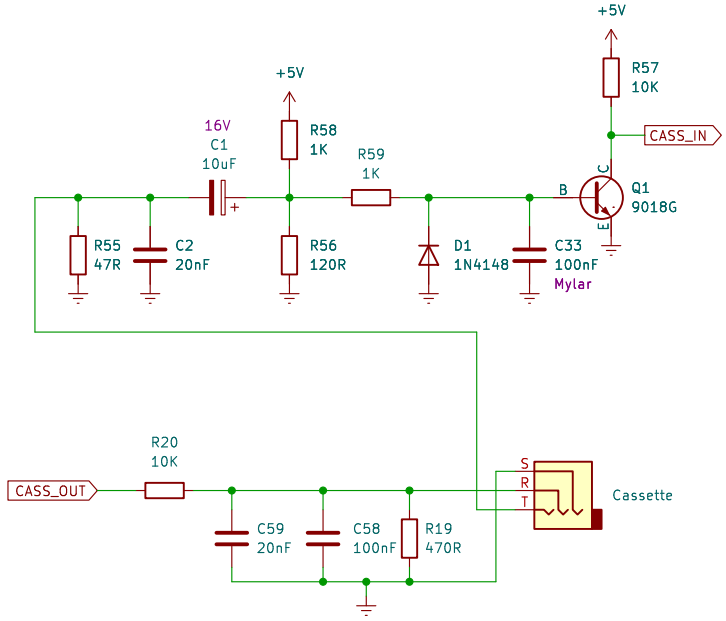
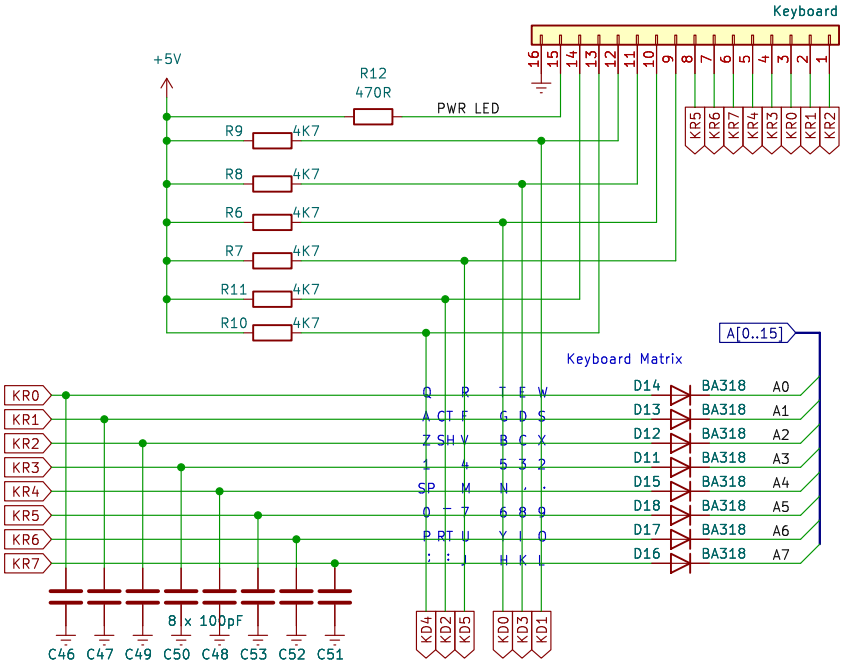

Input and Output
File: input_and_output.kicad_sch
Expansion Ports
File: expansion_ports.kicad_sch
Program RAM
File: program_ram.kicad_sch
Video Controller
File: video_controller.kicad_sch
Video Output
File: video_output.kicad_sch
Gate Arrays
File: gate arrays.kicad_sch
9V IN
SW1
PWR SW
Q8
LM7805
C45
0.04uF
C3
0.04uF
C28
100uF
16V
C31
0.04uF
C30
10uF
16V
C29
0.04uF
D6
1N4148
R3
10K
U9E
74LS04
U9F
74LS04
U9D
74LS04
C44
22uF
10V
U11
Z-80A
RESET
CPUCLK
NMI
INT
M1
RFSH
WAIT
HALT
BUSRQ
BUSACK
R16
3K3
R17
3K3
R15
3K3
A[0..15]
D[0..7]
U12
27128
U12 can be fitted with 27128, 27256, or 28C256.
32K EPROM's should put the code in the upper half.
R14
18K
C79
0.04uF
R32
3K3
D8
1N4148
D7
1N4148
R0
R1
U9G
74LS04
VC1
20pF
XTAL1
17.73447MHz
U9A
74LS04
C43
100pF
U9B
74LS04
U9C
74LS04
C80
47pF
R5
220R
R4
220R
SYSCLK
Microprocessor, ROM's, Power Supply, Clock, and Reset
Schematic Redrawn by Rhys Weatherley
Sheet: /
File: VZ300.kicad_sch
Title: VZ300 Computer
Size: A4
Date: 1985
Rev: 1
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1
Id: 1/7





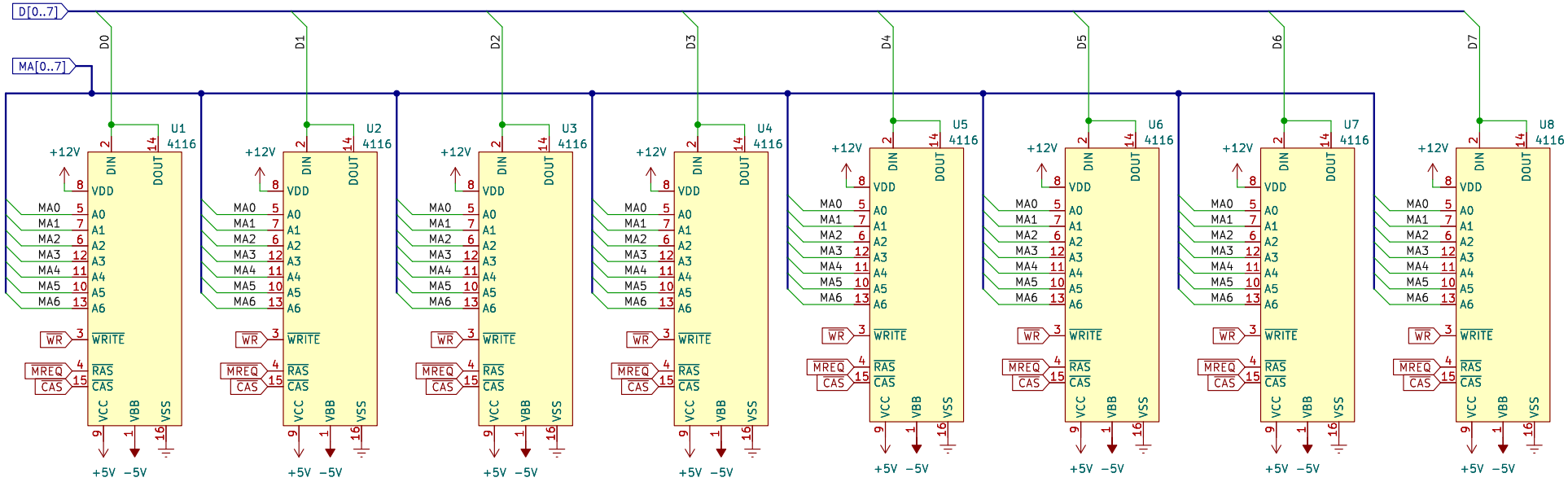
Input and Output

Schematic Redrawn by Rhys Weatherley

Sheet: /Input and Output/
File: input_and_output.kicad_sch

Title: VZ300 Computer

Size: A4	Date: 1985	**Rev: 1**
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1		Id: 2/7

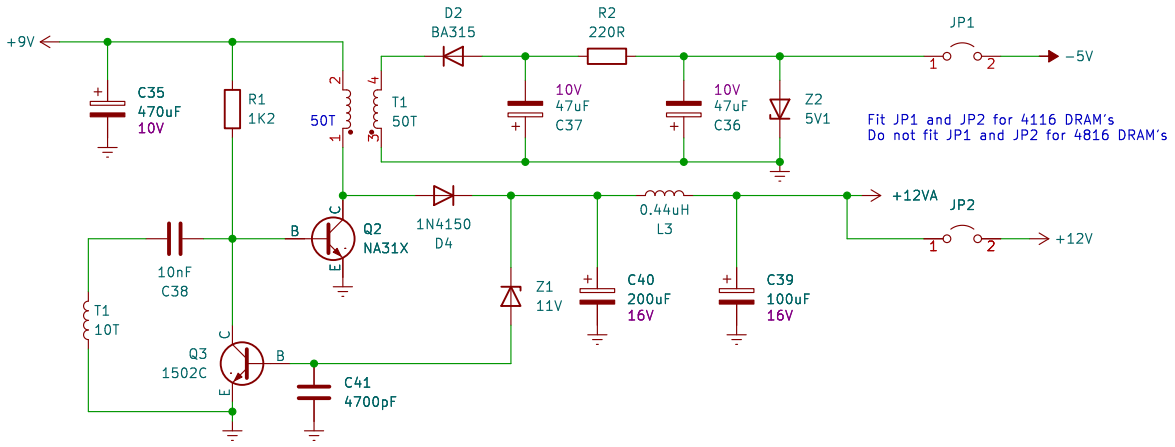


Placement of DRAM Chips on the PCB

Rear of Case

D3 – U4
D2 – U3
D4 – U5
D1 – U2
D5 – U6
D0 – U1
D6 – U7
D7 – U8

Front of Case



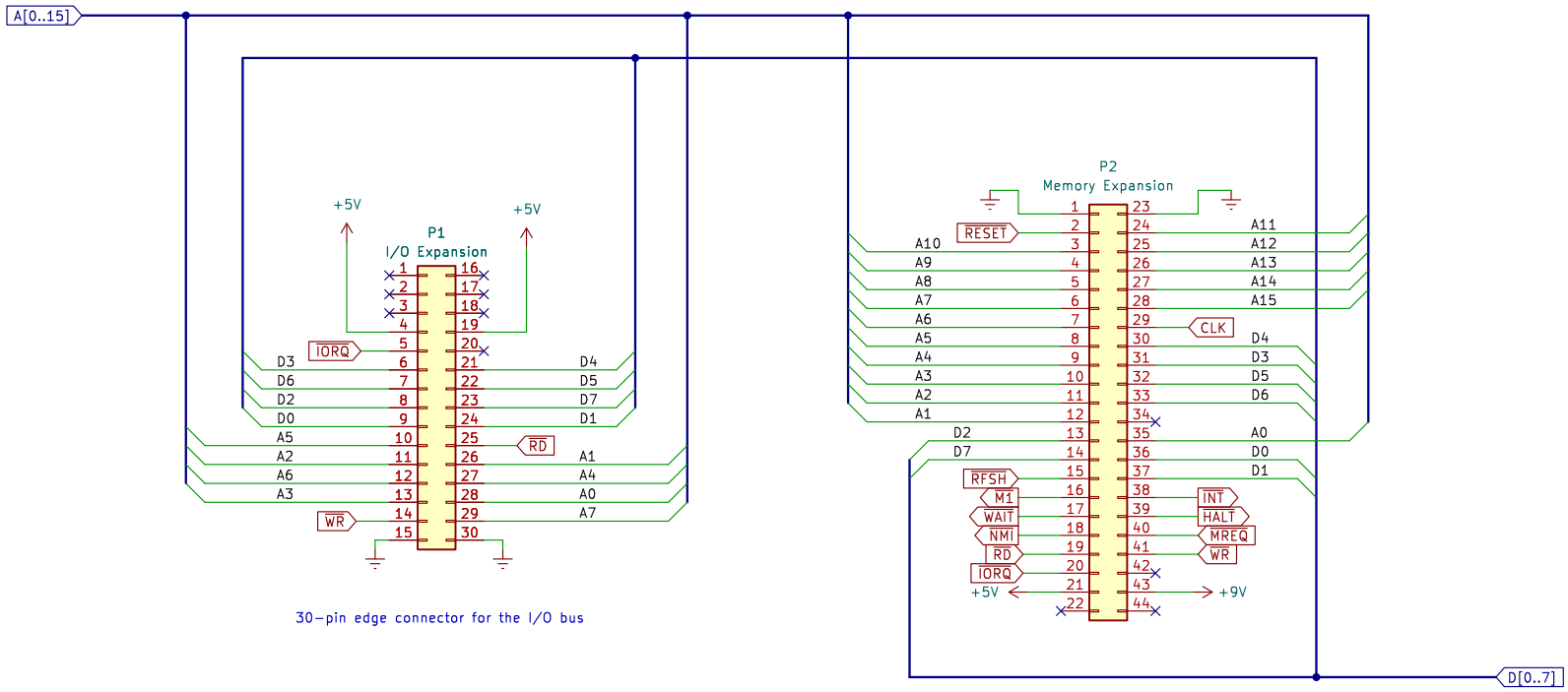
Program RAM (16K)

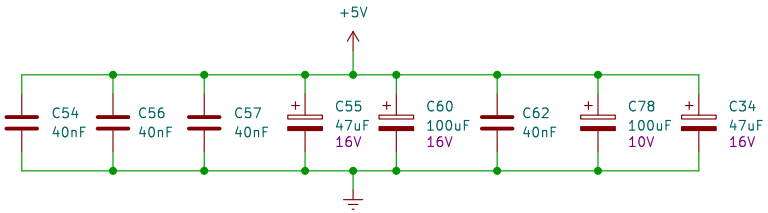
Schematic Redrawn by Rhys Weatherley

Sheet: /Program RAM/
File: program_ram.kicad_sch

Title: VZ300 Computer

Size: A4	Date: 1985	**Rev: 1**
KiCad E.D.A. kicad 7.0.10−7.0.10~ubuntu22.04.1		Id: 3/7





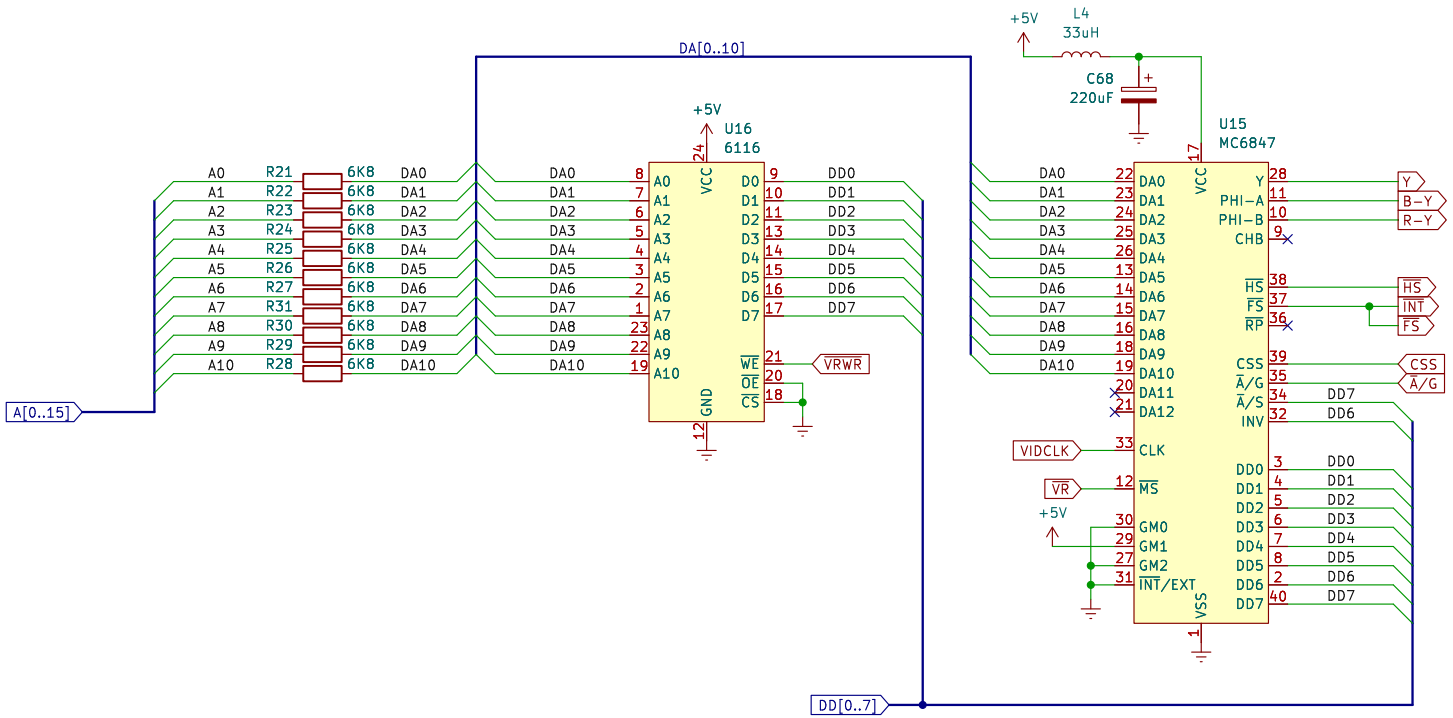
Expansion Ports

Schematic Redrawn by Rhys Weatherley

Sheet: /Expansion Ports/
File: expansion_ports.kicad_sch

Title: VZ300 Computer

Size: A4	Date: 1985	**Rev: 1**
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1		Id: 4/7



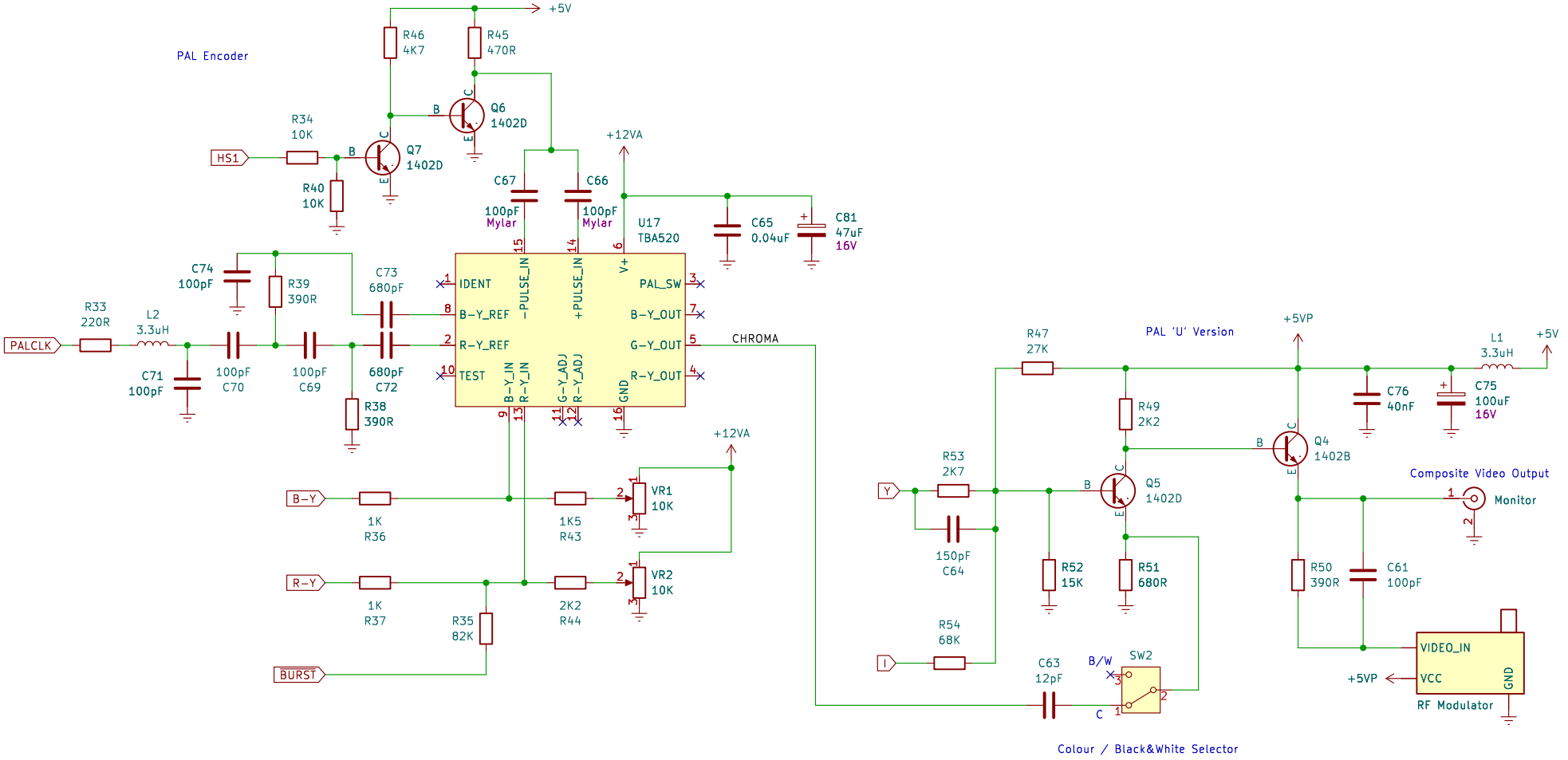
Video Display Generator and 2K of Display RAM

Schematic Redrawn by Rhys Weatherley

Sheet: /Video Controller/
File: video_controller.kicad_sch

Title: VZ300 Computer

Size: A4	Date: 1985	**Rev: 1**
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1		Id: 5/7



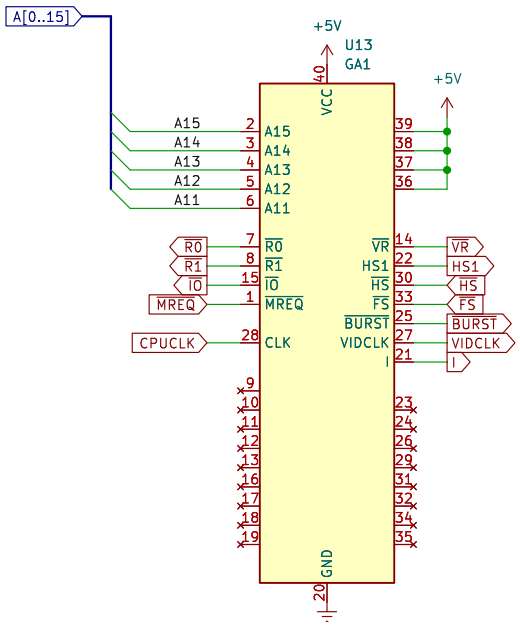
Composite and RF Video Output

Schematic Redrawn by Rhys Weatherley

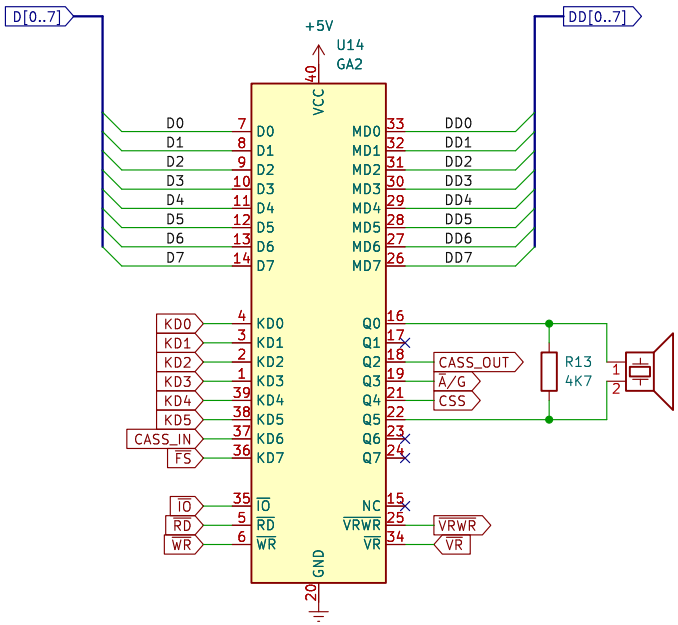
Sheet: /Video Output/
File: video_output.kicad_sch

Title: VZ300 Computer

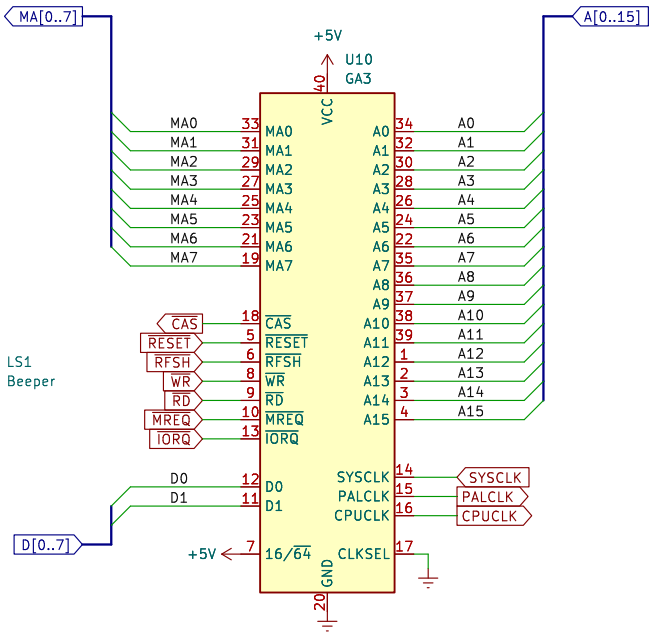
Size: A4	Date: 1985	**Rev: 1**
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1		Id: 6/7



Decode Main Memory Map and
Video Clock Generation



Video Memory Access and I/O



Clock Generation and
Dynamic RAM Management

Gate Arrays

Schematic Redrawn by Rhys Weatherley

Sheet: /Gate Arrays/
File: gate arrays.kicad_sch

Title: VZ300 Computer

Size: A4	Date: 1985	**Rev: 1**
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1		Id: 7/7