

Input and Output

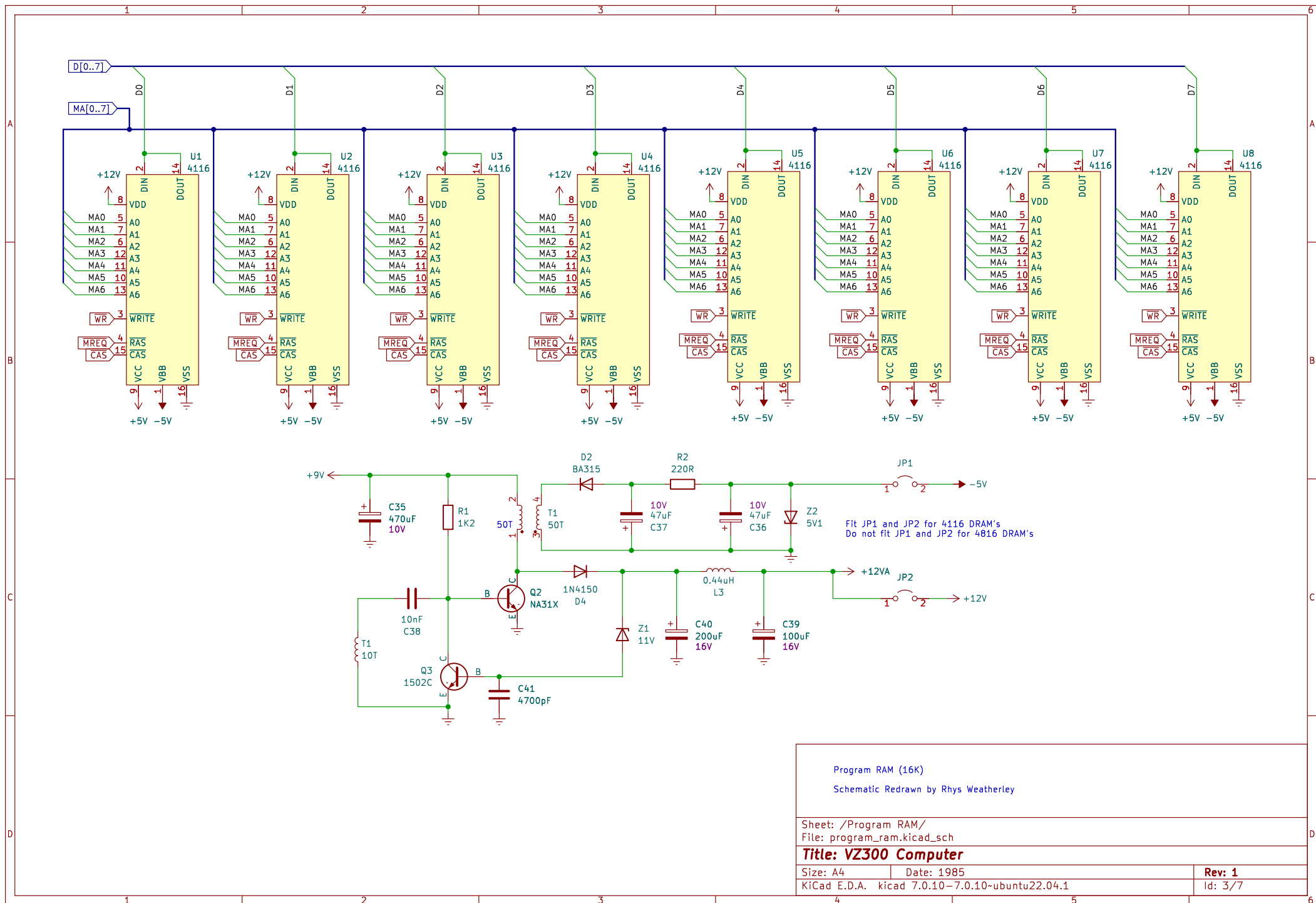
Schematic Redrawn by Rhys Weatherley

Sheet: /Input and Output/  
File: input\_and\_output.kicad\_sch

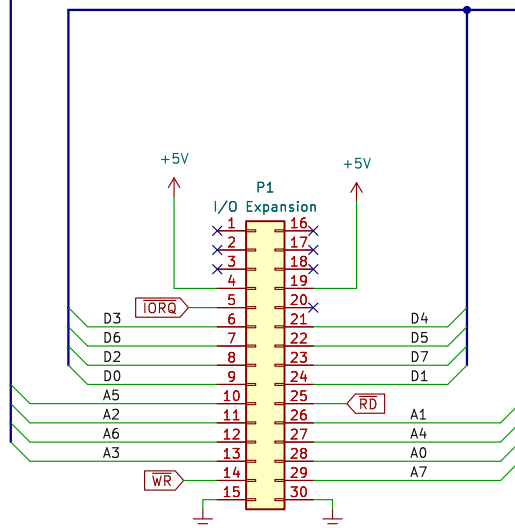
**Title: VZ300 Computer**

Size: A4 Date: 1985  
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

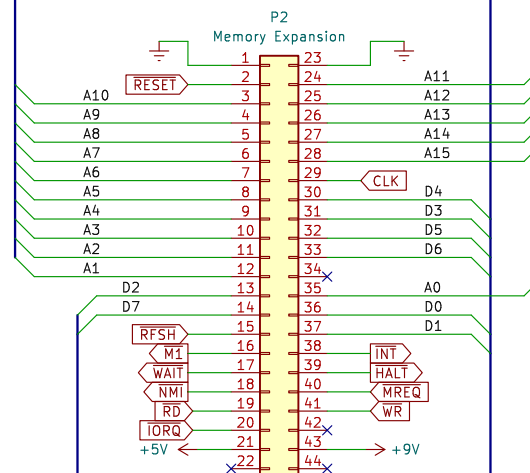
Rev: 1  
Id: 2/7



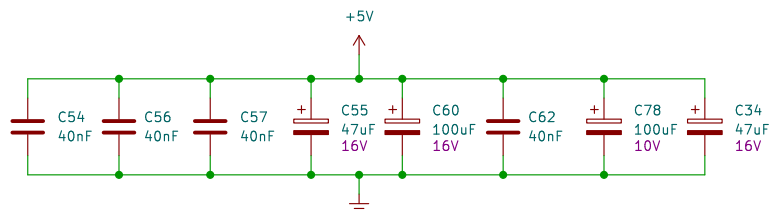
A[0..15]



30-pin edge connector for the I/O bus



44-pin edge connector for the memory bus



Expansion Ports

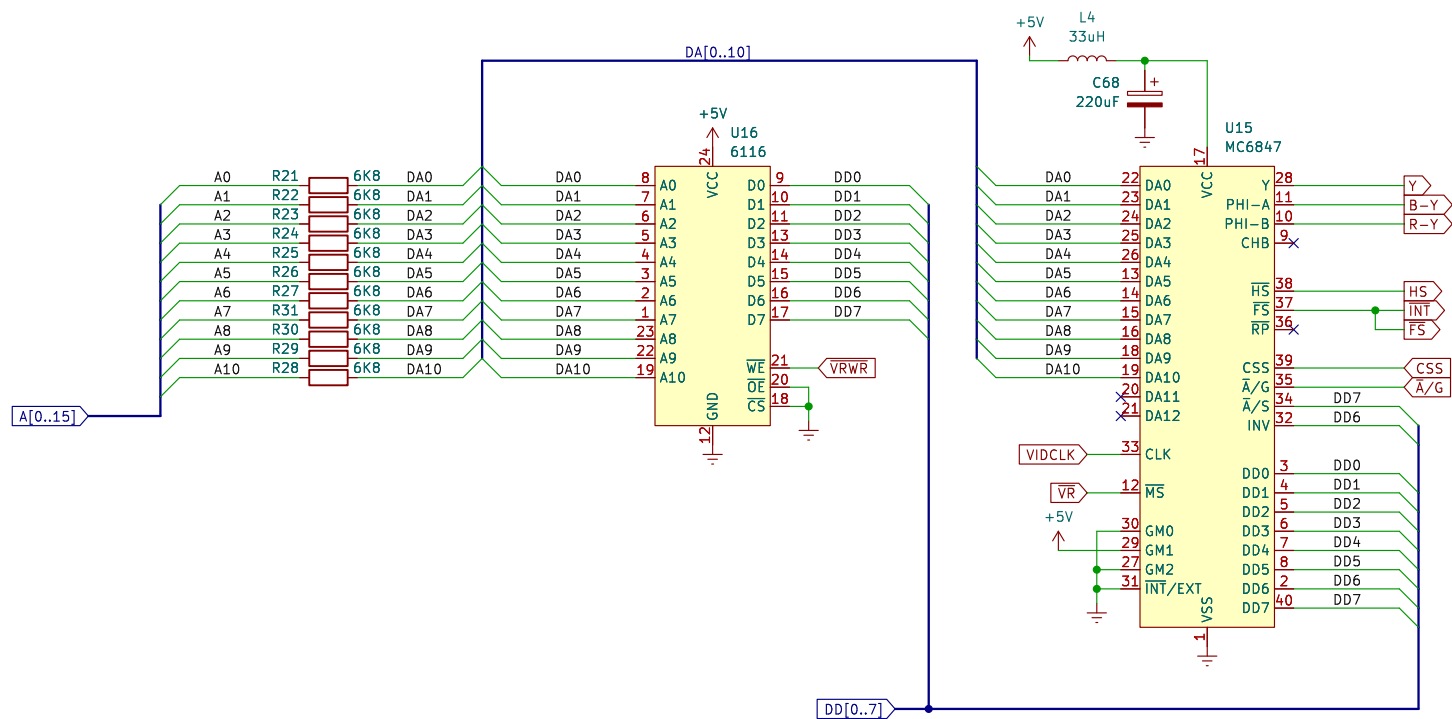
Schematic Redrawn by Rhys Weatherley

Sheet: /Expansion Ports/  
File: expansion\_ports.kicad\_sch

**Title: VZ300 Computer**

Size: A4 Date: 1985  
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

**Rev: 1**  
Id: 4/7



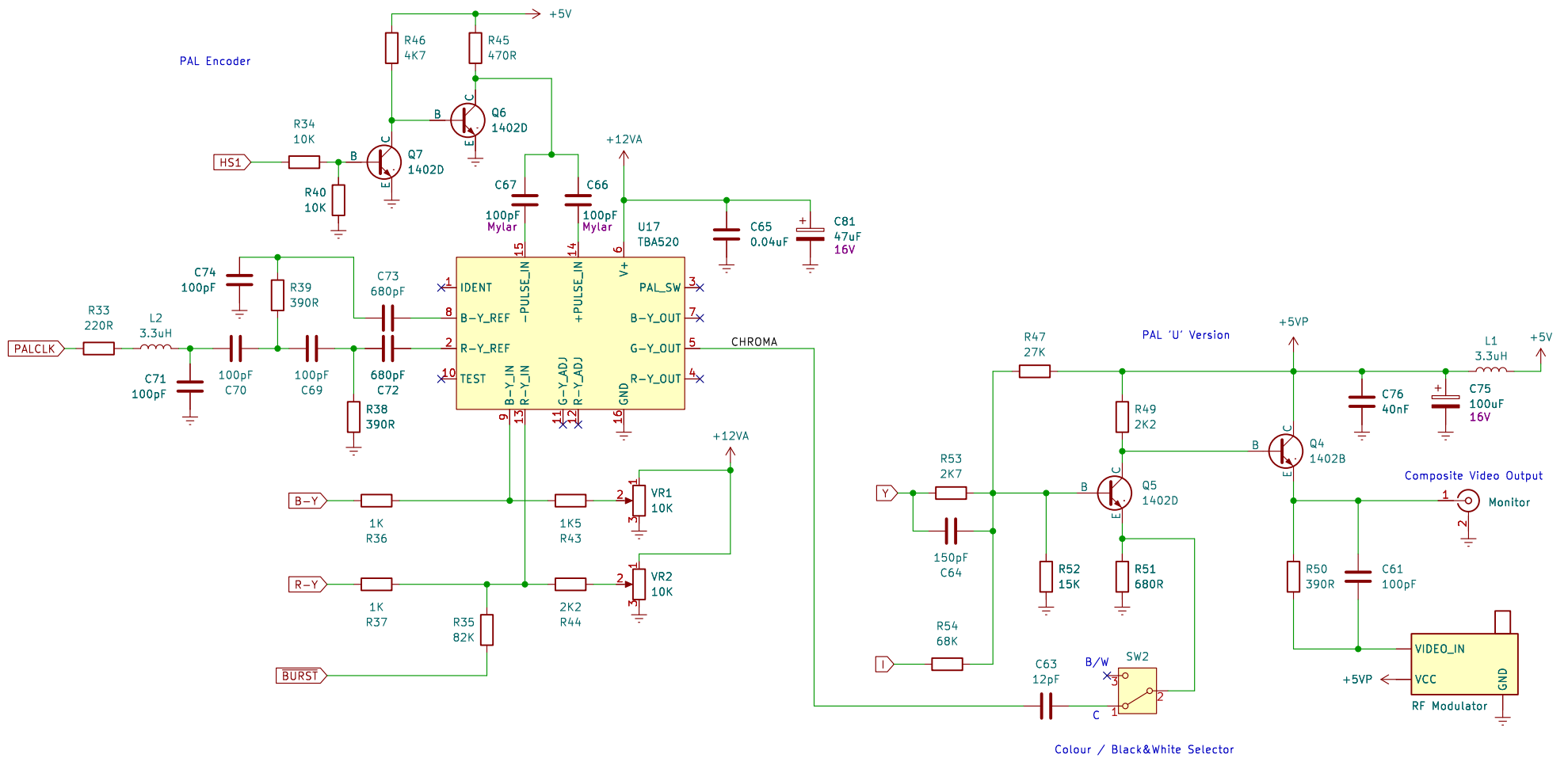
Video Display Generator and 2K of Display RAM  
Schematic Redrawn by Rhys Weatherley

Sheet: /Video Controller/  
File: video\_controller.kicad\_sch

**Title: VZ300 Computer**

Size: A4 Date: 1985  
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

Rev: 1  
Id: 5/7



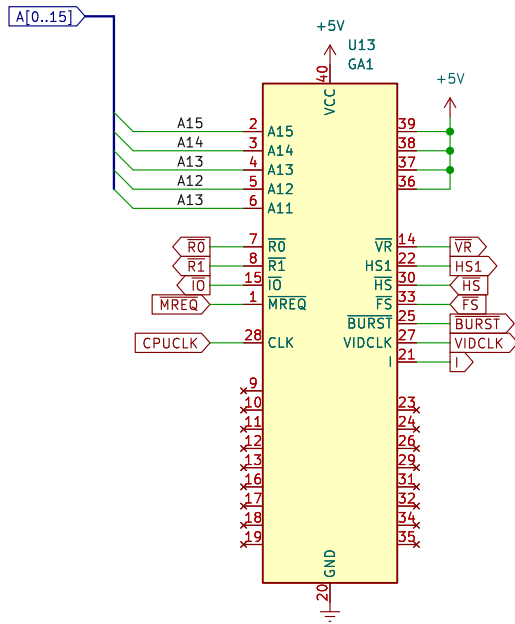
Composite and RF Video Output  
Schematic Redrawn by Rhys Weatherley

Sheet: /Video Output/  
File: video\_output.kicad\_sch

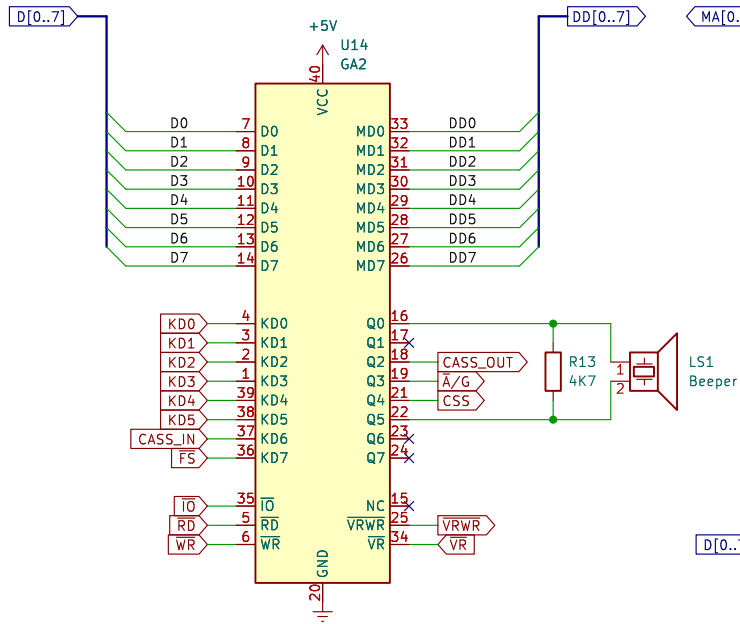
**Title: VZ300 Computer**

Size: A4 Date: 1985  
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

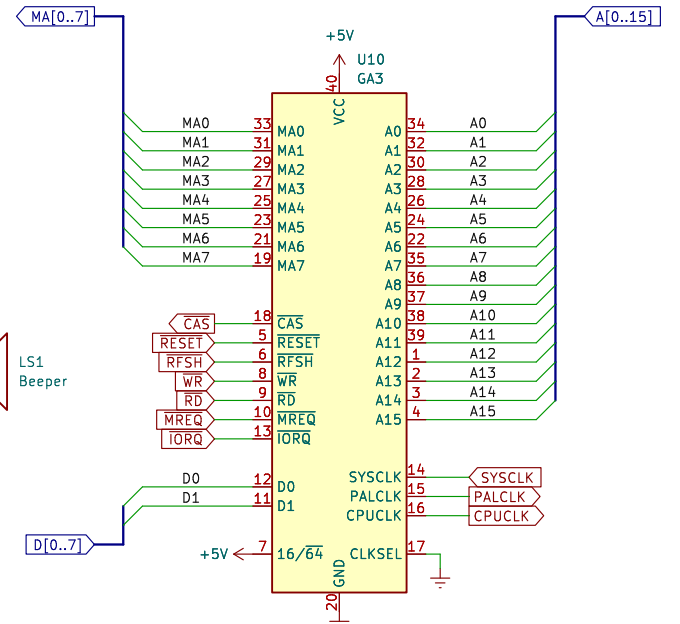
**Rev: 1**  
Id: 6/7



Decode Main Memory Map and  
Video Clock Generation



Video Memory Access and I/O



Clock Generation and  
Dynamic RAM Management

Gate Arrays

Schematic Redrawn by Rhys Weatherley

Sheet: /Gate Arrays/  
File: gate\_arrays.kicad\_sch

**Title: VZ300 Computer**

Size: A4 Date: 1985  
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

**Rev: 1**  
Id: 7/7