Lab 6

Field Effect Transistor (FET)

REFERENCE: Horowitz and Hill Chapter 6

EQUIPMENT

Prototyping board	
Oscilloscope	
Function generator	
Digital Multimeter	
JFET Transistor (2)	2N5457 or equivalent
Depletion MOSFET	*****
Enhancement MOSFET (2)	*****
Resistors	330 , 3.3 k, 1M
Capacitors	0.2 μF, 10 μF electrolytic
Potentiometer	200 with wires soldered on

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INTRODUCTION

Field effect transistors (FET's) come in two main types: junction (JFET) and metal-oxide-semiconductor (MOSFET). These transistors operate on a different principle than the junction transistor. Today, FET's are used mainly within integrated circuits (IC's). Uses for FET's as discrete devices are limited mainly to MOSFET power switches, JFET current diodes, and JFET variable resistors.

The JFET is essentially a cylinder of semiconductor (channel) girded about its center with a belt of opposite semiconducting material (gate - see Figure 6-1). Both N-channel and P-channel JFET's are available (Figure 6-2). The device is operated with the gate-source junction reverse biased, and the electric field at the junction controls the flow of current between the drain and source electrodes at opposite ends of the bar.

The channel of the MOSFET (Figure 6-3) can also be either N- or P-type. In this case, however, the channel is imbedded in a substrate of opposite semiconducting material, which is kept reverse biased. The gate of a MOSFET is actually insulated from the drain-source channel.

There are two kinds of MOSFET's - depletion and enhancement (Figure 6-4). In the former the channel is continuous across the gate region while in the latter the channel is broken at the gate region. The depletion MOSFET is similar in operation to a JFET, whereas there must be a voltage on the gate to complete the channel of the enhancement MOSFET. Both JFET's and MOSFET's have a high input impedance, which is a definite advantage over bipolar transistors. Also, MOSFET's can be used in matched pairs (these days monolithically) to form CMOS digital switches. These have very low power drain and have become the circuit of choice among digital designers because the low power permits high-density circuits.

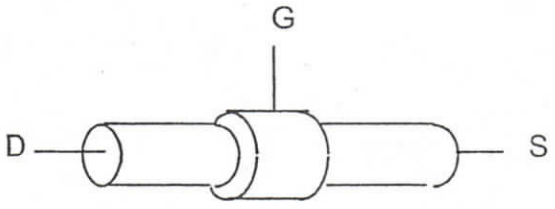

Figure 6-1

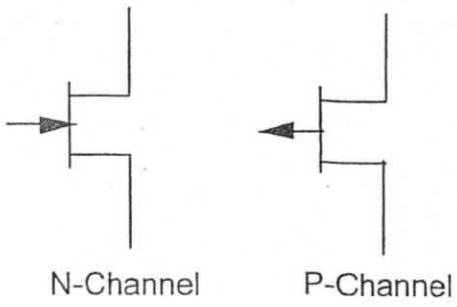

Figure 6-2

In this lab we will consider the properties of amplifier circuits employing both types of FET's.

a. Depletion Type

b. Enhancement Type

Figure 6-3

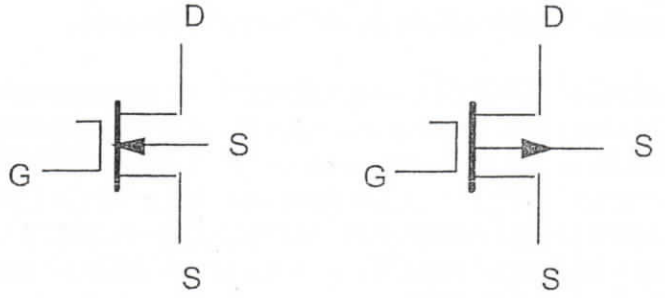

Figure 6-4

PROCEDURE

1. Multimeter check of FET

❝ Using an ohmmeter, it is possible to determine which lead is the gate and whether an unknown type is a P-channel or N-channel FET. This test can also tell whether an FET is good or not.

(a) Identify Gate (G)

☛ Since the gate-channel (D or S) junction is a diode, pick a pair of leads and see if they conduct one way and not the other. If touching your finger to the third lead affects the measurement, the third lead is the gate. If not, choosing another pair will eliminate either the gate or a channel connection. The forward biased gate resistance will be ≈ 1 k. If there is no conduction in either direction the device is a MOSFET.

✍ Sketch your result.

(b) N-channel or P-channel

☛ Use your oscilloscope to determine which leads of the ohmmeter are (+) and (-). Recall that a diode conducts when the P-type material is (+) and the N-type is (-).

✍ Sketch your result.

2. Basic depletion type amplifier (JFET or MOSFET)

❝ In this section the basics of amplifier circuits using field effect transistors will be explored. A basic common source amplifier using a JFET is shown in Figure 6-5. One big advantage of a depletion type FET besides the high input impedance is self-biasing, which allows the elimination of the bias network in the gate circuit. Self-biasing is achieved by the bypassed source resistor, which through the drain-source current reverse biases the gate relative to the source. The circuit shown uses an N-channel JFET, so the proper reverse biasing of the gate is produced by the positive voltage on the source from the voltage drop across the source resistor. Bypassing this resistor maintains a DC level on the source. A P-channel device operates similarly but with a negative drain supply voltage.

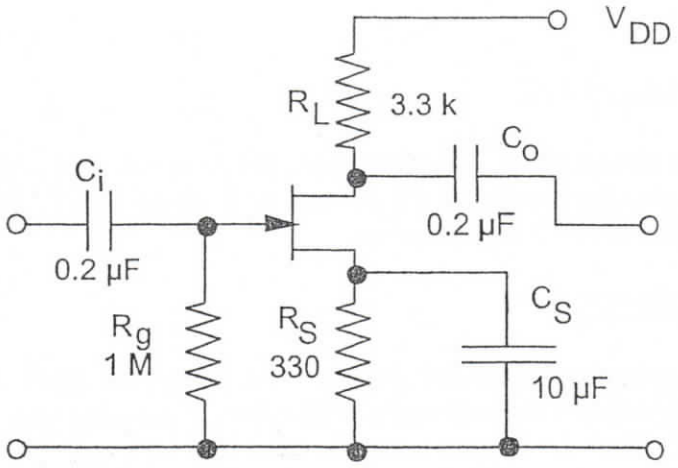

Figure 6-5

(a) Amplifier impedance measurement

☞ ✍ Measure the input and output impedance of the JFET amplifier using the methods of Lab 4. The purpose of R_g is to allow static accumulations of charge on the gate to bleed off. Remove R_g and re-measure the input impedance. Replace R_g and measure the input-output phase shift.

(b) Amplifier gain measurement

☞ ✍ Measure the voltage gain. Look at the signal on the drain (D). Record how the DC level changes with changing R_S. The nominal R_L and R_S values might not be right for your particular FET as FET's show unit-to-unit variations. With your best values of R_L and R_S sketch the load line and Q-point (quiescent or operating point). Show your calculations.

(c) Zero Bias Operation

❝ Correct bias can often be attained with $R_S = 0$. Lowering R_L can return the drain-source voltage to the original Q-point but with a higher drain current.

(i) gain and impedance

☛ ✍ Short out R_S and C_S and lower R_L to ≈ 1.5 k. Measure the gain and impedances.

(ii) load line

☛ ✍ Sketch your new load line and Q-point on the diagram you drew for Part (b).

3. Enhancement MOSFET circuit.

❝ Since the channel is cut in the enhancement MOSFET, the Q-point must be set by having a voltage on the gate that will connect the channel (turn on the device). The gate voltage that will do this is analogous to forward biasing a junction, which means self-biasing will not work (why). In this case fixed bias is again necessary (Figure 6-6).

(a) Biasing resistors

☛ ✍ Calculate the values of the biasing resistors R_1 and R_2.

(b,c) Impedance and gain

☛ ✍ Repeat the measurements of Parts 2a and 2b.

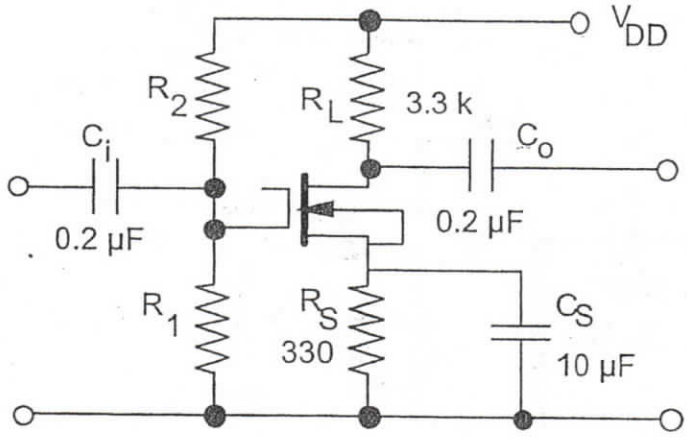

Figure 6-6

4. Active Load High Gain Amplifier.

" Although their high input impedance makes them very useful, a major drawback of FET's is their low gain. One obvious way to compensate for this is to use multiple stages. Another possibility, which we will explore here (Figure 6-7) is to replace the drain load resistor with a current source (active load). This enables one to have a very high effective AC load resistance while still remaining within the operating region of the MOSFET.

The variable source resistor R_S in Figure6-7 balances the drain current for maximum gain. You will find the circuit works differently when the FET's are interchanged. This amplifier has high temperature stability and low noise.

(a) Amplifier Impedance Measurement

☞ ✍ Measure the input &output impedances. Is the input-output phase shift the same as in Part 2?

(b) Amplifier Gain Measurement

(i) gain

☞ ✍ Measure the voltage gain.

(ii) sensitivity to power supply voltage

☞ ✍ Vary the power supply voltage. How is the gain affected? Be specific.

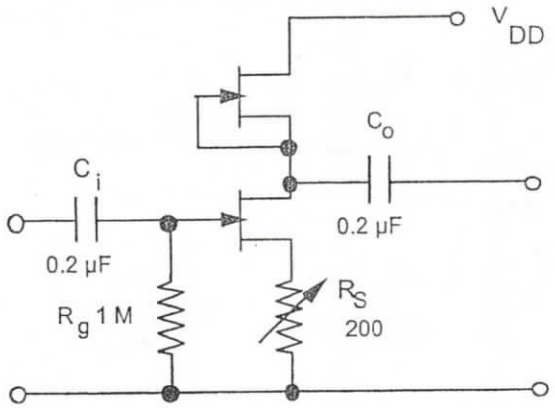

Figure 6-7