

VERIFICATION OF DIGITAL CIRCUITS USING JAVA

02125 BACHELOR PROJECT

by

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Draft

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1 SUMMARY

This section summarises the sections of the report.

Section 2 surmises UVM and some chosen chip verification frameworks, pivoting towards the motivation for, and introduction of, this project.

Section 3 breaks down the project into challenges and discusses solutions to these challenges.

Section 4 goes through the design considerations along with diagrams outlining the projects intended structure.

Section 5 describes the implementation and shows solutions of interest.

Section 6 explains the testing used during the project as well as discusses the usage of the program.

Section 7 summarises the project and discusses the results.

2 INTRODUCTION

Related works

In the world of designing integrated systems on chips, it is crucial to describe these in some hardware description language in order to test designs before actual manufacturing. Part of testing these designs include writing tests in some framework supporting some abstraction and then simulate the chip using the applied framework, a process known as *verification*. One verifies the *Device Under Test* or DUT. One of the most common methodologies is *Universal Verification Methodology*, or simply UVM.

2.1. THE UVM METHODOLOGY

Using UVM, one have to built testbench components. These include e.g. drivers for converting tests into proper DUT stimulus, monitors for reading the state of the DUT and scoreboards for comparing expected behaviour to actual behaviour, etc. UVM has the great benefit, that once these components have been defined, they can be reused within the scope of some system of designs. This means a high overhead, with high reusability.

2.2. CURRENT VERIFICATION TOOLS

In today's landscape a myriad of verification tools exists. Projects like Chisel¹, and it's forked project SpinalHDL² discards the traditional hardware description languages and testbenches altogether and implements their own, and pyuvvm³ takes UVM into python using cocotb⁴ as a backend driver. These tools do however have some problems. Chisel and SpinalHDL requires developers to learn a new description language, which means the communities of developers are small, increasing slowly. pyuvvm uses Python which itself is an interpreted language, meaning its runtime resource requirements do not scale well on large projects.

2.3. THE CASE AGAINST UVM AND THE MIGHTY ABV

Chip verification is inherently done by hardware designers and engineers and UVM is inherently created by and for hardware designers. When software engineers verify their software, they use unit tests and assertions along with formal proofs. In recent years these approaches have been adopted by hardware designers. *Assertion Based Verification*, or ABV, along with formal verification is increasingly being applied to complex computing chip design verification and increases performance metrics over classic UVM[2]. Key impacts from this paper is summarised on Table 1.

Table 1: Key impact of formal verification adoption over UVM[2]

Verification cycles reduced by 25-30%
Pre-silicon bug detection rates improved by 20%
Security vulnerability detection increased by 40%

¹On GitHub: github.com/chipsalliance/chisel

²On GitHub: github.com/SpinalHDL/SpinalHDL

³On GitHub: github.com/pyuvvm/pyuvvm

⁴cocotb on the web: www.cocotb.org/

SystemVerilog Assertions, or SVA has been defined in IEEE 1800-2023[1, Chapter 16] meaning ABV is already a part of the SystemVerilog syntax.

2.4. THE GOAL OF THIS PROJECT

The goal of this project is a framework written in a strongly typed language, supporting SystemVerilog and core ideas from ABV, thus making it easy for designers to write their designs in SystemVerilog and use a well known language to implement assertion based tests.

Introducing *SteelBrew*, the chip verification framework written in Java.

3 PROBLEM SPECIFICATION AND ANALYSIS

As mentioned in Section 2 this project aims to implement a testing framework for SystemVerilog designs, using core ideas of Assertion Based Verification, written in Java. This poses the following challenges:

- **Simulation driver:** The framework needs to communicate with some simulation driver.
- **Peek-poke-step:** Signal manipulation needs to be implemented to set up and carry out assertion of behaviour.
- **Assertion-logic:** ABV logic has to be implemented in the framework.
- **Test translation:** The framework has to translate test logic from Java to SystemVerilog and create a testbench for test simulation.
- **Coroutines/concurrency:** As assertions can be time-invariant, it makes sense to implement concurrency or coroutines to efficiently execute the simulation.

3.1. SIMULATION DRIVER

Driving the simulations is not part of the scope of this project. Instead, the simulations are run by a third-party tool using Java to invoke the tool and listen for the results. Verilator⁵ is a fast and community-driven simulator for SystemVerilog, which supports SVA directives. Through testbenches it is possible to set up and test DUT's fairly easily.

3.2. PEEK-POKE-STEP

Using the Java `BigInt` class, some logic for manipulating bits needs to be implemented in order to set up tests. `BigInt` enables describing integers in other bases, as is common in hardware design or low-level programming.

3.3. ASSERTION-LOGIC

There are some assertion directives of interest:

1. `Assert` which raises an exception if some property does not hold.
2. `Cover` which monitors the coverage of some property.

These are the minimum that should be implemented. Some object for a test should be created and react if the driver raises an exception pertaining to the used directive. The logic in the framework needs to adhere to the logic stated in the SVA documentation.

3.4. TEST TRANSLATION

Manipulation and assertions has to be properly translated into a testbench that, when run, carries out the verification. This should be done in a manner that translates the test logic into a series of strings that are placed correctly within a testbench.

3.5. COROUTINES/CONCURRENCY

To optimise runtime, it is desirable to run tests concurrently. For this purpose there are two options:

1. Java `Runnable`
2. Coroutines

⁵Verilator on the web: veripool.org/verilator

3.5.1. Java Runnable The Java Runnable interface⁶ enables thread creation and joining. Benefits include the native support for Java and the documentation and community surrounding developing with Runnable. The main disadvantage is that threads rely on the operating system's scheduler, thus removing some degree of control during execution, and in the worst case, if not run in an elevated mode, threads might not get priority to run.

3.5.2. Coroutines Coroutines are described as "light threads" and enables a thread to control its own behaviour. This means threads can execute with a high degree of control. Disadvantages is that Java does not natively support coroutines. Solutions include hacking the JVM or using third party projects to execute coroutines. One such example is Javaflow⁷ from Apache Commons or an interesting project called "Coroutines"⁸ inspired by Javaflow.

3.6. GOALS AND SUCCESS CRITERIA

The discussed challenges and their solutions are listed on Table 2.

Table 2: The projects challenges and success criteria

#	Challenge	Success Criteria
1	Simulation driver	Logic that launches Verilator and handles communication with the processes.
2	Peek-poke-step	Logic that, using BigInt, manipulates wires and ports in the tests.
3	Assertion-logic	Logic that sets up assertion directives supported by the driver and SVA to support ABV
4	Test-translation	Logic that translates the written test into a testbench that when executed, ensures the tests are carried out correctly.
5	Coroutines/concurrency	Implementation of concurrent execution of the simulations.

SteelBrew will be developed in an Agile way, based on use-cases. This ensures that a viable product is ready after dealing with challenge 1, 2 and 4 as these deals with setting up basic test functionality. Afterwards assertion logic, concluding with coroutines.

4 DESIGN

The design of SteelBrew will take an Agile approach to get going with some framework for writing and running simple tests on devices written in SystemVerilog, using Java.

4.1. USE CASES

Using SteelBrew should be as simple as possible. Fig. 1 shows an overview of the use cases for a developer. This is a simplification. As mentioned the framework is executed in Java, so to get started the user would start by creating a java project and importing SteelBrew. Hereafter the DUT is added and tests are defined and configured. A command should then execute the test and start the simulation.

4.1.1. Adding the device under test With the device design in the root folder, adding it to the framework should be as easy as adding the device to some object that handles device configuration. The underlying logic should take care of the rest.

4.1.2. Adding tests Since the tests are linked to some device, it is preferred that the same underlying logic ties tests and devices.

4.1.3. Configure tests This is the bulk of the interaction for the user. With some object carrying the tests and device, the user should be able to easily add new tests or assertions with some easy to use method calls. The underlying logic should resolve conflicts and handle test creation without the user getting much involved.

⁶Documentation on Oracle: docs.oracle.com/javase/8/docs/api/java/lang/Runnable.html

⁷Javaflow on Apache: commons.apache.org/sandbox/commons-javaflow/

⁸Coroutines on GitHub: github.com/offbynull/coroutines

Figure 1: Use case diagram for SteelBrew

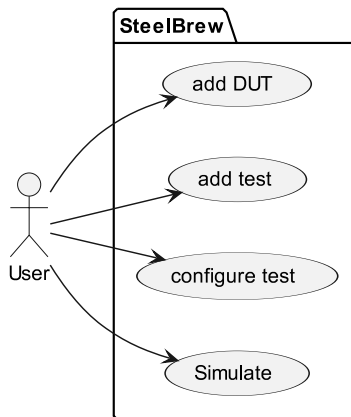
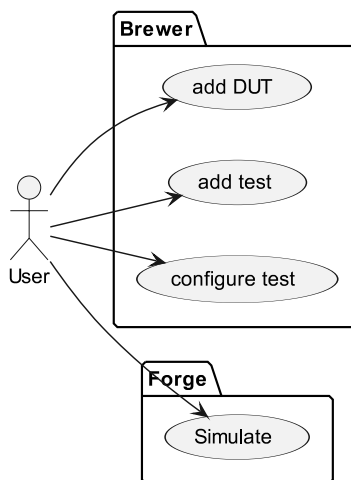


Figure 2: The expanded use case diagram for SteelBrew



4.1.4. Simulate Since the simulations are carried out by a third-party program, all handling between SteelBrew and said program, should be handled by yet another class, separate from the test-driven class. This ensures good separation of responsibility in the project.

4.2. SEPARATION OF RESPONSIBILITY

The project is considered two-fold:

1. Handling DUT's and tests
2. Handling concurrency and third-party software

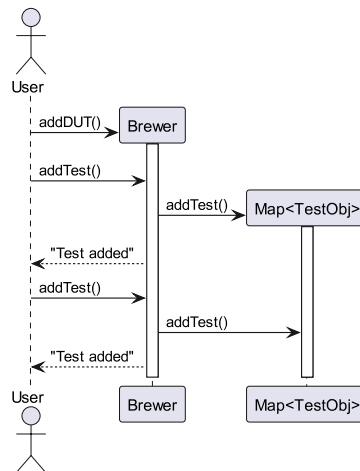
For this reason the program has to contain two main components. The *Brewer* and the *Forge*. A third class is introduced as the entry-point for the program, and will be accessible to all other classes. This class is simply *SteelBrew*. Expanding on Fig. 1, the use case diagram is expanded as seen on Fig. 2.

4.3. THE BREWER

The *Brewer* is the primary interface. There are several ways of going about this object handling multiple DUT's and tests. One aspect could be to hold Lists or Maps of the tests and devices, and then use methods to get these, and couple them accordingly. This has the advantage that from a schematic point of view it simplifies the program. However, once tests are applied to different devices, all contained within the same object, one has to keep track of internal links. The first major decision in the design phase was as such:

1. Give a *Brewer* to each DUT
2. Assign tests to each *Brewer*

Figure 3: Sequence diagram showing the idea behind the Brewer



This means more objects are created, but the Brewer object itself has a lot less responsibility in terms of tracking the internal links.

A sequence diagram on Fig. 3 shows this initial idea.

4.4. THE FORGE

The Brewers complement, the Forge handles another job, entirely. This class has to handle the responsibility of taking the tests from the Brewers and hand them down to the third-party tool. This prompts some considerations, namely how to launch other programs with very specific parameters and how to communicate with these programs.

4.4.1. Verilator and the Forge The third-party software chosen is Verilator. It is open-source and very quick at executing simulations. Verilator works like this:

1. The user prepares testbenches describing the testing environment and the tests
2. Verilator takes the testbench and some DUT as input and makes the files for compiling a C++ program
3. Compiling and running the program executes the tests and outputs a waveform-file, which can be inspected by e.g. GTKWave.⁹

This puts constraints on the design of the program. The Forge needs to call Verilator multiple times and then needs to run the compiled program. To ease this, the program creates a Makefile and executes through this. Simple redirects of stdout means that the Forge can collect the output from Verilator and the simulation.

4.4.2. Concurrency Up until now the main idea was to take a Brewer pointing to a DUT, add some tests and then hand it off to the Forge for Verilating, compiling and running the simulation. This poses one issue: This way of evaluating the program means that tests can only be parallelised in terms of Verilator's internal multithreading, and then one DUT with all its test per thread. Verilator's internal multithreading is outside the scope of this project, so the only option is to get creative with the way tests are run. Normally when using Verilator, one testbench with all testing is run per DUT. The design choice here was to split up the tests, such that each test, or set of tests, gets its own testbench and its own compiled program. This way tests can be carried out in parallel by launching each workflow on different threads.

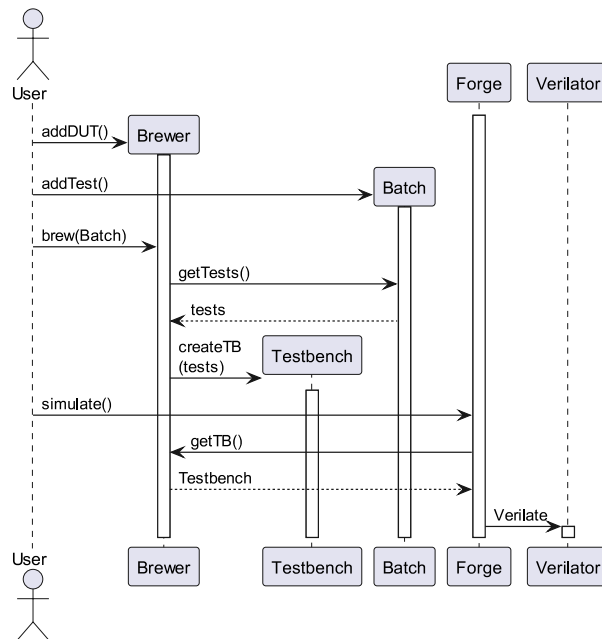
4.4.3. Coroutines It was of great interest to involve coroutines in the project. Java does not support coroutines natively, so workarounds were investigated. To this end, it turns out most coroutine frameworks and plugins are 6+ years old. They do not support newer Java versions, and thus not newer Java functionality. The design choice here was to use threads to execute tests.

4.5. TESTBENCH

The workflow of Verilator and the design choice of splitting up tests into separate executables meant that the definition of tests were somewhat straightforward. The Brewer would have Testbench objects. Whenever tests are defined they are added to this object, and just before simulation, testbench files are created based on the content of the object. The testbenches have to have unique names, otherwise the Verilator executable and GNU Make will be unable to execute the correct benches.

⁹GTKWave on the web: gtkwave.sourceforge.net

Figure 4: Final workflow example as a sequence diagram



4.6. BATCH

While the Testbench class is able to contain all tests put in, it is basically a collection of strings. Furthermore, it is often desirable to control the sequence in which tests are executed, as the result from one test might affect the other. Or if one has to test what happens when manipulating signals inside the DUT. A new class is introduced to handle a sequence of tests, along with logic transforming simple methods into cumbersome strings for the testbench. The Batch class keeps a record of signals and tests involved in some scenario and when ready, creates a testbench with these tests executed as they are added by the user. The functionalities here starts with:

- **Peek** Read signal
- **Poke** Change signal
- **Step** Increment DUT clock

4.7. ASSERTIONS

The last leg of the project is assertion support. Assertions is a formal way of ensuring certain properties of a design, either in the scope of its entire execution or in certain scenarios. SystemVerilog has long supported assertions, however Verilator has limited support for assertions. For this reason some core functionality is designed and implemented, namely relations between signals in the DUT, using logic and relational operators.

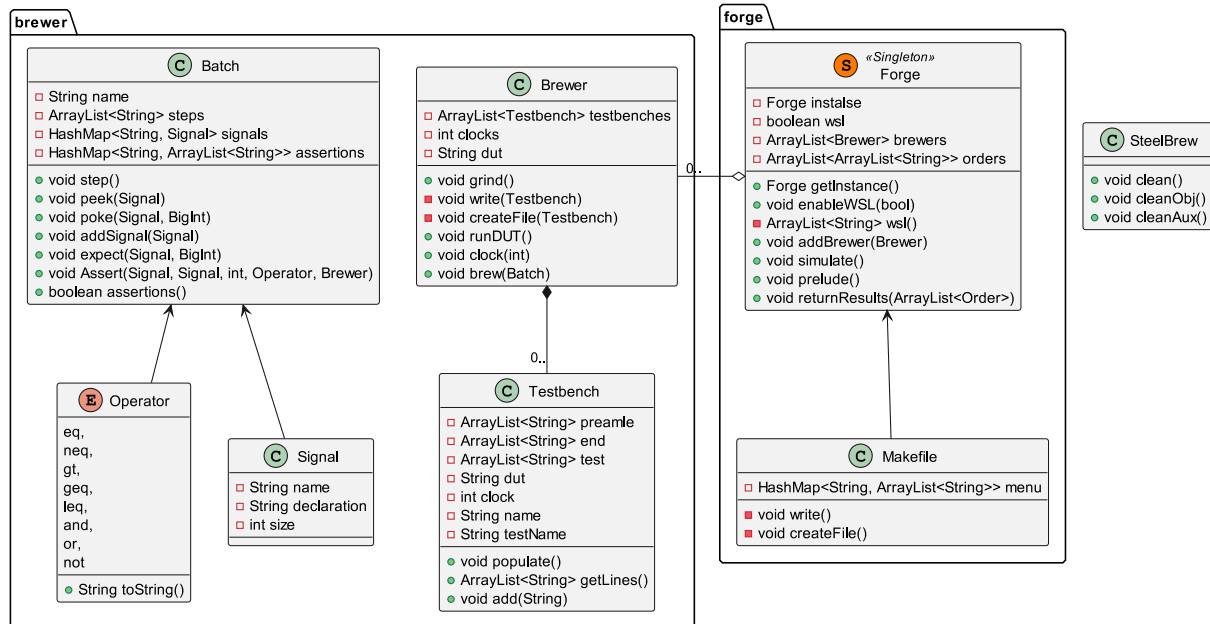
4.8. DESIGN OVERVIEW

The workflow is illustrated by the sequence diagram shown on Fig. 4. The class diagram is shown on Fig. 5. Notice that the Forge is a singleton. This was chosen to make access to the Forge easier and most importantly ensure that only one Forge is instantiated. The Forge handles the executed threads, and multiple instances could lead to race conditions. The Barista class has been omitted from the diagram but will be discussed further in Section 5.

5 IMPLEMENTATION

In this section the practical implementation is showcased and discussed. Each class is briefly summarised, and interesting solutions are shown.

Figure 5: Class diagram showing the structure of SteelBrew



5.1. BUILD ENVIRONMENT

The project exists in a Gradle¹⁰ build environment consisting of an app and a library. The reasoning is simple: This project is developed as a library that the developer can import into their own Java code. The app is a merely a demo of how the library can be used, while the library itself is the project. If the project should be published Gradle will easily publish it to the Maven central repo. The demo app is in the `app` folder and the project is in the `steelbrew` folder. The rootfolder contains two alu written in SystemVerilog to experiment on.

5.2. STEELBREW

This class is the entypoint for the project. It has two purposes. First it instantiates the Forge as a singleton. Second it has auxilary functions for cleaning files produced during simulation.

5.3. BREWER

The brewer class is constructed for each DUT to be tested. Upon construction it adds itself to the Forge. When the user is ready to simulate the Forge calls the `void grind()` method that creates and fills out testbench files. The `void brew(Batch batch)` method shows how a batch of tests are used to create a testbench. The method is shown on Listing 1. Listing 1 illustrates how tests are converted into testbench functions.

5.4. TESTBENCH

The Testbench class holds all of the necessary lines to make a testbench work. The `void add(String string)` method can then be used to add test lines to the testbench. The Brewer then assembles the file. Listing 2 shows how the testbench names are assigned. When a testbench is created the variable `testName` combines the name of the DUT, with the name of the test.

5.5. BATCH

The Batch class defines the test methods `step()`, `peek()`, `poke()`, `expect()` and `Assert()`. The peek method is interesting here, as it writes to stdout with its result. This can be seen on Listing 3. The assert method is also of interest. It takes two signals and an operator and then constructs a C++ method, that looks for some comparison, depending on the chosen operator. In Listing 1 the assertions are put into a testbench. The values of the assertion hashmap contains

¹⁰Gradle on the web: gradle.org

Listing 1: Brewers brew method for creating a testbench from a batch of tests

```

1 public void brew(Batch batch) {
2     Testbench testbench = new Testbench(dut, batch.getName(), clocks);
3     if (batch.assertions()) {
4         HashMap<String, ArrayList<String>> assertions = batch.getAssertions();
5         Set<String> functions = assertions.keySet();
6         functions.forEach(f -> assertions.get(f).forEach(s -> testbench.add(s)));
7         testbench.add("    while (sim_time < MAX_SIM_TIME) {\n");
8         testbench.add("        dut->clk ^= 1;\n");
9         testbench.add("        dut->eval();\n");
10        testbench.add("        if(dut->clk == 1){\n");
11        testbench.add("            posedge_cnt++;\n");
12        testbench.add("        }\n");
13        functions.forEach(f -> testbench.add(f+"\n"));
14        testbench.add("        m_trace->dump(sim_time);\n");
15        testbench.add("        sim_time++;\n");
16        testbench.add("    }\n");
17        testbench.add("\n");
18    }
19    ArrayList<String> steps = batch.getSteps();
20    for (String step : steps) {
21        testbench.add(step);
22    }
23    testbenches.add(testbench);
24 }

```

Listing 2: Example of inserting custom names into the testbench

```

1 preamble.add("int main(int argc, char** argv, char** env) {\n");
2 preamble.add("    V" + testName + " *dut = new V" + testName + ";\n");

```

Listing 3: The peek method

```

1 public void peek(Signal signal) {
2     steps.add("std::cout << \"\n Peek on " + signal.getName() + ": \" << (int)(dut->" + signal.getName()
3         + ") << \" @ simtime: \" << sim_time << std::endl;\n");
4 }

```

the method definition. The key is the function call. In Listing 1 the methods are defined early in the testbench and the call is placed in a loop that evaluates every clock cycle, thus the assertion has to hold throughout the DUT evaluation. The two helper classes Operator and Signal will briefly be explained.

5.5.1. Operator The operator is a Java enum that comprises all the operators for comparison. The enum has a toString() method. If an assertion is added as such, batch.Assert(signal, signal2, 1, Operator.neq, alu); the assert method uses the toString method to convert neq to “!=” when inserted in the C++ method.

5.5.2. Signal The Signal class is a POJO¹¹ that defines the signal with a name, signal size and declaration, when used as a variable in C++.

5.6. MAKEFILE

The Makefile class is used to create a GNU Make makefile to simplify process calls from the Forger. This can be seen on Listing 4. Lines 8-11 gives the test recipe a name, and calls for a waveform creation. 14-26 then recursively goes through the recipes:

1. The waveform depends on the executable
2. The executable depends on the verilaton stamp (an empty file telling Make that verilaton is not necessary on repeated makes)
3. The stamp then depends on verilating the testbench and DUT

¹¹Plain Old Java Object

Listing 4: The write method that creates the recipes for the verification, compilation and execution of simulations

```

1  private void write() {
2      try {
3          FileWriter writer = new FileWriter("Makefile");
4          Set<String> duts = menu.keySet();
5          for (String dut : duts) {
6              ArrayList<String> tests = menu.get(dut);
7              for (String test : tests) {
8                  writer.write(".PHONY: " + test + "\n");
9                  writer.write("\n");
10                 writer.write(test + ": waveform" + test + ".vcd\n");
11                 writer.write("\n");
12             }
13             for (String test : tests) {
14                 writer.write("waveform" + test + ".vcd: ./obj_dir/V" + test + "\n");
15                 writer.write("\t@./obj_dir/V" + test + "\n");
16                 writer.write("\n");
17                 writer.write("./obj_dir/V" + test + ": .stamp." + test + ".verilate\n");
18                 writer.write("\t@echo \"### Building executable ###\"\n");
19                 writer.write("\tmake -C obj_dir -f V" + test + ".mk V" + test + "\n");
20                 writer.write("\n");
21                 writer.write(".stamp." + test + ".verilate: " + dut + ".sv " + "tb_" + test + ".cpp\n");
22                 writer.write("\t@echo \"### VERILATING ###\"\n");
23                 writer.write("\tverilator --trace -cc " + dut + ".sv --exe tb_" + test + ".cpp --prefix V"
24                     + test + "\n");
25                 writer.write("\t@touch .stamp." + test + ".verilate\n");
26                 writer.write("\n");
27             }
28         }
29         writer.write(".PHONY: clean\n");
30         writer.write("clean:\n");
31         writer.write("\t rm -rf .stamp.*;\n");
32         writer.write("\t rm -rf ./obj_dir\n");
33         writer.write("\t rm -rf *.vcd\n");
34         writer.close();
35     } catch (IOException e) {
36         e.printStackTrace();
37     }
38 }

```

5.7. FORGE

The Forge is where processes are handled. It is instantiated as a singleton, which means it is always accessible and only one copy exists, making race-conditions less likely. The constructor also allows for lazy initialisation, meaning it is initialised when the `Forge.getInstance()` method is first called.

Forge has a `ws1()` method that solves the problem that Verilator does not ship binaries for Windows. However if Windows Subsystem for Linux is installed with Verilator, Verilator can be called from a Windows terminal with the command `ws1 -d Ubuntu <Command>`. The Forge executes simulations by calling `prelude()` which prompts the brewers to create testbench files. Afterwards the method creates an instance of Makefile and collects a list of all tests to be executed. The lists contains the command call for the process to start. Forge then constructs an instance of the Barista class, which in turn deals with a multithreaded approach.

5.7.1. Barista The Barista class is a helper class for the Forge class, that creates stringbuilders that in turn executes the “make” command and saves stdout and stderr. Barista runs a test on its own thread, enabling concurrent simulation. Upon completion Barista calls `Forge.returnResults()`, which then prints the output of the tests, thus completing the simulations.

6 TESTING

Insert and describe tests on framework

7 CONCLUSION

Write up conclusion

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