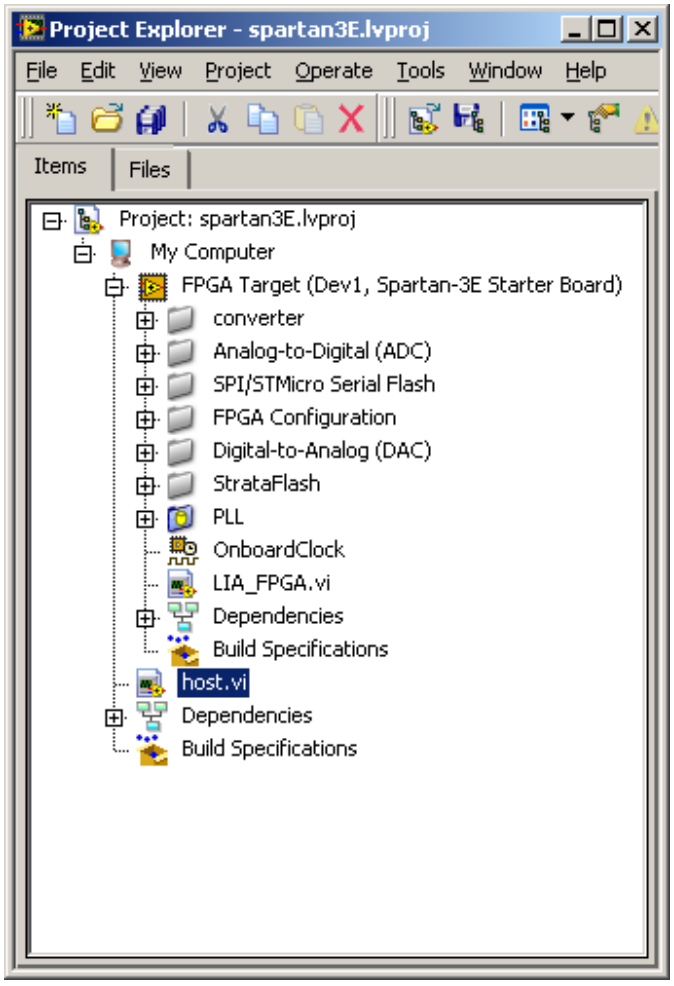
How to setup the Lock in Amplifier FPGA demo for cRIO

Hardware Requirement

1. Spartan3E academic board
2. Signal Generator or other signal source
3. Voltage offset circuit for analog input range

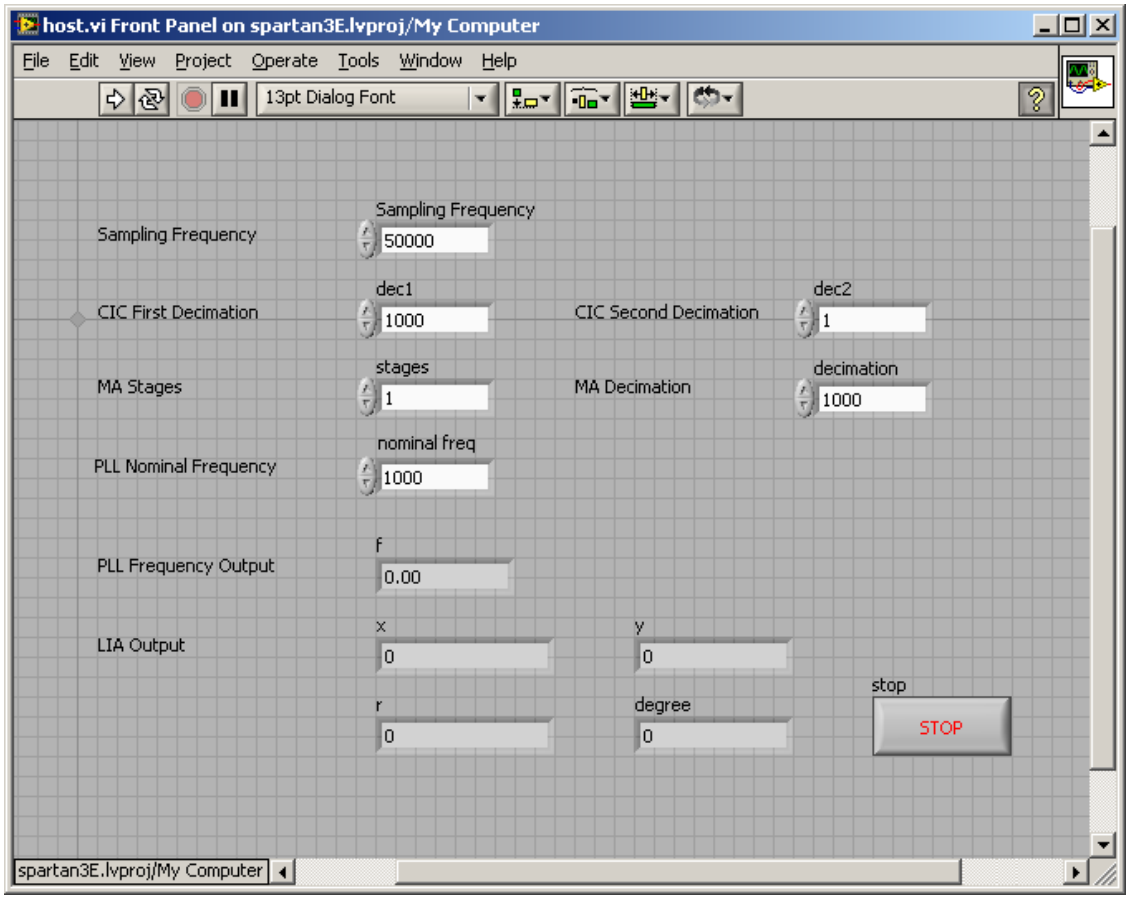
Software Setup

Open LIA.lvproj and you can find the RIO and FPGA target. You can create your own target and move all the VIs and resources to the new target.



The top FPGA VI is **LIA_FPGA.vi**. These are the files that need to be moved if you create your own target.

After the FPGA VI gets compiled, you can run the host VI **host.vi** listed under My Computer target.



There are several settings you can control in the GUI.

1. Sampling Frequency: The sampling frequency of AD converter
2. dec1, dec2: Decimation factor of first and second CIC filter
3. stages, decimation: number of stages (1 or 2) and decimation factor of MA filter
4. nominal freq: Center frequency of PLL as reference

Run the VI and press Start button. It starts to measure the voltage.