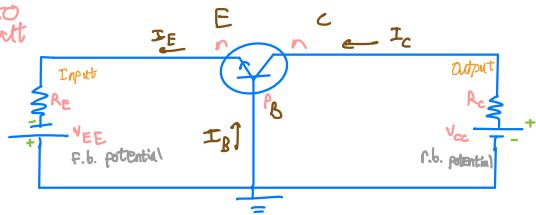


3 different configurations:

- i) common base → base is common to input and output
- ii) common emitter ↙ mostly used
- iii) common collector

If resistors are ignored

- $V_{RE} = V_{EE}$
- $V_{CB} = V_{CC}$



base is g rounded

KCL:

$$I_E = I_B + I_C$$

only true
in active
mode

2 plots:

input $\rightarrow I_E$ vs V_{BE}
output $\rightarrow I_C$ vs V_{CB}

J₁: EB is f.B.
J₂: BC is r.B.

weak signal \rightarrow amplified
signal

$$\alpha = \frac{I_C}{I_E}$$

$$\beta = \frac{I_C}{I_B}$$

$$I_B = (1 - \alpha) I_E$$

$I_C = \alpha I_E + I_{CBO}$ ↗ reverse saturation current
for common base
- current measured when
emitter terminal is open

$$I_E \gg I_{CBO}$$

due to min charge
carriers and they are
very small in number

$$I_C = \alpha I_E$$

$$\alpha = \frac{I_C}{I_E}$$

common base
current gain

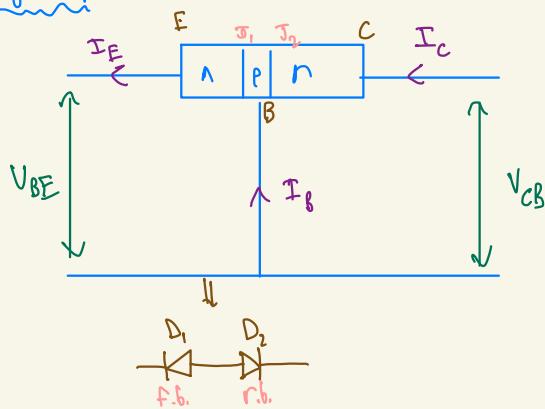
gain = $\frac{\text{output}}{\text{input}}$
amplification
factor

Input characteristics

← characteristics of f.b. diode

graphical relation of input V and I for different output V

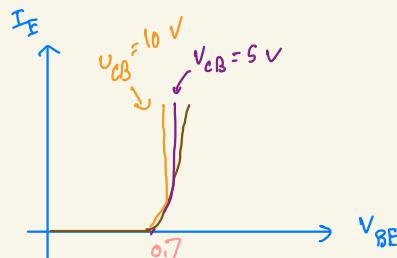
CB configuration



so we are plotting data for D_1
(f.b. Diode
= input characteristic of NPN)

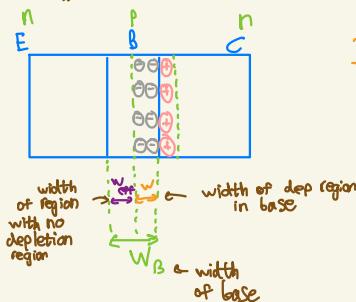
input
 $V : V_{BE}$
 $I : I_E$

output
 $V : V_{CB}$
 $I : I_C$



* Early effect : (base width modulation)

- when V_{CB} is inc



- width of depletion layer increases
- depletion layer will penetrate more in B since it's lightly doped

hole conc is low and immobile ions can be easily unpaired

$$W_B = W_{eff} + W$$

$$W_{eff} = W_B - W$$

AS V_{CB} , $I_E \uparrow$

output: $V_{CB} \uparrow$ $W \uparrow$ $W_{eff} \downarrow$ since penetration of depletion region in base will increase

region where recombination takes place

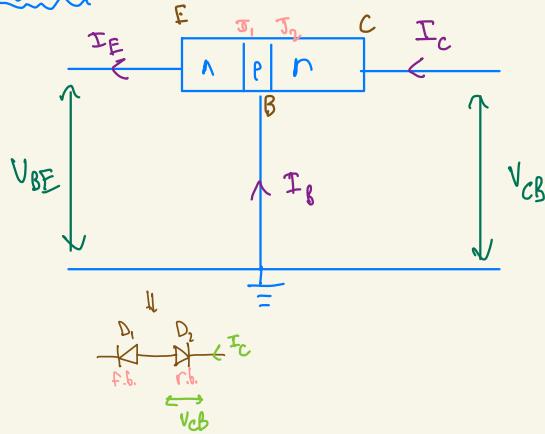
Also: increase in conc gradient due to $W_{eff} \downarrow$

when $W_{eff} \downarrow$ the chance of recombination in base decreases
⇒ leading to increase in input current I_E

out put characteristics \leftarrow r.b. characteristic of diode

graphical relation of out V and I for different input I

CB configuration



$$I_c = \alpha I_e + I_{CO} \quad (\text{independant of } V_{CB})$$

$$I_c \approx \alpha I_e$$

$$I_c \approx I_e \quad \alpha = 0.95 - 0.98$$

↳ output current is affected by input

In cutoff:

- both diodes are r.b.
- transistor will remain off
- can be represented by open switch

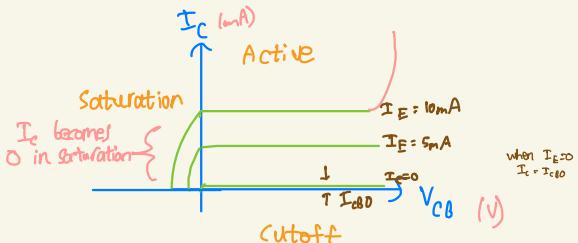
In Saturation:

- both diodes are f.b.
- transistor represented by closed switch
- logical ON

input
 $V: V_{BE}$
 $I: I_e$

output
 $V: V_{CB}$
 $I: I_c$

we want to plot
 V_{CB} vs I_c
for different values of I_e



- if V_{CB} continues to inc there will be breakdown and current will inc rapidly
- this never happens cuz transistor can't handle high power being dissipated

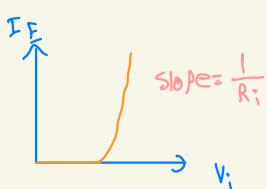
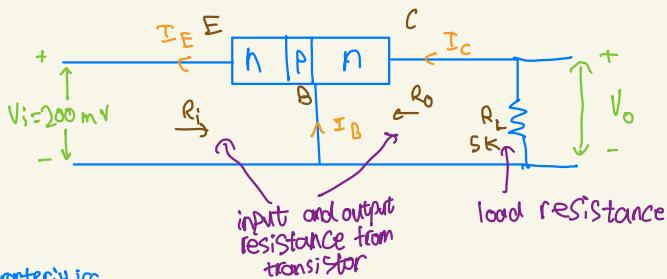
If plot was to be inverted, it would be similar to r.b. characteristics for p.n junction diode

Transistor Amplifying Action

using cB config

- interested
in AC response

→ find V_o



when slope ↑ $R_i \downarrow$

- so R_i of trans
is very small

$$R_i = 20 \Omega$$

input $V_i = I_E R_i \Rightarrow I_E = \frac{V_i}{R_i} \approx \frac{200 \times 10^{-3}}{20}$

neglect

$$= 10 \text{ mA}$$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha I_E$$

$$I_C \approx I_E \approx 10 \text{ mA}$$

$$V_o = I_C R_L$$

$$\begin{aligned} &= 10 \text{ mA} \times 5 \text{ k}\Omega \\ &\approx 50 \text{ V} \end{aligned}$$

output



$$R_o = 100 \text{ k}\Omega$$

can easily find V_o

$$V_o = I_C R_L = 10 \text{ mA} \times 5 \text{ k}\Omega = 50 \text{ V}$$

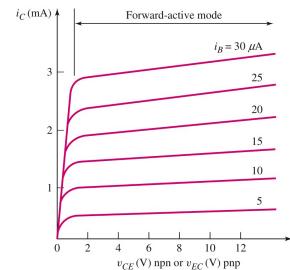
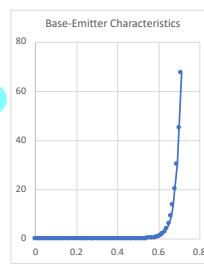
input was 200 mV
and out was 50 V.
∴ there is amplification

Why Biasing?

- The term **biasing** applies to a transistor just like we use it in general
- To create a **favourable or unfavourable condition** in transistor circuits

Recall that:

- BJT is a non-linear device**
- The slope of both the input and output characteristic curves vary from zero to infinity



- Thus, it is important to set the transistor at a desired operating condition
- A desired operating condition is set by applying DC biasing voltages to both the base-emitter and collector-base junctions

1

1

Common-Base Biasing Configuration

At this point, our goal is to bias a transistor in **active mode**, where the **base-emitter junction is forward biased**, and the **collector-base junction is reverse biased**. Let's consider this is the proper biasing for a transistor until we learn the other modes of operation.

NPN

Input terminal: Emitter
Output terminal: Collector
Common terminal: Base

- The base-emitter junction is forward biased by V_{EE}
- The collector-base junction is reverse biased by V_{CC}
- The base is common between input and output

PNP

Input terminal: Emitter
Output terminal: Collector
Common terminal: Base

- The base-emitter junction is forward biased by V_{EE}
- The collector-base junction is reverse biased by V_{CC}
- The base is common between input and output

2

I don't understand
these 2 slides

AC Equivalent Circuit

- An ideal voltage source has zero internal resistance
- Thus, a DC voltage source can be considered as a short circuit in an AC equivalent circuit

3

3

AC Equivalent Circuit of the CB Biasing Circuit

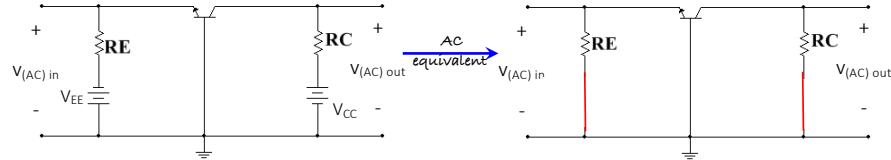
Do you see any problem in the equivalent circuit?

- How much signal voltage (AC component) is applied to the input of the transistor, which in this case is the voltage at emitter with respect to base?
- How much output voltage (AC component) is available at the output of the transistor, which in this case is the voltage at collector with respect to base?
- What happens if V_{EE} exceeds 0.7 V, say increases to 1V?

4

4

CB Biasing With Base and Collector Resistors



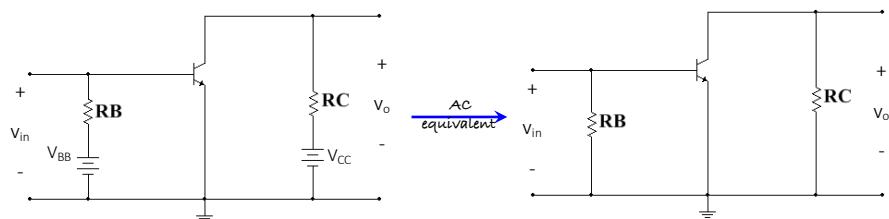
- R_E is in parallel to the base-emitter junction
- The signal voltage across the base-emitter junction, v_{be} is equal to the signal voltage drop across R_E
- The signal current will be divided
- Similarly, the signal voltage across the collector-base junction, v_{ce} is equal to the signal voltage drop across the collector resistor R_C
- The base resistor R_E limits DC biasing current
- Reverse the polarity of V_{EE} and V_{CC} for a pnp transistor

5

5

Common-Emitter Biasing Configuration

Again, the goal is to bias in active mode, where the base-emitter junction is forward biased, and the collector-base junction is reverse biased.



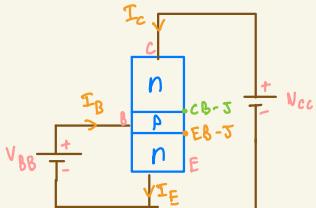
Input terminal: Base
Output terminal: Collector
Common terminal: Emitter

- The base-emitter junction is forward biased by V_{BB}
- The collector-base junction is reverse biased by V_{CC}
- The emitter is common between input and output
- Reverse the polarity of the sources for a pnp transistor

* 6

6

common-emitter configuration of transistor



← emitter is common to input side and output side

- To amplify signal BJT must work in active mode

E_B
full biased

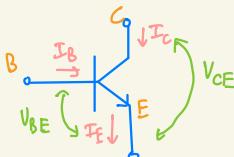
C.B.
rev biased

* P is +ve wrt n = +ve bias

$$I_E = I_C + I_B \quad \dots \textcircled{1}$$

} true for any BJT

$$I_C = \alpha I_E + I_{CBO} \quad \dots \textcircled{2}$$



input:
current $\rightarrow I_B$
voltage $\rightarrow V_{BE}$

output
current $\rightarrow I_C$
voltage $\rightarrow V_{CE}$

$$\beta = \frac{I_C}{I_B}$$

current amplification factor

↑
check reso
academy video #70
for proof

note:

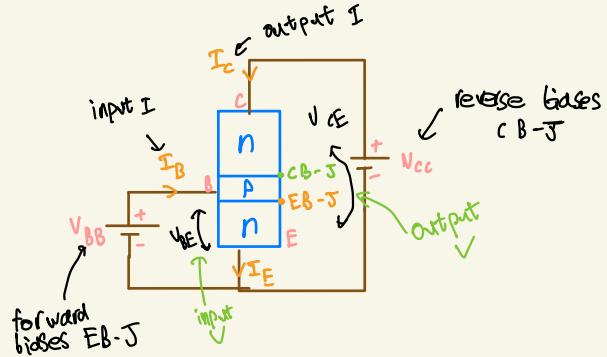
common base
 $I_C = \alpha I_E + I_{CBO}$

common emitter
 $I_C = \beta I_B + (\beta + 1) I_{CBO}$
 β is large

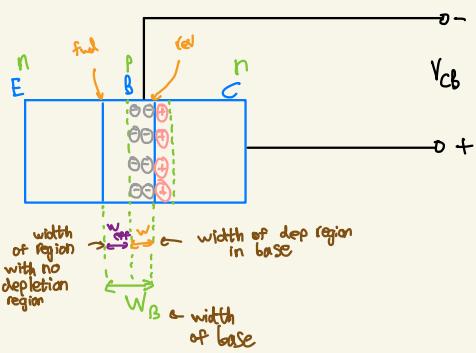
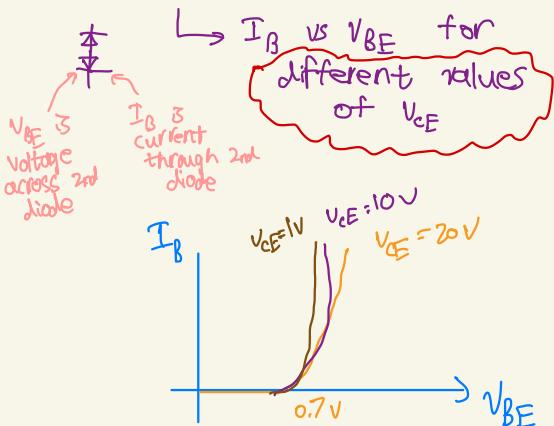
leakage current has more contribution with CE config than CB, in output current

common-emitter transistor

forward bias diode = input characteristics



revisit Early effect
to see how V_{CE} changes
graph
(base width modulation)



-width of depletion layer will increase
and penetrate more in base region.
cuz base is lightly doped

$$W_{eff} = W_B - W$$

↑

$V_{CE} = V_{CB} + V_{BE}$

$V_{CE} \uparrow \Rightarrow V_{CB} \uparrow \Rightarrow n \uparrow \Rightarrow W_{eff} \uparrow$

↑
width
of depletion
layer inc

$I_B \downarrow$

when $weff \downarrow$, the region where recombination takes place decreases.

Electrons from emitter won't recombine with holes in base region, reducing base current I_B (input)

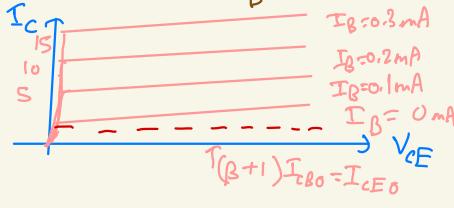
Output characteristics $\leftarrow I_C \text{ vs } V_{CE}$ for different levels of I_B

$$I_C = \beta I_B + (1 + \beta) I_{CBO} \quad \text{constant}$$

independent of output voltage V_{CE} , only depends on I_B

when $I_B = 0$, $I_C = (1 + \beta) I_{CBO}$

this small current is leakage current in CE config



In this case
 $\beta = 50$

* why is slope not 0 ?? *

- I_C also depends on V_{CE} due to early effect

$$\uparrow V_{CE} = V_{CB} + V_{BE}$$

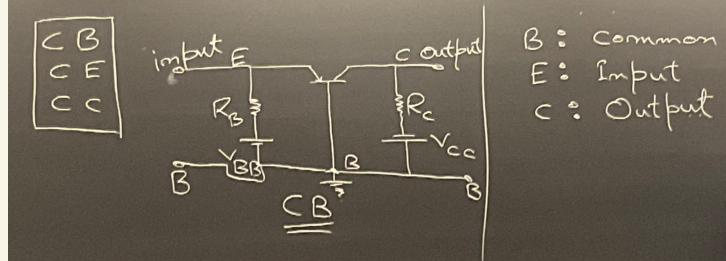
$$V_{eff} \downarrow \Rightarrow I_B \downarrow \Rightarrow I_C \uparrow$$

as I_B dec I_C inc
cuz more electrons from emitter will collect in collector and so it's current will inc

* Reswitch video

72 for discussion
on Active, Saturation, cutoff

- write KVL
- find currents using β relationship
- write KVL equations again



Example - CB
(DC analysis)

$$R_B = 120 \text{ k}$$

$$V_{BB} = 4V$$

$$V_{CC} = 10V$$

$$R_C = 1k$$

$$\beta = 100$$

find

$$(a) I_B$$

$$(b) I_C$$

$$(c) V_{CB}$$

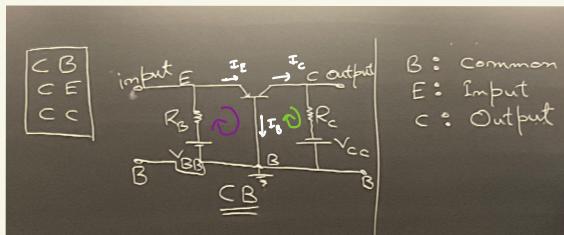
Approach

- always start from base

- assume base emitter voltage $= 0.7$

$$(V_{BE})$$

when its on $= 0.7$



② Now we can find I_B using an equation that relates them

$$I_B = \frac{I_E}{\beta + 1} = 0.27 \text{ mA}$$

③ Can now find I_C using either $I_C = \beta I_B$ or $I_C = I_E - I_B$

$$I_C = 27 \mu\text{A}$$

$$i_E = i_C + i_B$$

$$\frac{i_E}{i_B} = \frac{i_C}{i_B} + 1$$

$$\frac{i_E}{i_B} = \beta + 1$$

$$\rightarrow i_E = i_B(\beta + 1)$$

① write KVL equation

$$-V_{BB} + I_E R_B + V_{BE(on)} = 0$$

$$I_E = \frac{V_{BB} - V_{BE(on)}}{R_B}$$

$$= \frac{4 - 0.7}{120}$$

$$= 0.0275 \text{ A}$$

$$= 27.5 \times 10^{-6} \text{ A}$$

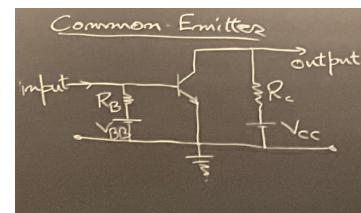
$$= 27.5 \text{ mA}$$

find V_{CB} by KVL

$$-V_{CC} - V_{CB} + I_C R_C = 0$$

$$V_{CB} = -V_{CC} + I_C R_C$$

$$= -9.97 \text{ V}$$



* most important configuration

Common-Emitter Biasing Configuration

Input terminal: Base
Output terminal: Collector
Common terminal: Emitter

More ways to bias a transistor are coming soon

- Is the transistor properly biased? Yes
- How much output signal V_o will be available at the collector?

7

7

Common-Collector Biasing Configuration

Again, the goal is to bias in **active mode**, where the **base-emitter junction is forward biased**, and the **collector-base junction is reverse biased**.

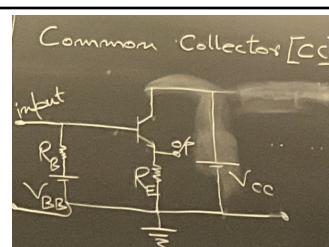
Input terminal: Base
Output terminal: Emitter
Common terminal: Collector

- V_{CC} is shorted for the signal

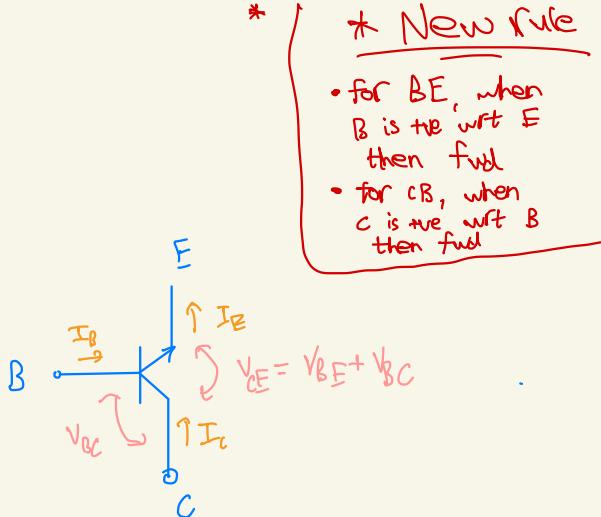
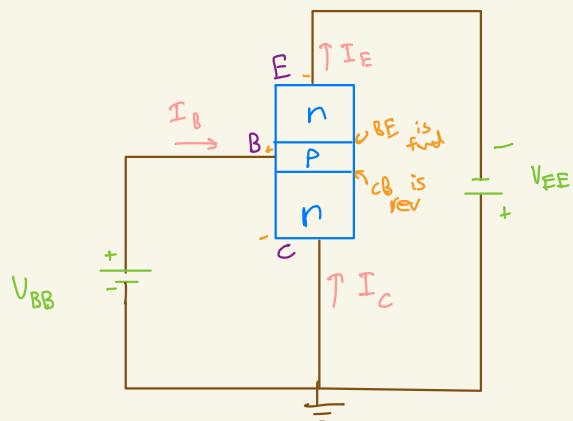
- The **base-emitter junction is forward biased by V_{BB}**
- The **collector-base junction is reverse biased by V_{CC}**
- The collector is common between input and output
- Reverse the polarity of the sources for a pnp transistor**

8

8



Common-collector



output characteristics

repire with I_E vs V_{CE} for diff values of I_B

$$I_c \propto I_E$$

$$\alpha = 0.98 - 0.98 \approx 1$$

$$I_c \approx I_E$$

** Output characteristics of CE = CC

gamma ??
current amplification factor

- I may want to amplify voltage / current in a circuit.
- Picking the correct configuration allows me to amplify specific values.

I forgot KVL

Common Collector: Example

Example: Consider the CC biasing circuit, where $V_{BB} = 5\text{ V}$, $V_{CC} = 10\text{ V}$, $R_B = 40\text{ k}\Omega$, $R_E = 1\text{ k}\Omega$, $\alpha = 0.994$, and $V_{BE(on)} = 0.7\text{ V}$. Determine I_B , I_C and V_{CE} . (DC analysis)

Soln: By applying KVL at the base circuit we have,

$$V_{BB} - I_B \times R_B + V_{BE(on)} + I_E \times R_E = 0$$
or,
$$V_{BB} - I_B \times R_B + V_{BE(on)} + I_B (\beta + 1) R_E = 0$$
 [since, $I_E = I_B(\beta + 1)$]

$$I_B = (V_{BB} - V_{BE(on)}) / (R_B + (\beta + 1) R_E)$$

$$\beta = \alpha / (1 - \alpha) = 165.7$$

$$I_B = (5.0 - 0.7) / (40 \times 10^3 + (165.7 + 1) \times 1 \times 10^3) = 20.8 \mu\text{A}$$

$$V_{BB} - V_{BE(on)} = + I_B R_B + I_B R_E (\beta + 1) \rightarrow I_B = (V_{BB} - V_{BE}) / (R_B + R_E)$$

We know, $I_C = \beta I_B = 165.7 \times 20.8 \times 10^{-6} = 3.45 \text{ mA}$

Again, by applying KVL at the collector circuit we have,

$$V_{CC} - I_E \times R_E + V_{CE}$$
or,
$$V_{CC} = (I_C / \alpha) R_E + V_{CE}$$
 [since, $I_C = \alpha I_E$]
or,
$$V_{CE} = \{V_{CC} - (I_C / \alpha) R_E\} = 6.53 \text{ V}$$

9

- when current flows from - to + it's +ve
- assume resistance to be a voltage drop

he made a mistake

Common Collector: Example

Example: Consider the CC biasing circuit, where $V_{BB} = 5\text{ V}$, $V_{CC} = 10\text{ V}$, $R_B = 40\text{ k}\Omega$, $R_E = 1\text{ k}\Omega$, $\alpha = 0.994$, and $V_{BE(on)} = 0.7\text{ V}$. Determine the biasing voltage applied to CB junction and the type of biasing applied to this junction. (The same as previous problem)

Soln: We have already obtained that $I_B = 20.8 \mu\text{A}$
Thus, $V_B = V_{BB} - I_B \times R_B = 5 - 20.8 \times 10^{-6} \times 40 \times 10^3 = 4.17 \text{ V}$
From the circuit, $V_C = 10 \text{ V}$

Thus, the collector base junction biasing voltage V_{CB} is given by

$$V_{CB} = V_C - V_B = 10 - 4.17 = 5.83 \text{ V}$$

Since V_{CE} is positive, the collector is at positive voltage with respect to the base, which makes the CB junction of the NPN transistor reverse biased.

10

properly biased

NE550 Academy:

73

10

Biasing Configurations and Biasing Techniques

- We have learned different biasing **configurations**, namely,
 - Common-base biasing (CB)
 - Common-emitter biasing (CE)
 - Common-collector biasing (CC)
- In active mode, **base-emitter junction is forward biased**, and the **collector-base junction is reverse biased** regardless
- This course will cover **CE and CC configurations in depth**

- So far, we have learned how to **bias a transistor using two separate sources**
- **use of two separate sources is not always feasible** for practical circuits
- The following section covers different **techniques** of biasing a transistor.

11

11

DC Analysis:

KVL:

$$V_{CC} = I_B R_B + V_{BE \text{ (on)}}$$

$$I_B = \frac{V_{CC} - V_{BE \text{ (on)}}}{R_B}$$

Thus,

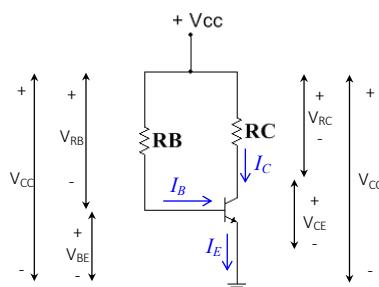
$$I_C = \beta I_B$$

KVL:

$$V_{CE} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

Fixed Bias Circuit



Draw the same circuit for a pnp transistor. Bias it with a negative V_{CC} and analyze the voltage drops to justify proper biasing.

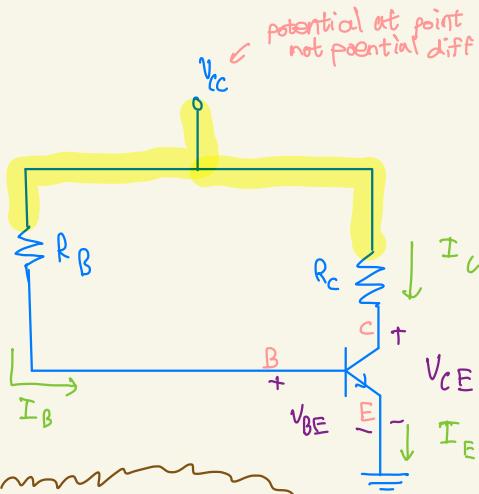
- As illustrated the **voltage drops**, the **base-emitter junction is forward biased**, and the **collector-base junction is reverse biased**
- **V_{CC} is generally much higher than 0.7V**
- The **base resistor R_B limits base current by $I_B = (V_{CC} - 0.7)/R_B$**
- $V_{CE} = (V_{CC} - I_C \times R_C)$
- For **collector-base junction to be reverse biased**, $V_C > V_B$

for this to be properly biased: $R_B > R_C$

12

12

fixed bias config



Find I_c and V_{CE}

① KVL in input loop

$$+V_C - I_B R_B - V_{BE} = 0$$

input current $I_B = \frac{V_{CC} - V_{BE}}{R_B} = 0.7\text{V}$

$$I_C = \beta I_B = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right)$$

② KVL in output loop

$$+V_{CC} - I_C R_C - V_{CE} = 0$$

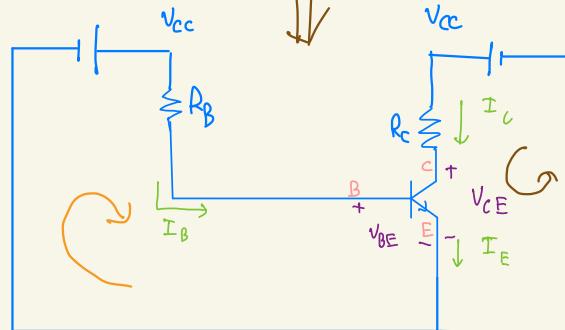
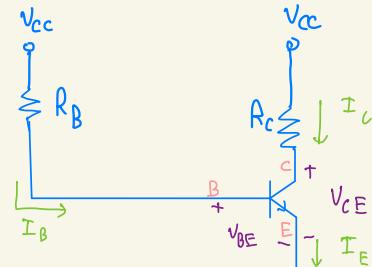
$$V_{CE} = V_{CC} - I_C R_C$$

• EB is fwd biased

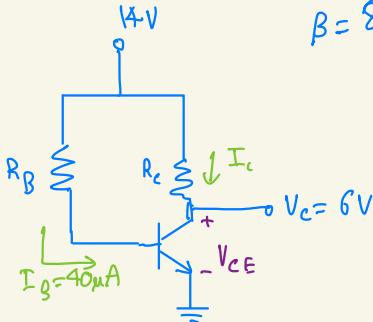
• CB is rev biased

also known as base-bias

equivalent



example



output

$$+V_C - V_{CE} = 0$$

$$V_{CE} = 6\text{V}$$

$$I_C = \beta I_B = 80 \times 40\mu\text{A} = 3.2\text{mA}$$

Input

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{14 - 0.7}{40 \times 10^{-6}} = 33.25 \text{ k}\Omega$$

Output

$$+V_C - I_C R_C - V_C = 0$$

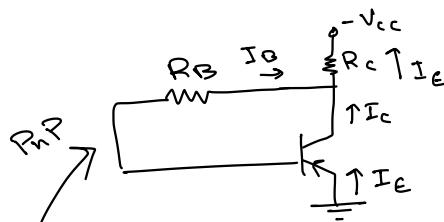
$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{14 - 6}{3.2 \text{mA}} = 2500 \Omega$$

ex 2

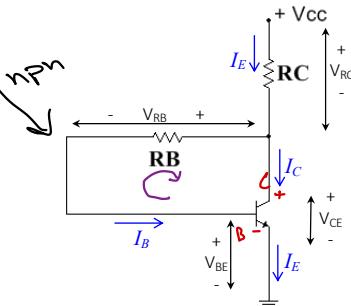
_video 77 from neso

extra

- can review series diode config
for point potentials



Collector to Base Bias



Draw the same circuit for a pnp transistor. Bias it with a negative V_{CC} and analyze the voltage drops to justify proper biasing.

- As illustrated the **voltage drops**, the **base-emitter junction is forward biased**.
- *Here, $V_{CB} = I_B \times R_B = V_{RB}$. *
- The **collector is positive with respect to base**, making the **collector-base junction reverse biased**.

13

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Collector to Base Bias: DC Analysis

DC Analysis for pnp:

$$\begin{aligned} V_{CC} &= I_E R_C + I_B R_B \\ &\quad + V_{BE(on)} \\ &= (\beta + 1) I_B R_C + I_B R_B \\ &\quad + V_{BE(on)} \end{aligned}$$

$$I_B = \frac{V_{CE} - V_{BE(on)}}{(\beta + 1) R_C + R_B}$$

$$V_{CC} = I_E R_C + V_{CE}$$

By KVL we can write,

$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE(on)}$$

$$V_{CC} = I_B (\beta + 1) R_C + I_B R_B + 0.7$$

$$I_B = \frac{V_{CC} - 0.7}{(\beta + 1) R_C + R_B}$$

DO NOT
memorize

Again by KVL,

$$V_{CE} = I_B R_B + V_{BE(on)}$$

$$V_{CE} = I_B R_B + 0.7$$

14

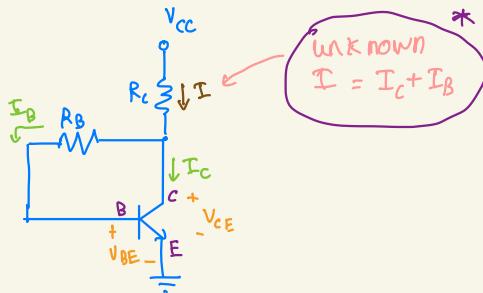
14

I don't
see how
KVL loop
was written

7

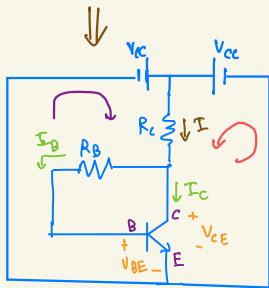
Collector feedback biasing

= collector to base bias



- feedback is introduced from collector to base

- I_c and V_{ce} are coordinates of operating point



① Apply KVL in input loop

$$V_{cc} - (I_c + I_B)R_C - I_B R_B - V_{BE} = 0$$

$$I_c = \beta I_B$$

$$V_{cc} - I_B [(\beta + 1)R_C + R_B] - V_{BE} = 0$$

$$I_B = \frac{V_{cc} - V_{BE}}{(\beta + 1)R_C + R_B}$$

$$I_c = \beta I_B = \frac{\beta(V_{cc} - V_{BE})}{(\beta + 1)R_C + R_B}$$

↙ y coordinate of operating point

② Apply KVL in output loop

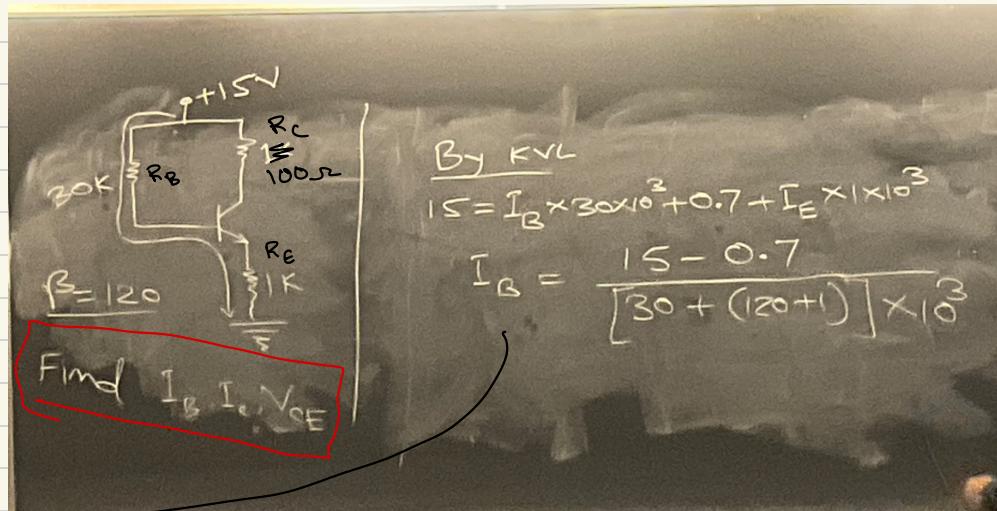
$$V_{cc} - (I_c + I_B)R_C - V_{CE} = 0$$

$$V_{CE} = V_{cc} - (I_c + I_B)R_C$$

- pros and cons discussed in vid 80

- watch vid 81
for example

collector-base ex



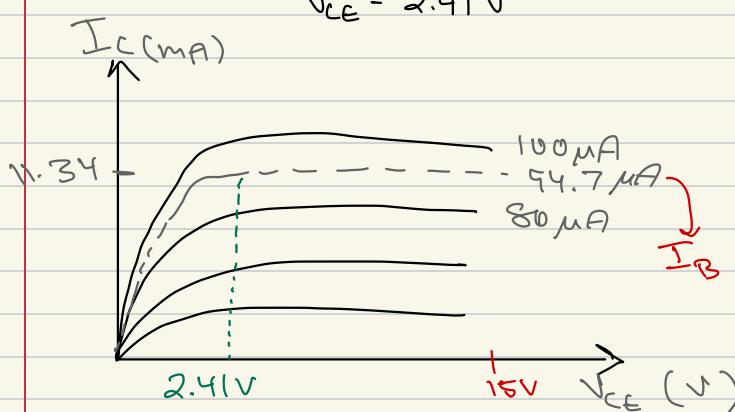
$$I_B = 94.7 \mu A$$

$$\beta I_B = I_C = 120 \cdot 94.7 \mu A = 11.34 \text{ mA}$$

$$\text{by KVL: } 15 = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = 15 - 11.34 \times 100 \times 10^{-3} - \underbrace{(120+1) \cdot 94.7 \times 10^{-6} \times 10^3}_{I_E R_E}$$

$$V_{CE} = 2.41 \text{ V}$$



*Note: The max \$V_{CE}\$ is 15V, this is the transistor model used in the course and \$V_{BE} = 0.7\$ is the on voltage for the transistor.

$$I_B = I_c \cdot \frac{V_{CE}}{V_{BE}}$$

$I_c (mA)$

Graph showing I_c vs V_{CE} with values 60 mA, 40 mA, 20 mA, and 0 mA.

$\beta = \frac{I_c}{I_B} = \frac{6 \times 10^{-3}}{60 \times 10^{-6}} = 100$

$\beta = 120$

Find I_B, I_c, V_{CE}

By KVL

$$15 = I_B \times 30 \times 10^3 + 0.7 + I_E \times 1 \times 10^3$$

$$I_B = \frac{15 - 0.7}{[30 + (20+1)] \times 10^3} = 94.7 \mu A$$

skipped step, find equation relating I_B and I_E

$$I_B \times 30 \times 10^3 + (\beta + 1) I_B \times 10^3 = V_{CC} - V_{BE (on)}$$

$$= 0.7 V$$

$$I_C = \beta I_B$$

$$= 120 \times 94.7 \mu A$$

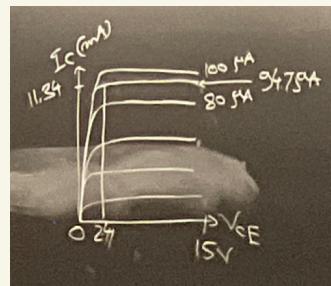
$$= 11.34 mA$$

By KVL

$$15 = I_c R_c + V_{CE} + I_E R_E$$

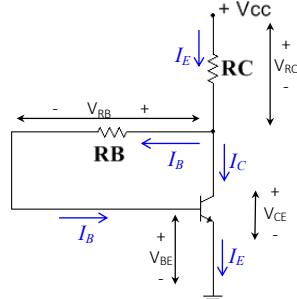
$$V_{CE} = 15 - 11.34 \times 100 \times 10^3 -$$

$$V_{CE} = 2.41 V$$



Collector to Base Bias: Example

Example: For the given collector to base bias circuit assume $V_{CC} = 15$ V. Design the circuit to set $I_B = 30 \mu A$, $I_C = 4.5 mA$, and $V_{CE} = 6V$. Determine R_B and R_C .



$$\text{Soln: } I_E = I_C + I_B = 4.5 \times 10^{-3} + 30 \times 10^{-6} = 4.53 mA$$

$$V_{RC} = V_{CC} - V_{CE} = 15 - 6 = 9 V$$

$$\text{By Ohm's Law, } R_C = V_{RC} / I_E = 9 / 4.53 \times 10^{-3}$$

or, $R_C = 1.99 k\Omega$

$$\text{Again, } R_B = (V_{CE} - 0.7) / I_B$$

or, $R_B = (6 - 0.7) / 30 \times 10^{-6}$

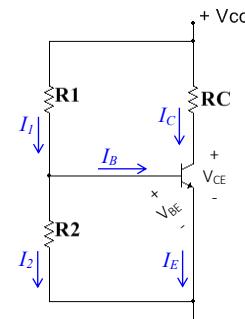
or, $R_B = 176.67 k\Omega$

15

15

Voltage Divider Bias or Self Bias

- Base-emitter junction is forward biased
- Collector-base junction is reverse biased
- *If B-E Junction is on then $V_{R2} = V_{BE} = 0.7V$*
- $I_1 = I_2 + I_B$ and $I_E = I_C + I_B$
- R_1 and R_2 are not in series
- Voltage division formula for R_1 and R_2 doesn't work here
- R_1 limits the current in base circuit
- The base-emitter junction is in parallel with R_2
- When R_1 remains constant, increase of R_2 will increase base current, and the opposite is also true.
- Generally, R_1 is higher than R_2

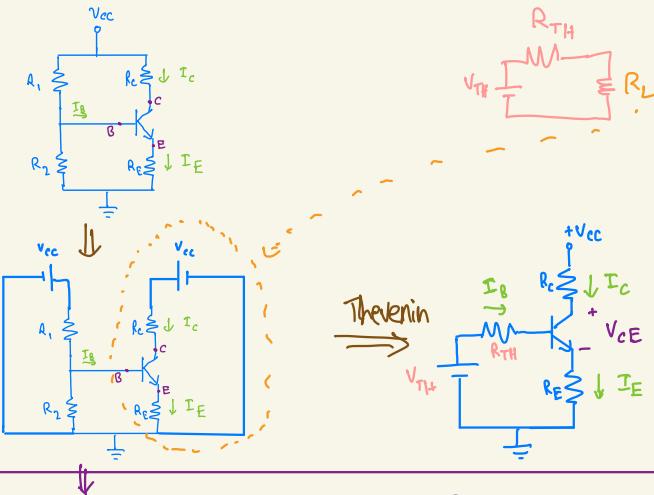


16

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Voltage - divider bias config

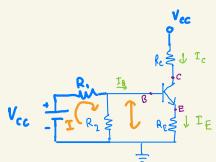
- must use thevenin's



current source = open circuit

voltage source = short circuit

STEPS



- To find V_{TH} :
- current in loop
- V across load i.e. across R_2

use KVL

$$V_{CC} - I(R_1 + R_2) = 0 \quad I \times R_2 = V_{TH} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$I = \frac{V_{CC}}{R_1 + R_2}$$

③ find V_{CE}

apply KVL in output loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$I_E \approx I_C$

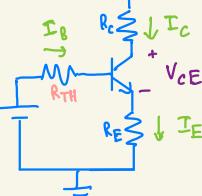
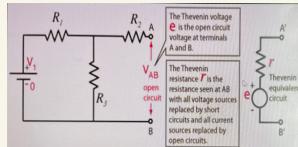
$$\text{also: } V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$I_C = \beta I_B$. will change

$I_E = I_B (\beta + 1)$ this eqn

- watch id for ad voltages of voltage divider

- watch 84 for example



① find R_{TH} and V_{TH}

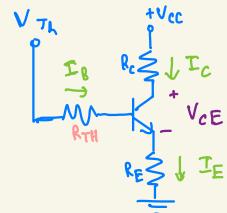
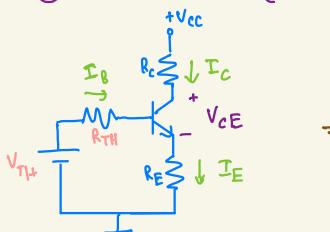
short circuit all V sources and open circuit load



$$R_{TH} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Now this is simply emitter bias config

② find I_B and I_C



apply KVL in input loop $I_E = (\beta + 1) I_B$

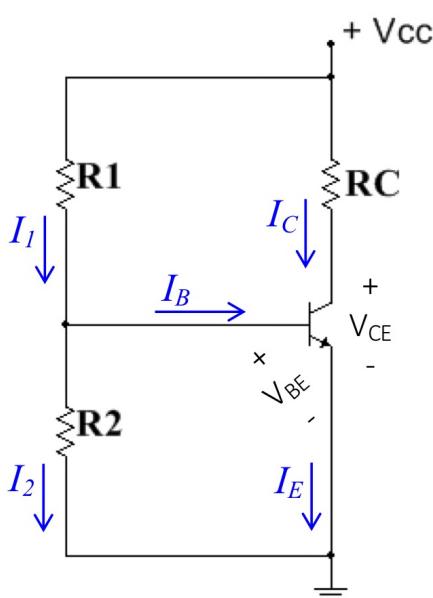
$$+V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

$$V_{TH} - I_B R_{TH} - (\beta + 1) I_B R_E - V_{BE} = 0$$

$$V_{TH} - I_B (R_{TH} + R_E (\beta + 1)) - V_{BE} = 0$$

$$I_C = \beta I_B$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}$$



→ If R_1 is changed
 → V_1 is not changed as $V_2 = V_{BE} = 0.7V$
 ∵ since $V_1 + V_2 = V_{CC}$
 If V_2 stays same then V_1 stays the same
 → $i_1 = \frac{V_1}{R_1}$ will change
 → $i_2 = \frac{V_2}{R_2}$ stays same
 → I_B will change
 Since $I_1 = I_B + I_2$
 Similar happens if R_2 is changed

In the above case, changing R_2 is better than changing R_1 .

DC Analysis of the above circuit:

$$i_1 = \frac{V_{CC} - V_2}{R_1}, \text{ since } V_2 = V_{BE(\text{on})} = 0.7V \rightarrow i_1 = \frac{V_{CC} - 0.7}{R_1}$$

$$i_2 = \frac{V_2}{R_2} = \frac{V_{BE(\text{on})}}{R_2} = \frac{0.7}{R_2}$$

$$i_B = i_1 - i_2$$

and

$$i_C = \beta i_B \rightarrow \text{a rule from unit 1}$$

By KVL:

$$\text{the KVL loop} \quad V_{CC} = i_C R_C + V_{CE}$$

using that:

$$V_{CE} = V_{CC} - i_C R_C$$

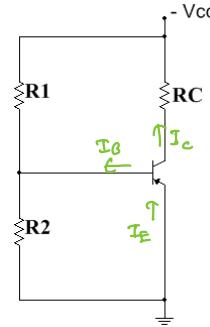


pnp would be same process, just switch polarities.

Voltage Divider Bias of a PNP Transistor

Here is your homework

- Compare this circuit with the circuit shown in previous slide
- Apparently, the only differences you will find are in transistor type and the polarity of V_{CC}



- Indicate the currents and voltages with right directions and polarities as shown in the previous slide
- Compare every bullet in the previous slide and identify what is valid and what is not valid for this pnp transistor

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Finding base current I_B

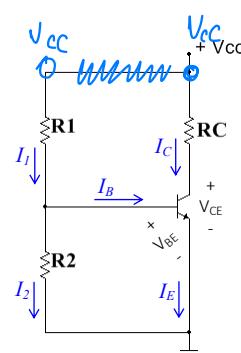
$$\text{Here, } I_1 \times R1 = V_{CC} - I_2 \times R2$$

$$\text{or, } I_B = (V_{CC} - 0.7) / R1$$

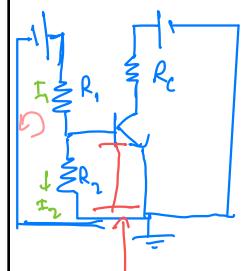
[since $I_2 \times R2 = 0.7$]

$$\text{By KCL, } I_B = I_1 - I_2$$

$$\text{or, } I_B = (V_{CC} - 0.7) / R1 - (0.7 / R2)$$



easier than
NESO academy
ex, cuz no
emitter resistor



$$V \text{ across } V_{BE} = I_2 R_2$$

Finding collector-emitter voltage V_{CE}

$$\text{By KVL, } V_{CC} = I_C \times RC + V_{CE}$$

$$\text{or, } V_{CE} = V_{CC} - I_C \times RC$$

$$\text{or, } V_{CE} = V_{CC} - \beta \times I_B \times RC \quad [\text{since } I_C = \beta I_B]$$

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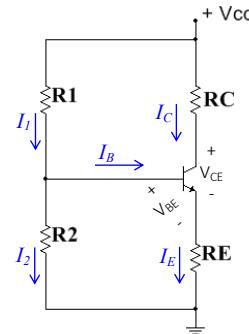
18

* Quiz 1 until *
here

same thing *Self-Bias*

Voltage Divider Bias With Emitter Resistor RE

- Base-emitter junction is forward biased
- Collector-base junction is reverse biased
- $V_{R2} = V_{BE} + I_E \times RE$ ($V_{R2} \neq V_{BE}$)
- $I_1 = I_2 + I_B$ and $I_E = I_C + I_B$
- R_1 and R_2 are not in series
- R_2 and RE are not in parallel
- R_1 limits the current in base circuit
- When R_1 remains constant, increase of R_2 will increase base current, and the opposite is also true.

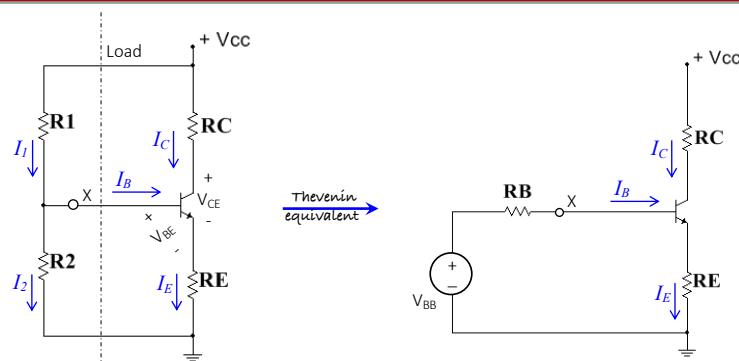


we need to apply thevenin to solve this circuit

19

19

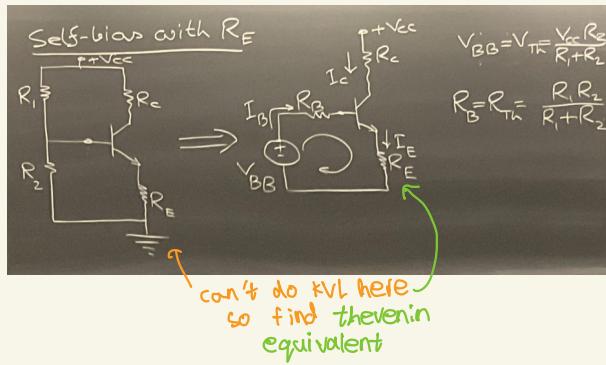
Voltage Divider Bias With Emitter Resistor RE: DC Analysis



- The circuit in the right is a Thevenin equivalent of the voltage divider bias circuit.
- Here, $R_B = R_1 // R_2 = (R_1 + R_2) / (R_1 \times R_2)$
- Also, $V_{BB} = V_{CC} \frac{R_2}{R_1 + R_2}$

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20



By KVL,

$$V_{BB} = I_B R_B + V_{BE(on)} + I_E R_E$$

$$I_B [R_B + (\beta + 1) R_E] = V_{BB} - V_{BE(on)}$$

or, $I_B = \frac{V_{BB} - V_{BE(on)}}{R_B + (\beta + 1) R_E}$

$$I_c = \beta I_B$$

KVL:

$$V_{cc} = I_c R_c + V_{CE} + I_E R_E$$

find V_{CE}

$\beta = 120$

$$I_B = \frac{V_{cc} - 0.7}{120K}$$

$$I_B = 60.8 \text{ mA}$$

$$I_c = \beta I_B$$

$$I_c = 7.3 \text{ mA}$$

$$V_{ce} = I_c R_c + V_E$$

$$\text{or } V_{ce} = V_E - I_c R_c$$

$$= 2 - 14.6 \leftarrow *$$

$$V_{ce} = -6.6$$

The transistor is in saturation.

Thus, $V_{ce} = 0.2$

Then, $I_E = \frac{V_{ce}}{R_E}$

$$I_E = 3.9 \text{ mA}$$

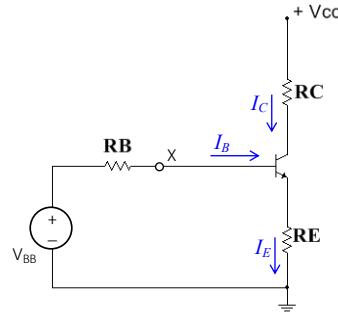
$I_c = \beta I_E$ does not work.

Voltage Divider Bias With Emitter Resistor RE: DC Analysis (Continued...)

$$V_{BB} = I_B RB + V_{BE} + I_E RE$$

$$V_{BB} = I_B RB + V_{BE} + I_B(\beta + 1)RE$$

$$I_B = \frac{V_{BB} - V_{BE}}{RB + (\beta + 1)RE}$$



$$V_{CC} = I_C RC + V_{CE} + I_E RE$$

$$V_{CE} = V_{CC} - I_C RC - I_E RE$$

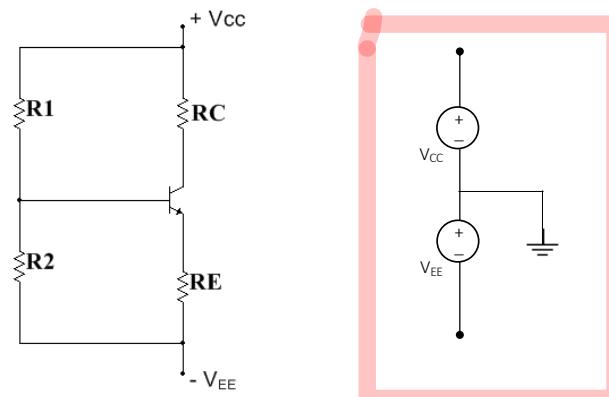
$$V_{CE} = V_{CC} - \beta I_B RC - I_B(\beta + 1)RE$$

$$V_{CE} = V_{CC} - I_B \{\beta RC + (\beta + 1)RE\}$$

21

21

Voltage Divider Bias With Collector and Emitter Sources



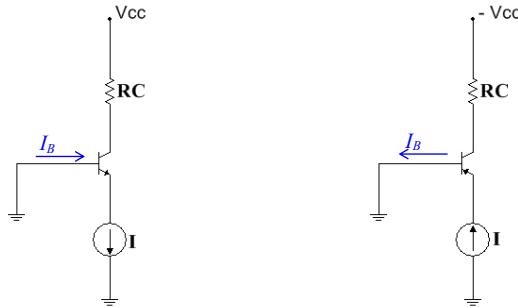
- Base-emitter junction is forward biased
- Collector-base junction is reverse biased
- use Thevenin equivalent circuit for DC analysis

(typo)

22

22

Biasing Using Current Source



- $I_B = \beta \times I$
 - Currents are determined by the current source I
 - Base-emitter junction is forward biased
 - Collector-base junction is reverse biased
- perfect
biasing*

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Voltage Divider Bias: Example

Example: Consider the given voltage divider bias. Given that $V_{CC} = 15\text{ V}$, $R_1 = 10\text{ k}\Omega$, $R_2 = 5\text{ k}\Omega$, $R_C = 1\text{ k}\Omega$, $R_E = 2\text{ k}\Omega$, and $\beta = 100$. Determine I_B , I_C , I_E , I_1 , I_2 , and V_{CE} .

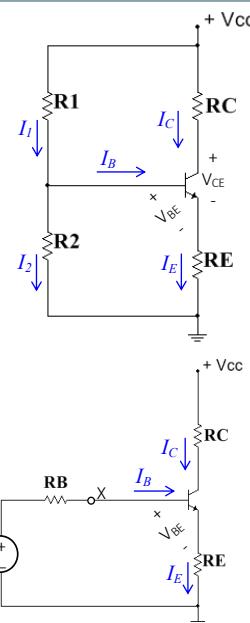
Soln: Obtain Thevenin equivalent circuit as shown at right.

$$V_{BB} = \frac{V_{CC} \times R_2}{R_1 + R_2} = (15 \times 5) / (10 + 5)$$

$$V_{BB} = 5\text{ V}$$

$$R_B = \frac{R_1 \times R_2}{R_1 + R_2} = (10 \times 5) \times 10^3 / (10 + 5)$$

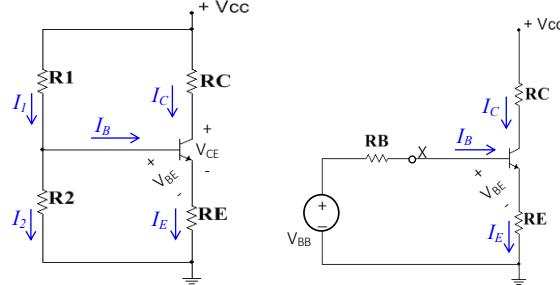
$$R_B = 3.33\text{ k}\Omega$$



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Voltage Divider Bias: Example (continued ...)

$V_{CC} = 15 V$, $R_1 = 10 k\Omega$, $R_2 = 5 k\Omega$, $R_C = 1 k\Omega$, $R_E = 2 k\Omega$, and $\beta = 100$.



$$V_{BB} = I_B R_B + V_{BE(on)} + I_E R_E$$

$$V_{BB} = I_B R_B + V_{BE(on)} + I_B(\beta + 1)R_E$$

$$I_B = \frac{V_{BB} - V_{BE(on)}}{R_B + (\beta + 1)R_E} = \frac{(15 - 0.7) \times 10^{-3}}{3.33 + (100 + 1) \times 2}$$

$$I_B = 20.94 \mu A$$

We know,
 $I_C = \beta \times I_B = 2.09 mA$

Again,
 $I_E = I_C + I_B$
 $I_E = 2.11 mA$

25

25

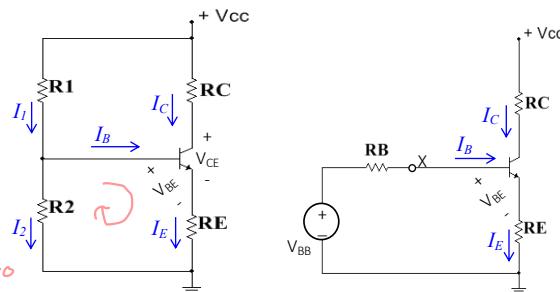
Voltage Divider Bias: Example (continued ...)

$V_{CC} = 15 V$, $R_1 = 10 k\Omega$, $R_2 = 5 k\Omega$, $R_C = 1 k\Omega$, $R_E = 2 k\Omega$, and $\beta = 100$.

$$\begin{aligned} -V_{BE} - I_E R_E + I_2 R_2 &= 0 \\ -V_{BE} - I_B(\beta + 1)R_E + I_2 R_2 &= 0 \\ I_2 &= \frac{V_{BE} + I_B(\beta + 1)R_E}{R_2} \end{aligned}$$

From the given circuit,

$$\begin{aligned} I_2 &= \{V_{BE} + I_B(\beta + 1)R_E\} / R_2 \\ I_2 &= 0.7 + 4.23 \\ I_2 &= 0.986 mA \end{aligned}$$



By KVL,
 $V_{CC} = I_C \times R_C + V_{CE} + I_E \times R_E$
 $V_{CE} = V_{CC} - I_C \times R_C - I_E \times R_E$
 $V_{CE} = 15 - 2.09 - 4.22$
 $V_{CE} = 8.69 V$

Also,

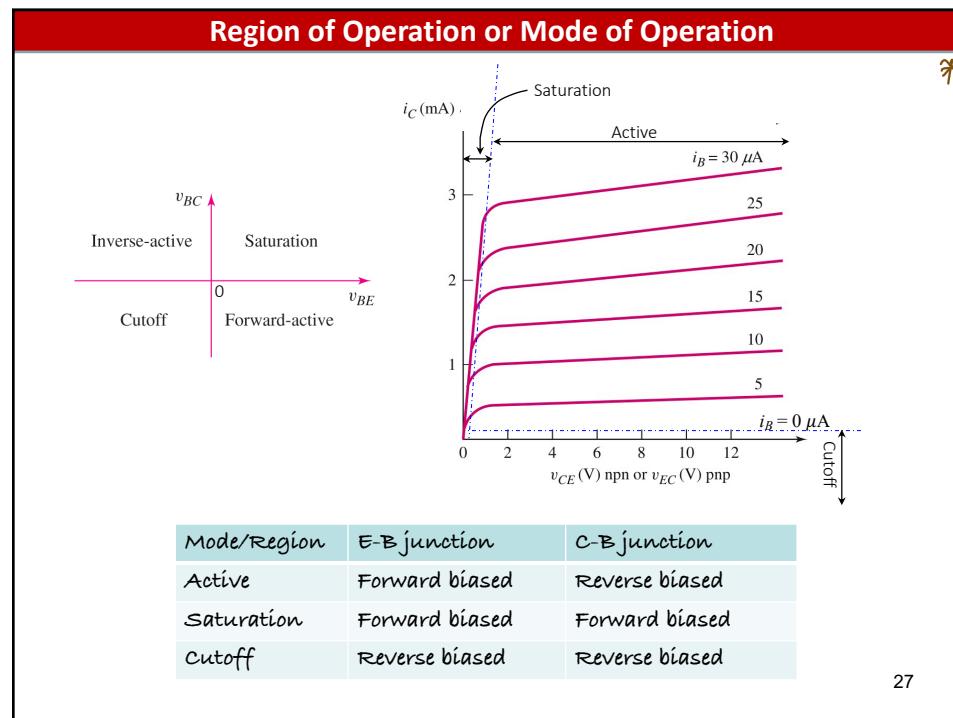
$$\begin{aligned} I_1 &= I_2 + I_B \\ I_1 &= 0.986 mA + 20.94 \mu A \\ I_1 &= 1.01 mA \end{aligned}$$

26

26

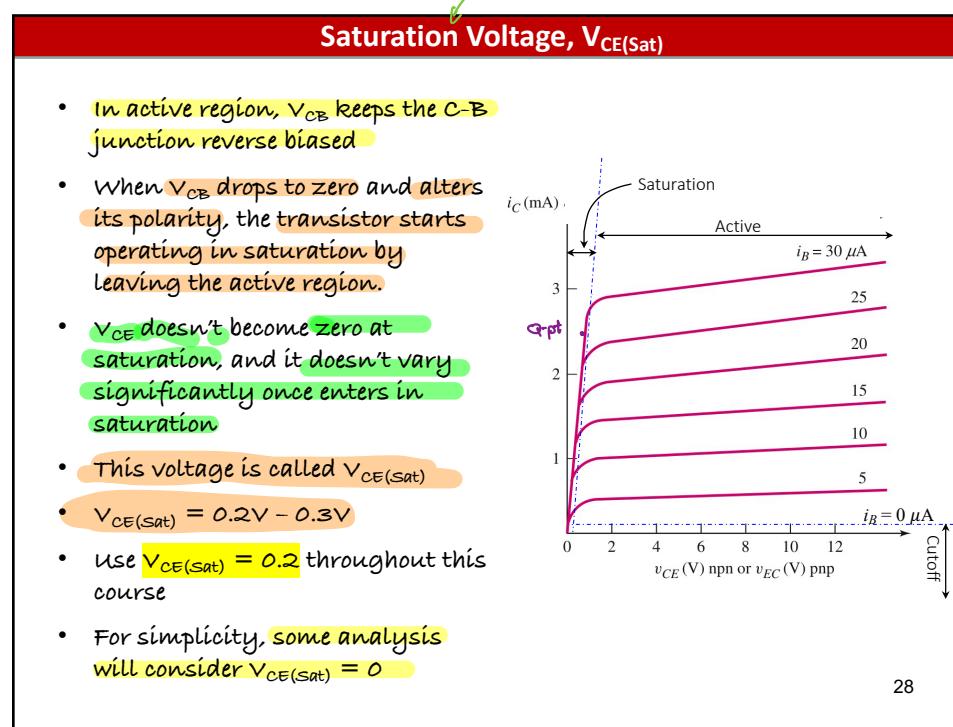
J ₁	J ₂	Region of Operation
f.b.	f.b.	Active
f.b.	f.b.	Saturation → "ON"
r.b.	r.b.	Cutoff → "off"
r.b.	f.b.	Inverted

J₁ is EB
J₂ is CB



- we try to avoid saturation cuz CB is fwd biased and there is distortion in amplified signal

when $I_{C\max} \leq I_{C\text{sat}}$



- both regions are fwd biased
- resistance in circuit = 0

* In saturation I_C is high and V_{CE} is zero
using ohms $R_{CE} = \frac{OV}{I_{C\text{sat}}} = 0$
can short circuit C and E

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video 91 - Neso

for fixed-bias

$$I_{C\text{sat}} = I_{C\text{max}} \frac{V_{CC}}{R_C}$$

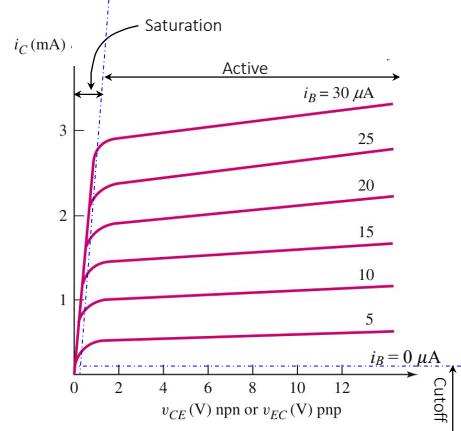
for emitter bias

$$I_{C\text{sat}} = I_{C\text{max}} = \frac{V_{CC}}{R_C + R_E}$$

Cutoff Mode or Cutoff Region

- In cutoff mode, the base-emitter junction is reverse biased.
- Note that a reverse biased base-emitter junction cannot result any negative base current except a negligible amount of leakage current.
- Thus, the base current essentially remains zero, which results no current in collector and emitter.

$$I_B = 0 \Rightarrow I_C = I_E$$



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Saturation Mode: Example

Example: Consider the given circuit where $V_{CC} = 8 \text{ V}$, $R_B = 120 \text{ k}\Omega$, $\beta = 120$, and $R_C = 2 \text{ k}\Omega$. Determine the mode of operation and collector current I_C .

Soln: It is clear from the circuit that the base-emitter junction is forward biased.

$$\text{Here, } I_B = \frac{V_{CC} - V_{BE(on)}}{R_B} = \frac{8 - 0.7}{120 \times 10^3} = 60.8 \mu\text{A}$$

$$\text{Here, } I_C = \beta \times I_B = 120 \times 60.8 \times 10^{-6} = 7.3 \text{ mA}$$

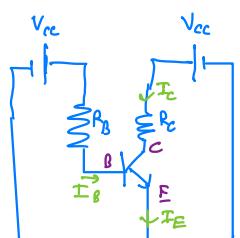
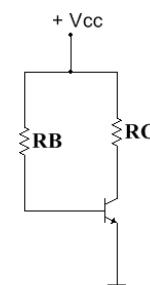
If $I_C = 7.3 \text{ mA}$, the voltage drop across R_C must be

$$V_{RC} = I_C \times R_C = 7.3 \times 2 = 14.6 \text{ V}$$

Can V_{RC} be higher than V_{CC} ? KVL becomes invalid for $I_C = 7.3 \text{ mA}$. We know, $I_C = (V_{CC} - V_{CE}) / R_C$. For the largest possible value of I_C , V_{CE} must have its lowest value, which is $V_{CE(sat)} = 0.2 \text{ V}$.

$$\text{Thus, } I_{C(max)} = (8 - 0.2) / 2 \times 10^3 = 3.9 \text{ mA}$$

This situation ($I_C > I_{C(max)}$) indicates that the transistor is in saturation.



- BE Junctions is fwd biased
- find I_B
- find I_C
- voltage drop across R_C can't be greater than V_{CC}
- must be in saturation
- $V_{CE(sat)} = 0.2$
- find new I_C

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Saturation Mode: Example (Continued ...)

Given, $V_{CC} = 8 \text{ V}$, $R_B = 120 \text{ k}\Omega$, $\beta = 120$, and $R_C = 2 \text{ k}\Omega$. Determine the mode of operation and I_C .

Thus, the correct collector current is $I_C = 3.9 \text{ mA}$
And $V_{CE} = 0.2 \text{ V}$

Let's verify the biasing voltage applied to C-B junction

With $I_C = 3.9 \text{ mA}$, $V_C = V_{CE} = 0.2 \text{ V}$

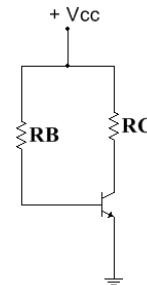
Also, $V_B = V_{BE} = 0.7 \text{ V}$

Thus, $V_{CB} = V_C - V_B = 0.2 - 0.7$

or, $V_{CB} = -0.5 \text{ V}$

This means the n-type collector has negative voltage with respect to the p-type base. Thus, the C-B junction is forward biased.

Hence, the transistor is operating in saturation.



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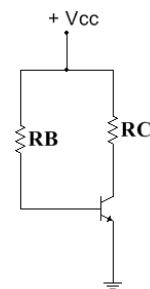
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Saturation Mode: Example (Continued ...)

Gain a Deeper Understanding (GADU)

For the given circuit, can we switch the mode of operation from saturation to active by:

- increasing RC only? If so, at what value does it switch?
- decreasing RC only? If so, at what value does it switch?
- increasing R_B only? If so, at what value does it switch?
- decreasing R_B only? If so, at what value does it switch?
- increasing V_{CC} only?
- decreasing V_{CC} only?
- choosing a transistor with large value of β ?
- choosing a transistor with small value of β ?



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Forced β

Refer to the previous example again, where we determined

$$I_B = 60.8 \mu A \quad \text{and} \quad I_C = 3.9 \text{ mA}$$

$$\text{But we know, } \beta = \frac{I_C}{I_B} = \frac{3.9 \times 10^{-3}}{60.8 \times 10^{-6}} = 64.1$$

Thus, in saturation mode the inherent parameter β is forcefully changed to a lower value, 64.1 in this case.

This decreased β in saturation mode is called forced β .

In this example $\beta = 120$ and $\beta_{(\text{forced})} = 64.1$

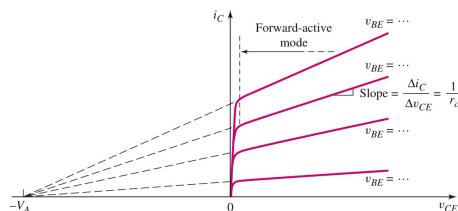
$$\beta_{(\text{forced})} < \beta$$

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Early Voltage V_A

- Ideally, I_C should remain constant with the increase of v_{CE} in active region
- In practice, it increases
- When extrapolated to $I_C = 0$, the curves meet at $v_{CE} = -V_A$
- This is called Early voltage V_A
- V_A is an inherent property
- V_A is always positive
- This effect was first studied by J. M. Early
- At a given v_{BE} increasing v_{CE} increases the reverse bias at CB junction
- The increased reverse bias increases the width of the depletion region
- The scale current I_S increases with the increase of depletion region
- The increased I_S increases collector current I_C



Typically, $50 < V_A < 200 \text{ V}$

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