ENEL469: Analog Electronic Circuits

Department of Electrical and Computer Engineering
University of Calgary

Lab #1: Analyzing a BJT Common Emitter amplifier and logic gates

Everyone must complete pre-lab and bring his/her own (printed) copy of this lab manual

Student's Name	

Do not write here

	Late arrival	
	Pre-lab ready	
	Report printed	
	Table interview	

Supplies:

a) BJT transistor: 2N3904 (Datasheet uploaded on Blackboard)
b) Available resistors: See a list posted on D2L
c) Potentiometer (10k)
d) Assume $\beta = 165$, $V_A = 100$ V, $V_{CE(Sat)} = 0.2$ V, $V_{BE(ON)} = 0.7$ V

Pre-lab Exercises

Pre-lab (Part 1):

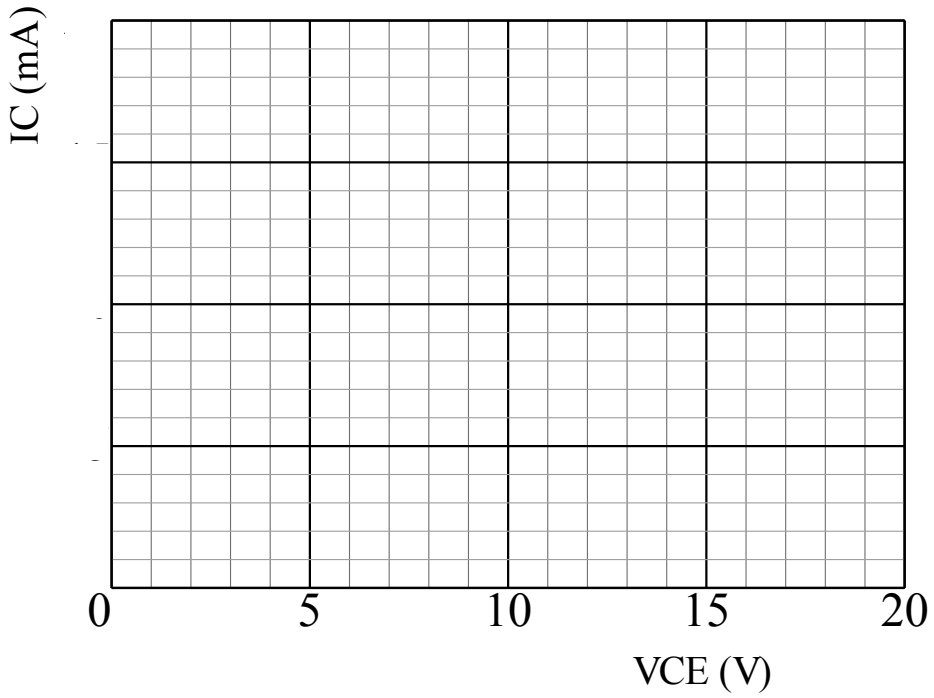
Consider the circuit shown in figure 1 with R_2 = 6.8K. Determine I_B, I_C, I_E, and V_{CE}. Assume $V_{BE(ON)}$ = 0.7 V. Show your work in the space provided below and write these calculated current and voltage values in the second column of table-1 on page #7.

Pre-lab (Part 2): Consider the circuit shown in figure 1 with R_2 = 6.8K. Calculate the small signal parameters r_π, r_e, r_0 and g_m. Show your work and write your answers in the table below.

r_π	KΩ
r_e	Ω
r_0	K Ω
g_m	mA/V

Pre-lab (Part 3): Consider the circuit shown in figure 1 with R_2 = 6.8K. Draw the load line in the graph provided below (Do not neglect base current).

Show your work here.



Pre-lab (Part 4): Consider the BJT NAND gate circuit given in figure 3. V_A and V_B are two inputs of the logic gate. The dc output is taken from the collector of Q_1. Design (i.e., determine R_{B1} and R_{B2}) the circuit for NAND operation. Determine the currents and voltages indicated in the following table for all four possible combinations. For simplicity, assume the collector emitter saturation voltage is 0.2 V (i.e., $V_{CE(Sat)} = 0.2$ V) and $I_C = I_E$.

Space for calculating R_{B1} and R_{B2}

Case-A: $V_A = 0$ V and $V_B = 0$ V:

Case-B: V_A = 0 V and V_B = 5 V:

Case-C: V_A = 5 V and V_B = 0 V:

Case-D: V_A = 5 V and V_B = 5 V:

Current and voltage values obtained in part-4 of the pre-lab exercise

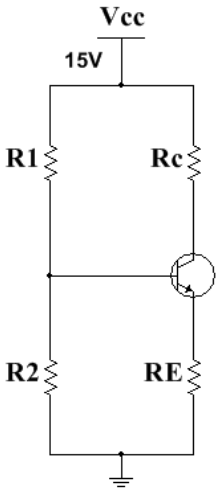
	Input voltages		Input currents		Output currents		Output
	V_A (V)	V_B (V)	I_{B1} (μA)	I_{B2} (μA)	I_{C1} (mA)	I_{C2} (mA)	V_0 (V)
Case-A	0	0					
Case-B	0	5					
Case-C	5	0					
Case-D	5	5					

Does it look like an AND gate?

Lab Studies

A: Measure biasing currents and voltages

Implement the following circuit on a breadboard. This is the circuit, which you have analyzed in the pre-lab. Record the data in table 1.



Resistor values as per colour code

R_1 = 47 KΩ R_2 = 6.8 KΩ

R_C = 1 KΩ R_E = 150 Ω

Measured values of the resistors

R_1 = KΩ R_2 = KΩ

R_C = KΩ R_E = Ω

Figure 1: Common-emitter amplifier circuit with emitter resistor

Table 1: A comparison between calculated (pre-lab) and experimental results

Parameters	Calculated result (from the pre-lab)	Experimental result
V_{BE} (V)		
I_B (μA)		
V_{CE} (V)		
I_C (mA)		
I_E (mA)		
Effective β at the operating condition		
Effective α at the operating condition		

Verify $I_E = I_C + I_B$ using the obtained current values in your experiment. Do you see anything strange? Why so?

B: Determine DC gains and small-signal parameters

For this part, you need to measure currents and voltages at two different operating points Q1 and Q2. The only element you are allowed to change in this circuit is R_2. It would be better to use a potentiometer to set the operating points Q1 and Q2.
You must be able to explain how I_C and V_{CE} depend on R_2?

a) Set the operating point (Q_1) at V_{CE} = 3 V by adjusting R_2. Measure I_B, V_{BE}, I_C, and V_{CE} and record these in table-2.

b) Set the operating point (Q_2) at V_{CE} = 11 V by adjusting R_2. Measure I_B, V_{BE}, I_C, and V_{CE} and record these in table-2.

Table-2: Data for DC gains

	I_B (μA)	V_{BE} (V)	I_C (mA)	V_{CE} (V)
At Q_1				
At Q_2				

c) Determine the DC current gain, DC voltage gain and DC power gain using the current and voltage values recorded in table 2.

DC current gain = $A_{I(DC)} = (I_{C,\,Q1} - I_{C,\,Q2})/(I_{B,\,Q1} - I_{B,\,Q2})$

Voltage gain = $A_{V(DC)} = (V_{CE,\,Q1} - V_{CE,\,Q2})/(V_{BE,\,Q1} - V_{BE,\,Q2})$

Power gain = $A_{P(DC)} = A_{V(DC)} \times A_{I(DC)}$

d) Using the current and voltage values recorded in table 2, calculate the small-signal parameters and voltage gain [Av = – $g_m \times$ (load)] and record them in table 3.

Table-3: Obtained values of the small signal parameters.

	r_π (kΩ)	r_e (Ω)	r_0 (kΩ)	g_m (mA/V)	$A_V \approx -(g_m R_C)/(1+g_m R_E)$
At Q_1					
At Q_2					

Discussion:
Did you expect the corresponding small-signal parameters at Q1 and Q2 to be different?

Are the values obtained in table-3 reasonable?

Compare the DC voltage gain with the voltage gains recorded in table 3. Are they same or different? Why so?

C: Determine the load-line

Measure collector currents for different collector-emitter voltages. Change V_{CE} by changing R_2. You can use a potentiometer. Record your data in table 4 and plot these in the graph provided in figure 2.

Table-4: Data for determining load-line

V_{CE} (V)	**2**	**4**	**8**	**10**	**12**	**14**
I_C (mA)						

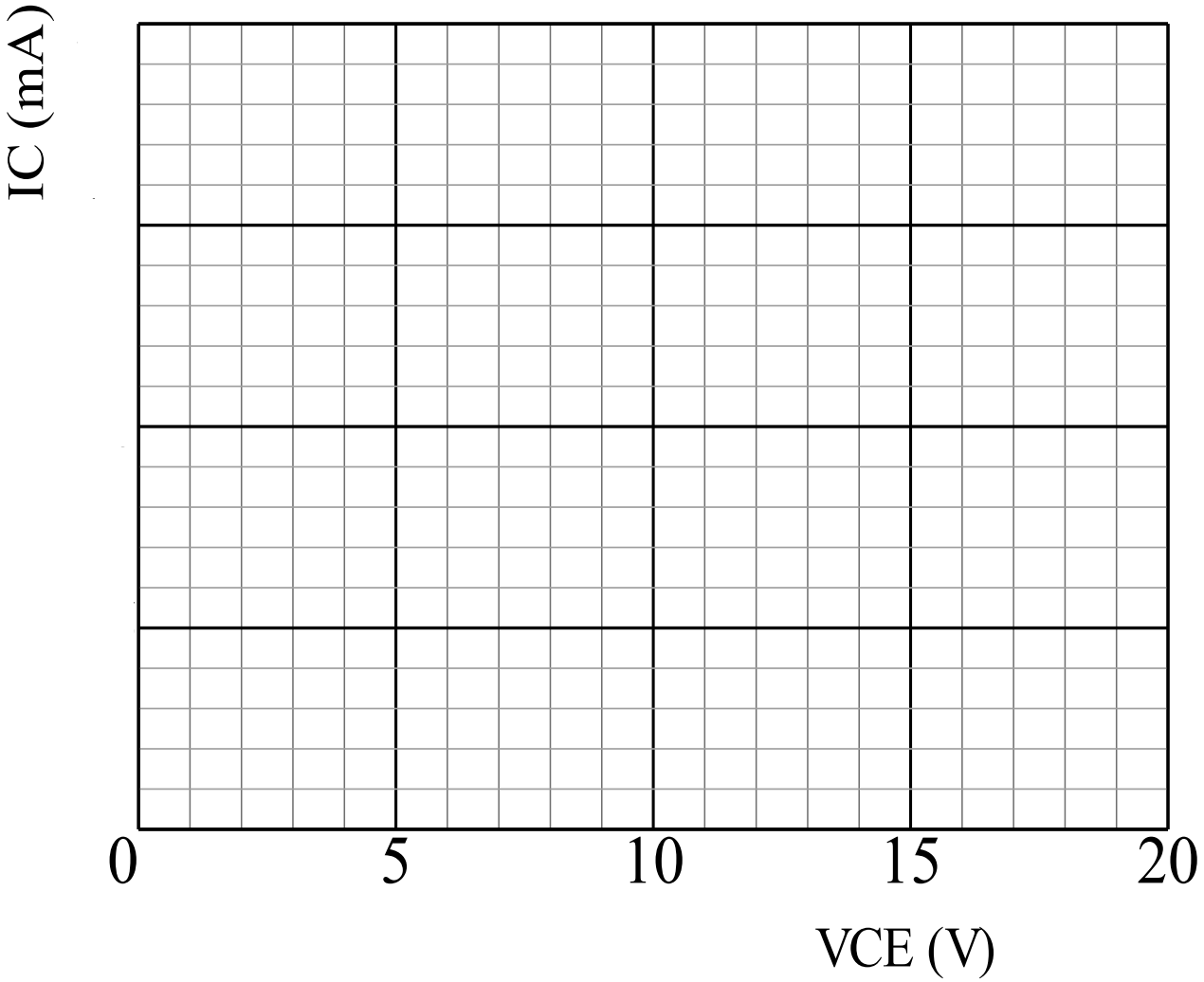


Figure 2. Load line determined from experimental data

C: Construct a two-input BJT NAND gate

a) Implement the circuit shown in figure 3.
b) Consider the following logic definition: 0.0–0.5 V: Logic '0' and 4.5–5.0 V: Logic '1'
c) Verify the NAND operation

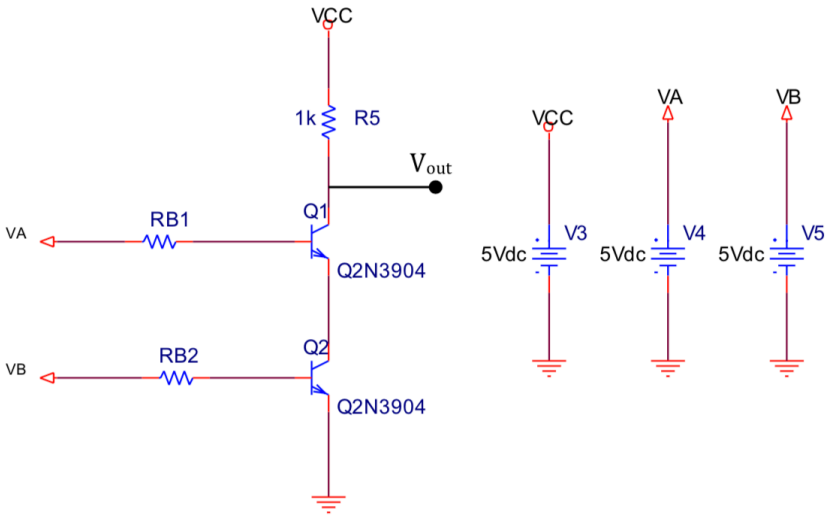


Figure 3. Two-input BJT NAND gate.

Table-5: The BJT NAND gate truth table

V_A		V_B		V_o	
Logic	(V)	Logic	(V)	Logic	(V)
0	0	0	0		
0	0	1	5		
1	5	0	0		
1	5	1	5		
Observations					

Optional work: Construct and verify a two-input AND gate