ENEL469: Analog Electronic Circuits

Department of Electrical and Computer Engineering
University of Calgary

Lab #2: Single-stage CE amplifier design
(On-line version)

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Lab group number	10	Lab section (B01/B02)?	B02

Instructions

For prelab exercise

- All members in a lab group will work together on the same circuit even when there are flexibilities in circuit design
- Everyone in a lab group must submit their own prelab work via D2L
- All lab studies must be completed using Multisim 14.2 or higher
- A pdf or scanned (combined into one file) copy must be submitted via D2L

For lab studies

- All parts of this lab study must be done using Multisim 14.2
- Use the transistor 2N3904 for all experiments in lab 01
- All parts of the lab studies must be saved in separate design window, as the TAs may ask you to show your work at any time during the lab. Students failed to show their work will receive an automatic zero for the respective part.

Part 1: Prelab Exercise

a. Design a common-emitter amplifier circuit, as shown in figure 1, to meet the following specifications.

Design specifications

- The acceptable no-load AC voltage gain is 230 with $\pm 13\%$ deviation, where the voltage gain is defined by $A_v = (v_{ce})/(v_{be})$.
  Hint: Although there is no penalty for the above-mentioned $\pm 13\%$ deviation, target your gain to be 230 with no deviation. A design with voltage gains outside of the allowed deviation will be subject to penalty.
- Use a sinusoidal input signal of $v_{be,rms}$ = 5mV at 50 kHz
- For both, with and without the load R_L, the obtained output voltage (v_c) has to be complete sinusoidal without any clipping and with minimum distortion.

Given parameters

- Use the transistor 2N3904 for simulation purpose.
- V_{CC} = 15 V
- $R_S = 0$, $R_L = 1k\Omega$
- In order to keep your design unique from others, you can pick any set of values of R_1, R_2, and R_C as long as they meet the design specifications.
- $\beta = 160$
- $V_{CE(Sat)} = 0.2$ V
- $V_{BE(on)} = 0.7$ V
- $V_T = 25$ mV
- $V_A = 120$ V
- C1 = C2 = 0.1μF, 0.22 μF, or 0.47 μF

Write the selected values of R_1, R_2, R_C, C_1, and C_2

Resistor	Value (kΩ)
R_1	55kΩ
R_2	3kΩ
R_C	1.4kΩ
R_L	1kΩ
$C_1 = C_2$	0.1 μF

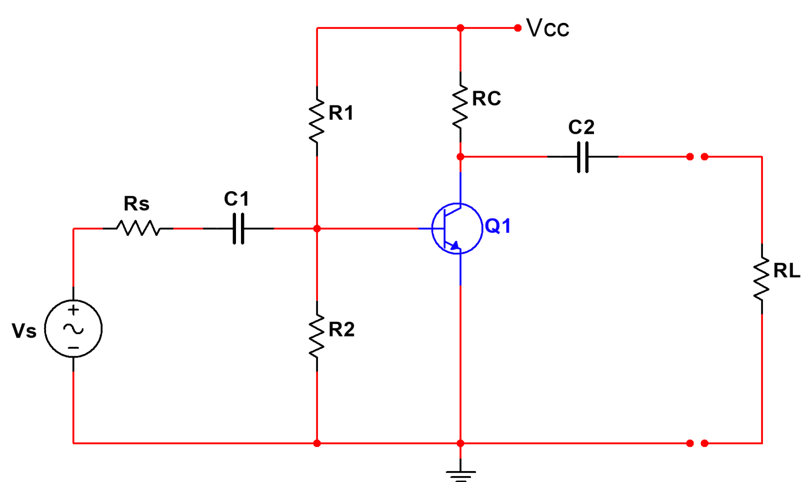

Figure 1. CE amplifier circuit

b. Determining biasing currents and voltages

Using the given parameters and the selected values of R_1 and R_2 in part a, determine:

i) I_1, the current in R_1

ii) I_2, the current in R_2

iii) I_B, the current in the base

iv) I_C, the current in the collector

v) I_E, the current in the emitter

vi) V_{CE}, the voltage between the collector and emitter

Workspace for determining the asked parameters in part b

Determine I_1:

$$\frac{(V_{CC} - V_{BE(on)})}{R_1} = \frac{14.3}{55{,}000} = 260\,\mu A$$

$\boxed{I_1 = 260\ \mu A}$

Determine I_2:

$$\frac{V_{BE\ (on)}}{R_2} = \frac{0.7}{3000} = 233.3\,\mu A$$

$\boxed{I_2 = 233.3\,\mu A}$

Determine I_B:

$$I_1 - I_2 = (260 - 233.3)\times 10^{-7}$$
$$= 26.67\,\mu A$$

$\boxed{I_B = 26.67\,\mu A}$

Determine I_C:

$$I_C = \beta I_B = 160 I_B$$
$$= 4.27 mA$$

$\boxed{I_C = 4.27 mA}$

Determine I_E:

$$I_E = (\beta + 1) I_B = 161 I_B$$
$$= 4.293 mA$$

$\boxed{I_E = 4.293 mA}$

Determine V_{CE}:

$$V_{RC} = I_C R_C$$
$$= 4.267 \times 1.4$$
$$= 5.9738 V$$

$$V_{CE} = 15 - 5.9738$$
$$= 9.0262 V$$

$\boxed{V_{CE} = 9.026\ V}$

c. Determining the small signal parameters r_π, r_e, r_o, and g_m

Determine the small signal parameters r_π, r_e, r_o, and g_m of your designed amplifier circuit.

$$r_\pi = \frac{V_T}{I_B} = \frac{25\times 10^{-3}}{26.7\times 10^{-6}} = 936.3\ \Omega$$

$$r_o = \frac{V_A}{I_C} = \frac{120}{4.27\times 10^{-3}} = 28,103\ \Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{4.27\times 10^{-3}}{25\times 10^{-3}} = 170.7\ mA/V$$

$$r_e = \frac{V_T}{I_E} = \frac{25\times 10^{-3}}{4.293\times 10^{-3}} = 5.82\ \Omega$$

r_π = 936.3 Ω	r_e = 5.82 Ω
r_o = 28,103 Ω	g_m = 170.7 mA/V

d. Determining voltage gain with and without load

Determine the voltage gains A_{vo} without load and A_{vL} with load.

$$A_{vo} = -g_m (r_o // R_C)$$

$$= -32\times 10^{-3} \times \frac{28103 \times 1.4\times 10^3}{28103 + 1400} = -227.64$$

$$= |227.64|$$

$$A_{vL} = -g_m (r_o // R_C // R_L)$$

$$= -100.26$$

$$= |100.26|$$

A_{vo} = 227.64	A_{vL} = 100.26

Part 2: Lab Studies

a. Determining biasing currents and voltage

Consider the same circuit designed in part a (Figure 1) in the prelab section. Construct this circuit in Multisim. Use voltage and current probes to measure the following voltages and currents.

Values calculated in prelab	
I_B (μA)	
I_C (mA)	
V_{CE} (V)	
β	160

Values obtained in Multisim	
I_B (μA)	
I_C (mA)	
V_{CE} (V)	
β	

b. Measuring the AC voltage gain

Use voltage and current probs in Multisim 14.2 and determine the AC voltage gain. Recall that the AC voltage gain is defined by $A_v = (v_{be})/(v_{ce})$ at 50kHz.

Freq kHz	$v_{be,rms}$ (mV)	$v_{ce,rms}$ (mV)	A_{vo}		A_{voL}	
			Calculated	Measured	Calculated	Measured
50	5					

Observations:

i) What is the impedance of capacitors C1 and C2 at 50kHz?

ii) What voltage drop have you observed across the capacitors? Does it make sense to you?

iii) How much difference have you observed between calculated and measured voltage gains?

Deliverables:

i) Perform this simulation in a different design window and save the design window as "ENEL469_Lab-2_01". Your TA will examine your work anytime during the lab.

c. Output waveshape

Connect an oscilloscope to the output terminal and observe the input and output shape.

Observations:

i) Was there any clipping in the output waveshape? Please note that a clipped output doesn't meet the design criteria and will not be accepted.

ii) Have you observed 180^{o} phase difference between the input and output?

Deliverables:

i) Perform this simulation using an oscilloscope and save the waveform as "ENEL469_Lab-2_02". Your TA will examine your work anytime during the lab.

d. Output AC voltage gain at different frequencies

Use voltage and current probs in Multisim 14.2 and determine the AC voltage gain at all different frequencies indicated below.

Freq kHz	$v_{be,rms}$ (mV)	$v_{ce,rms}$ (mV)	A_{vo}		A_{voL}	
			Calculated	Measured	Calculated	Measured
0.02	5					
0.05	5					
0.10	5					
0.20	5					
1	5					
5	5					
100	5					
	5					
	5					
	5					
	5					
	5					
	5					
	5					
	5					
	5					
	5					
	5					

Observations:

i) Does the voltage gain remain constant over the entire frequency range? If not, what is the trend?

ii) What might be the reason for variations at the lower frequency range if there is any?

Deliverables:

i) Perform this simulation in a different design window and save the design window as “ENEL469_Lab-2_03”. Your TA will examine your work anytime during the lab.