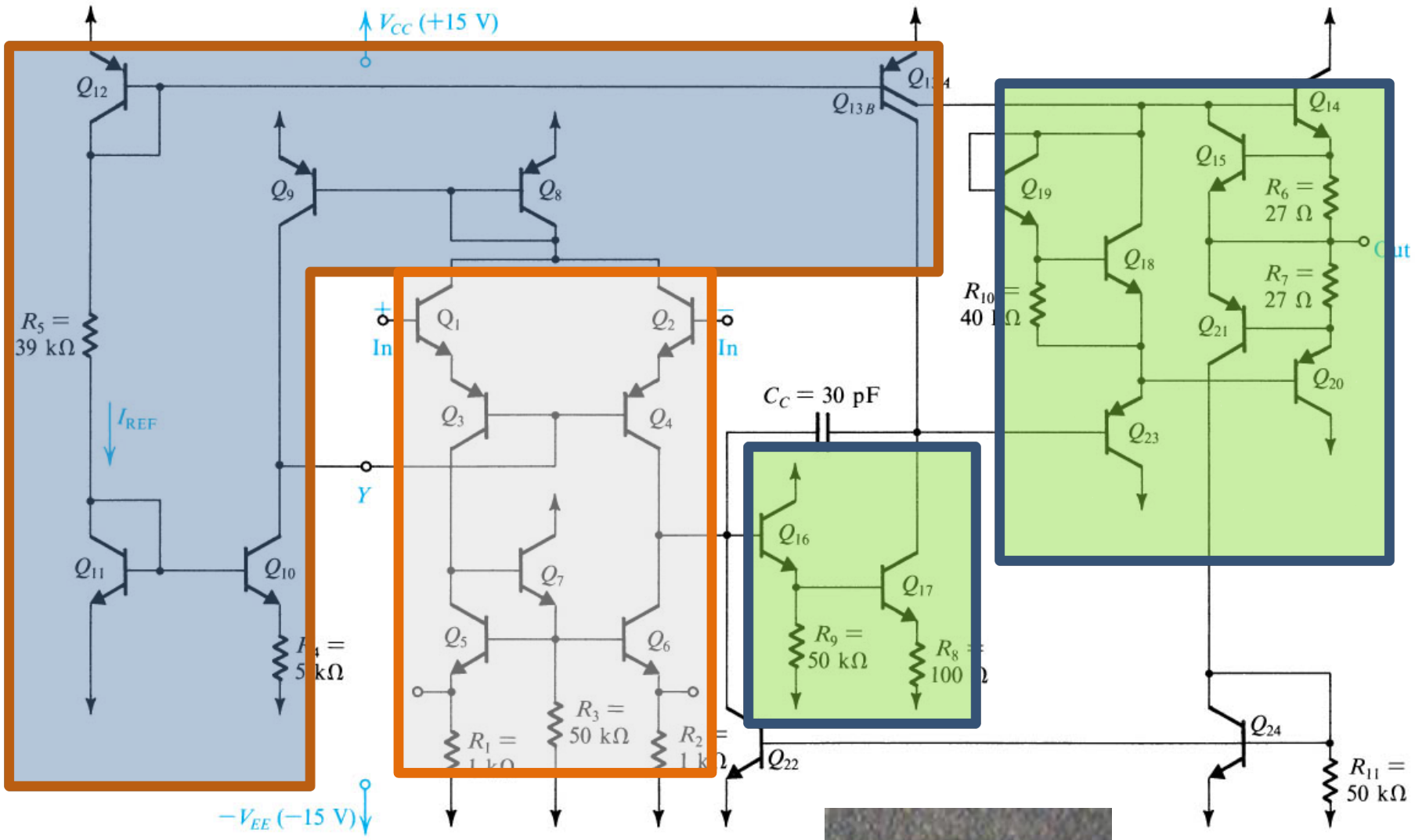
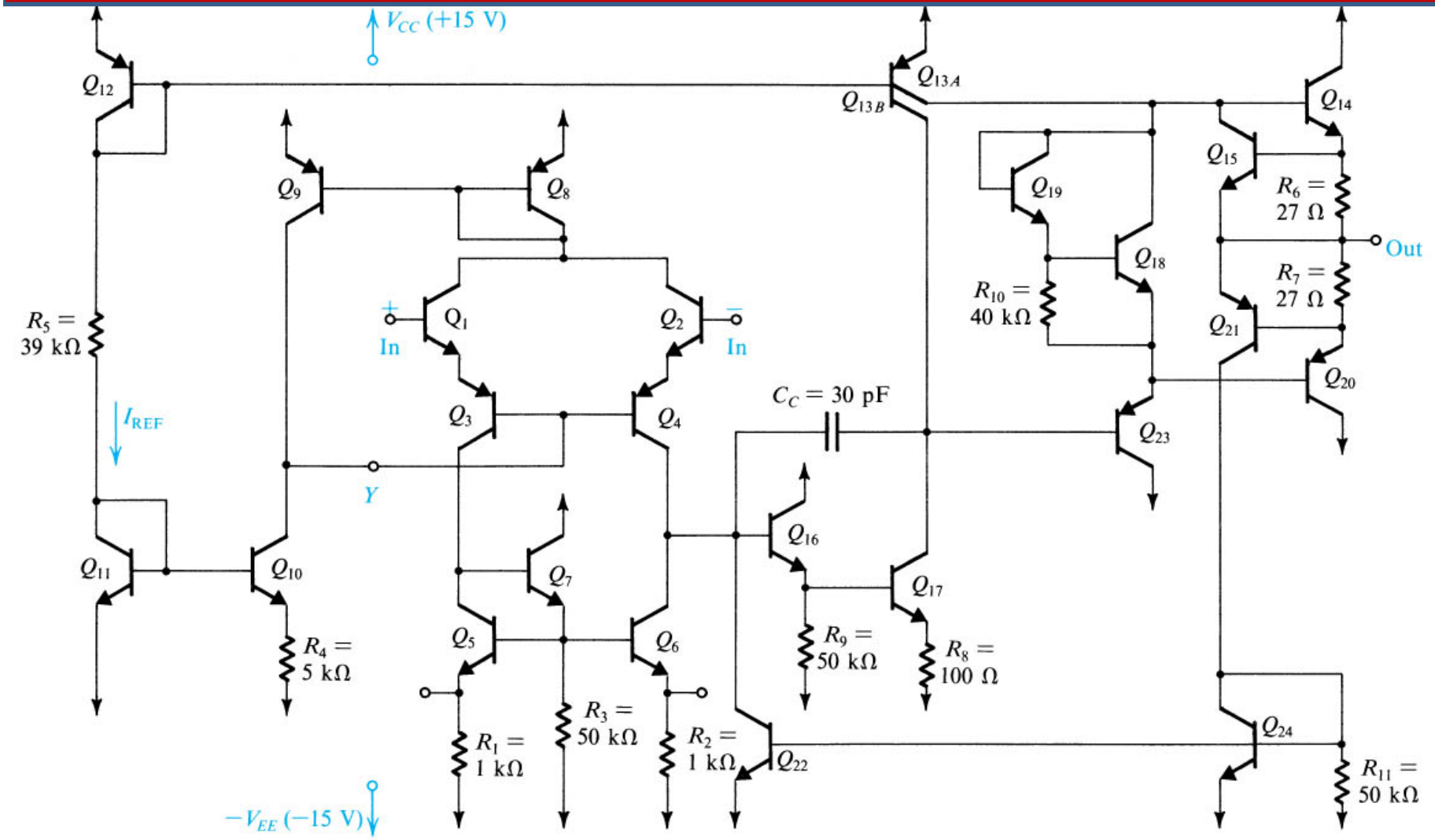
LM 741 Op-Amp Circuit



LM 741 Op-Amp Circuit (Continued …)



Current Source: Q_8, Q_9, Q_{10}, Q_{11}, Q_{12}, and Q_{13}

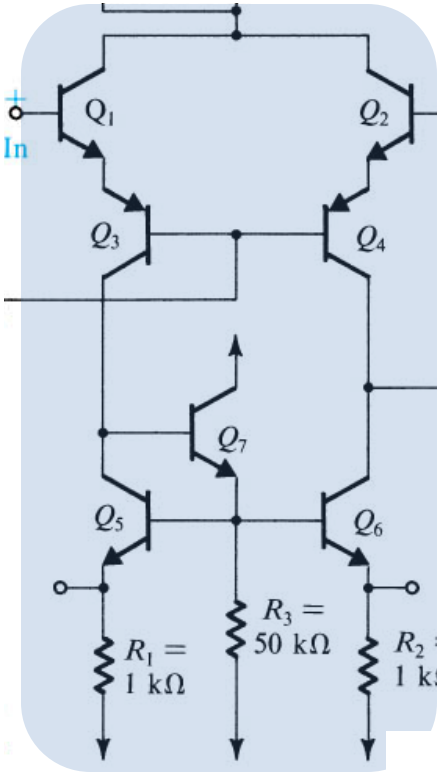
Gain Stage: Q_{13B}*, Q_{16}, and Q_{17}

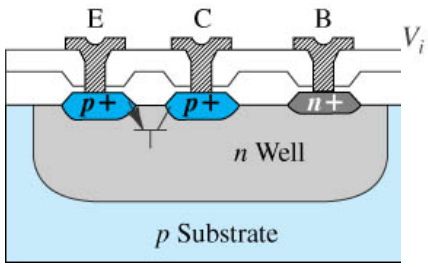
Input Stage: Q_1, Q_2, Q_3, Q_4, Q_5, Q_6, and Q_7

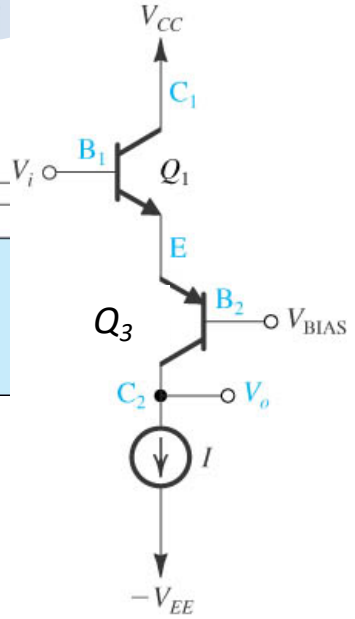
Output Stage: Q_{14}, Q_{18}, Q_{19}, Q_{20}, and Q_{23}

Short Circuit Protection Network: Q_{15}, Q_{21}, Q_{22}, Q_{24}, R_6, R_7, and R_{11}

The Input Stage of LM 741 Op-Amp Circuit



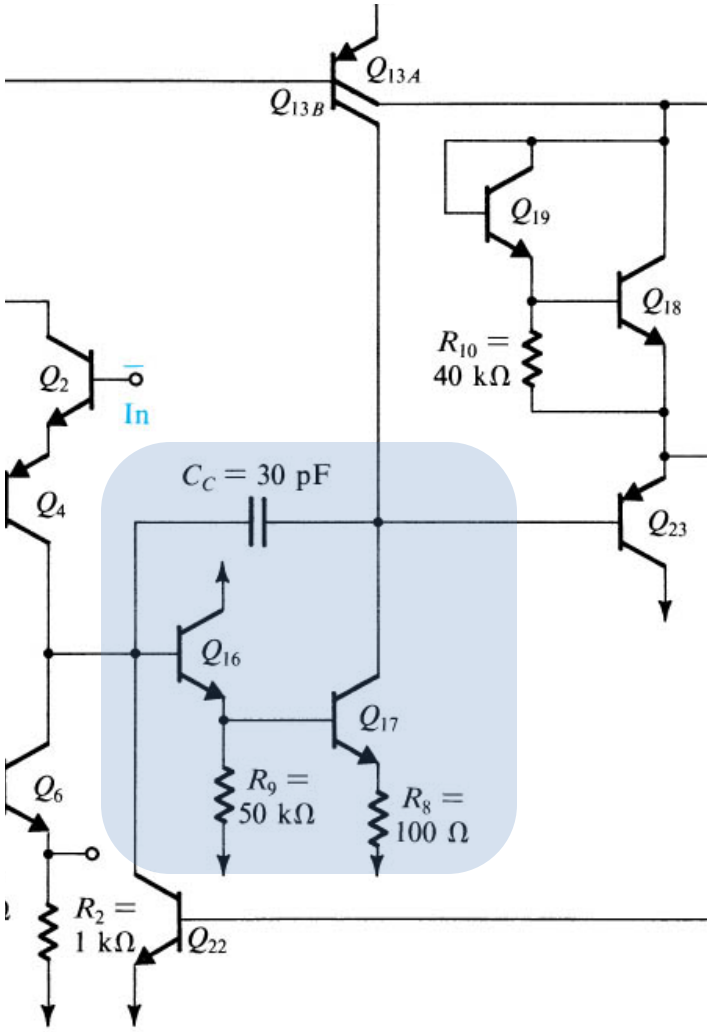




(b)

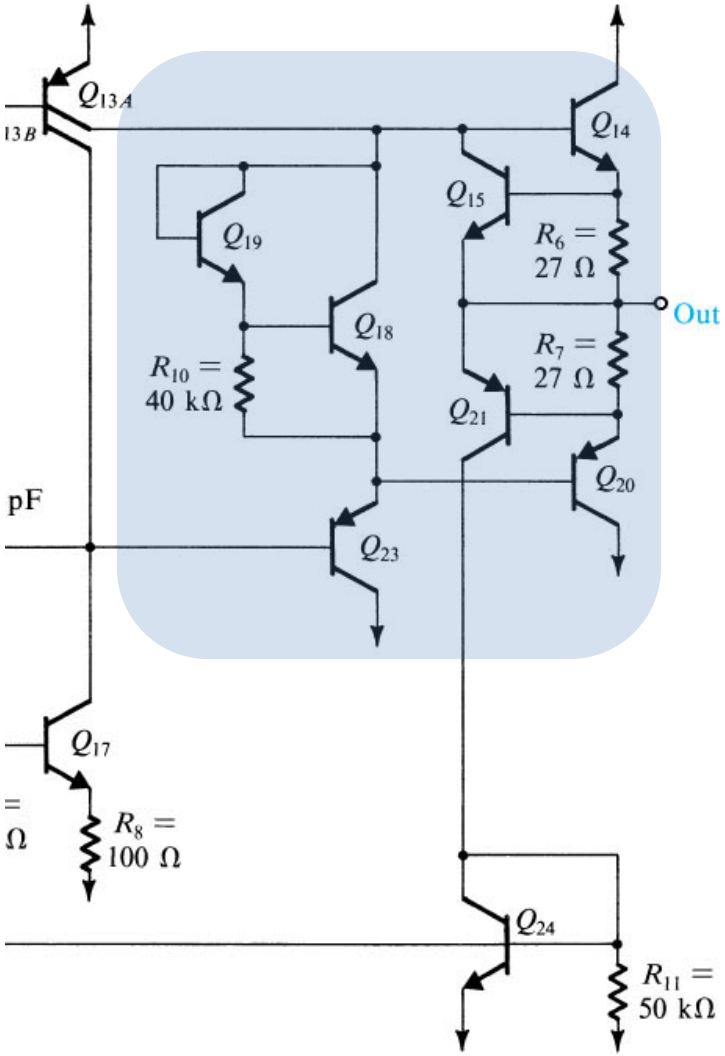
- Q1 and Q2 are emitter follower – high input resistance.
- Q3 and Q4 are differential common base amplifier.
- Input stage is differential version of the CC-CB configuration.
- Lateral pnp transistors (Q3 and Q4) in CB configuration have high frequency response.
- Q3 and Q4 protect the input stage transistors Q1 and Q2 against emitter-base junction breakdown. Reverse breakdown voltage of an npn transistor is about 7 V. The same for a lateral pnp transistor is about 50 V.
- Q5, Q6, and Q7 [also R1, R2, and R3] form the load circuit.
- The output is taken single endedly at the collector of Q6.

The Gain Stage of LM 741 Op-Amp Circuit



- Q13B, Q16, Q17, R8 and R9 form the gain stage.
- Q16 is an emitter follower.
  - Current gain (but no voltage gain).
  - High input resistance.
  - Minimized loading effect.
- Q13B is an active load and current source.
- Q17 is a common emitter amplifier – voltage and current gain.
- The load of Q17 is an effective high resistor provided by Q13B (cheap) and the input resistance of Q23 in parallel.
- C_C is a frequency compensation capacitor.

The Output Stage of LM 741 Op-Amp Circuit



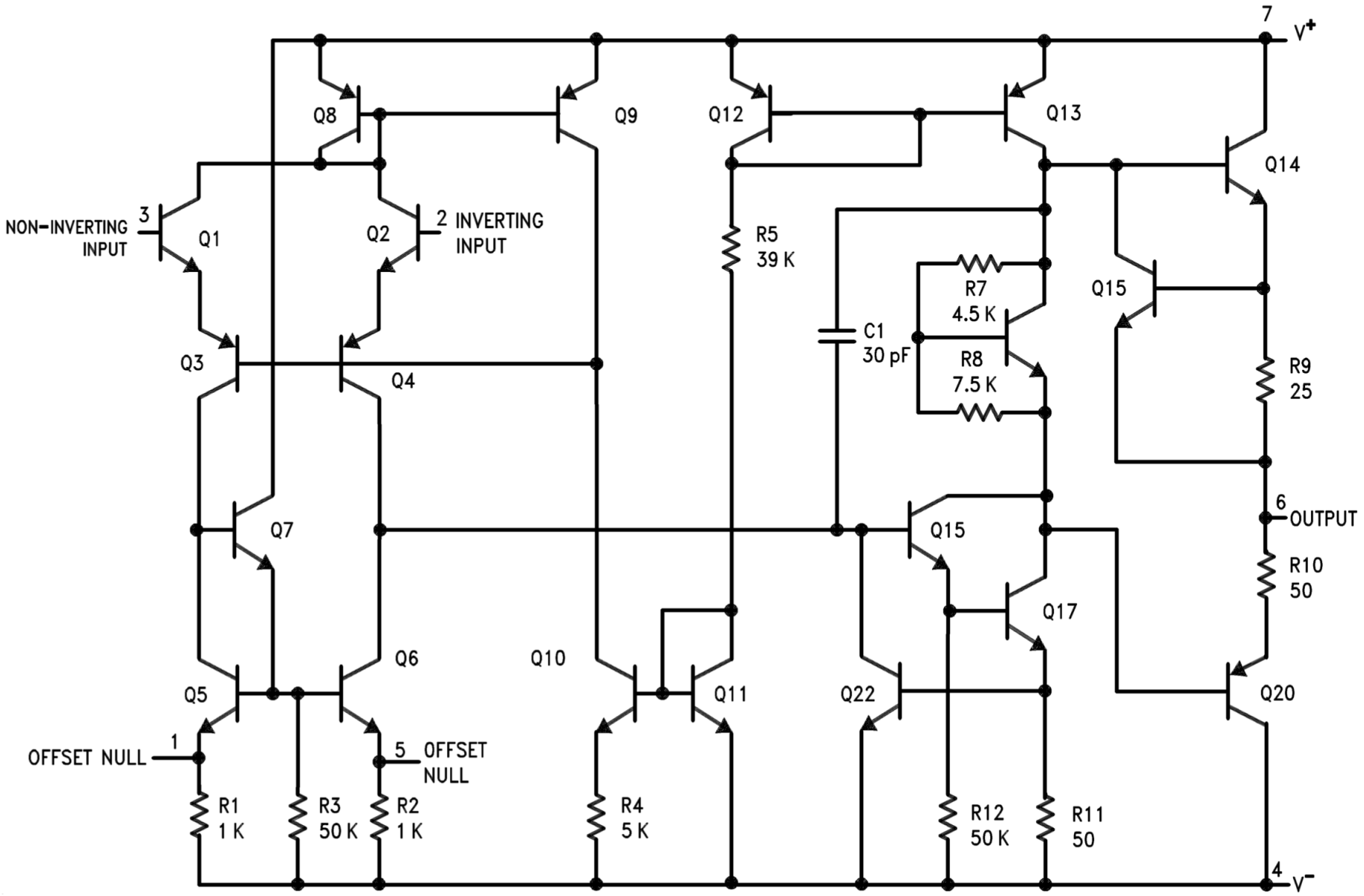
- Design objectives:
  - Low output resistance.
  - Relatively large load current.

- Class AB output stage. This will be covered later in this course.

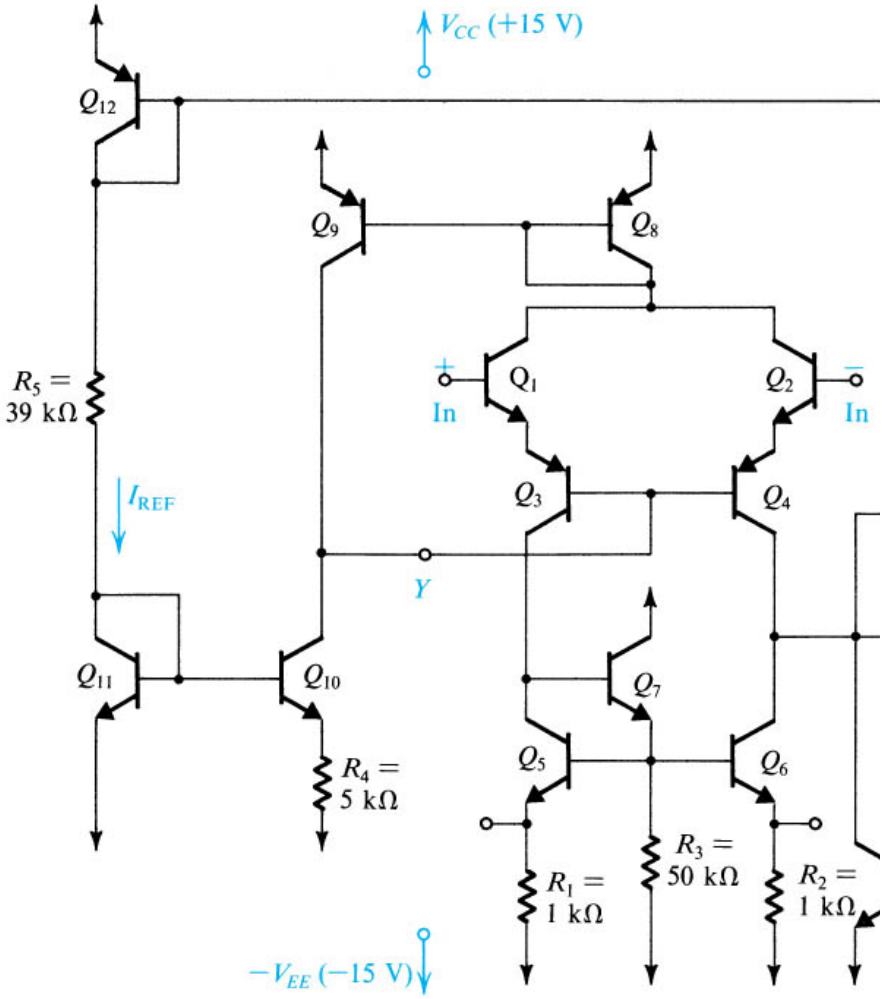
- Q23 is an emitter follower (minimized loading effect).

- Q15 and Q21 are providing short circuit protection. They are biased by R6 and R7.

LM 741 Op-Amp Circuit – National Semiconductor/Texas Instruments



DC Analysis of LM 741 Op-Amp Circuit



- Resistor R5 is the reference resistor
- I_{Ref}, the current in R5 is

$$I_{Ref} = \frac{V_{CC} - 0.7 - 0.7 - (-V_{EE})}{R_5}$$

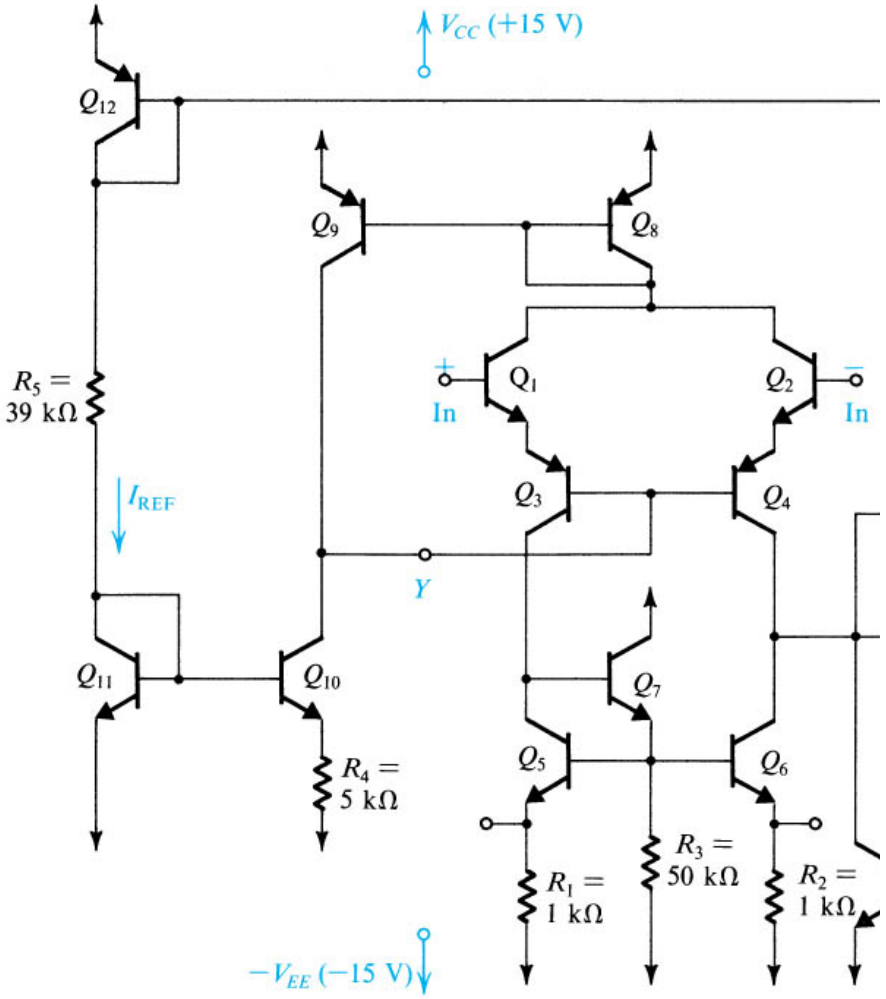
or, I_{Ref} = 0.73 mA

- Q10 and Q11 form a Widlar current source
- Using the current equation

$$I_o R_E = V_T \ln\left(\frac{I_{Ref}}{I_o}\right)$$

- We have, I_{10} = 19 μA
- None of your exam questions will require solving this equation

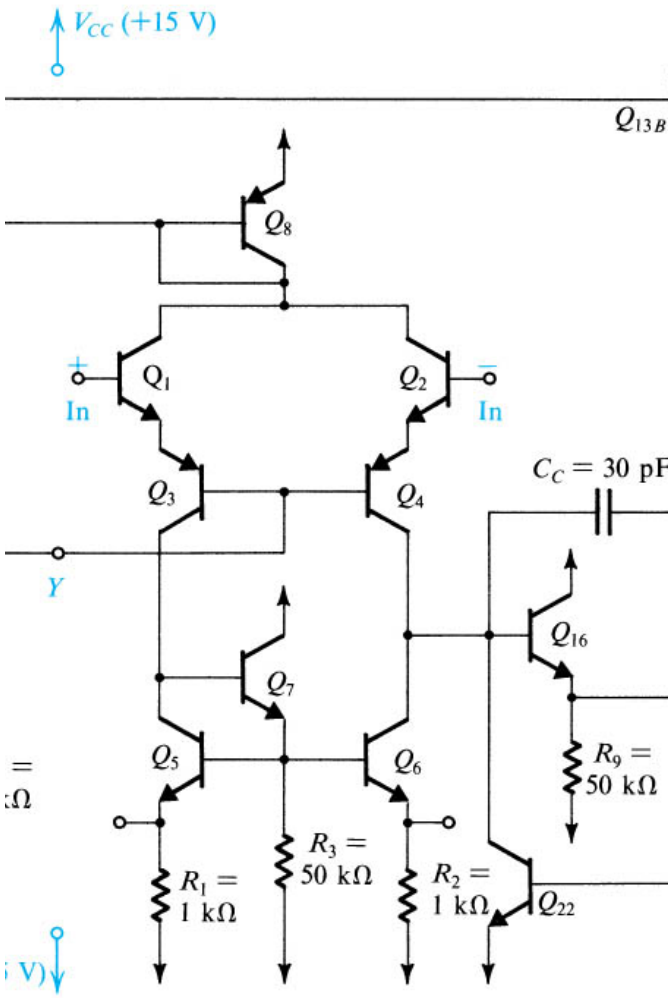
DC Analysis of LM 741 Op-Amp Circuit (Continued …)



- Here, $I_{C1} = I_{C2}$
- Assume, $I_{C1} = I_{C2} = I$, and $I_{B1} = I_{B2} \approx 0$
- Thus, $I_{E3} = I_{E4} \approx I$

- Here, $I_{B3} = I_{B4} = \frac{I}{\beta+1} \approx \frac{I}{\beta}$
- By KCL,
  $I_{C10} = I_{C9} + \frac{2I}{\beta}$
- In practice, the term $(2I/\beta)$ is negligible compared to I_{C9}
- Thus, $I_{C10} \approx I_{C9}$
- Which yields, $2I = I_9 \approx I_{10} = 19\ \mu A$
- Thus, $I = 9.5\ \mu A$

DC Analysis of LM 741 Op-Amp Circuit (Continued …)



- Assume, the base currents $I_{B7} = I_{B16} \approx 0$
- Thus, $I_{C5} = I_{C6} \approx I = 9.5\ \mu A$

- By KCL,

$$I_{C7} \approx I_{E7} = \frac{V_{BE6}+IR_2}{R_3} + \frac{2I}{\beta}$$

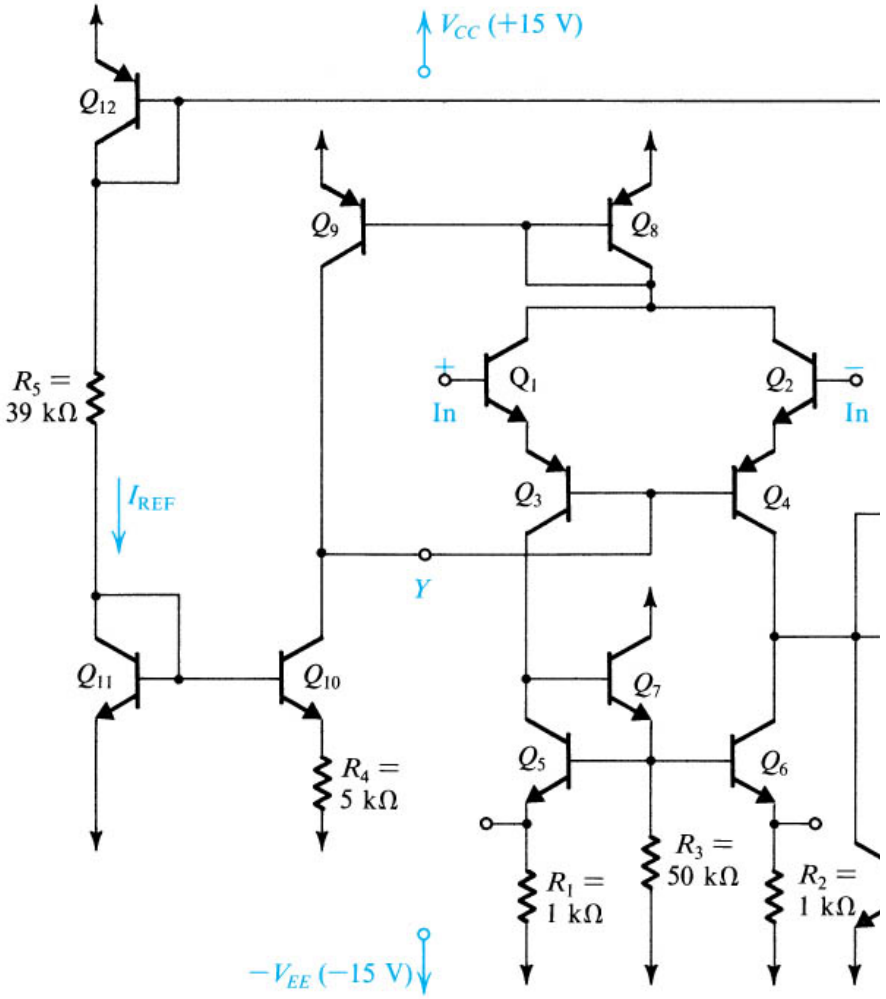
- Again, neglecting the last term ($2I/\beta$), we have,

$$I_{C7} \approx I_{E7} = \frac{V_{BE6}+IR_2}{R_3}$$

- But, $V_{BE6} = V_T ln\left(\frac{I}{I_S}\right)$, where I = 9.5 μA
- Assuming $I_S = 10^{-14}$ A, we have,
- $V_{BE6} = 0.517$ V

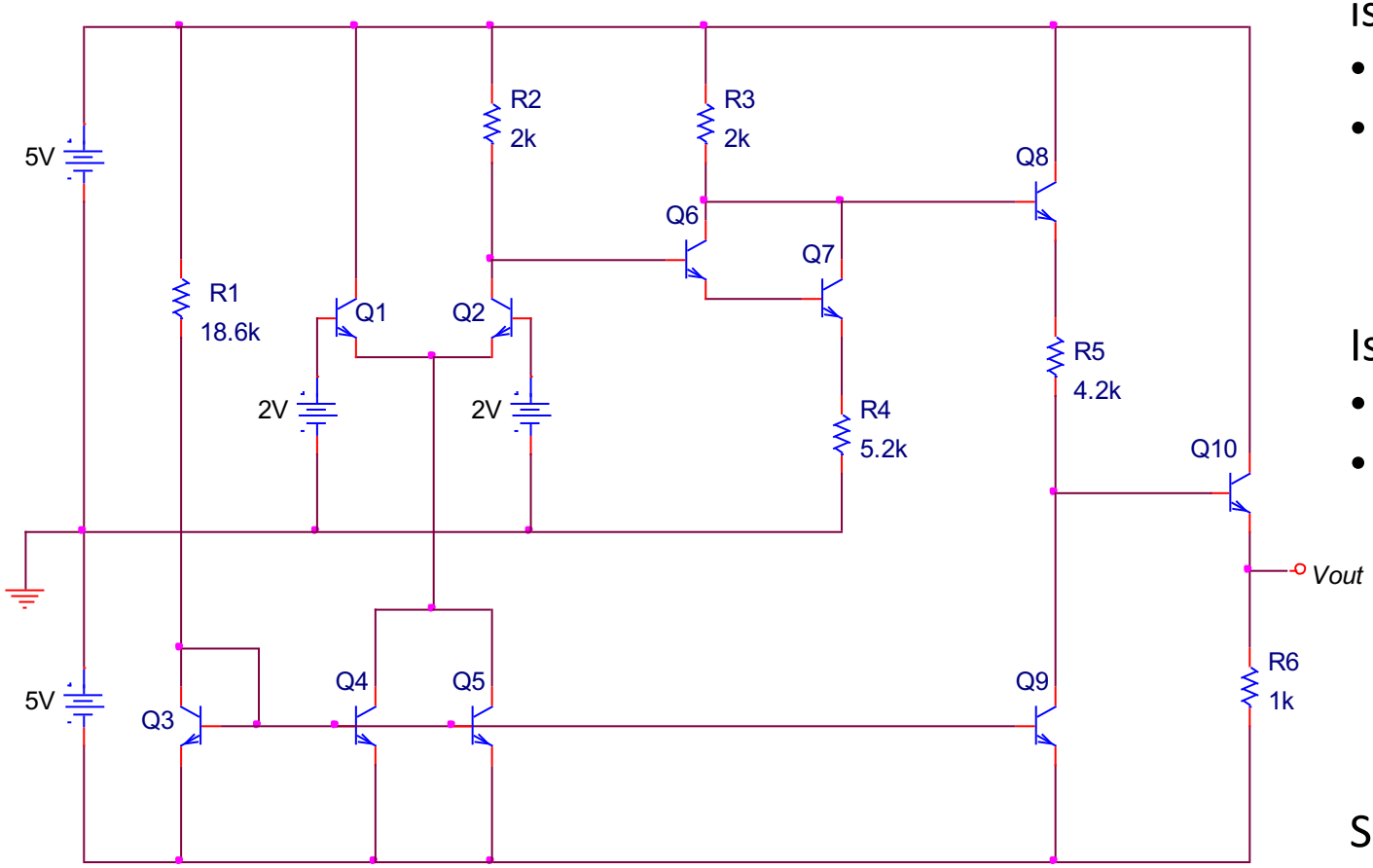
- $$I_{E7} = \frac{0.517+9.5\times10^{-6}\times1\times10^{3}}{50\times10^{3}}$$
- $I_{E7} = 10.5\ \mu A$

Current Stabilization in Q1 and Q2



- If I increases, I_{C8} will increase
- If I_{C8} increases, I_{C9} will increase
- If I_{C9} increases, I_{B3} and I_{B4} will decrease
- Reduced I_{B3} and I_{B4} will drop the current I

Upper and Lower Limits of Common-Mode Input Voltage



is there any upper limit?

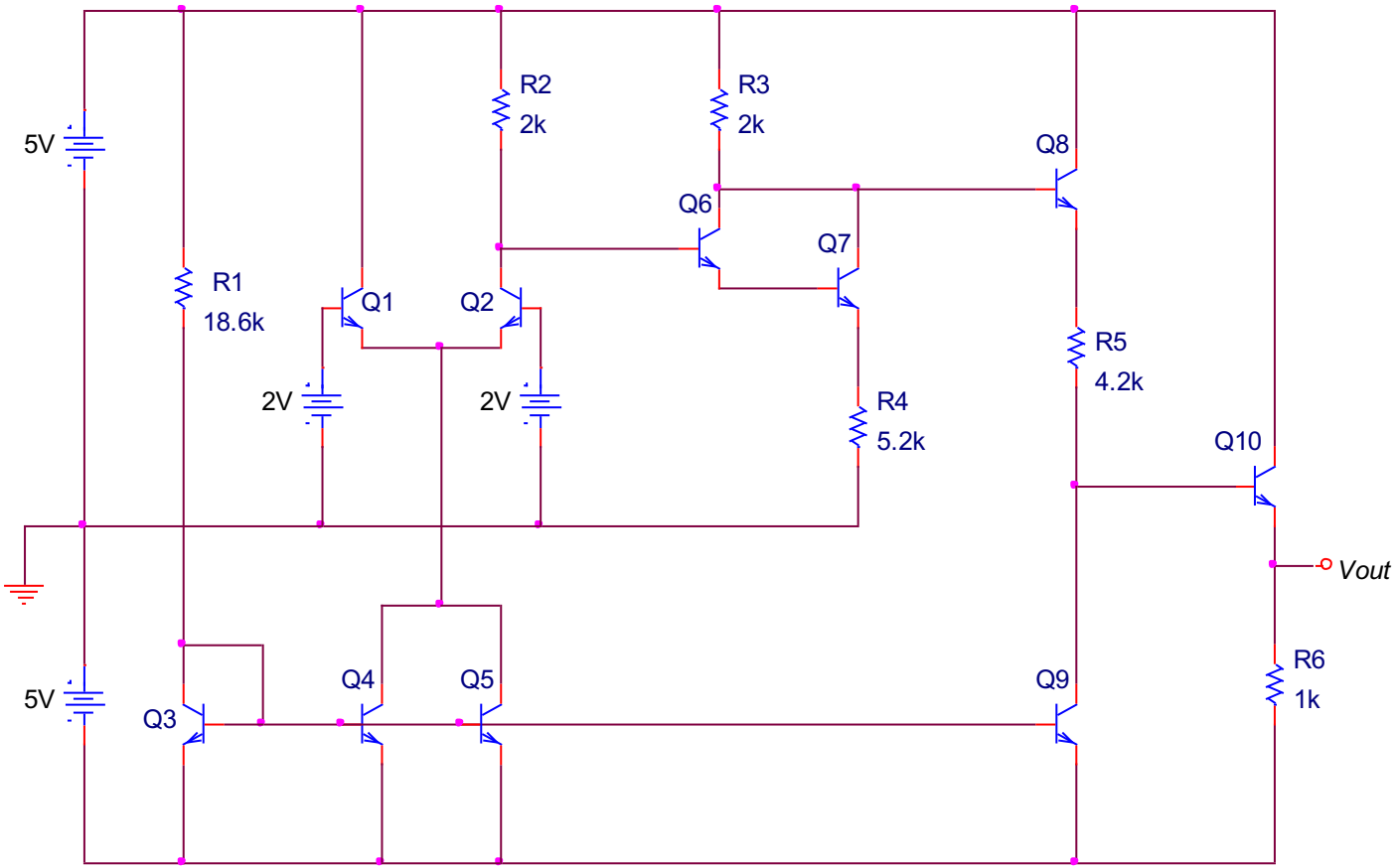
- Assume $v_{cm,in}$ = 100 V
- Do you see any problem?

Is there any lower limit?

- Assume $v_{cm,in}$ = -100 V
- Do you see any problem?

So, there are both upper and lower limits

Determining Upper Limit



We know the transistors forming differential pair and current source including current steering circuits **must remain in active region**.

$V_{cm,in(max)} = V_{C1} - V_{CB1(min)}$

By KVL,

$V_{CE1} = V_{CB1} + V_{BE1}$

For the upper limit,

$V_{CE1(sat)} = V_{CB1(min)} + V_{BE1(on)}$

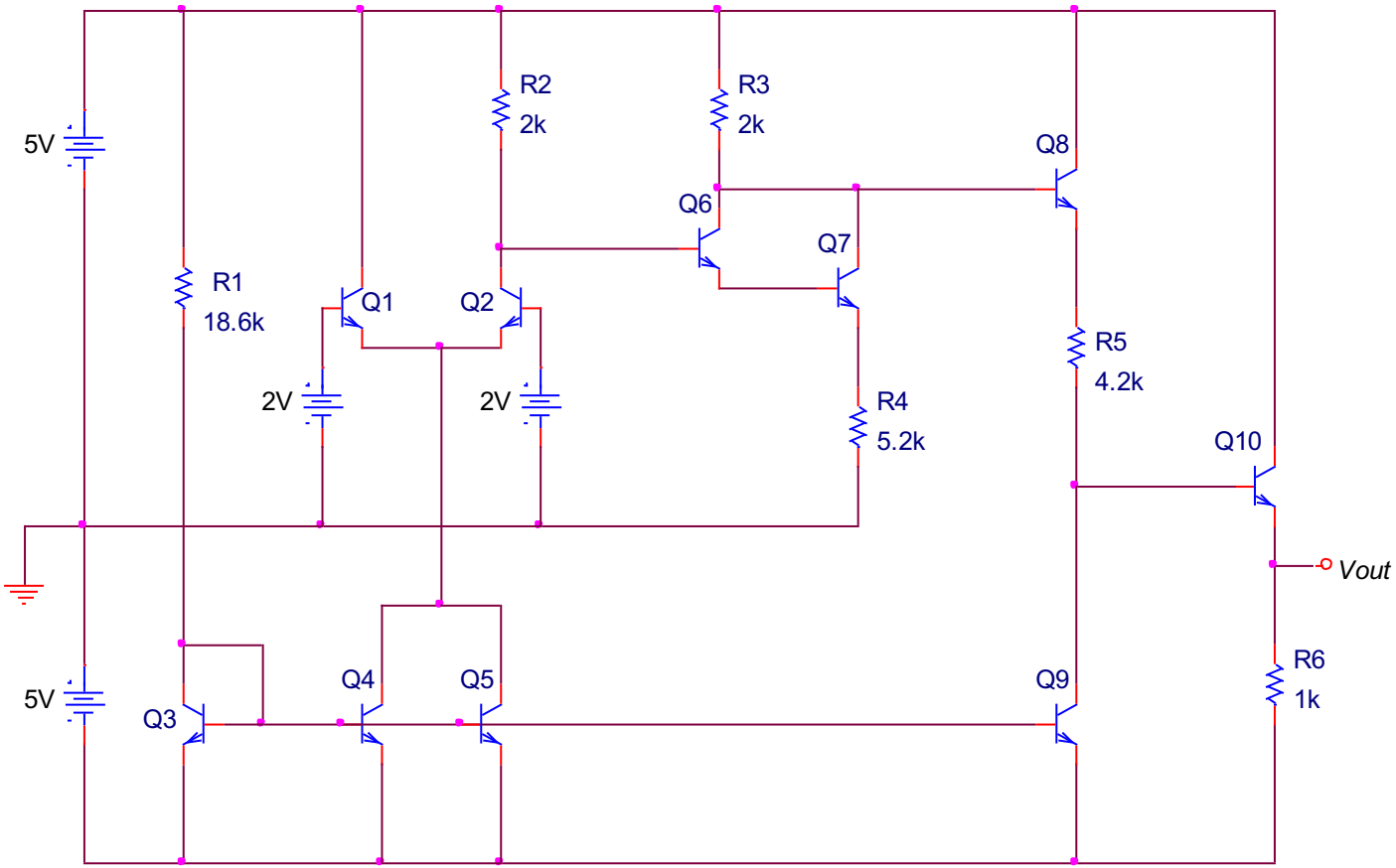
or, $V_{CB1(min)} = 0.2 - 0.7 = -0.5$ V

Thus,

$V_{cm,in(max)} = 5 - (-0.5)$

or, **$V_{cm,in(max)} = 5.5$ V**

Determining Lower Limit



We know the transistors forming differential pair and current source including current steering circuits **must remain in active region**.

$$V_{cm,in(min)} = V_{BE(on)} + V_{CE5(min)} - V_{CC}$$

or, $V_{cm,in(min)} = V_{BE(on)} + V_{CE5(sat)} - V_{CC}$

or, $V_{cm,in(min)} = 0.7 + 0.2 - 5$

or, $\mathbf{V_{cm,in(min)} = -4.1\ V}$