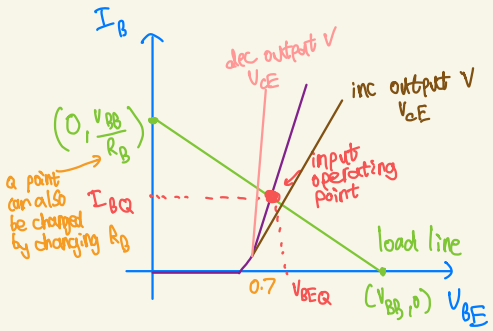
Operating points

input → coordinates obtained by intersection of load-line with transistor input characteristics for a particular value of output voltage V_{CE}

* important for setting amplification

input characteristics of CE

similar to fwd bias characteristics of pn junction

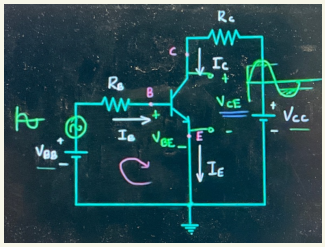


input operating point $Q\text{-pt} = (V_{BEQ}, I_{BQ})$

$\text{slop} = -\frac{1}{R_B}$

- increasing R_B will cause slope to decrease and vice versa

Apply KVL in input loop



$+V_{BB} - I_B R_B - V_{BE} = 0$

I_B = y, V_{BE} = x

$P_1 = (0, \quad)$ $\quad P_2 = (\quad, 0)$

find these values

$V_{BE} = 0$

$I_B = \frac{V_{BB}}{R_B}$

$I_B = 0$

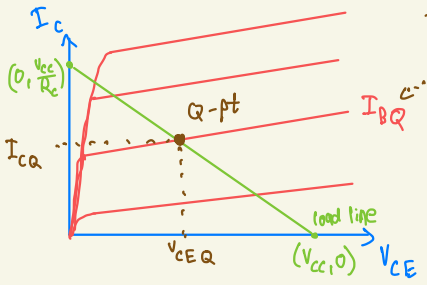
$V_{BE} = V_{BB}$

$\therefore \quad P_1 = (0, \frac{V_{BB}}{R_B}) \quad P_2 = (V_{BB}, 0)$

use P_1 and P_2 to plot load line

output Q point

- intersection of load line with transistor output characteristics for particular value of I_B



- have to consider particular base current

* changing base current will shift operating point

apply KVL in output loop

$+V_{CC} - I_C R_C - V_{CE} = 0$

I_C = y, V_{CE} = x

$\text{slope} = -\frac{1}{R_C}$

$V_{CE} = 0$

$I_C = \frac{V_{CC}}{R_C}$

$P_1 = (0, \frac{V_{CC}}{R_C})$

$I_C = 0$

$V_{CE} = V_{CC}$

$P_2 = (V_{CC}, 0)$

- if Q point is near saturation or cutoff the signal will be distorted

- Q point at middle will allow it to have max swing without distortion

nesO academy at 14:00

9/28/21

Transistor Load-Line

By writing KVL at the collector circuit, we have,

$V_{CC} = I_C \times RC + V_{CE}$

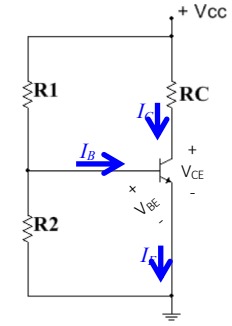
straight line equation

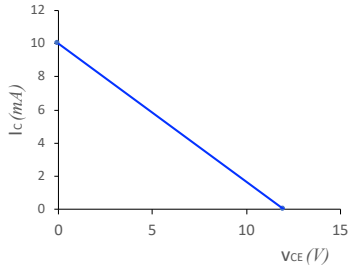
or, $I_C = (-1/RC) \times V_{CE} + V_{CC}/RC$

$y = m \times + c$

This is an equation of straight line in V_{CE}-I_C plane with slope = $(-1/RC)$ and intercept = (V_{CC}/RC).

This straight line as shown below is called load-line of a transistor





Set, $V_{CC} = 12$ V and $RC = 1.2$ kΩ

At $I_C = 0$, $V_{CE} = V_{CC} = 12$ V

At $V_{CE} = 0$, $I_C = V_{CC}/RC = 10$ mA

This gives the load-line for this circuit, which depends on biasing.

1

* β value of 2 transistors are rarely the same

- Once Q point is fixed it shouldn't change with change in I_C

I_C could change in 2 cases:

- change in β

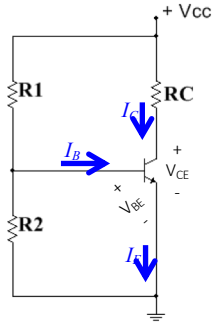
$I_C = \beta I_B$

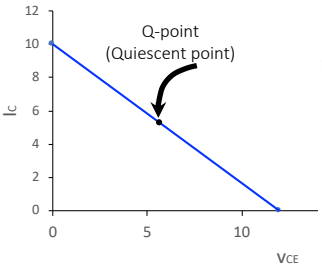
- change in temp

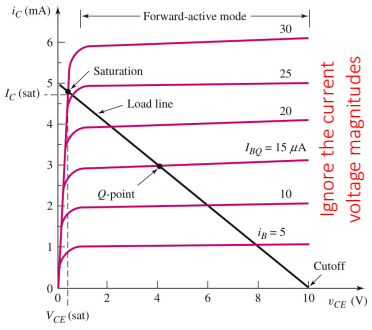
$I_C = \beta I_B + (\beta+1) I_{CBO}$

leakage current that changes on minority charge carriers which is affected by temp

Q-Point or Operating Point



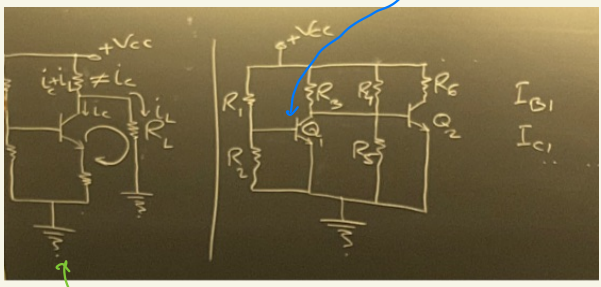




- In active region, a transistor is biased to have a certain V_{CE} and I_C. This is called the operating point or Q-point, which is a point in the V_{CE}-I_C plane.
- For a given biasing condition (design) the Q-point must lie on the load-line
- Note that the load-line and Q-point both are obtained from the same KVL equation.

2

some assignment problems?



-always start with 1st transistor when solving

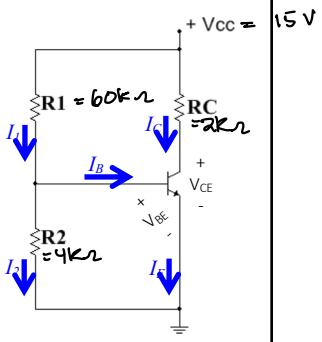
write 2 KVL equations

Learned:
- load line
- operating point

* Voltage divider bias

Load-Line and Q-Point: Example

Example: In the given circuit, $V_{CC} = 15$ V, R1 = 60 kΩ, R2 = 4 kΩ, RC = 2 kΩ, and $\beta = 65$. Draw the load-line for this circuit and indicate the Q-point on it.



Soln: Here, $I_1 = [V_{CC} - V_{BE(on)}]/R1$

$I_1 = 238.3\ \mu A$

and, $I_2 = V_{BE(on)} / R2 = 175\ \mu A$

Thus, $I_B = I_1 - I_2 = 63.3\ \mu A$

We know, $I_C = \beta \times I_B = 4.11$ mA

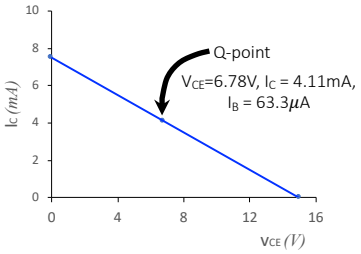
By KVL, $V_{CE} = V_{CC} - I_C \times R_C = 6.78$ V

For load-line, use the above KVL equation

At $I_C = 0$, $V_{CE} = V_{CC} = 15$ V and

at $V_{CE} = 0$, $I_C = V_{CC} / RC = 7.5$ mA

Thus, the Q-point is at $V_{CE,Q} = 6.78$V, $I_{C,Q} = 4.11$ mA, and $I_{B,Q} = 63.3\ \mu A$



① find I_C and V_{CE}

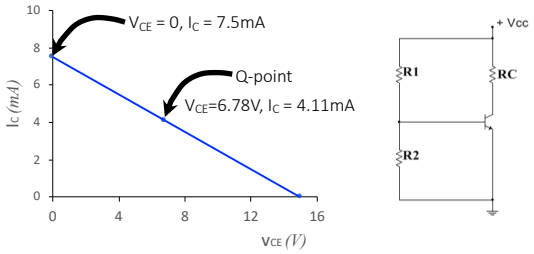
② find load line points

$I_2 R_2$

$V_{CC} - I_1 R_1 - V_{BE(on)} = 0$

Load-Line and Maximum Collector Current

We have just obtained this load-line with $V_{CC} = 15$ V, R1 = 60 kΩ, R2 = 4 kΩ, RC = 2 kΩ, and $\beta = 65$.

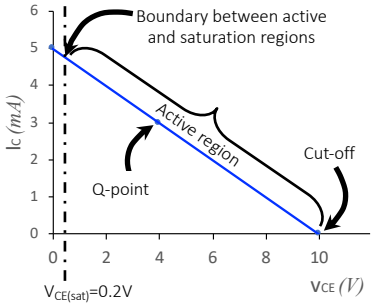


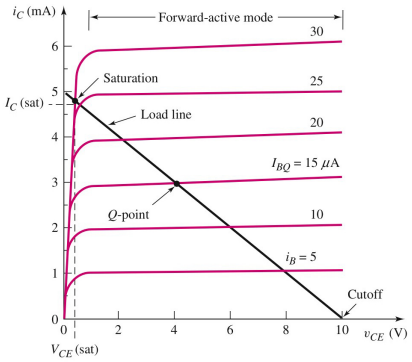
- Notice that the maximum collector current $I_{C(max)}$ cannot be 7.5 mA
- $I_{C(max)} = (V_{CC} / RC) - V_{CE(sat)}$ $\quad [I_{C(max)} \neq (V_{CC} / RC)]$
- For the purpose of obtaining the load-line, we can assume a point on the I_C-axis, where $I_{C(max)} = (V_{CC} / RC)$ is applicable
- In actual circuit, the operating point cannot be on the I_C-axis because $V_{CE(sat)} = 0.2$ V, and this vale cannot be zero
- The figure in the next slide illustrates it clearly

because V_{CE} can't be zero

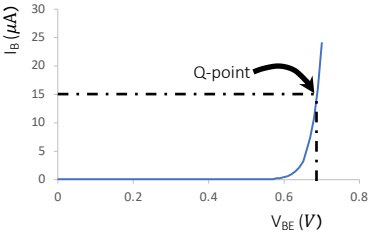
4

Load-Line and Maximum Collector Current (Continued…)





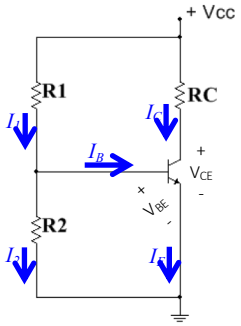
- Q-point can be adjusted (by changing biasing) at any point on the load-line in the active region
- Q-point sets operating base current ($I_{B,Q}$) and base-emitter voltage ($V_{BE,Q}$) as well



Load-Line: Example

Gain a Deeper Understanding (GADU)

Example: In the given circuit, V_{CC} = 8 V, R1 = 73 kΩ, R2 = 14 kΩ, RC = 0 Ω, and β = 80. Draw the load-line for this circuit and indicate the Q-point on it.



Soln:

Solve it based on the discussion in lecture

$+V_{CC} - I_1 R_1 - V_{BE(on)} = 0$

$I_1 = \frac{V_{CC} - V_{BE(on)}}{R_1} = \frac{8 - 0.7}{73\,k\Omega} = 100\,\mu A$

$I_2 = \frac{V_{BE(on)}}{R_2} = \frac{0.7}{14k\Omega} = 50\,\mu A$

$I_B = I_1 - I_2 = 50\,\mu A$

$I_C = \beta I_B = 4mA$

By KVL in output loop

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C$

$= 8 - (4mA \times 0) = 8$

$V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C}$, $(0, \infty)$

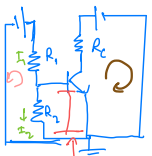
$I_C = 0$, $V_{CE} = V_{CC}$, $(8, 0)$

huh??

$I_E = I_B + I_C$

$I_1 = I_B + I_2$

$V_{BE(on)} = I_2 R_2$



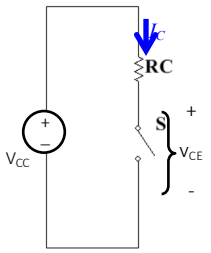
V across V_{BE} = $I_2 R_2$

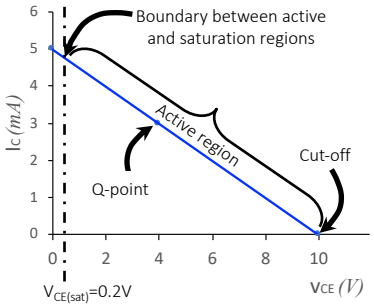
Fri Sep 29th

- he always makes quizzes based on what he taught in class

must operate in cutoff or saturation

Transistor as a Switch





- Consider this simple resistive circuit with an ideal switch S
- When the switch is OFF (open)
  $I_C = 0, V_{CE} = V_{CC}, V_{RC} = 0$
- When the switch is ON (short)
  $I_C = V_{CC}/RC, V_{CE} = 0, V_{RC} = V_{CC}$

- Consider a transistor load-line
- At cut-off,
  $I_C = 0, V_{CE} = V_{CC}, V_{RC} = 0$
  (Similar to an OFF switch)
- At saturation,
  $I_C \approx V_{CC}/RC, V_{CE} = 0, V_{RC} \approx V_{CC}$
  (Similar to an ON switch)

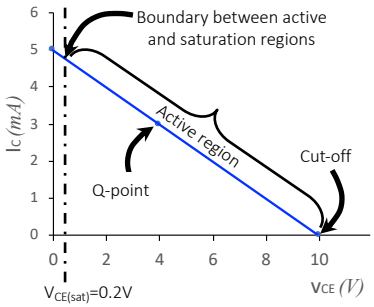
7

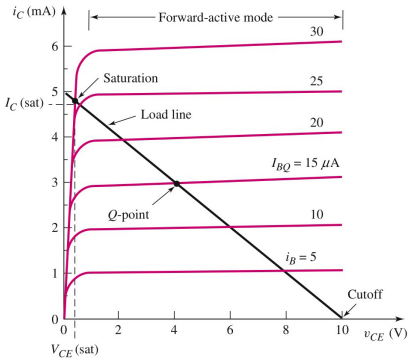
Switch dissipates no power

Is Transistor an IDEAL Switch

might come in quiz *

- $V_{CE(SAT)}$ is the voltage drop across "switch"





At cut-off,

- $I_B = 0$, but $I_C \neq 0$
- $I_C = I_{CBO}$ = leakage current
- The value of I_{CBO} is very low and it can be easily neglected

always there

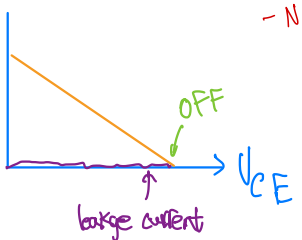
due to minority carriers

At saturation,

- $V_{CE} \neq 0$
- $V_{CE} = V_{CE(sat)} = 0.2$ V
- Power loss = $V_{CE(sat)} \times I_C$
- Count this in circuit design

8

- Non ideal factor is more dominant in "ON" than "OFF". Due to 0.2V drop.

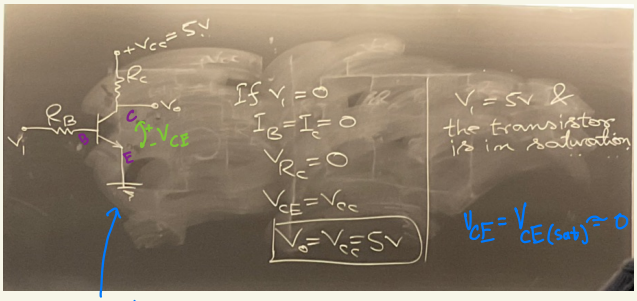


→ An ideal switch should not have current flowing when off, but above we have a leakage current

→ we shouldn't have voltage drop in on condition for an ideal switch but we do have, there is a power loss.

by changing V_i from 0 to 5:

$0 \rightarrow 1 \rightarrow 0 \rightarrow 1$



transistor is off

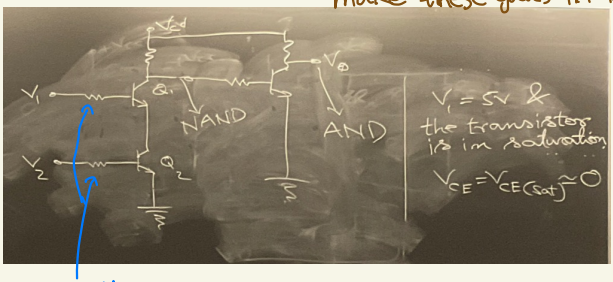
for CE, everytime in saturation it's a NOT gate

If
- $V_i \rightarrow$ high, $V_0 \rightarrow$ low
- $V_i \rightarrow$ low, $V_0 \rightarrow$ high

looks like NOT gate

$$R_B = \frac{V_i - 0.7}{I_{B(max)}} \simeq \frac{V_{CC}}{R_C}$$

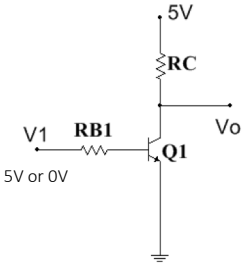
will be asked to make these gates in lab



use the same R_B values

*Come back to lectures 8-10

Transistor Switching Circuit and NOT Gate



V1 (Volt)	V1 (Logic)	Vo (Volt)	Vo (Logic)	Mode of operation
5	1	≈ 0	0	Saturation
0	0	5	1	Cut-off

NOT Gate

NOT Gate → V_i → high, V_o → low; V_i → low, V_o → high

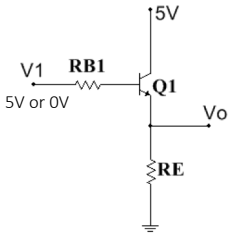
- Assume that V1 = 5 V can set the transistor in saturation
- At saturation, $V_O \approx 0V$ ($V_O = V_{CE(sat)} = 0.2\ V \approx 0\ V$)
- At V1 = 0, $V_{BE} = 0$ and $I_B = 0$; the transistor is at Cut-off
- Thus, at V1 = 0, $I_C = 0$ and $V_{CE} = V_{CC} = 5\ V$
- An input voltage at base can switch a transistor
- A transistor in CE configuration can function as a NOT gate
- Note that the transistor cannot operate in active region for switching

9

do analysis myself

Transistor Switching Circuit and NOT Gate

Gain a Deeper Understanding (GADU)



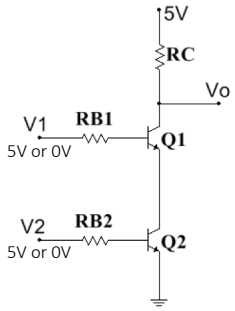
V1 (Volt)	V1 (Logic)	Vo (Volt)	Vo (Logic)	Mode of operation
5	1			Saturation
0	0			Cut-off

?? Gate

- Assume that V1 = 5 V can set the transistor in saturation
- At saturation, $V_O \approx$?
- At V1 = 0, $V_{BE} = 0$ and $I_B = 0$; the transistor is at Cut-off
- Thus, at V1 = 0, I_C = ? and V_O = ?

10

BJT Logic Gate: NAND Gate



V1 (Volt)	V2 (Volt)	Vo (Volt)	Vo (Logic)	Q1	Q2
0	0	5	1	Cut-off	Cut-off
0	5	5	1	Cut-off	Cut-off
5	0	5	1	Cut-off	Cut-off
5	5	0.4	0	Saturation	Saturation

- Higher value of V1 cannot set Q1 in saturation until Q2 turns on
- Higher value of V2 cannot set Q2 in saturation until Q1 turns on
- The two switches are in series
- This is a 2-input NAND gate

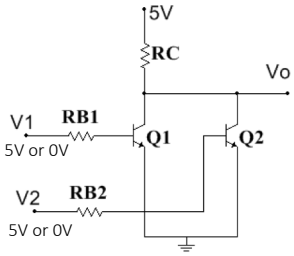
Truth table: NAND Gate

V1 (Logic)	V2 (Logic)	Vo (Logic)
0	0	1
0	1	1
1	0	1
1	1	0

11

I don't understand how these gates work

BJT Logic Gate: NOR Gate



V1 (Volt)	V2 (Volt)	Vo (Volt)	Vo (Logic)	Q1	Q2
0	0	5	1	Cut-off	Cut-off
0	5	0.2	0	Saturation	Cut-off
5	0	0.2	0	Cut-off	Saturation
5	5	0.2	0	Saturation	Saturation

- The output becomes 0.2 V if either transistor saturates
- The two switches are in parallel
- This is a 2-input NOR gate

Truth table: NAND Gate

V1 (Logic)	V2 (Logic)	Vo (Logic)
0	0	1
0	1	0
1	0	0
1	1	0

12

β = 165 in datasheet for pre-lab

BJT Logic Gate: AND and OR Gates