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Signature:

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1. DOCUMENT INFORMATION

Table 1-1: Document information

Document Information	Change Detail Summary	Document Control
Rev. No.: 00.00 Effective Date: 07-04-2022 Change Record No.: - Affected Section Ref.: All	First draft created.	Author: Lourens Janse van Rensburg, Design Engineer Reviewed By: - Approved By: -
Rev. No.: 00.01 Effective Date: 18-07-2022 Change Record No.: - Affected Section Ref.: 12.5, 0, 12.3, 12.4, 12.5.2.1.1, 11.2.1	• Updated the APPLICATION-TELEMETRY telecommand fields. • Updated the APPLICATION-COMMAND telecommand fields. • Added the NSP PEEK command description and memory map. • Added the NSP POKE command description and memory map. • Added the status register description. • Updated the redundant serial port offset.	Author: Lourens Janse van Rensburg, Design Engineer Reviewed By: - Approved By: -
Rev. No.: 00.02 Effective Date: 05-12-2022 Change Record No.: - Affected Section Ref.: See cross-refs.	• Updated Table 10-3: Power supply parameters. • Removed APPLICATION-TELEMETRY “MINIMAL”. • Removed the SYS-TELEMETRY COMMAND, replaced with APPLICATION-TELEMETRY “DIAGNOSTICS”. • Updated the versions of the Applicable Documents. • Updated Figure 5-2: Drive electronics architecture. • Updated Figure 10-4: Grounding diagram. • Updated Figure 8-1: Torque capability vs. angular momentum under vacuum . • Updated Figure 10-6: Power consumption as a function of wheel speed under vacuum conditions.	Author: Lourens Janse van Rensburg, Design Engineer Reviewed By: - Approved By: -
Rev. No.: 00.03 Effective Date: 16-03-2023 Change Record No.: - Affected Section Ref.: 5.3.3, 9, see cross-refs.	• Updated Core Logic. • Updated Control Modes. • Updated braking load switching frequency in Table 10-3: Power supply parameters. • Updated Table 12-7: Initialized Parameters detailed memory map.	Author: Lourens Janse van Rensburg, Design Engineer Reviewed By: - Approved By: -
Rev. No.: 00.04 Effective Date: 14-04-2023 Change Record No.: - Affected Section Ref.: All, see cross-refs.	• Post peer-review minor updates to various sections. • Updated Figure 5-1: Mechanical concept to include cover. • Updated Figure 5-2: Drive electronics architecture. • Updated Figure 10-4: Grounding diagram.	Author: Lourens Janse van Rensburg, Design Engineer Reviewed By: Ayoub Mbogela, Design Engineer Approved By: -
Rev. No.: 10.00 Effective Date: 17-05-2023 Change Record No.: - Affected Section Ref.: 6.7, 7.3, 7.5, 5.1, 9.4, 12.5.2, 12.5.2.1.1, 12.5.2.1.2, see cross-refs.	• Updated Mass Properties. • Updated Heat Capacity. • Temperature Reference Points. • Updated Table 2-1: Abbreviations, acronyms, symbols and definitions. • Updated the listed control modes to include the PWM Backup Mode. • Updated Figure 5-2: Drive electronics architecture. • Updated 12V Regulator switching frequency and removed start up current in Table 10-3: Power supply parameters. • Updated Figure 10-1: Overview of power supply and conversion circuitry. • Removed the connector’s manufacturer and part number from Table 10-1: Power interface connector specifications. • Added the CLEAR-FAULT command to Table 12-1: Applicable NSP command codes.	Author: Lourens Janse van Rensburg, Design Engineer Reviewed By: Gareth Gericke, Design Engineer Approved By: Braam Heyns, Quality Technician

	• Split the EXTENDED data block into TEMPERATURES, VOLTAGES and CURRENTS data blocks. • Split the DIAGNOSTICS data block into DIAGNOSTICS-GENERAL, DIAGNOSTICS-EDAC, DIAGNOSTICS-SCIA and DIAGNOSTICS-SCIB data blocks. • Removed the Temperature fields from the Table 12-13: APPLICATION-TELEMETRY STANDARD Data Block Content. • Updated the Status register contents with PSU PGOOD Flags. • Added Fault Register. • Updated the protection fields in Table 12-24: Control-mode register contents to be disabled when set high. • Added raw value to temperature conversion for the • TEMPERATURES Data Block. • Updated the RXD permissible baud rate specification in Table 10-10: 'RXD [+|-]' electrical specification. • Updated Fault (Worst case failure on secondary) current in Table 10-3: Power supply parameters. • Updated the Supply Voltage: Continuous specification in Table 10-3: Power supply parameters. • Updated idle power consumption in Table 10-3: Power supply parameters.	
Rev. No.: 10.01 Effective Date: 12-10-2023 Change Record No.: CR-057-2023 Affected Section Ref.: 8.1, 8.2, 8.3, 8.4, 8.5, 9.4, 9.5, 10.1.5, 10.1.7, 0, 12.5.2.1.1, 12.5.2.1.2, 12.5.2.7, 12.5.2.8, 12.6.1, 12.7, 12.8, 12.9	• Updated the Status register contents order and Motor Direction bit polarity. • Replaced the Status register Drive Quadrant bit with Drive polarity. • Added overspeed fault and other limited flags to Fault register. • Updated CLEAR-FAULT Command description to indicate the selective flag clearing. • Updated Control-mode setpoint to 32-bit from 16-bit. • Replaced the protection disable fields in the Control-mode register with the CONFIGURE-PROTECTION command. • Added PWM Control Mode (Backup Mode) section. • Added Protection Mechanisms section, including the Hard Protection Mechanisms and Soft Protection Mechanisms. • Removed placeholder INIT Command [0x01] section. • Moved contents into new document template. • Added in-rush current characterization. • Added torque controller steady-state error. • Added torque controller zero crossing performance. • Increased the fraction bits of the "Speed measurement" field in the APPLICATION-TELEMETRY STANDARD data block to 8 from 4. • Removed CRC calculation code snippet. • Updated motor drive output power limit. • Updated DIAGNOSTICS-SCIA and DIAGNOSTICS-SCIB field number 3 description to NSP messages received count. • CONFIGURE-PROTECTION and TRIP-LCL COMMAND sections added. • Updated Fault, Peak and Idle current in Table 10-3: Power supply parameters. • Updated Table 12-7: Initialized Parameters detailed memory map. • Updated PEEK/POKE NSP command accessible address range. • Updated Figure 8-1: Torque capability vs. angular momentum under vacuum and ambient pressure conditions. • Updated Figure 10-7: Power consumption as a function of angular momentum under vacuum conditions • Updated Table 10-4: NRWA-T6 power consumption specification under vacuum conditions. • Added Figure 10-5 Peak power consumption and reaction torque over momentum under vacuum and ambient pressure conditions.	Author: Lourens Janse van Rensburg Design Engineer Matthew Milne Technical Writer Reviewed By: Gareth Gericke Design Engineer Approved By: Braam Heyns Quality Technician

		• Updated Figure 8-2: Torque availability and power consumption vs. angular momentum for multiple drive power limits under ambient pressure conditions. • Added Figure 10-6: Power consumption as a function of wheel speed under vacuum conditions, Figure 10-8: Power consumption as a function of wheel speed under ambient pressure conditions, Figure 10-9: Power consumption as a function of angular momentum under ambient pressure conditions	
Rev. No.: 10.02	Effective Date: 18-12-2023	• Added additional MICD document number for NRWA-T6-B. • Updated RS485 multi-drop bus scheme to RS485 point-to-point scheme for NRWA-T6-B. • Added termination resistors for NRWA-T6-B.	Author: Phillip Booysen Senior Mechanical Design Engineer Gareth Gericke Design Engineer
Change Record No.: CR-121-2023			Reviewed By: Lourens Janse Van Rensburg Design Engineer
Affected Section Ref.: 4.1, 5.3.3, 10.2.7.1			Approved By: Braam Heyns Quality Technician

2. ABBREVIATIONS, ACRONYMS, SYMBOLS AND DEFINITIONS

Table 2-1: Abbreviations, acronyms, symbols and definitions

Term	Meaning
AD	Applicable Document
ADC	Analog to Digital Converter
CRC	Cyclic Redundancy Check
CTE	Coefficient of Thermal Expansion
ECSS	European Cooperation for Space Standardization
EDAC	Error Detection and Correction
EMF	Electromagnetic Field
ESD	Electrostatic Discharge
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
GND	Ground (Electrical)
ICD	Interface Control Document
JTAG	Joint Test Action Group
LCL	Latching Current Limiter
MICD	Mechanical Interface Control Document
MWA	Momentum Wheel Assembly
NSP	Nanosatellite Protocol
NTC	Negative Temperature Coefficient
PCB	Printed Circuit Board
OBDH	On-Board Data Handling
OTW	Over Temperature Warning
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
RD	Reference Document

ROM	Read-Only Memory
RWA	Reaction Wheel Assembly
SECDED	Single Error Correction, Double Error Detection
SCI	Serial Communication Interface
SET	Single Event Transient
SEU	Single Event Upset
SRAM	Static Random-Access Memory
TBC	To be confirmed
TMR	Triple Modular Redundancy
WDE	Wheel Drive Electronics

3. INTRODUCTION AND SCOPE

This Interface Control Document (ICD) provides the relevant mechanical, thermal and electrical information for the NRWA-T6. It details the device's functional performance, various control modes (including protection mechanisms) and different protocol layers (including telecommands and replies).

4. DOCUMENTS

4.1 Applicable Documents

The following documents are applicable and are referred to as [ADxx] in the text. Documents are applicable in their entirety. For unspecified issues of document, the latest signed version should be used. For specified issues, subsequent amendments to or revisions of any of these publications do not apply. However, parties to the agreement based on this document are encouraged to investigate the possibility of applying the most recent issue.

Table 4-1: Applicable documents

Ref.	Document No.	Document Title
AD01	N2-A2a-DD0022	NRWA-T6 Mechanical Interface Control Document
AD02	N2-A2a-DD0029	NRWA-T6-B Mechanical Interface Control Document

4.2 Reference Documents

The following documents are referenced for supporting information only and are referred to as [RDxx] in the text. For unspecified issues of a document, the latest issue should be used. Any sections that are applicable will be referenced directly in the requirements section of this technical specification.

Table 4-2: Reference documents

Ref.	Document No.	Date	Document Title
RD01	RFC 1055	1988	A Nonstandard for Transmission of IP Datagrams over Serial Lines: SLIP
RD02	ARM DUI 0066D	1999	ARM Developer Suite AXD and armsd Debuggers Guide Version 1.2
RD03	ECSS S-ST-00-01C	2012	ECSS Systems: Glossary of terms

5. OVERVIEW

5.1 Functional Description

The NRWA-T6 reaction wheel was designed to serve as a satellite actuator. The basic principle of operation is that the momentum exchange in a closed system (in the absence of external torque) remains constant (is conserved). Any change in the speed of rotation of the reaction wheel will therefore cause the spacecraft to counter-rotate proportionally through the conservation of angular momentum. Consequently, the reaction wheel can counteract (balance) an external torque applied to the spacecraft by varying its own angular momentum. The wheel therefore "reacts" to the external torque.

The angular momentum of the driven RWA/MWA can be changed through four separate control modes:

1. Current Control Mode
2. Speed Control Mode
3. Torque Control Mode
4. PWM Control Mode (Backup mode)

Each control mode is described in more detail in Section 9.

5.2 Mechanical Concept

The reaction wheel design is built around a three-phase brushless-DC motor with built in feedback from Hall-effect and temperature sensors. To ensure reliable operation in a space environment, the overhung flywheel is supported by 2 large space rated bearings with lubricants suitable for the space environment.

To accommodate coefficient of thermal expansions (CTE) stresses, the bearing configuration consists of one fixed and one floating bearing supported by a wave spring. This allows for free expansion of the various parts that make up the flywheel rotor under various temperature conditions, while still ensuring the required preload is present on the bearings during ground operation and testing.

The mounting of the NRWA-T6 onboard electronics is done so to maximize conductive heat transfer from active electronics components to its mounting surface while maintaining its structural integrity throughout the launch environment. Communication and power are supplied to and from the electronics via the 2 main D-sub connectors.

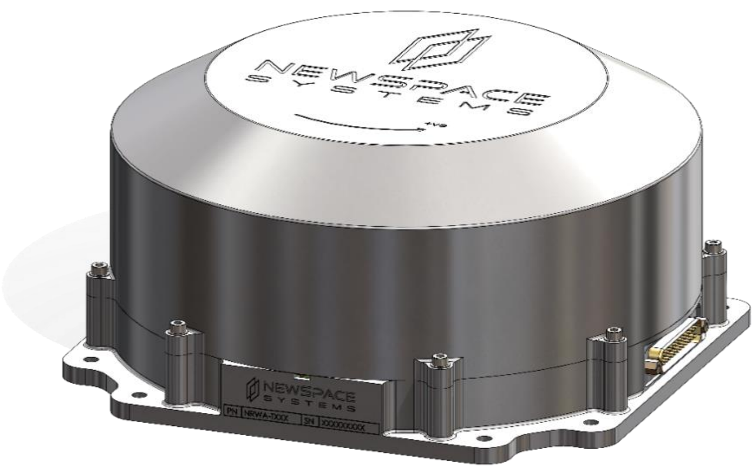


Figure 5-1: Mechanical concept

5.3 Drive Electronics Module

Figure 5-2 provides an overview of the NRWA-T6 electrical architecture. The various subsystems are characterized and described throughout this document.

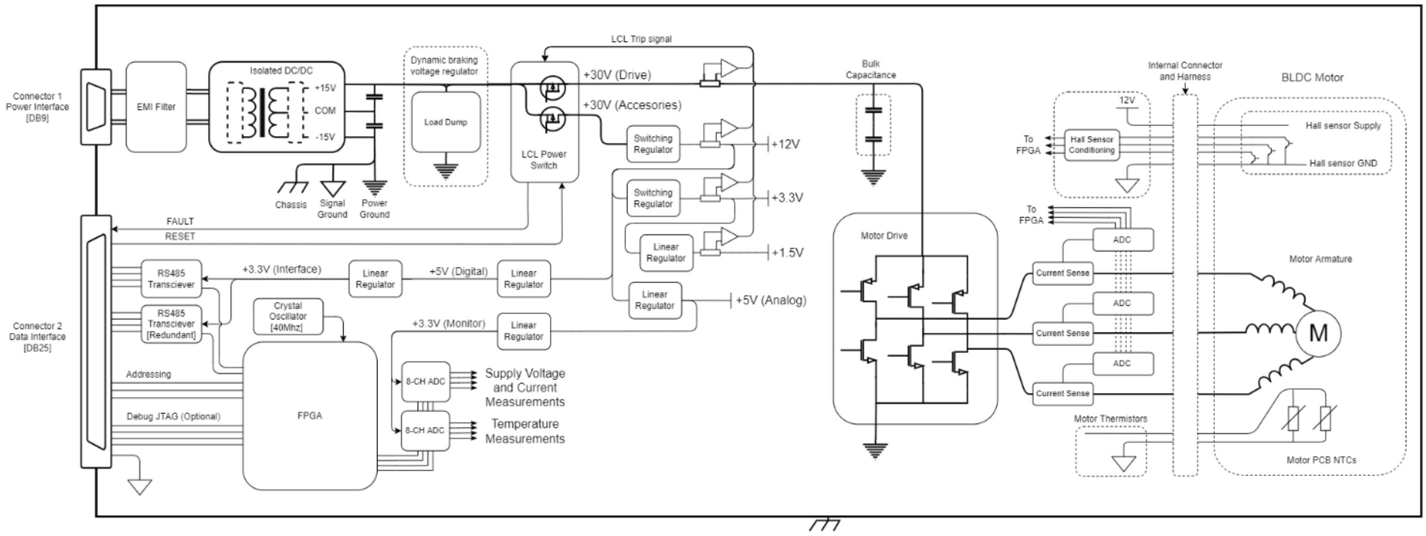


Figure 5-2: Drive electronics architecture

The reaction wheel drive electronics consist of the following major parts:

5.3.1 Motor Drive

The drive electronics commutate the brushless-DC motor by evaluating the status (feedback) of its Hall sensors. Closed-loop control of the motor speed or acceleration is implemented by measuring the motor speed from the Hall sensor feedback and varying the current flowing through the motor windings. The current flowing through the motor windings is directly measured and controlled by PWM modulation of the motor drive inverter to achieve digital closed-loop current control.

5.3.2 Power Stage

The power stage is designed to be powered from an unregulated [+28V] supply rail through the dedicated Power connector. The power conversion and conditioning stage is detailed in Section 10.1.

5.3.3 Core Logic (FPGA)

The design employs a military grade Microsemi ProASIC3 FPGA. The ProASIC3 FPGAs are based on non-volatile flash technology and are immune to configuration loss due to atmospheric neutrons (firm errors). On power up, the FPGA firmware reads the internal ROM to initialize a configuration portion of EDAC protected RAM, where it will be accessed/retrieved by the firmware during operation. The firmware makes extensive use of the EDAC protected SRAM during operation to store variables accessed by multiple firmware subsystems or by telemetry requests and commands. The EDAC implementation utilises 7-bit parity SECDED codes allowing the correction of single-bit upsets and the detection of double-bit upsets. Scrubbing of the SRAM is also performed periodically to prevent the accumulation of bit flips. Scrubbing is performed during the idle time of the SRAM access controller and does not degrade the performance or functionality of any subsystems. Both the amount of single-bit SEUs corrected and the uncorrectable double-bit SEUs detected by the EDAC implementation are recorded and available through telemetry. In core firmware subsystems, the critical registers are protected using local TMR. The FIFOs used in the dual serial transceivers are protected using Hamming codes, allowing the correction of single-bit SEUs in this subsystem. All state machines are implemented as "Safe" state machines by using one-hot encoding with invalid state reset. Separate slow and fast internal clocks are synthesized using the internal PLL, the bulk of the sequential logic in the design is driven from the slower clock to reduce the probability of SETs propagating into the sequential logic and becoming SEUs. Dual redundant full-duplex RS-485 links are implemented allowing up to 4 NRWA-T6s to be used on each RS-485 bus (refer to NRWA-T6: N2-A2a-DD0022 [AD01]). For NRWA-T6-B: N2-A2a-DD0029 [AD02], Dual redundant full-duplex RS-485 links are implemented allowing for single NRWA-T6 units to be used on each bus, as recommended, due to the added termination resistors. The communication protocol is detailed in Sections 10 to 12.

6. MECHANICAL

The mechanical interface control document (MICD) [see AD01] describes the structural/mechanical interface of the NRWA-T6. Supplementary information provided in the sections below should be considered alongside information presented in the MICD.

6.1 Dimensions

Refer to the MICD [AD01] for detailed dimensions.

6.2 Reference Frame

The design defines a right-handed orthogonal Cartesian coordinate system, aligned to the structure as per the MICD [AD01].

6.3 Mounting Interface

The intended mounting interface and hole pattern is detailed in the MICD [AD01]. The design provides eight (metric) M5-sized mounting holes. Clearances support most standard/common head types (socket, rounded, hex, etc.), as well as M5 washers sized per ISO 7089.

It is recommended to use some form of anti-rotation technology, such as safety wire (sufficient clearances provided), staking of the fastener heads, locking threaded inserts (Helicoil or similar), or appropriate locking washers.

Mounting holes are slightly undersized relative to tight/fine M5 clearance hole per ISO 724 to support alignment and mounting repeatability. The design does not provide any dedicated alignment features.

6.4 Grounding Stud

The design provides a single (metric) M4 threaded hole to be used for a grounding stud (if necessary for the application). This interface may be used to tie the chassis to a desired (ground) reference point on the satellite (if grounding through the mounting interface directly is not sufficient) or during EMC testing.

6.5 Connector Location

The positioning, alignment and orientation of the interface connector is detailed in the MICD [AD01].

6.6 Venting

The NRWA-T6 has one venting hole. The venting hole is positioned between the interface of the T6 cover and base. See Figure 5-1 for the venting hole position.

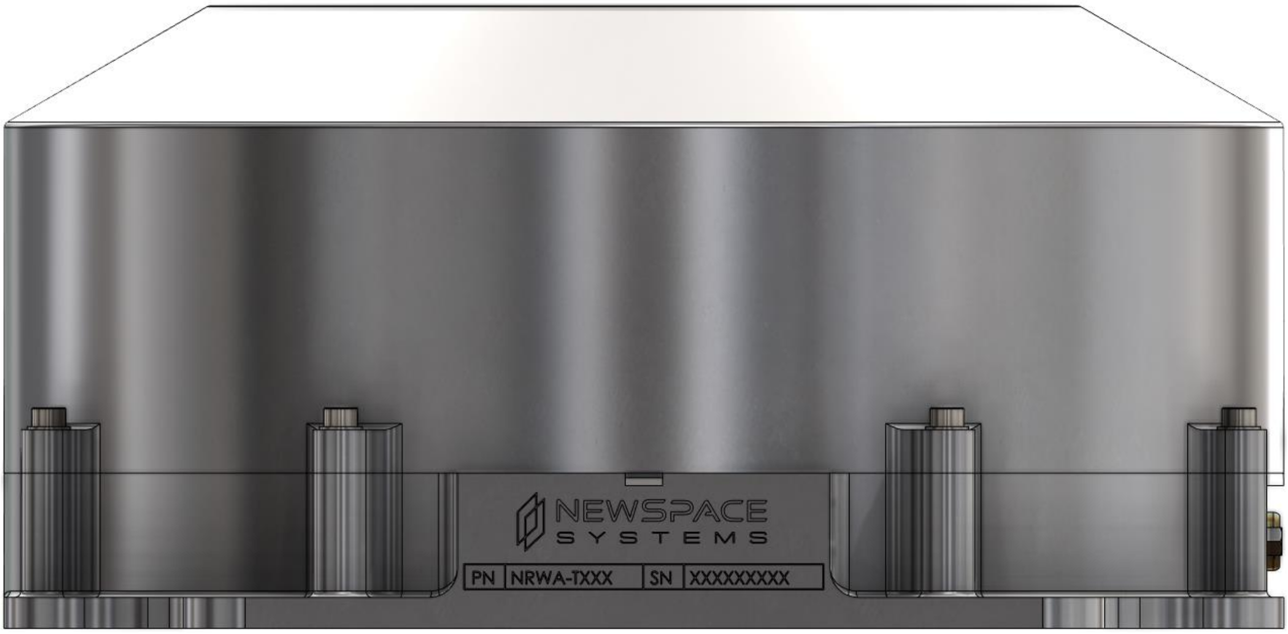


Figure 6-1: Venting hole position

6.7 Mass Properties

The mass figure detailed in the MICD [AD01] is estimated (calculated) using CAD software. Due to certain design simplifications, slight inaccuracies in material specification and manufacturing tolerances, the actual (as-built) mass often deviates from the estimated figure. The adjusted mass and allowable tolerance are detailed in Table 6-1.

Table 6-1: Mass characteristics

Property	Min	Typical	Max	Units
Design (estimated) mass	4207	4674	5141.4	g
Verification mass	-	4300[1]	-	g

[1] Measurement of original prototype (excludes lid and revised parts).

Additional mass properties (centre of mass, moment of inertia) are detailed on the MICD [AD01].

6.7.1 Markings

The NRWA-T6 assembly has two markings on the unit. The first marking is engraved and situated on the front of the unit. The marking displays the unit's part number, serial number and branding. See Figure 6-2.

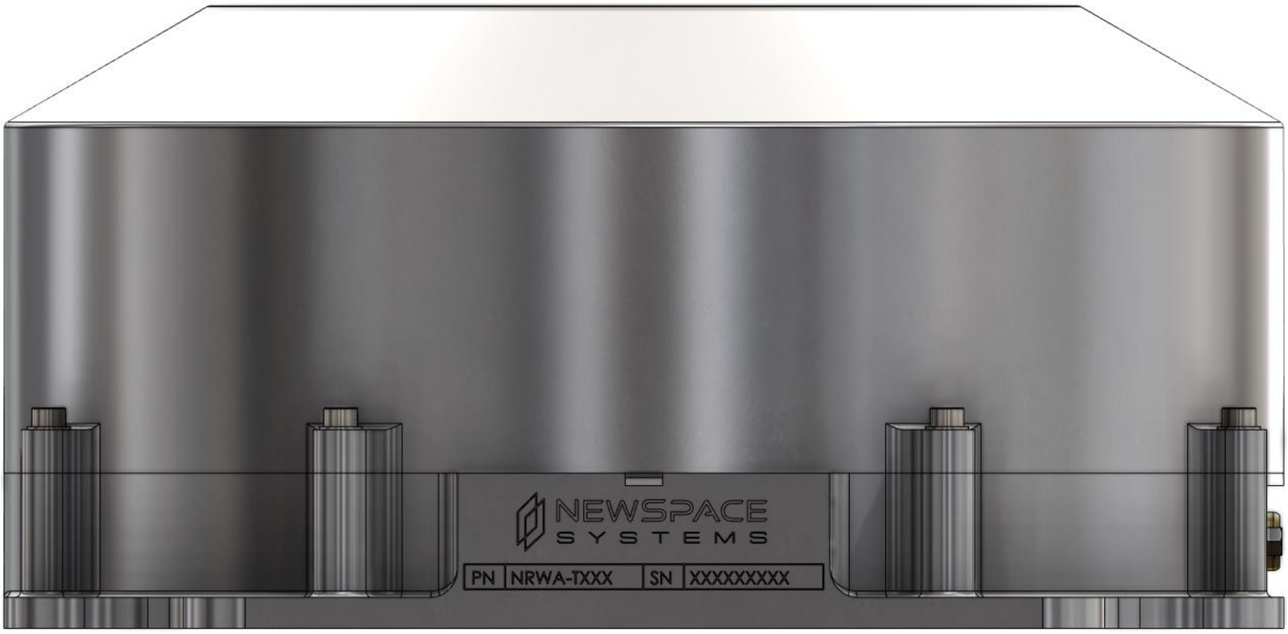


Figure 6-2: Unit front marking

The second marking is engraved and situated on the lid of the unit. The marking displays the spin orientation and branding. See Figure 6-3.

Figure 6-3: Unit cover markings

7. THERMAL

7.1 Characteristics

Table 7-1 details the thermal characteristics of the design.

Table 7-1: Thermal characteristics

Property	Minimum [°C]	Maximum [°C]
Operating Temperature	-25	+50
Survivable (Non-Op.) Temperature	-30	+55

7.2 Paths

The primary thermal path is conduction through the mounting interface. The MICD [AD01] details the contact area between the base of the unit and the spacecraft structure.

7.3 Heat Capacity

Table 7-2 details the heat capacities of the major components.

Table 7-2: Heat capacity of major components

Component	Specific [J/kg.K]	Mass [kg]	Heat Capacity [J/K]
Silicon (electronics)	700	0.1	70
Aluminium (structure)	900	1.45	1305
FR4 Laminate (PCB)	1127	0.060	68
Stainless steel (internals)	473	2.4	1135

7.4 Thermal Surface Properties

Table 7-3 details the estimated thermal surface properties of the unit. There is no thermal coating on the unit.

Table 7-3: Estimated thermal surface properties of major components

Material	Emissivity [ε]	Solar Absorptance [α]
Aluminium (structure) – SurTec 650 Passivation	0.03	0.44

7.5 Temperature Reference Points

Figure 7-1 shows the positioning of the temperature reference points relative to the reference frame origin as per [AD01].

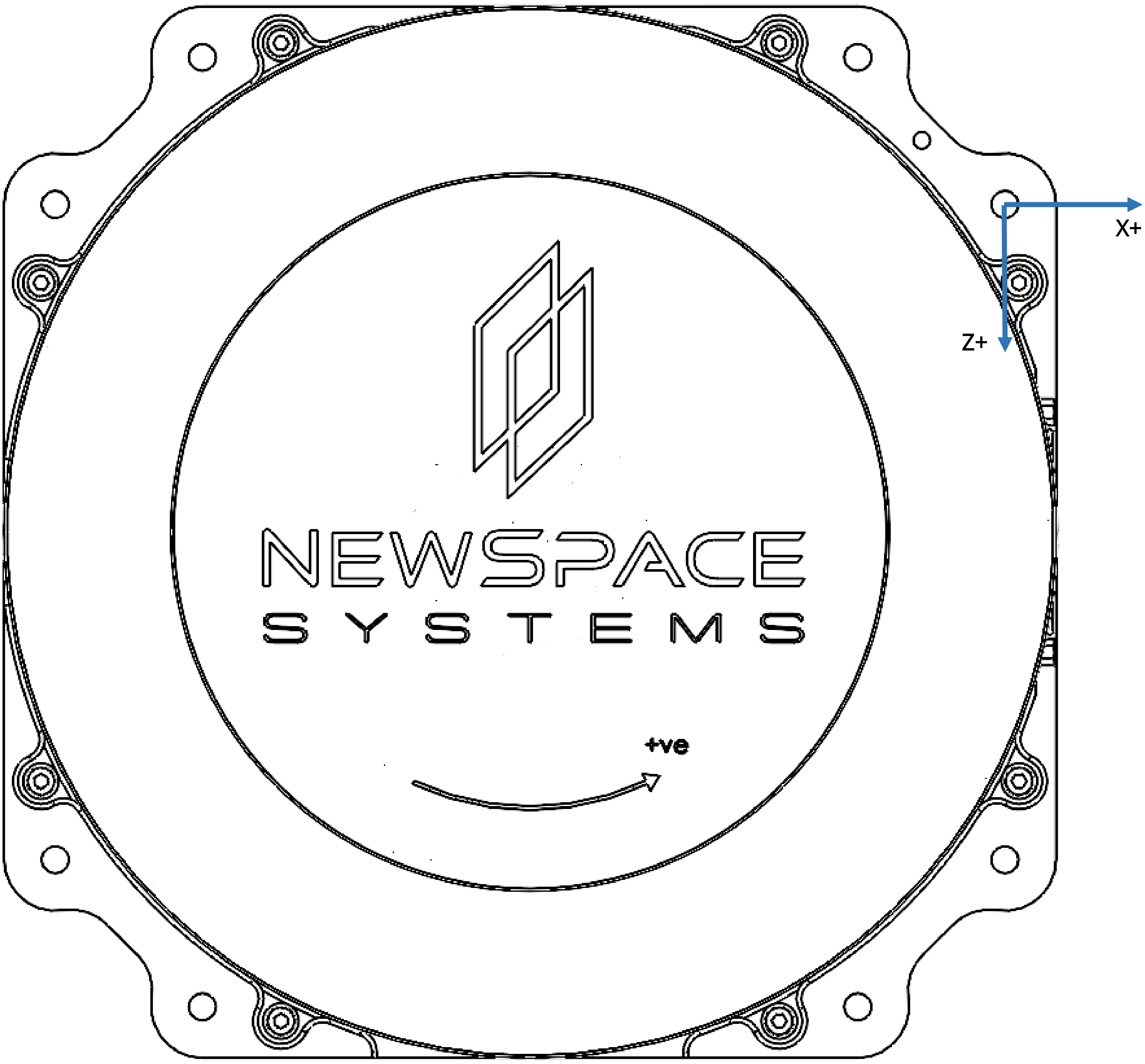


Figure 7-1: Temperature reference points

Table 7-4: Temperature reference points

Temperature Reference Number	Temperature Reference Item	Position (X,Y,Z) From Reference Point (+\- 5mm)
1	DC-DC	-142, 4, 41
2	Enclosure Temperature	-24, 9, 133
3	Motor Driver	-125, 42, 147
4	Motor	-93, 29, 86

8. FUNCTIONAL PERFORMANCE

8.1 Motor Drive Output Current and Voltage

The NRWA-T6 can drive its brushless DC motor at a maximum motor current of 6A, motor voltage of 30V and up to a maximum output power of 100W.

8.2 Performance Parameters

The torque capability of the device is defined as the torque that can be generated through acceleration/deceleration of the flywheel from an initial angular velocity. The torque capability of the NRWA-T6 at maximum current is 310mNm under vacuum conditions. The maximum speed that the motor can be driven to is 5000RPM under vacuum conditions. Figure 8-1 details the NRWA-T6 motor torque capability as a function of angular momentum for both vacuum and ambient pressure conditions.

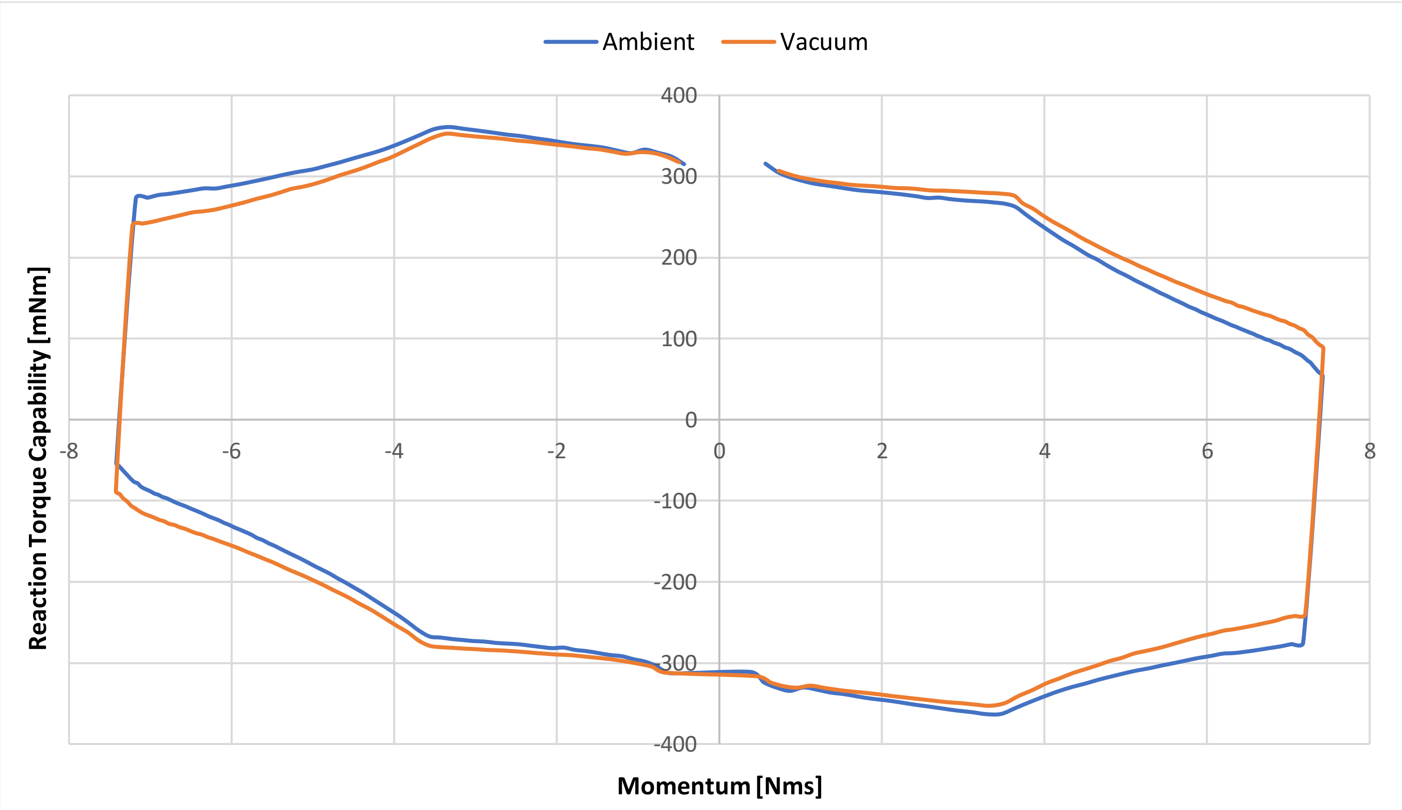


Figure 8-1: Torque capability vs. angular momentum under vacuum and ambient pressure conditions

Figure 8-1 suggests that the reaction wheel torque (angular momentum variation) capability has some normal limitation. The torque vs. angular momentum behaviour reveals a knee point at around [3.6Nms, 276mNm](Vacuum). Increasing the angular momentum above this knee point decreases the torque capabilities of the unit due to the output power limitation of the power stage. Another knee point at around [7.1Nms, 110mNm] is due to the motor back-EMF and the power stage output voltage limitation. Increasing the angular momentum above the knee point value drastically decreases the torque capabilities of the unit (down to 0mNm at maximum angular momentum). This is a natural safeguard of the wheel to avoid overspeed conditions (back-EMF limit).

8.3 Performance Parameters with an Adjusted Drive Power Limit

The motor drive output power of the NRWA-T6 can be limited to values below 100W for a use case where the peak supply current is required to be limited to below the values detailed in Table 10-3: Power supply parameters. Figure 8-2 details the NRWA-T6 reaction torque capability as a function of angular momentum for a case where the drive output power was limited to 70W compared to the nominal limit of 100W with a 28V supply.
Note that the maximum unit power draw is proportional but not equal to the motor power limit.

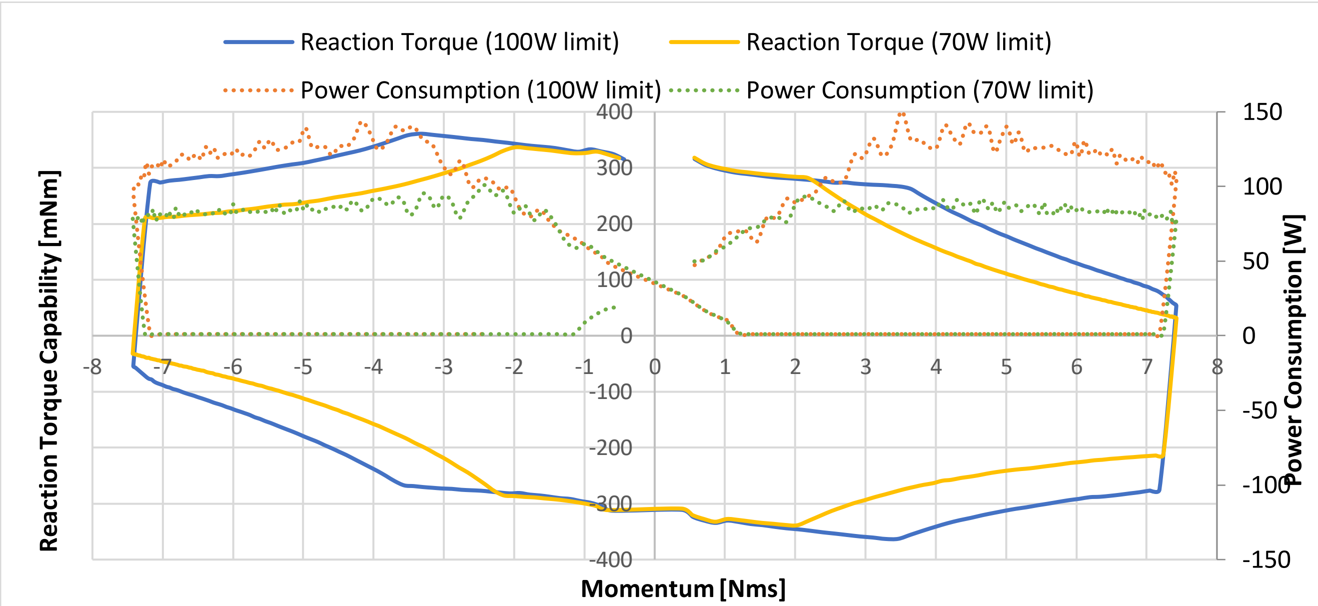


Figure 8-2: Torque availability and power consumption vs. angular momentum for multiple drive power limits under ambient pressure conditions with a 28V supply.

8.4 Torque Controller Steady-State Error

Figure 8-3 details the torque controller steady-state error after a 2000ms settling time for torque setpoint steps at various RPMs. The reaction torque is inferred from flywheel angular acceleration and the theoretical rotating inertia ($\tau = \alpha I$).

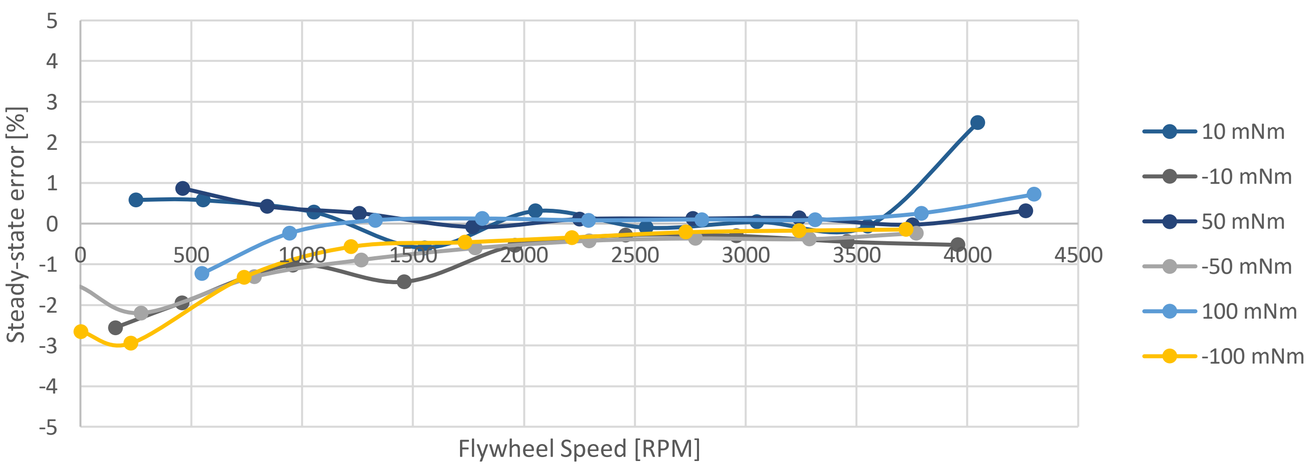


Figure 8-3: Torque controller steady-state error after 2000ms settling time for torque setpoint steps at various RPMs

8.5 Torque Controller Zero Crossing Performance

The following figures (Figure 8-4, Figure 8-5, Figure 8-6, Figure 8-7, Figure 8-8, Figure 8-9) detail the zero crossing performance of the torque controller. The data was obtained under coarse vacuum conditions. The reaction torque is inferred from flywheel angular acceleration and the theoretical rotating inertia ($\tau = \alpha I$).

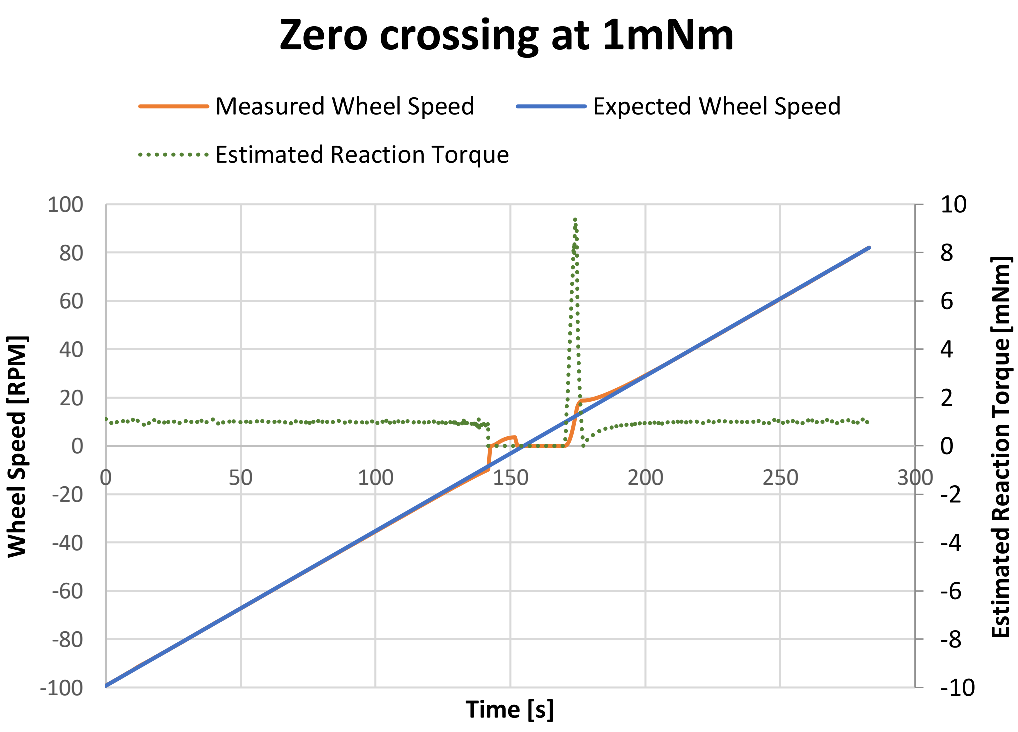


Figure 8-4: Zero crossing a 1mNm

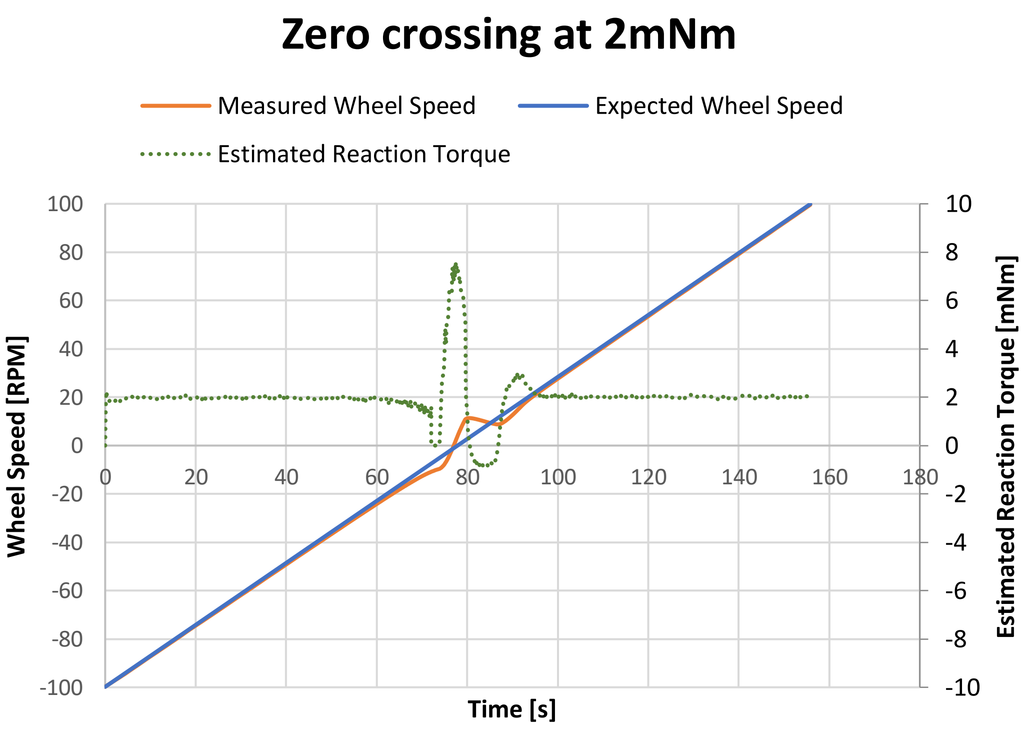


Figure 8-5: Zero crossing a 2mNm

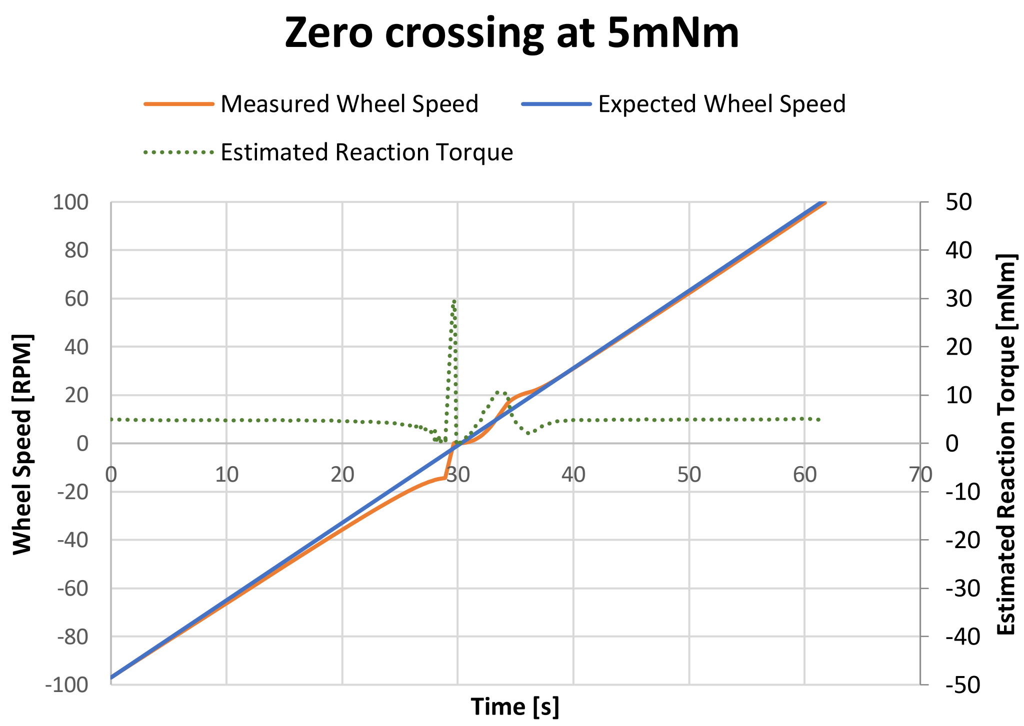


Figure 8-6: Zero crossing at 5mNm

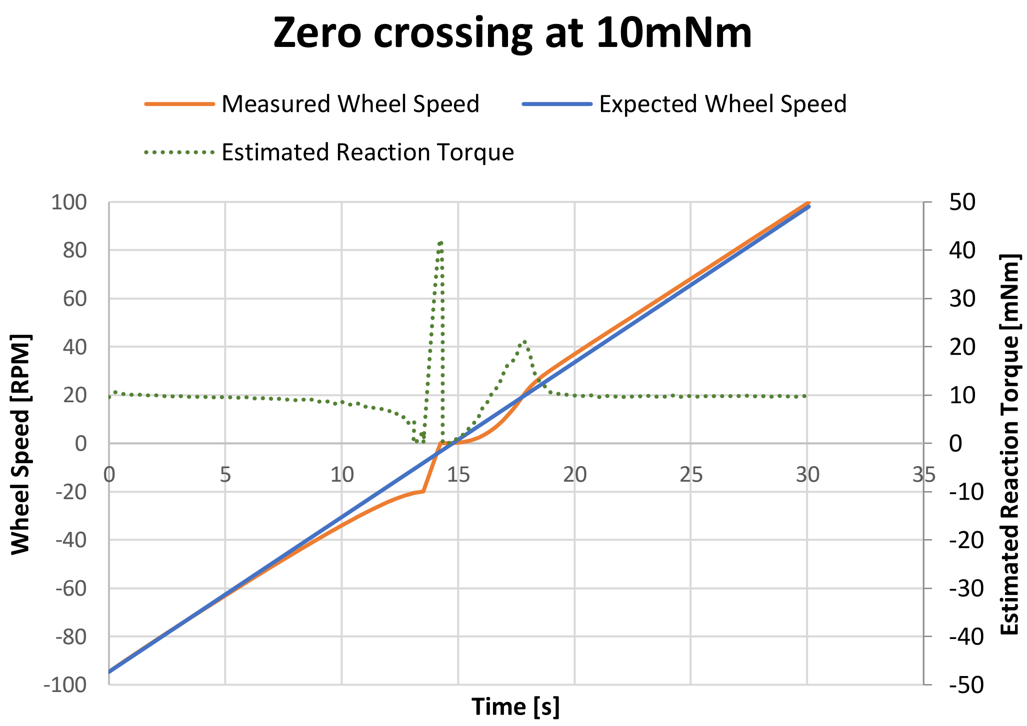


Figure 8-7: Zero crossing at 10mNm

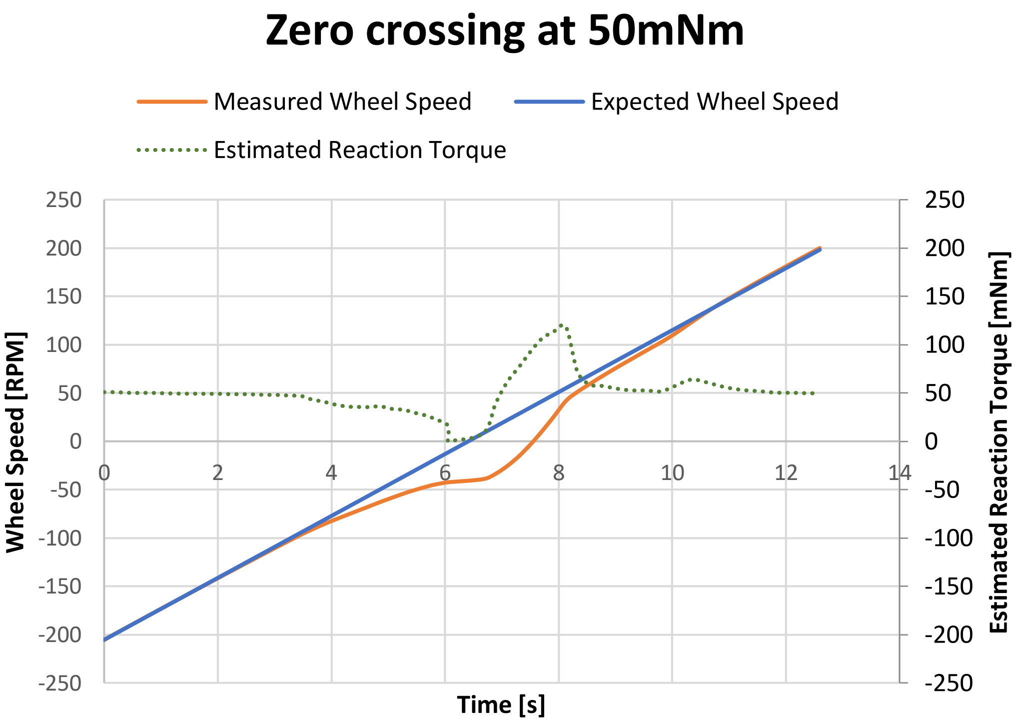


Figure 8-8: Zero crossing at 50mNm

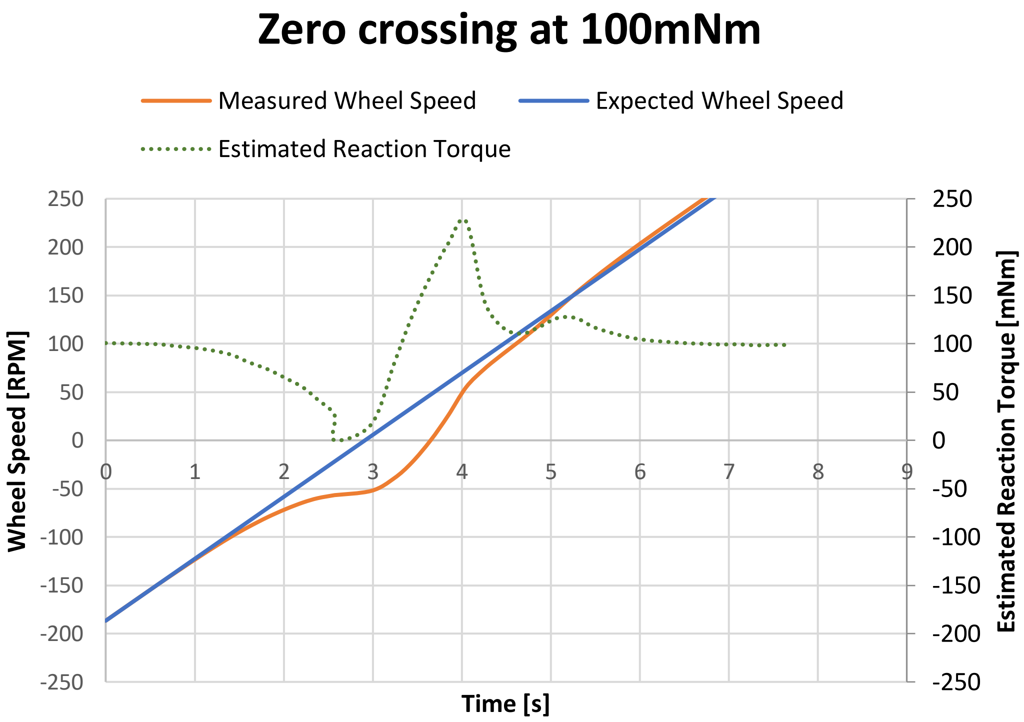


Figure 8-9: Zero crossing at 100mNm

9. CONTROL MODES

9.1 Current Control Mode

In Current Control Mode, the wheel drive electronics (WDE) controls the current flowing into the motor drive stage and through the motor windings according to the commanded current setpoint. This results in a motor torque in the direction of the current sign. This torque is proportional to the motor torque constant equal to 53.4mNm/A. Note that this value will not be equal to the net torque produced by the reaction wheel unit and is subject to motor and bearing losses. The largest current that can be commanded to flow through the motor windings is software limited to 6000mA, and hardware limited to 11000mA. Closed-loop current control is performed through sensing of the motor current and PWM switching of the motor drive. See Figure 9-1 for a model.

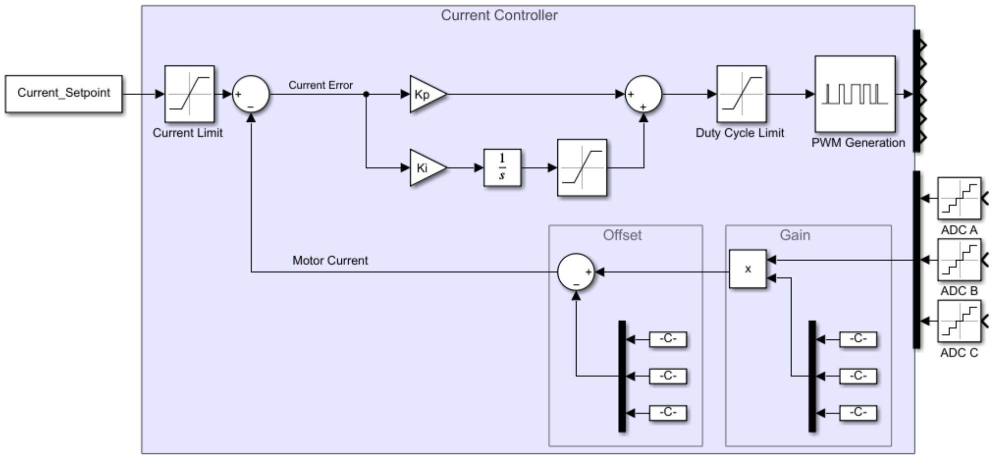


Figure 9-1: Current controller model

9.2 Speed Control Mode

In Speed Control Mode, the motor drive will be commutated according to the motor Hall sensor inputs, the closed-loop current controller will also be active. Closed-loop speed control of the flywheel is performed through measuring the motor speed from the Hall sensor inputs and updating the current controller setpoint. The flywheel speed can be controlled in both directions with wheel speed feedback acquired from the motor Hall sensors. When commanded to a new speed value, the acceleration of the flywheel is not constant. The angular momentum variation between two different speed commands is therefore not constant, but rather the mean value equal to the speed variation (commanded speed – actual speed) in the time frame between the commands.
The speed controller is implemented in firmware as a digital PI-controller. The control interval of the digital speed control loop is 10ms. See Figure 9-2 for a model.

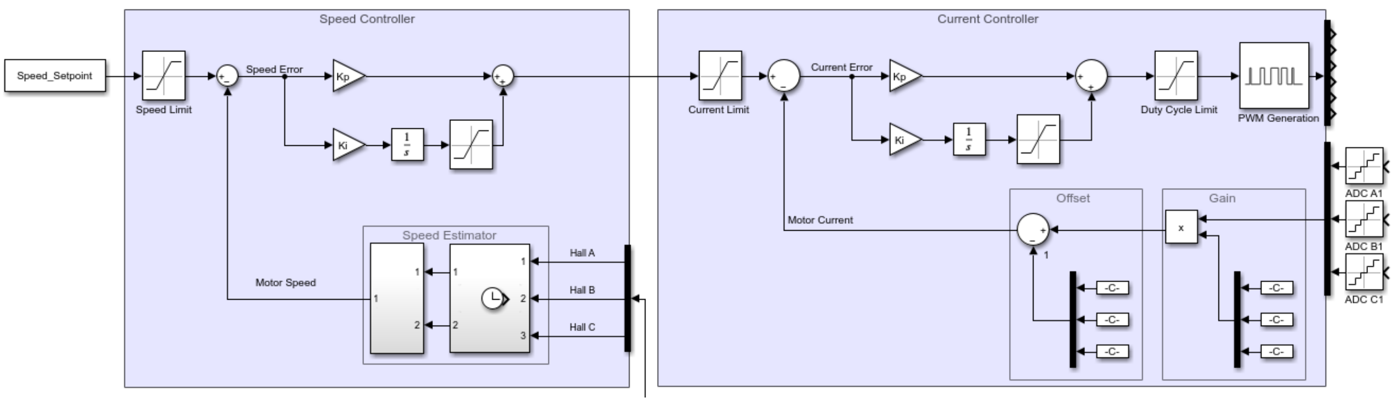


Figure 9-2: Speed controller model

9.3 Torque Control Mode

In Torque Control Mode, the desired net torque produced by the reaction wheel is directly commanded. The motor drive will be commutated according to the motor Hall sensor inputs and the closed-loop current controller will also be active. Reaction torque control is inferred through control of the flywheel acceleration by applying a ramp function to the speed PI controller proportional to the required acceleration. The required angular momentum variation is computed according to the total inertia of the rotating flywheel assembly. The wheel electronics will control the speed of the wheel in such a way that the angular momentum variation over the control loop interval of 10ms is equal to the commanded torque. Improved bandwidth and dynamic response are achieved by feeding forward the desired reaction torque and expected disturbance torque to the current controller. See Figure 9-3 for a model.

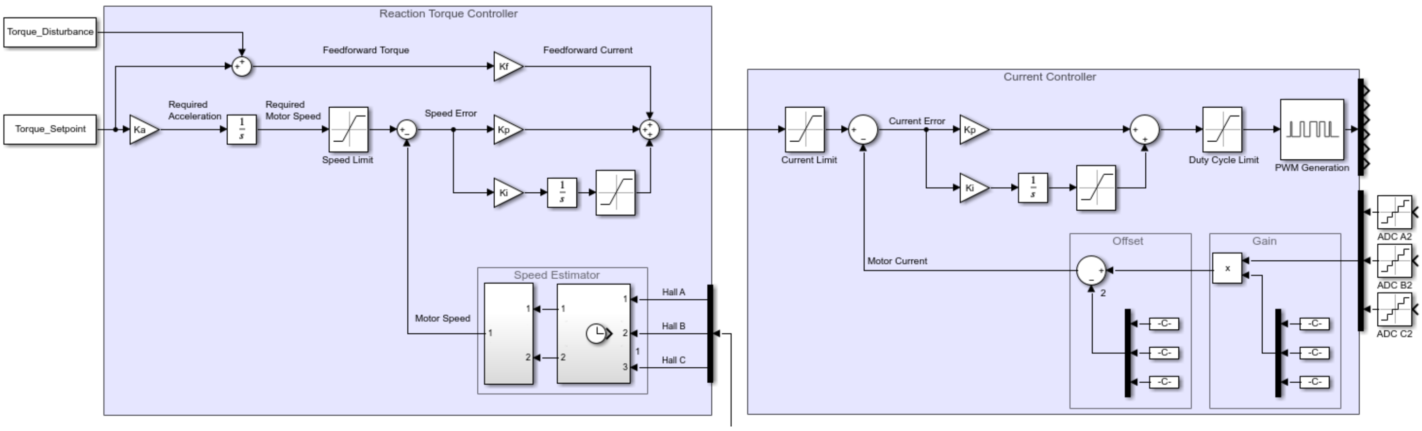


Figure 9-3: Torque controller model

9.4 PWM Control Mode (Backup Mode)

If component failure renders the other control modes unusable, the PWM Control Mode provides backup control with reduced functionality. This mode allows direct control over the duty cycle of the motor drive PWM. In PWM Control Mode:

- Current sense ADCs and speed measurements are not required.
- Closed-loop current/speed control are not active. PWM Control Mode is open-loop.
- Software overcurrent protection is not active.

Despite reduced functionality, the following functionality will remain active:

- Hardware cycle by cycle overcurrent protection remains active.
- Overvoltage protection and overvoltage braking load remains active in this mode (and in all other control modes).

9.5 Protection Mechanisms

9.5.1 Hard Protection Mechanisms

The following hard protection mechanisms are implemented to protect the WDE from permanent damage. Hard protection mechanisms will always override any active soft protection mechanisms. Users cannot disable the hard protection mechanisms.

9.5.1.1 +30V Drive Overvoltage Limit

Power regeneration during braking could cause overvoltage if the power is not dissipated. To prevent such a scenario, this hard protection mechanism protects the internal +30V (Drive) voltage rail. It is triggered when the sensed +30V (Drive) voltage exceeds 36V. When triggered, the motor drive is set to a high impedance state until the voltage drops below the threshold, after which normal operation resumes. The overvoltage limit threshold can be updated using a telemetry command. The default threshold is 36V.

The drive overvoltage threshold can be updated by sending a POKE Command [0x03], with the "Write address" field byte set to 0x05 and the "Write data word" field set according to the format UQ16.16 (V). Please note that it is not recommended to change the threshold from the default of 36V, reducing the threshold might cause the unit to exhibit abnormal behaviour and increasing the threshold beyond the default might allow permanent degradation or damage to the unit's drive electronics.

9.5.1.2 Hard Motor Phase Overcurrent Limit

This hard protection mechanism protects the motor and motor drive inverter from excessive current setpoints. It limits the current controller setpoint to 6A. This hard limit is active in the following control modes only:

- Current Control Mode
- Speed Control Mode
- Torque Control Mode

9.5.1.3 Maximum Motor Drive Duty Cycle Limit

This hard protection mechanism ensures the proper charging of the bootstrap capacitors supplying the high-side gate drive in the chosen motor driver. The motor drive requires a minimum 50-100ns PWM pulse at each switching cycle at the lower side for this charging to occur. The maximum duty cycle limit implemented is 97.85%.

9.5.1.4 Motor Overpower Limit

The function of this hard protection mechanism is to limit the power draw from the isolated DC/DC converter to below its rated limit of 120W. This is achieved by dynamically limiting the current controller setpoint to ensure that the power delivered to the motor does not exceed the set motor power limit. This limit could also be used to limit the maximum power draw of the device. Note that the maximum unit power draw is proportional but not equal to the motor power limit. The overpower limit can be updated using a telemetry command. The default motor power limit is 100W. This hard limit is active in the following control modes only:

- Current Control Mode
- Speed Control Mode
- Torque Control Mode

The motor overpower limit can be updated by sending a POKE Command [0x03], with the "Write address" field byte set to 0x08 and the "Write data word" field set according to the format UQ18.14 (mW). Please note that it is not recommended to increase the limit above the default of 100W, doing so might cause the unit to exhibit abnormal behaviour.

9.5.2 Soft Protection Mechanisms

The following soft protection mechanisms can be enabled/disabled and have their thresholds changed through telemetry commands. See the CONFIGURE-PROTECTION command, detailed in Section 12.8.

9.5.2.1 +30V Drive Braking Overvoltage Load

Power regeneration during braking increases the voltage on the +30V (Drive) voltage rail. Consequently, this soft protection mechanism is implemented to control the voltage rise of the internal +30V (Drive) voltage rail. It proportionally loads the +30V (Drive) voltage when exceeding the braking load setpoint of 31V.

The “+30V drive braking overvoltage load” setpoint can be updated by sending a POKE Command [0x03], with the “Write address” field byte set to 0x20 and the “Write data word” field set according to the format UQ16.16 (V). Please note that it is not recommended to change the setpoint from the default of 31V, doing so might cause the unit to exhibit abnormal behaviour.

9.5.2.2 Soft Motor Phase Overcurrent Limit

This soft protection mechanism limits the current command output of the speed/torque loops to set a closed-loop overcurrent threshold. It can be enabled/disabled using a telemetry command. The default is set to 6A, but can be updated using a telemetry command.

This limit provides a soft version of the hard limit detailed in Section 9.5.1.2: Hard Motor Phase Overcurrent Limit. Note that the hard limit is enforced in addition to this soft limit and will always override the soft limit. The soft limit applies to the following control modes only:

- Current Control Mode
- Speed Control Mode
- Torque Control Mode

The soft motor phase overcurrent limit can be updated by sending a POKE Command [0x03], with the “Write address” field byte set to 0x09 and the “Write data word” field set according to the format UQ18.14 (mA).

9.5.2.3 Active Overspeed Limit

This soft protection mechanism prevents the wheel speed increasing above a set threshold. When triggered, the following events occur:

- The commanded speed is limited to prevent the wheel speed increasing above the max setpoint. Note that triggering the limit does not change the wheel to a different control mode.
- An OVERSPEED-LIMITED flag is latched in the Fault register. Note that the flag will remain raised until it is manually lowered.
- An OVERSPEED-LIMITED flag is raised in the Status register while the speed is actively being limited. This flag will lower when the limit is not active.

This limit can be enabled/disabled using a telemetry command. The max setpoint can be updated using a telemetry command. The default max setpoint is 5000RPM. This soft limit is active for the following control modes only:

- Speed Control Mode
- Torque Control Mode

The active overspeed limit can be updated by sending a POKE Command [0x03], with the "Write address" field byte set to 0x07 and the "Write data word" field set according to the format UQ14.18 (RPM).

9.5.2.4 Overspeed Fault

This soft protection mechanism is implemented as an independent monitor in the firmware. The threshold is set to 6000RPM by default. It can be updated using a telemetry command. When the set threshold is exceeded, the following events occur:

- The motor drive is set to and kept at a high-impedance state.
- No current is driven through the motor.
- An OVERSPEED-FAULT flag is raised in the Fault register.

Clearing the OVERSPEED-FAULT flag in the Fault register returns the drive to a normal operating state. Overspeed Fault can be enabled/disabled using a telemetry command.

This protection mechanism is active in all control modes, namely:

- Current Control Mode
- Speed Control Mode
- Torque Control Mode
- PWM Control Mode (Backup Mode)

The overspeed fault threshold can be updated by sending a POKE Command [0x03], with the "Write address" field byte set to 0x06 and the "Write data word" field set according to the format UQ24.8 (V).

10. PROTOCOL LAYER 1-2 (PHYSICAL & DATA LINK)

10.1 Interface 1 (Power Interface)

10.1.1 Connector 1 (Power Interface Connector)

Table 10-1 provides part information for the power interface connector. All units are shipped with the power connector covered by an ESD-safe dust cap.

Table 10-1: Power interface connector specifications

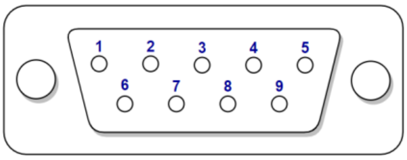
Parameter	Specification
Connector number	1
Type	D-Sub, Standard Density
Number of Contacts	9
Gender	Male [Pin]
Mounting Hardware	Fixed Female Jackpost, #4-40 UNC-2B
Recommended Connector Saver	TBC

10.1.2 Interface 1 Pinout (Power Interface)

The power interface connector pinout is detailed in Table 10-2. Pins are colour-coded based on functional grouping. The configuration column indicates if the pin is required for basic system functionality or optional for added flexibility or extending functionality.

Table 10-2: Power interface connector pinout

Pin Allocation



Con	Pin	Signal	Functional Description	Dir	Config
1	1	28V_SUPPLY	Unregulated 28V (primary) supply	IN	Required
1	2	28V_SUPPLY	Unregulated 28V (primary) supply	IN	Required
1	3	NC	Not connected	-	-
1	4	28V_RETURN	Unregulated 28V (primary) return	OUT	Required
1	5	28V_RETURN	Unregulated 28V (primary) return	OUT	Required
1	6	28V_SUPPLY	Unregulated 28V (primary) supply	IN	Required
1	7	NC	Not connected	-	-
1	8	NC	Not connected	-	-
1	9	28V_RETURN	Unregulated 28V (primary) return	OUT	Required

10.1.3 Power Supply

The unit is powered from an unregulated [+28V] supply rail. The main supply rail [+30V] is generated by a 120W isolated DC/DC converter. The main supply rail [+30V] is used to drive the motor and from it the wheel drive electronics (WDE) [+1.5V, +3.3V, +3.3V (Monitor), +3.3V (Interface), +5V (Analog), +5V (Digital), +12V] supply rails are regulated using downstream switching and linear regulators. An EMI filter is used to reduce the input line reflected ripple current of the DC/DC converters. The voltages and current draw of all the supply rails are monitored and available as telemetry. A LCL circuit offers protection for all components connected to the supply rails by independently monitoring the current draw on each supply rail. Figure 10-1 provides an overview of the power supply and conversion circuitry.

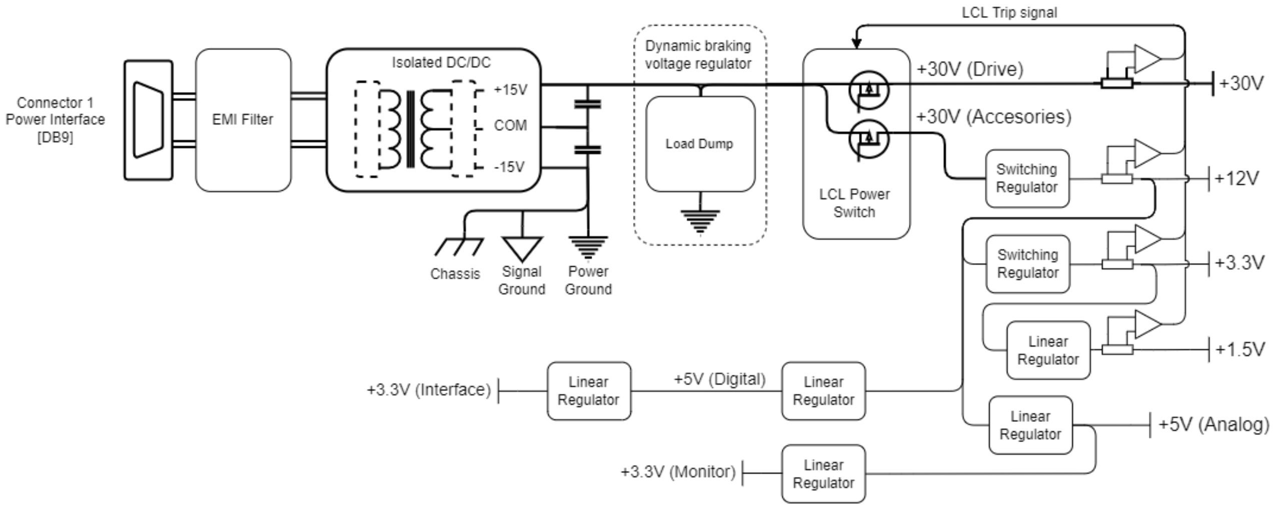


Figure 10-1: Overview of power supply and conversion circuitry

Table 10-3 details the power supply parameters.

Table 10-3: Power supply parameters

Property		Min	Typical	Max	Units
Supply Voltage: Continuous		20	28	36	V
Supply Voltage: Transient (50ms)		0	-	50	V
Current Consumption	Idle	130 (@36V)	180 (@28V)	240 (@20V)	mA
	Peak	3955 (@36V)	4986 (@28V)	7093 (@20V)	mA
	Fault (Worst case failure on secondary)	5515 (@36V)	6697 (@28V)	9375 (@20V)	mA
Isolated DC/DC (±12V)	Isolation @ 500VDC (Input-Output-Case)	100	-	-	MΩ
	Switching Frequency	425	500	600	kHz
Switching regulator (12V)	Switching Frequency	-	1000	-	kHz
Switching regulator (3.3V)	Switching Frequency	-	1000	-	kHz
Braking Load	Switching Frequency	-	72	-	kHz

10.1.4 Primary (28V Unregulated) Power Input Protections

10.1.4.1 Undervoltage Lockout

The main isolated DC/DC converter implements undervoltage lockout on the 28V unregulated power input.

The undervoltage lockout activation threshold (UVLO Turn On) is between 13.5V – 15.5V.

The undervoltage lockout deactivation threshold (UVLO Turn Off) is between 14.5V – 16V.

10.1.4.2 *Overcurrent Protection*

The main isolated DC/DC implements overcurrent protection by restricting its output voltage when the output current exceeds 5.2A.

The isolated DC/DC can implement this overcurrent protection indefinitely during a short circuit condition.

10.1.5 Inrush Current

Figure 10-2 and Figure 10-3 show the measured in-rush voltage and current characteristics of the unit supply, and return power interface when powered at the nominal supply voltage of 28V.

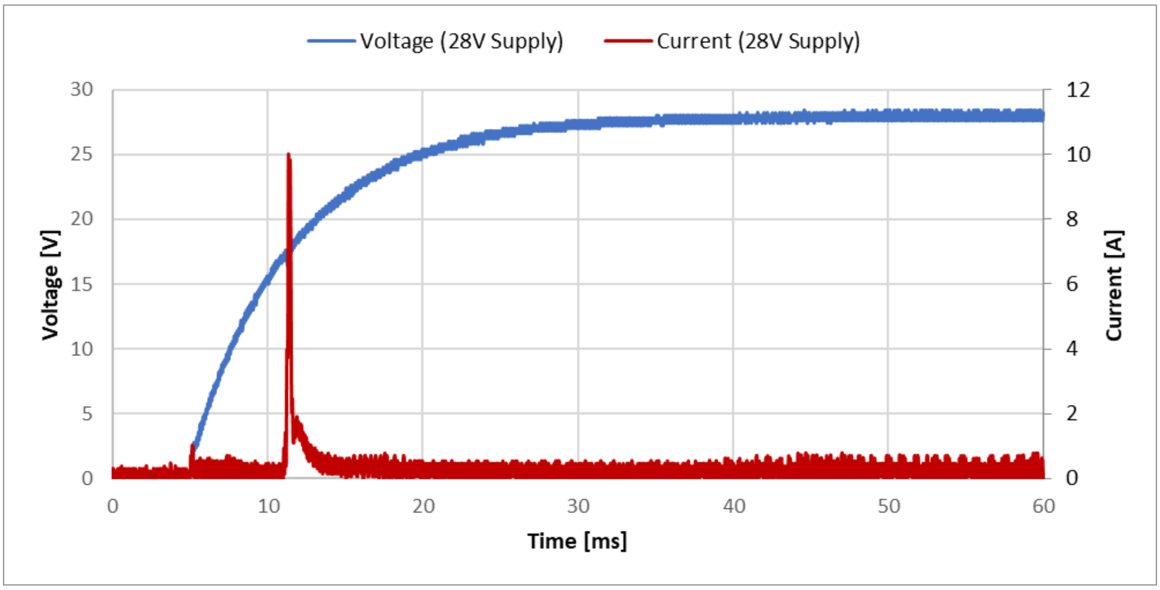


Figure 10-2 In-rush voltage and current measurement over 60ms

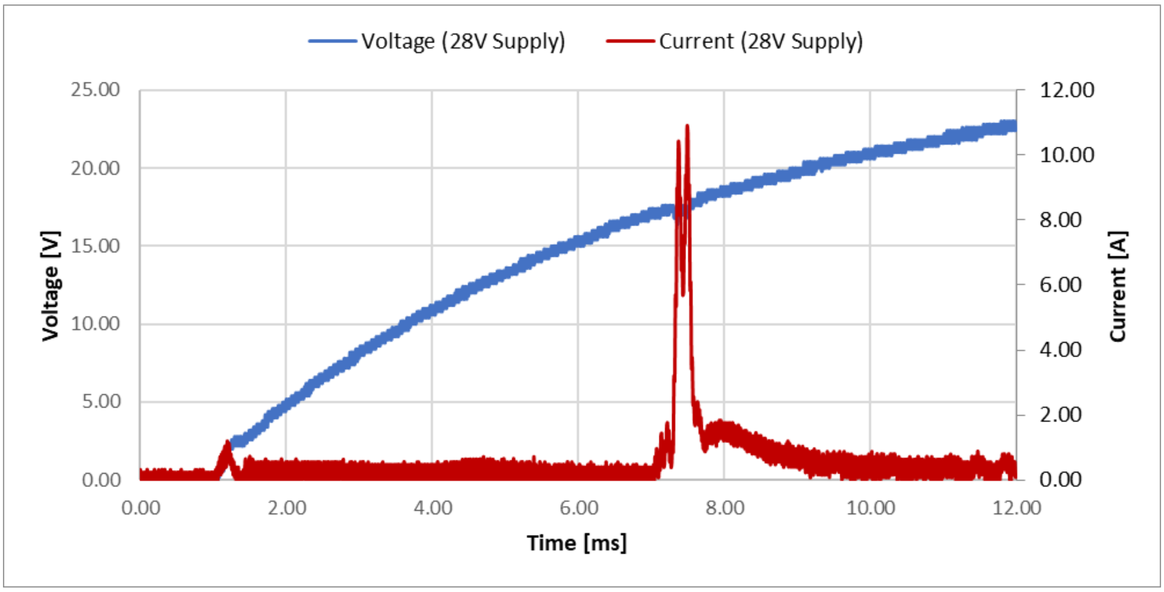


Figure 10-3 In-rush voltage and current measurement over 12ms

10.1.6 Grounding and Isolation

All electrical signals apart from the unregulated 28V input and return are referenced to chassis (on the secondary side of the isolated DC/DC converter). All unused connector pins are tied to chassis with a high impedance (100kOhms). DC/DC isolation (input to output, input to case, output to case) is detailed in Table 10-3. A grounding diagram is given in Figure 10-4.

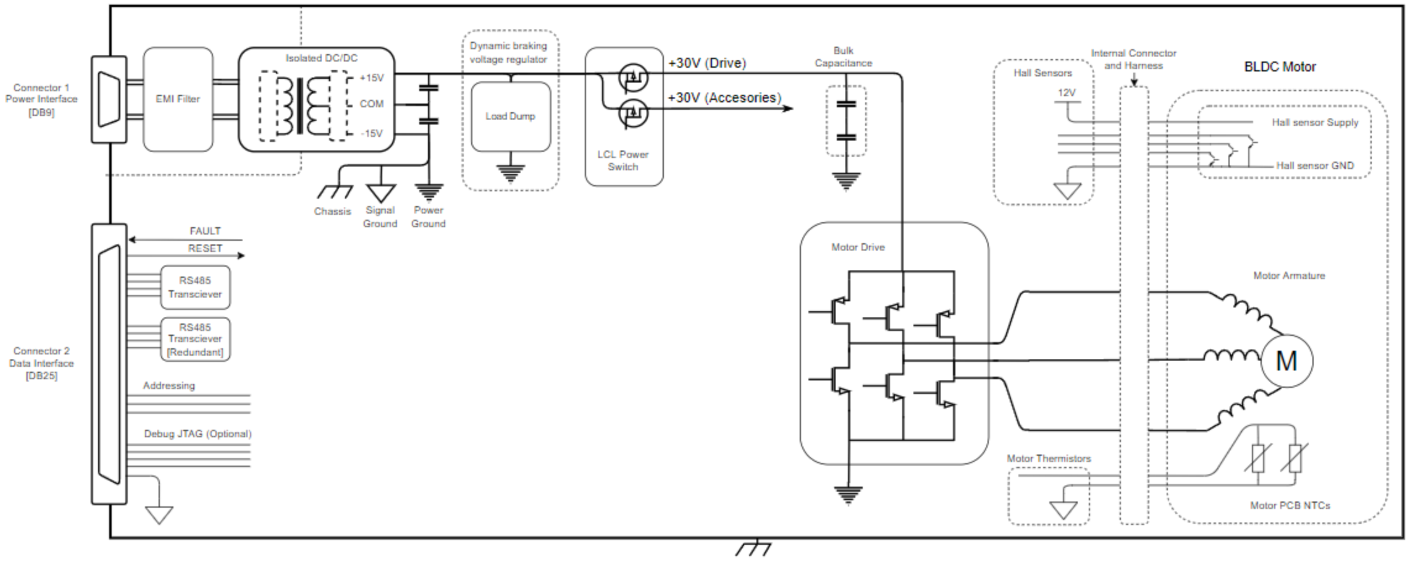


Figure 10-4: Grounding diagram

10.1.7 Power Consumption

This section details the power consumption for specific use cases of the NRWA-T6 under vacuum conditions.

The indicated power consumption specifications are given for the Unregulated 28V (primary) supply on Interface 1 (Power Interface). This is the only power input to the unit.

Table 10-4: NRWA-T6 power consumption specification under vacuum conditions

Parameter	Conditions			Specification
	Reaction Torque	Momentum	Supply Voltage	
Quiescent power consumption	0mNm	0Nms	28V (Nominal)	5.1W
Steady state power consumption @3Nms	0mNm	3Nms	28V (Nominal)	15.3W
Steady state power consumption @6Nms	0mNm	6Nms	28V (Nominal)	29.3W
Peak power consumption	262mNm	3.65Nms	28V (Nominal)	139.6W

The peak power consumption of the NRWA-T6 at any specific momentum occurs when the maximum motor current of 6A is commanded. Figure 10-5 details the peak power consumption and reaction torque as a function of momentum under vacuum conditions.

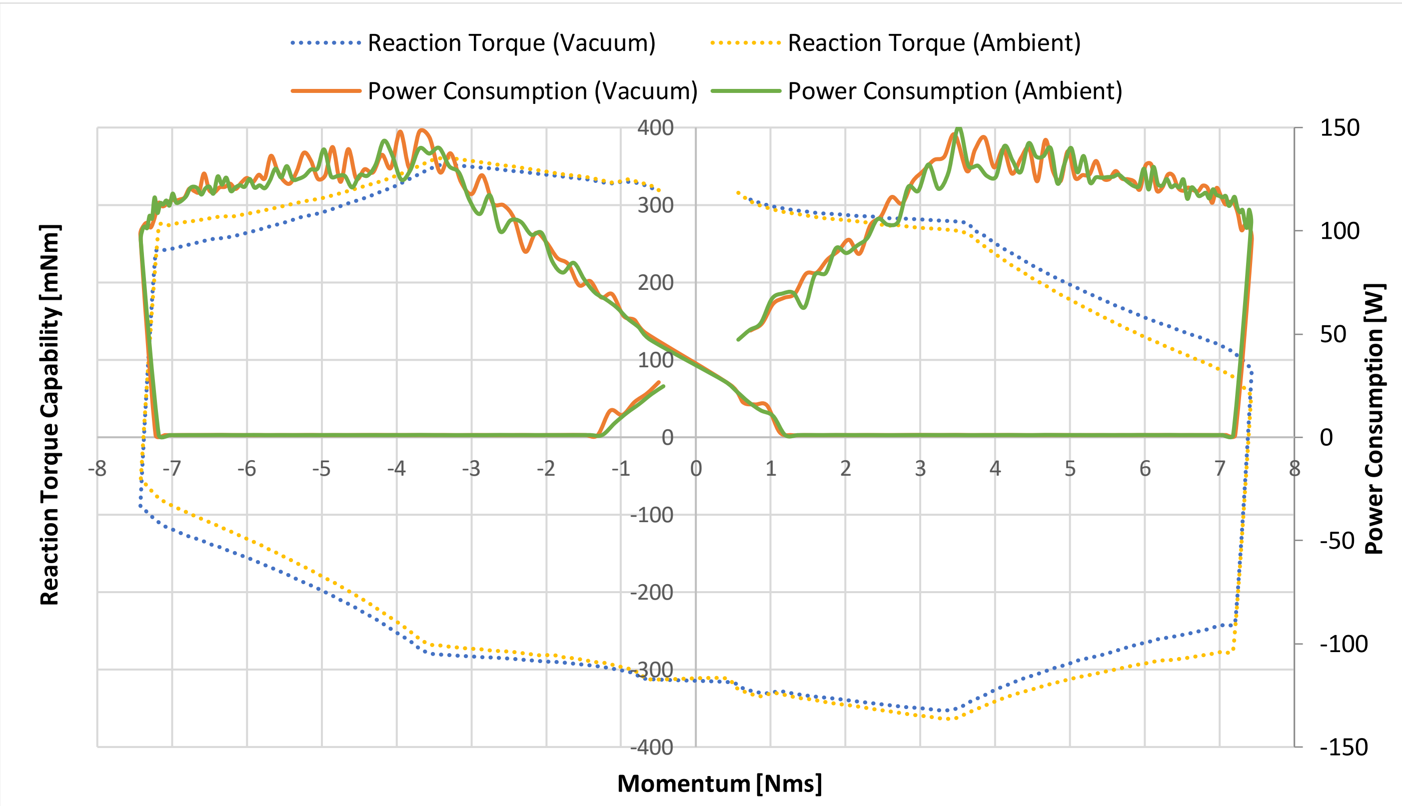


Figure 10-5 Peak power consumption and reaction torque over momentum under vacuum and ambient pressure conditions

The detailed power consumption in vacuum conditions of the NRWA-T6 for various reaction torques is shown in Figure 10-6 as a function of wheel speed and shown in Figure 10-7 as a function of angular momentum. Note that the power consumption drops to approximately 1W (which is below the nominal quiescent power consumption) if the motor drive is regenerating power when operating in the deceleration (braking) quadrant; excess power is dissipated as heat in the "braking-load" shunt resistors.

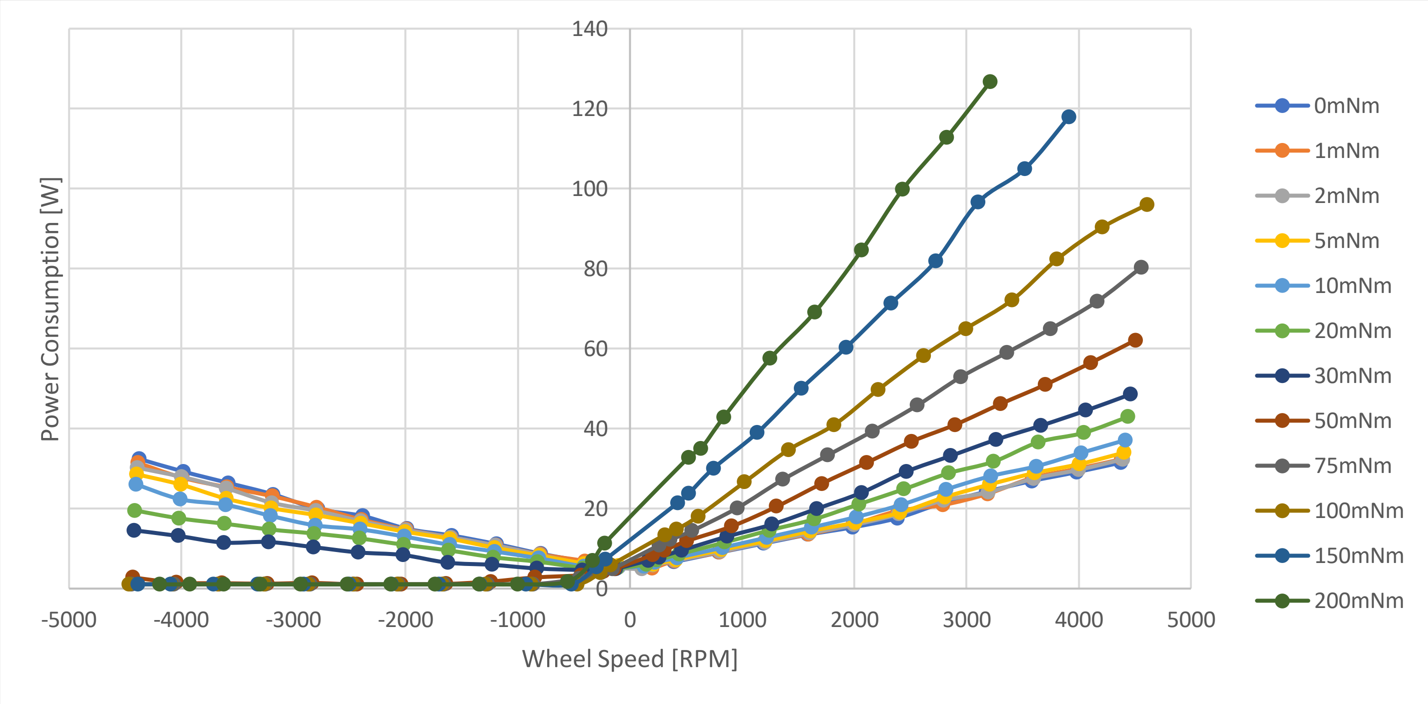


Figure 10-6: Power consumption as a function of wheel speed under vacuum conditions

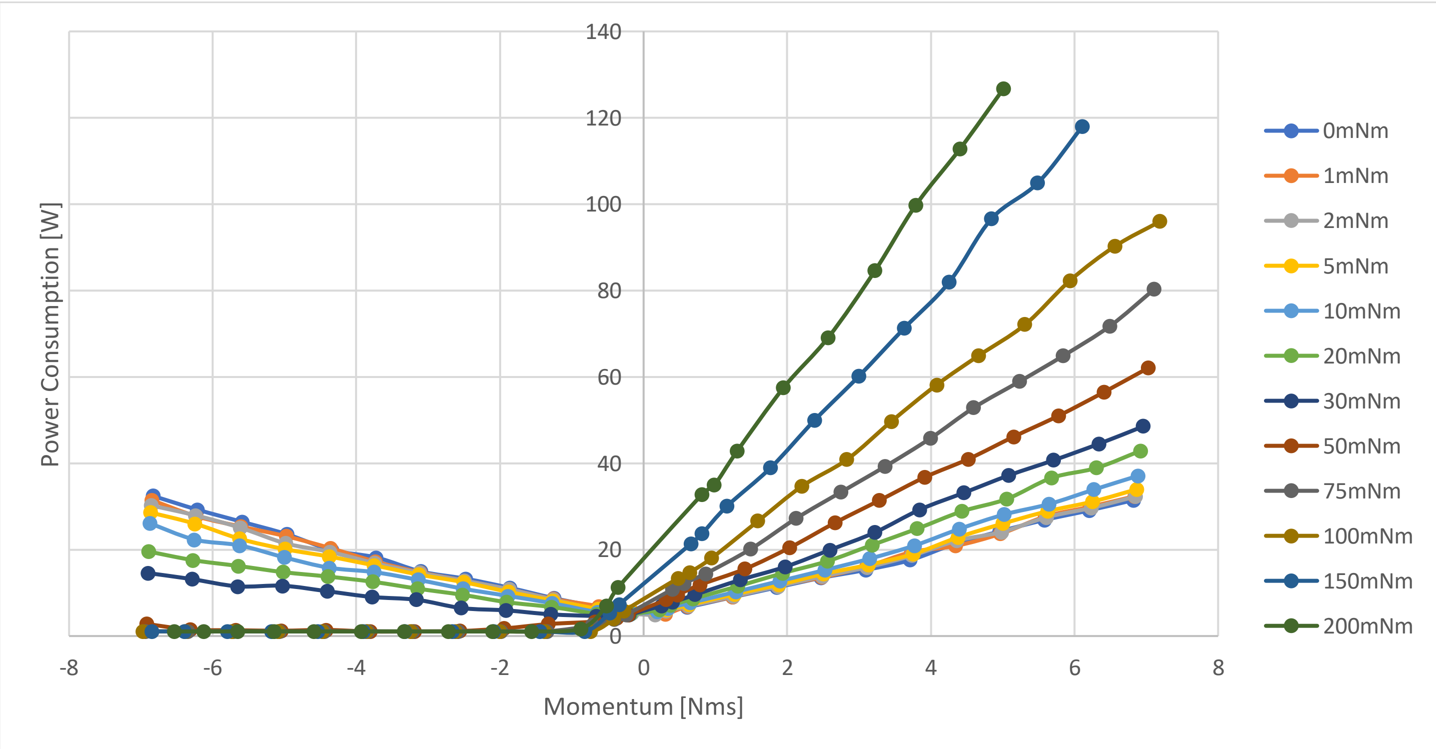


Figure 10-7: Power consumption as a function of angular momentum under vacuum conditions

The detailed power consumption in ambient pressure conditions of the NRWA-T6 for various reaction torques is shown in Figure 10-8 as a function of wheel speed, and shown in Figure 10-9 as a function of angular momentum.

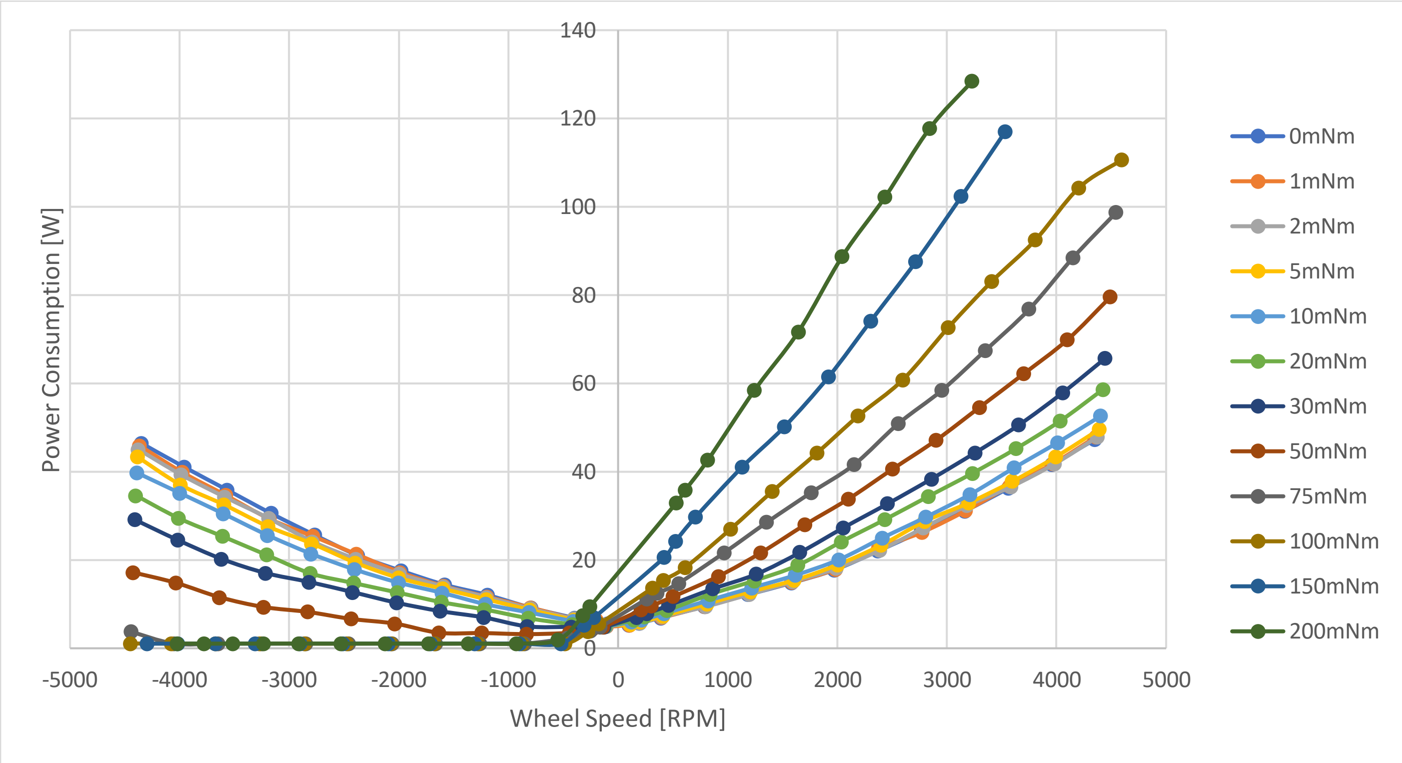


Figure 10-8: Power consumption as a function of wheel speed under ambient pressure conditions

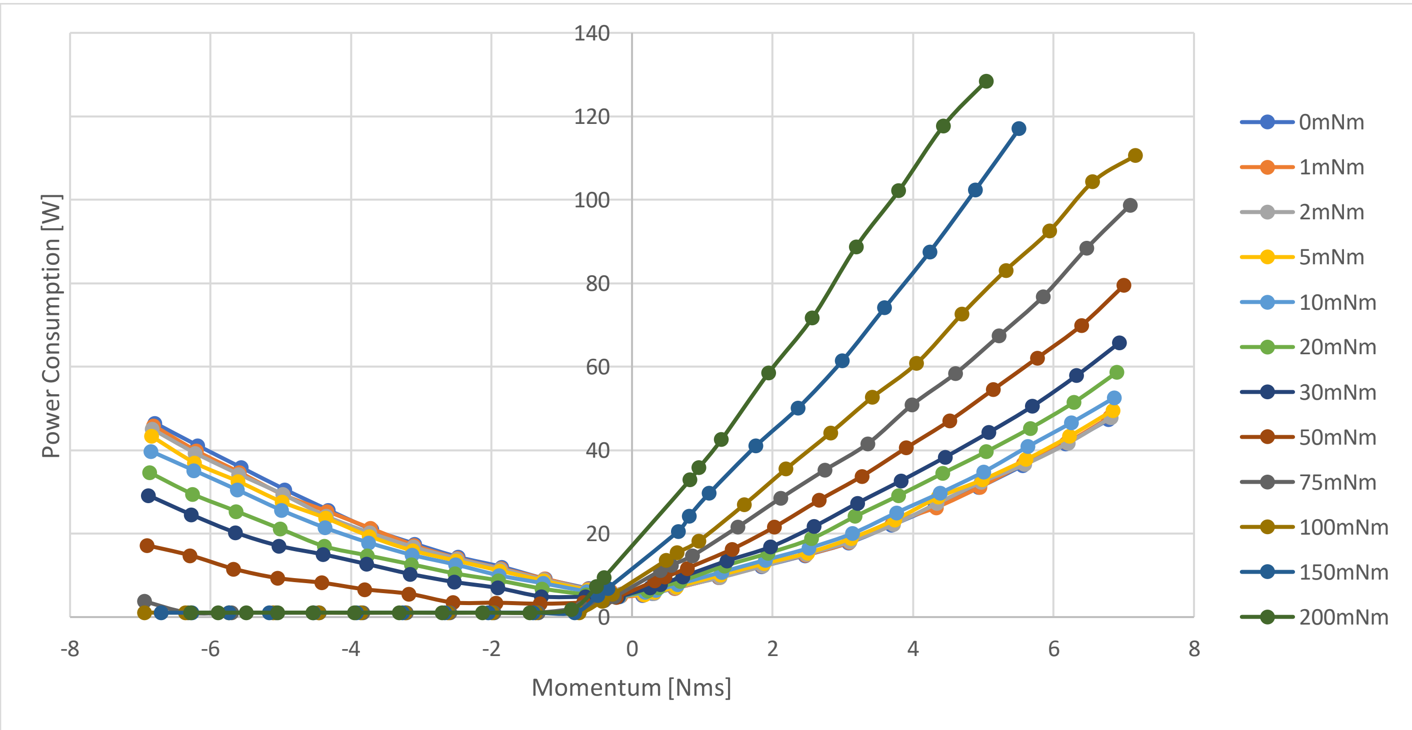


Figure 10-9: Power consumption as a function of angular momentum under ambient pressure conditions

10.2 Interface 2 (Data Interface)

10.2.1 Connector 2 (Data Interface Connector)

Table 10-5 provides part information for the data interface connector. All units are shipped with the power connector covered by an ESD-safe dust cap.

Table 10-5: Data interface connector specifications

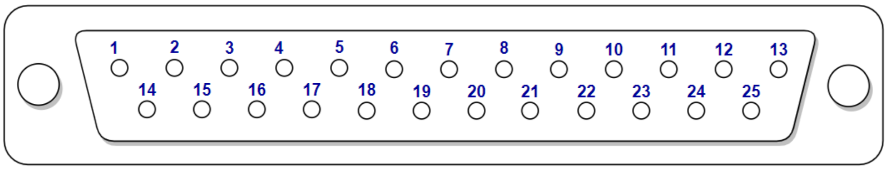
Parameter	Specification
Connector number	2
Type	D-Sub, Standard Density
Number of Contacts	25
Gender	Male [Pin]
Mounting Hardware	Fixed Female Jackpost, #4-40 UNC-2B
Recommended Connector Saver	TBC

10.2.2 Interface 2 Pinout (Data Interface)

The data interface connector pinout is detailed in Table 10-6. Pins are colour colour-coded on functional grouping. The configuration column indicates if the pin is *required* for basic system functionality or *optional* for added flexibility or extending functionality.

Table 10-6: Data interface connector pinout

Pin Allocation



Con	Pin	Signal	Functional Description	Dir	Config
2	1	FAULT	Active low FAULT output	OUT	Required
2	2	RESET_n	Active low RESET input (10kΩ pullup to 3.3V)	IN	Required
2	3	ADDR2	Harness addressing pin 2	IN	Required
2	4	ADDR1	Harness addressing pin 1	IN	Required
2	5	ADDR0	Harness addressing pin 0	IN	Required
2	6	VJTAG	Programmer JTAG supply voltage	OUT	Optional
2	7	R-RXD+	[Redundant RS-485] Positive polarity receive	IN	Optional
2	8	R-TXD-	[Redundant RS-485] Negative polarity transmit	OUT	Optional
2	9	RXD+	[RS-485] Positive polarity receive	IN	Required
2	10	TXD-	[RS-485] Negative polarity transmit	OUT	Required
2	11	TCK	FPGA JTAG TCK connection	OUT	Optional
2	12	TMS	FPGA JTAG Test mode select	IN	Optional
2	13	nTRST	FPGA JTAG Boundary scan reset	IN	Optional
2	14	GND	Signal GND	-	Required
2	15	GND	Address GND	-	Required
2	16	GND	Address GND	-	Required

2	17	GND	Address GND	-	Required
2	18	GND	Signal GND	-	Optional
2	19	VPUMP	FPGA Programming supply voltage	IN	Optional
2	20	R-RXD-	[Redundant RS-485] Negative polarity receive	IN	Optional
2	21	R-TXD+	[Redundant RS-485] Positive polarity transmit	OUT	Optional
2	22	RXD-	[RS-485] Negative polarity receive	IN	Required
2	23	TXD+	[RS-485] Positive polarity transmit	OUT	Required
2	24	TDI	FPGA JTAG Test data input	IN	Optional
2	25	TDO	FPGA JTAG Test data output	OUT	Optional

10.2.3 Ground (GND) Pins

The “GND” pins are directly connected to signal ground within the unit.

10.2.4 Addressing Pins

The three addressing signals (ADDR0 – ADDR2) are used to set the NSP destination address of the unit. This is described in more detail in Section 11.2.1, as is as the recommended address configurations for use with multiple NRWA-T6s.

The addressing signals (ADDR0 – ADDR2) are internally terminated with 10kΩ to +3.3V.

While the addressing pins are technically digital inputs, it is recommended that they be used only for addressing purposes by hard wiring to the adjacent “Address GND” pins or isolating. Shorting an address pin to GND will set the address bit to “0”, isolating the address pin will set the address pin to “1”. If shorting an address signal together, do so close to the connector. If isolating, cut the wire short near the connector. This will help to reduce radiated susceptibility EMC problems.

Table 10-7 details the electrical specification of addressing signals.

Table 10-7: ‘ADDR0, ADDR1, ADDR2’ signals electrical specification

Parameter	Specification	
Operating Range / Conditions	2V < ADDRX < 3.3V	Logic High “1”
	0V < ADDRX < 0.8V	Logic Low “0”
Termination	10kΩ to +3.3V	
ESD Protection	IEC 61000-4-2; level 4 (ESD) > 15 kV (air); > 8 kV (contact)	

10.2.5 Fault

The FAULT signal indicates when the internal latching current limiter (LCL) circuit has triggered and isolated power from all the internal supply rails.

The FAULT signal is a digital output. When active (indicating a fault condition), the FAULT signal will be pulled low in reference to signal ground.

Table 10-8 details the electrical specification of addressing signals.

Table 10-8: 'FAULT' signal electrical specification

Parameter	Specification	
Operating Range / Conditions	Logic High (IDLE)	3.3V
	Logic Low (FAULT)	0V
Maximum output current	5mA	
ESD Protection	IEC 61000-4-2; level 4 (ESD) > 15 kV (air); > 8 kV (contact)	

10.2.6 Reset

The RESET signal is pulled low to reset the internal LCL circuit, cycling and restoring power to the internal WDE [+1.5V, +3.3V, +5V, +12V] supply rails.

The RESET signal is internally terminated with 10kΩ to +5V.

Table 10-9 details the electrical specification of the RESET signal.

Table 10-9: 'RESET' signal electrical specification

Parameter	Specification	
Operating Range / Conditions	3.15V < RESET < 5V	Logic High (IDLE)
	0V < RESET < 1.35V	Logic Low (RESET)
Termination	10kΩ to +5V	
ESD Protection	IEC 61000-4-2; level 4 (ESD) > 15 kV (air); > 8 kV (contact)	

10.2.7 RS-485

Data interfacing occurs over the dual redundant RS-485 (TIA/EIA-485-A standard) interface. The interface is implemented as command-response. The NRWA-T6 will only reply after a telecommand addressed to the specific unit was received. The address of the unit is set using the addressing pins as described in Section 10.2.4: Addressing Pins.

10.2.7.1 RXD [+|-] Electrical Specification

The two RS-485 pairs carrying commands from the spacecraft to the device are called "RXD" and the redundant pair "R-RXD". No line termination is used as multiple NRWA-T6s can share the same RXD bus. It is recommended that the NRWA-T6 furthest away from the OBDH be terminated in harnessing (Refer to NRWA-T6: N2-A2a-DD0022 [AD01]). Otherwise, line termination is included per unit with a 120 Ohm resistor (Refer to NRWA-T6-B: N2-A2a-DD0029 [AD02]).

Table 10-10 details the electrical specification of the RXD and R-RXD signals.

Table 10-10: 'RXD [+|-]' electrical specification

Parameter	Specification	
Operating Range / Conditions	RXD- < RXD+	MARK (Idle, "1")
	RXD- > RXD+	SPACE (On, "0")
Input convention	RXD+	Non-Inverting
	RXD-	Inverting
Absolute Minimum / Maximum	-11V / +15V (each signal, with respect to signal ground)	

ESD Rating	IEC 61000-4-2; level 4 (ESD) > 15 kV (air); > 8 kV (contact)	
Line Termination	None (NRWA-T6: N2-A2a-DD0022 [AD01]), 120 Ohm (NRWA-T6-B: N2-A2a-DD0029 [AD02])	
Input Differential Threshold	± 0.2V max.	
Input Resistance	> 96 kΩ each signal to Power Ground	
Protocol	8-N-1 (8 bits per byte, no parity, 1 stop bit)	
Baud Rates	Nominal	460.8 kbps
	Permissible	455.623 – 465.688kbps

10.2.7.2 TXD [+|-] Electrical Specification

The two RS-485 pairs carrying replies from the device to the spacecraft is called “TXD” and the redundant pair “R-TXD”. In order to facilitate the sharing of the same TXD bus among multiple NRWA-T6 units, when not actively transmitting data in response to a telecommand, the TXD and R-TXD drivers switch to a three-state mode. This ensures that their outputs maintain a high output impedance across the entire common mode range, enabling another unit to drive the bus. To prevent excessive power dissipation in the event of bus contention, the RS-485 drivers have current-limiting mechanisms in place to restrict the output current.

Table 10-11 details the electrical specification of the TXD and R-TXD signals.

Table 10-11: ‘TXD [+|-]’ electrical specification

Parameter	Specification	
Operating Range / Conditions	TXD- < TXD+	MARK (Idle, “1”)
	TXD- > TXD+	SPACE (On, “0”)
Input convention	TXD+	Non-Inverting
	TXD-	Inverting
Absolute Minimum / Maximum	-11V / +15V (each signal, with respect to signal ground)	
ESD Rating	IEC 61000-4-2; level 4 (ESD) > 15 kV (air); > 8 kV (contact)	
Differential Output Voltage	>2.0V into 50Ω termination >1.5V into 27Ω termination	
Short-Circuit Output Current	300mA max.	
Three-State Output Current	± 50uA max.	
Output Impedance	100Ω @ 100MHz, common mode	
Protocol	8-N-1 (8 bits per byte, no parity, 1 stop bit)	
Baud Rates	Nominal	460.8 kbps
	Actual	460.6 kbps

10.2.7.3 Optional JTAG Interface

The optional external JTAG interface is included to allow ground-based maintenance of the FPGA firmware to be performed on built/delivered units.

11. PROTOCOL LAYER 3 (NETWORK AND TRANSPORT LAYER)

Two serial data ports are implemented in the NRWA-T6, providing redundancy on both the physical and network layer. Each serial port consists of unidirectional data channels corresponding with their physical full-duplex RS-485 receive and transmit channels. The physical signals of the redundant serial port are indicated as R-RXD and R-TXD in Table 10-6: Data interface connector pinout.

Communication with the NRWA-T6 occurs through either one of the two redundant serial data port's unidirectional data channels: the RXD port for receiving data and the TXD port for transmitting data. The OBDH is the master of the communication bus, therefore controlling the bus and initiating data communication by transmitting a telecommand message to a slave such as the NRWA-T6, which responds with a reply message on the same serial port that the telecommand was issued to.

The telecommand and reply messages are encapsulated into framed data packets using SLIP framing [RD01]. SLIP framing is required on physical links that do not have out-of-band message completion signals.

The telecommand and reply messages are implemented using the Nanosatellite Protocol (NSP). The NSP protocol was originally developed at the UTIAS Space Flight Laboratory for use on the CanX nanosatellites.

The basic unit of communication in the NSP is a message which is composed of an ordered sequence of bytes:

- Wherever multiple adjacent bytes are grouped together to form larger storage units (16-bit integers, 32-bit floats, etc.) the least significant bytes of each individual storage unit are transmitted and received first unless stated otherwise.
- The bit-level transmission order (Endianness) of bytes grouped as larger storage units (16-bit integers, 32-bit floats, etc.) is little-endian.
- The bit-level formats used by the NRWA-T6 for numeric values include:
    - 8-Bit Unsigned
    - 16-Bit Unsigned
    - 32-Bit Unsigned
    - Q10.6 (Signed 10-Bit integer + 6-Bit fraction)
    - Q8.8 (Signed 8-Bit integer + 6-Bit fraction)
    - Q12.4 (Signed 12-Bit integer + 4-Bit fraction)
    - Q14.2 (Signed 14-Bit integer + 2-Bit fraction)
    - Q20.12 (Signed 20-Bit integer + 12-Bit fraction)
    - UQ30.2 (Unsigned 30-Bit integer + 2-Bit fraction)
- The AMD variant of Q notation for fixed-point numeric values is implemented [RD02].

11.1 NSP Encapsulation (SLIP Framing)

The telecommand and reply messages are encapsulated into framed data packets using SLIP framing [RD01]. Upon reception the framing is removed.

A special character FEND (0xc0) marks both the beginning and end of each NSP message. Wherever FEND would occur within the message, it is replaced by two bytes: FESC TFEND (0xdb 0xdc). Wherever FESC (0xdb) would occur within the message, it is replaced by FESC TFESC (0xdb 0xdd).

When processing a SLIP framed message, a FESC character can only be followed by a TFEND or TFESC character. Any other character is incorrect.

11.2 NSP Message Format

NSP messages, and therefore the telecommand and reply messages, are composed of five data fields as shown in Table 11-1.

Table 11-1: NSP message fields

Length	Field
1 Byte	Destination Address
1 Byte	Source Address
1 Byte	Message Control Field
0 or more Bytes	Data Field (Least significant byte transmitted/received first)
2 Bytes	Message CRC (Least significant byte transmitted/received first)

11.2.1 Destination Address

The Destination Address is 8 bits in length. The specific NSP destination address of each NRWA-T6 is set by the three harness addressing pins on the data interface connector as detailed in Section 10.2.4: Addressing Pins.

The three least significant bits of the main serial port's NSP destination address is set directly by the three harnessing pins. The redundant serial port's NSP destination address is offset by 0x80 from the main serial port destination address, with the three least significant bits of the address also corresponding to the three harnessing pins.

The recommended address configuration for use with four NRWA-T6s is shown in Table 11-2.

Table 11-2: Recommended address configurations

ADDR0	ADDR1	ADDR2	Main serial port Destination Address	Redundant serial port Destination Address
0	0	1	0x01	0x81
0	1	0	0x02	0x82
1	0	0	0x04	0x84
1	1	1	0x07	0x87

Using these address configurations for four NRWA-T6s ensures a Hamming distance of 1 between each set NRWA-T6 address. This ensures that if a minimum of one addressing pin fails, it will not result in any of the four wheels being set to the same destination address.

11.2.2 Source Address

The Source Address identifies the initiator of the message. Recommended address ranges are between 0x01 and 0xFF. Users of the NRWA-T6 should choose an NSP address for the OBDH. By convention, 0x11 is used as the NSP address for the primary computer.

11.2.3 Message Control

Within each NSP message is a Message Control field byte. Table 11-3 shows how the individual bits in this byte are decoded. There are three Boolean quantities, labelled “A”, “B” and “Poll”. There is also a five-bit command code, interpreted as an unsigned integer between 0 and 31.

Table 11-3: NSP Message Control field

Range	Designation
Bit 7 (MSB)	"Poll" Bit
Bit 6	"B" Bit
Bit 5	"A" (ACK) Bit
Bits 4 – 0	Command code

Table 11-4 shows the NSP command codes that are recognized by the NRWA-T6.

Table 11-4: NSP command codes

Command Code	Function
0x00	PING
0x01	INIT
0x02	PEEK
0x03	POKE
0x04	RESERVED
0x05	RESERVED
0x06	CRC
0x07	APPLICATION-TELEMETRY
0x08	APPLICATION-COMMAND
0x09	CLEAR-FAULT
0x0A	CONFIGURE-PROTECTION
0x0A	TRIP-LCL

11.2.4 Message Data

The Message Data is a variable number of bytes, from 0 or more bytes. The setting of and interpretation of the Message Data is defined in Section12.

11.2.5 Message CRC

Each NSP message ends with a 2-byte Message CRC. The Message CRC is sent with the least significant byte first and then the most significant byte. The Message CRC is used to verify the integrity of the entire NSP message. The Message CRC uses the CCITT polynomial X16 + X12 + X5 + 1. The CRC is initialised to 0xFFFF. Bytes are fed into the CRC computation starting with the Destination Address and concluding with the last byte of the Message Data field.

11.3 Telecommand Format

The OBDH will send telecommands to the NRWA-T6. The specific implementation of the NSP telecommand message's format and interpretation of different data fields are defined in Table 11-5.

Table 11-5: NSP telecommand format

Length		Field	Description
1 Byte		Destination Address	Address of the RWA
1 Byte		Source Address	Unique address of the OBDH
1 Byte	1 bit	"Poll" bit	'1' if reply is required, '0' if no reply is required
	1 bit	"B" bit	Ignored
	1 bit	"A" bit	Ignored

	5 bits	Command Code	System or Application Command Code
0 or more Bytes		Data Field	Data bytes according to specific command
2 Bytes		CRC	CCITT CRC computed from message

When a sequence of bytes that may be a telecommand are received, a device will take the following steps to validate it:

1. The destination address will be compared to the set NSP destination address of a specific NRWA-T6, as detailed in Section 11.2.1: Destination Address.
2. The message must meet the minimum message length (5 bytes).
3. The message must not have more than 260 bytes of data.
4. The SLIP framing must be correct.
5. The message CRC must be correct.

Messages that fail any of these criteria are cleared from the receiver buffer and no reply message will be generated.

11.4 Reply Format

After a telecommand has been executed, the NRWA-T6 will generate a reply message if (and only if) the telecommand "Poll" bit was set to '1'. Reply attributes are listed in Table 11-6.

Table 11-6: NSP reply format

Length		Field	Description
1 Byte		Destination Address	Address of the RWA
1 Byte		Source Address	Unique address of the OBDH
1 Byte	1 bit	"Poll" bit	'1' if reply is required, '0' if no reply is required
	1 bit	"B" bit	Ignored
	1 bit	"A" bit	Ignored
	5 bits	Command Code	System or Application Command Code
0 or more Bytes		Data Field	Data bytes according to specific command
2 Bytes		CRC	CCITT CRC computed from message

Most of the reply message is a direct echo of the telecommand message. This makes inefficient use of the link bandwidth but makes the context of each reply completely unambiguous.

The NRWA-T6's RS-485 output driver will be enabled only for the transmission of the message. Once the stop bit of the final character has been sent, the output will be set to high impedance.

12. PROTOCOL LAYER 5 (SESSION LAYER)

12.1 NSP Command Codes

The defined NSP command codes are shown in Table 12-1.

Table 12-1: Applicable NSP command codes

Command Code	Function	Implemented	Application Use
0x00	PING	YES	YES
0x01	INIT	NO	NO
0x02	PEEK	YES	NO
0x03	POKE	YES	NO
0x04	RESERVED	NO	NO
0x05	RESERVED	NO	NO
0x06	CRC	NO	NO
0x07	APPLICATION-TELEMETRY	YES	YES
0x08	APPLICATION-COMMAND	YES	YES
0x09	CLEAR-FAULT	YES	YES
0x0A	CONFIGURE-PROTECTION	YES	YES
0x0B	TRIP-LCL	YES	YES
0x0C-0x1F	RESERVED	NO	NO

12.2 PING Command [0x00]

The PING Command is typically used during testing to verify communications. The reply message generated by the NRWA-T6 will contain information including the device type, unit serial number and firmware version.

12.2.1 Telecommand Format of the PING Command

The data field of the NSP telecommand for the PING Command is empty. Table 12-2 gives an example.

Table 12-2: Example of PING Command inside a telecommand NSP packet

Field	FEND	Destination	Source	Message Control Field				Data	CRC	FEND
				P	B	A	Command			
Length	1 Byte	1 Byte	1 Byte	1 Byte				0 bytes	2 Bytes	1 Byte
Content	0xC0	0xC1	0x11	0b10100000				-	0xXXXX	0xC0

12.2.2 Reply Format of the PING Command

The NRWA-T6 will reply to any PING telecommand (provided the “Poll” bit is set) with a NSP message in the format detailed in Section 11.2. The data field of the NSP message will contain content as specified in Table 12-3.

The “A” bit is set to indicate an ACK – that the telecommand has successfully executed. If the “A” bit is clear a NACK is indicated – there has been a problem, and the telecommand has not executed.

Table 12-3: PING Command Reply Data Field Content

Length	Field	Function	Format
1 Byte	Device Type	NRWA Device numeric identifier	8-Bit Unsigned
1 Byte	Device Serial Number	Unit specific firmware serial number	8-Bit Unsigned
1 Byte	Firmware Version MAJOR	FPGA Firmware major number	8-Bit Unsigned
1 Byte	Firmware Version MINOR	FPGA Firmware minor	8-Bit Unsigned
1 Byte	Firmware Version Patch	FPGA Firmware patch number	8-Bit Unsigned

12.3 PEEK Command [0x02]

The PEEK Command is used to read the volatile device memory directly. The data field of the PEEK Command is a single byte corresponding to the memory address that is to be read, each address location contains a 32-bit value grouped as 4 bytes that will be echoed back in the data field of the reply message.

An overview of the device memory map is shown in Table 12-4, also detailing the range of addresses that can be accepted by the PEEK Command.

Table 12-4: PEEK Command device memory map overview

Address range	Field	Function	Accessible
0x00-0x30	Initialized Parameters	Initialized and volatile RAM block used to store system parameters.	Yes
0x31-0x9F	Reserved	-	No
0xA0-0xFF	Application Data	Non-initialized and volatile RAM block used for storing measurements and data available as telemetry.	Yes (Not recommended, for debugging use only)

12.3.1 Telecommand Format of the PEEK Command

The data field of the PEEK Command is a single byte corresponding to the memory address that is to be read. See Table 12-5 for an example.

Table 12-5: Example of PEEK Command inside a telecommand NSP Packet

Field	FEND	Destination	Source	Message Control Field				Data	CRC	FEND
				P	B	A	Command			
Length	1 Byte	1 Byte	1 Byte	1 Byte				1 Byte (RAM Address)	2 Bytes	1 Byte
Content	0xC0	0x01	0x11	0b10000010				0x01	0xXXXX	0xC0

12.3.2 Reply Format of the PEEK Command

The NRWA-T6 will reply to any PEEK telecommand (provided the “Poll” bit is set) with a NSP message in the format detailed in Section 11.2. The data field of the NSP message will contain content as specified in Table 12-6.

The “A” bit is set to indicate an ACK – that the telecommand has successfully executed. If the “A” bit is clear a NACK is indicated – there has been a problem, and the telecommand has not executed.

Table 12-6: PEEK Command Reply Data Field Content

Length	Field	Function	Format
4 Bytes	Read data word	Data word read at the specified location	Refer to Table 12-7

12.3.3 Detailed Initialized Parameters Address Range Memory Map and Description

The addresses ranging from 0x00 to 0x2D is defined as the Initialized and volatile RAM block used to store system parameters. This address range is accessible by both PEEK and POKE Commands.

Table 12-7: Initialized Parameters detailed memory map

Address	Function	Format
0x00	Unit Firmware Serial Number	32-Bit Unsigned
0x01	Device Type	32-Bit Unsigned
0x02	FW_VERSION_MAJOR	32-Bit Unsigned
0x03	FW_VERSION_MINOR	32-Bit Unsigned
0x04	FW_VERSION_PATCH	32-Bit Unsigned
0x05	+30V Drive Overvoltage Limit	UQ16.16 (V)
0x06	Overspeed Fault Threshold	UQ24.8 (RPM)
0x07	Active Speed Limit	UQ14.18 (RPM)
0x08	Motor Overpower limit	UQ18.14 (mW)
0x09	Soft Motor Phase Overcurrent Limit	UQ18.14 (mA)
0x0A	PHASE A CURRENT ADC OFFSET	32-Bit Unsigned
0x0B	PHASE A CURRENT ADC GAIN	32-Bit Unsigned
0x0C	PHASE B CURRENT ADC OFFSET	32-Bit Unsigned
0x0D	PHASE B CURRENT ADC GAIN	32-Bit Unsigned
0x0E	PHASE C CURRENT ADC OFFSET	32-Bit Unsigned
0x0F	PHASE C CURRENT ADC GAIN	32-Bit Unsigned
0x10	Phase current controller Kp	32-Bit Unsigned
0x11	Phase current controller Ki	32-Bit Unsigned
0x12	Phase current controller integral term limit	32-Bit Unsigned
0x13	Speed controller Kp @ < 10RPM	32-Bit Unsigned
0x14	Speed controller Ki @ < 10RPM	32-Bit Unsigned
0x15	Speed controller Kp @ < 100RPM	32-Bit Unsigned
0x16	Speed controller Ki @ < 100RPM	32-Bit Unsigned
0x17	Speed controller Kp @ >100RPM	32-Bit Unsigned
0x18	Speed controller Ki @ >100RPM	32-Bit Unsigned
0x19	Speed controller coulomb friction disturbance	Q26.6 (mNm)
0x1A	Speed controller integral term limit	32-Bit Unsigned
0x1B	Torque controller conversion factor	Q16.16 (RPM/mNm)
0x1C	Torque controller motor Kt parameter	Q24.8 (mA/mNm)
0x1D	Torque controller coulomb friction disturbance	Q26.6 (mNm)
0x1E	Braking Overvoltage Load proportional gain	32-Bit Unsigned
0x1F	Braking Overvoltage Load duty cycle limit	32-Bit Unsigned
0x20	Braking Overvoltage Load setpoint	Q16.16 (V)
0x21	Monitor ADC generic gain	32-Bit Unsigned
0x22	Monitor ADC +30V Drive voltage gain	32-Bit Unsigned
0x23	Monitor ADC 5V supply current gain	32-Bit Unsigned
0x24	Monitor ADC 3.3V supply current gain	32-Bit Unsigned
0x25	Monitor ADC 1.5V supply current gain	32-Bit Unsigned
0x26	Monitor ADC 30V supply current gain	32-Bit Unsigned
0x27	Monitor ADC 5V digital supply current gain	32-Bit Unsigned
0x28	Monitor ADC 5V supply voltage gain	32-Bit Unsigned

0x29	Monitor ADC 12V supply current gain	32-Bit Unsigned
0x2A	Monitor ADC 1.5V supply voltage gain	32-Bit Unsigned
0x2B	Monitor ADC 3.3V supply voltage gain	32-Bit Unsigned
0x2C	Monitor ADC 12V supply voltage gain	32-Bit Unsigned
0x2D	Monitor ADC 2.5V reference voltage gain	32-Bit Unsigned
0x2E	Monitor ADC generic offset	32-Bit Unsigned
0x2F	Monitor ADC +30V Drive current offset	32-Bit Unsigned
0x30	Reserved	-

12.4 POKE Command [0x03]

The POKE Command is used to write to the volatile device memory directly. The data field of the POKE Command consists of a single byte corresponding to the desired memory address followed by 4 bytes of data that will be written to the specified memory address.

Table 12-8 gives an overview of the device memory map and details the range of addresses that can be accepted by the POKE Command.

Table 12-8: POKE Command device memory map overview

Address range	Field	Function	Accessible
0x00-0x30	Initialized Parameters	Initialized and volatile RAM block used to store system parameters.	Yes
0x31-0x9F	Reserved	-	No
0xA0-0xFF	Application Data	Non-initialized and volatile RAM block used for storing measurements and data available as telemetry.	Yes (Not recommended, for debugging use only)

12.4.1 Telecommand Format of the POKE Command

Address ranges not mentioned in Table 12-8 are unsupported, and attempted writes could generate NACKs.

Table 12-9: POKE Command telecommand Data Field Content

Length	Field	Function	Format
1 Byte	Write address	Address in device RAM to be written to.	Refer to Table 12-4.
4 Bytes	Write data word	Data word to be written to the specified RAM address.	Refer to Table 12-7.

Table 12-10: Example of POKE Command inside a telecommand NSP Packet

Field	FEND	Destination	Source	Message Control Field				Data	CRC	FEND
				P	B	A	Command			
Length	1 Byte	1 Byte	1 Byte	1 Byte				1 Byte (RAM address) + 4 Bytes (Data)	2 Bytes	1 Byte
Content	0xC0	0x01	0x11	0b10000011				0x0100000001	0xXXXX	0xC0

12.4.2 Reply Format of the POKE Command

The NRWA-T6 will reply to any POKE telecommand (provided the "Poll" bit is set) with a NSP message in the format detailed in Section 11.2. The data field of the NSP message will be empty.

The "A" bit is set to indicate an ACK – that the telecommand has successfully executed. If the "A" bit is clear a NACK is indicated – there has been a problem, and the telecommand has not executed.

12.5 APPLICATION-TELEMETRY Command [0x07]

The APPLICATION-TELEMETRY Command is used to request telemetry associated with standard reaction wheel operation.

12.5.1 Telecommand Format of the APPLICATION-TELEMETRY Command

The data field of the NSP telecommand corresponds to the identifier of the desired block of application-level telemetry data fields that will be contained in the data field of the NSP reply message. The available types of data blocks are shown in Table 12-11.

Table 12-11: APPLICATION-TELEMETRY Reply data block types

Identifier	Designation	Reply NSP data field size
0x00	STANDARD	25 Bytes
0x01	TEMPERATURES	8 Bytes
0x02	VOLTAGES	24 Bytes
0x03	CURRENTS	24 Bytes
0x04	DIAGNOSTIC-GENERAL	20 Bytes
0x05	DIAGNOSTIC-EDAC	20 Bytes
0x06	DIAGNOSTIC-SCIA	16 Bytes
0x07	DIAGNOSTIC-SCIB	16 Bytes

Table 12-12: Example of APPLICATION-TELEMETRY Command inside a telecommand NSP Packet

Field	FEND	Destination	Source	Message Control Field				Data	CRC	FEND
				P	B	A	Command			
Length	1 Byte	1 Byte	1 Byte	1 Byte				1 Byte (Data)	2 Bytes	1 Byte
Content	0xC0	0x01	0x11	0b10000111				0x00	0xXXXX	0xC0

12.5.2 Reply Format of the APPLICATION-TELEMETRY Command

The NRWA-T6 will reply to any APPLICATION-TELEMETRY telecommand (provided the "Poll" bit is set) with a NSP message in the format detailed in Section 11.2.

The "A" bit is set to indicate an ACK – that the telecommand has successfully executed. If the "A" bit is clear a NACK is indicated – there has been a problem, and the telecommand has not executed.

12.5.2.1 STANDARD Data Block

The data field format of the reply message for the STANDARD Data Block type of the APPLICATION-TELEMETRY Command is shown in Table 12-13.

Table 12-13: APPLICATION-TELEMETRY STANDARD Data Block Content

Length	Field	Function	Format
4 Bytes	Status register	State and health flag register	32-Bit Unsigned
4 Bytes	Fault register	Latching fault flag register	32-Bit Unsigned
1 Byte	Control Mode register	Controller mode state register. Indicates the active wheel control mode.	8-Bit Unsigned
4 Bytes	Control setpoint	Setpoint of the active control mode (CURRENT)	Q14.18 (mA)
		Setpoint of the active control mode (SPEED)	Q14.18 (RPM)
		Setpoint of the active control mode (TORQUE)	Q10.22 (mN-m)
		Setpoint of the active control mode (PWM)	32-Bit Signed (Absolute value of the least significant 9 bits is the drive duty cycle. The sign is the drive direction.)
2 Bytes	PWM duty cycle	Motor drive PWM duty cycle	16-Bit Signed (Absolute value of the least significant 9 bits is the drive duty cycle. The sign is the drive direction.)
2 Bytes	Current control target	Target motor current	Q14.2 (mA)
4 Bytes	Current measurement	Motor phase current measurement	Q20.12 (mA)
4 Bytes	Speed measurement	Motor speed measurement	Q24.8 (RPM)

12.5.2.1.1 Status Register Contents

The Status register contents are detailed in Table 12-14.

Table 12-14: Status register contents

Bit	Field	Function
0	RAM boot state	This flag is asserted when the initialization from device FROM of the Initialized Parameters address range in device RAM is completed.
1	Motor drive fault	Motor drive fault condition indicating an overtemperature shutdown event. This signal is asserted by the motor drive when it enters an over temperature protection state when the drive junction exceeds 150°C.
2	Motor drive OTW	Motor drive over temperature warning flag. This signal is asserted by the motor drive when the drive junction exceeds 125°C.
3	Overvoltage limited	Flag indicating that overvoltage protection has been enabled due to the set overvoltage limit on the 30V supply rail being exceeded. The motor drive is in a high-impedance state when this flag is active.
4	Overspeed limited	Flag indicating that the set closed-loop overspeed limit has been reached and the closed-loop speed/torque controller might not reach its target setpoint.
5	Overpower limited	Flag indicating that the set motor power limit has been reached and that the closed-loop motor current target is being limited.
6	Current limited	Flag indicating that the set closed-loop motor current limit has been reached.
7	PWM limited	Flag indicating that the drive PWM duty cycle is being limited, this condition will occur when the required motor drive duty cycle has reached its upper limit.
8	Motor direction	Flag indicating the motor rotation direction as determined from the motor Hall sensors. (0 => Anti-Clockwise, 1 => Clockwise).
9	Drive state	Indication of the motor drive state. (0 => High-Z, 1 => Commutating)

10	Drive polarity	Flag indicating the motor drive commutation polarity. (0 => Positive, 1 => Negative).
11	Braking dynamic load active	Flag indicating that the active braking dynamic load is active and sinking power from the 30V supply rail to avoid an overvoltage condition due to the motor drive operating in a braking quadrant.
12	Speed timeout	Flag indicating that no Hall sensor transitions have been detected over a set period, and the speed measurement has defaulted to a 0RPM measurement.
13	Hall A	Flag indicating the motor Hall sensor A state (0 => low, 1 => high).
14	Hall B	Flag indicating the motor Hall sensor B state (0 => low, 1 => high).
15	Hall C	Flag indicating the motor Hall sensor C state (0 => low, 1 => high).
16	Motor Hall sensor invalid state	Flag indicating that the motor Hall sensors are in an invalid state (000 or 111). The motor drive is in a high-impedance state when this flag is active.
17	Overspeed-fault protection disabled	Overspeed-fault intervention disabled flag. (0 => protection enabled, 1 => protection disabled)
18	Overspeed-limit protection disabled	Overspeed-limit protection disabled flag. (0 => protection enabled, 1 => protection disabled)
19	Overcurrent-limit protection disabled	Motor overcurrent-limit disabled flag. (0 => protection enabled, 1 => protection disabled)
20	EDAC scrub disabled	Scrubbing of the EDAC protected SRAM disabled flag. (0 => scrub enabled, 1 => scrub disabled)
21	Braking overvoltage-load disabled	Braking overvoltage-load disabled flag. (0 => load enabled, 1 => load disabled)
22	PGOOD 1V5	+1.5V Supply power good flag (0 => fault, 1 => ok).
23	PGOOD 3V3	+3.3V Supply power good flag (0 => fault, 1 => ok).
24	PGOOD 5VA	+5V (Analog) Supply power good flag (0 => fault, 1 => ok).
25	PGOOD 3V3M	+3.3V (Monitor) Supply power good flag (0 => fault, 1 => ok).
26	PGOOD 5VD	+5V (Digital) Supply power good flag (0 => fault, 1 => ok).
27	PGOOD 3V3I	+3.3V (Interface) Supply power good flag (0 => fault, 1 => ok).
28	PGOOD 12V	+12V Supply power good flag (0 => fault, 1 => ok).
29-31	RESERVED	-

12.5.2.1.2 Fault Register Contents

The Fault register contents are detailed in Table 12-15. Note that the Fault register is a latching flag register, any flag signal will be latched high until it is cleared using the CLEAR-FAULT Command [0x09].

Table 12-15: Fault register contents

Bit	Field	Function
0	Motor drive fault	Motor drive fault condition indicating an overtemperature shutdown event. This signal is asserted by the motor drive when it enters an over temperature protection state when the motor drive junction exceeds 150°C.
1	Motor drive OTW	Motor drive over temperature warning flag. This signal is asserted by the motor drive when the motor drive junction exceeds 125°C.
2	Motor Hall sensor invalid state	Flag indicating that the motor Hall sensors are in an invalid state (000 or 111). The motor drive is in a high-impedance state when this flag is active.
3	Motor Hall sensor invalid transition	Flag indicating that an invalid sequence transition has been detected on the motor Hall sensors inputs.
4	Overvoltage fault	Flag indicating that overvoltage protection has been enabled due to the set overvoltage limit on the 30V supply rail being exceeded.
5	Overspeed fault	Flag indicating that the overspeed fault protection has been triggered due to the set overspeed-fault threshold being exceeded. The motor drive is in a high-impedance state when this flag is active. Clearing this flag returns the drive to normal operating state.
6	Overspeed limited	Flag indicating that the set closed-loop overspeed limit has been reached and the closed-loop speed/torque controller might not reach its target setpoint.
7	Overpower limited	Flag indicating that the set motor power limit has been reached and that the closed-loop motor current target is being limited.

8	Current limited	Flag indicating that the set closed-loop motor current limit has been reached.
9	EDAC SEU Error	Flag indicating that an uncorrectable SEU has occurred in the EDAC protected SRAM.
10	RS485 Port A UART-Frame error	Flag indicating that a UART Frame error has occurred on RS485 Port A.
11	RS485 Port A SLIP Frame error	Flag indicating that a SLIP Frame error has occurred on RS485 Port A.
12	RS485 Port A CRC error	Flag indicating that a received message CRC error has occurred on RS485 Port A.
13	RS485 Port B UART-Frame error	Flag indicating that a UART Frame error has occurred on RS485 Port B.
14	RS485 Port B SLIP Frame error	Flag indicating that a SLIP Frame error has occurred on RS485 Port B.
15	RS485 Port B CRC error	Flag indicating that a received message CRC error has occurred on RS485 Port B.
16	PGOOD 1V5 fault	Flag indicating that a +1.5V Supply power good fault has occurred.
17	PGOOD 3V3 fault	Flag indicating that a +3.3V Supply power good fault has occurred.
18	PGOOD 5VA fault	Flag indicating that a +5V (Analog) Supply power good fault has occurred.
19	PGOOD 3V3M fault	Flag indicating that a +3.3V (Monitor) Supply power good fault has occurred.
20	PGOOD 5VD fault	Flag indicating that a +5V (Digital) Supply power good fault has occurred.
21	PGOOD 3V3I fault	Flag indicating that a +3.3V (Interface) Supply power good fault has occurred.
22	PGOOD 12V fault	Flag indicating that a +12V Supply power good fault has occurred.
23-31	RESERVED	-

12.5.2.2 TEMPERATURES Data Block

The data field format of the reply message for the TEMPERATURES Data Block type of the APPLICATION-TELEMETRY Command is shown in Table 12-16.

Table 12-16: APPLICATION-TELEMETRY TEMPERATURES Data Block Content

Length	Field	Function	Format
2 Bytes	DC-DC Temperature (Temperature reference point 1)	Temperature measurement of the electrically isolated DC-DC converter module. Conversion parameters: $\mathrm{R_s} = 10\mathrm{k}[\Omega], \mathrm{R_p} = 100\mathrm{k}[\Omega], \mathrm{T_{25}} = 298.15[\mathrm{K}], \mathrm{R_{25}} = 10\mathrm{k}[\Omega], \mathrm{beta} = 3450.$	16-Bit Unsigned
2 Bytes	Enclosure Temperature (Temperature reference point 2)	Temperature measurement of the enclosure interior. Conversion parameters: $\mathrm{R_s} = 10\mathrm{k}[\Omega], \mathrm{R_p} = 100\mathrm{k}[\Omega], \mathrm{T_{25}} = 298.15[\mathrm{K}], \mathrm{R_{25}} = 10\mathrm{k}[\Omega], \mathrm{beta} = 3450.$	16-Bit Unsigned
2 Bytes	Motor Driver Temperature (Temperature reference point 3)	Temperature measurement of the motor driver. Conversion parameters: $\mathrm{R_s} = 10\mathrm{k}[\Omega], \mathrm{R_p} = 100\mathrm{k}[\Omega], \mathrm{T_{25}} = 298.15[\mathrm{K}], \mathrm{R_{25}} = 10\mathrm{k}[\Omega], \mathrm{beta} = 3450.$	16-Bit Unsigned
2 Bytes	Motor Temperature (Temperature reference point 4)	Temperature measurement acquired from the parallel thermistors located on the motor PCB. Conversion parameters: $\mathrm{R_s} = 5.1\mathrm{k}[\Omega], \mathrm{R_p} = 100\mathrm{k}[\Omega], \mathrm{T_{25}} = 298.15[\mathrm{K}], \mathrm{R_{25}} = 5\mathrm{k}[\Omega], \mathrm{beta} = 3490.$	16-Bit Unsigned

12.5.2.2.1 Raw Value to Temperature Conversion

The resistance of the NTC thermistors can be calculated from the raw value provided in telemetry by using Equation (1) below:

$$R_{TH} = \frac{x_{uint16} \cdot R_p \cdot R_s}{2^{12} \cdot R_p - x_{uint16} \cdot R_p - x_{uint16} \cdot R_s} \tag{1}$$

The measured temperature in Kelvin can be calculated from each previously calculated NTC thermistor resistance using Equation (2) below:

$$T(R) = \frac{1}{\frac{ln(\frac{R_{TH}}{R_{25}})}{beta} + \frac{1}{T_{25}}} [K] \tag{2}$$

12.5.2.3 VOLTAGES Data Block

The data field format of the reply message for the VOLTAGES Data Block type of the APPLICATION-TELEMETRY Command is shown in Table 12-17.

Table 12-17: APPLICATION-TELEMETRY VOLTAGES Data Block Content

Length	Field	Function	Format
4 Bytes	Monitor 1V5 supply voltage	Voltage measurement of the +1.5V supply rail	UQ16.16 (V)
4 Bytes	Monitor 3V3 supply voltage	Voltage measurement of the +3.3V supply rail	UQ16.16 (V)
4 Bytes	Monitor Analog 5V supply voltage	Voltage measurement of the +5V (Analog) supply rail	UQ16.16 (V)
4 Bytes	Monitor 12V supply voltage	Voltage measurement of the +12V supply rail	UQ16.16 (V)
4 Bytes	Monitor 30V supply voltage	Voltage measurement of the +30V supply rail	UQ16.16 (V)
4 Bytes	Monitor 2V5 reference voltage	Voltage measurement of the +2.5V reference	UQ16.16 (V)

12.5.2.4 CURRENTS Data Block

The data field format of the reply message for the CURRENTS Data Block type of the APPLICATION-TELEMETRY Command is shown in Table 12-18.

Table 12-18: APPLICATION-TELEMETRY CURRENTS Data Block Content

Length	Field	Function	Format
4 Bytes	Monitor 1V5 supply current	Measurement of the current drawn from the +1.5V supply rail	UQ16.16 (mA)
4 Bytes	Monitor 3V3 supply current	Measurement of the current drawn from the +3.3V supply rail	UQ16.16 (mA)
4 Bytes	Monitor Analog 5V supply current	Measurement of the current drawn from the +5V (Analog) supply rail	UQ16.16 (mA)
4 Bytes	Monitor Digital 5V supply current	Measurement of the current drawn from the +5V (Digital) supply rail	UQ16.16 (mA)
4 Bytes	Monitor 12V supply current	Measurement of the current drawn from the +12V supply rail	UQ16.16 (mA)
4 Bytes	Monitor 30V supply current	Measurement of the current drawn from the +30V supply rail	Q16.16 (A)

12.5.2.5 DIAGNOSTICS-GENERAL Data Block

The data field format of the reply message for the DIAGNOSTICS-GENERAL Data Block type of the APPLICATION-TELEMETRY Command is shown in Table 12-19.

Table 12-19: APPLICATION-TELEMETRY DIAGNOSTICS-GENERAL Data Block Content

Length	Field	Function	Format
4 Bytes	Uptime counter	Unit uptime counter	UQ30.2 (s)
4 Bytes	Revolution count	Flywheel revolution counter	32-Bit Unsigned
4 Bytes	Motor Hall sensor invalid transition count	Motor Hall sensor invalid sequence transition count	32-Bit Unsigned
4 Bytes	Drive-Fault count	Motor drive fault condition count	32-Bit Unsigned
4 Bytes	Drive-Overtemperature count	Motor drive overtemperature condition count	32-Bit Unsigned

12.5.2.6 DIAGNOSTICS-EDAC Data Block

The data field format of the reply message for the DIAGNOSTICS-EDAC Data Block type of the APPLICATION-TELEMETRY Command is shown in Table 12-20.

Table 12-20: APPLICATION-TELEMETRY DIAGNOSTICS-EDAC Data Block Content

Length	Field	Function	Format
4 Bytes	EDAC RAM Correctable SEU count	EDAC RAM Correctable SEU count	32-Bit Unsigned
4 Bytes	EDAC RAM ERROR SEU count	EDAC RAM ERROR SEU count	32-Bit Unsigned
4 Bytes	EDAC RAM Write usage	EDAC RAM Controller Write usage, where 100% usage = 0x00FFFFFF	32-Bit Unsigned
4 Bytes	EDAC RAM Read usage	EDAC RAM Controller Read usage, where 100% usage = 0x00FFFFFF	32-Bit Unsigned
4 Bytes	EDAC RAM Scrub count	EDAC RAM Scrub procedures completed	32-Bit Unsigned

12.5.2.7 DIAGNOSTICS-SCIA Data Block

The data field format of the reply message for the DIAGNOSTICS-SCIA Data Block type of the APPLICATION-TELEMETRY Command is shown in Table 12-21.

Table 12-21: APPLICATION-TELEMETRY DIAGNOSTICS-SCIA Data Block Content

Length	Field	Function	Format
4 Bytes	RXD Bytes received count	RS485 Port A UART Bytes received	32-Bit Unsigned
4 Bytes	TXD Bytes transmitted count	RS485 Port A UART Bytes transmitted	32-Bit Unsigned
4 Bytes	RXD NSP Received count	RS485 Port A NSP Message received count	32-Bit Unsigned
4 Bytes	RXD NSP Discarded count	RS485 Port A NSP Message discarded count	32-Bit Unsigned

12.5.2.8 DIAGNOSTICS-SCIB Data Block

The data field format of the reply message for the DIAGNOSTICS-SCIB Data Block type of the APPLICATION-TELEMETRY Command is shown in Table 12-22.

Table 12-22: APPLICATION-TELEMETRY DIAGNOSTICS-SCIB Data Block Content

Length	Field	Function	Format
4 Bytes	R-RXD Bytes received count	RS485 Port B UART Bytes received	32-Bit Unsigned
4 Bytes	R-TXD Bytes transmitted count	RS485 Port B UART Bytes transmitted	32-Bit Unsigned
4 Bytes	R-RXD NSP Received count	RS485 Port B NSP Message received count	32-Bit Unsigned
4 Bytes	R-RXD NSP Discarded count	RS485 Port B NSP Message discarded count	32-Bit Unsigned

12.6 APPLICATION-COMMAND Command [0x08]

The APPLICATION-COMMAND Command is used to set and update the WDE drive mode and parameters as well as controller mode, parameters and setpoints associated with standard reaction wheel operation.

12.6.1 Telecommand Format of the APPLICATION-COMMAND Command

The data field of the NSP telecommand consists of the Control-mode register followed by the relevant parameters and setpoints as shown in Table 12-23.

Table 12-23: APPLICATION-COMMAND Data Field Content

Length	Field	Function	Format
1 Byte	Control-mode register	WDE Control mode	8-Bit Unsigned
4 Bytes	Control-mode setpoint	Current controller setpoint	Q14.18 (mA)
		Speed controller setpoint	Q14.18 (RPM)
		Torque controller setpoint	Q10.22 (mN-m)
		Low-level PWM duty cycle	32-Bit Signed (Absolute value of the least significant 9 bits is the drive duty cycle. The sign is the drive direction.)

The contents of the Control-mode register are defined in Table 12-24.

Table 12-24: Control-mode register contents

Bit	Field	Function
0 (LSB)	WDE Control-mode identifier	Sets or updates the WDE control-mode as described in Table 12-25.
1		
2		
3		
4-6	RESERVED	-
7	Debug enable	Set to low/0 for nominal operation

Table 12-25: WDE Control-mode identifier

Value	Field	Function
0b0000 or any state not defined below	IDLE	Motor drive will be in high-Z mode. No active control of the motor current and speed is performed, and freewheeling will occur if the flywheel is at speed.
0b0001	CURRENT-Control	The motor drive will be commutated according to the motor Hall sensor outputs. Closed-loop current control is performed through in-phase sensing of the motor current and complementary PWM switching of the motor drive.
0b0010	SPEED-Control	The motor drive will be commutated according to the motor Hall sensor outputs. Closed-loop current control is active. Closed-loop speed control is performed through measuring the motor speed from the Hall sensor outputs and updating the current controller setpoint.
0b0100	TORQUE-Control	The motor drive will be commutated according to the motor Hall sensor outputs. Closed-loop current control is active. Closed-loop torque control is estimated through estimating the motor acceleration from the Hall sensor inputs and updating the current controller setpoint.
0b1000	PWM-Control	Direct control over the duty cycle of the PWM switching of the motor drive. The motor drive will be commutated according to the motor Hall sensor outputs. To be used when no closed-loop control of the motor current or speed by the WDE controller is desired.

Table 12-26 shows an example of the APPLICATION-COMMAND with the control mode identifier set to CURRENT-Control, the Braking overvoltage-load enabled and the Control-mode setpoint set to 1000mA.

Table 12-26: Example of APPLICATION-COMMAND Command inside a telecommand NSP Packet

Field	FEND	Destination	Source	Message Control Field				Data	CRC	FEND
				P	B	A	Command			
Length	1 Byte	1 Byte	1 Byte	1 Byte				5 Bytes	2 Bytes	1 Byte
Content	0xC0	0x01	0x11	0b10001000				0x810FA00000	0xXXXX	0xC0

12.6.2 Reply Format of the APPLICATION-COMMAND Command

The NRWA-T6 will reply to any APPLICATION-COMMAND telecommand (provided the “Poll” bit is set) with a NSP message in the format detailed in Section 11.2. The data field of the reply message will contain only a read of the updated Control-mode register from RAM.

The “A” bit is set to indicate an ACK – that the telecommand has successfully executed. If the “A” bit is clear a NACK is indicated – there has been a problem, and the telecommand has not executed.

A reply to the example telecommand is shown below in Table 12-27.

Table 12-27: Example of the reply to an APPLICATION-COMMAND

Field	FEND	Destination	Source	Message Control Field				Data	CRC	FEND
				P	B	A	Command			
Length	1 Byte	1 Byte	1 Byte	1 Byte				1 Byte	2 Bytes	1 Byte
Content	0xC0	0x11	0x01	0b10101000				0x81	0xXXXX	0xC0

12.7 CLEAR-FAULT Command [0x09]

The CLEAR-FAULT Command is used to clear the flags latched in the Fault register. This command:

- Selectively clears flags latched in the Fault register.
- Does not change any modes or toggle any logical switches.
- Is only used to clear the register.

12.7.1 Telecommand Format of the CLEAR-FAULT Command

The data field of the NSP telecommand for the CLEAR-FAULT command consists of 32 bits corresponding to the relevant flags in the Fault register to be cleared. A latched Flag will be cleared when its corresponding bit in the data field of the CLEAR-FAULT Command is set. See Table 12-28 for a definition of the Fault register contents.

Table 12-28: Example of a CLEAR-FAULT command inside a telecommand NSP packet, clearing the “Drive Fault” flag

Field	FEND	Destination	Source	Message Control Field				Data	CRC	FEND
				P	B	A	Command			
Length	1 Byte	1 Byte	1 Byte	1 Byte				4 bytes	2 Bytes	1 Byte
Content	0xC0	0x01	0x11	0b10101001				0x00000001	0xXXXX	0xC0

12.7.2 Reply Format of the CLEAR-FAULT Command

The NRWA-T6 will reply to any CLEAR-FAULT telecommand (provided the "Poll" bit is set) with a NSP message in the format detailed in Section 11.2. The data field of the NSP message will be empty.

The "A" bit is set to indicate an ACK – that the telecommand has successfully executed. If the "A" bit is clear a NACK is indicated – there has been a problem, and the telecommand has not executed.

12.8 CONFIGURE-PROTECTION Command [0x0A]

The CONFIGURE-PROTECTION Command is used to enable/disable supported protection mechanisms of the NRWA-T6's drive electronics.

12.8.1 Telecommand Format of the CONFIGURE-PROTECTION Command

The data field of this NSP telecommand consists of 32 bits corresponding to the relevant protection enable/disable fields, as defined in Table 12-29 below.

Table 12-29: CONFIGURE-PROTECTION Command Data Field Content

Bit	Field	Function	Format
0	Overspeed-fault disable bit	Disable overspeed-fault intervention.	Disabled=1
1	Overspeed-limit disable bit	Disable overspeed-limit during closed-loop speed/torque control.	Disabled=1
2	Overcurrent-limit disable bit	Disable motor overcurrent-limit during closed-loop current/speed/torque control.	Disabled=1
3	EDAC scrub disable bit	Disable the periodic scrubbing of the EDAC protected SRAM.	Disabled=1
4	Braking overvoltage-load disable bit	Disable closed-loop loading of the 30V power rail to prevent overvoltage due to regenerated power during deceleration of the flywheel.	Disabled=1
5-31	RESERVED	-	-

Table 12-30 shows an example of the CONFIGURE-PROTECTION command with Overcurrent-limit protection disabled and all other protection mechanisms enabled.

Table 12-30: Example of CONFIGURE-PROTECTION Command inside a telecommand NSP Packet

Field	FEND	Destination	Source	Message Control Field				Data	CRC	FEND
				P	B	A	Command			
Length	1 Byte	1 Byte	1 Byte	1 Byte				4 Bytes	2 Bytes	1 Byte
Content	0xC0	0x01	0x11	0b10001010				0x00000004	0xXXXX	0xC0

12.8.2 Reply Format of the CONFIGURE-PROTECTION Command

The NRWA-T6 will reply to any CONFIGURE-PROTECTION telecommand (provided the "Poll" bit is set) with a NSP message in the format detailed in Section 11.2. The data field of the NSP message will be empty.

The "A" bit is set to indicate an ACK – that the telecommand has successfully executed. If the "A" bit is clear a NACK is indicated – there has been a problem, and the telecommand has not executed.

12.9 TRIP-LCL Command [0x0B]

The TRIP-LCL Command is used to force trigger/trip the latching current limiter (LCL) protection mechanism of the NRWA-T6's drive electronics.

12.9.1 Telecommand Format of the TRIP-LCL Command

The data field of the NSP telecommand for the TRIP-LCL Command is empty. Table 12-31 shows an example of the TRIP-LCL command message.

Table 12-31: Example of TRIP-LCL Command inside a telecommand NSP Packet

Field	FEND	Destination	Source	Message Control Field				Data	CRC	FEND
				P	B	A	Command			
Length	1 Byte	1 Byte	1 Byte	1 Byte				0 Bytes	2 Bytes	1 Byte
Content	0xC0	0x01	0x11	0b10001011				-	0xXXXX	0xC0

12.9.2 Reply Format of the TRIP-LCL Command

The NRWA-T6 will not reply to a TRIP-LCL telecommand is the command is acknowledged and executed correctly due to the relevant power rails being disabled by the triggered/tripped LCL.

If the command is not acknowledged or executed the NRWA-T6 will reply (provided the "Poll" bit is set) with a NSP message in the format detailed in Section 11.2. The data field of the NSP message will be empty.