UCSD MAS WES268A - Lab 3 Report

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Contents

1 Part 1: Phase Estimation Using PLL

1.1 Manual PLL

1. - No narrative required for this section.

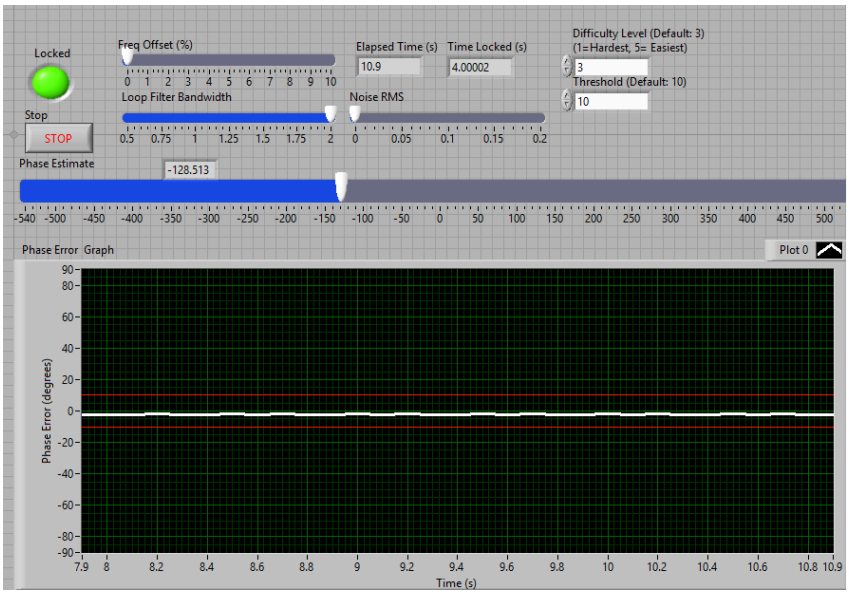

Figure 1: 1.1 - Output of Phase Detector with Freq. Offset = 0Hz, Bandwidth = 2, Noise = 0

1.2 Write-Up

1.2.1

Qualitatively explain the results of experiments using the manual PLL with respect to the loop-filter bandwidth, the amount of noise, and the speed of the loop's response.

Answer. With a wide loop filter the VCO sees plenty of low-frequency gain, so it wipes out frequency error almost immediately. The downside is that the same wide band lets noise into the loop, and even moderate noise ($\sigma \approx 0.2$) makes the phase jitter and can break lock. A narrow filter quiets the noise and keeps the phase steady, but the VCO now moves more slowly, so pull-in takes longer, especially when the initial offset is large. In short, wide bandwidth is fast but jittery, while narrow bandwidth is slow but steady.

2 Part 2: Performance of PLLs

2.1 Tracking the Frequency of a Sinusoidal Signal

2.1.1 Transmitter VI Setup

No narrative required for this section.

2.1.2 Receiver VI Setup

No narrative required for this section.

2.1.3 Basic Measurements

Loop Type	f_n	Δ_f	σ	ζ	**Freq. Pull-in**	**Phase Pull-in**
Costas	2kHz	5kHz	0	$1/\sqrt{2}$	1.25ms	1.7ms
Costas	2kHz	10kHz	0	$1/\sqrt{2}$	6.33ms	6.76ms
Standard	5kHz	5kHz	0.1	$1/\sqrt{2}$	61.63us	198.57us
Standard	10kHz	5kHz	0.1	$1/\sqrt{2}$	23.24us	48.59us
Standard	1kHz	5kHz	0.1	$1/\sqrt{2}$	3.19ms	3.99ms

Table 1: Frequency and Phase Pull-in Times for Data Modulated Signals

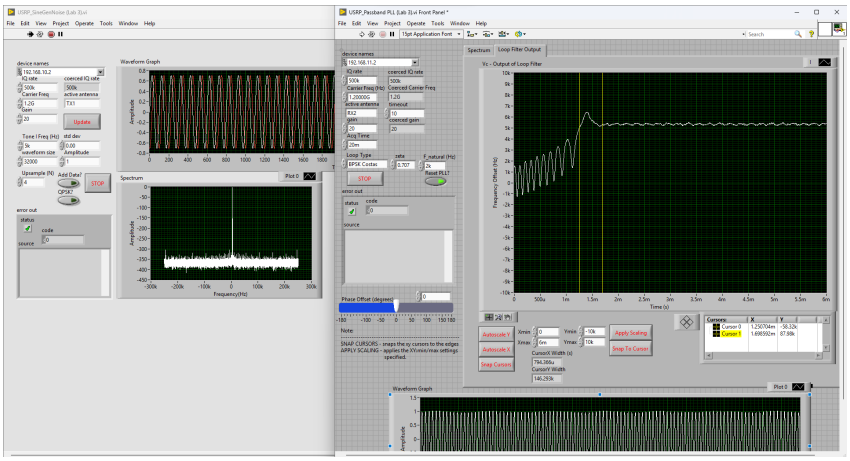

Figure 2: 2.1.3.1 - Costas PLL $f_n = 2$ kHz, $\Delta_f = 5$ kHz, $\sigma = 0$, $\zeta = 1/\sqrt{2}$

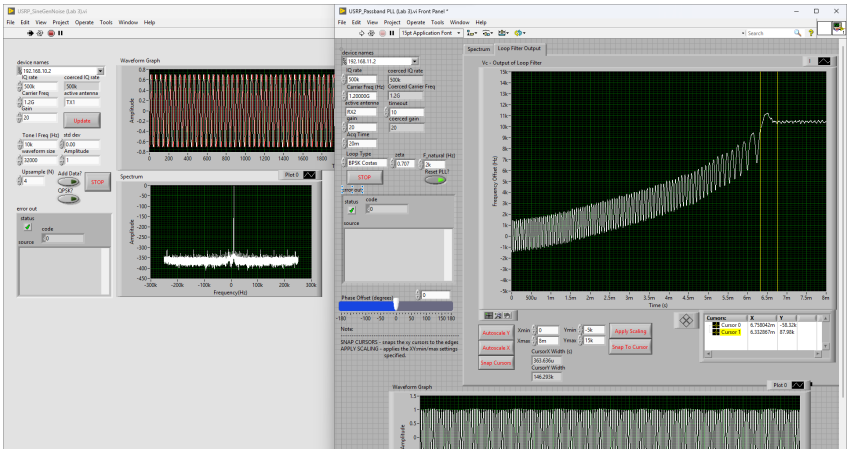

Figure 3: 2.1.3.2 - Costas PLL $f_n = 2$ kHz, $\Delta_f = 10$ kHz, $\sigma = 0$, $\zeta = 1/\sqrt{2}$

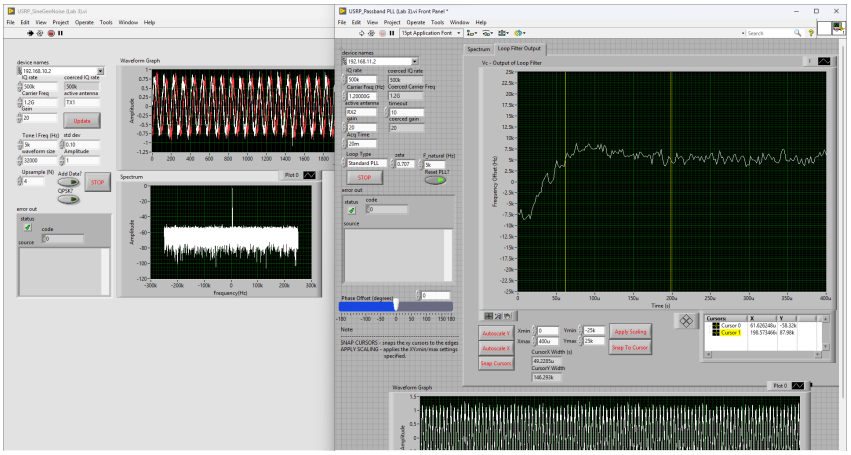

Figure 4: 2.1.3.6 - Standard PLL $f_n = 5$ kHz, $\Delta_f = 5$ kHz, $\sigma = 0.1$, $\zeta = 1/\sqrt{2}$

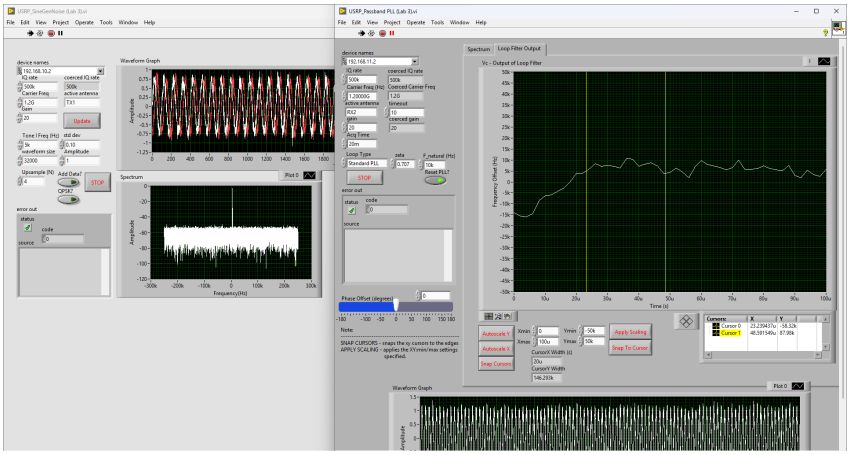

Figure 5: 2.1.3.7 - Standard PLL $f_n = 10$ kHz, $\Delta_f = 5$ kHz, $\sigma = 0.1$, $\zeta = 1/\sqrt{2}$

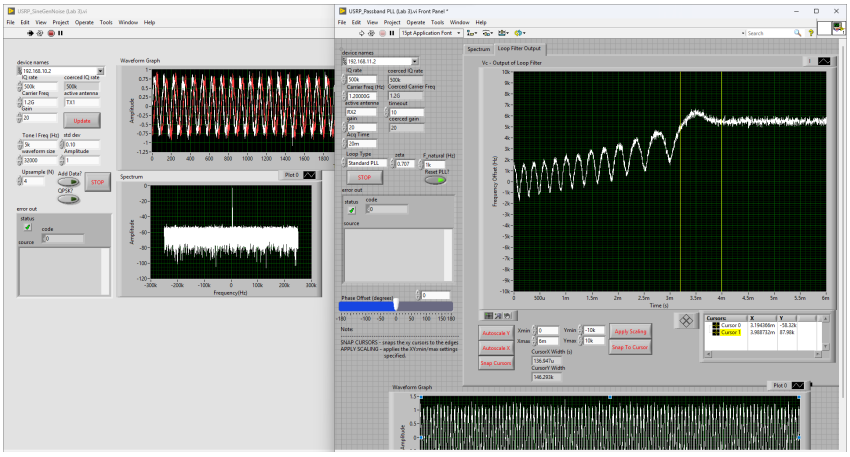

Figure 6: 2.1.3.8 - Standard PLL $f_n = 1$ kHz, $\Delta_f = 5$ kHz, $\sigma = 0.1$, $\zeta = 1/\sqrt{2}$

2.2 Tracking the Frequency of a Data Modulated Signal

2.2.1 Transmitter VI Setup

No narrative required for this section.

2.2.2 Receiver VI Setup

No narrative required for this section.

2.2.3 Measurements

Loop Type	f_n	Δ_f	σ	ζ	$\mathbb{M}$	**Freq. Pull-in**	**Phase Pull-in**
Standard	0.5kHz	4kHz	0	$1/\sqrt{2}$	1	NoTrack	NoTrack
Costas	0.5kHz	4kHz	0	$1/\sqrt{2}$	1	62.66ms	65.2ms
Standard	0.5kHz	4kHz	0	$1/\sqrt{2}$	2	NoTrack	NoTrack
Costas	0.5kHz	4kHz	0	$1/\sqrt{2}$	2	59.3ms	67.3ms

Table 2: Frequency and Phase Pull-in Times for Data Modulated Signals

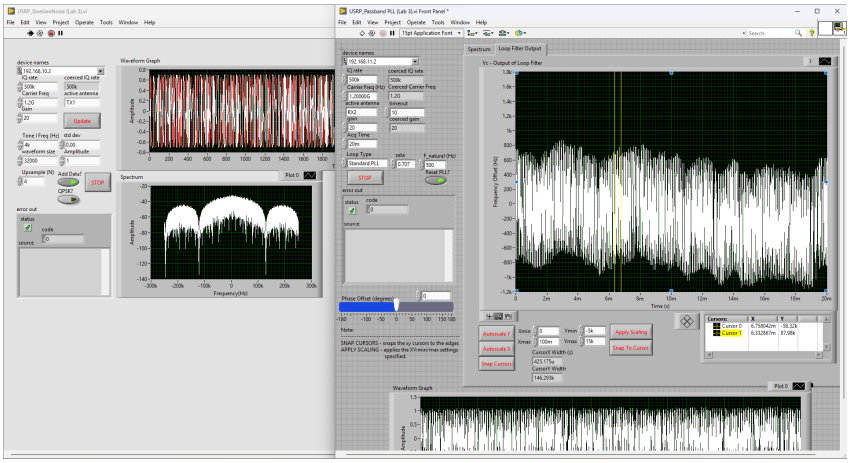

Figure 7: 2.2.3.1 - Standard PLL $f_n = 0.5$ kHz, $\Delta_f = 4$ kHz, $\sigma = 0$, $\zeta = 1/\sqrt{2}$, $\mathbb{M} = 1$

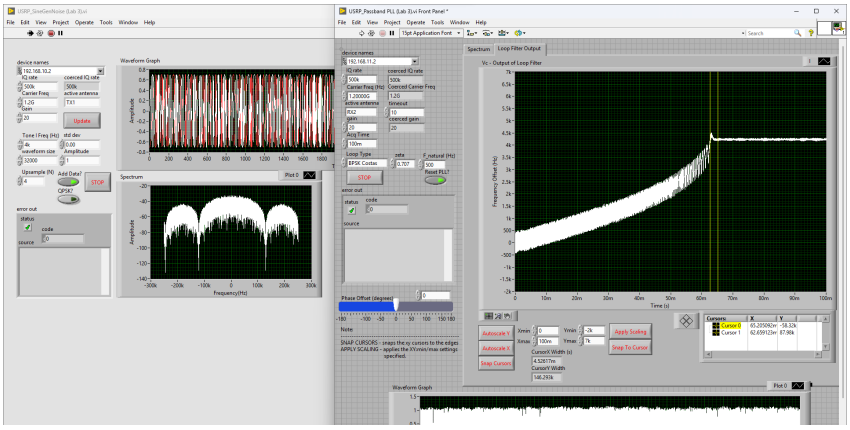

Figure 8: 2.2.3.2 - Costas PLL $f_n = 0.5$ kHz, $\Delta_f = 4$ kHz, $\sigma = 0, \zeta = 1/\sqrt{2}, \mathbb{M} = 1$

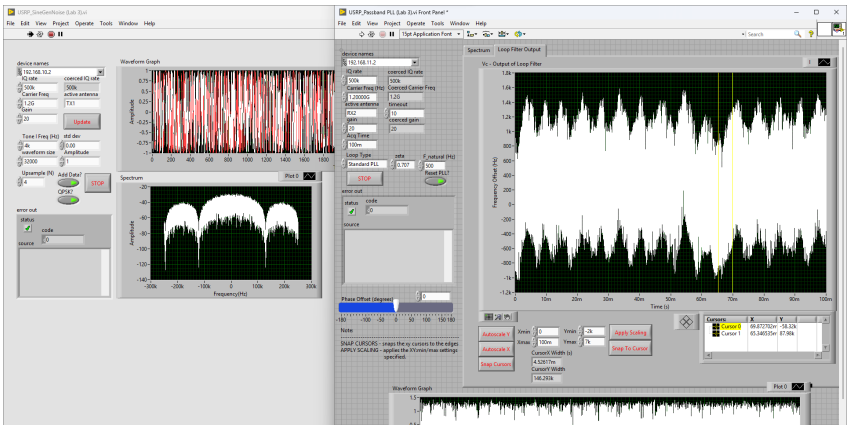

Figure 9: 2.2.3.3 - Standard PLL $f_n = 0.5$ kHz, $\Delta_f = 4$ kHz, $\sigma = 0, \zeta = 1/\sqrt{2}, \mathbb{M} = 2$

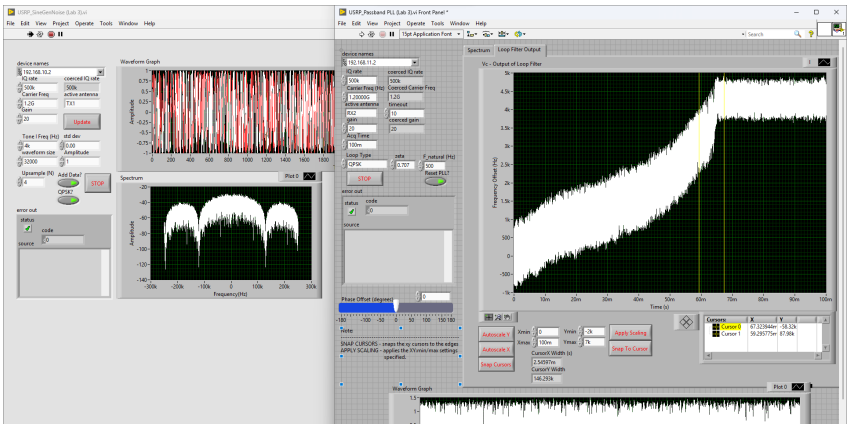

Figure 10: 2.2.3.4 - Costas PLL $f_n = 0.5$ kHz, $\Delta_f = 4$ kHz, $\sigma = 0, \zeta = 1/\sqrt{2}, \mathbb{M} = 2$

2.3 Write-Up

2.3.1

Using the data, discuss the relative performance of the PLLs with respect to the following parameters: (a) frequency-pull-in time vs. phase-pull-in time versus damping ζ;

(b) phase-pull-in time vs. total phase noise versus f_n;
(c) ability to lock in the presence of BPSK/QPSK data.
Answer. (a) Light damping ($\zeta < 1/\sqrt{2}$) pulls frequency in quickly but produces more ringing in the phase response. Heavy damping smooths the phase but lengthens the time needed to remove the frequency error. A critically damped loop sits between these two cases and gives a reasonable compromise between speed and overshoot.
(b) Raising f_n widens the loop bandwidth, so both the frequency pull-in time and the phase pull-in time decrease. The cost of this wider bandwidth is that the loop passes more noise, so the locked phase shows more jitter and a higher total phase noise level.
(c) A standard PLL does not lock when data flips the carrier phase each symbol because the data transitions look like additional phase error to the loop. A Costas loop multiplies the in-phase and quadrature components so that the data term cancels on average and the carrier component can be tracked.

2.3.2

How would you create a PLL to track a general $2M$-PSK signal whose possible phases are $\phi_k = (2\pi/2M)k$?
Answer. Raise the received signal $r(t) = Ae^{j(\omega_c t+\phi_k)}$ to the $2M$-th power: $r^{2M}(t) = A^{2M}e^{j2M\omega_c t}$. The symbol phase disappears because $e^{j2M\phi_k} = 1$ for every allowed ϕ_k. Track this new carrier with a standard PLL running at $2M\omega_c$, then divide the recovered phase (or the NCO count) by $2M$ to obtain the original carrier phase. There is still a fixed phase ambiguity that can be resolved with a differential decoder or a short known preamble.

3 Part 3: Clock Estimation

3.1 Timing Recovery - Matched Filters

3.1.1 Receiver VI Setup

No narrative required for this section.

3.1.2 Transmitter VI Setup

No narrative required for this section.

3.1.3 Measurements

3.1.3.i Matched Filter Analysis

β	ζ
0	6.86
0.5	21.63
1.0	30.79

Table 3: Measured ζ for Different Roll-off Factors β

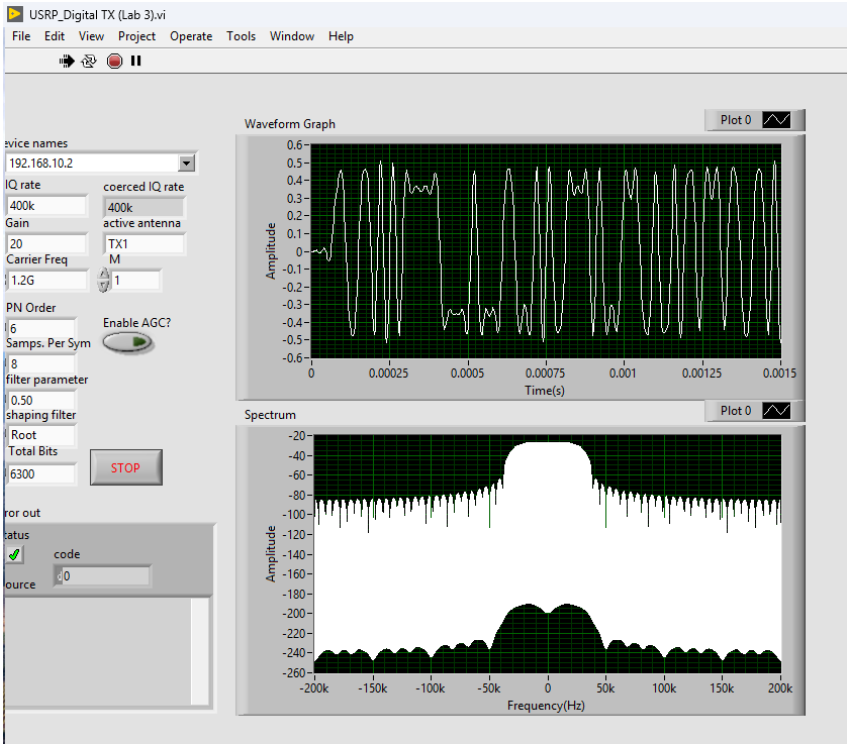

Figure 11: 3.1.3 - Transmitter Output Signal with Matched Filter

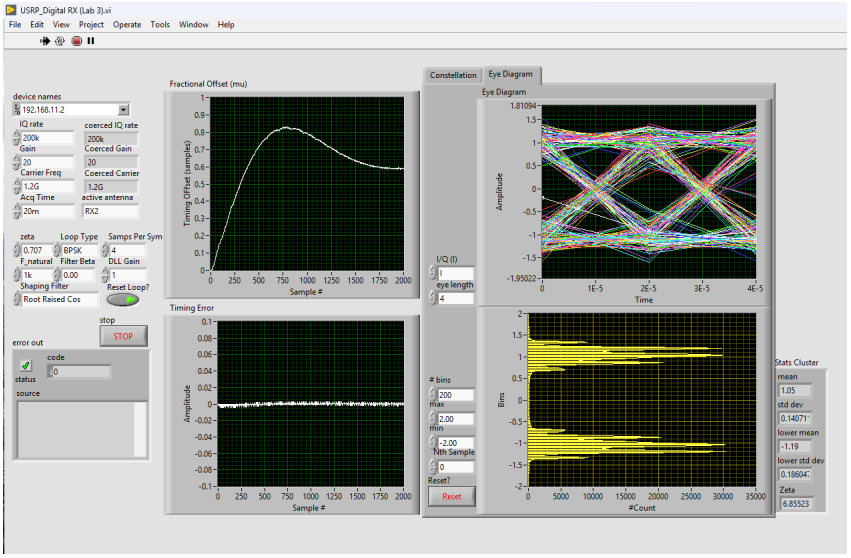

Figure 12: 3.1.3 - Receiver Output Signal with Matched Filter, $\beta = 0$

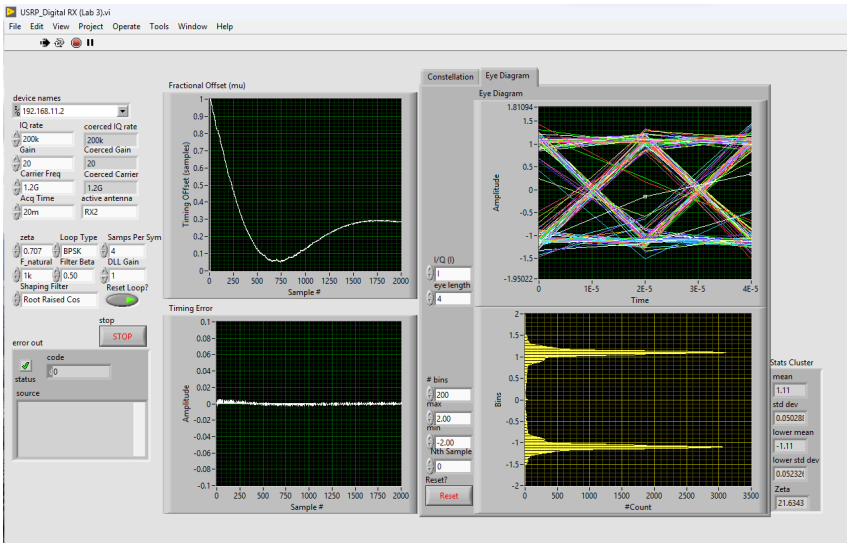

Figure 13: 3.1.3 - Receiver Output Signal with Matched Filter, $\beta = 0.5$

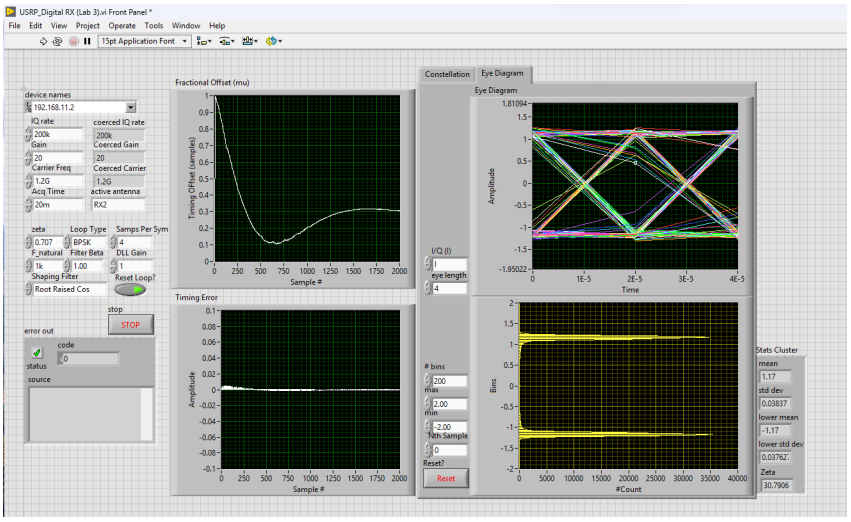

Figure 14: 3.1.3 - Receiver Output Signal with Matched Filter, $\beta = 1$

3.2 Write-Up

3.2.1

From the notes we know the Gardner algorithm is insensitive to carrier phase errors; therefore, symbol timing can be estimated before carrier phase. Briefly explain why this ordering is advantageous.
Answer: The Gardner detector forms products of samples separated by half a symbol, so a constant carrier phase multiplies every term by the same complex number and cancels out. Getting timing first centres each symbol, which boosts E_b/N_0 for the carrier loop, and it lets that carrier loop run with a narrower bandwidth, further reducing phase noise without risking loss of lock.

feelsgoodman