

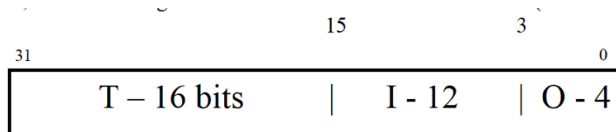
Section:

Name:

Email:

1. Draw and label the partitioning of the 32-bit memory address into the segments that are used to access the cache; Label each segment with its name and its width in bits. (shows bit numbers) **(5 points)**

Solution



A. Multiple Choice

For each of the following questions, select the option which is most often true: **(5 points)**

**Increases, decrease, doesn't affect**

- i. Increasing the capacity of a cache **Increases** its access time
- ii. Decreasing the capacity of a cache **Increases** its miss rate
- iii. Decreasing the capacity of a cache **doesn't effect** its miss penalty
- iv. Increasing a cache's hit rate **decrease** the effective average memory access time
- v. Assuming constant capacity, increasing a cache's block size (cache line size)  
**decrease or doesn't affect** the amount of tag storage required