

CS 261 Machine Organization Lab Week 15 Worksheet

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This week's lab we are going to examine the cache behavior.

Let's assume we have a memory system with the following properties:

The memory is byte addressable. Addresses are 14-bit wide (4 bits for the set index, 8 bits for tag and 2 bits for block offset).

The cache is a direct mapped cache that can hold 16 blocks (or has 16 lines) and each block is 4 bytes. The table shown below details the contents of the cache at a particular point in time. If the valid bit is 1, there is a cache block loaded into the cache with Tag as detailed in the "Tag" column. The columns B0-B3 then show the actual data in the cache block that is loaded in the cache. The "Set Index" column is an index for each of the positions in the cache.

Contents of a Cache at a particular instance of time:

| Set Index | Tag | Valid | B0 | B1 | B2 | B3 |
|-----------|-----|-------|----|----|----|----|
| 0 | 88 | 1 | FE | 96 | CA | D0 |
| 1 | 0B | 1 | 40 | 46 | 48 | 44 |
| 2 | 06 | 0 | - | - | - | - |
| 3 | 2D | 1 | 9A | 3D | 24 | 4C |
| 4 | 36 | 1 | 20 | 40 | FF | 32 |
| 5 | 32 | 0 | - | - | - | - |
| 6 | 24 | 0 | - | - | - | - |
| 7 | A8 | 1 | 9C | A4 | C1 | E0 |
| 8 | 40 | 1 | 12 | 45 | 82 | 88 |
| 9 | 60 | 1 | C0 | B3 | 68 | 62 |
| A | 40 | 1 | 18 | 21 | 80 | 54 |
| B | CC | 0 | - | - | - | - |
| C | 93 | 1 | DD | AB | 33 | 60 |
| D | 16 | 1 | A6 | 32 | BC | 93 |
| E | 33 | 0 | - | - | - | - |
| F | 54 | 1 | 86 | 80 | 36 | 06 |

[Note: All columns except column "Valid" are in hexadecimal representation.]

Answer the following questions for the cache as shown.

Please submit your answers by filling in the worksheet and submit to Gradescope.

1) How many bytes are in the main memory? (5 points)

2^{14}

2) How many bytes can the cache hold? (5 points)

64

3) How many blocks is the main memory divided into? (5 points)

2^{12}

4) How many blocks from the main memory want to be placed into the slot of set index B in the cache? (5 points)

2^8

5) Consider the following addresses that are each reading a single byte and detail whether they result in a hit or a miss in the cache. If the address results in a hit, then state the value that gets sent to the processor. (5 points x 4 = 20 points)

0b00110011111001

Miss

0b00010110110111

Hit - 93 is sent

0b00101110001110

Miss

0b00100100011000

Miss

6) Now go back to the original cache state (ignore any changes the above reads may have caused), and list 5 addresses, that are in 5 different blocks, that all result in hits in the cache. (20 points)

0b00100100010000

0b00001011000101

0b00110110010001

0b01000000101001

0b10010011110001

7) Now go back to the original cache state (ignore any changes the above reads may have caused), and list 5 addresses, that are in 5 different blocks, that all result in misses in the cache, and do not require data to be removed from the cache. (20 points)

0b11001100101100

0b00000110001000

0b00110010010100

0b00110011111000

0b00100100011000

8) Now go back to the original cache state (ignore any changes the above reads may have caused), and list 5 addresses, that are in 5 different blocks, that all result in misses in the cache and require data to be removed from the cache. (20 points)

0b00100100010000

0b00000110001000

0b00110010010100

0b00110011111000

0b00100100011000