```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 11/12/2019 05:24:28 PM
// Design Name:
// Module Name: counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module counter(
    input clk,
    input reset,
    output reg [2:0] count_o
    );

    always @(posedge clk or negedge reset) begin
        if(~reset) begin
            count_o <= 3'b000;
        end else if(clk) begin
            if(count_o < 3'b010)
                count_o <= count_o + 3'b001;
            if(count_o >= 3'b010)
                count_o <= count_o + 3'b010;
        end
    end
endmodule
```