```
module fib_series(series, enable, clock, reset);
   parameter n = 16;
   input enable;
   input clock;
   input reset;
   output [9:0] series;
   reg [9:0] series, prev1, prev2, temp;
   reg [1:0]count = 0;
   initial begin
     temp = 10'b0000000000;
     prev2 = 10'b0000000000;
     prev1 = 10'b0000000000;
     series = 10'b0000000000;
   end

   always @(posedge clock or negedge reset) begin
       if(reset) begin
           series = 10'b0000000000;
           prev2 = 10'b0000000000;
           prev1 = 10'b0000000000;
           temp = 10'b0000000000;
       end else if(enable) begin
           if(series == 10'b1111011011) begin
               series = 10'b0000000000;
               prev2 = 10'b0000000000;
               prev1 = 10'b0000000001;
               temp = 10'b0000000000;
           end else begin
               if((prev1 == 10'b0000000001)&&(prev2 == 10'b0000000000)&&(series ==
10'b0000000000))begin           // initial cases
                   series = 10'b0000000001;
                   temp = prev1 + prev2;
                   prev2 = prev1;
                   prev1 = series;
               end else if(prev1 == 10'b0000000000) begin
                   temp = prev1 + prev2;
                   series = temp;
                   prev2 = prev1;
                   prev1 = 10'b0000000001;
               end else begin
                   temp = prev1 + prev2;
                   series = temp;
                   prev2 = prev1;
                   prev1 = series;
               end
           end
```

```
        end
    end
endmodule
```