```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 11/10/2019 12:25:30 PM
// Design Name:
// Module Name: j_counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module j_counter(
    input clk,
    input reset,
    output reg [3:0] count
    );

    always @ (posedge clk or negedge reset) begin
        if(~reset) begin
            count <= 4'b0000;
        end else if(clk) begin
            count[2:0] <= count[3:1];
            count[3] <= ~count[0];
        end
    end
endmodule
```