```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 10/31/2019 03:47:38 PM
// Design Name:
// Module Name: question1
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module question1(clk, reset, in, out);
    input clk, reset, in;
    output reg out;
    reg out_int;
    reg [1:0] curr_state, next_state;
    parameter s0 = 2'b00, s1 = 2'b01, s2 = 2'b10, s3 = 2'b11;

    always@(posedge clk or posedge reset) begin
        if(reset) begin
            curr_state <= s0;
            out <= 0;
        end else begin
            curr_state <= next_state;
            out <= out_int;
        end
    end

    always@(*) begin
        case(curr_state)
            s0: begin
                next_state = (~in)?s1:s0;
                out_int = 1'b0;
                end
            s1: begin
```

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                next_state = (~in)?s2:s0;
                out_int = 1'b0;
                end
            s2: begin
                next_state = (~in)?s3:s0;
                out_int <= 1'b0;
                end
            s3: begin
                next_state = s0;
                out_int = 1'b1;
                end
        endcase
    end
endmodule
```