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EC413_Lab5

Modules:

ALU_32bit: The parameterized ALU, it contains all of the constituent modules along with the MUX.

FA_str: A structurally defined full 1-bit adder, takes two bits and a carry_in bit and outputs their sum and carry_out.

FA: A parameterized ripple-carry full adder where N = number of bits required, defaulted to 32-bits, and the outputs of which are the same as the structural full adder.

NOT_str: A structural NOT gate, used so that it can be more easily parameterized.

NOT_p: A parameterized bitwise NOT gate series.

AND_str: A structural AND gate, used so that it can be more easily parameterized.

AND_p: A parameterized bitwise AND gate series.

OR_str: A structural OR gate, used so that it can be more easily parameterized.

OR_p: A parameterized bitwise OR gate series.

FS: A parameterized full subtractor, it uses the already defined FA and NOT_p modules, as a subtractor can be seen as a simple full-adder with an inverted input and added 1.

dff: A behaviourally coded D Flip-Flop that is positive clock edge triggered and simply sets the output bit to the input bit every clock cycle.

REG_p: A parameterized register composed of a series of D Flip-Flops that is positive clock edge triggered.

Waveforms:

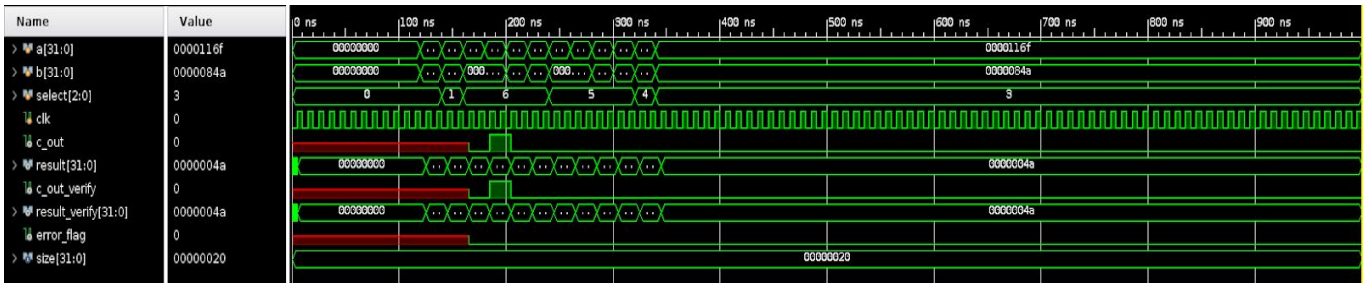

Figure 1.1: The waveforms from tb_ALU, the error flag is undefined in the beginning as c_out is undefined until the add function is called.