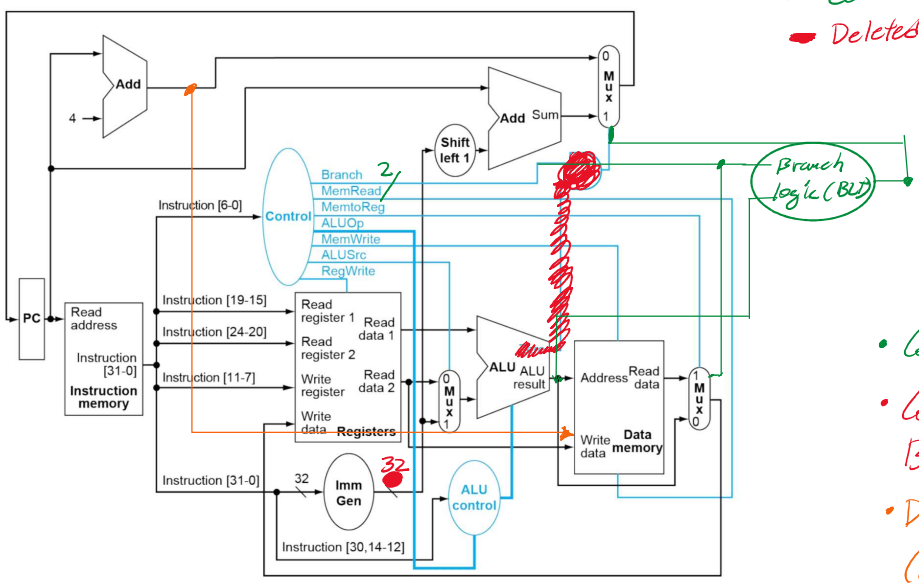
Control added Datapath added
Deleted



*Images were taken from Hennessy Patterson Book [1].

- Control added for BLT op
- Control deleted, no need since BEQ was not present
- Datapath added for JALR (store RA into Reg)

Instruction	Opcode	RegWrite	AluSrc	Branch	MemRe	MemWr	MemtoReg	ALUOp
R-type	0110011	1	0	00	0	0	0	10
I-type	0010011	1	1	00	0	0	0	00
lw	0000011	1	1	00	1	0	1	00
sw	0100011	0	1	00	0	1	0	00
BLT	1100011	0	0	01	0	0	0	01
JALR	1100111	1	1	10	0	0	0	00

1. The total number of cycles for running “All” trace is 14 cycles.
2. There are two R-type instructions
3. IPC of the processor is 1, because for one cycle(one while loop iteration), only one instruction is fetched and being ran.