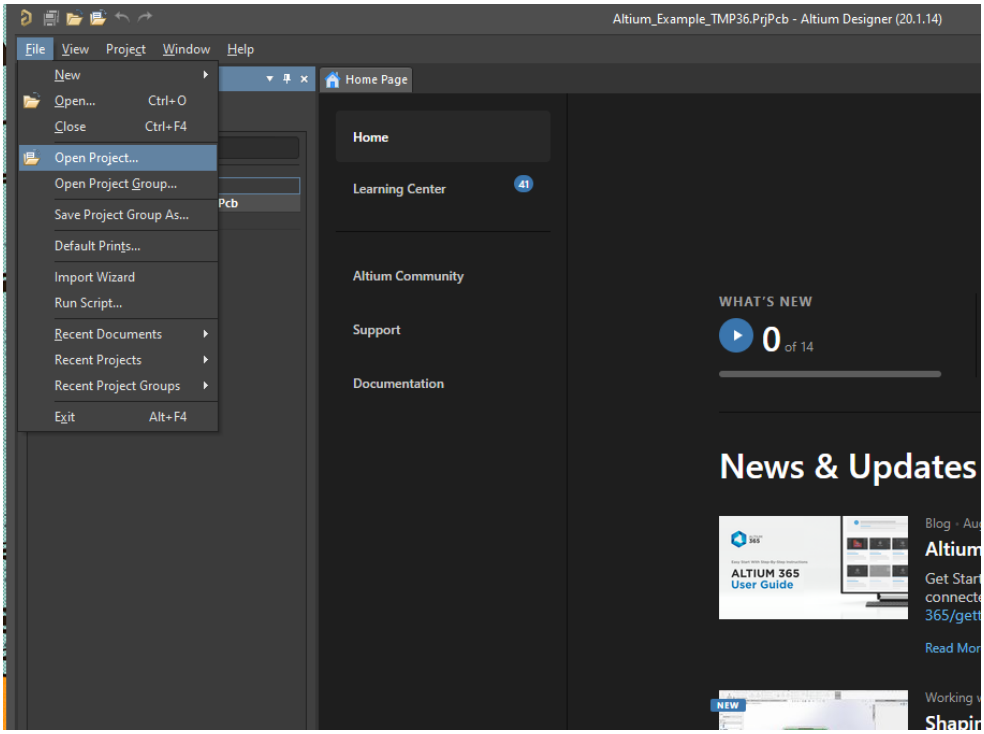
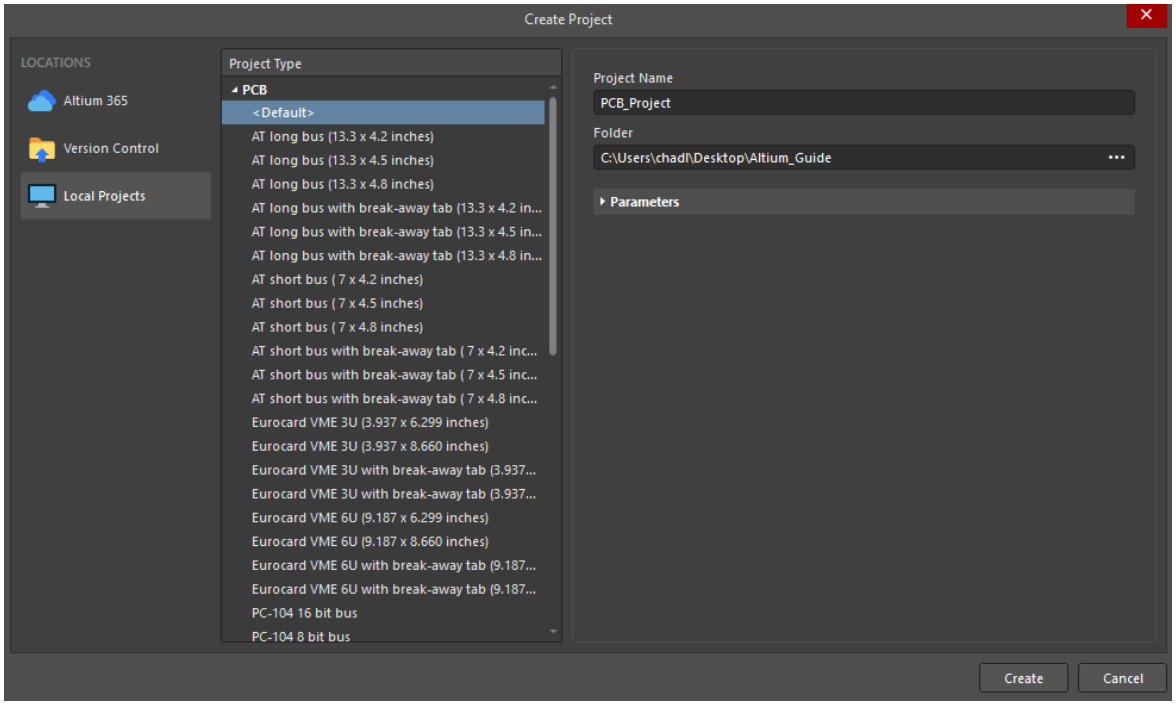
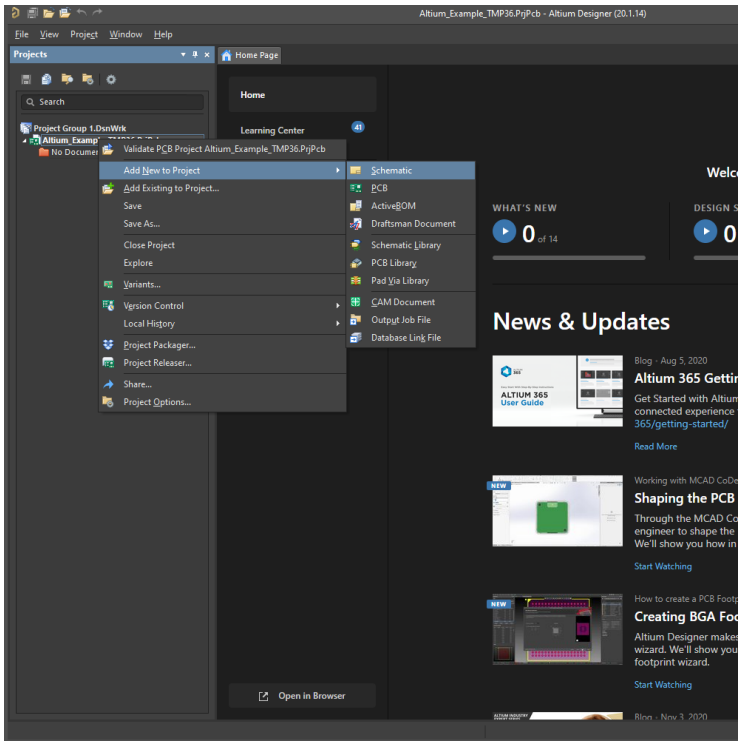
1. **Create a project** in Altium:



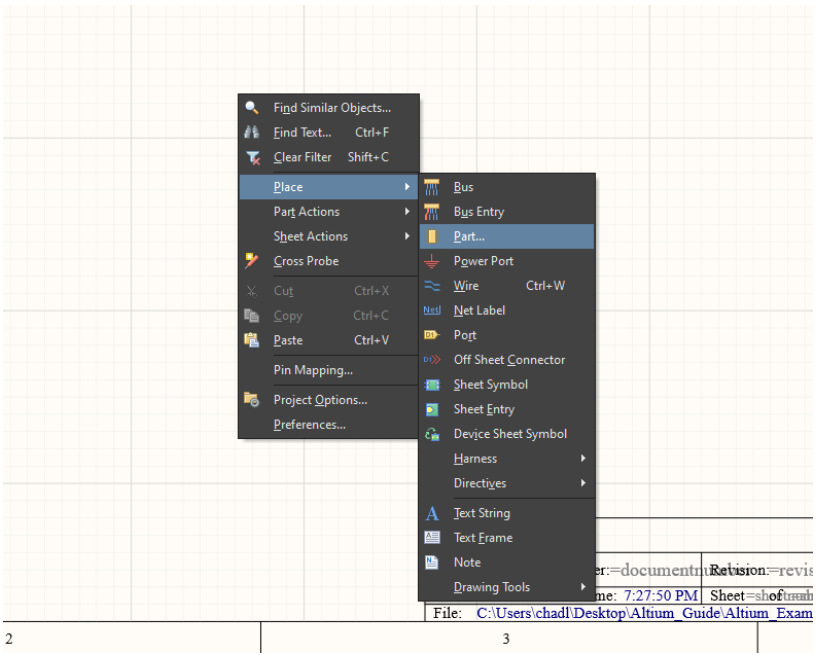
Choose a place for your project:



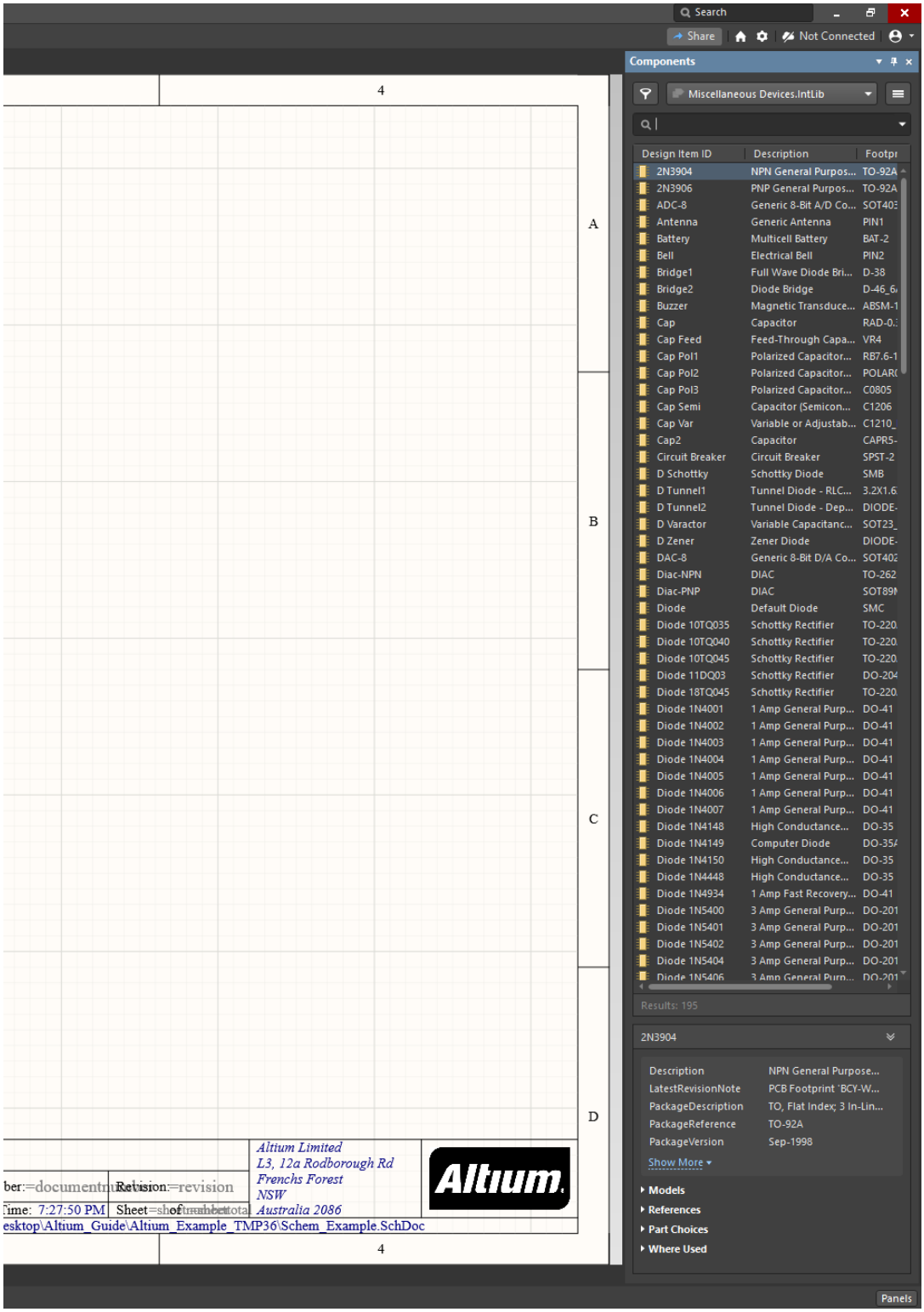
2. **Add schematic file** to project:



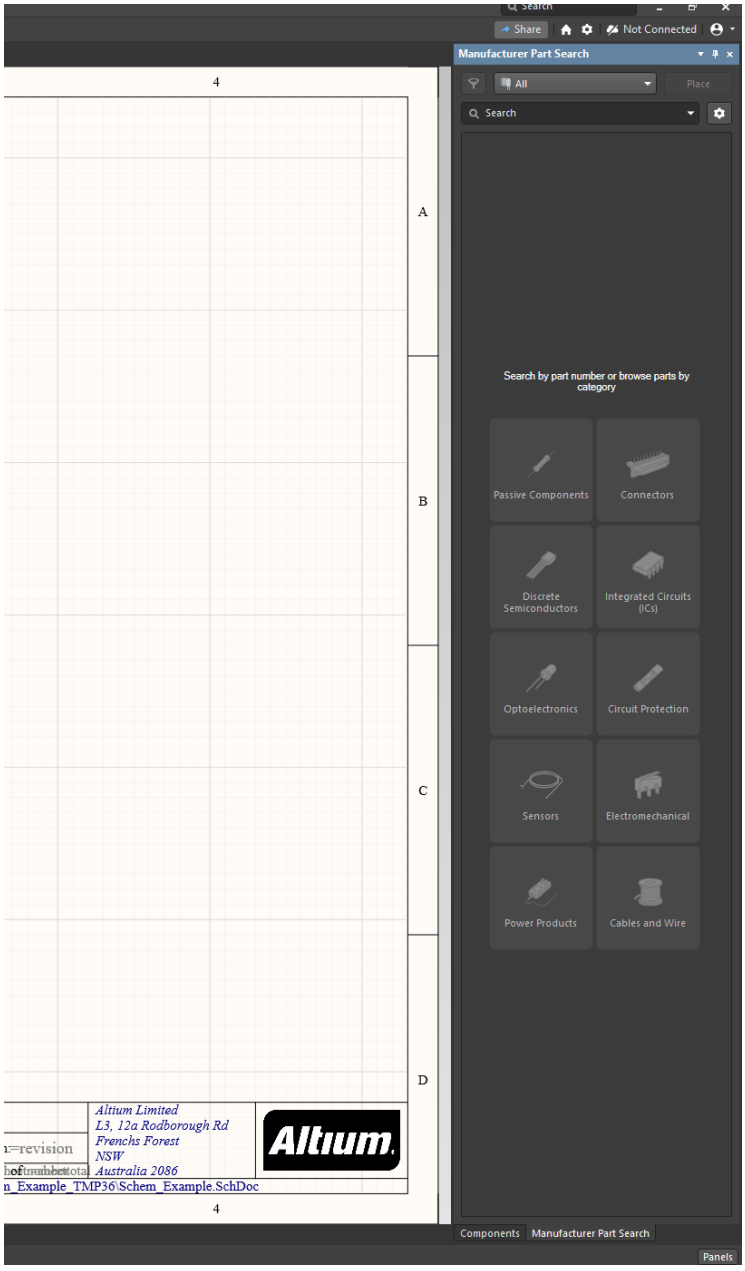
Place part by right clicking the schematic > place > part (or hit “p” key twice)



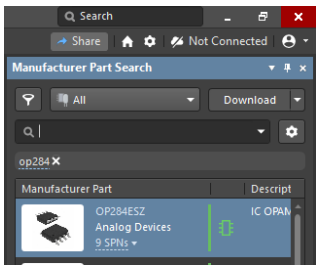
Place Part list: Choose or search for a part:



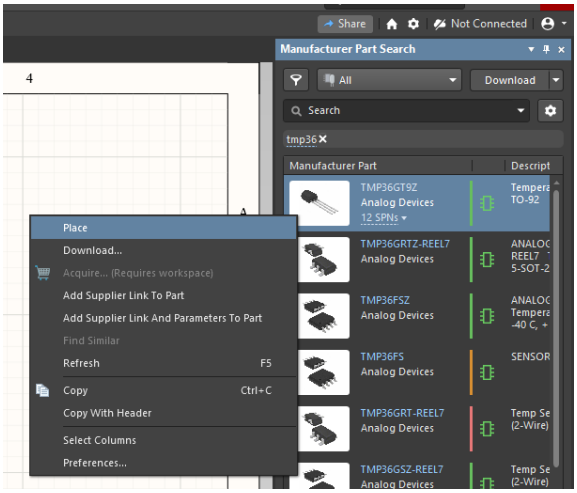
To open Manufacturer part search > click on “Panels” in the bottom right:



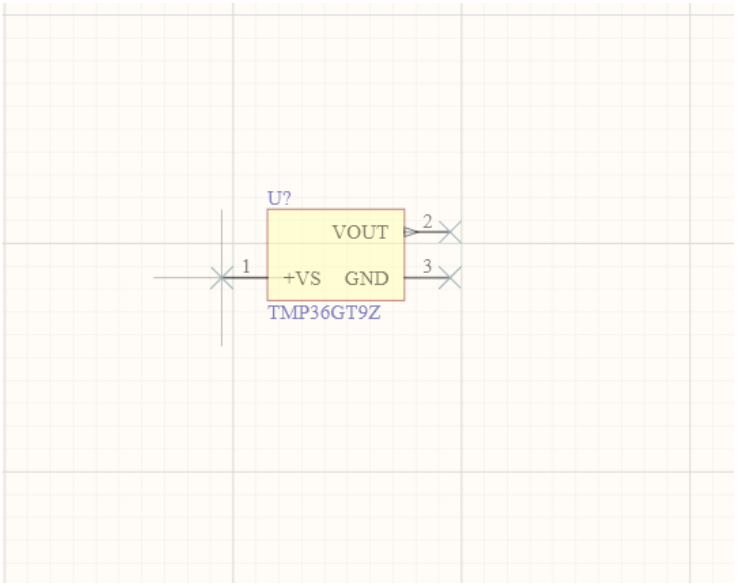
Search for a part:



Right click the part and hit “place”:

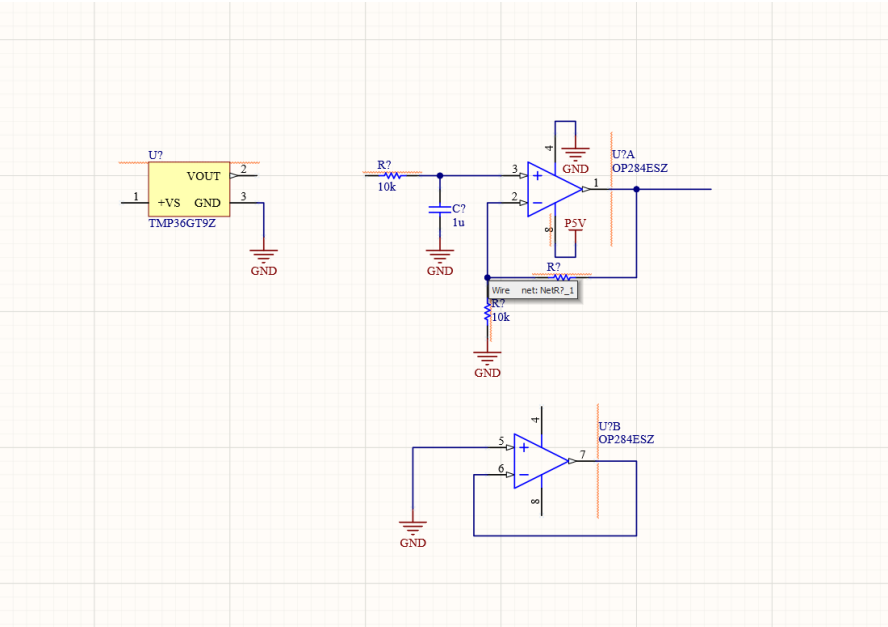


The part will now appear with your cursor in your schematic, click to place the part:

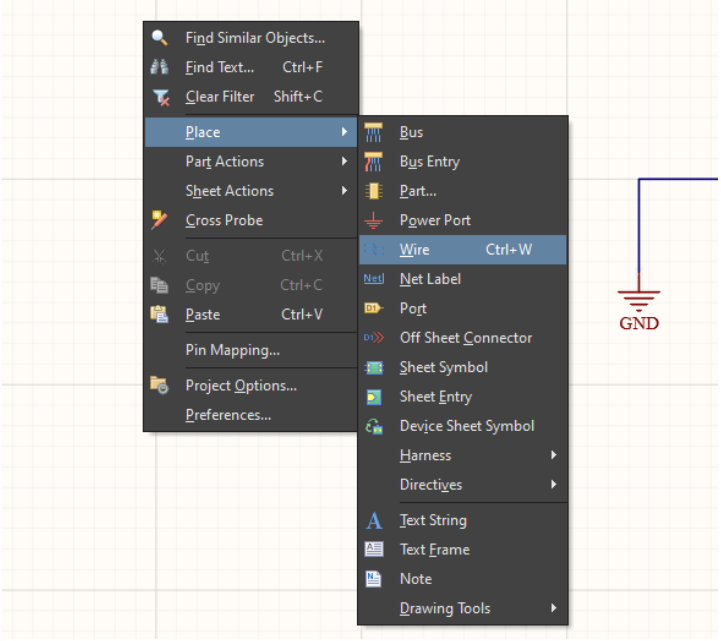


Note that the part is not named yet (U?) but we will deal with this later

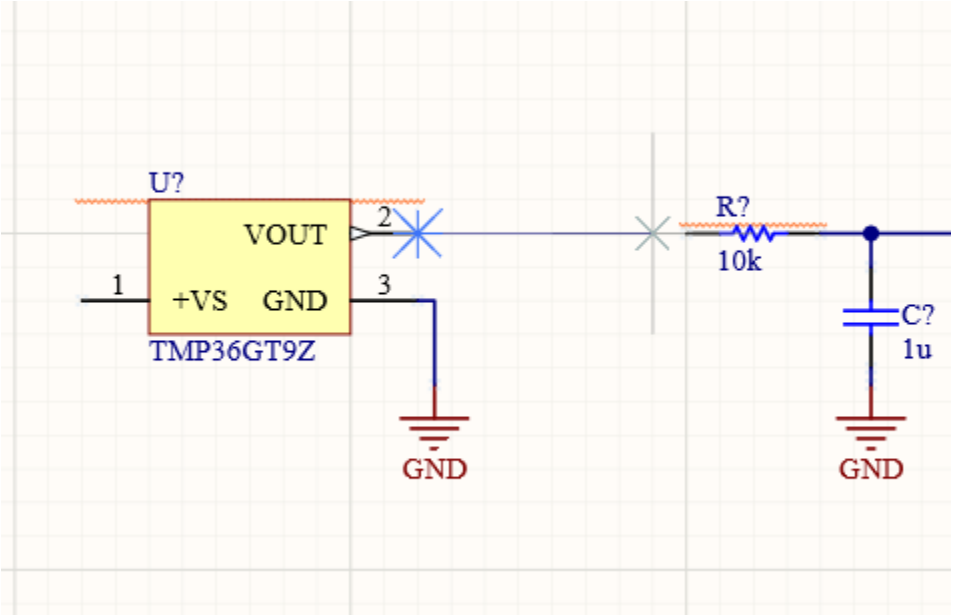
Place the other parts you will need:



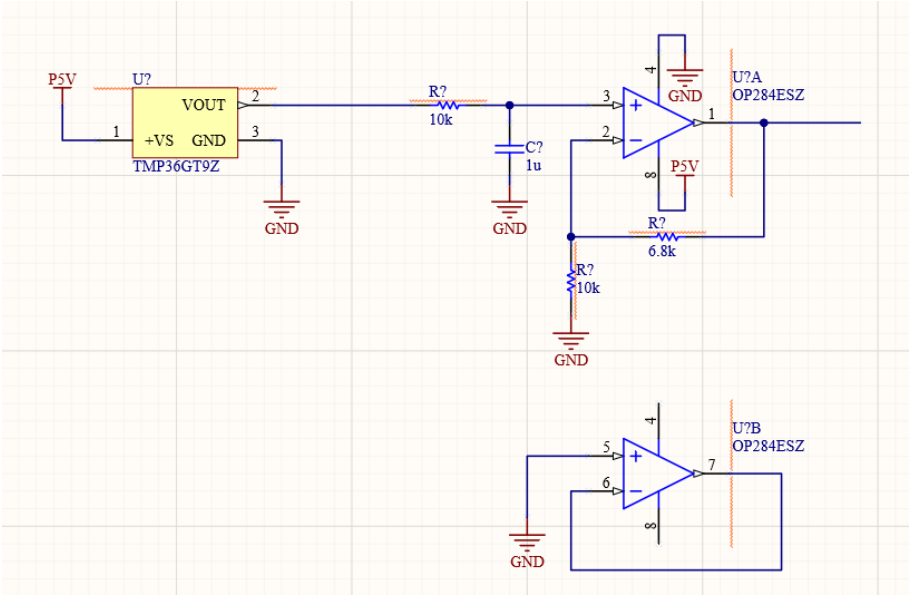
To place wire, right click > place > wire or hit CTRL + W:



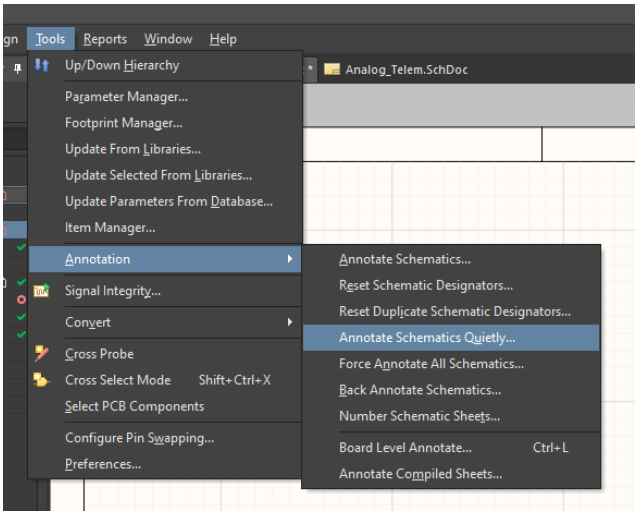
Placing the wire: Click once to "start" a wire" & then move the cursor and click again to "finish" the wire



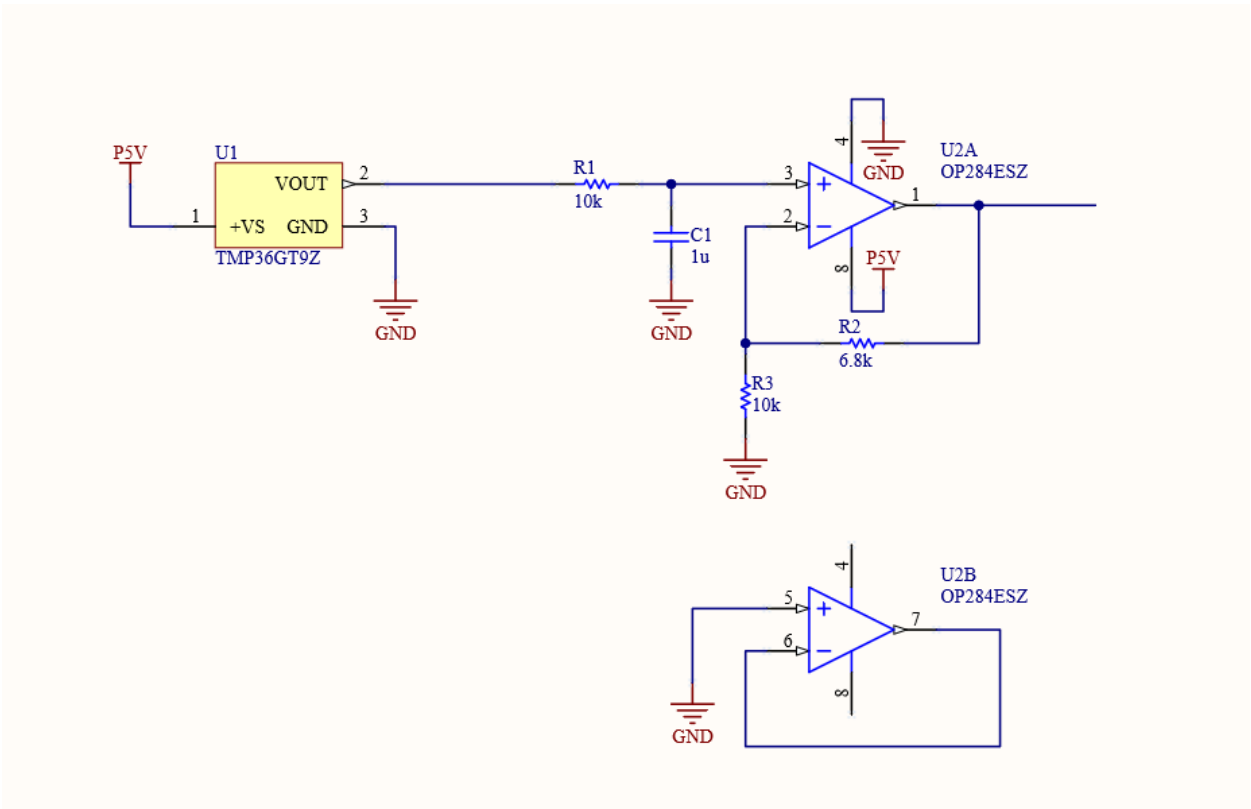
Finished Schematic:



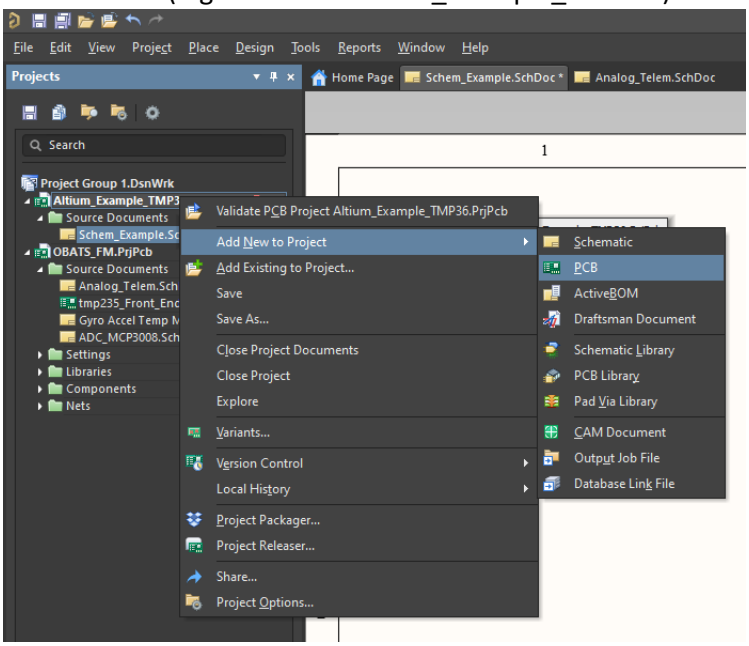
Naming parts on the schematic: (Tools > Annotation > Annotate Schematics Quietly)



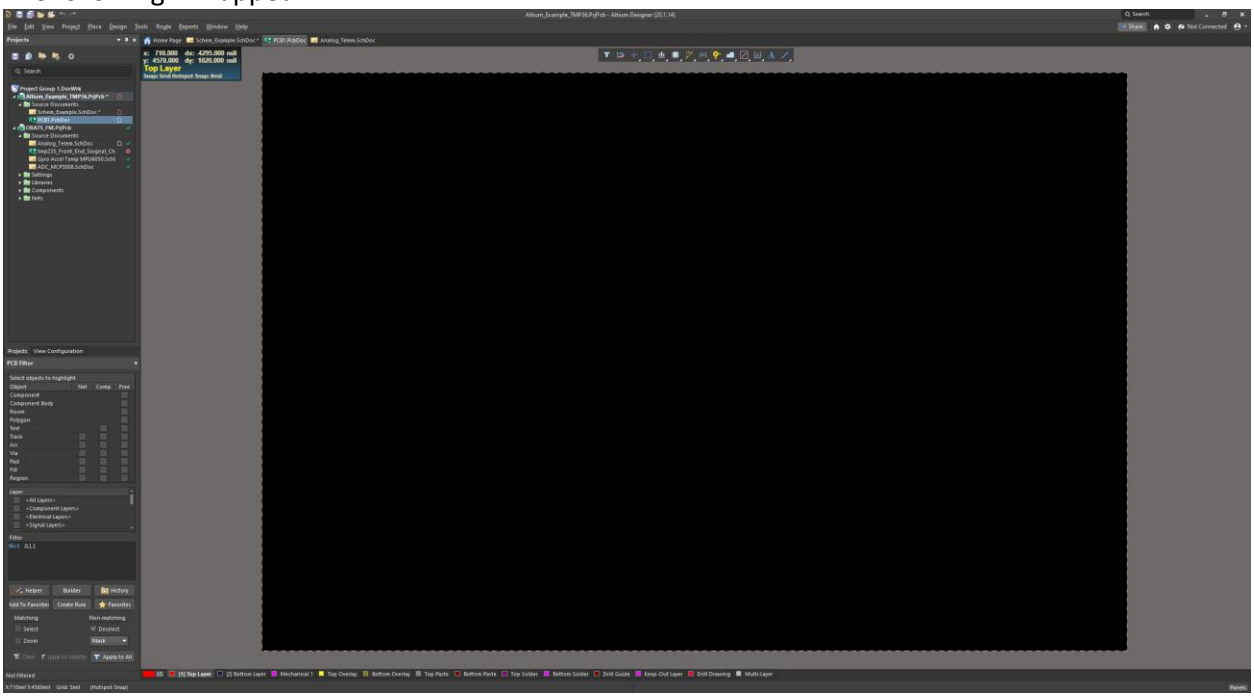
Complete Schematic:



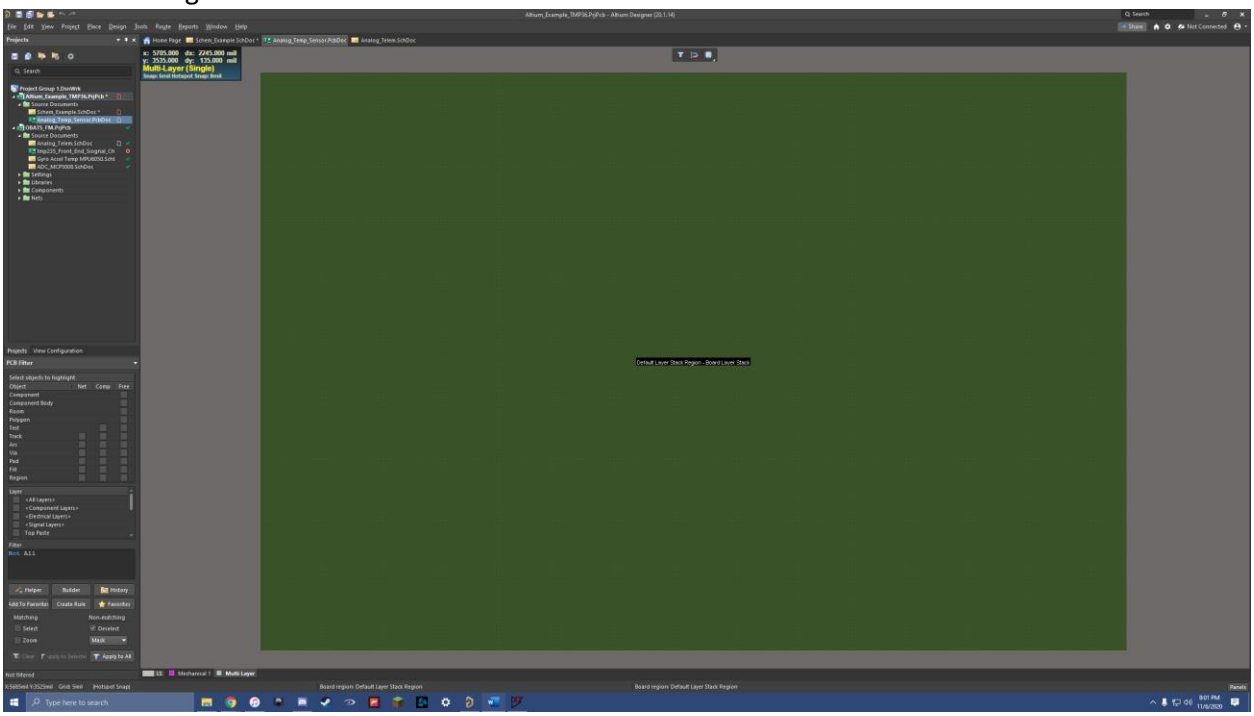
3. **Add PCB file:** (Right click on “Altium_Example_TMP36”)



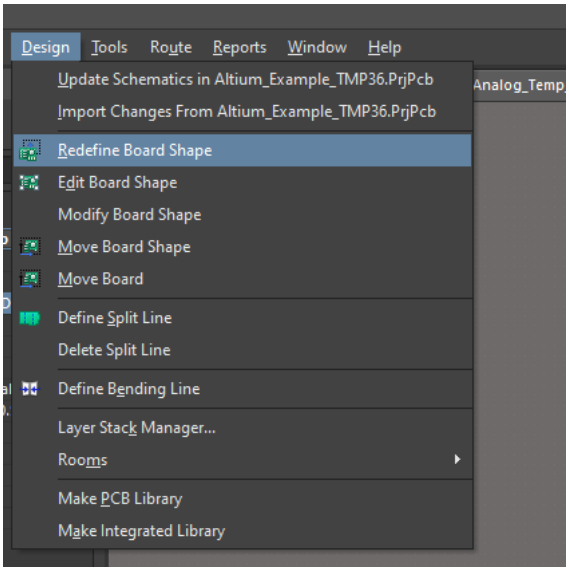
The following will appear:



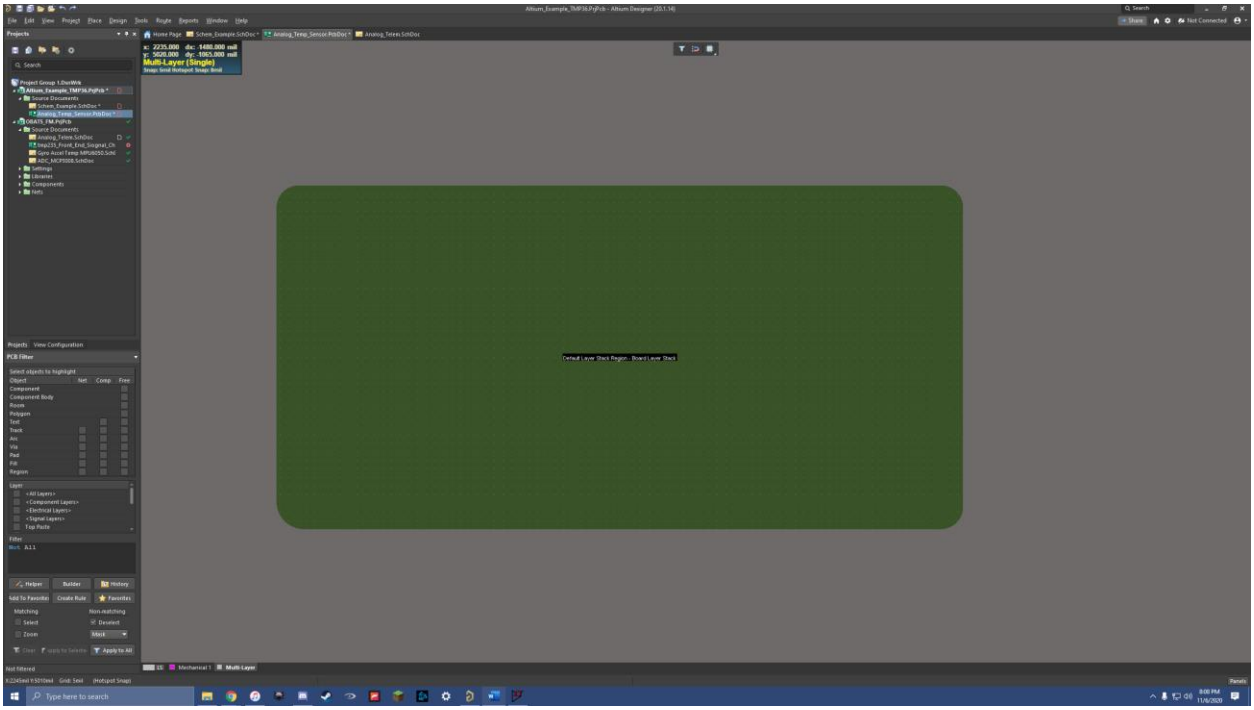
Press 1 to change view:



Hit Design > Redefine board shape

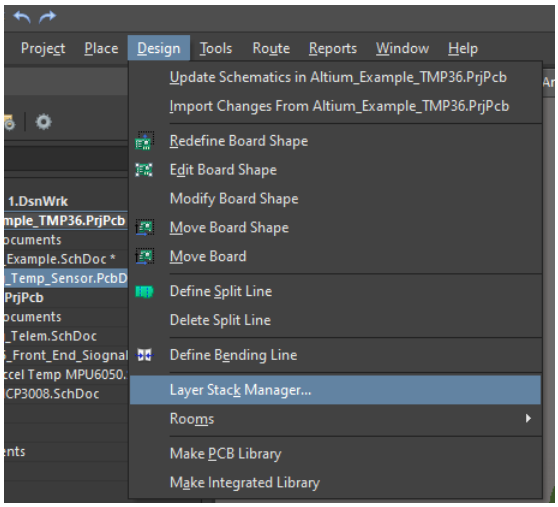


Finished Board:

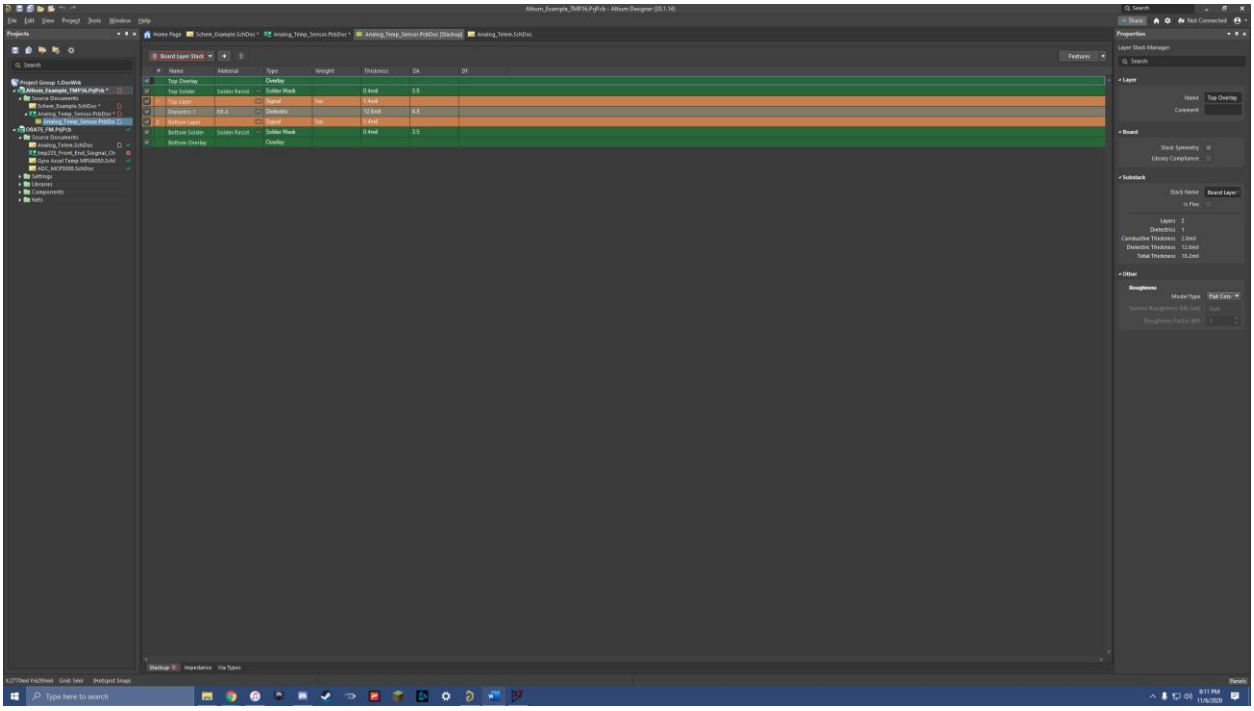


Add Layers to board: (we will do 2 layers for simplicity):

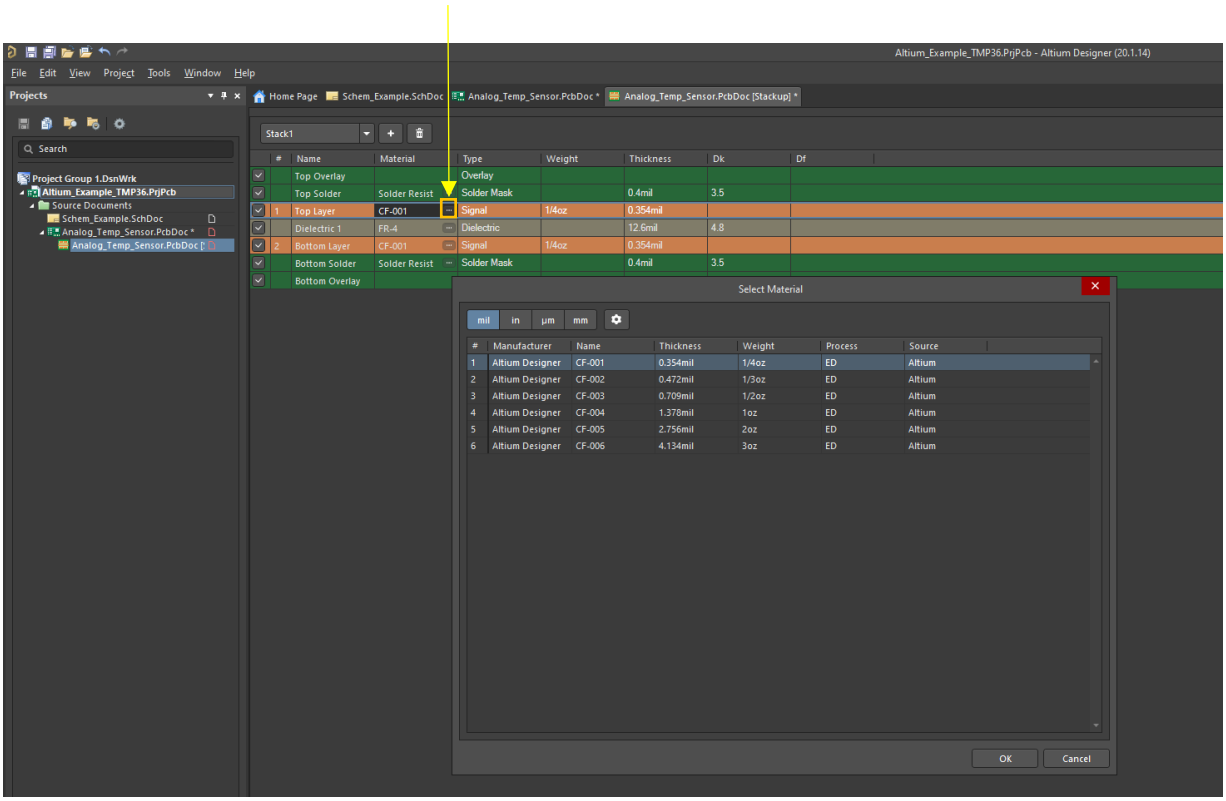
Hit Design > Layer Stack Manager:



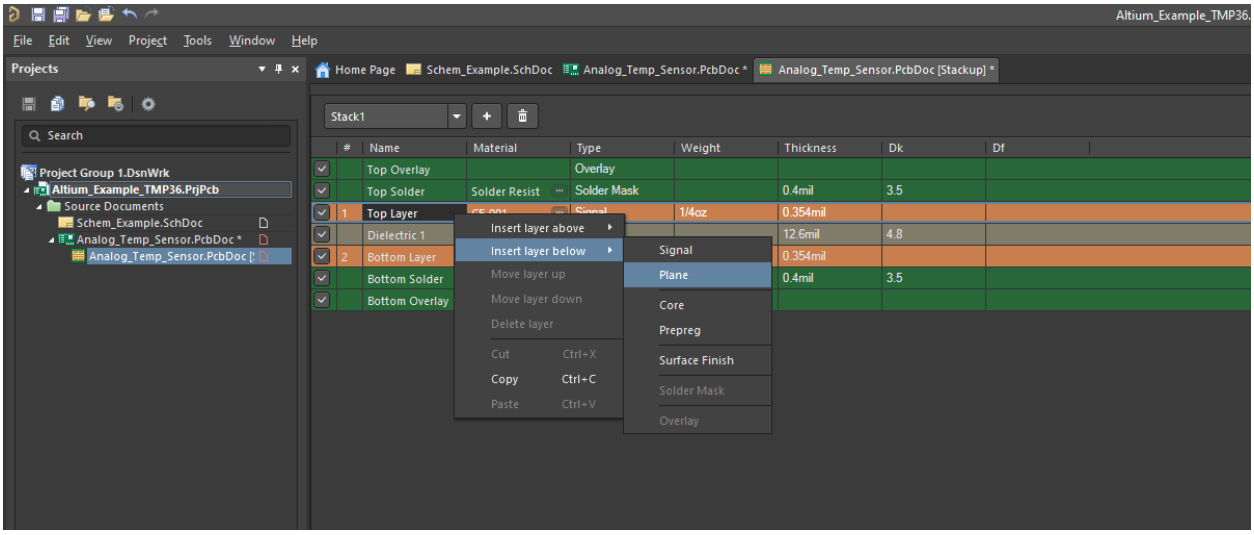
Following page will open:



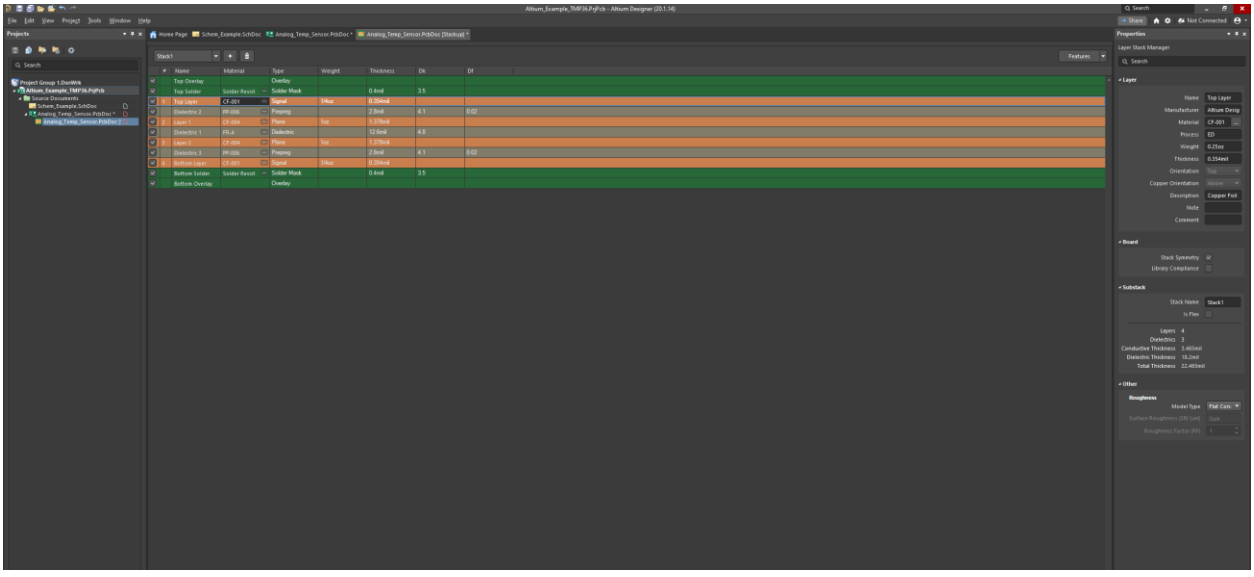
Select Material dimensions for insulators signal layers:



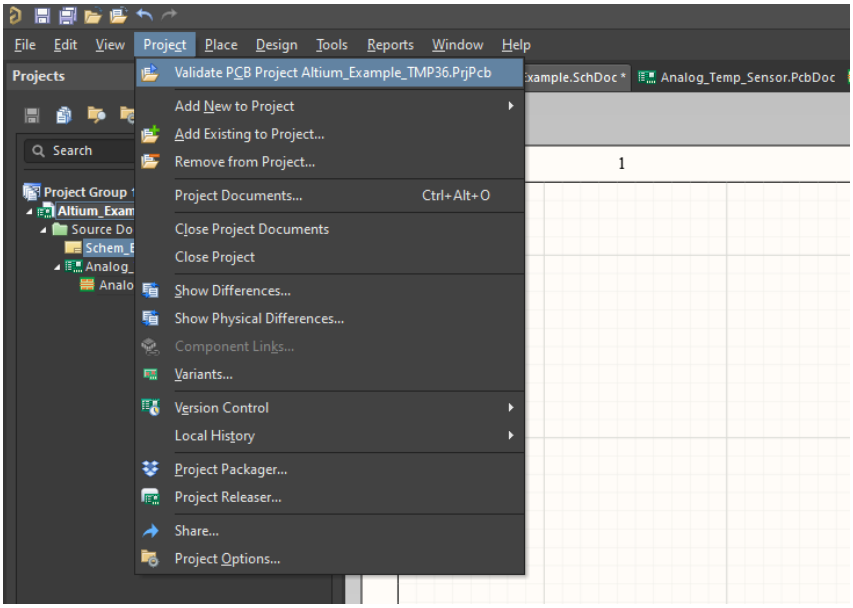
Add a plane layer: (Right click anywhere on layer “1”)



New Layer Stack:

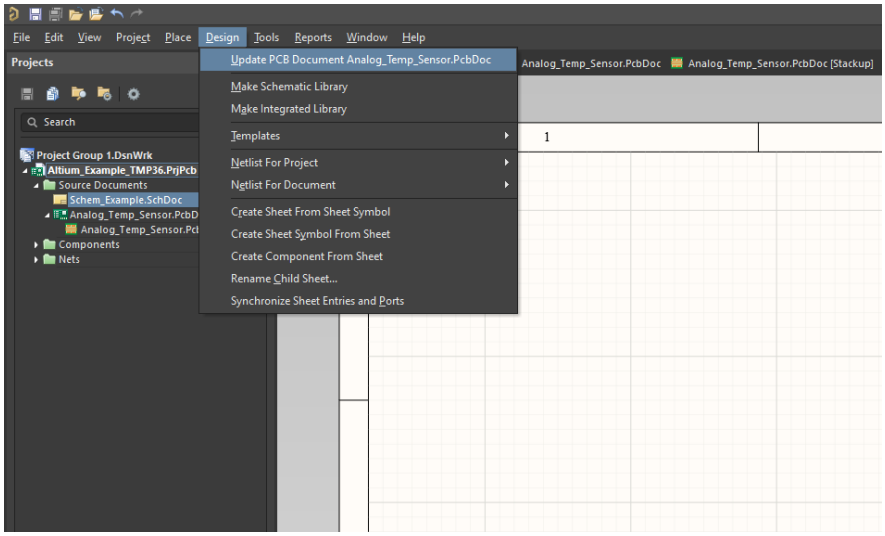


4. **Run (Validate) DRC on Schematic** (Design Rule Check):

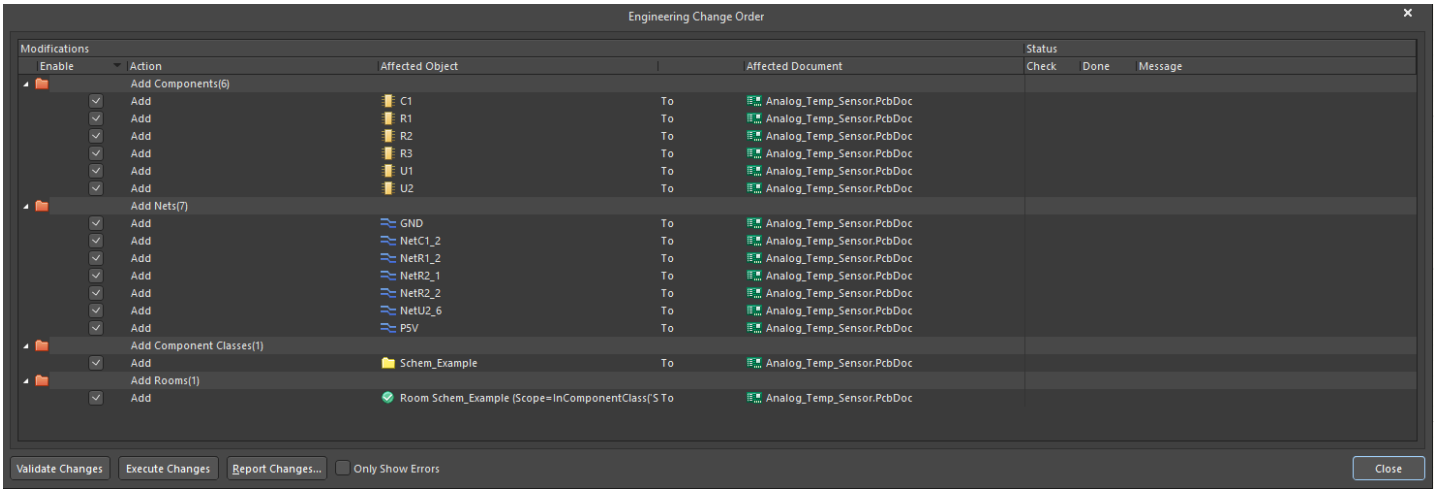


If there is nothing wrong with schematic, nothing will happen

5. **Update PCB Document with Schematic components:**



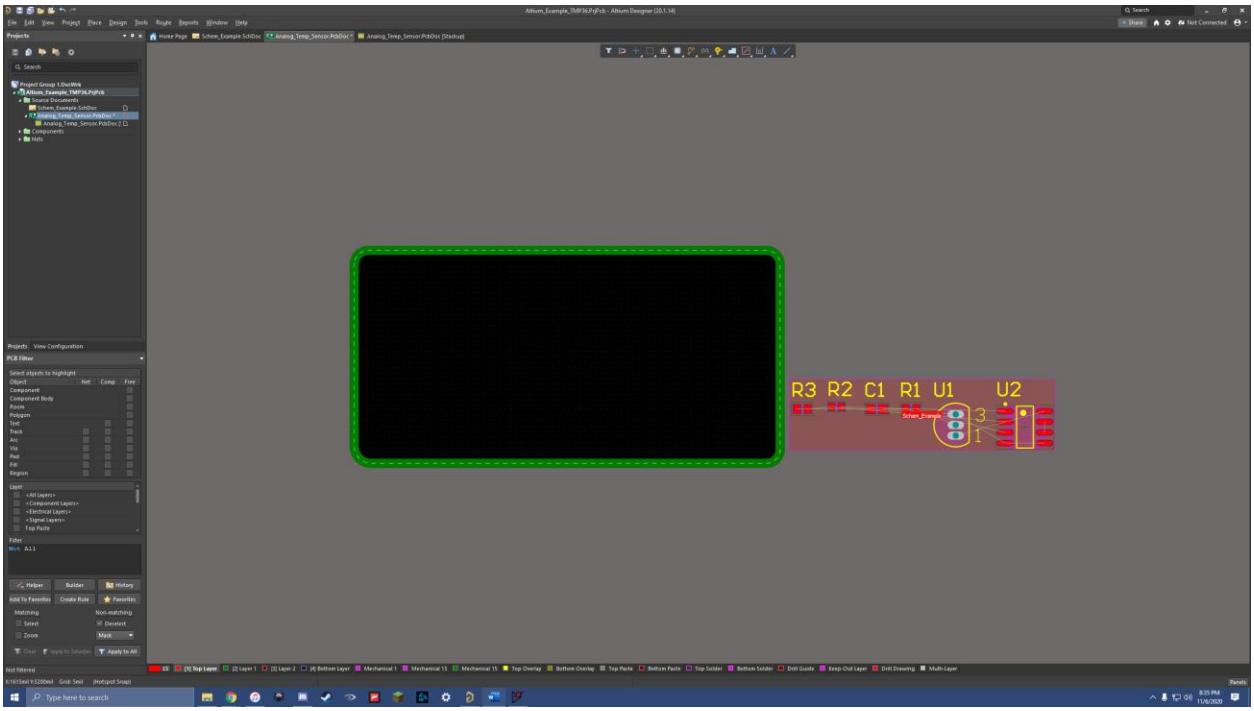
Validate changes before moving to PCB file:



Hit “Validate Changes” and then “Execute Changes”

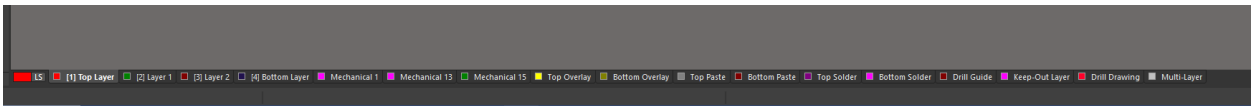
This should open the PCB document with the schematic components

Hit the “2” key to switch to 2D mode:



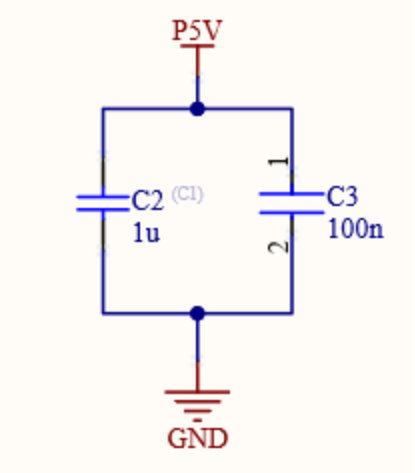
Before we start placing:

The bottom of the screen can be used to select layers of the board:



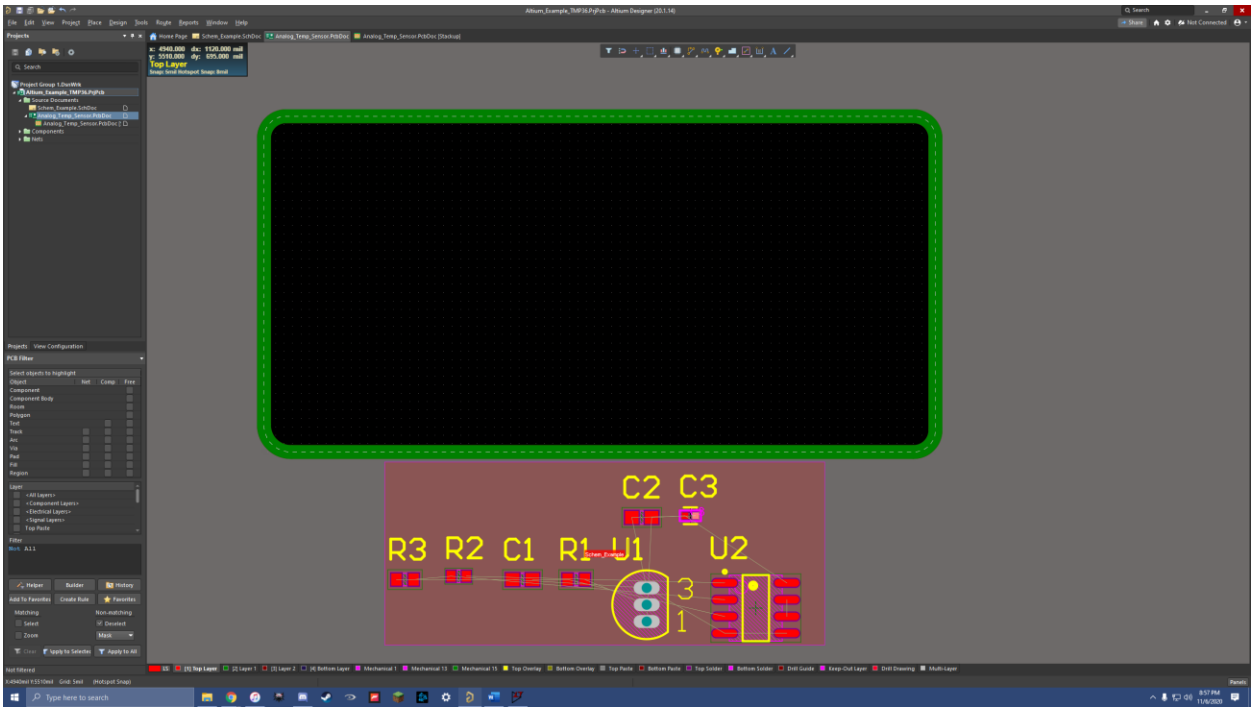
***While making this portion of the guide, I realized that I forgot to connect power and GND to capacitors and a solder pad

Schematic Parts Added:

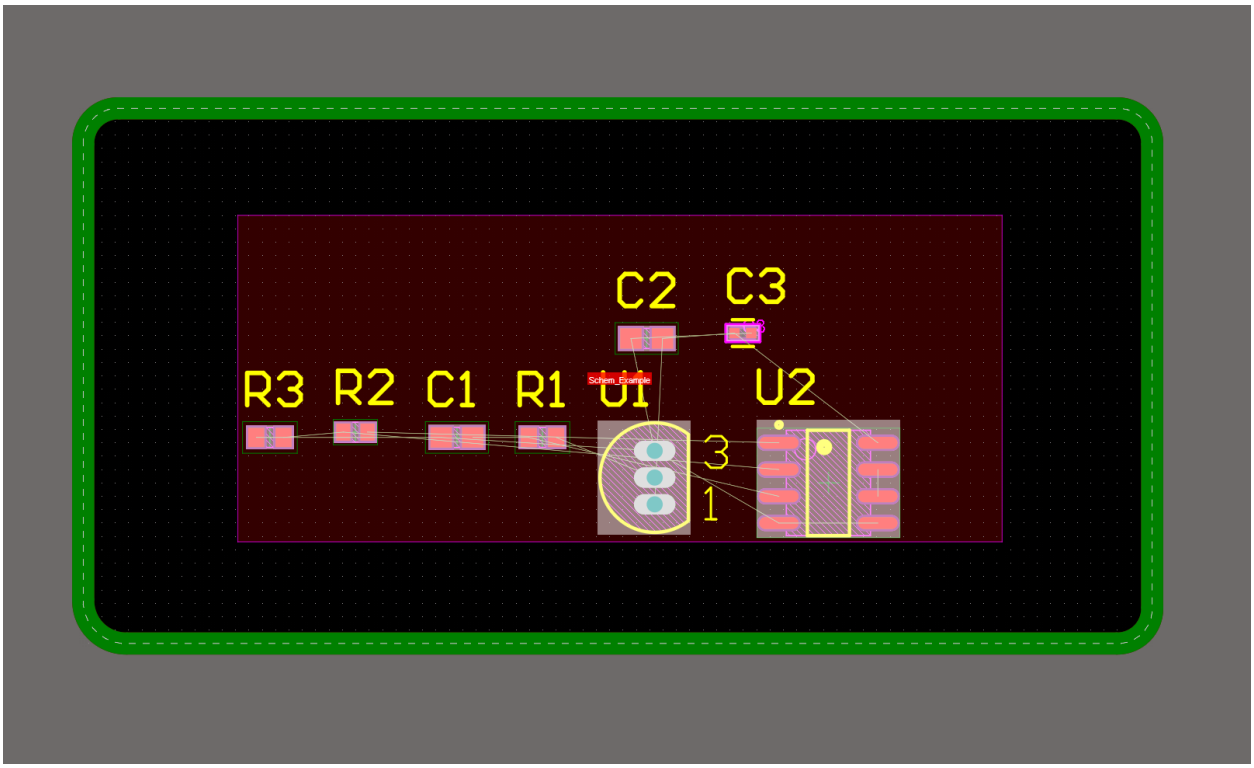


***Make sure to update changes to PCB after editing schematic file

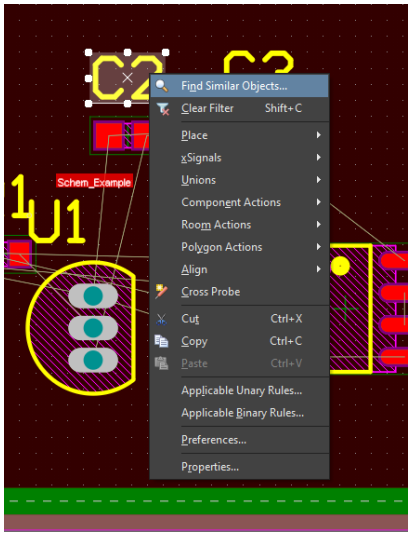
6. Place Parts Onto PCB



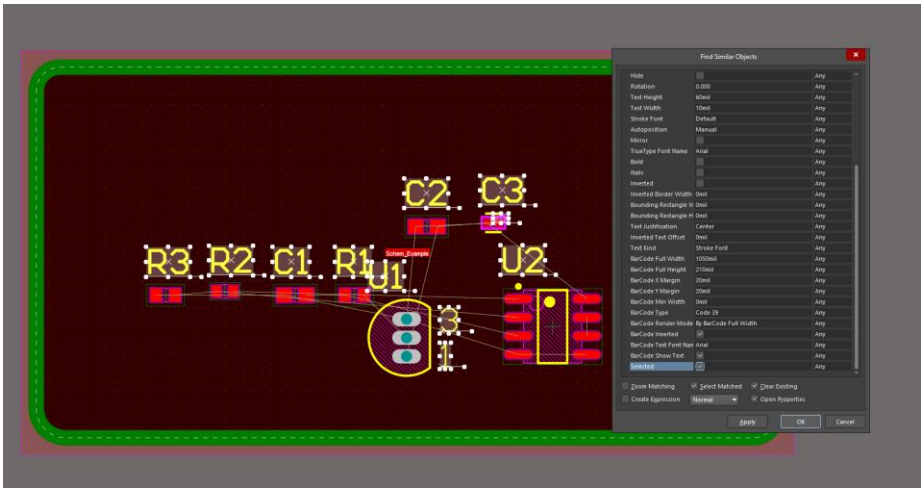
Move Keep out layer along with parts onto board:



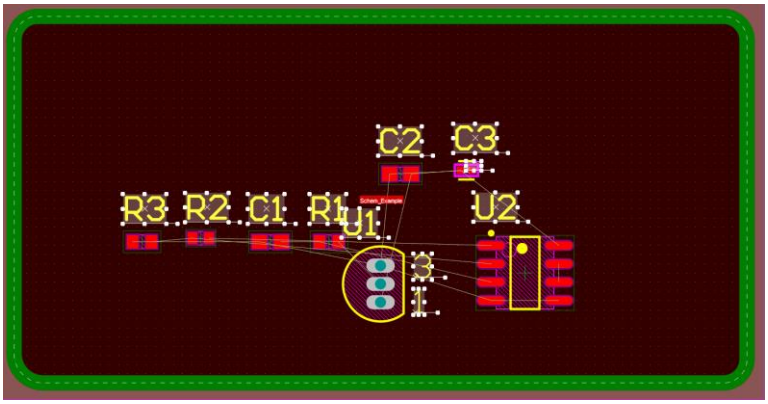
Before moving parts, lets make these giant designators smaller:



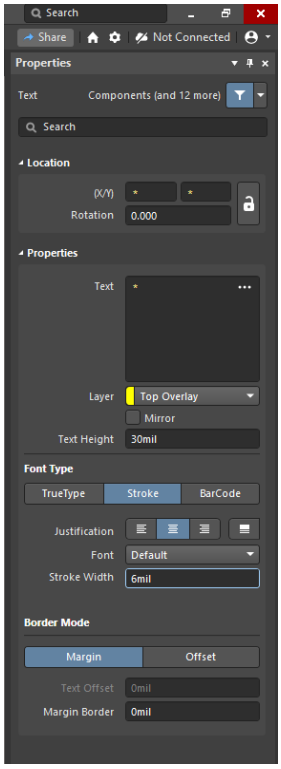
Hit “okay”



Now all designators are selected:



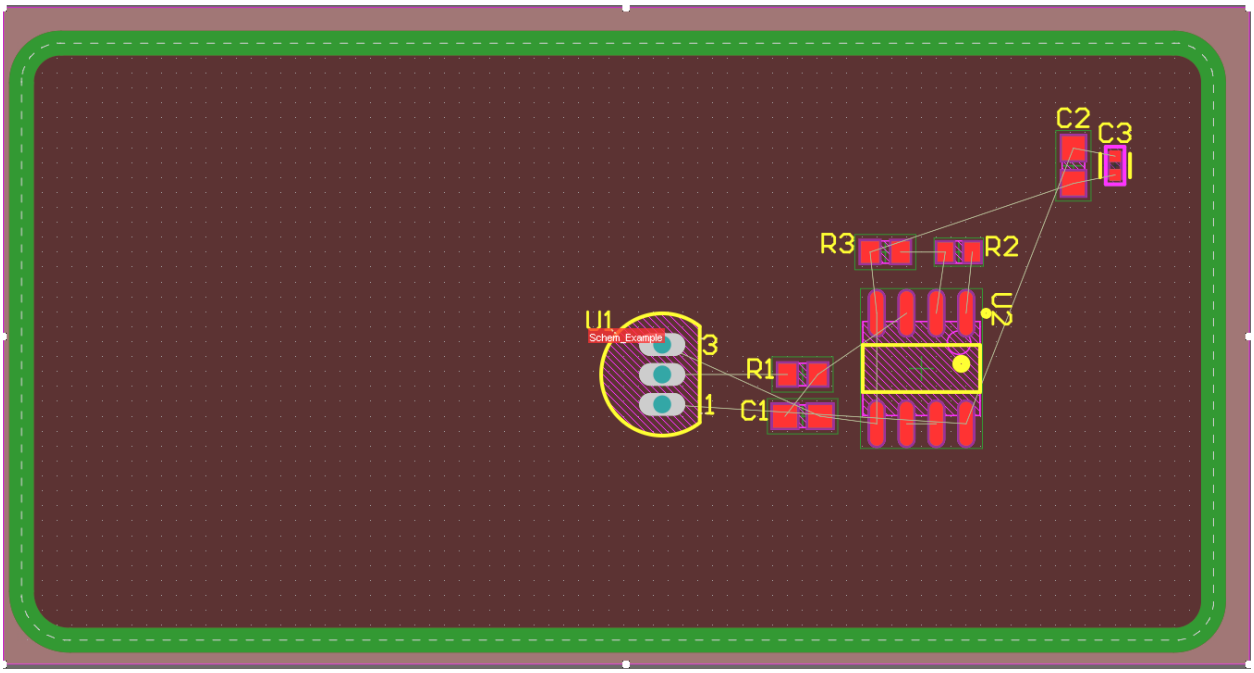
Look towards the right side of the screen, change “Text Height” & “Stroke Width”:



(I chose 30mil height and 6 mil width)

Now Designators are an appropriate size

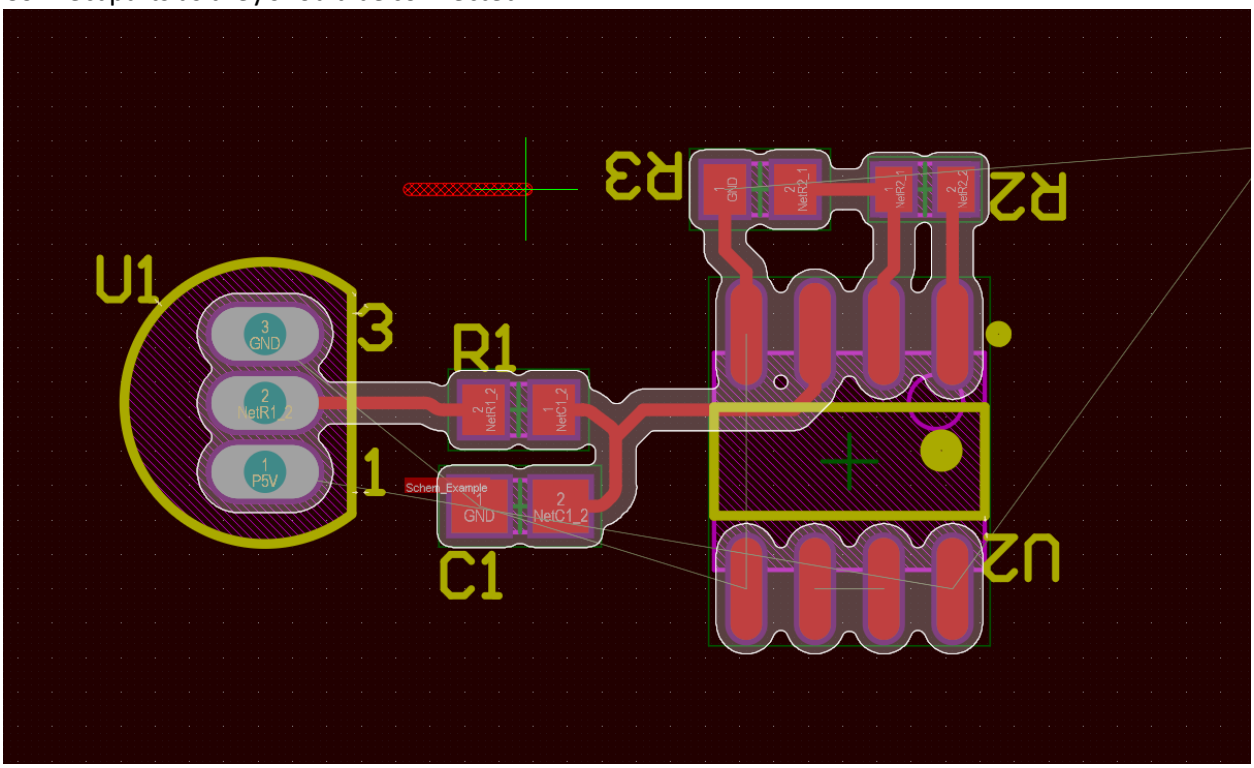
Arrange Parts onto PCB that allows for connections (disregard power pins for now):



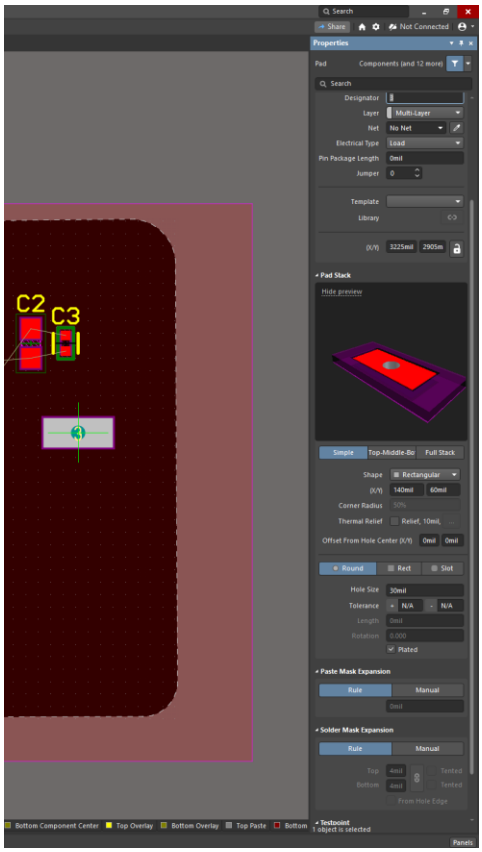
Note that lines appear to show you “net” connections

Place Tracks using “p” and then “t” keys:

Connect parts as they should be connected:

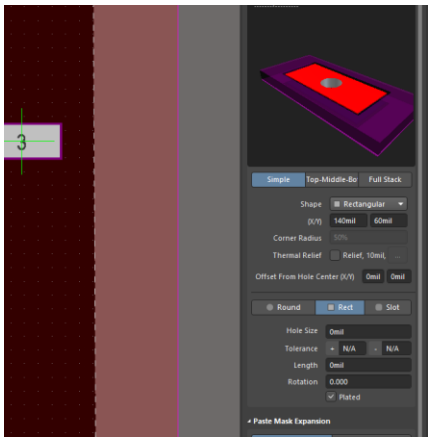


Add solder pads: hit “p” twice, and then hit TAB key:

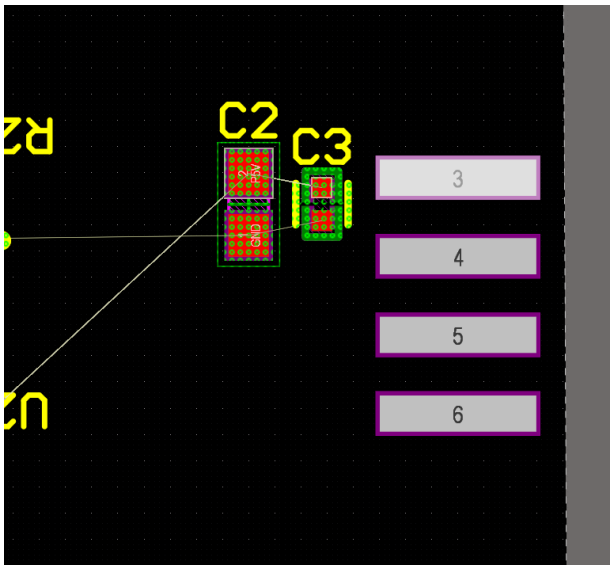


A solder pad will appear, adjust the Shape and then X/Y to make a rectangular like shape (this pad will be solder to a wire)

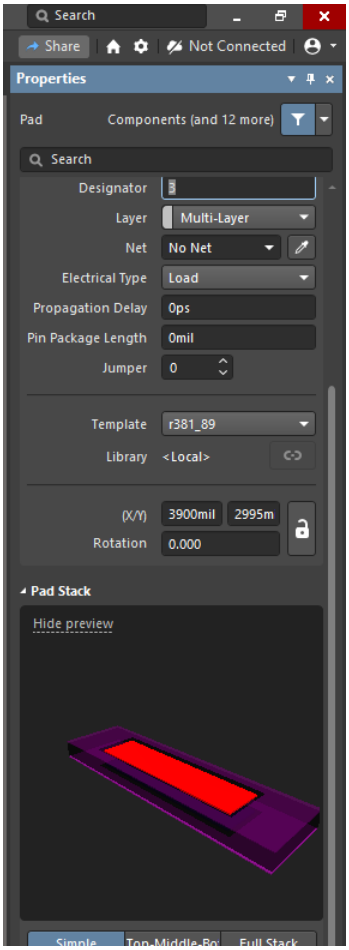
Then, Change hole size of pad to zero:



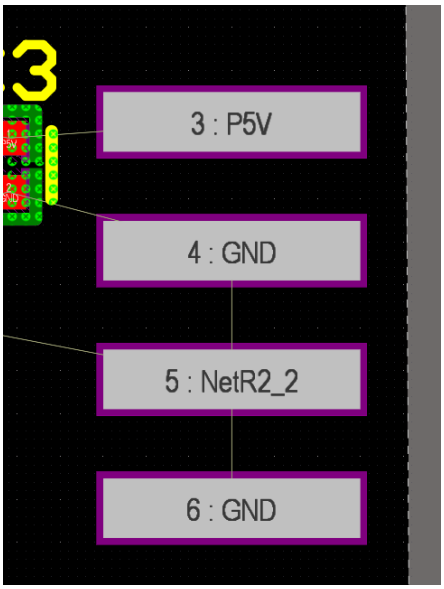
Place pads:



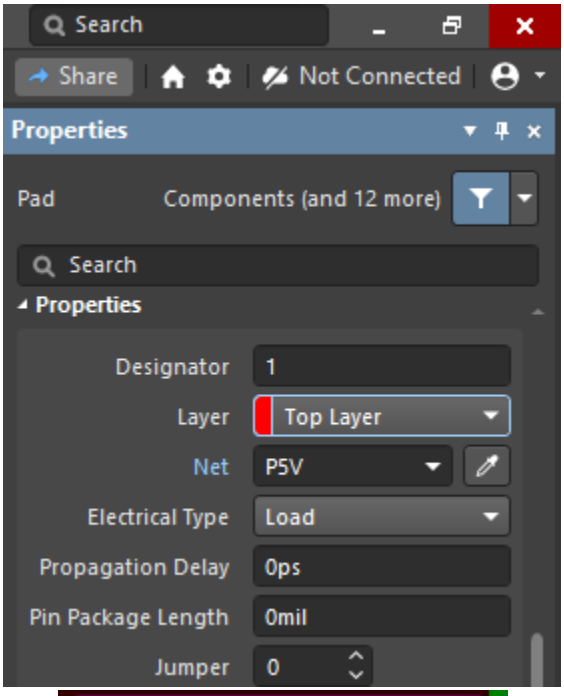
Assign nets to solder pads:



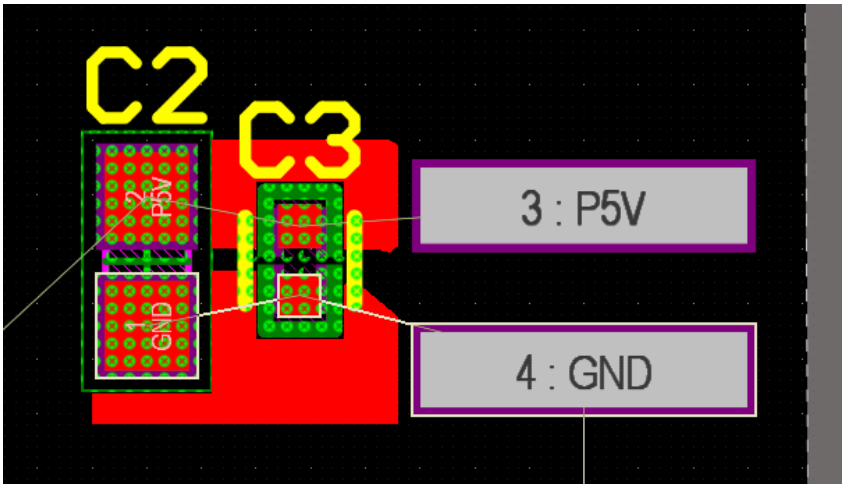
Netted Pads:



Make pads single layer:



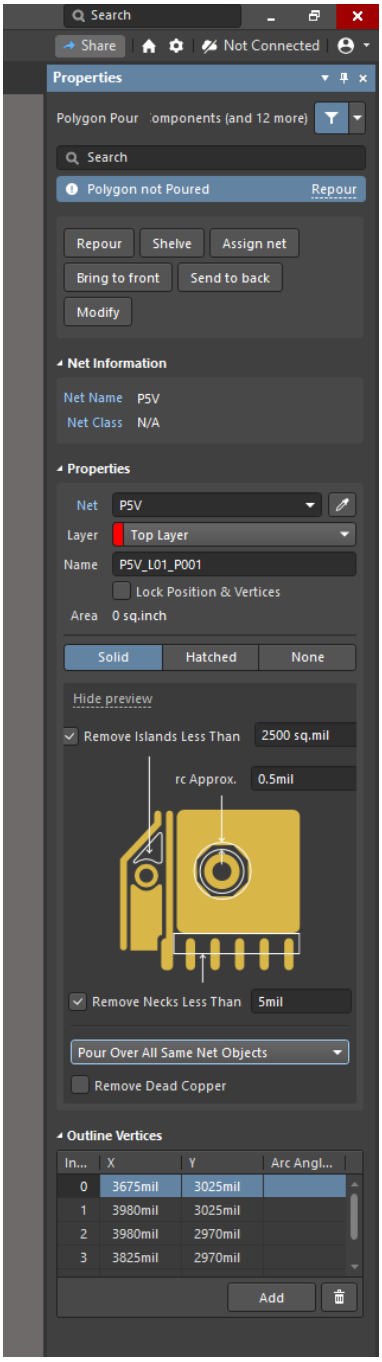
Polygon Pours type “p” and then “g” and then drag over objects: (SHIFT + SPACE to change curve)



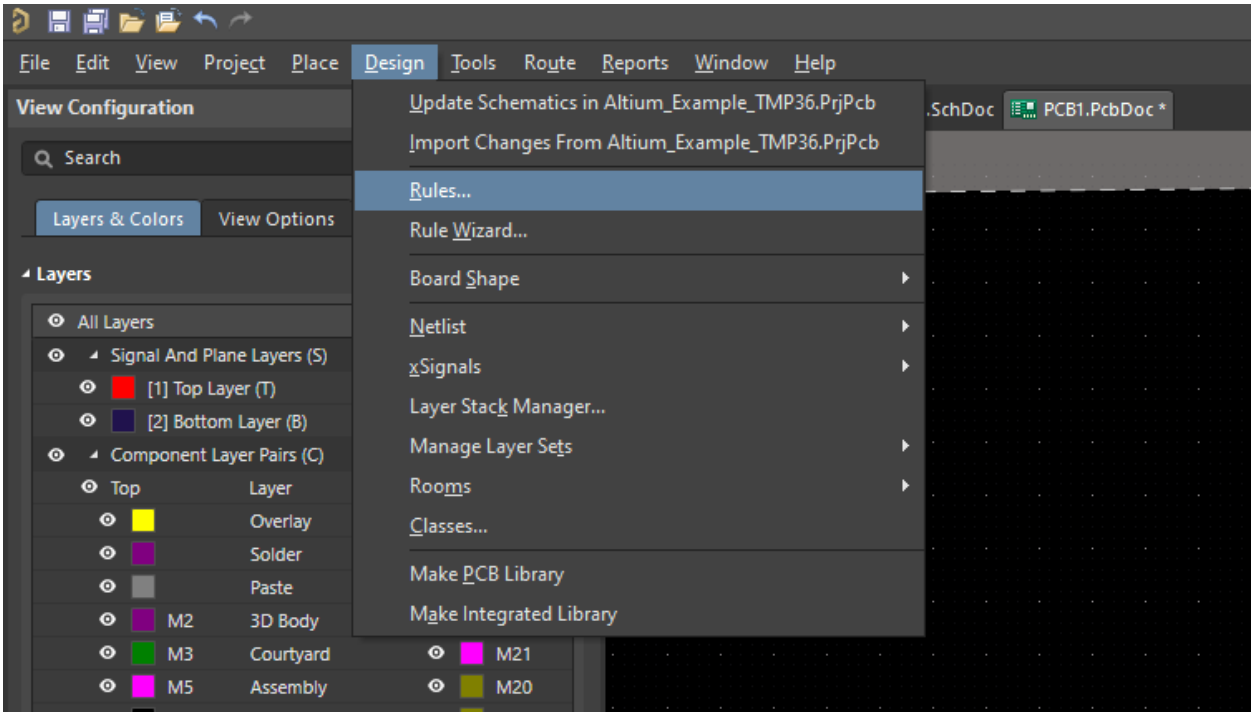
Assign poly pour nets to pads and then repour all polygon (hit “t” “g” “a”)

If pours come out weird:

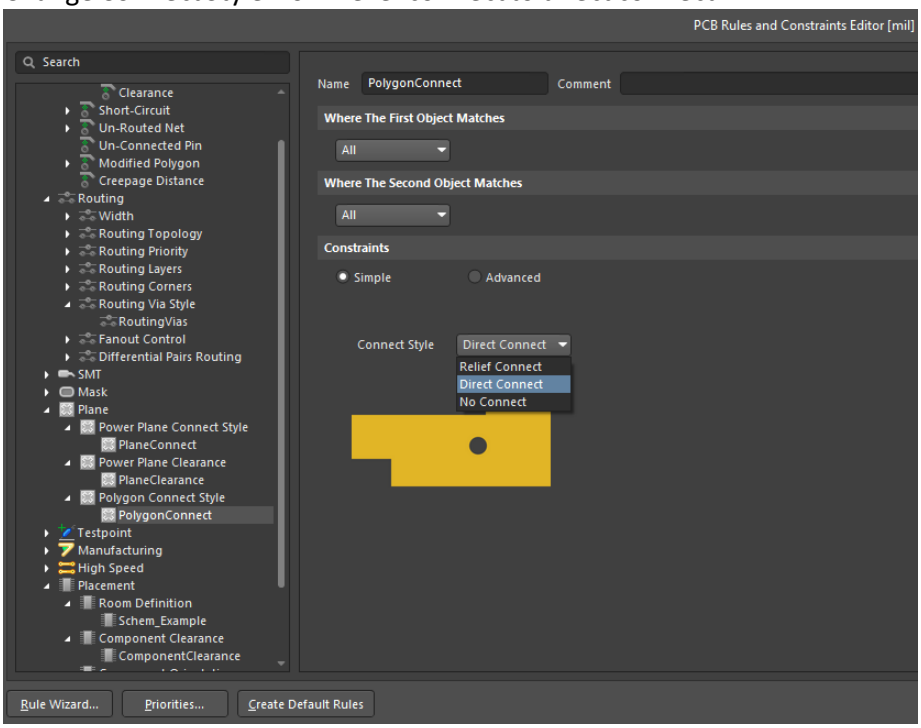
Change pour settings to “Pour Over All Same Net Objects”



If still weird, perform the following:

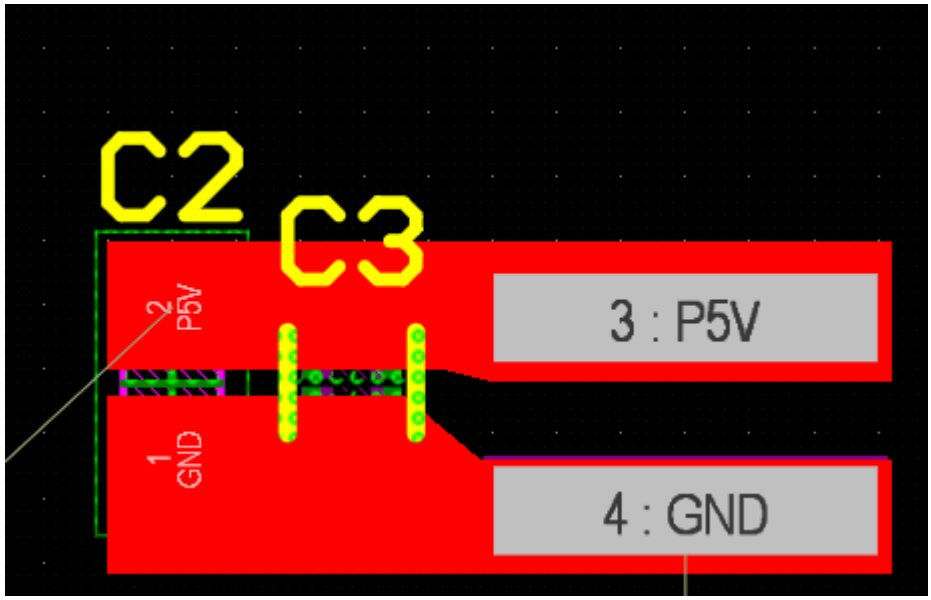


- Plane > Polygon Connect
  - Change Connect Style from Relief connect to direct connect:



Hit Apply and then Okay

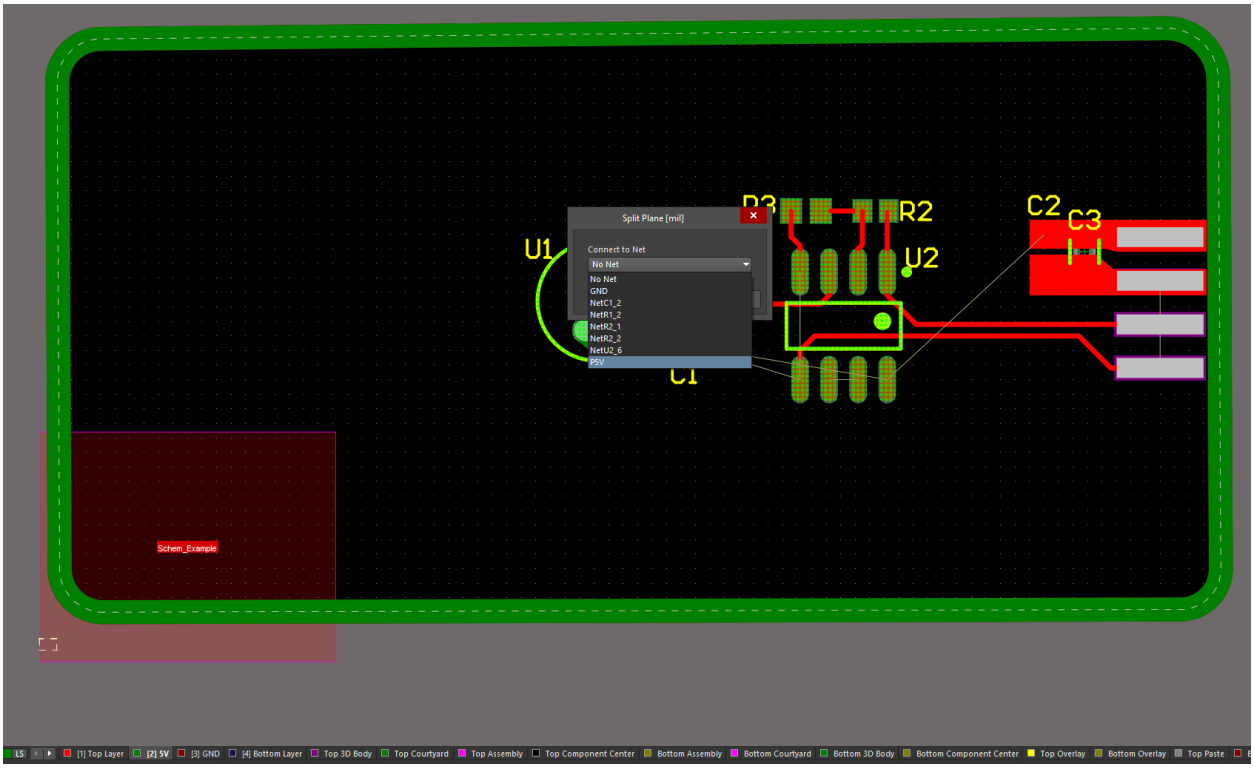
Repour using “t” “g” “a”:



Now all tracks and resistors are placed (Time for Vias!!!!)

Before Vias, we must net layers of the board (we are connecting power to layers, 5V & GND)

Select the layer in the bottom that you wish to net, right click the board (anywhere with empty black space), hit Properties, and then choose the net you want:



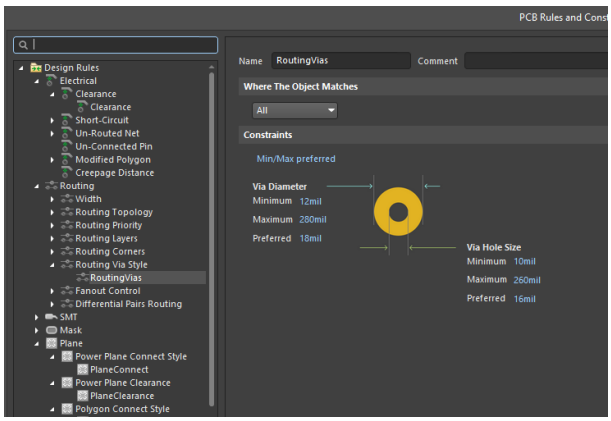
Repeat for any other layers

OSHPARK Via Requirements:

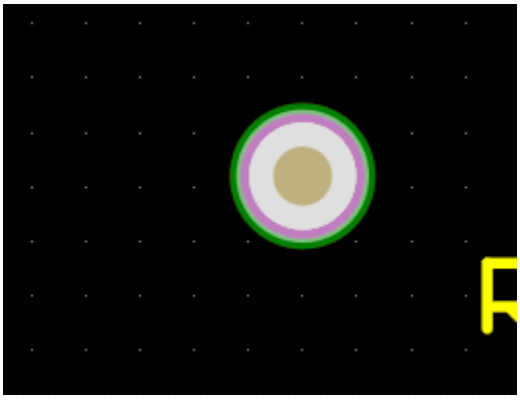
4 Layer Services

Spec Type		Note
Minimum Hole size	10 mil (0.254mm)	Holes belows this size will be rounded up
Maximum Drilled Hole Size	260 mil (6.604mm)	Holes exceeding this size will be milled
Annular Ring	4 mil (0.1016mm)	
Via Plating Thickness	1 mil (0.0254mm)	
Fabricated Hole Size Tolerance	+/-2.5mil max (0.0635mm)	+/-1 mil typical (0.0254mm)
Fabricated Hole Position Tolerance	+/-2.5mil max (0.0635mm)	+/-1 mil typical (0.0254mm)

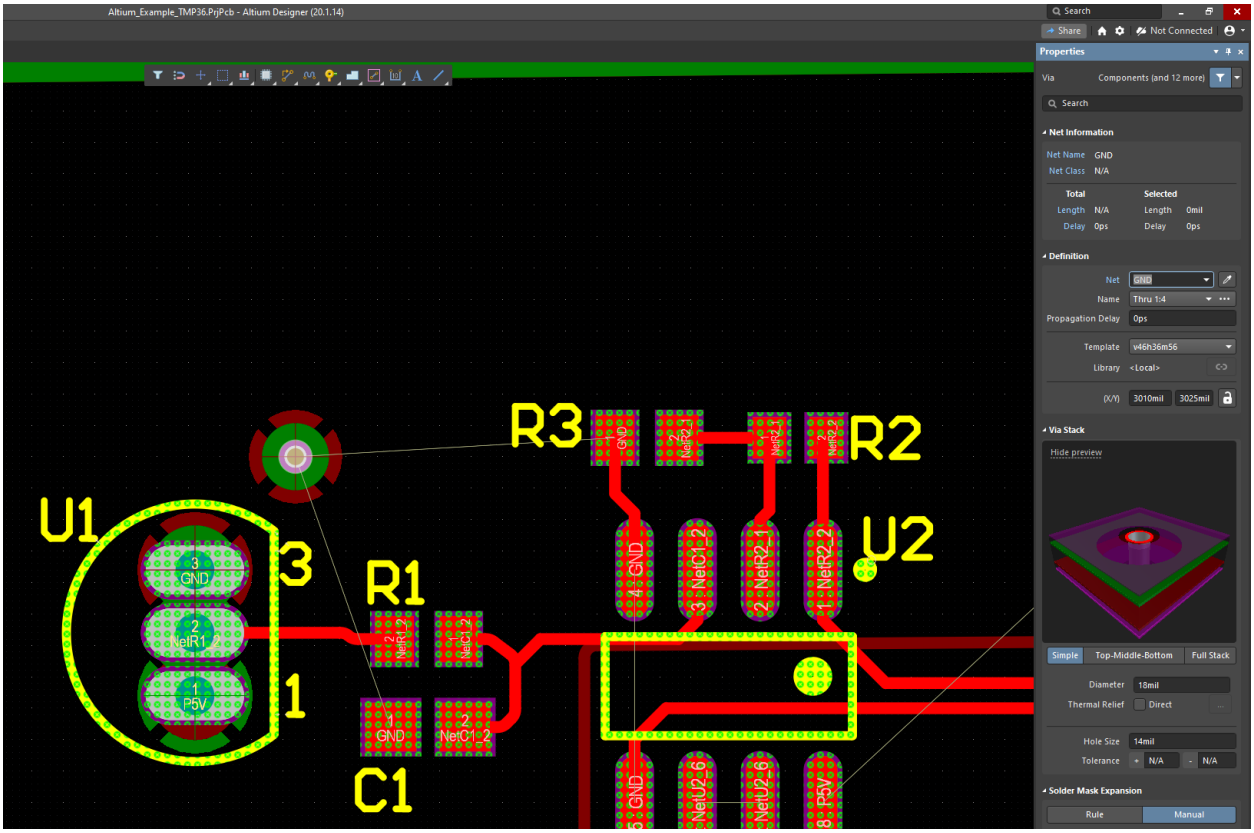
Settings in Altium (Design > Rules > Routing Via Style > Routing Vias: Adjust Settings:



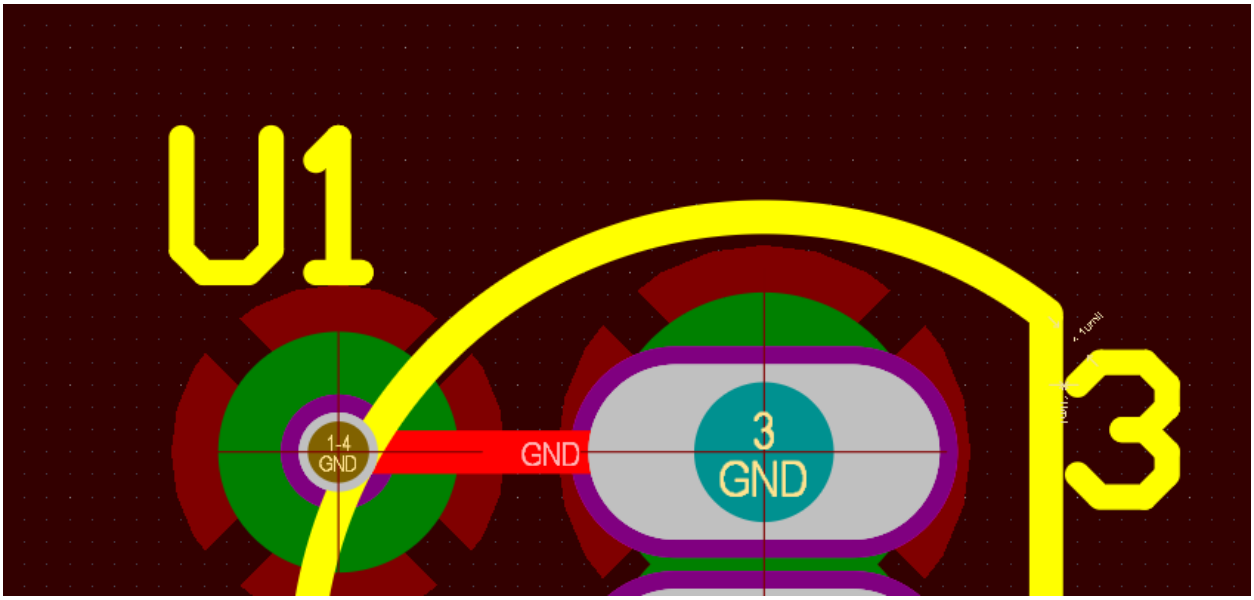
Placing Vias: Hit “p” “v” and then click:



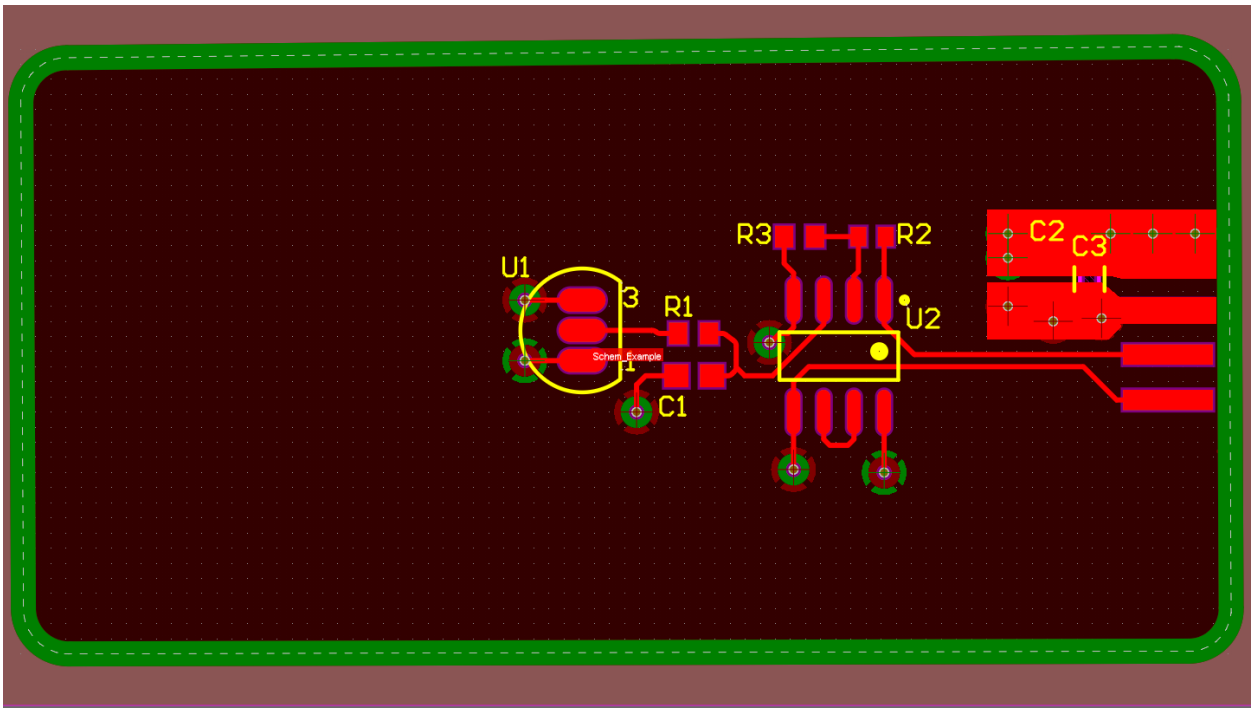
Assign net to Via:



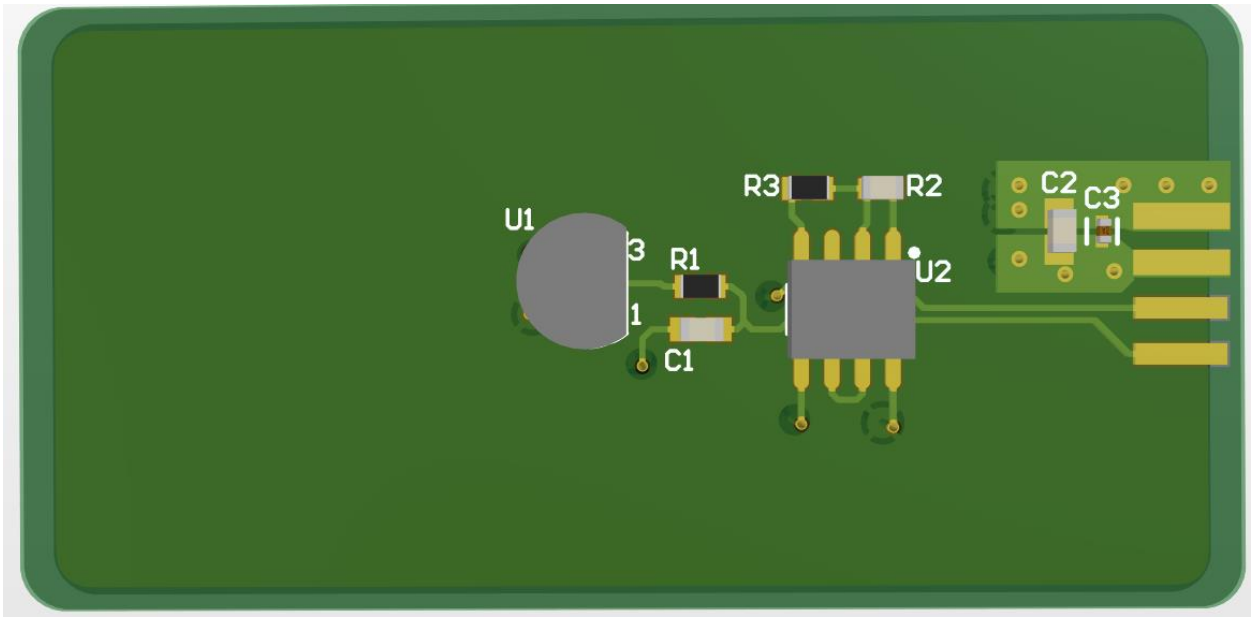
Connect to via using track:

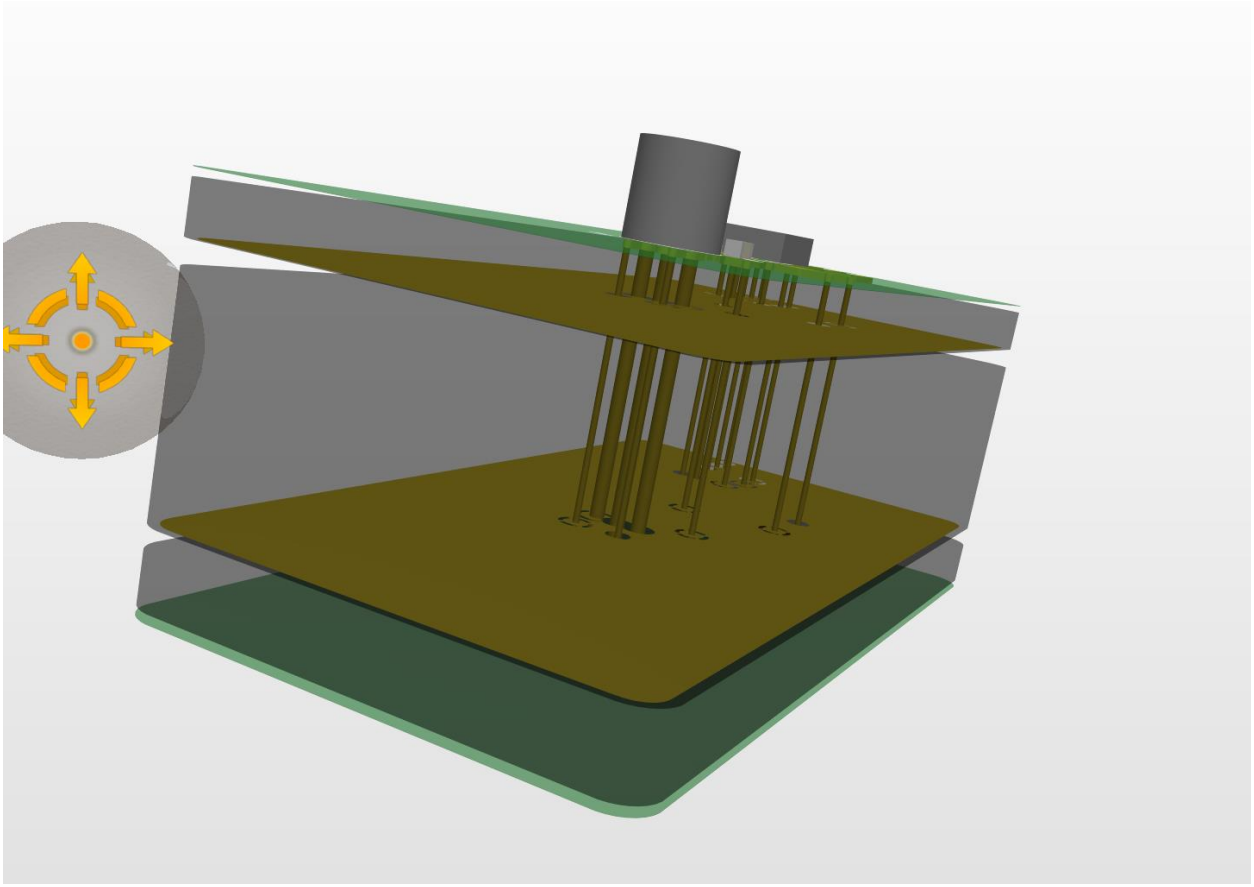


Place and connect all Vias:

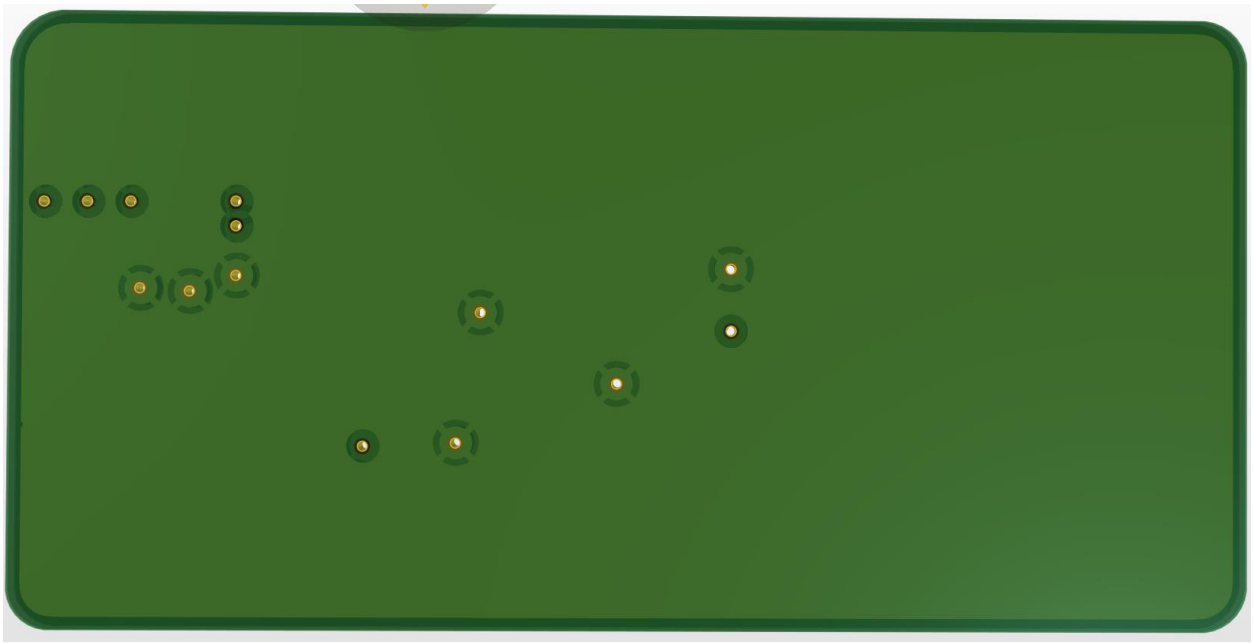


Board is Complete:

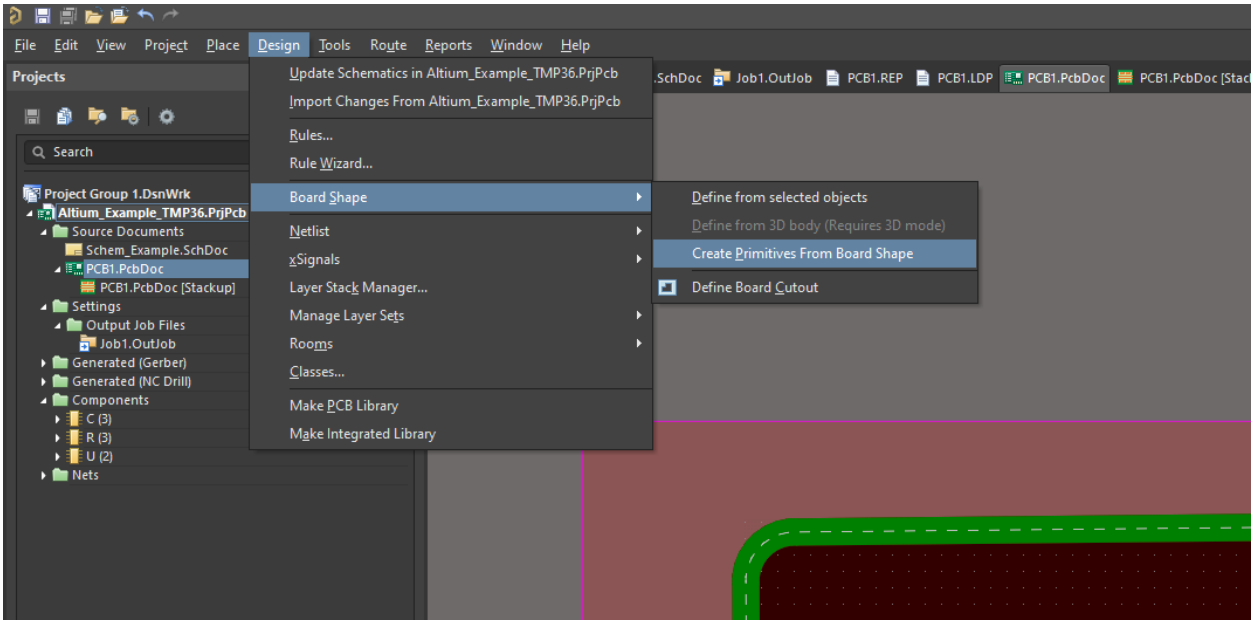




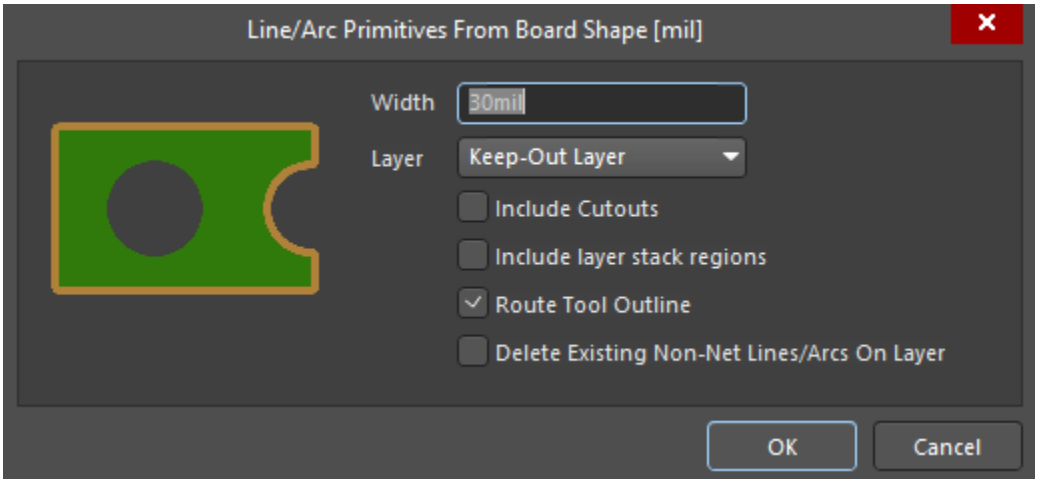
Bottom view:



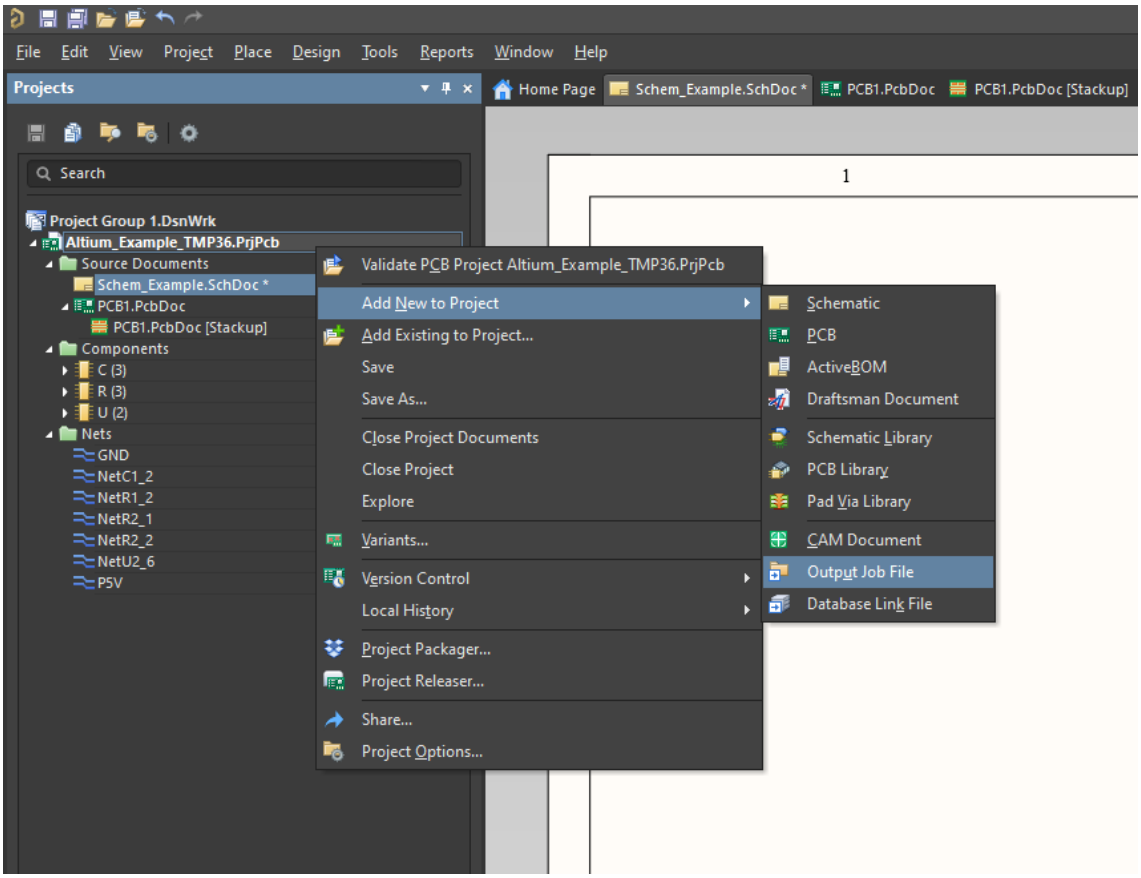
DEFINE BOARD SHAPE:

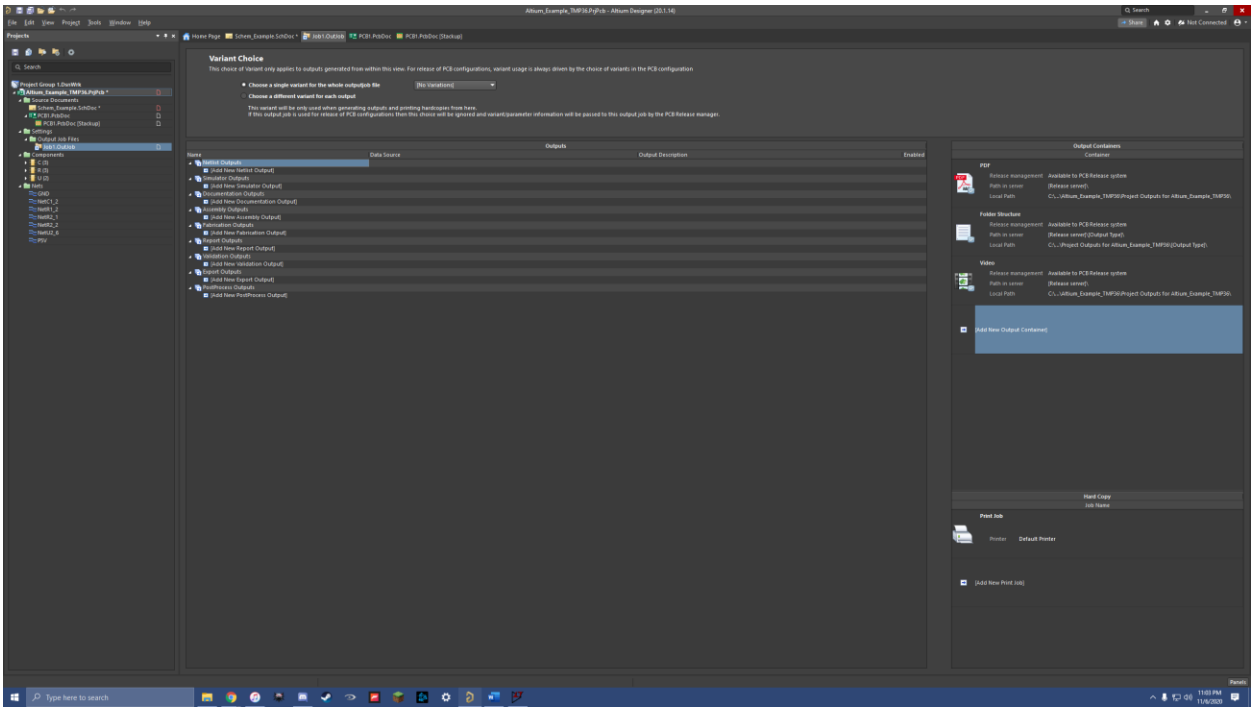


KEEP EXACT SETTINGS AS THE FOLLOWING:

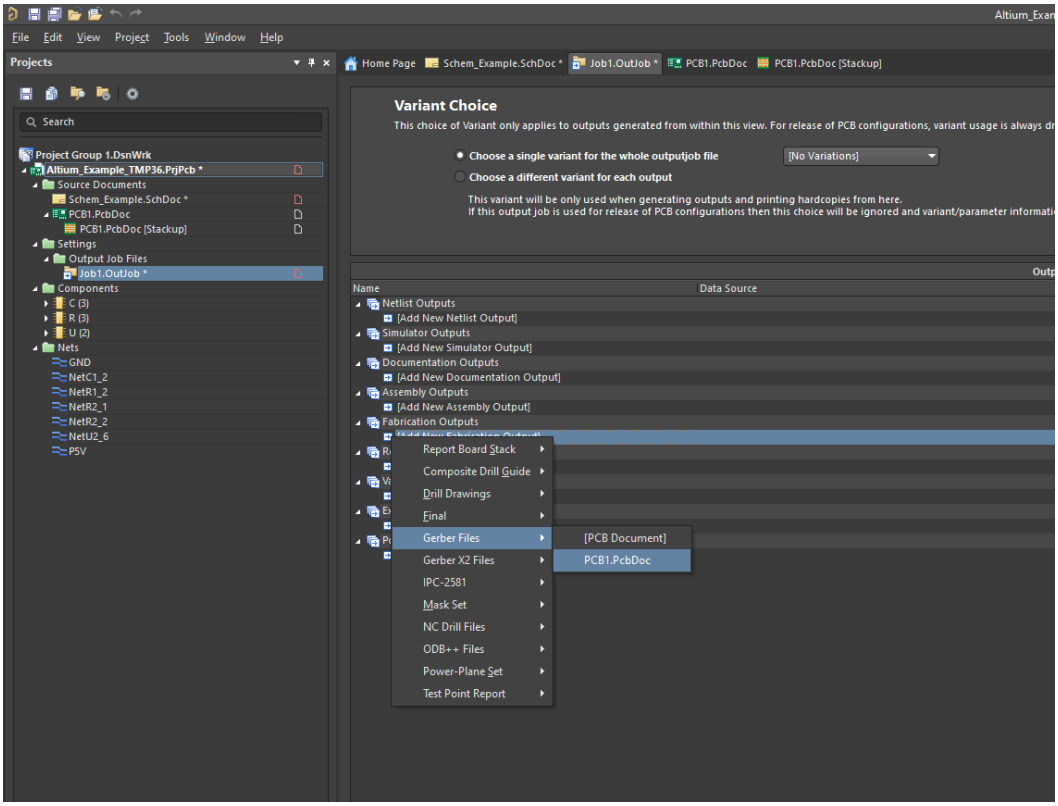


Output Job Guide:

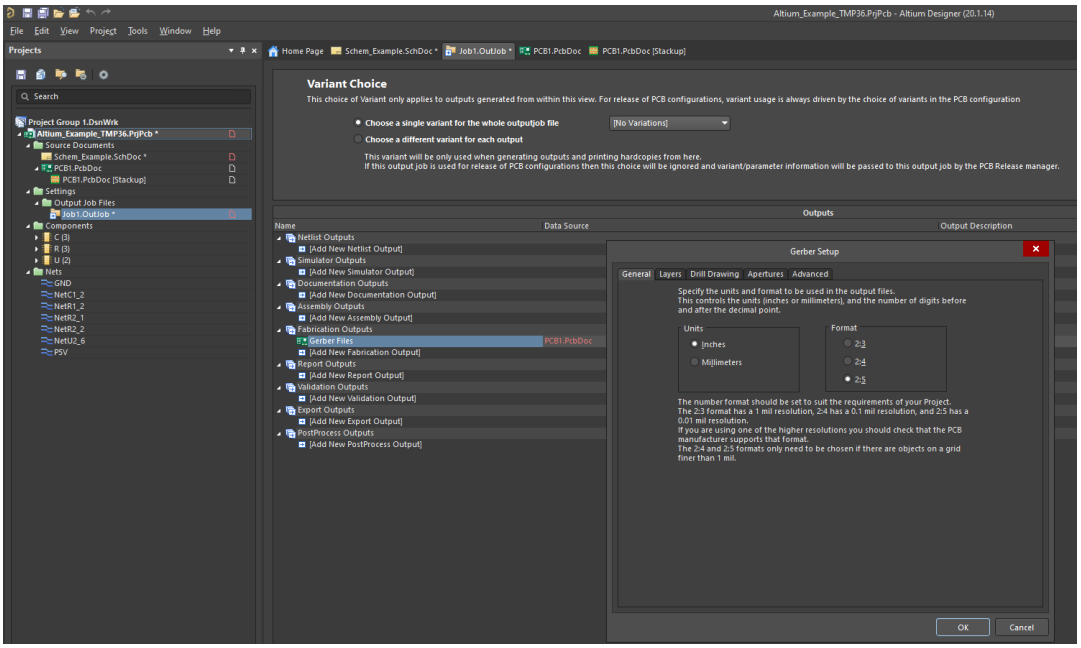




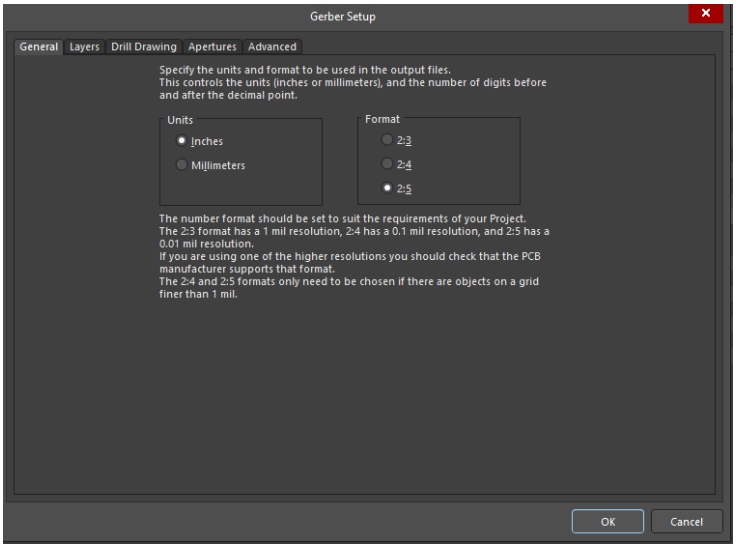
Fabrication files:



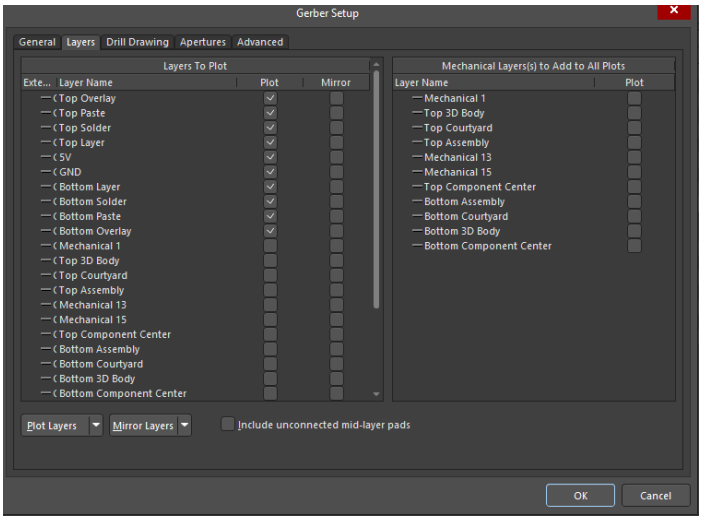
Double click “Gerber Files”



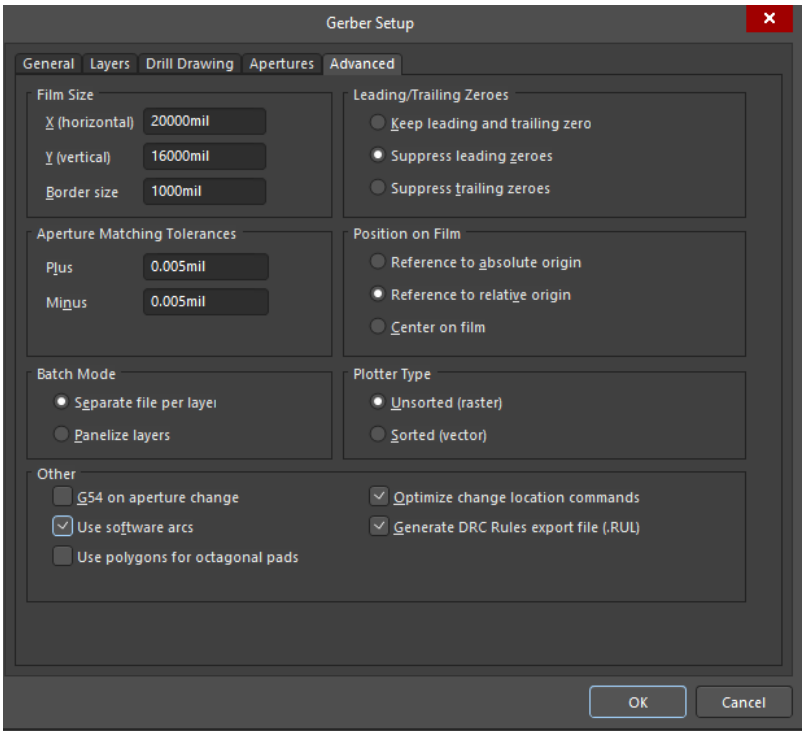
Set these settings up:



Under “Layers” Click the following:

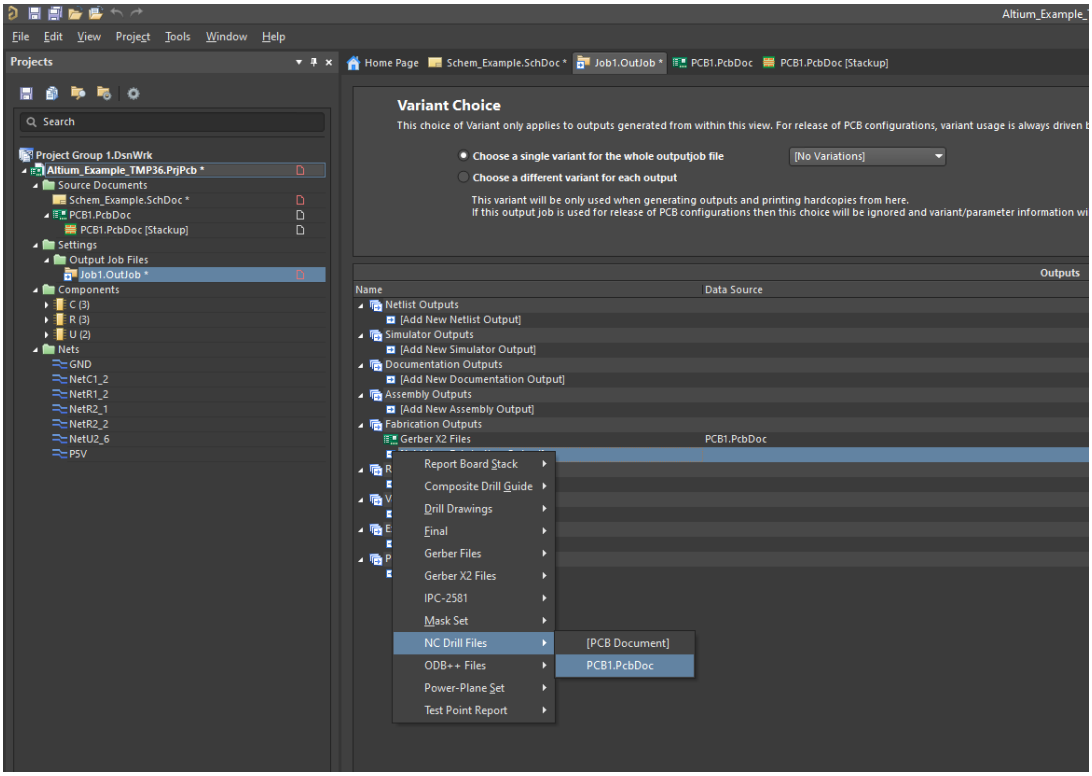


Under Advanced: (click use software Arcs)

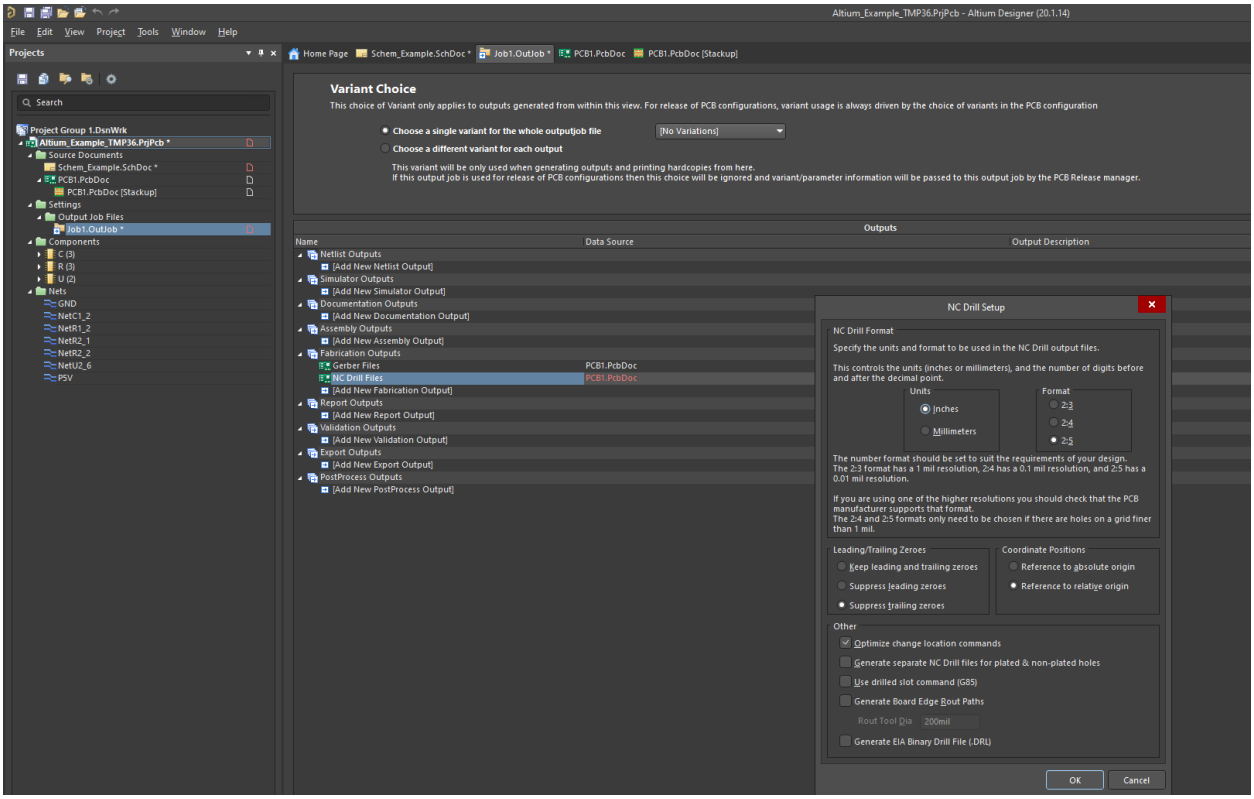


Clic

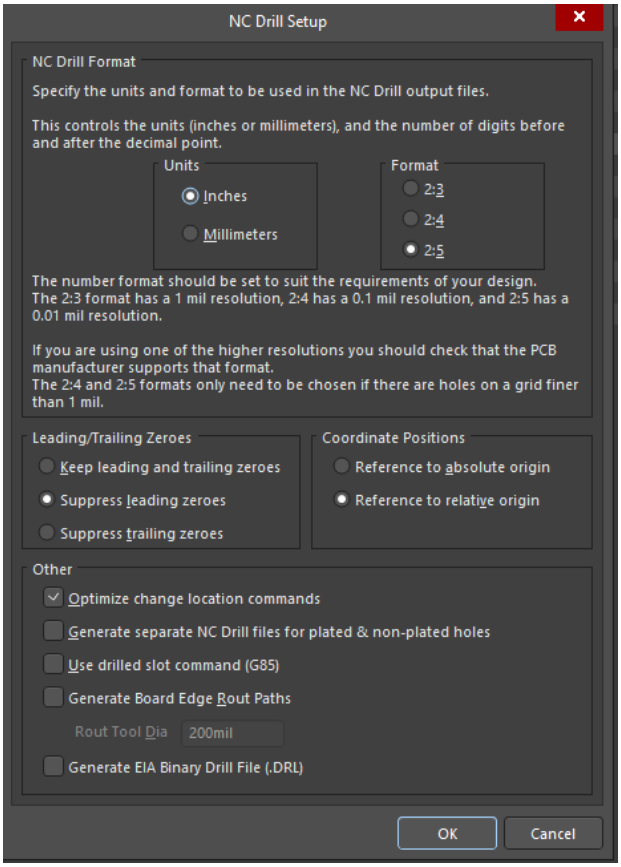
NC Drill Files:



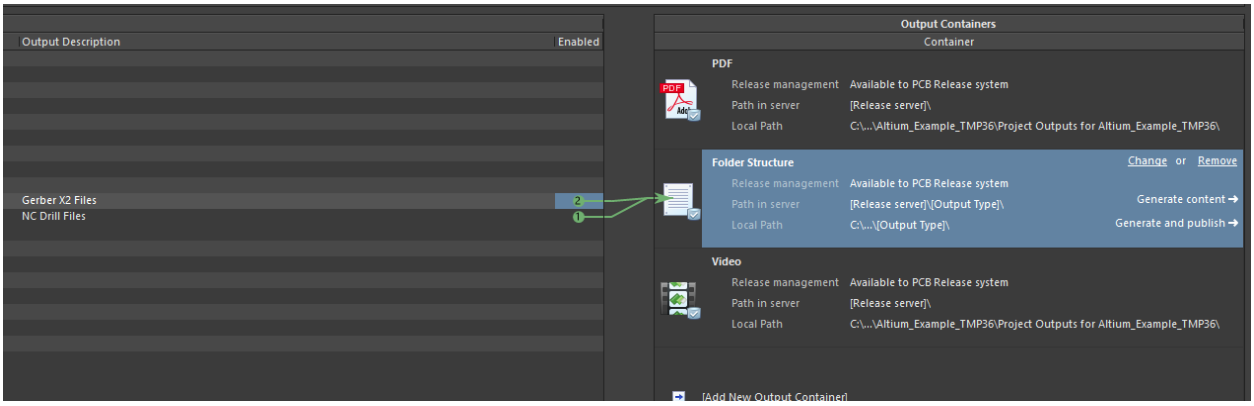
Double click NC Drils:



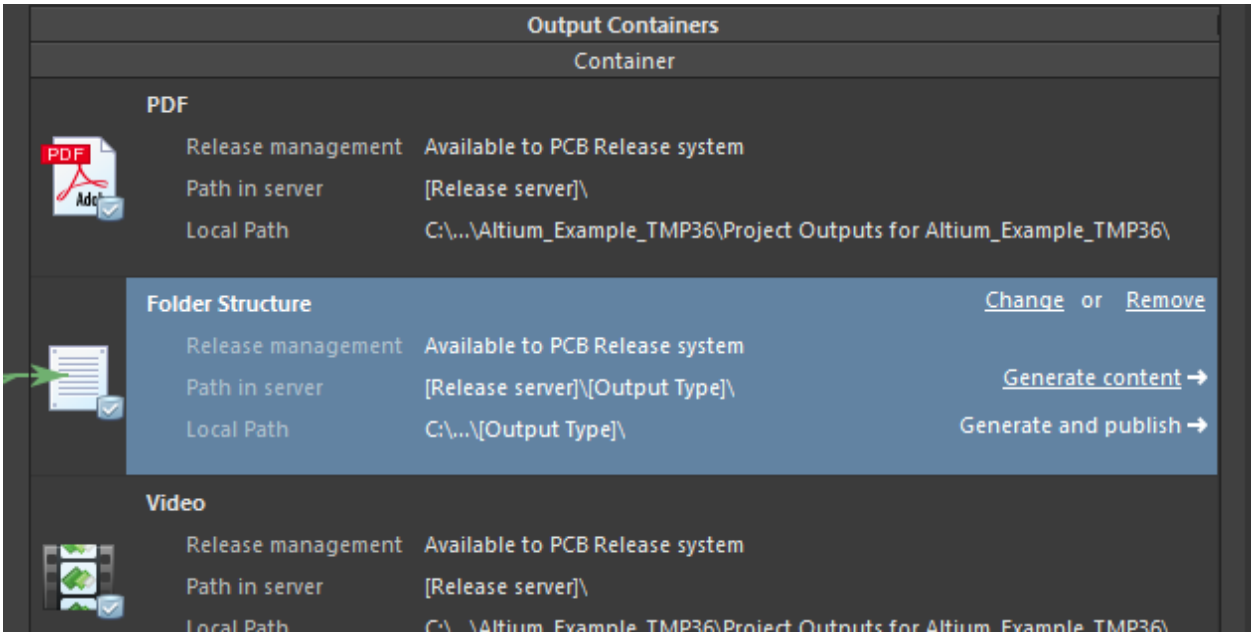
Change to these settings:



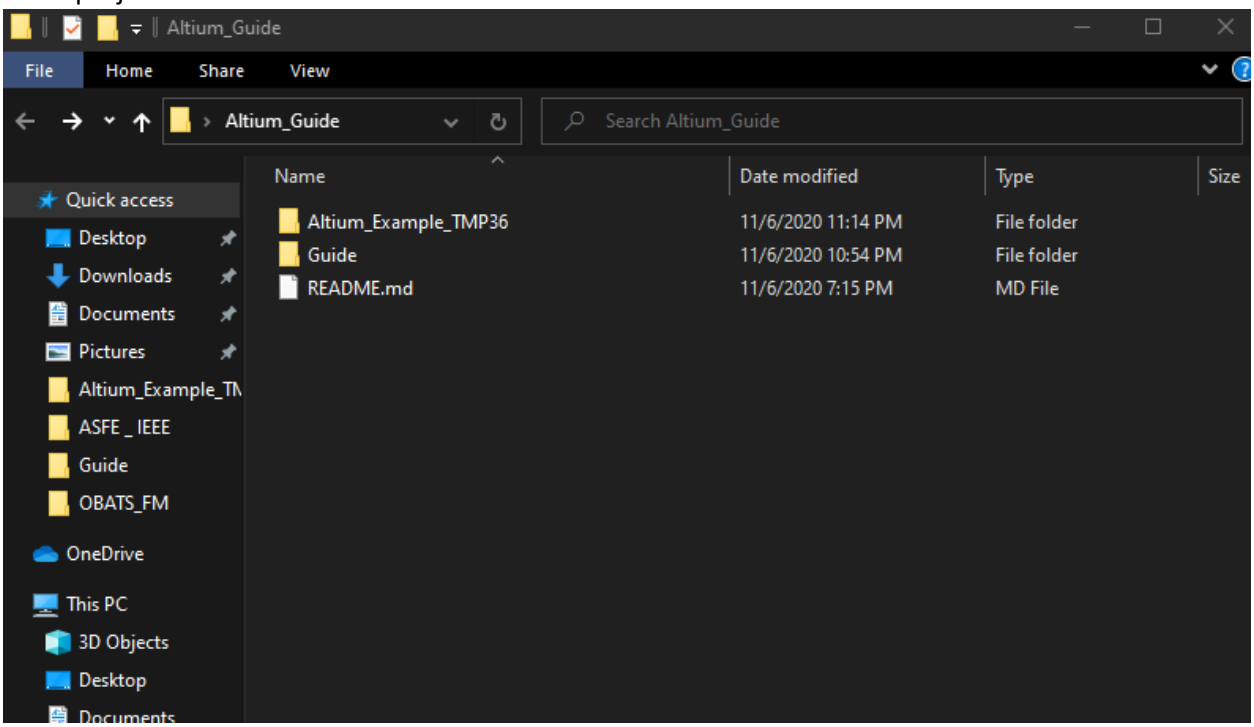
Hit 2 dots near “Folder Structure”

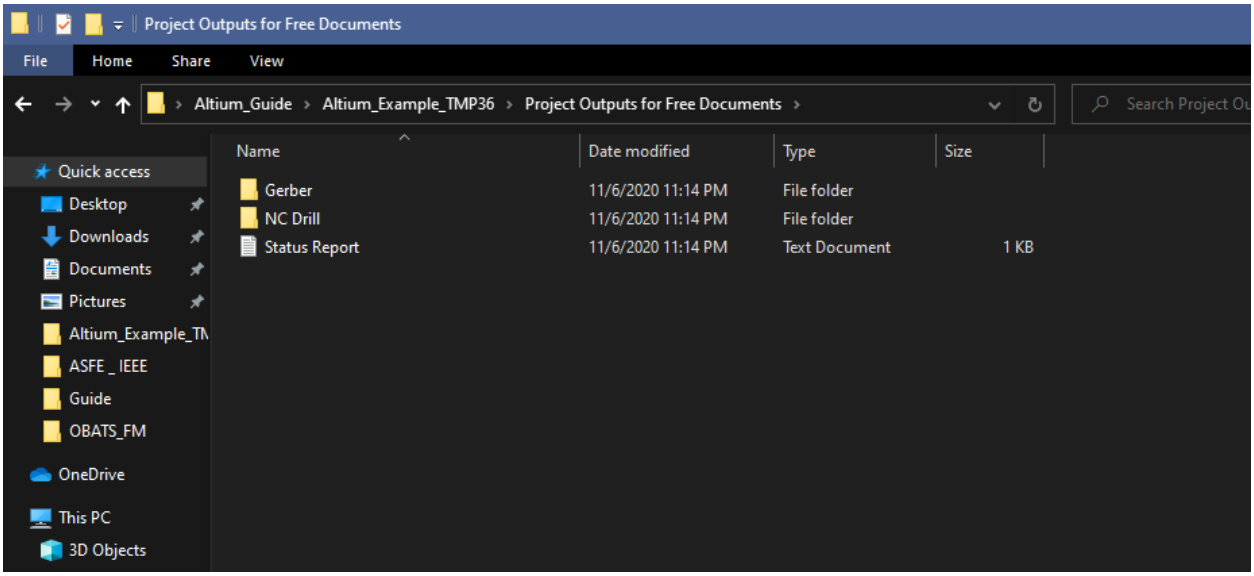


Click “Generate Content”:

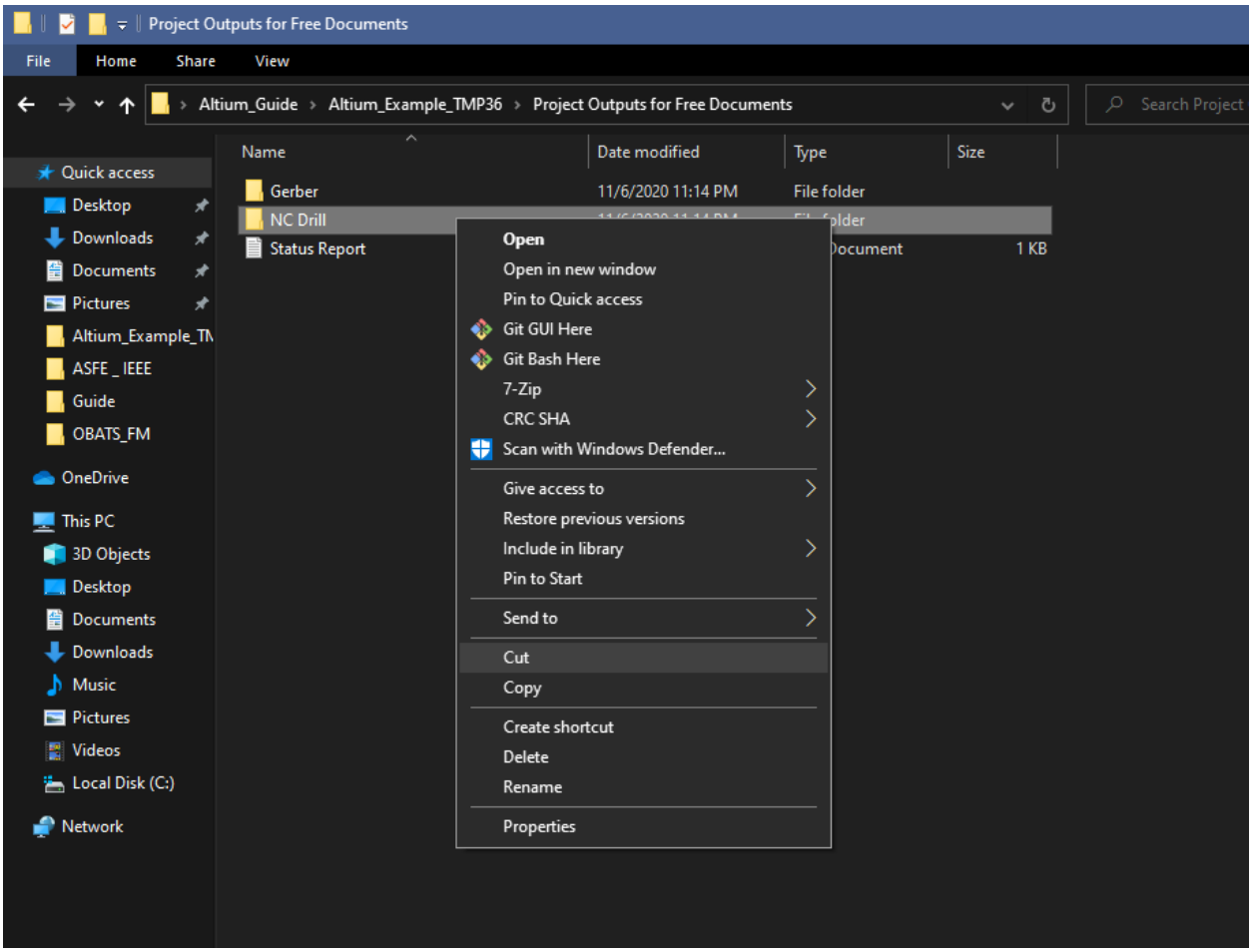


Go to project folder:





Cut the NC Drills folder and paste into Gerber folder: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Altium_Example_TMP36
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Search Project
Quick access
Desktop
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Git Bash Here
7-Zip
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Scan with Windows Defender...
Give access to
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Include in library
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Rename
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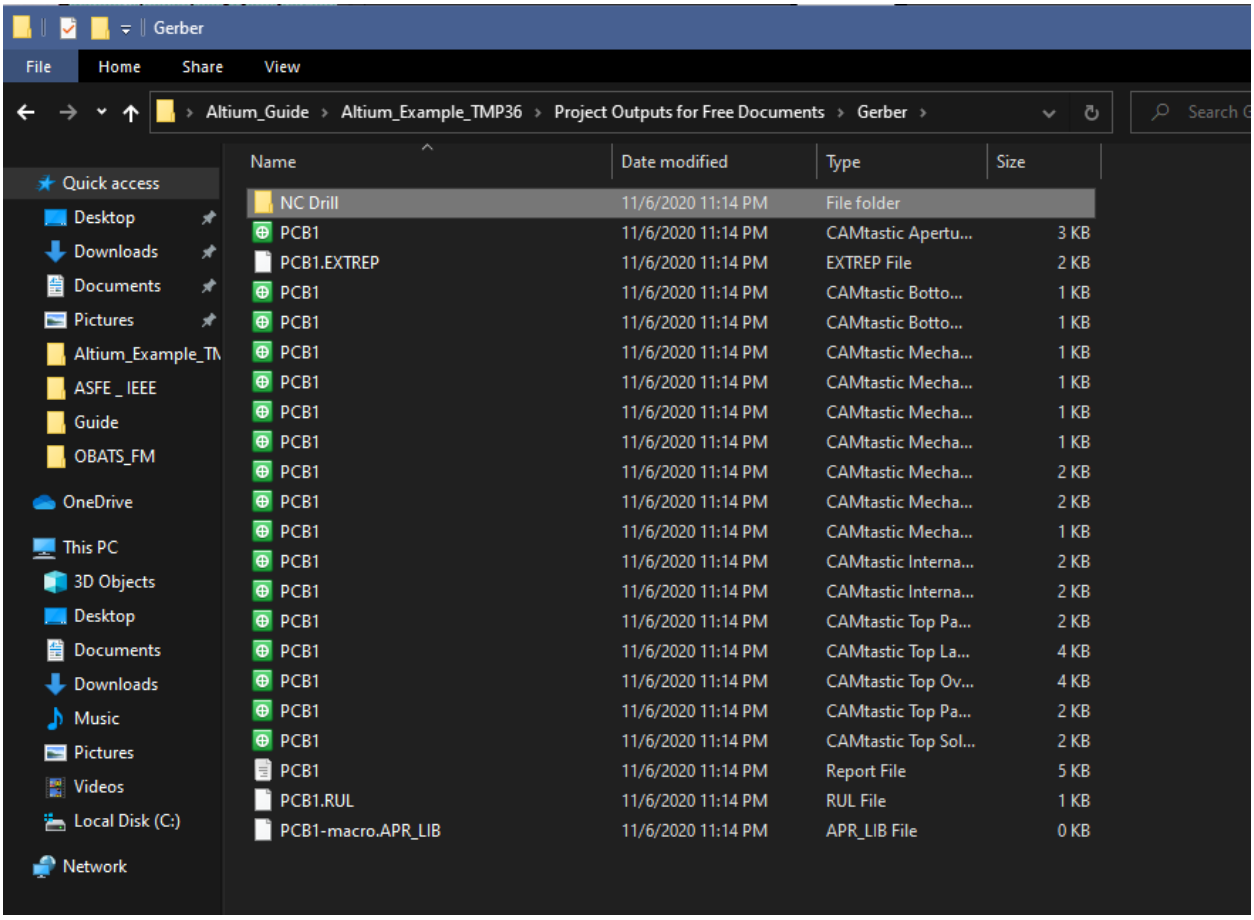
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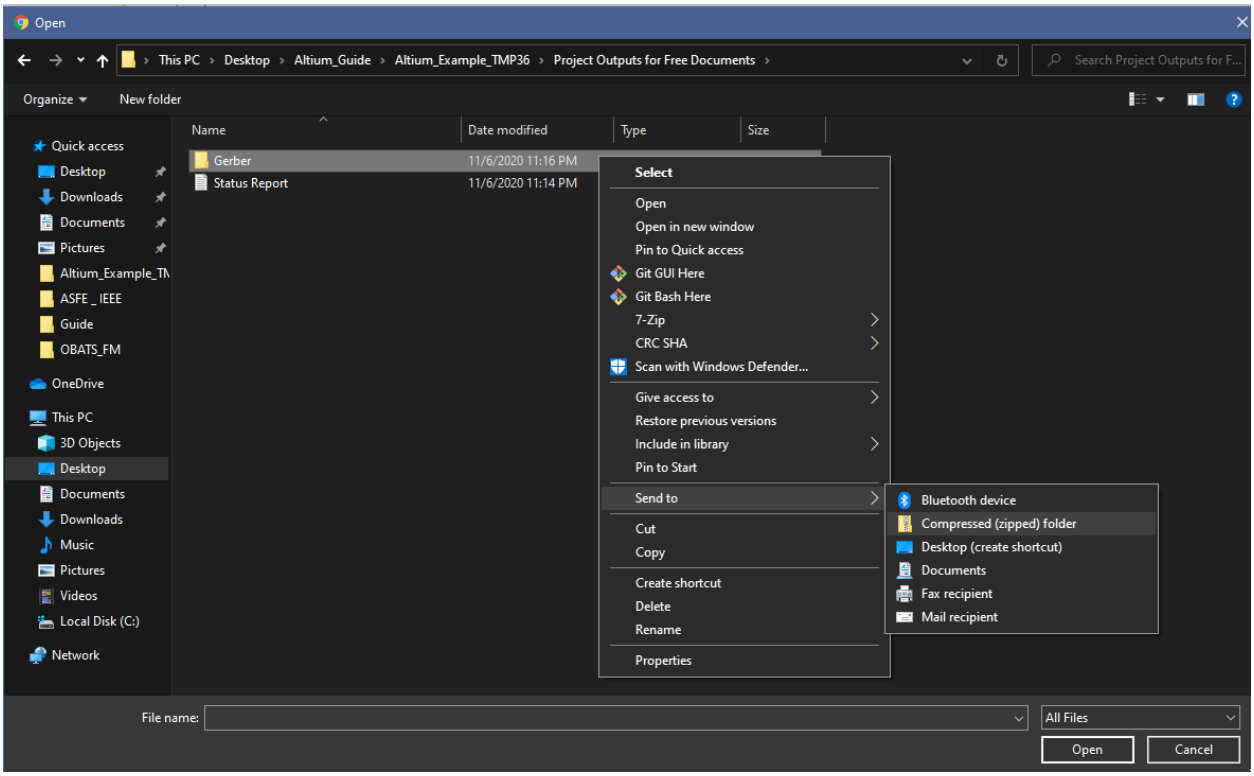
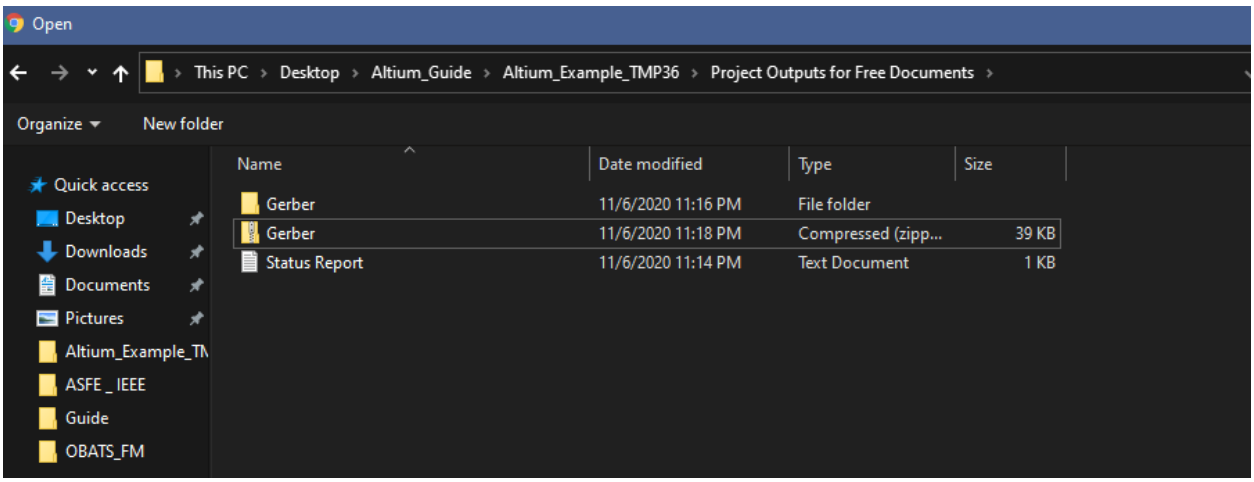
PCB1-macro.APR_LIB 11/6/2020 11:14 PM APR_LIB File 0 KB

Compress the Gerber Folder:





Upload zip folder to OSHPARK: