Project Title: Enabling long wavelength streaking for attosecond x-ray science

PI(s): Ryan N Coffee
Institution: SLAC National Accelerator Laboratory
Collaborations: LCLS, AD, L2SI, PULSE, DESY, XFEL, Stanford CS

Begin Date: 9/2018
End Date: 9/2020

Presenter Name: Ryan N Coffee

Project goals and accomplishments

Major goals:

- Install eToF array on LCLS(-II) and benchmark time-energy resolution by end of Run 18 (Nov-Dec 2020)
- Attosecond Streaking demonstration with streaming pulse reconstruction

1) On schedule for hardware and electronics.
2) Slightly ahead of schedule for simulations and machine learning development.
3) On schedule for FPGA deployment.

Accomplishments:

- Initial DESY tests for MCP depletion
- Upgraded digitizers on order
- Designed Detector Flange assembly and first two units in fabrication
- Test set of small pore MCPs on order
- Oversize ML model works well at 25 e-/angle/shot
- Docker containers with Vivado HLS and spatial-lang for FPGA development

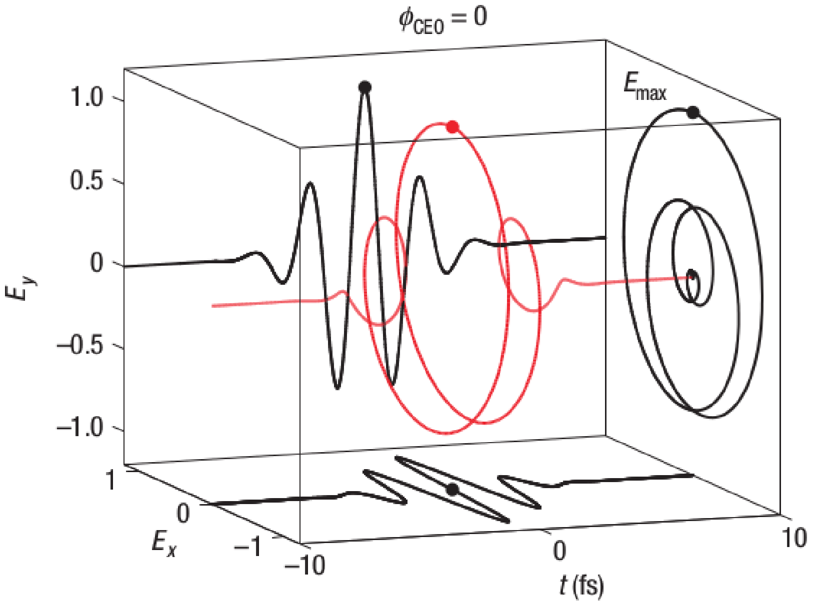
Machine Learning successfully predicts x-ray temporal shape

Outline

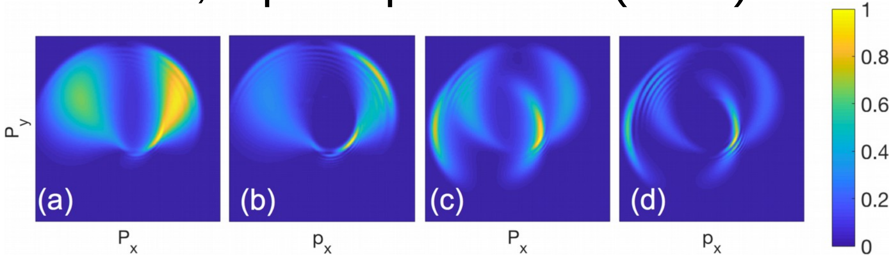
- Angular Streaking and the “CookieBox”
- Machine Learning
- Integrative Design
- Engineering and Project coordination

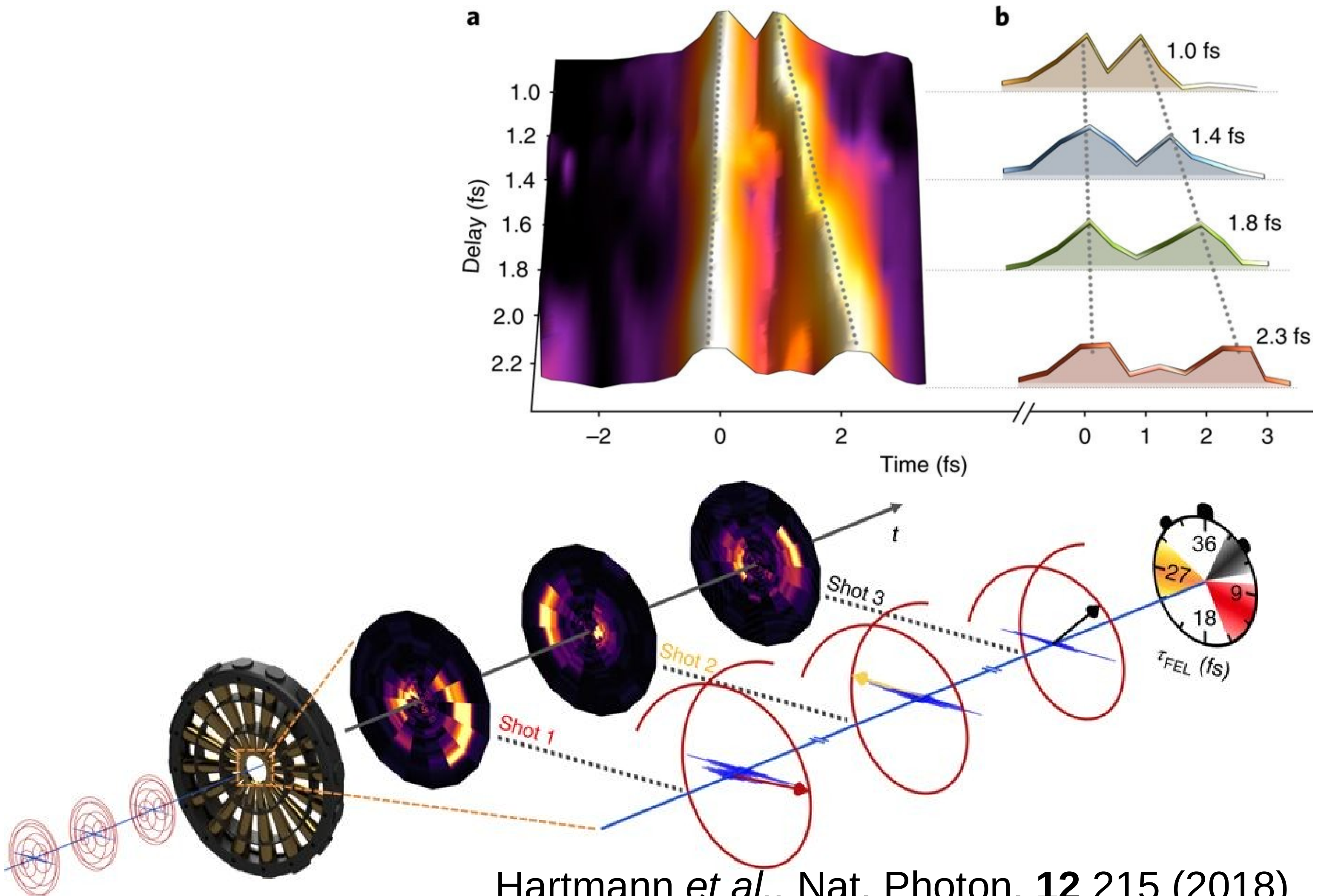
Attosecond Angular Streaking

Eckle *et al.*, Nat. Phys. **4** 565 (2008)



Li *et al.*, Opt. Exp.**26** 4531 (2018)

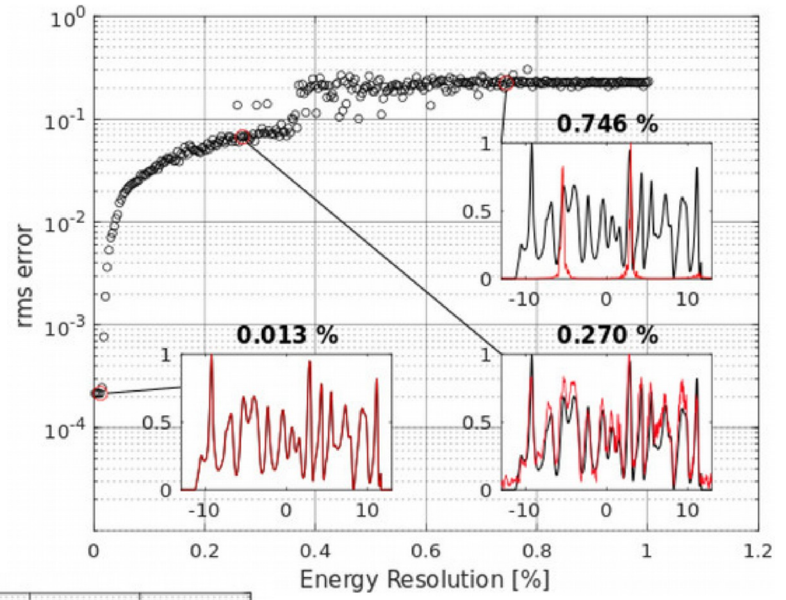


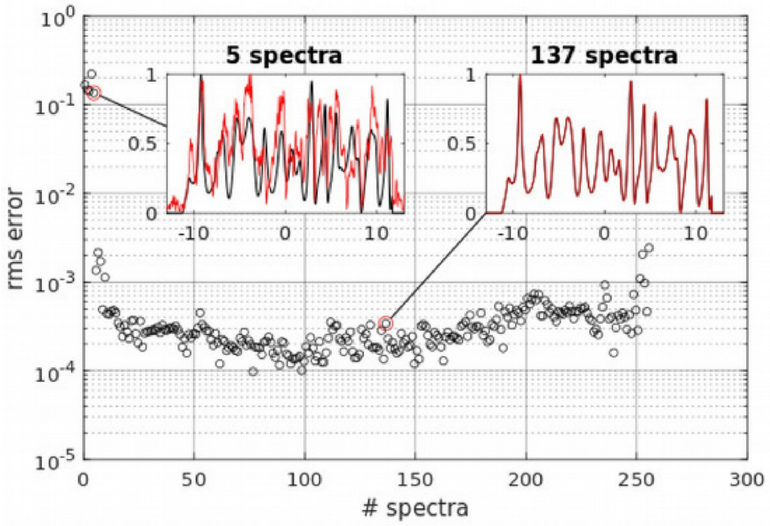


Hartmann *et al.*, Nat. Photon. **12** 215 (2018)

Constraints

- ¼ eV over 50 eV window
- Interleaved retardation
- At least 8 angle samples (16 ideal)
- Prefer >1e-3 collection
- Single shot pulse recovery at beam rate
- Latency for veto/sort decisions below 1ms





Schweizer *et al.*, App. Sci. **8** 1039 (2018)

Why not ARTOF2?

- Need 250 meV resolution over a 50 eV window with keV electrons
- Energy spectrum in single pulse each angle
- Analysis with ms scale latency for data routing and veto

Technical Data

Property	Specification
Max.Theoretical Energy Resolving Power	13000
Energy Resolution	< 0.36 meV FWHM at 2 eV kinetic energy[A]
	< 1.6 meV FWHM at 10 eV kinetic energy[A]
	< 265 meV FWHM at 300 eV kinetic energy[A]
Kinetic Energy Range	0.2 - 1000 eV
Angular Modes	±7°, ±15°
Alignment Mode	Yes
Angular Resolution	<0.06°
Working Distance	34 mm
Pass Energy	Not applicable[B]
Slits	No
Energy Window	CRR: 2%, 5%, 10%, 15%, 20%, 50%, 100%[C]
Vacuum Tank	Electro-polished stainless steel
Mounting	NW200CF
Magnetic Shielding	Double mu-metal liner
Analyser Pump Port	Two
Port Length	300 mm
Lens Clearance	< 40°
Detector Type	Delay-line detector
Detector Interface	Ø 40 mm MCP
Count Rate Tolerance	> 1 MHz[D]
Maximum Repetition Rate	Approximately 3.0 MHz

High Voltage Electronics

Property	Specification
Temperature stability	< 2 ppm/°C (R-version)
Noise (AV at analyser)	< 1 ppm + < 500 µV
Drift	< 20 ppm/year
Electric isolation	6 kV
Min. step size HV100	1.6 mV
Min. step size DAC	200 µV
DAC bits	16
Modular	Yes
Communication	USB

[A] Calculated for 2 % energy window, ±15° angular mode, and 50 µm sample radius.

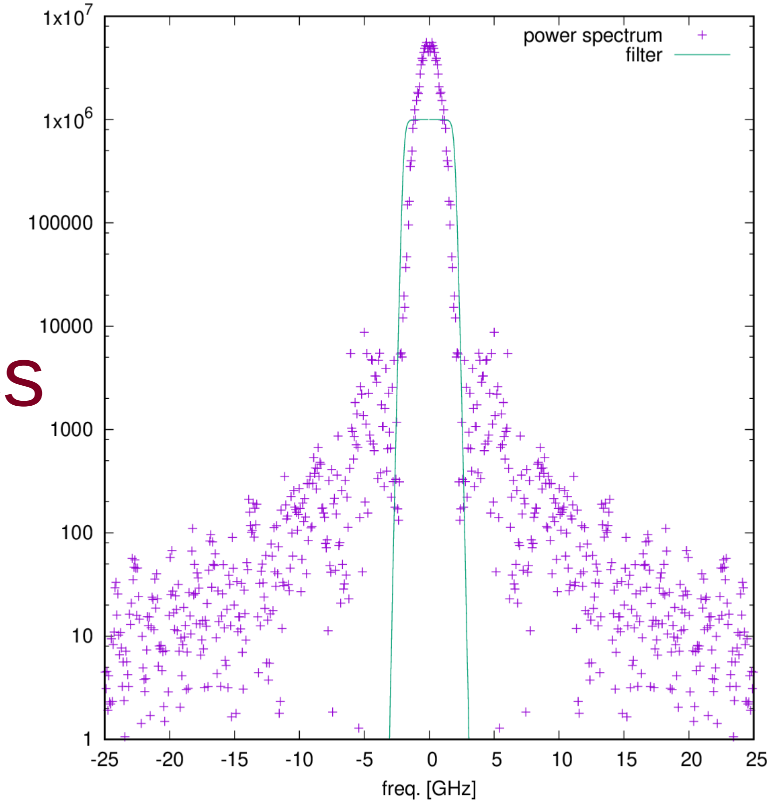
[B] Set instead by a time window in the spectrometer and optimized lens tables for each kinetic energy window.

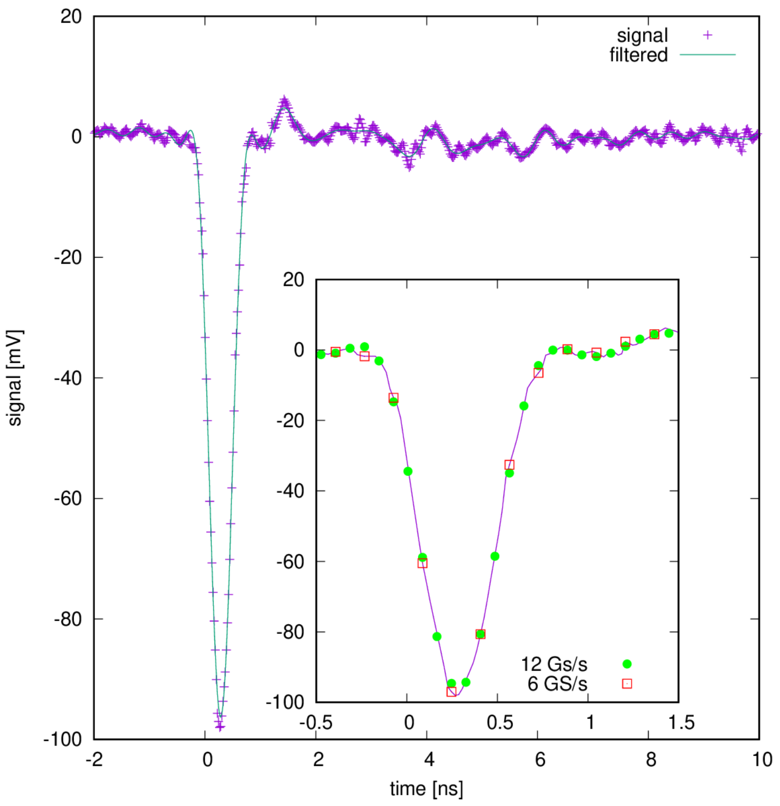
[C] Available in a limited kinetic energy range

[D] Property of the RoentDek DLD40 detector.

MCP waveform measurements

- Tests in Dec-18 / Jan-19
- 50 GSps scope
- 25 GHz BWD
- Keep the electronics above 5GHz





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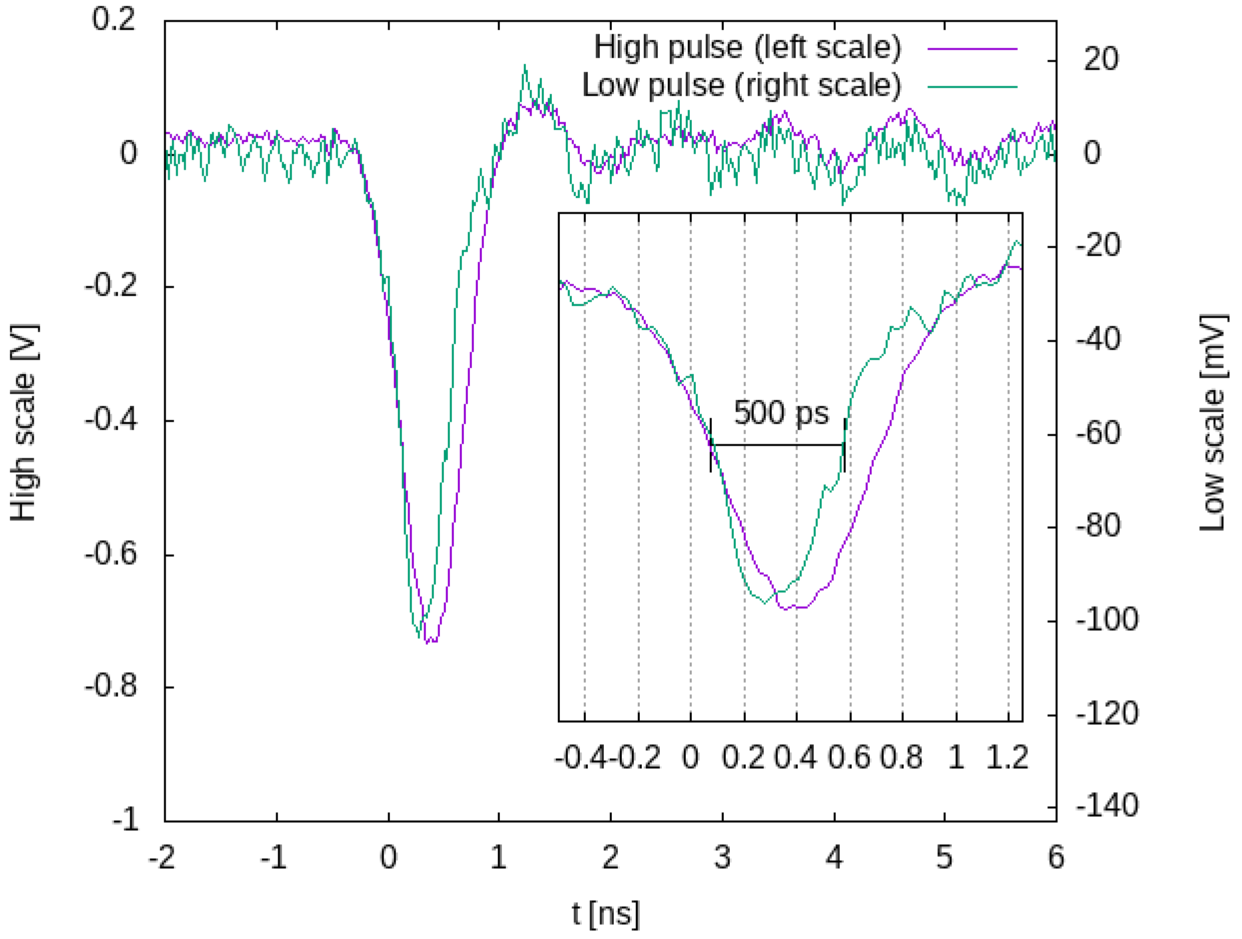
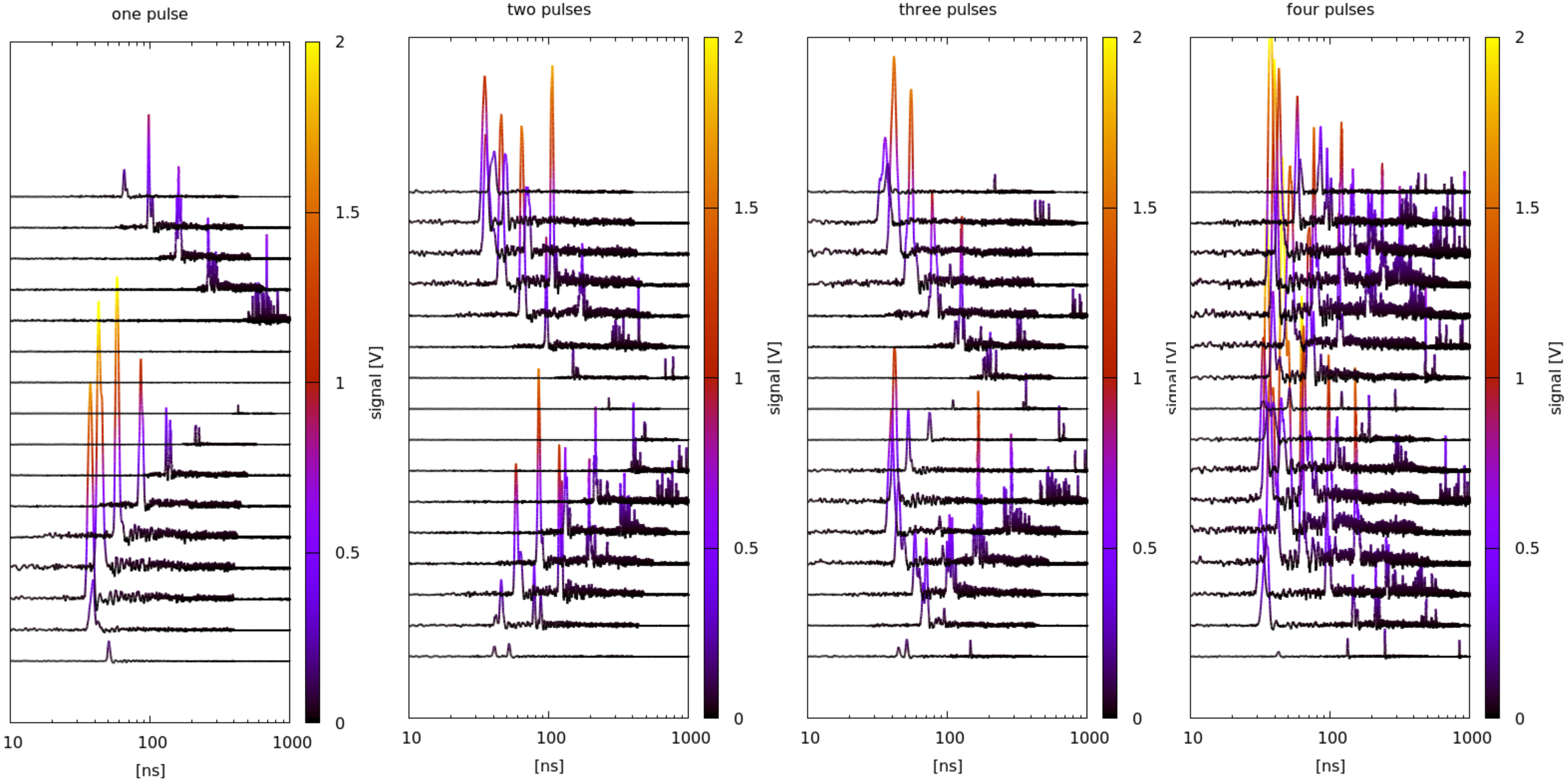
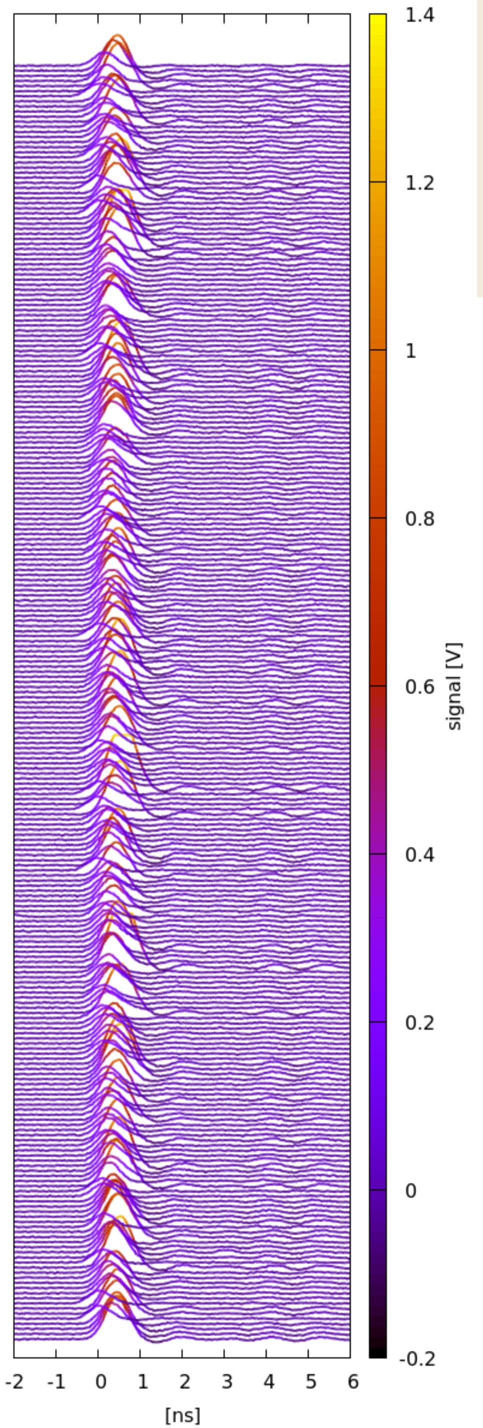
- We're going to hate gain in the end



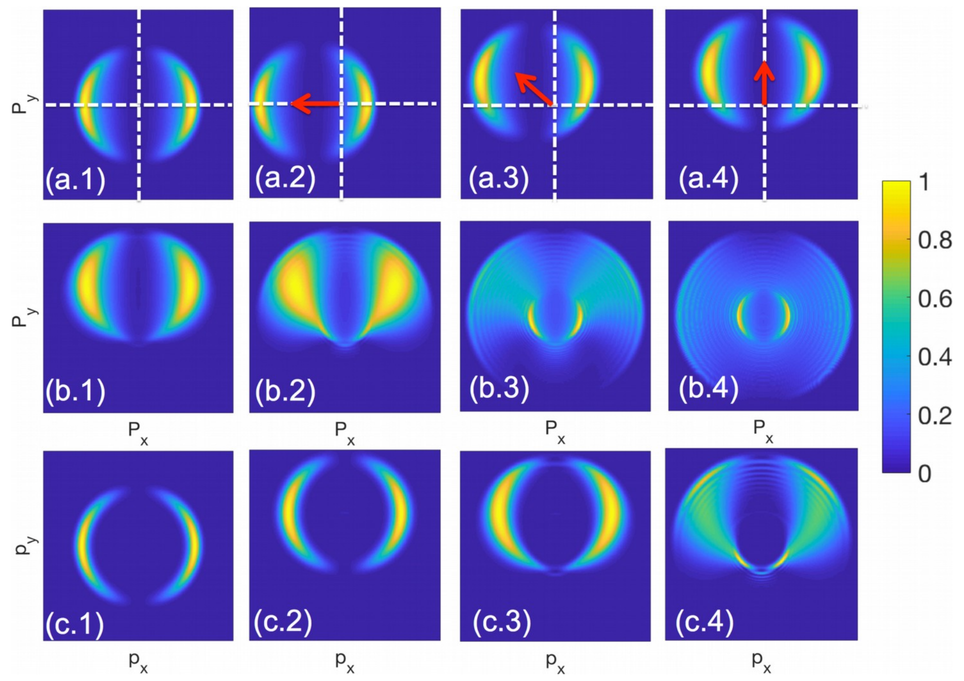
Measurement based Simulations

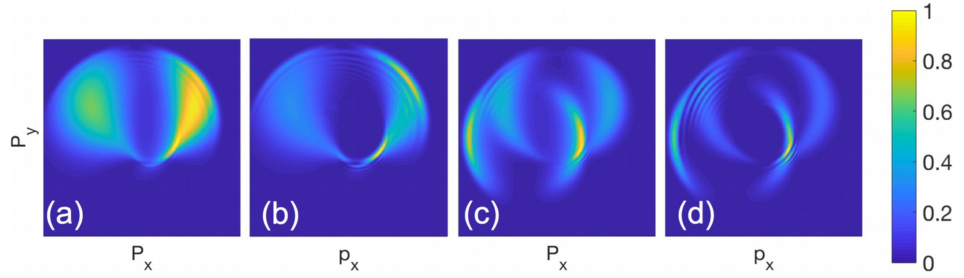




Machine Learning results

- Compute the momentum distribution from Angular streaking simulation [1]
- Sample the momentum space PDF
- Convolve with measured impulse response
- Feed temporal waveforms as if nX16 image





Li *et al.*, Opt. Exp. **26** 4531 (2018)

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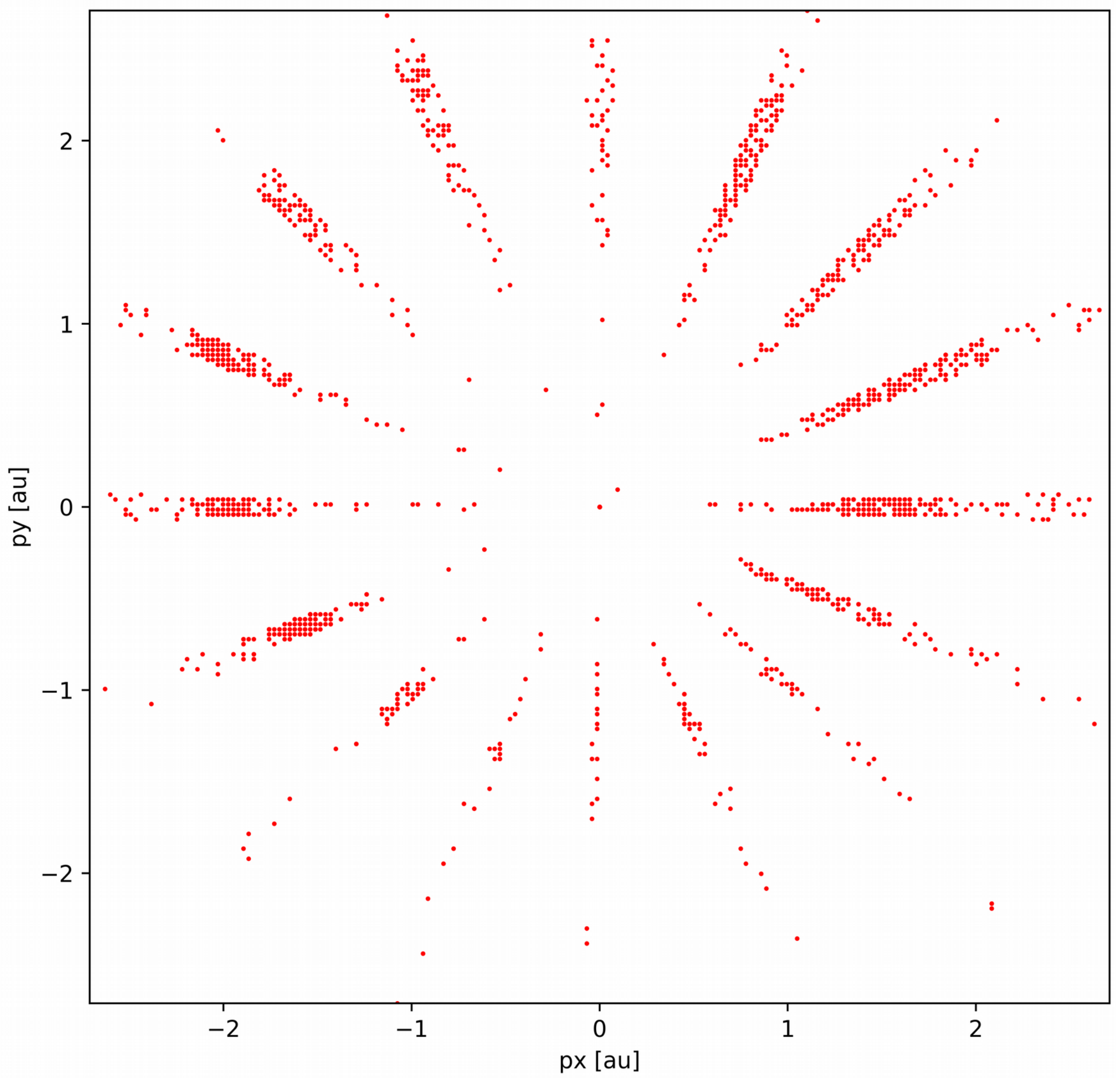
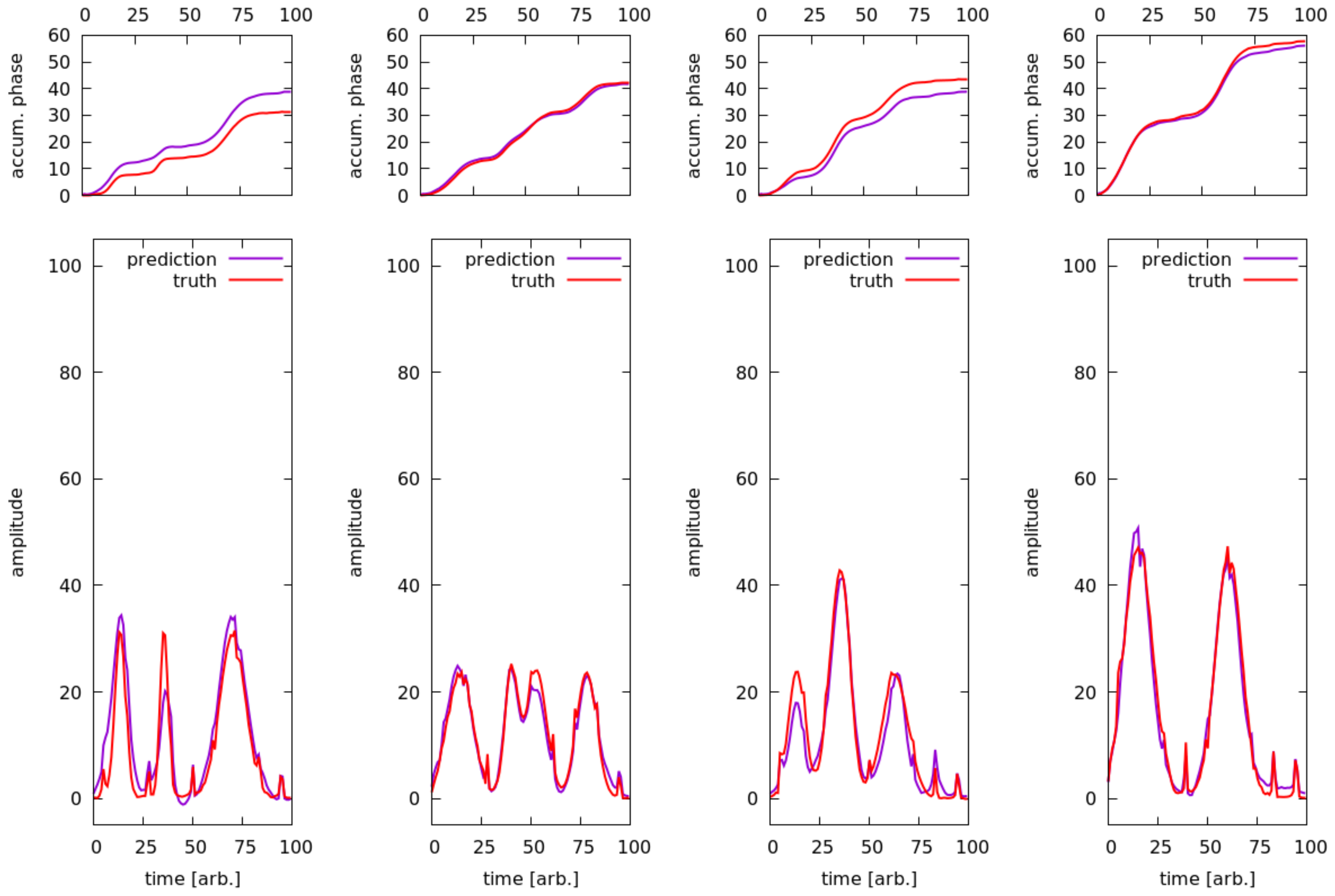


Machine Learning Results

- Promising initial results for Machine Learning inference based on ~50 e-/shot
- At ~12 e-/shot retrieval is challenging
- Look into adaptive Kernel Density Estimation



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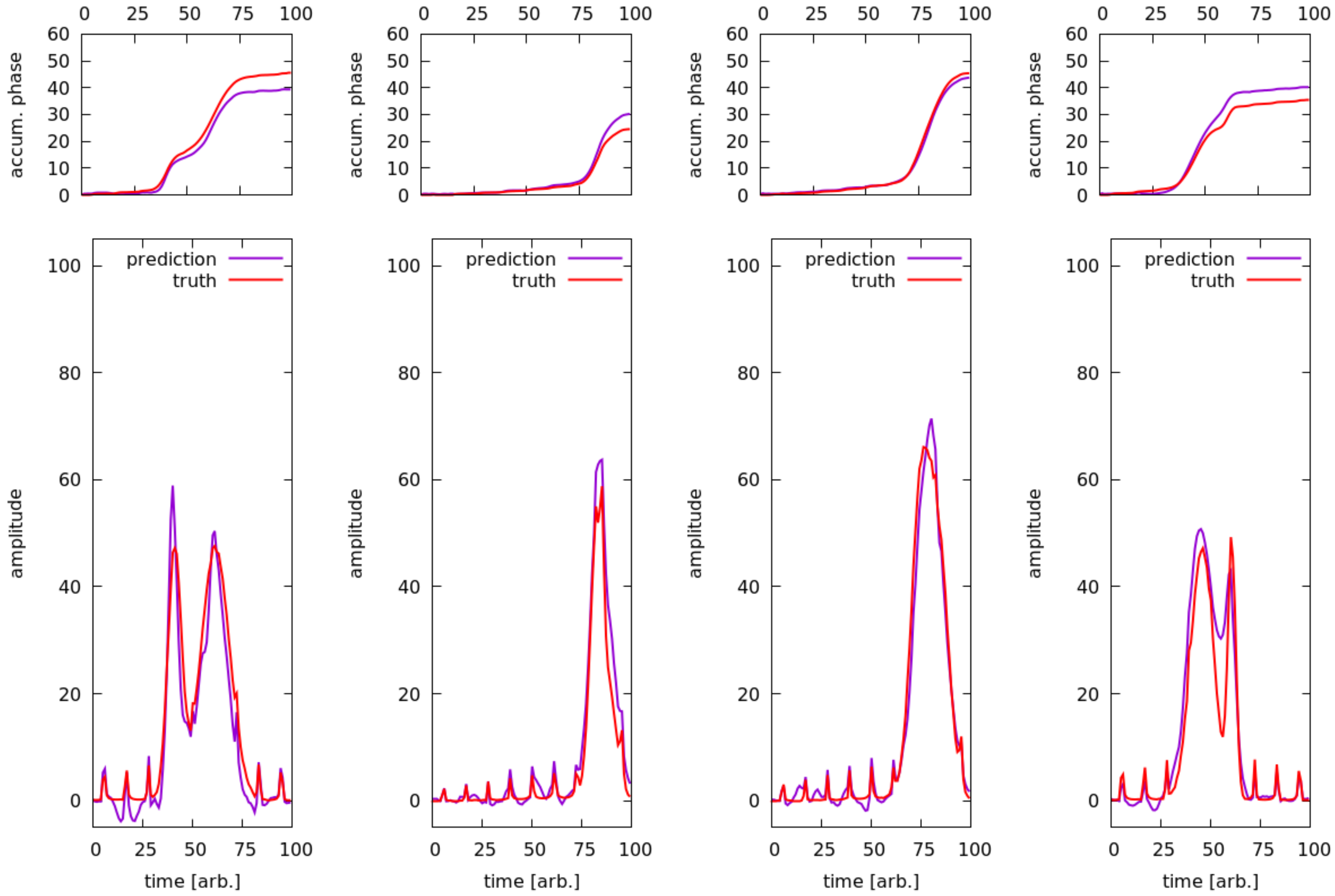

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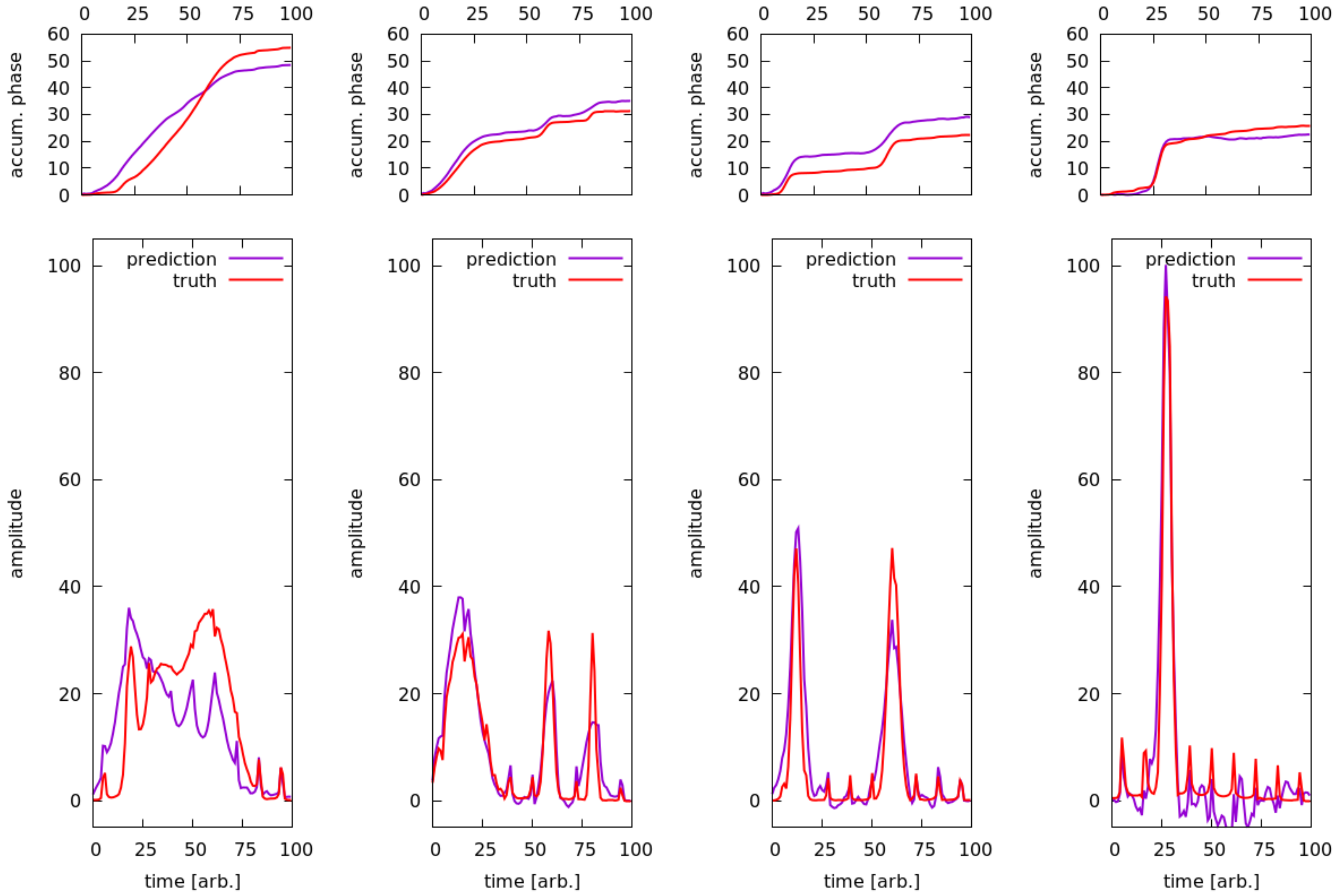
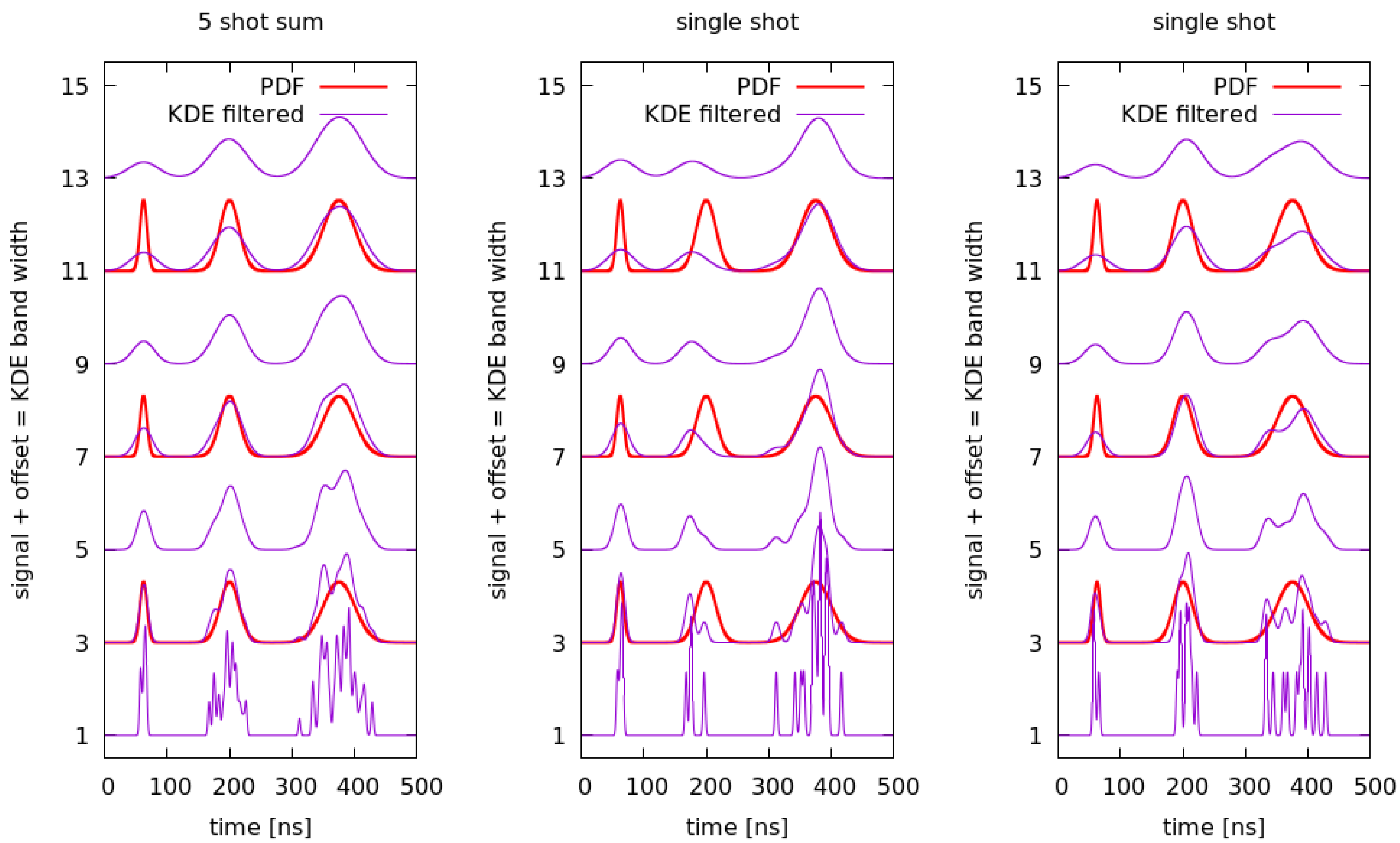


MCP Depletion Study

- FLASH beamtime ran Hamamatsu F9890-31 MCPs at 50 counts/shot with 1MHz bunch train (600 μsec duration)
- Depletion of signal from 1V to 100mV by the end of th ebunch train
- Based on the Hamamatsu , we have ordered two model F9890-32 MCPs to test with PULSE EUV source and then with the Tavella High rep-rate source in neighboring lab.

Kernel Density Estimation

- Applied Physics student Debadri Das
- Kernel shapes vary across the waveform
- Not a typical CNN modality
- Benefit by constrianing center at this stage – motivates 2 channels into initial FPGA
- Expand resources on FPGA



Kernel Density Estimation

SLAC

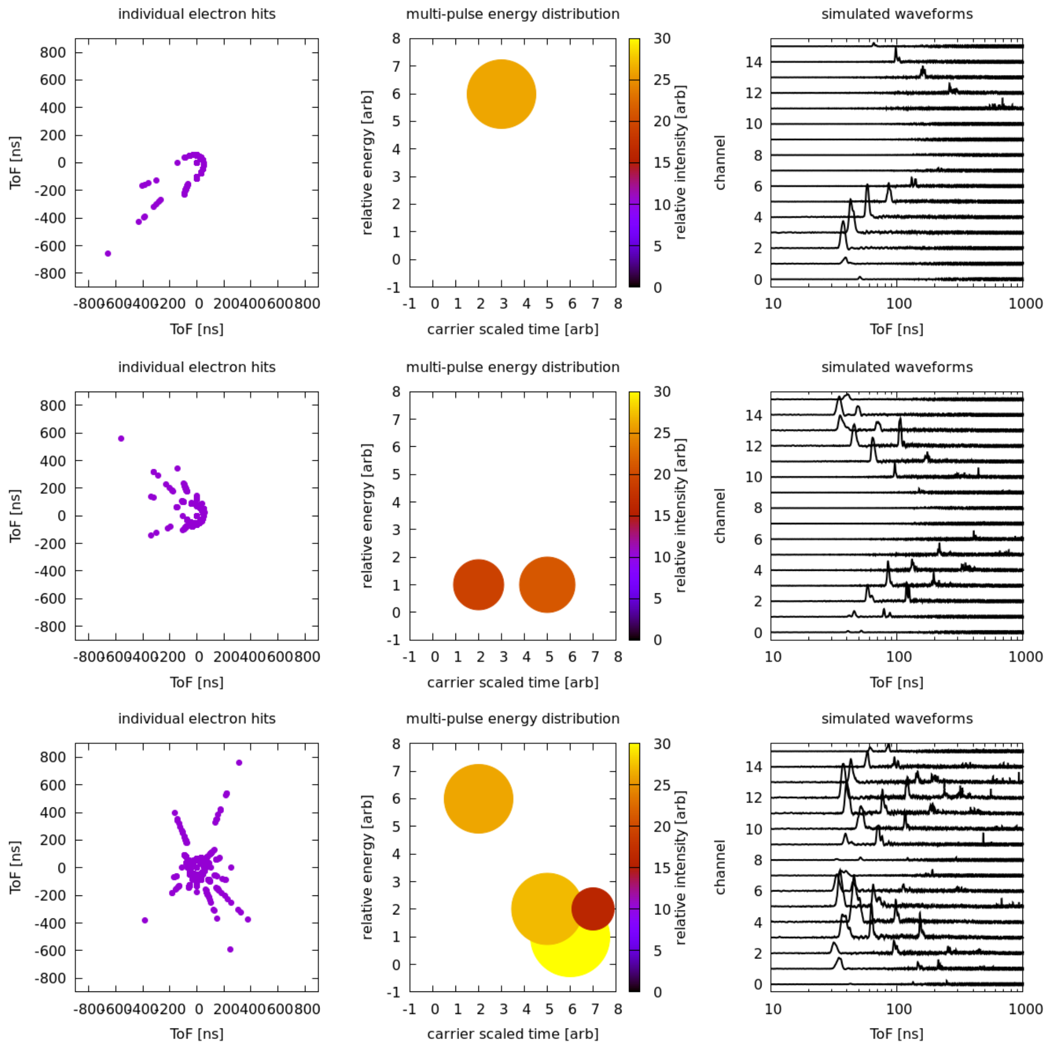
- Applied Physics student
  D
- K
  a(
- N
  m
- B
  c
  m
  in
- E
  FPGA

Kintex® UltraScale™ FPGAs

	Device Name	KU025[1]	KU035	KU040	KU060	KU085	KU095	KU115
Logic Resources	System Logic Cells (K)	318	444	530	726	1,088	1,176	1,451
	CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
	CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Memory Resources	Maximum Distributed RAM (Kb)	4,230	5,908	7,050	9,180	13,770	4,800	18,360
	Block RAM/FIFO w/ECC (36Kb each)	360	540	600	1,080	1,620	1,680	2,160
	Block RAM/FIFO (18Kb each)	720	1,080	1,200	2,160	3,240	3,360	4,320
	Total Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
	I/O DLL	24	40	40	48	56	64	64
I/O Resources	Maximum Single-Ended HP I/Os	208	416	416	520	572	650	676
	Maximum Differential HP I/O Pairs	96	192	192	240	264	288	312
	Maximum Single-Ended HR I/Os	104	104	104	104	104	52	156
	Maximum Differential HR I/O Pairs	48	48	48	48	56	24	72
Integrated IP Resources	DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
	System Monitor	1	1	1	1	2	1	2
	PCIe® Gen1/2/3	1	2	3	3	4	4	6
	Interlaken	0	0	0	0	0	2	0
	100G Ethernet	0	0	0	0	0	2	0
	16.3Gb/s Transceivers (GTH/GTY)	12	16	20	32	56	64[2]	64
Speed Grades	Commercial	-1	-1	-1	-1	-1	-1	-1
	Extended	-2	-2 -3	-2 -3	-2 -3	-2 -3	-2	-2 -3
	Industrial	-1 -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -2	-1 -1L -2

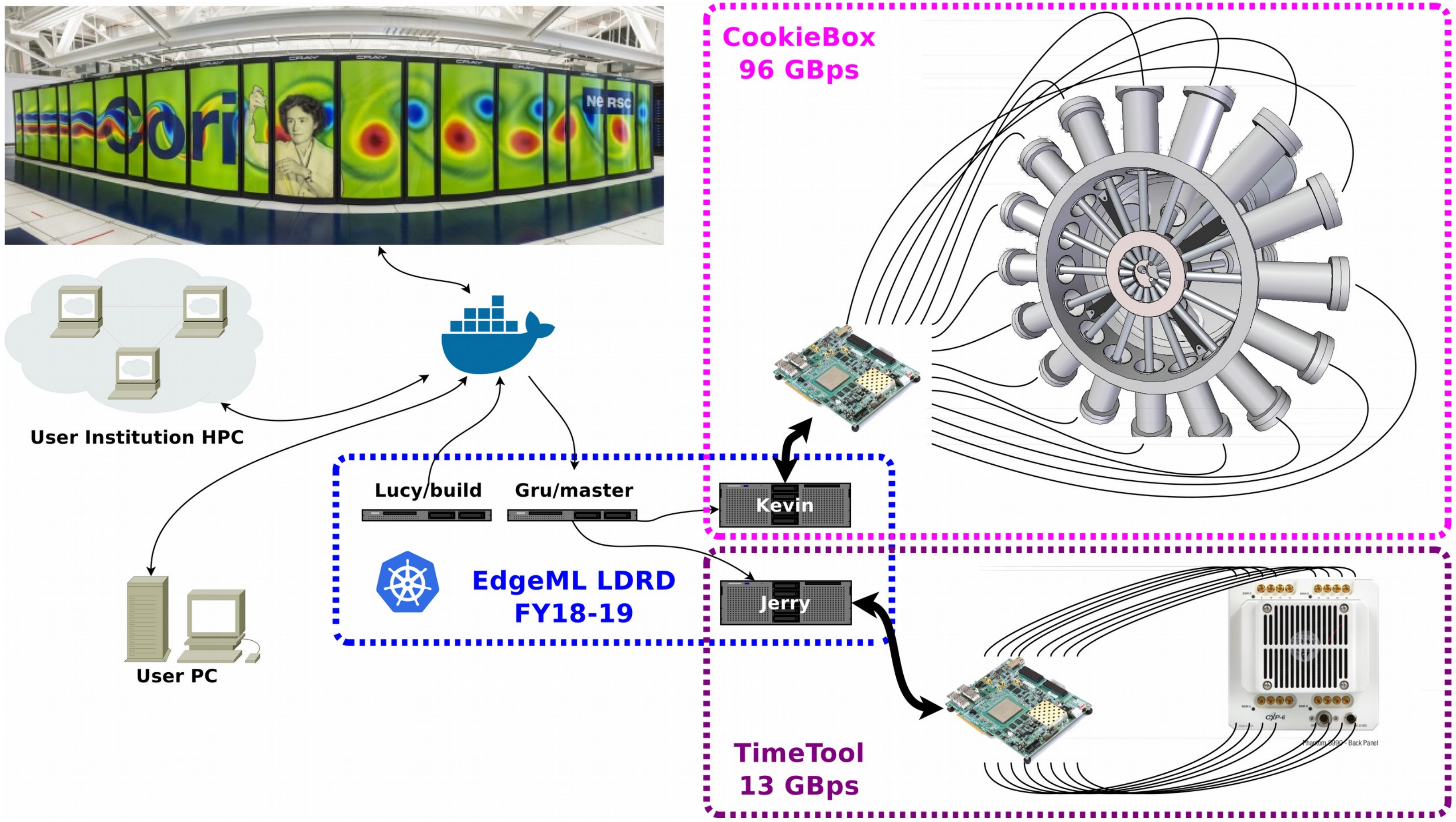
Alternative is Recurrent Neural Network

- Hidden state evolves to final answer after processing sub-strings
- Like processing sentences
- Same word, different meanings depending on placement in the sentence string
- 16 sentences define an angular streaking measurement
- Sentiment analysis of the 16 sentences uncovers ‘one-pulse’ or ‘delay-at-same-energy’, etc.



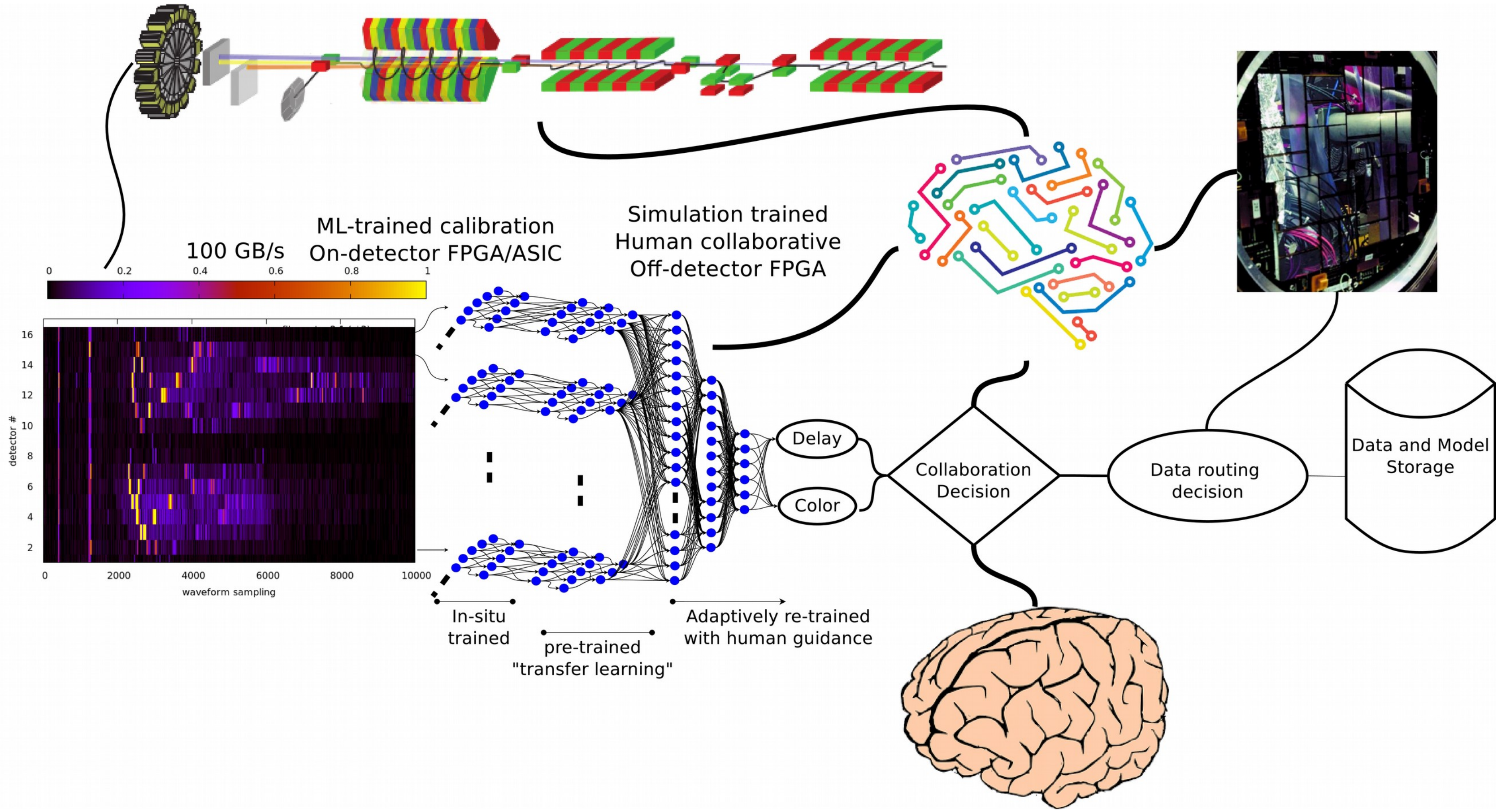
EdgeML LDRD + new TID-AIR LDRD

- Co-leading and leveraging lab EdgeML initiative
- Building industry partners
- Defining a sharable development environment container image
- Based on industry compatible development tools

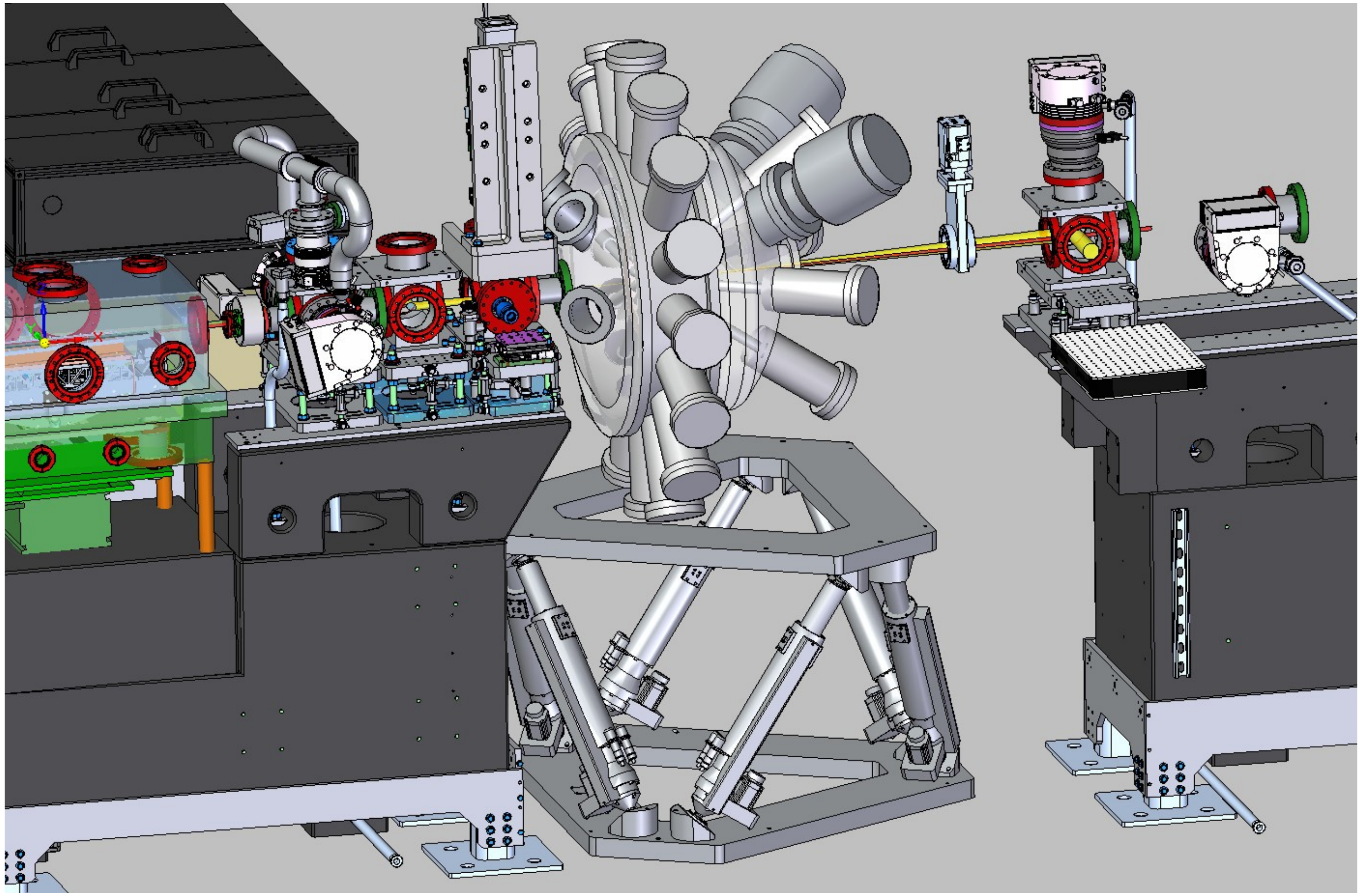


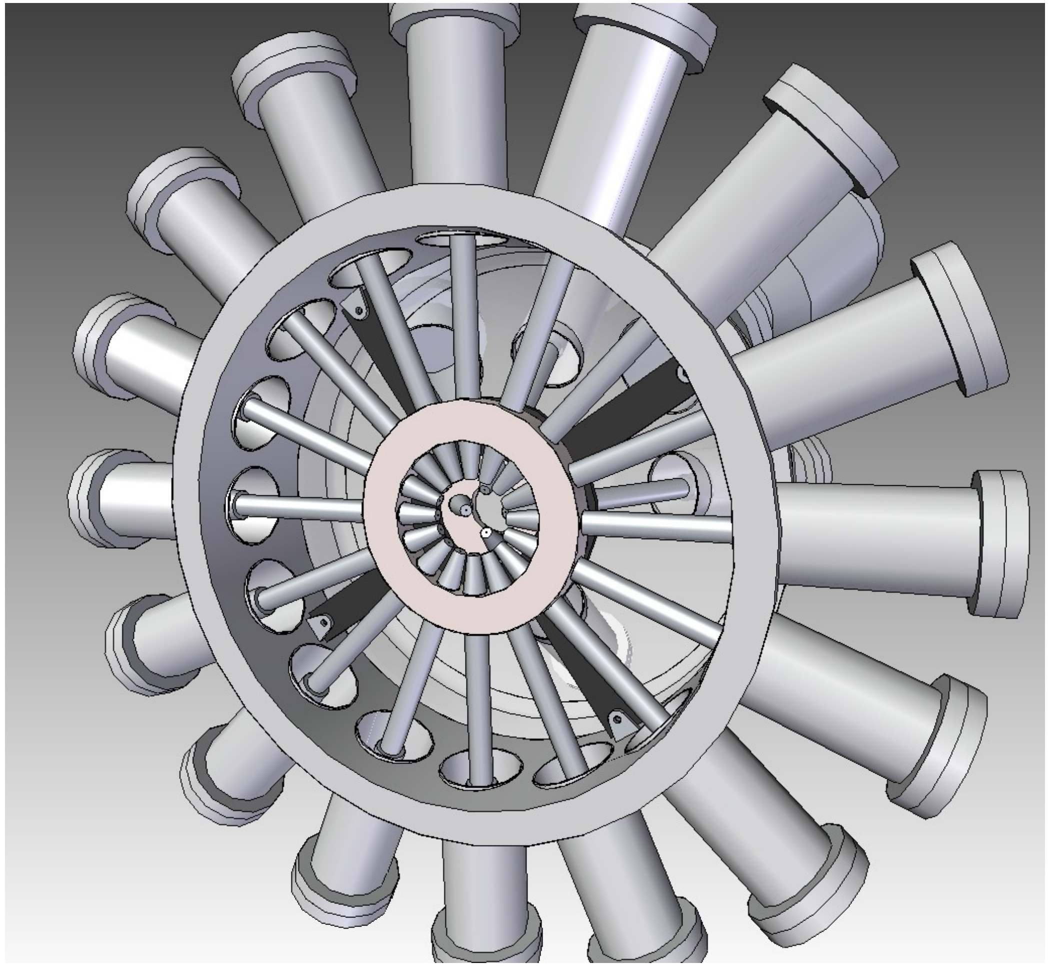
Co-design principle

- From MCP pore diameter to “Heavy Edge” machine learning
- Integrative adaptation to sub-system shortcomings, e.g. MCP depletion, ToF collection, KDE on FPGA
- Targeting a streaming decision maker diagnostic for data routing and veto in LCLS-II



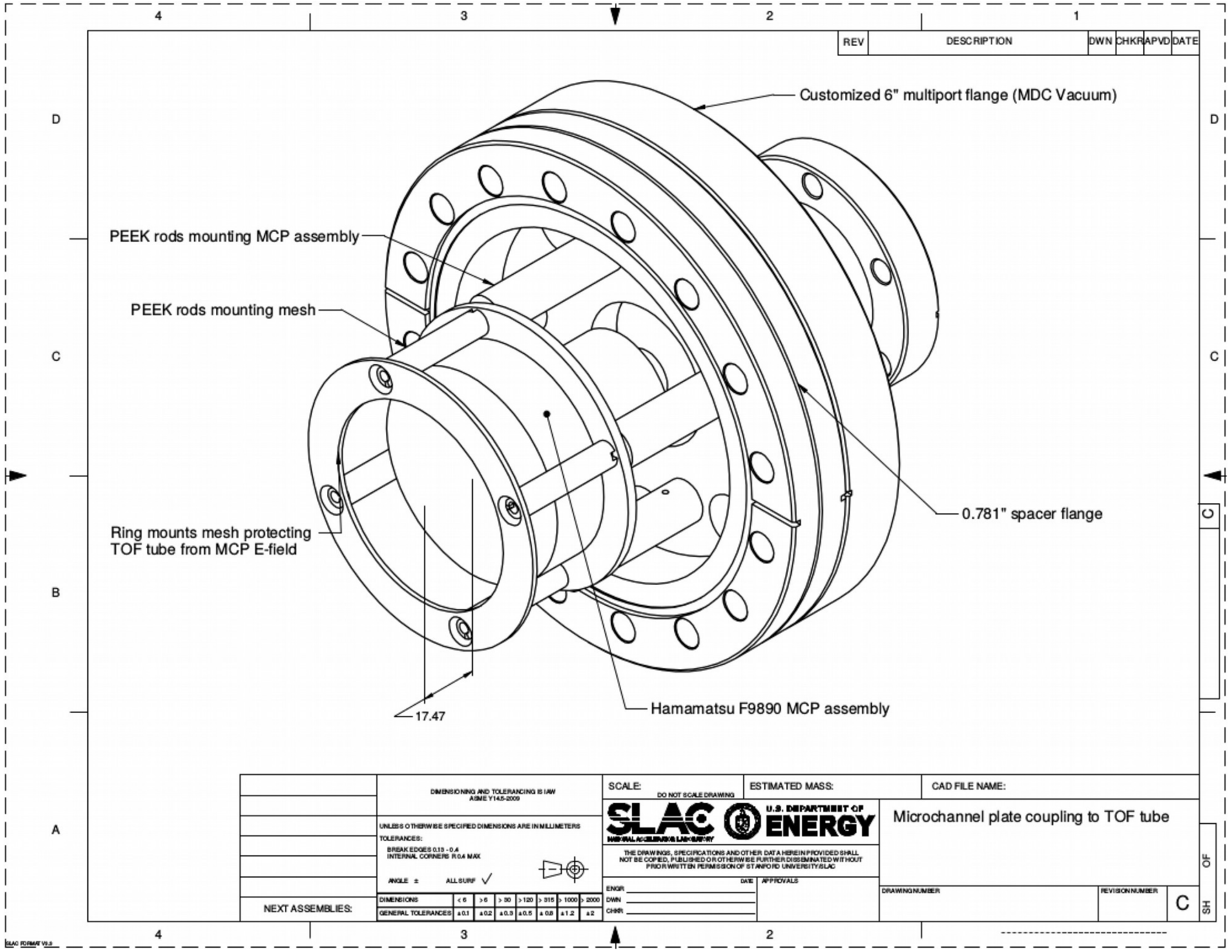
CookieBox Hutch Integration





Detector flange assembly

- Standard 6” UHV flange and feed throughs
- Custom parts in fabrication
- 1st of May arrival
- 40cm distance gives 3.5 10^{-3} collection / detector
- Could increase resolution by extending flight tube



Design drawing courtesy of Taran Driver

Engineering Coordination Schedule

Phase	Task / Milestone	Description	Start date	Planned finish date	Actual finish date	Dependency	Comment
Phase I – FWP	2	Finalize R&D TOF design	Feb-19	Jun-19			Need Design Eng
	4	Simulate reducing signal	Feb-19	Jun-19			Ongoing
	6	Iterate Simulation and Eng. Design of R&D TOFs	Apr-19	Jul-19			Ongoing
	8	Order 2 initial R&D TOFs	May-19	Aug-19			
	10	Order 6 R&D TOFs	Sep-19	Dec-19			
	12	Initial Digitizer arrival	Jan-19	May-19			
	14	Other three digitizers	May-19	Sept. 2019			
	16	Iterate Chamber Eng. Design	Jun-19	Aug-19			Need Design Eng
	18	Order initial R&D MCP (2)	May-19	Aug-19			
	20	Order full set of R&D MCPs (6)	Jul-19	Nov. 2019			
	M1	Prototype Chamber Final Design		Aug-19		16	PEC for XIP
	22	Order Prototype mu metal chamber	Sep-19	Jan-20		M1	Lead time = 3-6 months
	24	Assemble Prototype	Dec-19	Feb. 2020		M1, 22	need 4-6 weeks
	M2	(Adjust) Final Design TMO version Chamber Design and make FDR		Feb. 2020			XIP FDR
Phase II - XIP	28	Order Parts	Jan-20				
	30	Assemble	Jul-20				
	32	Test	Aug-20				
	34	Offline commissioning	Oct-20				
	M3	RFI					
	36	Install MRCOFFE in TMO	Dec-20				
	M4	TTO		Apr-21			
	M5	Project closeout		Sept-21			

Conclusions

- ~ ½ effort so far on ToF module design and simulation
  - "Known" parts ordered for May/June tests in PULSE EUV lab
  - Coordinating with L2SI to develop the final ToF and Chamber design by Sept-2019
- ~ ½ effort so far on matching detector electronics to pulse retrieval algorithm to support streaming analysis
  - Quintessential "firehose" data source but required for ultralow latency decision making
  - Design is informing also the data systems for LCLS-II
  - ML requirements are presenting the upgrade path for PCDS Digitizer specifications
- Very close cooperation with AD, L2SI, PCDS, PULSE, TID-AIR, and Stanford CS/EE