

# Hardware Reference Manual

## FMC134\* 4-Channel Analog-to-Digital Daughter Card

THE FM134 IS DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTIONS OF HAZARDOUS SUBSTANCE (ROHS) DIRECTIVE (2015/863) CURRENT REVISION.

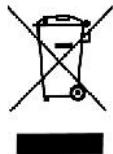
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## Document History

Revision	Date	Changes	Author	Peer Review	Quality Approval
r1.0	12/12/2017	Initial Release	CNS	RTM	JDS
r1.1	02/12/2018	Updated Main Characteristics Updated power Corrected table 3	CNS	RTM	JDS
r1.2	02/20/2018	Updated block diagram Updated photo	CNS	RTM	JDS
r1.3	08/09/2018	Updated operating temperature and convert to new Abaco formatting	CNS	PKO	PKO
r1.4	11/30/2018	Updated to include information for the high frequency variant. Removed LMX readback section.	CNS	ANE RTM	PKOhi

## Waste Electrical and Electronic Equipment (WEEE) Returns



Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

# About This Manual

## Conventions

### Notices

This manual may use the following types of notice:



#### WARNING

Warnings alert you to the risk of severe personal injury.



#### CAUTION

Cautions alert you to system danger or loss of data.



#### NOTE

Notes call attention to important features or instructions.



#### TIP

Tips give guidance on procedures that may be tackled in a number of ways.



#### LINK

[Links take you to other documents or websites.](#)

## Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a "D" subscript and binary numbers have a "b" subscript. The prefix "0x" shows a hexadecimal number, following the 'C' programming language convention. Thus:

$$\text{One dozen} = 12_{\text{D}} = 0x0C = 1100_{\text{b}}$$

The multipliers "k", "M" and "G" have their conventional scientific and engineering meanings of  $\times 10^3$ ,  $\times 10^6$  and  $\times 10^9$ , respectively, and can be used to define a transfer rate. The only exception to this is in the description of the size of memory areas, when "K", "M" and "G" mean  $\times 2^{10}$ ,  $\times 2^{20}$  and  $\times 2^{30}$  respectively.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

## Text

Signal names ending with a tilde ("\\") denote active low signals; all other signals are active high. "N" and "P" denote the low and high components of a differential signal respectively.

# Further Information

## Abaco Website

You can find information regarding Abaco products on the following website:



**LINK**

<https://www.abaco.com/products>

## Third-party Documents

- J ANSI/VITA 57d4-r1d0t-2016-Mar-17, FPGA Mezzanine Card Plus(FMC+) Draft Standard
- J ANSI/VITA 57.1-2010, FPGA Mezzanine Card (FMC) Standard



**LINK**

<https://www.vita.com/>

- J Datasheet ADC2DJ3200, Digital to Analog Converter
- J Datasheet LMK04832, PLL and Clock Generator
- J Datasheet LMX2581, RF Synthesizer with Integrated VCO



**LINK**

<https://www.ti.com>

- J JESD204B Specification, JEDEC Standard No. 204B.01



**LINK**

<https://www.jedec.org>

- J Datasheet AD7291, 8 - Channel I<sup>2</sup>C 12Bit SAR ADC with Temp Sensor
- J Datasheet HMC987LP5E, Low Noise 1:9 Fanout Buffer



**LINK**

<https://www.jedec.org>



**NOTE**

Technical literature describing components used on the FMC134 is available from the manufacturers' websites.

## Technical Support Contact Information

You can find technical assistance contact details on the website Support page.



LINK

<https://www.abaco.com/support>

Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

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[support@abaco.com](mailto:support@abaco.com)

## Returns

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LINK

<https://www.abaco.com/support>

Do not return products without first contacting the Abaco Repairs facility.

## EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

## Safety

This module presents no hazard to the user.

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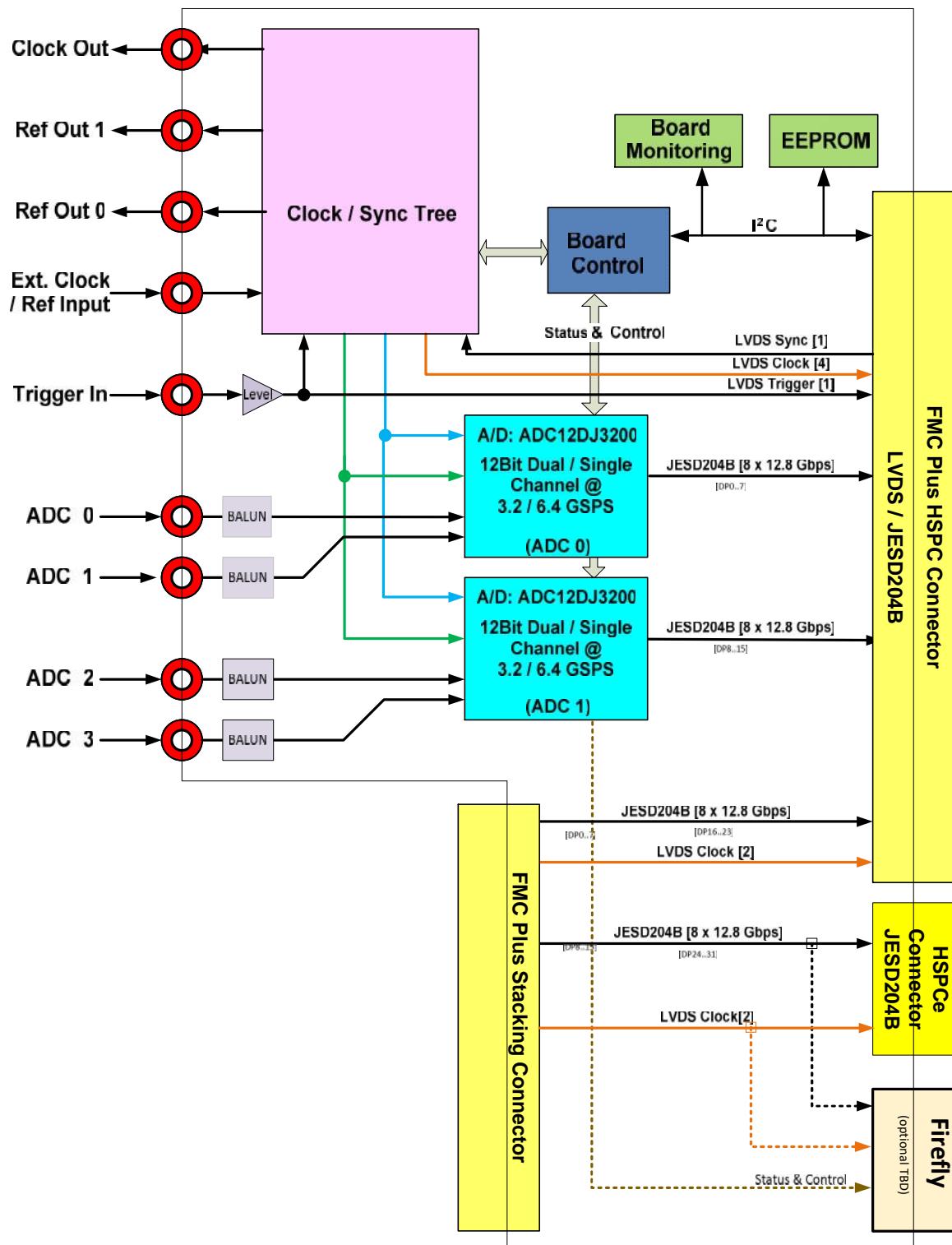
# 1 • General Description

The FMC134 is a four channel Analog-to-Digital FMC daughter card based on the ADC12DJ3200, dual channel 12-bit 3.2 GSPS ADC from Texas Instruments. The two ADCs support a maximum lane rate of 12.8 GBPS providing four 12-bit channels at a sample rate of 3.2 GSPS, or two 12-bit channel at 6.4 GSPS. Clocking can be from an internal source (optionally locked to an external reference) or an externally supplied sample clock. The board includes a trigger input for customized sampling control. The board is specifically designed to allow a second FMC134 to be stacked on its carrier connector allowing synchronous 8-channel operation. The FMC134 daughter card is mechanically and electrically compliant to the draft FMC+ standard (VITA\_v57d4-r1d0t-2016-Mar-17). Onboard peripherals can be programmed through the I<sup>2</sup>C serial communication channel. Furthermore, the card is equipped with power supply and temperature monitoring and offers several power-down modes to switch off unused functions.

## 1.1 Installation and Handling Instructions

- ]) Prevent electrostatic discharges by observing ESD precautions when handling the card.
- ]) Do not flex the card and do not exceed the maximum torque specification on the coax connectors.
- ]) The FMC134 daughter card must be installed on a carrier card compliant to the FMC+ standard.
- ]) The FMC carrier card must support the HSPC FMC+ connector (560-pins)
- ]) The carrier card can support VADJ/VIO\_B voltage range of 1.65 V to 3.3 V, but typically VADJ will be 1.8 V or 2.5 V for LVDS operation.

Figure 1-1 FMC134 Block Diagram



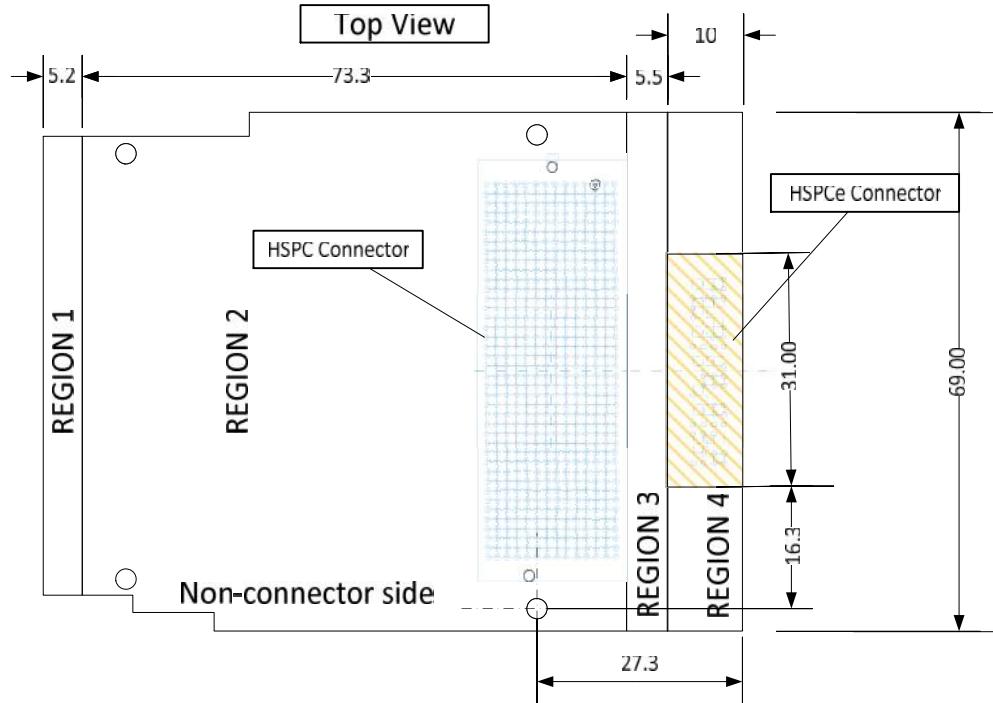
# 2 • Design

## 2.1 Physical Specifications

### 2.1.1 Board Dimensions

The FMC134 card complies with the draft FMC+ standard known as VITA\_v57d4-r1d0t-2016-Mar-17. The card is a single width conduction cooled mezzanine module (with region 1 and front panel I/O). The front bezel contains 9 coaxial I/O signals. The stacking height is 10 mm; the maximum component height on the bottom layer is 1.3 mm. The general outline of the board is shown below.

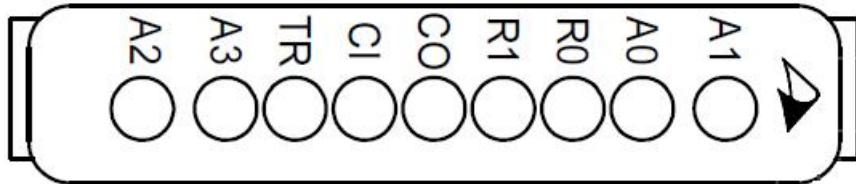
Figure 2-1 FMC134 Dimensions



## 2.1.2 Front Panel Connectors

The front panel of the FMC134 contains 9 Connectors as shown below.

Figure 2-2 Bezel



The text on the bezel is expanded as follows:

**A2** Analog input #2

**A3** Analog input #3

**TR** Trigger input

**CI** Clock input, ADC sample clock, or external reference

**CO** Clock output, ADC sample clock

**R1** 100 MHz reference output #1

**R0** 100 MHz reference output #0

**A0** Analog input #0

**A1** Analog input #1

## 2.2 Main Characteristics

Table 2-1 FMC134 Daughter Card Main Characteristics

FMC134 Main Characteristics	
Analog Inputs (A0...A3)	
<b>Number of channels</b>	4
<b>Channel resolution</b>	12-bit
<b>Full scale input amplitude (default variant)</b>	+6 dBm (+/- .5 dB across frequency) / ~1.3Vpp AC Coupled into 50 Ω Typ. ADFS = 0xFFFF (+3.8 dBm ADFS = 0xA000) (ADC FS can be adjusted from ~ +6 to +0 dBm)
<b>Full scale input amplitude (high frequency variant)</b>	+6.6 dBm Typ. @3910 MHz ADFS=0xFFFF (ADC FS can be adjusted from ~ +6.6 to +.6 dBm) (+/- 1dB across frequency see response in <a href="#">Figure 2-12</a> )
<b>Input impedance</b>	50 Ω
<b>Analog input bandwidth (default variant)</b>	~5 to 4000 MHz Amplitudes referenced to a 100 MHz input signal at -2 dBFS
<b>Analog 3 dB input bandwidth (high frequency variant)</b>	1700 MHz to 6700MHz
<b>SFDR (default variant)</b>	Typical values at -1 dBFS input - ADC Full scale set to +6 dBm @25 MHz: 58 dBFS Typ. @101.39 MHz: 58 dBFS Typ. @450 MHz: 58 dBFS Typ. @849 MHz: 57 dBFS Typ. @1300 MHz: 56 dBFS Typ. @3950 MHz: 52 dBFS Typ.
<b>SFDR (high frequency variant)</b>	Typical values at -1 dBFS input - ADC Full scale set to +6.6 dBm @1700MHz 58 dBFS Typ. @4200MHz 54 dBFS Typ. @6700MHz 49 dBFS Typ.
<b>Sampling frequency range</b>	0.8 to 3.2 GSPS dual channel 6.4 GSPS interleaved
<b>Data width</b>	16 JESD204B lanes, 8-lanes per ADC, 4-lanes per channel, max lane rate 12.8 GBPS
<b>Data format</b>	Offset binary or 2's complement(default)
External Reference Input (CI)	
<b>Frequency range</b>	10 to 900 MHz
<b>Input amplitude</b>	-10 to +9.1dBm / ~0.2 to 1.8Vp-p AC coupled into 50 Ω Recommended input: +9 dBm / 1.8Vp-p. Phase noise improves with increasing input level
External Clock Input (CI)	
<b>Frequency range</b>	800 to 3200 MHz

FMC134 Main Characteristics	
<b>Input amplitude</b>	+3 to +15 dBm / ~0.9 to 3.6Vp-p AC coupled into 50 Ω Recommended input: +10 dBm / 2.0Vp-p (phase noise improves with increasing input level)
External Trigger / Timestamp Input (TI)	
<b>Trigger input signal</b>	LVPECL compatible input, 1.8 V threshold voltage, DC coupled into 50 Ω Optional LVTLL/LVCMSO compatible, 1.25 V Threshold voltage, DC coupled into 2.5kΩ, Optional AC coupling
<b>Input impedance</b>	50 Ω LVPECL compatible, (2.5kΩ DC coupled / AC coupled option available)
<b>Trigger frequency range</b>	Single ended 50 Ω LVPECL Levels 2 GHz min, 2.7GHz Typ. LVTTL & LVCMSO limited by source
<b>Time-stamp frequency range</b>	Single ended 50 Ω LVPECL Levels 3.2 GHz min. LVTTL & LVCMSO limited by source
Internal 100MHz Reference Output (R0, R1)	
<b>Output level</b>	>0dBm, AC coupled into 50Ω (when enabled)

## 2.3 Electrical Specifications

Each ADC device uses JESD204B subclass 1 coded differential pairs connected to the GBT pins on the FMC+ connector to transfer sample data. There are normally four lanes available per ADC channel. Control signals operate in LVCMSO/LVDS mode. A VADJ range of 1.65 V to 3.3 V is supported. The voltage on the VIO\_B pins will follow the voltage on VADJ. All CLK pins are LVDS per the FMC standard.

### 2.3.1 EEPROM

The FMC134 card carries a 2-kbit EEPROM (M24C02-WDW) which is accessible (read only) from the carrier card through the I2C bus. The EEPROM is powered by 3P3VAUX. The standby current is only 0.01 μA when SCL and SDA are kept at 3P3VAUX level

### 2.3.2 FMC Mezzanine Connector

Both the recommendations from AV57.4 Table 14 and the FMC134 pin definitions (for stacked operation), have been considered. The FMC+ HSPC connector is required for operation of the FMC134.

- ▀ The JESD204B ADC data pairs are mapped to DP [0...15]M2C.
- ▀ The reference clocks for the gigabit lanes are mapped to GBTCLK [0...3]M2C
- ▀ The reference clock for the FPGA logic is mapped to CLK0\_M2C.
- ▀ The SYSREF clock for the FPGA logic is mapped to CLK1\_M2C.

- | Other signals are mapped to LA bank starting at index 0.
- | The signals are routed such that board with a standard FMC HPC connector will support a 2 channel (Ch0, Ch1) version of the product.

Table 2-2 HSPC Signal Utilization

# LVDS Clock Pairs	# LVDS Data Pairs	#GBT Clock Pairs	#GBT Data Pairs M2C	#GBT Data Pairs C2M
CLK0 – LVDS Ref CLOCK	1			
CLK1 – LVDS SYSREF	1			
CLK2 – n/c				
CLK3 – n/c				
GBTCLK0 – REF CLK		1		
GBTCLK1 – REF CLK		1		
GBTCLK2 – REF CLK		1		
GBTCLK3 – REF CLK		1		
Trigger to FPGA	1			
Sync from FPGA to Trig Mux	1			
ADC-0 NCO	2			
ADC-1-NCO	2			
ADC-0 Over-range	2			
ADC-1 Over-range	2			
ADC0_SYNCSE_1P9V_L	0.5			
ADC1_SYNCSE_1P9V_L	0.5			
ADC0_CALSTAT_1P9V	0.5			
ADC0_CALSTAT_1P9V	0.5			
LMK_SYNC_SYSREF_REQ	0.5			
Firefly Interrupt	0.5			
CPLD CTRL0-CTRL3	2			
JESD204B lanes ADCA			8	
JESD204B lanes ADCB			8	
# Total Pairs	17	4	16	0

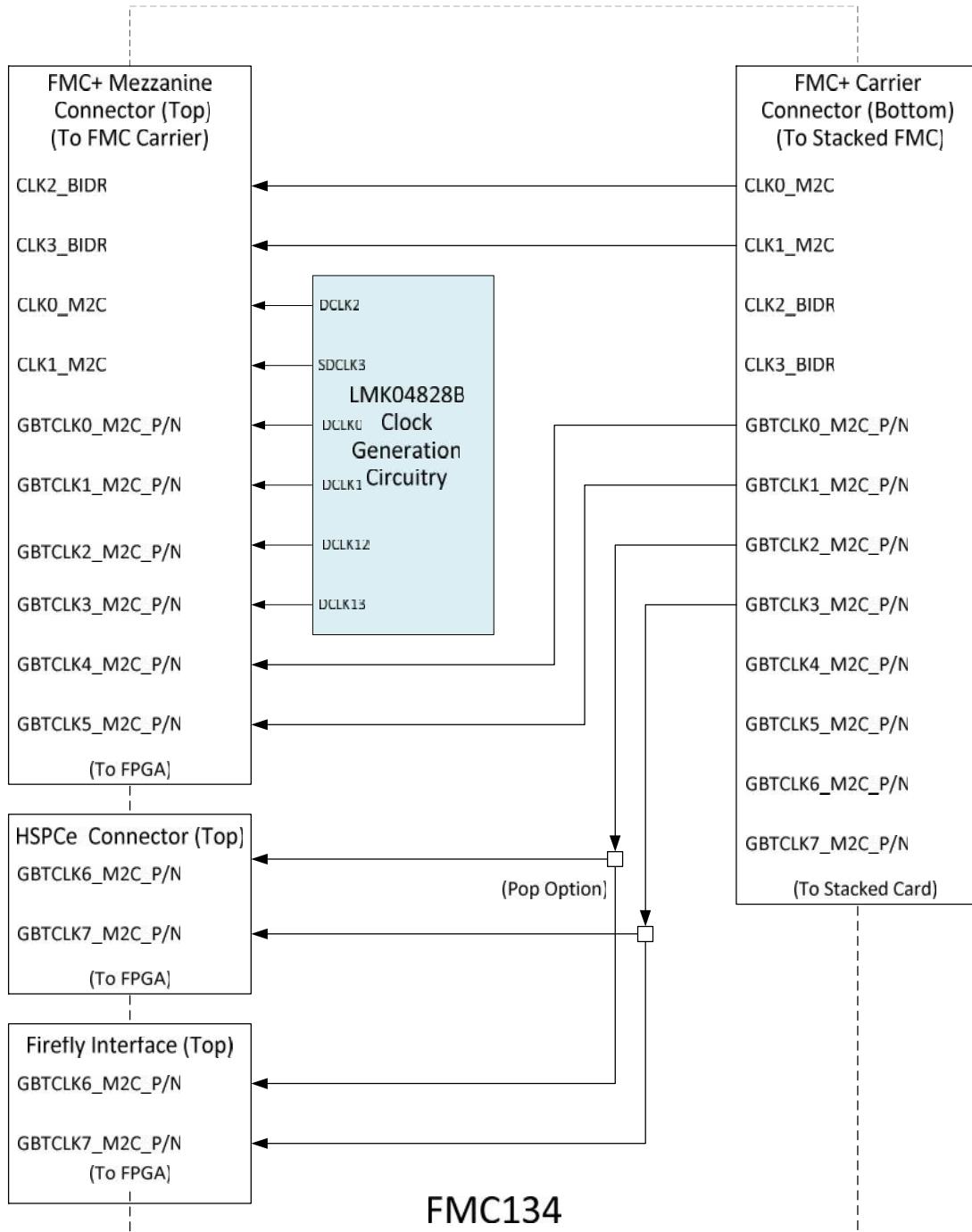
### 2.3.3 FMC Carrier Connector

All FMC pins not used by the FMC134 will be passed through to the carrier connector, to allow stacking of a second FMC card, for example for stacking a second FMC134. To prevent I<sup>2</sup>C bus conflicts, the global address signals GA0 and GA1 are read by the CPLD and a translated version is presented to the carrier connector. To allow stacked operation with a second FMC134, certain signals are remapped to the stacked carrier connector as described in subsequent sections.

### 2.3.4 Clock Signal Mapping

The FMC134 uses CLK0, CLK1, and GBTCLK0 through GBTCLK3, additionally, to support a second FMC134 in a synchronous stacked 8-channel configuration, CLK2\_BIDIR, CLK3\_BIDIR, and GBTCLK4 through GBTCLK7 are re-mapped to the carrier connector on the bottom of the board as shown below.

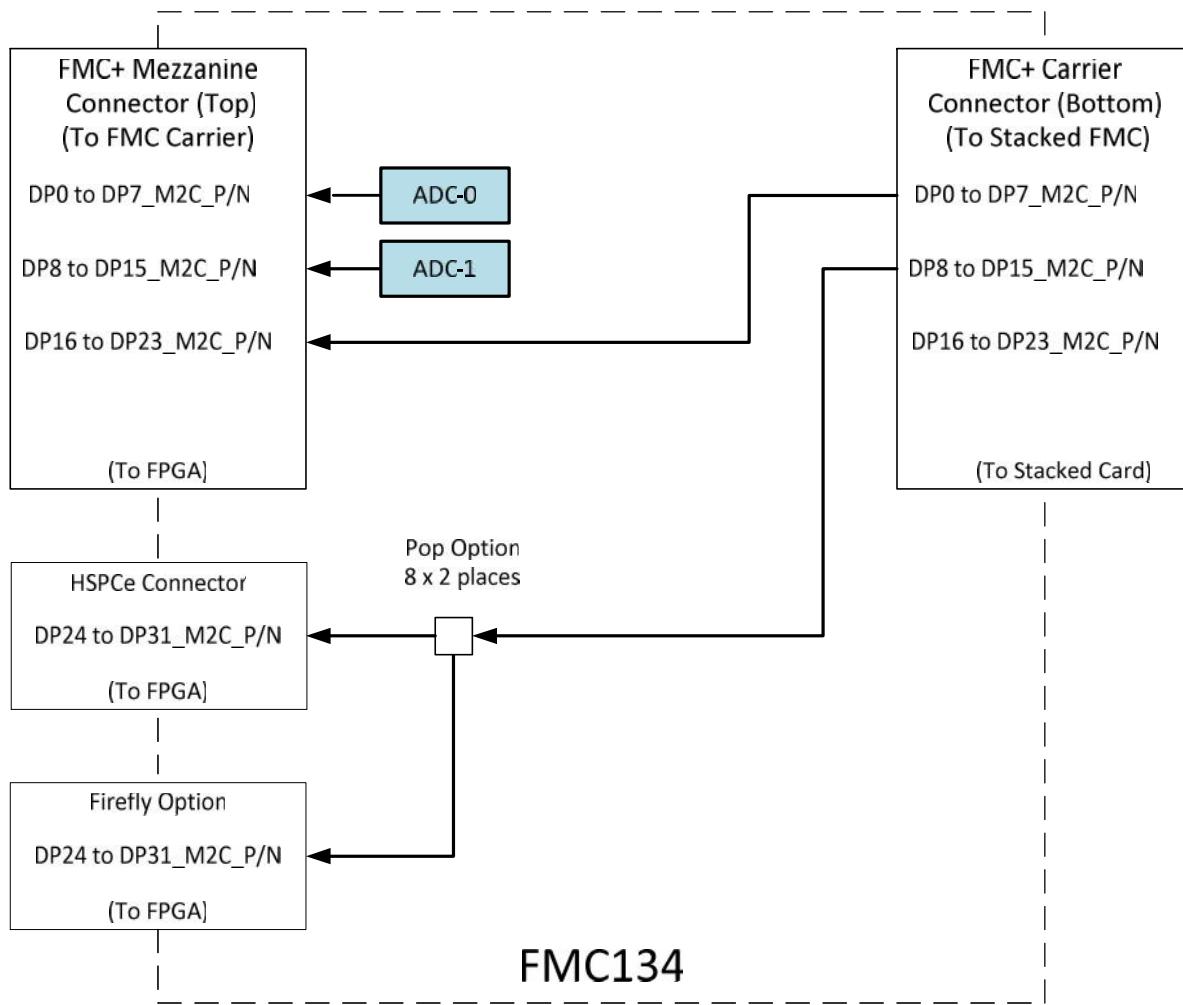
Figure 2-3 Clock Signal Mapping



### 2.3.5 M2C GBT Data Pair Mapping

The FMC134 uses DP0...DP7 for ADC-A and DP8...DP15 for ADC-B. To support a stacked FMC134 in an 8-channel synchronous configuration, DP16...DP23 are mapped to carrier connector pins DP0...DP7 for ADC-A and DP23...DP31 from the HSPCe or the optional Firefly connector to support ADC-B as shown below.

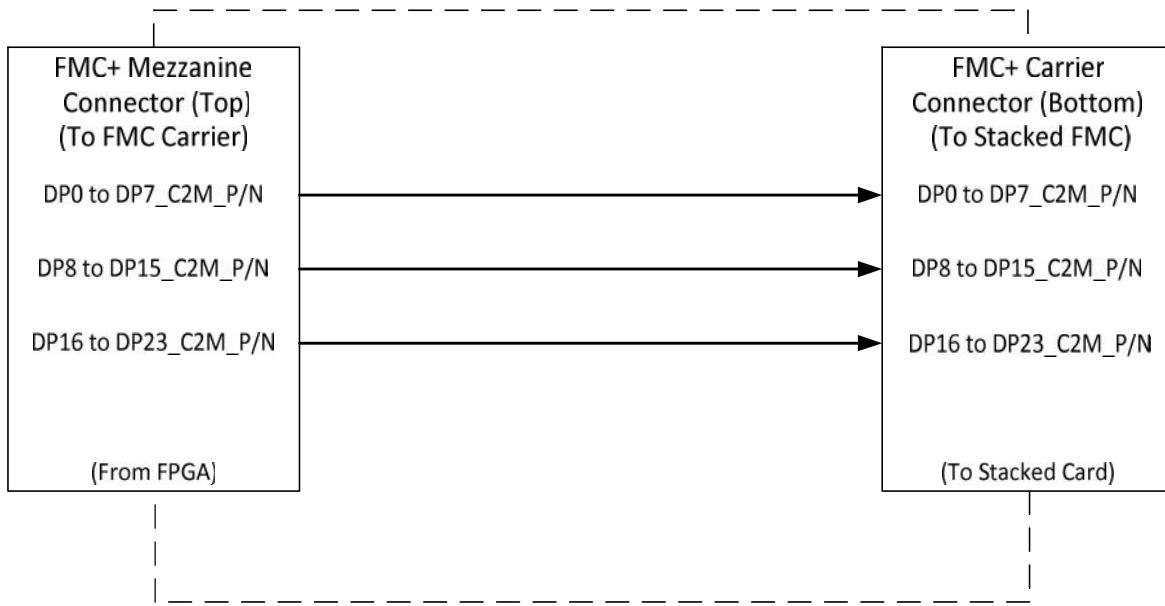
Figure 2-4 M2C GBT Data Pair Mapping



### 2.3.6 C2M GBT Data Pair Mapping

To support a DAC JESD-204B DAC card, the FMC134 routes the first 24 C2M GBT lanes (DP0... DP23...) from the HSPC mezzanine connector to the carrier connector. The signal routing is shown below.

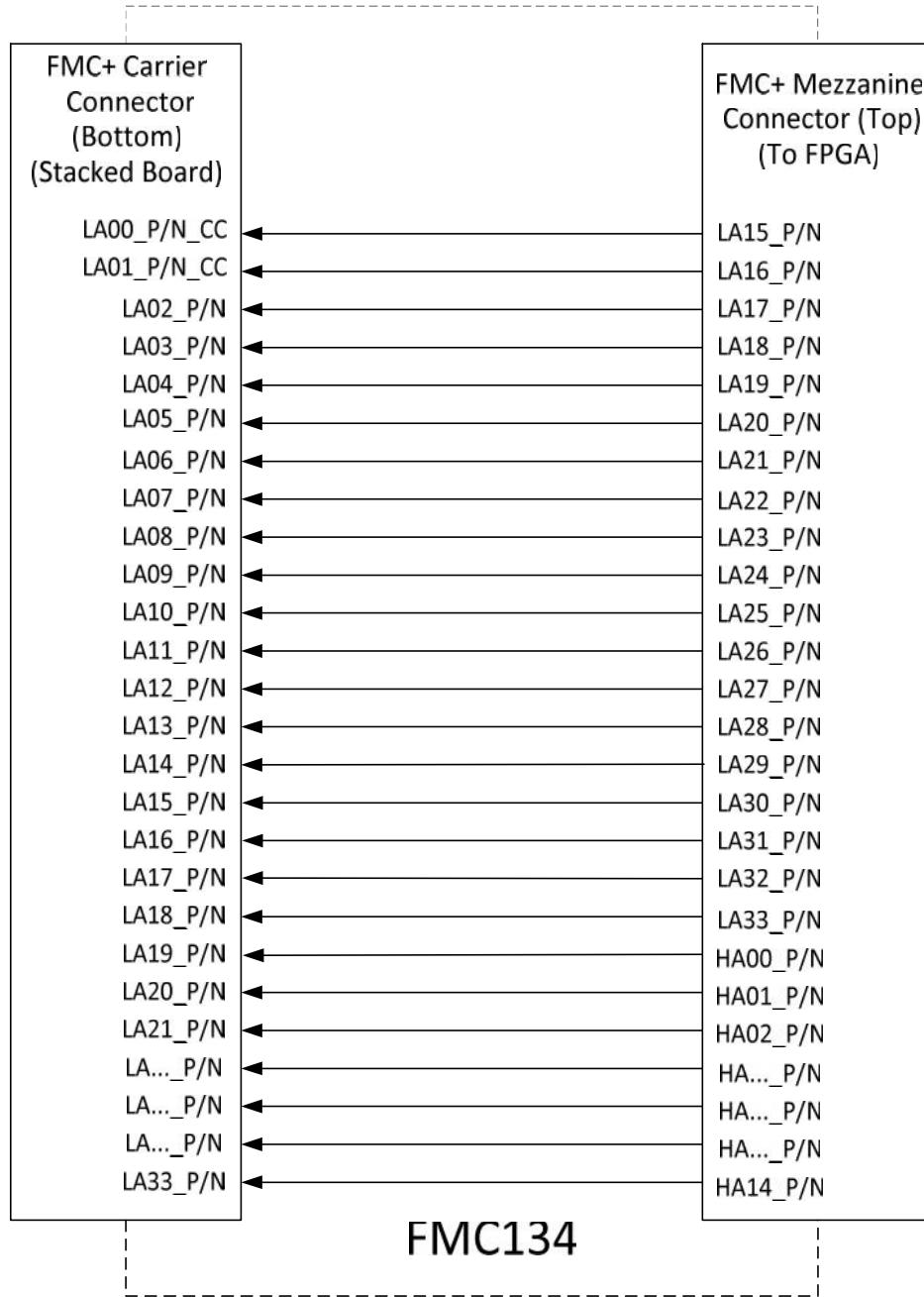
Figure 2-5 FMC134 C2M GBT Lane Mapping



### 2.3.7 LVDS Signal Re-Mapping for Stacked Operation

The FMC134 uses LVDS pairs LA00 through LA14, to support stacked operation, mezzanine LVDS signals LA15\_P/N through LA33\_P/N, and HA00 through HA14 are remapped to the carrier connector starting at LA00, as shown below.

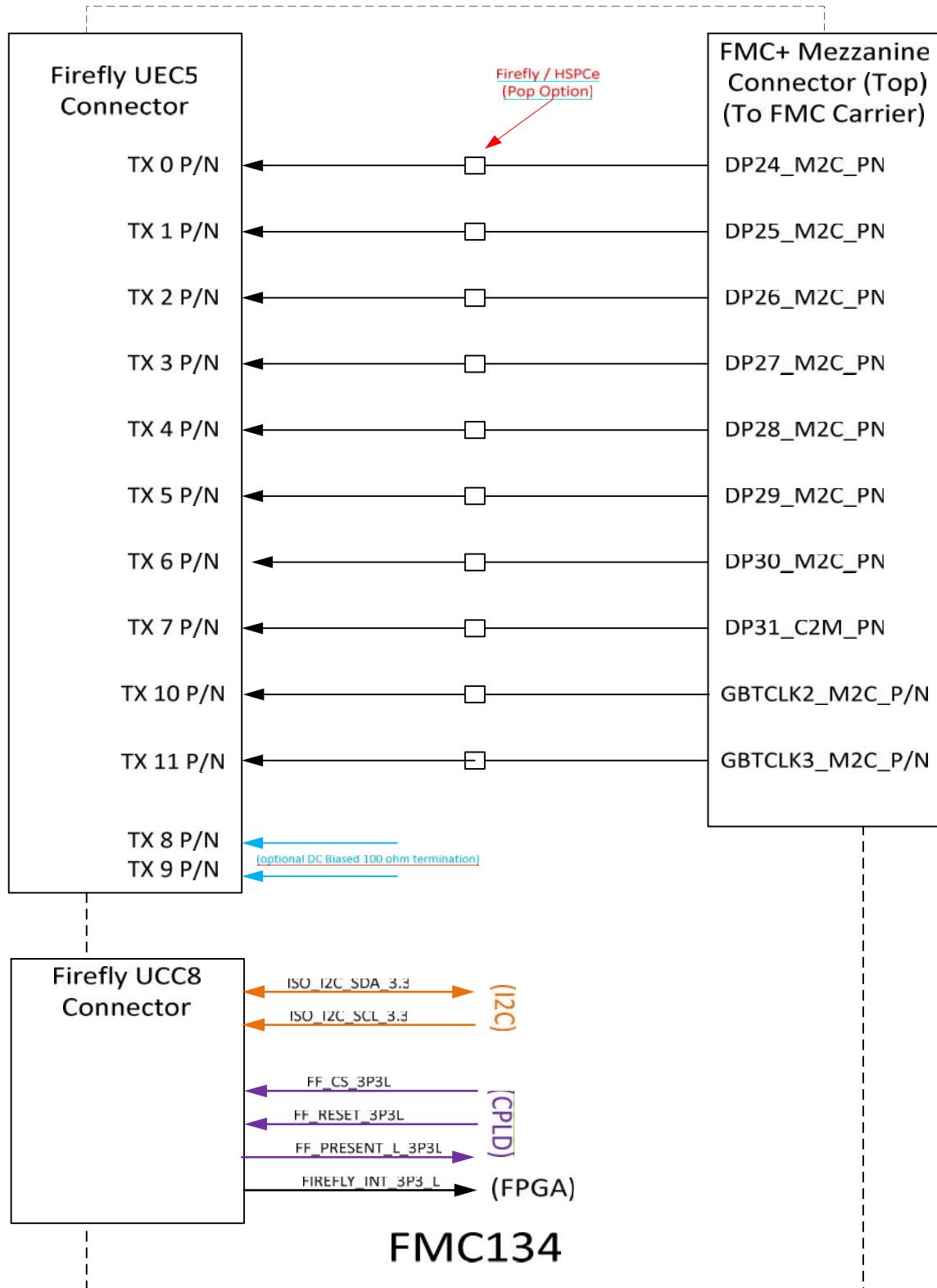
Figure 2-6 LVDS Signal Re-Mapping



### 2.3.8 Firefly Interface Signal Mapping

The optional firefly interface is available via pop options, installing this option provides a connection path for GBT lanes DP24 through DP31 to ADC B in a stacked configuration. The configuration is shown below.

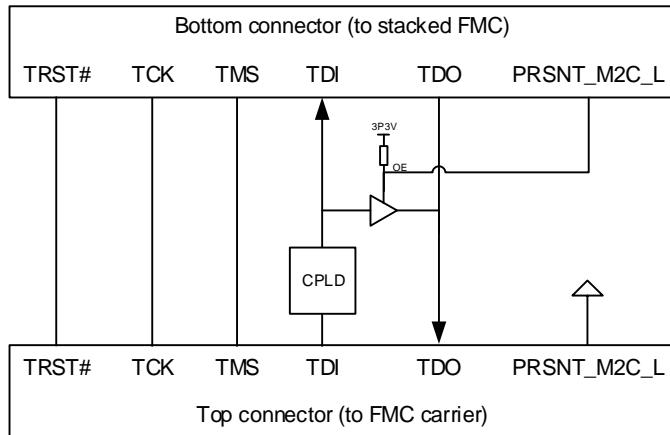
Figure 2-7 Firefly Interface Signal Routing



### 2.3.9 FMC JTAG Chain

In a stacked environment, the TDI pin will be decoupled from the TDO pin by the PRST\_M2C\_L signal coming from the bottom connector. TRST#, TCK, TMS, TDI and TDO are directly connected between top to bottom connector on the FMC134.

Figure 2-8 JTAG Connection



## 2.4 Analog Inputs

### 2.4.1 AC Coupling

The FMC134 uses transformer / balun coupling for single-ended to differential conversion. The analog input is AC-coupled at the connector to limit DC biasing of the transformer.

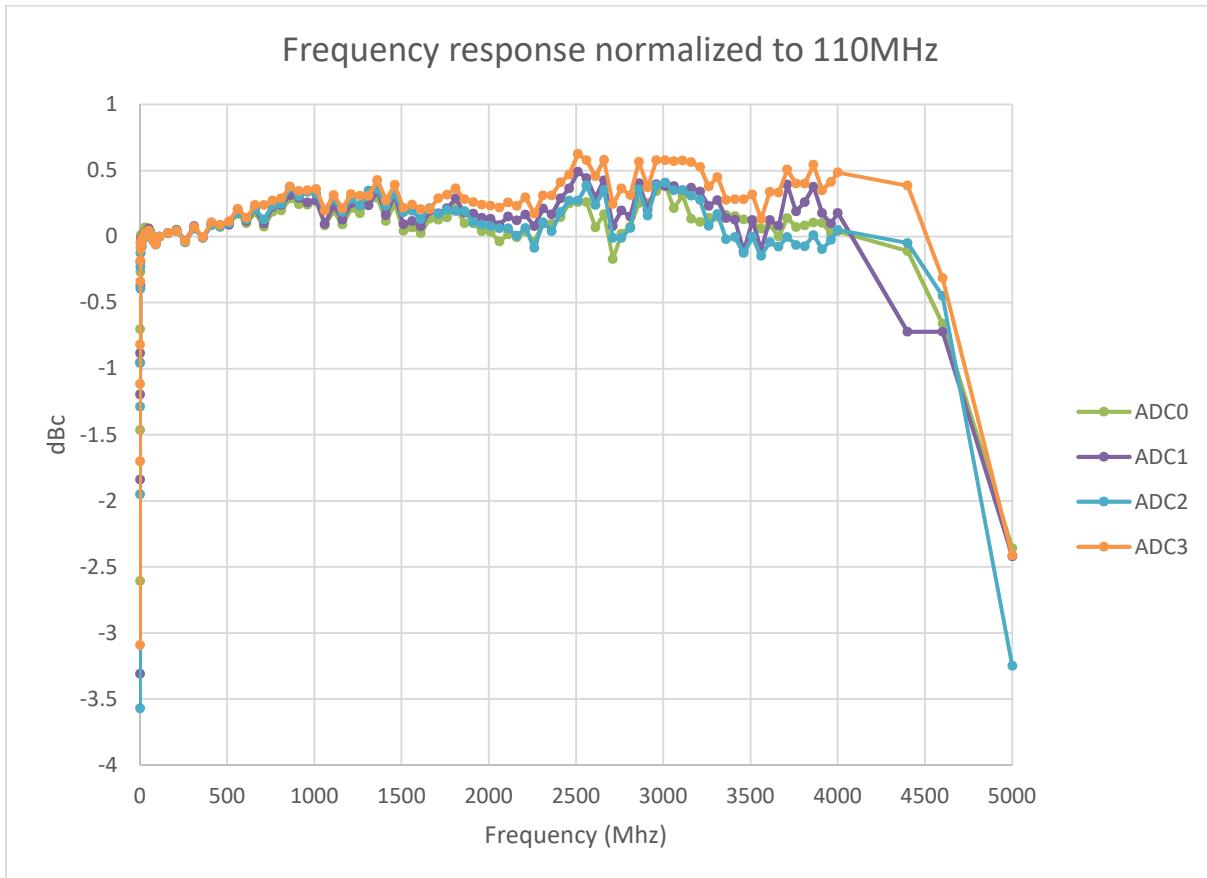
### 2.4.2 Full Scale Adjustment

Input full-scale voltage adjustment is available by adjusting the FS\_RANGE\_A and FS\_RANGE registers in the ADCs. The default value is 0xA000 which provides a nominal full scale of +3.8 dBm. A value of 0xFFFF is used in Fmc134APP reference software, which results in a higher SNR and decreased SFDR. Refer to section 7.3.1.2 (Full-Scale Voltage Adjustment) of the TI ADC12DJ3200 datasheet for details.

### 2.4.3 Typical Frequency Response (Default Variant)

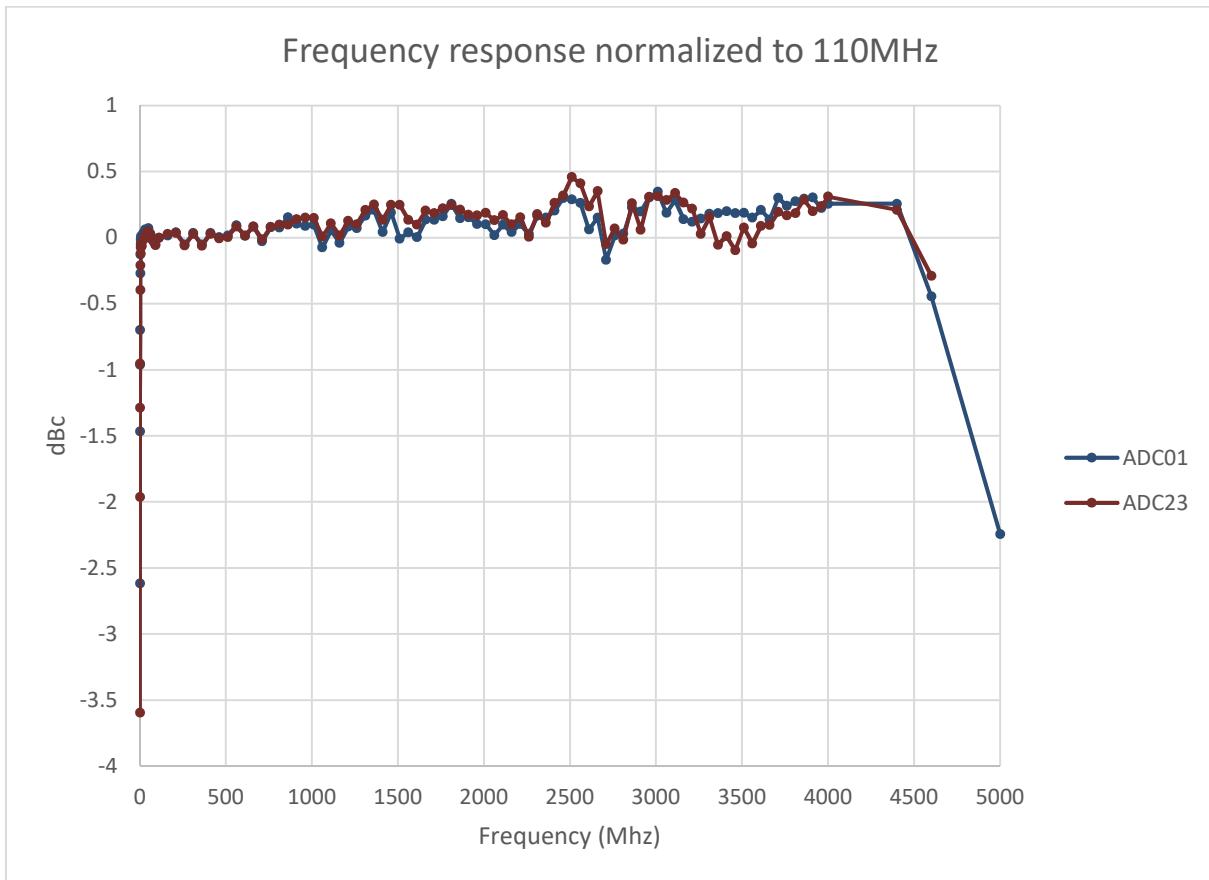
The typical input frequency responses of Channels 0-3 of the FMC134 are shown below.

Figure 2-9 Frequency Response Channels 0-3



The typical input frequency responses of Channels 01 and 23 of the FMC134 are shown below.

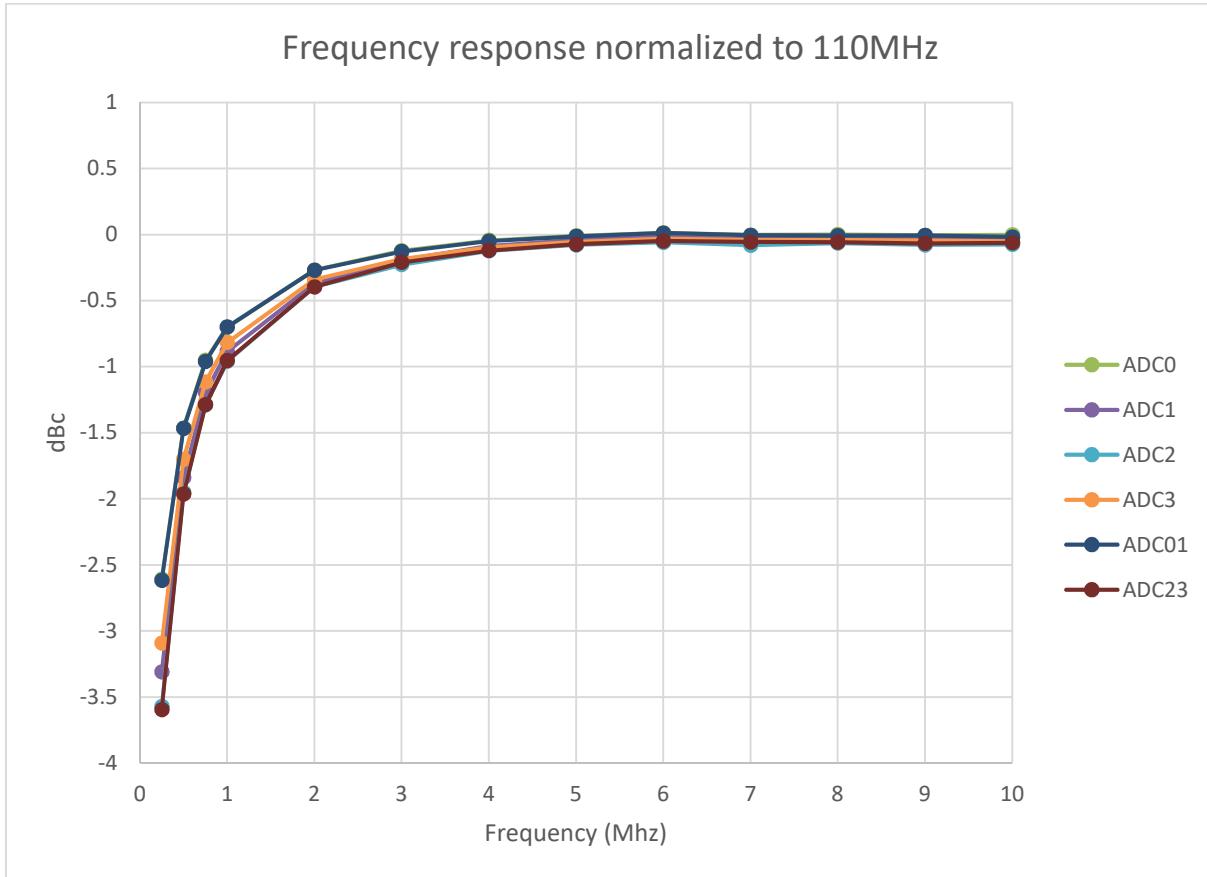
Figure 2-10 Frequency Response Channels 01 And 23



#### 2.4.4 Low Frequency Response (Default Variant)

The typical Low frequency input frequency responses of all channels of the FMC134 are shown below.

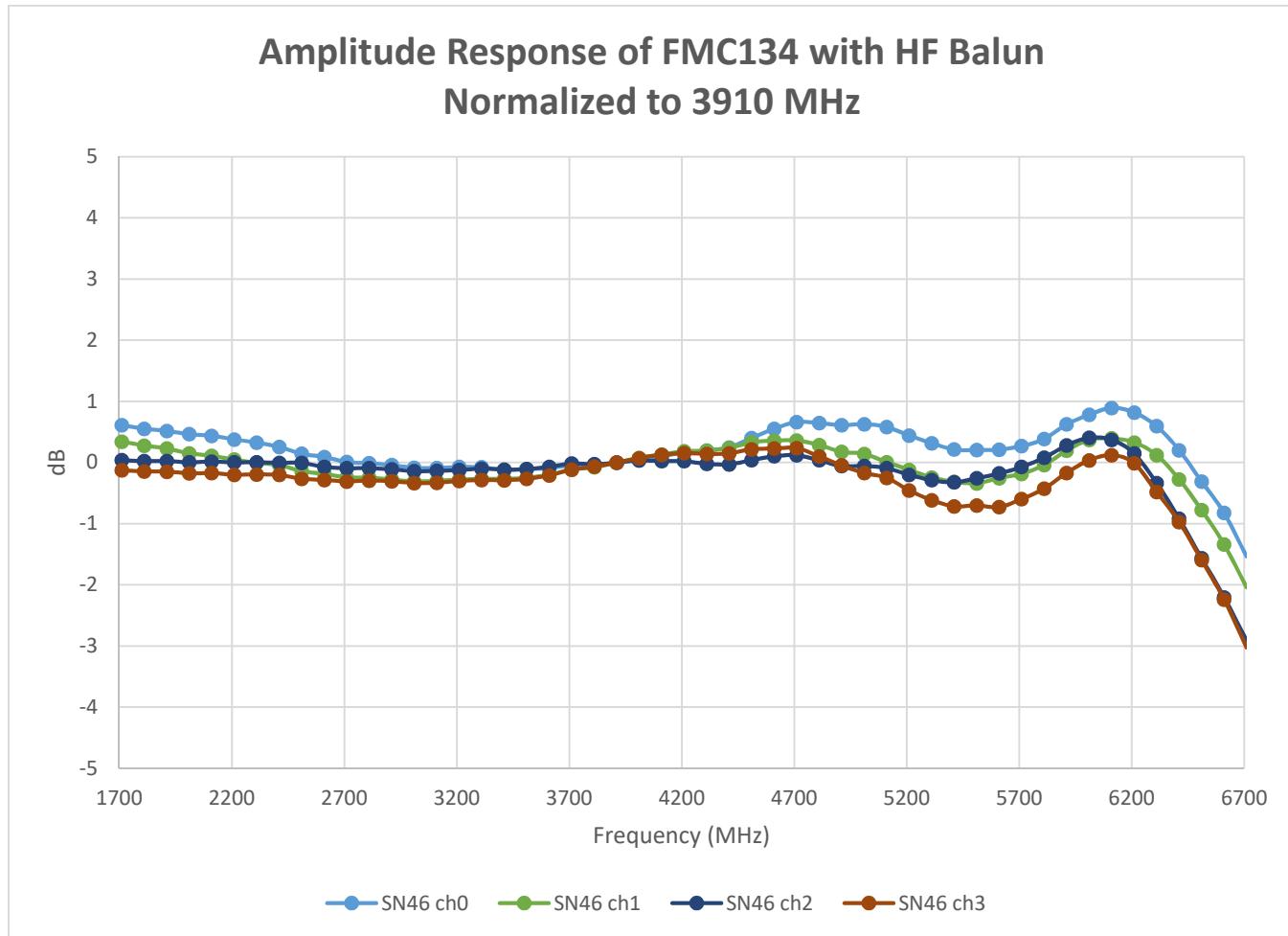
Figure 2-11 Low Frequency Response



## 2.4.5 High Frequency Variant Response

The typical response of the high frequency variant is shown below.

Figure 2-12 High Frequency Variant Response

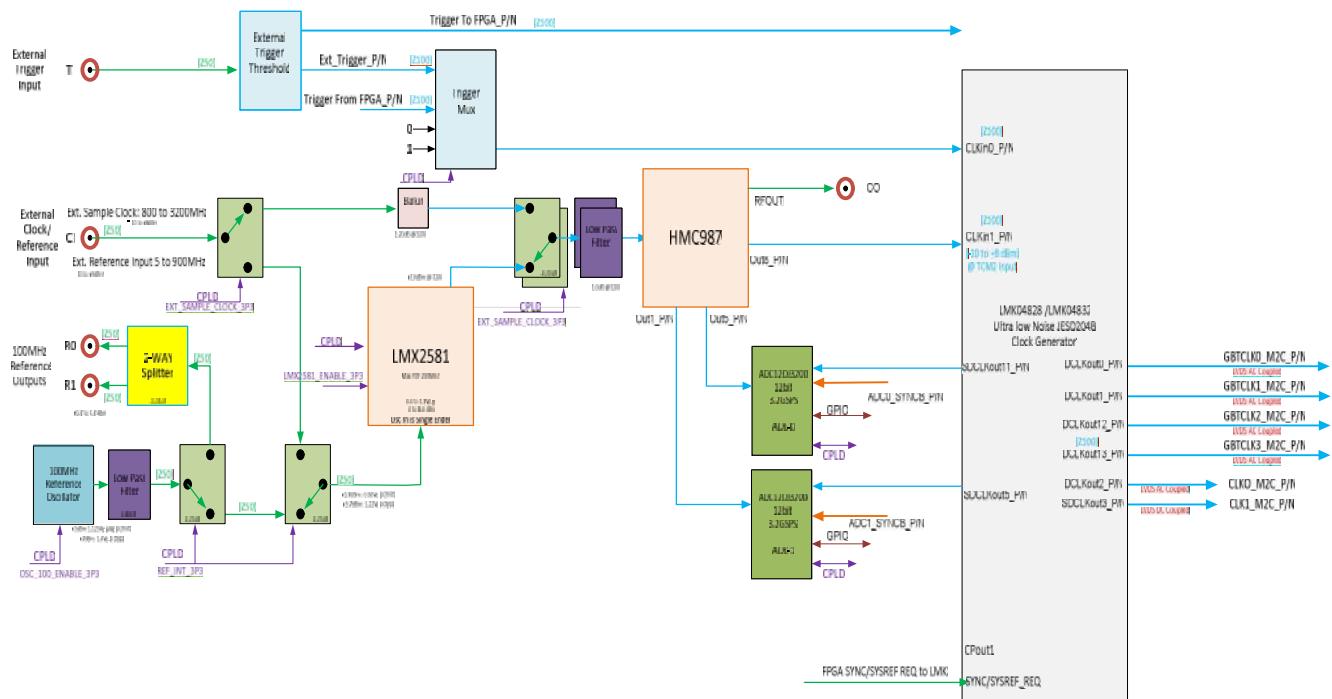


## 2.5 Clock Tree

### 2.5.1 Architecture

The FMC134 card offers a versatile clocking architecture that combines flexibility and high performance. The user may choose to use an external sampling clock or the internal N /fractional N PLL synthesizer, as well as an internal or external reference clock.

Figure 2-13 Clock Tree Architecture



The sample clock is generated by a TI LMX2581PLL synthesizer. Then distributed by an Analog Devices HMC987 clock buffer. A TI LMK04832 is used to generate the clocks for JESD204B synchronization. The following modes are possible:

- 1: LMX – LMK clock tree using internal 100 MHz reference oscillator:

The LMX2581 PLL is locked to the internal 100 MHz reference oscillator, its output drives the HMC987 clock buffer which distributes the sample clock to the converters and the CLK1 input to the LMK04832. The LMK04832 divides the sample clock to generate the SYSREF signals and distributes them to the ADCs and FPGA. This configuration can also be used in a stacked mode described in [Section 2.5.7](#).

- 2: LMX - clock tree locked to an external reference oscillator

The LMX2581 PLL is locked to an external 100 MHz reference oscillator, its output drives the HMC987 clock buffer which distributes the sample clock to the converters and the CLK1 input to the LMK04832. The LMK04832 divides the sample clock to

generate the SYSREF signals and distributes them to the ADCs and FPGA. This configuration can also be used in a stacked mode described in [Section 2.5.7](#). The FMC134 hardware will support an external reference input of ~ 5 MHz to ~1400 MHz with appropriate programming of the LMX2581.

### 3: External Sample Clock Distribution

The LMX2581 PLL and the 100 MHz internal reference oscillator are powered down. The external clock input drives the HMC987 clock buffer which distributes the sample clock to the converters and the CLK1 input to the LMK04832. The LMK04832 divides the sample clock to generate the SYSREF signals and distributes them to the ADCs and FPGA.

In any of the above cases, the master clock signal, whether generated by the LMX2581 PLL synthesizer or an external clock source, feeds the master SYSREF divider and each of the five DCLK outputs and three SCLK outputs through independent dividers.

#### 2.5.2 100 MHz reference Oscillator

The FMC134 uses an ultra-low phase noise sine wave oscillator as a reference. When not used, this oscillator should be powered down via the OSC100\_EN bit in the CPLD to prevent any potential interference.

#### 2.5.3 LMX2581 PLL Design

The FMC134 uses a TI LMX2581 high performance, wideband n / frac-n PLL to generate the sample clock. The circuit is powered from its own dedicated low noise LDO to minimize supply induced noise. Wide bandwidth low loss RF switches controlled by the CPLD are used to configure the circuit.

#### 2.5.4 LMX2581 Clock Ranges

The LMX2581 PLL synthesizer can output a sample clock anywhere in the ADCs range of 800 to 3200MHz. The best noise performance will occur when using directly using the 100 MHz as the phase detector reference signal. Lower PFDs will have the greatest impact on higher frequency input signals.

#### 2.5.5 LMX2581 PLL Loop Filter Design

The default loop filter for PLL1 is optimized for a phase detector frequency of 100 MHz, a loop filter bandwidth of 237 kHz, and a phase margin of 48°. This gives an estimated jitter of 95 fs in a 1 Hz to 3200 MHz bandwidth, for comparison this is 89.7 fs in a 12 kHz to 40 MHz bandwidth. Using the doubler on the reference input will drop the jitter down to about 82 fs, however this may place a half clock ambiguity in a multi-board system.



##### NOTE

Changing the phase detector frequency will also change the performance of the loop filter, [Table 2-3](#) shows the effect of the PFD on bandwidth and phase margin.

Table 2-3 Effect of PDF on LMX Loop Filter Parameters

PDF Frequency	Bandwidth (kHz)	Phase Margin (Deg.)	Phase Noise (fs)
200 MHz	411.7	45.6	82
100 MHz	237.1	48	95
50 MHz	139.4	42.5	128
10 MHz	51.1	22.4	315
1 MHz	15.4	7.3	1628

As would be expected, this shows that PLL performance is only optimized for a single PFD

## 2.5.6 Single FMC134 Using Internal 100 MHz Reference Oscillator

The FMC134 contains a low-noise 100 MHz reference oscillator for the sample clock PLL that drives the clock tree, the default configuration is shown below.

- ↳ OSC100\_EN\_3P3 = 1
- ↳ REF\_INT\_3P3 = 1
- ↳ LMX2581\_ENABLE\_3P3 = 1
- ↳ EXT\_SAMPLE\_CLK\_3P3 = 0

## 2.5.7 Stacked Operation 100 MHz Reference Oscillator Circuitry

In a stacked configuration, the FMC134 can be configured to output its 100 MHz reference signal to a stacked card. To maintain phase matching, the signal path must be equal between both cards. The output of the reference oscillator is passed through a 3-dB splitter. The output of the splitter drives two identical front panel connectors, Ref-0 and Ref-1 (R0 and R1). The input of the low-pass filter is now driven through front panel connector clock / reference input (Cl). The R0 output should be used to drive the Cl input of the board closest to the carrier card, The R1 output should be used to drive the Cl input of the stacked card.

The 100 MHz reference oscillator should be turned off on the stacked card.



### NOTES

OSC100\_EN\_3P3 = 1 onboard providing reference, 0 on Stacked board.

REF\_INT\_3P3 = 0

LMX2581\_ENABLE\_3P3 = 1

EXT\_SAMPLE\_CLK\_3P3 = 1

The coax cables must be the same length and type for this function to perform properly.

## 2.5.8 External Reference Operation

The FMC134 can be configured to use an external reference to accomplish this the following CPLD bits must be programmed.

- J OSC100\_EN\_3P3 = 0
- J REF\_INT\_3P3 = 0
- J LMX2581\_ENABLE\_3P3 = 1
- J EXT\_SAMPLE\_CLK\_3P3 = 1
- J When using this mode in a stacked configuration the external reference cable type and lengths should be tightly matched.

## 2.5.9 External Sample Clock Input

The clock input, labelled CI on the front panel, is used to provide an external sample clock to the FMC134. The input from this jack is routed through an RF switch to the HMC987 which then distributes it to the CLKin1 pins on the LMK04832 and to the ADCs.



### NOTE

To minimize noise and interference the following the following bits must be configured.

- J OSC100\_EN\_3P3 = 0
- J REF\_INT\_3P3 = 0
- J LMX2581\_ENABLE\_3P3 = 0
- J EXT\_SAMPLE\_CLK\_3P3 = 0

## 2.6 Multi-Channel Synchronization

The ADC12DJ3200 converters are JESD204B subclass 1 devices and therefore support deterministic latency across the JESD interface. Frame and local multi-frame clock (LMFC) clocks are generated inside the ADC12DJ3200 converters and are phase-aligned to a SYSREF signal generated by the LMK04832. The SYSREF signals are synchronous to the sample clock and can be skewed by the LMK04832 to guarantee setup and hold times are satisfied. The external trigger input can also be utilized to generate synchronous SYSREF events across multiple FMC134 boards. The synchronization pulse is also routed to the FPGA.

To initiate JESD204B frame alignment of the output samples from the four A/D converters, the FPGA must assert the SYNCSE\_L signal. When synchronization is complete, the FPGA must release the SYNCSE\_L signal high.



### NOTE

The ADC must be programmed to use the SYNCSE\_L signal as a SYNC input.

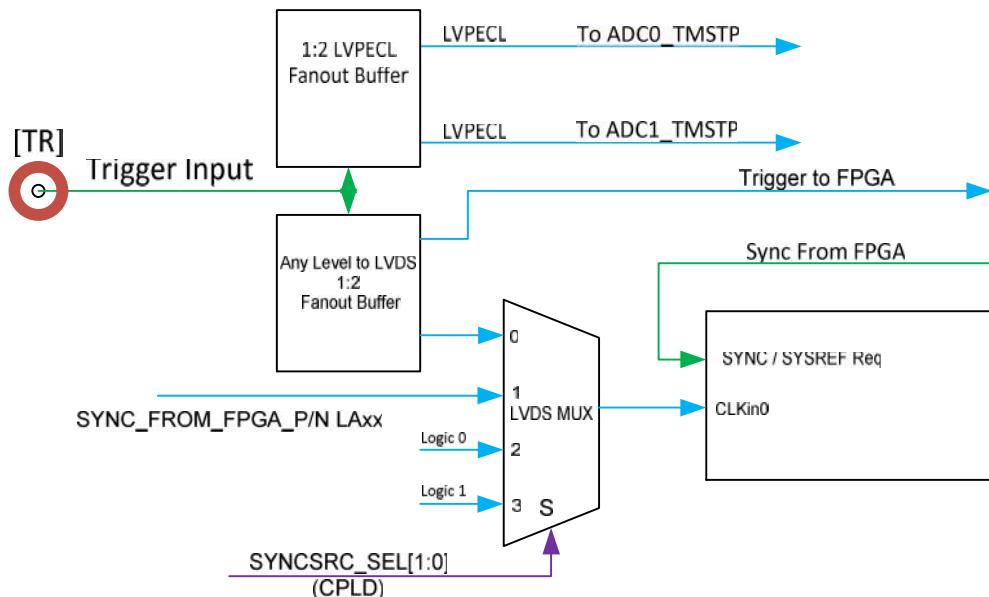
## 2.7 External Trigger/Synchronization/ Time-Stamp Input

The trigger input can be used as sync input, synchronizing local converters, or synchronizing multiple cards. The default trigger input is  $50\ \Omega$  single-ended with an LVPECL compatible threshold. As an option, the input can be configured as AC-coupled, or as a  $\sim 2.5\ k\Omega$  input with a threshold of 1.25 V to support LVTTL and LVCMOS trigger sources.

### 2.7.1 Time Stamp Input

This signal can be used with the ADC in 11-bit mode to set the LSB on the rising edge of the trigger edge. The typical silicon delay is 280 ps with an output-to-output skew of less than 15 ps and a device-to-device skew of less than 80 ps. The External Trigger connector is always routed to the ADC's TMSTP pins, refer to the TI ADS54J60 data sheet for information on configuring the ADC to output time-stamped data.

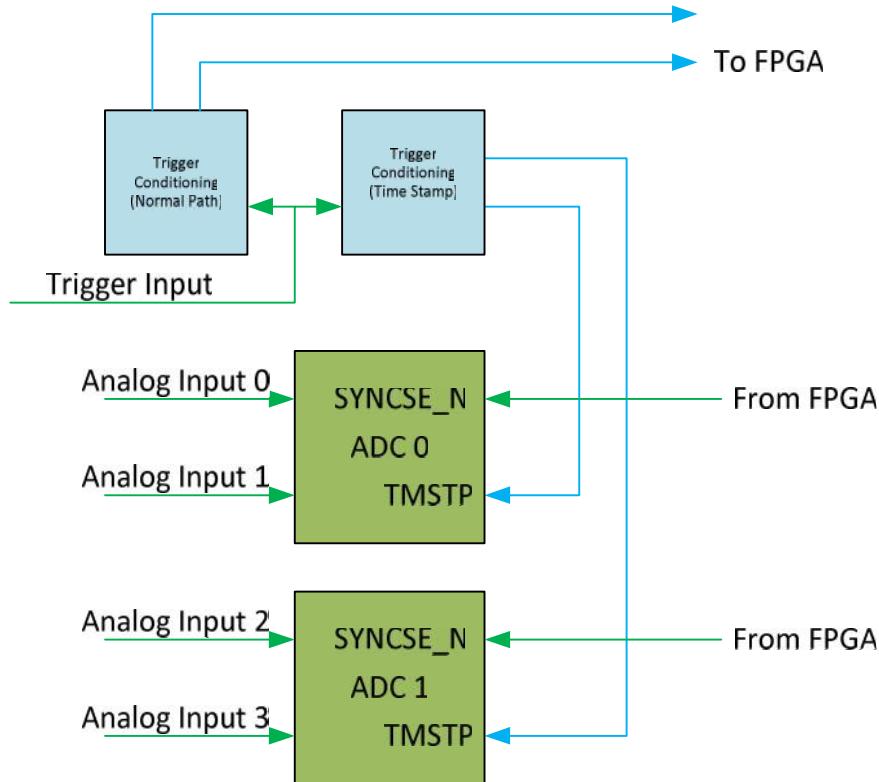
Figure 2-14 Trigger / Synchronization / Time Stamp Signal Path



## 2.7.2 Time Stamping Directly from Trigger

The split trigger input topology explained in [Section 2.6](#) provides a clean way to accurately timestamp raw ADC data across multiple converters and multiple boards using a common trigger / sync source. In this configuration FPGA sync requests must come through the SYNCSE\_L single ended sync input or must have been previously set with the TMSTP configured as the SYNC source.

Figure 2-15 ADC Time Stamp Topology

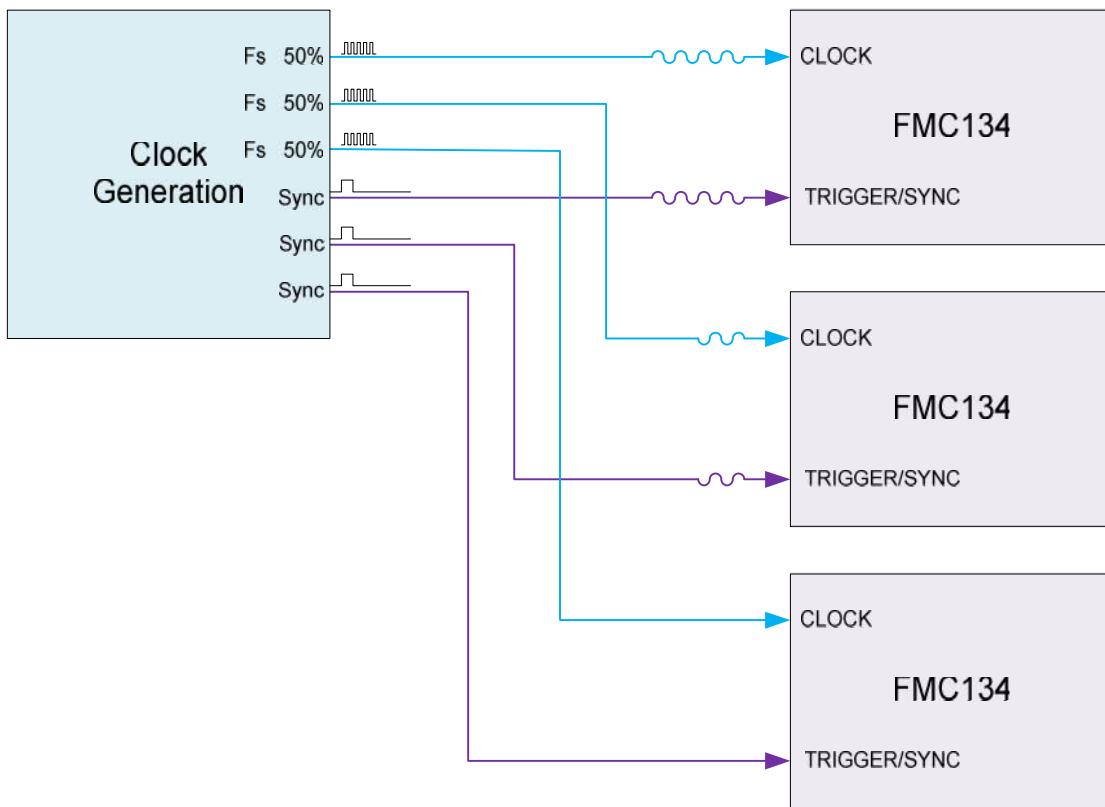


## 2.8 Multi-Card Synchronization

For synchronization to work across multiple cards, the cards need to be supplied with synchronized clock or reference signals. In addition, an external synchronization signal is required. Match the cable length between the clock/sync generator and each FMC134. The external clock generator needs to be able to tune the phase relationship between the clock and sync signal to satisfy the setup/hold timing requirements defined in the TI ADS54J50 data sheet.

The basic concept is shown in the block diagram below.

Figure 2-16 Synchronizing Multiple Cards



## 2.9 Dual-FMC134 8-Channel Stacked Synchronization Scheme

The FMC134 can be configured to share a single board's internal 100 MHz reference with a second stacked card, allowing the clocks between two boards to be synchronized. Both boards are configured via I<sup>2</sup>C with control bits from the CPLD.

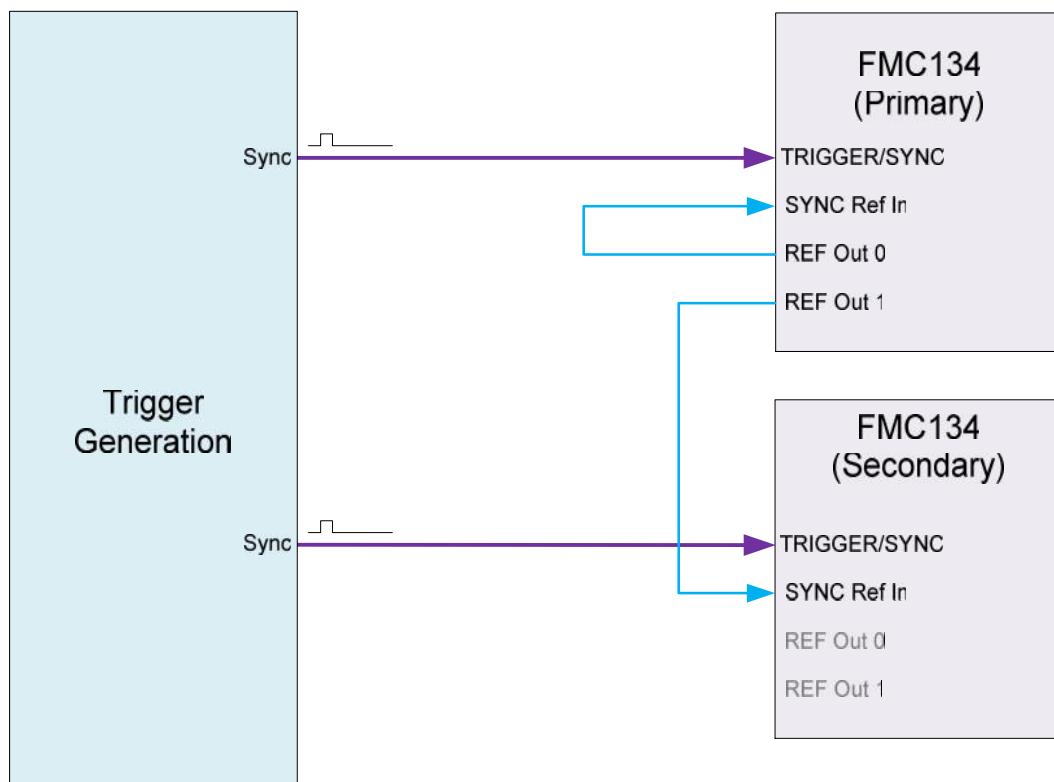
For this configuration, both boards are configured to output their reference oscillator via an onboard splitter to the front panels R0 and R1 connectors. The SI connector is routed to the CLKin0 pins on the LMK.

The boards are configured as shown in [Figure 2-17](#) below, the secondary board should have its internal 100 MHz reference oscillator turned off to reduce interference.

Both sync cables shown in must be the same length, the trigger cables must also be the same length.

First the ADCs are configured, then the JESD lanes are synchronized and then an external trigger event is sent to the FPGA to start data collection.

Figure 2-17 8-Channel Stacked Synchronization



## 2.10 JESD204B Default Setup for ADCs

The default configuration is 4 JEDS204B data lanes per individual ADC, as such the ADC's should be configured for:

L = 8

M = 2

F = 1

S = 1

HD = 1

### 2.10.1 JESD Lane Configuration

The FMC134 is designed to the FMC+ standard, The GBT Lanes are mapped to the ADCs as shown below in the following table.

Table 2-4 GBT Lane Mapping

Configuration	ADC Channels	Lane Assignment
Single FMC134	ADC-A (Ch0 & Ch1)	DP0_C2M to DP7_C2M
	ADC-B (Ch2 & Ch3)	DP8_C2M to DP15_C2M
Stacked FMC134	ADC-A (Ch0 & Ch1)	DP16_C2M to DP23_C2M
	ADC-B (Ch2 & Ch3)	DP24_C2M to DP31_C2M

## 2.11 Power Supply

The available input power, through the FMC+ HSPC connector, along with the calculated typical and maximum current consumption is shown the table below.



### NOTES

At 3.2 GSPS there is only about 1 W difference between all the operating modes.

Power consumption does NOT include the Firefly Interface.

Table 2-5 FMC Available Power and Power Consumption

Power Plane	Maximum Available	Typical Current (mA)	Maximum Current (mA)	Typical Power (Watts)	Maximum Power (Watts)
VADJ	4000 mA	20			
3P3V	3000 mA	2810	2819	6.1	9.3
12P0V	1000 mA	516	591	6.2	7.1
VIOB	1 mA				
3P3VAUX (Operating) 3P3VAUX (Standby)	20 mA  1 µA				

## 2.12 Phase Coherent Interleaving

Each ADC IC has the capability to be a single input 6.4 GSPS converter, register access is provided to adjust the ADCs Full Scale, as well as access to the individual ADC's, gain, offset, and timing.

# 3 • Controlling the FMC134

## 3.1 I<sup>2</sup>C Devices

The devices shown in [Table 3-1](#) are directly connected to the I<sup>2</sup>C bus. The EEPROM is powered by VAUX and directly faces the I<sup>2</sup>C bus, the other devices are behind an I<sup>2</sup>C level translator for isolation until full power is applied.

Table 3-1 I<sup>2</sup>C Slave Addresses

Device	I <sup>2</sup> C Address	GA1	GA0	Address Binary	Address Hex
M24C02 (EEPROM)	10100XX	0	0	1010000	0x50
		0	1	1010010	0x52
		1	0	1010001	0x51
		1	1	1010011	0x53
AD7291 (ADC Monitor)	010XXXX	0	0	0101111	0x2F
		0	1	0101100	0x2C
		1	0	0100011	0x23
		1	1	0100000	0x20
AD7291 (Voltage Monitor)	010XXXX	0	0	See <a href="#">Table 3-2</a>	(Translated)
		0	1		0x2E
		1	0		0x2B
		1	1		0x28
CPLD (Board Control)	00111XX	0	0	0011100	0x1C
		0	1	0011101	0x1D
		1	0	0011110	0x1E
		1	1	0011111	0x1F
Firefly Interface		N/A	N/A		



### NOTES

To provide isolation from the FMC connector's GA0 and GA1 lines, and to prevent any device from being powered up through its address inputs, the CPLD reads the GA0 and GA1 lines and provides signals CPLD\_GA0\_OUT\_3P3 and CPLD\_GA1\_OUT\_3P3.

To allow operation of a stacked card, the CPLD reads the GA0 and GA1 and provides output signals CPLD\_GA0\_OUT\_CC\_3P3 and CPLD\_GA1\_OUT\_CC\_3P3.

To allow a second AD7291 to exist on the FMC134 address re-mapping is used as described in the following section.

### 3.1.1 I<sup>2</sup>C Address Translation for Second AD7291

To monitor all the supply voltages as well as the ADC's temperature a second AD7291 is located on the FMC134 with an alternate set of addresses provided by the CPLD. The CPLD either drives the XGA0 and XGA1 pins based on the lookup table shown in the table below.

Table 3-2 AD7291 #2 Address Translation

FMC Signal		CPLD Output		Final Address	
GA1	GA0	XGA1/AS1	XGA0/AS0	Binary	Hex
0	0	0	Tri-State	010 1110	0X2E
0	1	Tri-State	1	010 1011	0x2B
1	0	Tri-State	0	010 1010	0x28
1	1	1	Tri-State	010 0010	0x22

## 3.2 Controlling the CPLD

The CPLD is implemented as an I<sup>2</sup>C device with 16 registers that are used to control devices, read status bits and perform I<sup>2</sup>C to SPI transactions.

Good knowledge of the internal structure and communication protocol of relevant onboard devices is required for controlling the FMC134. For detailed information, it is recommended to refer to the datasheets mentioned in the [Third-party Documents](#) section. In addition, Abaco may be contacted for support.



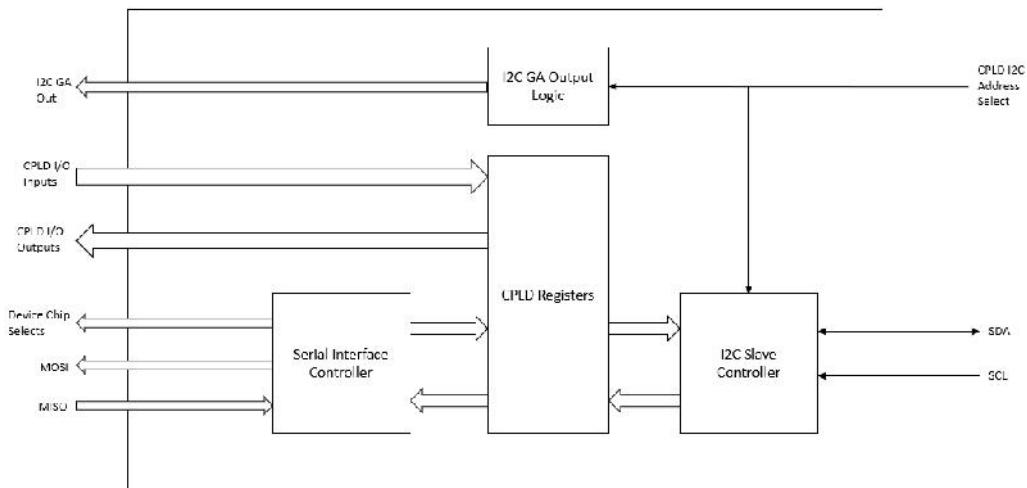
LINK

<https://www.abaco.com/support>

### 3.2.1 CPLD Simplified Block Diagram

A Xilinx XC2C256 CPLD is used to implement the control logic between the host I<sup>2</sup>C bus and the FMC134. See [Table 3-3](#) for a full list of signals connected to the CPLD.

Figure 3-1 CPLD Architecture



### 3.2.2 CPLD Register Map

Register	Address	R/W	Description
ADDR_COMMAND	0x00	W	Selects which device to communicate with. BIT 0: ADC0, default = 0 BIT 1: ADC1, default = 0 BIT 2: LMX2581, default = 0 BIT 3: LMK04832, default = 0 BIT 4: HMC987, default = 0
ADDR_CONTROL0	0x01	R/W	BIT 0: RESERVED, default = 0 BIT 1: RESERVED, default = 0 BIT 2: EXT_SAMPLE_CLK_3P3, default = 1 BIT 3: LMK04832_RESET_3P3, default = 0 BIT 4: SYNC_SRC_SEL_3P3_0, default = 0 BIT 5: SYNC_SRC_SEL_3P3_1, default = 0 BIT 6: ADC_CALTRIG_1P9_0, default = 0 BIT 7: ADC_CALTRIG1P9_1, default = 0
ADDR_CONTROL1	0x02	R/W	BIT 0: OSC100_EN_3P3, default = 1 BIT 1: REF_INT_3P3, default = 1 BIT 2: AD7291_RESETS_3P3 (both devices), default = 1 BIT 3: LMX2581_ENABLE_3P3, default = 1 BIT 4: FF_CS_3P3_L, default = 1 BIT 5: FF_RESET_3P3_L, default = 1 BIT 6: LED_ENABLE_3P3, default = 1 BIT 7: Reserved, must write 1, default = 1
ADDR_STATUS0	0x04	R	BIT 0: ADC0_CAL_STAT_1P9 (Alarm output) BIT 1: ADC1_CAL_STAT_1P9 (Alarm output) BIT 2: ALARM_AD7291_0_3P3 Temperature ALARM BIT 3: ALARM_AD7291_1_3P3 Voltage ALARM BIT 4: LMX_STATUS_LD_3P3 BIT 5: FF_PRESENT_L_3P3 BIT 6: GA0_MOD_IN_3P3 BIT 7: GA1_MOD_IN_3P3
ADDR_VERSION	0x05	R	0x10
ADDR_I2C_DATA_0	0x06	W	LSB byte to send to the selected SPI device
ADDR_I2C_DATA_1	0x07	W	2nd byte to send to the selected SPI device
ADDR_I2C_DATA_2	0x08	W	3rd byte to send to the selected SPI device
ADDR_I2C_DATA_3	0x09	W	4th byte to send to the selected SPI device
ADDR_I2C_READ_0	0x0A	R	LSB byte read from SPI device
ADDR_I2C_READ_1	0x0B	R	2nd byte read from SPI device
ADDR_I2C_READ_2	0x0C	R	3rd byte read from SPI device
ADDR_I2C_READ_3	0x0D	R	4th byte read from SPI device

### 3.2.3 CPLD Signals Functional Description

I/O's are level shifted as required. The signal direction is as follows:

- ]) Output signals from the CPLD are identified with an 'O'
- ]) Input Signals to the CPLD are identified with an 'I'
- ]) Bidirectional Signals are identified with an 'I/O'
- ]) Initial state 1, 0, or either indeterminate or based on associated documentation
- ]) IFF there is an associated register field is entered x.x (Address.Bit)

The signal names and functions are listed in the table below.

Table 3-3 CPLD Control Signals

Signal Name	Initial State	I/O	ADR	Description
ADC0_SPI_SCS_1P9_L	1	0	0.0	Chip select output for ADC0 SPI
ADC1_SPI_SCS_1P9_L	1	0	0.1	Chip select output for ADC0 SPI
LMX2581_SPI_CS_3P3_L	1	0	0.2	Chips select output for LMX2581 SPI
LMK04832_SPI_CS_3P3_L	1	0	0.3	Chips select output for LMK04832 SPI
HMC987_SPI_CS_3P3_L	1	0	0.4	Chips select output for HMC987 SPI
RESERVED	0	0	1.0	SET TO 0
RESERVED	0	0	1.1	SET TO 0
EXT_SAMPLE_CLK_3P3	1	0	1.2	Configures sample clock selection. See <a href="#">Table 3-4</a> .
LMK04832_RESET_3P3	0	0	1.3	A logic 1 resets the LMK04832 Clock Chip
SYNC_SRC_SEL_3P3_0	0	0	1.4	00 = External trigger 01 = FPGA trigger 02 = Logic 0 02 = Logic 1
SYNC_SRC_SEL_3P3_1	0	0	1.5	00 = External trigger 01 = FPGA trigger 02 = Logic 0 02 = Logic 1
ADC0_CALTRIG_1P9	0	0	1.6	A logic 1 initiates an ADC0 calibration cycle
ADC1_CALTRIG_1P9	0	0	1.7	A logic 1 initiates an ADC1 calibration cycle
OSC100_EN_3P3	1	0	2.0	A logic 1 enables the power supply to the onboard 100 MHz reference oscillator
REF_INT_3P3	1	0	2.1	A logic 1 routes the 100 MHz reference oscillator to the LMX PLL clock input
AD7291_RESET_3P3_L	1	0	2.2	A logic 0 resets both AD7291 Devices 10 k external pull up to VCC. This line must default to a 1, do not hold this line at a logic 0
LMX2581_ENABLE_3P3	1	0	2.3	A logic 1 enables the LMK2581 PLL synthesizer via CE pin
FF_CS_3P3_L	1	0	2.4	A logic 0 enables the Firefly I <sup>2</sup> C bus

Signal Name	Initial State	I/O	ADR	Description
FF_RESET_3P3_L	1	0	2.5	A logic 0 resets the FF module Open Drain, 24K internal to 3.3V at FF
LED_ENABLE_3P3	1	0	2.6	Software controllable LED 1 = ON
EEPROM_WP_3P3	1	0	2.7	must write 1, default = 1
ADC0_CAL_STAT_1P9	x	I	4.0	ADC-0 calibration in progress signal
ADC1_CAL_STAT_1P9	x	I	4.1	ADC-1 calibration in progress signal
ALARM_AD7291_0_3P3	x	I	4.2	AD7291 Alarm output mostly temp and Voltage
ALARM_AD7291_1_3P3	x	I	4.3	AD7291 Alarm output mostly voltages
LMX_STATUS_LD_3P3	x	I	4.4	Lock detect output from LMX2581
FF_PRESENT_L_3P3	x	I	4.5	Low when FF module is present Requires Pull Up to 3.3 V
GA0_MOD_IN_3P3	x	I	4.6	Input state of GA0
GA1_MOD_IN_3P3	x	I	4.7	Input state of GA1
SPI_SCLK_3P3	0	0		3.3 V SPI serial clock to LMX and LMK
SPI_MOSI_3P3	0	I/O		3.3 V SPI data to LMK & LMX
SPI_LMK_MISO_3P3	x	I		3.3 V LMK SPI data output
ADC_SPI_SCLK_1P9	0	0		1.9 V SPI serial clock to ADCs
ADC_SPI_MOSI_1P9	0	I/O		1.9 V SPI data to ADCs
ADC_SPI_MISO_1P9	x	I		1.9 V SPI data from ADCs
ISO_I2C_SCL_3P3		I		I <sup>2</sup> C clock input to CPLD, on isolated side of PCA9517
ISO_I2C_SDA_3P3		I/O		I <sup>2</sup> C data I/O CPLD, on isolated side of PCA9517
CPLD_XGA0_OUT_3P3		0		Alternate address controls for AD7291 (LUT output from GA0:GA1)
CPLD_XGA1_OUT_3P3		0		(LUT output from GA0:GA1)
CPLD_GA0_OUT_3P3	x	0		Tracks GA0, provides isolated buffered signal
CPLD_GA1_OUT_3P3	x	0		Tracks GA1, provides isolated buffered signal
CPLD_CLOCK_4MHZ_3P3	x	I		4 MHz clock input to CPLD
PRESENT_M2C_CC_L_3P3	x	I		Connection only CPLD vision to stacked card present
PG_C2M_3P3	x	I		Connection only
PG_M2C_3P3	x	I		Connection only
RES0	x	I		Connection only
GA0_CC_OUT_3P3	x	0		GA0...GA1_CC = (GA0...GA1) +1
GA1_CC_OUT_3P3	x	0		(Read input and increment by 1)
				CPLD Auxiliary Control Signals
CPLD_AUX_CTRL0	x	I/O		FMC_CPLD_CTRL0_VADJ (level translated to VADJ)
CPLD_AUX_CTRL1	x	I/O		FMC_CPLD_CTRL1_VADJ
CPLD_AUX_CTRL2	x	I/O		FMC_CPLD_CTRL2_VADJ
CPLD_AUX_CTRL3	x	I/O		FMC_CPLD_CTRL2_VADJ

## 3.3 Controlling the Clock Tree

### 3.3.1 Oscillators and switches

The FMC134 has two sets of RF switches that select whether an internal or external reference or internal or external oscillator is used. These switches must be configured via I<sup>2</sup>C register writes for the supported configurations. The following table lists the CPLD bits that are required to be modified for a specific mode of operation.

Table 3-4 Supported Clocking Modes

Function	Mode	EXT_SAMPLE_CLK_3P3	REF_INT_3P3	OSC100_EN_3P3	LMX2581_ENABLE_3P3
Power-Down	0	0	0	0	0
LMX PLL with External reference	1	1	0	0	1
Stacked mode Ref Internal Reference On	3	1	0	1	1
LMX PLL with int. 100 MHz reference (Default)	7	0	1	1	1
LMK ext. clock distribution, [C1] connector	8	0	0	0	0

### 3.3.2 General Guidelines

Apart from enabling the onboard reference oscillators, RF switches, and trigger circuitry, which are controlled by I<sup>2</sup>C writes to the CPLD, the remainder of the clock-tree is programmed via SPI writes to the LMX04832, LMK2581, and HMC987 devices.

1. Before programming the LMK04832 device, initiate an I<sup>2</sup>C write to the CPLD to clear, set, and then clear the LMK\_RESET.
2. The unused outputs on the LMK04832 must be disabled.
3. The unused outputs on the HMC987 must be disabled.
4. All PLL1 and PLL2 functions should be disabled on the LMX04832 since it is being used only for clock distribution.
5. TI notes that sending SPI commands while the PLL is locked may degrade phase noise performance, so the I<sup>2</sup>C / SPI bus should remain static as much as possible during normal operation.

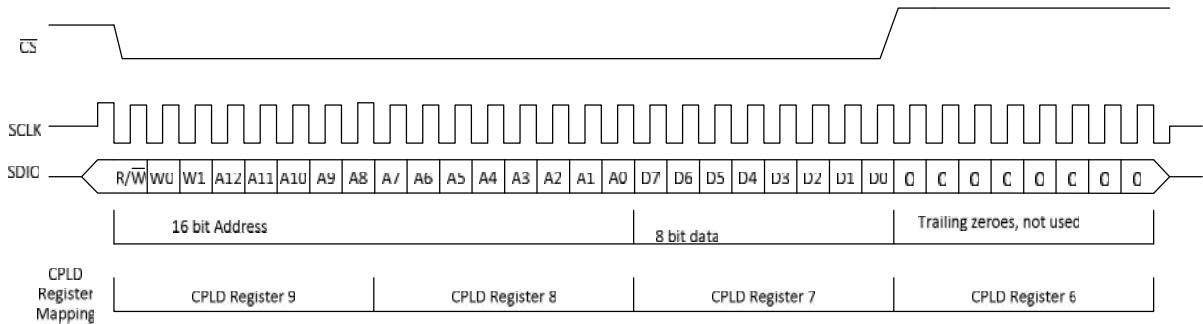
### 3.3.3 LMK04832 Clock Tree SPI Communication

Communication with the LMK04832 clock generator IC is via the CPLD and I<sup>2</sup>C bus. Based on the desired clock source, configure the OSC100EN and OSC500\_EN bits in the CPLD.

Based on the Trigger / Sync requirements, configure bit 4 and bit 5 of CPLD register 1 (sync\_src\_sel\_0 and sync\_src\_sel\_1)

Per the TI data sheet, the LMK04832 communicates with 24-bit words across the SPI bus, with the command organized as shown in the figure below.

Figure 3-2 LMK 04828 / LMK04832 SPI Transaction



The I<sup>2</sup>C register transactions to the CPLD listed in Sections 3.1 and 3.2 describe the operation.

### 3.3.4 LMK04832 SPI Write Register Command Sequence:

- J To write an LMK04832 register the R/W bit in the SPI command must be '0'
- J Write the second byte to send, bits R/W through A8 to CPLD Register 9
- J Write the third byte to send, bits A7 through A0 to CPLD register 8
- J Write the last byte to send, D7 through D0 to CPLD Register 7
- J Write an 0x01 to the CPLD register 0, to initiate a SPI bus write of the message

### 3.3.5 LMK04832 SPI Read Register Command Sequence:

- J To write an LMK04832 register the R/W bit in the SPI command must be '1'
- J Write the second byte to send, bits R/W through A8 to CPLD Register 9
- J Write the third byte to send, bits A7 through A0 to CPLD register 8
- J Write the last byte to send, D7 through D0 to CPLD Register 7 (data = don't care)
- J Write an 0x01 to the CPLD register 0, to initiate a SPI bus transaction
- J The result of the read operation can be read out of CPLD Register 0x0F,

### 3.3.6 LMX2581 PLL Synthesizer Communication

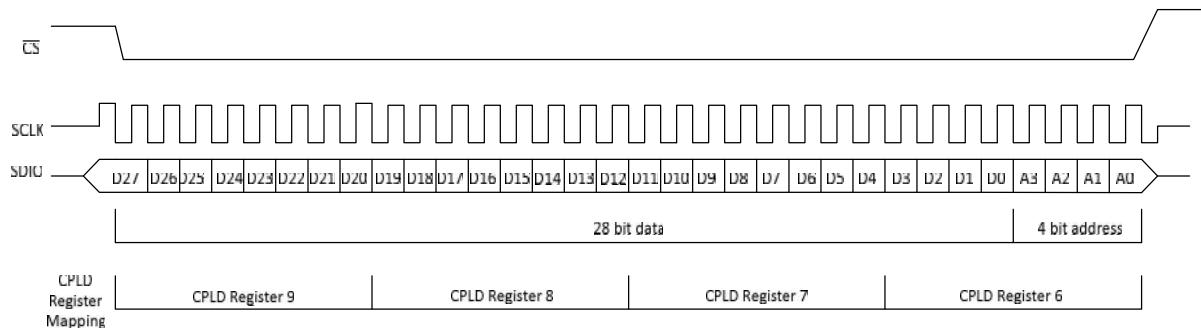
Communication with the LMX2581 PLL Synthesizer IC is performed via the CPLD and I<sup>2</sup>C bus.

Based on the desired clock source, configure the CPLD OSC100\_EN bit, to minimize interference turn off the 500 MHZ VCXO, and Disable the LMX PLL1, PLL2, VCOs, and configure the LMX to use the external oscillator input.

Based on the Trigger / Sync requirements, configure the CPLD sync\_src\_sel\_0, and sync\_src\_sel\_1 bits.

Per the TI data sheet, the LMX2581 communicates with 32-bit words across the SPI bus, to send an SPI bus command to the device, the control word is mapped as shown below.

Figure 3-3 LMX2581 SPI Configuration



The I<sup>2</sup>C register transactions to the CPLD listed in Sections 3.1 and 3.2 describe the operation.

### 3.3.7 LMX2581 SPI Write Register Command Sequence:

- | To write to an LMX2581 register, the R/W bit in the SPI command must be '0'
  - | Write the first byte to send bits D27 through D20 to CPLD Register 9
  - | Write the second byte to send bits D19 through D12 to CPLD register 8
  - | Write the third byte to send bits D11 through D4 to CPLD register 7
  - | Write the last byte to send D3 through A0 to CPLD Register 6
  - | Write a 0x01 to the CPLD register 0 to initiate a SPI bus write of the message

### 3.3.8 Controlling the HMC987 Fanout Buffer

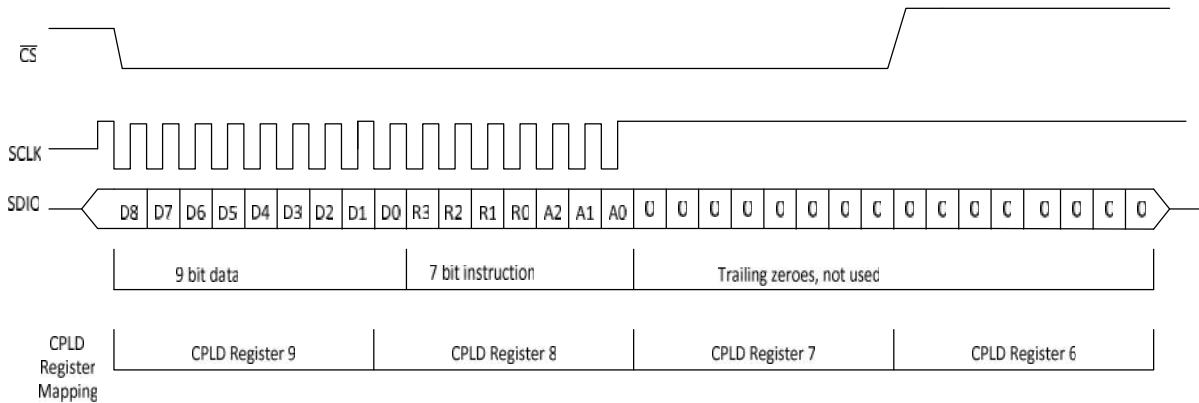
The sample clock is distributed using the HMC987 fanout buffer. Output 5 goes to ADC0, output 1 goes to ADC1, output 8 goes to the LMK04832, RFOUT goes to the front panel connector CO Communication with the HMC987 PLL Synthesizer IC is performed via the CPLD and I<sup>2</sup>C bus.

Based on the desired clock source, configure the CPLD OSC100\_EN bit, to minimize interference turn off the 500MHZ VCXO, and Disable the LMX PLL1, PLL2, VCOs, and configure the LMX to use the external oscillator input.

Based on the Trigger / Sync requirements, configure the CPLD sync\_src\_sel\_0, and sync\_src\_sel\_1 bits.

Per the Analog Devices data sheet, the HMC987 communicates with 16bit words across the SPI bus, to send an SPI bus command to the device, the control word is mapped as shown in [Figure 3-4](#).

Figure 3-4 HMC987 SPI Timing



### 3.3.9 HMC987 SPI Write Register Command Sequence:

Write the first byte to send, bits D8 through D1 to CPLD Register 9.

Write the second byte of the message, bits D0 through A0 to CPLD register 8.

Write an 0x10 to the CPLD register 0, to Initiate a SPI bus write of the message

## 3.4 Controlling the ADC

There are 2 Texas Instruments ADC12DJ3200 Dual-Channel, 14-Bit, 3.0-GSPS Analog to Digital Converters on the FMC134. Most communication with the ADC is performed via the I<sup>2</sup>C to SPI bridge in the CPLD.

### 3.4.1 ADC Reset Signals

The TI ADC12DJ3200 ADC's RESET pins are directly controlled by the CPLD signals ADC0\_RESET and ADC1\_RESET.

The normal state of this bit is a logic 0, on powerup, prior to programming the ADCs, an I<sup>2</sup>C command should write the pin high and then low to put the ADC into a known state

### 3.4.2 ADC GPIO Signals

The four GPIO lines are bidirectionally level translated to VADJ with a TI TXB0304 to allow fast interaction between the FPGA for over-range, alarms, or NCO control functions as defined in the data sheet.

The hardware power-down and over-range signals are level translated to VADJ appear on Signals LA06\_P through LA08\_N. Everything else is controlled by programming the ADC12DJ3200 ADCs via SPI through the CPLD's I<sup>2</sup>C serial interface.

### 3.4.3 General Guidelines for Controlling the ADCs

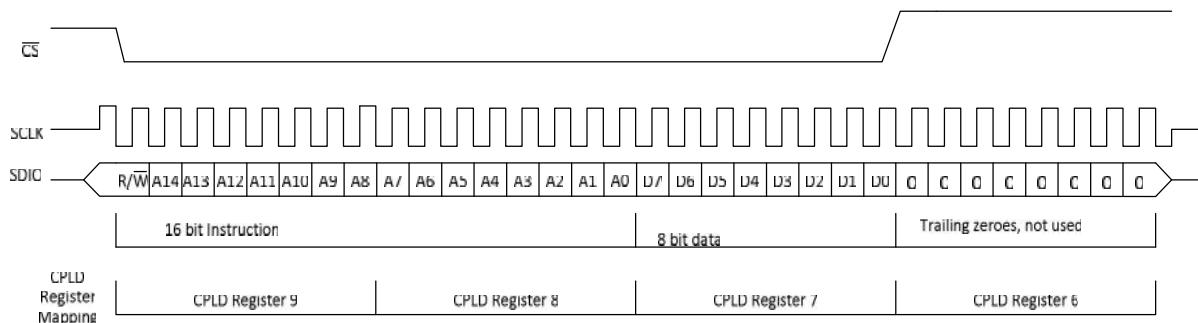
The SYSCLK signal to the ADC(s) must be enabled for proper programming of the ADC, it may be disabled after the ADC is fully programmed.

Communicating with the ADC over the SPI while collecting data may introduce noise into the ADC.

### 3.4.4 ADC12DJ3200 ADC SPI Communication

Per the TI data sheet, the ADC12DJ3200 communicates with 24-bit words across the SPI bus, the control word is mapped as shown below.

Figure 3-5 ADC12DJ3200 SPI Transaction



### 3.4.5 ADC12DJ3200 SPI Write Register Command Sequence:

To write an ADC12DJ3200 register the R/W bit in the SPI command must be '0'.

- ) Write the first byte to send, bits R/W through A8 to CPLD Register 9.
  - ) Write the second byte of the message, bits A7 through A0 to CPLD register 8.
  - ) Write the last byte of the message, D7 through D0 to CPLD Register 7.
  - ) To write to ADC-A inputs A0 and A1, write an 0x04 to CPLD Register 0, or for ADC-B inputs A2 and A3, write an 0x08 to CPLD register 0, or for both ADC-A and ADC-B simultaneously, write an 0x0C to CPLD register 0. This initiates an SPI bus write of the message.

### 3.4.6 ADC12DJ3200 SPI Read Register Command Sequence:

To read an ADC12DJ3200 register the R/W bit in the SPI command must be '1'.

- ) Write the first byte to send, bits R/W through A8 to CPLD Register 9.
  - ) Write the second byte of the message, bits A7 through A0 to CPLD register 8.
  - ) Write the last byte to send, D7 through D0 to CPLD Register 7 (data = don't care)
  - ) To read from ADC-A inputs A0 and A1, write an 0x04 to CPLD Register 0, or for ADC-B inputs A2 and A3, write an 0x08 to CPLD register 0. This initiates an SPI bus write of the message.
  - ) The result of the read operation can be read out of CPLD Register 0xA.

## 3.5 Guidelines for Controlling Onboard Voltage and Temp Monitoring

The FMC134 includes two AD7291 ‘8-channel I<sup>2</sup>C 12-bit SAR ADCs with temperature monitor’ devices for monitoring power supply voltages as well as local and remote temperatures. The device can be programmed and read through the I<sup>2</sup>C bus at the address defined in [Section 3.1](#).

1. At powerup, the firmware should write a ‘1’ to the Reset bit in the Command Register to initialize the part to a known state.
2. All measured values must be multiplied by a constant to convert to the actual analog level, formulas are included in the associated tables and text.
3. Continuously operating the I<sup>2</sup>C bus might interfere with the A/D conversion process resulting in signal distortion. It is recommended to program the minimum and maximum thresholds in the monitoring device and only read from the device when the interrupt line is asserted

### 3.5.1 AD7291 (ADC Monitor)

The first device, identified in [Section 3.1](#) as (ADC monitor) is configured to monitor the ADC voltages and temperatures shown in the table below. To convert the ADC reading to voltage or temperature multiply the ADC value by the scaling factor listed in the table. For the ADCs 2 onboard temperature monitors see [Section 3.5.2](#).

Table 3-5 AD7291 Voltage Parameters

Parameter:	Voltage	Formula
Channel 0	VP_ADC0_1P1V_ANA	ADC0 * .00061035 V
Channel 1	VP_ADC0_1P1V_DIG	ADC1 * .00061035 V
Channel 2	VP_ADC0_1P9V_ANA	ADC2 * .00061035 V
Channel 3	VP_ADC1_1P1V_ANA	ADC3 * .00061035 V
Channel 4	VP_ADC1_1P1V_DIG	ADC4 * .00061035 V
Channel 5	VP_ADC1_1P9V_ANA	ADC5 * .00061035 V
Channel 6	ADC0_TEMP	(ADC6) 1.6 mV / °C, see text
Channel 7	ADC1_TEMP	(ADC7) 1.6 mV / °C, see text
Temperature	(internally generated)	AD7921 ADC TEMP * .0625 °C

### 3.5.2 ADC Temperature Measurement

Texas Instruments specifies a maximum die temperature of 105 °C for the ADCDJ3200 ADC IC, and notes that operation above this point will degrade the life expectancy of the ADC.

As explained below, operation with the reference design at an indicated ADC die temperature at or above ~+90 °C requires calibration of the temperature diodes to ensure the maximum die temperature is not exceeded!

On the FMC134, each ADC has a temperature diode, (TDIODE) which can be used to monitor the ADC's temperature, unfortunately this diode is not very well characterized and has a spread of about +/- 23 mV or ~ +/- 14 °C.

The FMC134 forward biases the TDIODE with a 100  $\mu$ A current source, the resulting temperature dependent voltages can be monitored on channels 6 and 7 of the AD7291 described in the previous section.

Abaco (and TI) does not provide individual 25 °C calibration data on the ADC's TDIODE voltage at 25 °C. The Fmc134APP reference application uses a nominal value of ~0.750 V as the 25 °C offset value. Taking the +/- 14 °C error budget into account, this means that the board can safely operate at a displayed temperature of ~+90 °C.

For applications that run the board at high ambient temperatures, the temperature diode should be measured at 25 °C to get an accurate offset voltage.

Once the 2 ADC temperatures are accurately calibrated further temperature testing can proceed. If the actual ADC die temperature is at or above 105 °C the user should take additional measures to further cool the board.

To accurately measure the diode temperature, the board should be stable at room temperature, with proper ventilation applied, the software application should then perform the following:

- ]) At powerup hold both ADCs in reset, measure the ambient temperature on the two AD7291's, average the readings, and save this value as the ambient temperature offset as the baseline temperature in °C.
- ]) Measure each respective temperature diode.
- ]) Save these two voltages as the ambient temperature offset voltage,
- ]) This voltage is board and ADC specific and should be used in the individual boards end application.
- ]) Continue with normal power up sequencing, do not leave the ADC in this state!

On subsequent temperature readings, measure the ADC's internal TDIODE voltage,

- ]) Subtract out the ambient temperature reference voltage
- ]) Multiply the result by .00061035 V              (convert to volts)
- ]) Divide this result by .0016                          (convert to °C)
- ]) Add this result to the ambient temperature offset to get the die temperature in °C.

Once this code is functional, it will be possible to extrapolate a nominal upper temperature limit to program into the AD7291 for alarm.

### 3.5.3 AD7291(Voltage Monitor)

The second device, identified in [Section 3.1](#) as (temperature monitor) is configured to monitor the voltages are shown in the table below. To convert the ADC reading to a voltage or temperature multiply the ADC value by the scaling factor listed in the table.

Table 3-6 AD7291 Temperature and Voltage Parameters

Parameter:	Voltage	Formula
Channel 0	VP5P5_OSC100	$ADC0 * .00183105V$
Channel 1	VP3P3_CLOCK	$ADC1 * .0012207V$
Channel 2	VP3P3_LMXPLL	$ADC2 * .0012207V$
Channel 3	VP_CPLD_1P8V	$ADC3 * .00061035V$
Channel 4	VADJ	$ADC4 * .0012207V$
Channel 5	3.3V FMC	$ADC5 * .0012207V$
Channel 6	12.0V FMC	$ADC6 * .0036621V$
Channel 7	VIO_M2C	$ADC7 * .0012207V$
Temperature	(internally generated)	$AD7921 \text{ ADC TEMP} * 0.0625 ^\circ\text{C}$

## 3.6 Firefly Interface

The Firefly interface is powered from the FMC 3.3 V bus, the module present signal is connected to the CPLD FF\_PRESENT\_3P3 bit can be monitored by the CPLD to determine when a module is present, the bit is pulled high to the CPLD's 3.3 V supply.

The optional firefly interface resides on the isolated side of the I<sup>2</sup>C interface, and the normal I<sup>2</sup>C protocol is used, however, on the FMC134, the Module Select line FF\_CS\_3.3L must be asserted low prior to any communication, The Module select line allows multiple Firefly modules to reside on the same I<sup>2</sup>C bus, (this is a firefly function).

The firefly Interrupt pin is level translated to VADJ and routed to the FPGA.

# 4 • Specifications

## 4.1 Environmental Specifications

**Operating temperature:**

- J 0 °C to +50 °C (Commercial)
- J -40 °C to +71 °C (Industrial)

**Storage temperature:**

- J -40 °C to +120 °C

## 4.2 Cooling

The FMC134 has an integral heatsink, the board should not be operated without its heatsink, furthermore, Benchtop operation requires a fan to be used to maintain a safe operating temperature. In all cases the temperature should be monitored, and steps taken to limit the temperature rise of the board.

Two different types of cooling will be available for the FMC134.

### 4.2.1 Convection Cooling

The air flow provided by the chassis fans that the FMC134 is enclosed in must dissipate the heat generated by the onboard components. A minimum airflow of 300 LFM is recommended.

The card has 2 test points which could be used for a 12 V fan power connection. For standalone operations (such as on a Xilinx development kit), it is highly recommended to blow air across the FMC and ensure that the temperature of the devices is within the allowed range. Abaco warranty does not cover boards on which the maximum allowed temperature has been exceeded.

### 4.2.2 Conduction Cooling

In demanding environments, the ambient temperature inside a chassis could be close to the operating temperature defined in this document. It is very likely that in these conditions the junction temperature of power consuming devices will exceed the operating conditions recommended by the devices manufacturers (mostly +85 °C). While a low-profile heat sink coupled with sufficient air flow might be sufficient to maintain the temperature within operating boundaries, some active cooling would yield better results and would certainly help with resuming operations much faster in the case the devices were disabled because of a temperature “over range”.

# A • FMC134 FMC Mezzanine and Carrier Connector Pinout Table

Table Notes: (Apply to Appendices A and B)

- ✓ All power and ground pins are connected to their common nets on both mezzanine and carrier connectors for stacked operation
- ✓ All pins not explicitly noted in the table are passed through between the mezzanine and carrier connectors for stacked operation
- ✓ Mezzanine (module) connector exclusive pins are noted in **RED**
- ✓ Carrier connector exclusive pins are noted in **BLUE**
- ✓ Common (pass through pins) are noted in **GREEN**
- ✓ Mezzanine signals remapped to Carrier Connector for FMC134 are in **VIOLET**

AV57.4	Pin	FMC134 Signal	Notes
Clock Signal Name			
CLK0_M2C_P	<b>H4</b>	LMK_OUT_2_P	D-Clock
CLK0_M2C_N	<b>H5</b>	LMK_OUT_2_N	D-Clock
CLK1_M2C_P	<b>G2</b>	LMK_OUT_3_P	S-Clock
CLK1_M2C_N	<b>G3</b>	LMK_OUT_3_N	S-Clock
GBTCLK0_M2C_P	<b>D4</b>	LMK_OUT0_P	D-Clock Quad 0
GBTCLK0_M2C_N	<b>D5</b>	LMK_OUT0_N	D-Clock
GBTCLK1_M2C_P	<b>B20</b>	LMK_OUT0_P	D-Clock Quad 1
GBTCLK1_M2C_N	<b>B21</b>	LMK_OUT1_N	D-Clock
GBTCLK2_M2C_P	<b>L12</b>	LMK_OUT12_P	D-Clock Quad 2
GBTCLK2_M2C_N	<b>L13</b>	LMK_OUT12_N	D-Clock
GBTCLK3_M2C_P	<b>L8</b>	LMK_OUT13_P	D-Clock Quad 3
GBTCLK3_M2C_N	<b>L9</b>	LMK_OUT13_N	D-Clock
GBT Lanes			ADCA-Pin Signal Name
DP0_M2C_P	<b>C6</b>	DP0_M2C_P	ADCA-DA0P
DP0_M2C_N	<b>C7</b>	DP0_M2C_N	ADCA-DA0N
DP1_M2C_P	<b>A2</b>	DP1_M2C_P	ADCA-DA1P
DP1_M2C_N	<b>A3</b>	DP1_M2C_N	ADCA-DA1N
DP2_M2C_P	<b>A6</b>	DP2_M2C_P	ADCA-DA2P
DP2_M2C_N	<b>A7</b>	DP2_M2C_N	ADCA-DA2N
DP3_M2C_P	<b>A10</b>	DP3_M2C_P	ADCA-DA3P
DP3_M2C_N	<b>A11</b>	DP3_M2C_N	ADCA-DA3N
GBT Lanes			ADCA-Pin Signal Name

AV57.4	Pin	FMC134 Signal	Notes
Clock Signal Name			
DP4_ M2C_P	<b>A14</b>	DP4_ M2C_P	ADCA-DB0P
DP4_ M2C_N	<b>A15</b>	DP4_ M2C_N	ADCA-DB0N
DP5_ M2C_P	<b>A18</b>	DP5_ M2C_P	ADCA-DB1P
DP5_ M2C_N	<b>A19</b>	DP5_ M2C_N	ADCA-DB1N
DP6_ M2C_P	<b>B16</b>	DP6_ M2C_P	ADCA-DB2P
DP6_ M2C_N	<b>B17</b>	DP6_ M2C_N	ADCA-DB2N
DP7_ M2C_P	<b>B12</b>	DP7_ M2C_P	ADCA-DB3P
DP7_ M2C_N	<b>B13</b>	DP7_ M2C_N	ADCA-DB3N
GBT Lanes			ADCB-Pin Signal Name
DP8_ M2C_P	<b>B8</b>	DP8_ M2C_P	ADCB-DA0P
DP8_ M2C_N	<b>B9</b>	DP8_ M2C_N	ADCB-DA0N
DP9_ M2C_P	<b>B4</b>	DP9_ M2C_P	ADCB-DA1P
DP9_ M2C_N	<b>B5</b>	DP9_ M2C_N	ADCB-DA1N
DP10_ M2C_P	<b>Y10</b>	DP10_ M2C_P	ADCB-DA2P
DP10_ M2C_N	<b>Y11</b>	DP10_ M2C_N	ADCB-DA2N
DP11_ M2C_P	<b>Z12</b>	DP11_ M2C_P	ADCB-DA3P
DP11_ M2C_N	<b>Y13</b>	DP11_ M2C_N	ADCB-DA3N
GBT Lanes			ADCB-Pin Signal Name
DP12_ M2C_P	<b>Y14</b>	DP12_ M2C_P	ADCB-DB0P
DP12_ M2C_N	<b>Y15</b>	DP12_ M2C_N	ADCB-DB0N
DP13_ M2C_P	<b>Z16</b>	DP13_ M2C_P	ADCB-DB1P
DP13_ M2C_N	<b>Z17</b>	DP13_ M2C_N	ADCB-DB1N
DP14_ M2C_P	<b>Y18</b>	DP14_ M2C_P	ADCB-DB2P
DP14_ M2C_N	<b>Y19</b>	DP14_ M2C_N	ADCB-DB2N
DP15_ M2C_P	<b>Y22</b>	DP15_ M2C_P	ADCB-DB3P
DP15_ M2C_N	<b>Y23</b>	DP15_ M2C_N	ADCB-DB3N
LVDS Signal Pairs			
LA00_P_CC	<b>G6</b>	BUF_EXT_TRIG_TO_FPGA_P	From external trigger to FPGA
LA00_N_CC	<b>G7</b>	BUF_EXT_TRIG_TO_FPGA_N	From external trigger to FPGA
LA01_P_CC	<b>D8</b>	FPGA_SYNC_OUT_P	From FPGA to clock tree Trigger Mux
LA01_N_CC	<b>D9</b>	FPGA_SYNC_OUT_N	From FPGA to clock tree Trigger Mux
LA02_P	<b>H7</b>	ADC0_ORA0	(input Ch 0) ADC0 Ch-A over-range 0 Output Level translate from P1P9VA to Vadj
LA02_N	<b>H8</b>	ADC0_ORA1	(input Ch 0) ADC0 Ch-A over-range 1 Output Level translate from P1P9VA to Vadj
LA03_P	<b>G9</b>	ADC0_ORB0	(input Ch 1) ADC0 Ch-B over-range 0 Output Level translate from P1P9VA to Vadj
LA03_N	<b>G10</b>	ADC0_ORB1	(input Ch 1) ADC0 Ch-B over-range 1 Output Level translate from P1P9VA to Vadj

AV57.4	Pin	FMC134 Signal	Notes
Clock Signal Name			
LA04_P	<b>H10</b>	ADC1_ORA0	(input Ch 2) ADC1 Ch-A over-range 0 Output Level translate from P1P9VA to Vadj
LA04_N	<b>H11</b>	ADC1_ORA1	(input Ch 2) ADC1 Ch-A over-range 1 Output Level translate from P1P9VA to Vadj
LA05_P	<b>D11</b>	ADC1_ORB0	(input Ch 3) ADC1 Ch A over-range 0 Output Level translate from P1P9VA to Vadj
LA05_N	<b>D12</b>	ADC1_ORB1	(input Ch 3) ADC1 Ch A over-range 1 Output Bidirectional level translator. Vadj to P1P9VA
LA06_P	<b>C10</b>	ADC0_NCOA0	(input Ch 0) ADC0 NCOA0 control input Level translate from Vadj to P1P9VA
LA06_N	<b>C11</b>	ADC0_NCOA1	(input Ch 0) ADC0 NCOA1 control input Level translate from Vadj to P1P9VA
LA07_P	<b>H13</b>	ADC0_NCOB0	(input Ch 1) ADC0 NCOB0 control input Level translate from Vadj to P1P9VA
LA07_N	<b>H14</b>	ADC0_NCOB1	(input Ch 1) ADC0 NCOB1 control input Level translate from Vadj to P1P9VA
LA08_P	<b>G12</b>	ADC1_NCOA0	(input Ch 2) ADC1 NCOA0 control input Level translate from Vadj to P1P9VA
LA08_N	<b>G13</b>	ADC1_NCOA1	(input Ch 2) ADC1 NCOA1 control input Level translate from Vadj to P1P9VA
LA09_P	<b>D14</b>	ADC1_NCOB0	(input Ch 3) ADC1 NCOB0 control input Level translate from Vadj to P1P9VA
LA09_N	<b>D15</b>	ADC1_NCOB1	(input Ch 3) ADC1 NCOB1 control input Level translate from Vadj to P1P9VA
LA10_P	<b>C14</b>	FMC_CPLD_CTRL0_VADJ	CPLD Control Signal, Bidirectional level translate Vadj to P1P9VA (TXB0304RUTR)
LA10_N	<b>G15</b>	FMC_CPLD_CTRL1_VADJ	CPLD Control Signal, Bidirectional level translate Vadj to P1P9VA
LA11_P	<b>H16</b>	FMC_CPLD_CTRL2_VADJ	CPLD Control Signal, Bidirectional level translate Vadj to P1P9VA
LA11_N	<b>H17</b>	FMC_CPLD_CTRL3_VADJ	CPLD Control Signal, Bidirectional level translate Vadj to P1P9VA
LA12_P	<b>G15</b>	ADC0_SYNCSE_N	ADC0 Single Ended Sync Input low, level translate from Vadj to P1P9VA
LA12_N	<b>G16</b>	ADC1_SYNCSE_N	ADC1 Single Ended Sync Input low, level translate from Vadj to P1P9VA
LA13_P	<b>D17</b>	ADC0_CALSTAT	ADC0 Calibration or Alarm Status out, level translate from P1P9VA to Vadj

AV57.4	Pin	FMC134 Signal	Notes
Clock Signal Name			
LA13_N	<b>D18</b>	ADC1_CALSTAT	ADC0 Calibration or Alarm Status out, level translate from P1P9VA to Vadj
LA14_P	<b>C18</b>	FPGA_SYNC_OUT_TO_LMK	SYNC from FPGA to LMK, level translate from Vadj to 3P3V
LA14_N	<b>C19</b>	FIREFLY_INT	FIREFLY INTERRUPT to FPGA
GA0	<b>C34</b>	GA0_MOD_IN_3.3	Card Global Address 0 from mezzanine connector
GA1	<b>D35</b>	GA1_MOD_IN_3.3	Card Global Address 1 from mezzanine connector
PRSNT_M2C_L	<b>H2</b>	PRSNT_M2C_L	Tied to GND (FMC134 is present)
PG_M2C	<b>F1</b>	PG_M2C	Indicate FMC134 power good status to carrier
CLK_DIR	<b>B1</b>	CLK_DIR	Driven by mezzanine, pop option to tie high or low
<b>FMC134 Signals Exclusive to Carrier Card</b>			
GA0	<b>C34</b>	GA0_CC_OUT_3.3	Card Global Address 1 from CPLD to carrier connector
GA1	<b>D35</b>	GA0_CC_OUT_3.3	Card Global Address 1 from CPLD to carrier connector
PRSNT_M2C_L	<b>H2</b>	FMC_PRSNT_M2C_L_CARRIER	Indicates that a stacked card is present (from carrier connector to CPLD)
PG_M2C	<b>F1</b>	PG_M2C	Power good status from stacked card (from carrier connector to CPLD)
<b>FMC134 Signals Used that are also Passed Through to the Carrier Connector</b>			
TSRT_L	<b>D34</b>	TRST_L	JTAG Port (also passed through)
TCK	<b>D29</b>	TCK	JTAG Port (also passed through)
TMS	<b>D33</b>	TMS	JTAG Port (also passed through)
TDI	<b>D30</b>	TDI	JTAG Port (also passed through)
TDO	<b>D31</b>	TDO	JTAG Port (also passed through)
PG_C2M	<b>D1</b>	PG_C2M	Carrier power is OK (also passed through)
I2C_SCL	<b>C30</b>	I2C_SCL	I <sup>2</sup> C Bus Clock (also passed through)
I2C_SDA	<b>C31</b>	I2C_SDA	I <sup>2</sup> C Bus Data (also passed through)
RES0	<b>B40</b>	RES0	System Reset (also passed through)
RES1	<b>L1</b>	RES1	System Reset (also passed through)

# B • FMC134 Mezzanine to Carrier Connector Mapping

Carrier Connector (Stacked FMC)	Pin	Mezzanine Signal (FMC134)	Pin	Notes
<b>These are Mezzanine Signals that are Re-Mapped to the Carrier Connector</b>				
Clock Signal Name				
CLK0_M2C_P	H4	CLK2_BIDR_P	K4	D-Clock
CLK0_M2C_N	H5	CLK2_BIDR_N	K5	D-Clock
CLK1_M2C_P	G2	CLK3_BIDR_P	J2	S-Clock
CLK1_M2C_N	G3	CLK3_BIDR_N	J3	S-Clock
GBTCLK0_M2C_P	D4	GBTCLK4_M2C_P	L4	D-Clock Quad 0
GBTCLK0_M2C_P	D5	GBTCLK4_M2C_P	L5	D-Clock
GBTCLK1_M2C_P	B20	GBTCLK5_M2C_P	Z20	D-Clock Quad 1
GBTCLK1_M2C_P	B21	GBTCLK5_M2C_P	Z21	D-Clock
GBT Lanes				
DP0_M2C_P	C6	DP16_M2C_P	Z32	ADCA-DA0P
DP0_M2C_N	C7	DP16_M2C_N	Z33	ADCA-DA0N
DP1_M2C_P	A2	DP17_M2C_P	Y34	ADCA-DA1P
DP1_M2C_N	A3	DP17_M2C_N	Y35	ADCA-DA1N
DP2_M2C_P	A6	DP18_M2C_P	Z36	ADCA-DA2P
DP2_M2C_N	A7	DP18_M2C_N	Z37	ADCA-DA2N
DP3_M2C_P	A10	DP19_M2C_P	Y38	ADCA-DA3P
DP3_M2C_N	A11	DP19_M2C_N	Y39	ADCA-DA3N
GBT Lanes		GBT Lanes		
DP4_M2C_P	A14	DP20_M2C_P	M14	ADCA-DB0P
DP4_M2C_N	A15	DP20_M2C_N	M15	ADCA-DB0N
DP5_M2C_P	A18	DP21_M2C_P	M10	ADCA-DB1P
DP5_M2C_N	A19	DP21_M2C_N	M11	ADCA-DB1N
DP6_M2C_P	B16	DP22_M2C_P	M6	ADCA-DB2P
DP6_M2C_N	B17	DP22_M2C_N	M7	ADCA-DB2N
DP7_M2C_P	B12	DP23_M2C_P	M2	ADCA-DB3P
DP7_M2C_N	B13	DP23_M2C_N	M3	ADCA-DB3N
LVDS Signal Pairs		Mezzanine Signal name		Stacked FMC134 Function
LA00_P_CC	G6	LA15_P	H19	BUF_EXT_TRIG_TO_FPGA_P
LA00_N_CC	G7	LA15_N	H20	BUF_EXT_TRIG_TO_FPGA_N
LA01_P_CC	D8	LA16_P	G18	FPGA_SYNC_OUT_P
LA01_N_CC	D9	LA16_N	G19	FPGA_SYNC_OUT_N
LA02_P	H7	LA17_P	D20	ADC0_ORA0

Carrier Connector (Stacked FMC)	Pin	Mezzanine Signal (FMC134)	Pin	Notes
LA02_N	<b>H8</b>	LA17_N	D21	ADC0_ORA1
LA03_P	<b>G9</b>	LA18_P	C22	ADC0_ORB0
LA03_N	<b>G10</b>	LA18_N	C23	ADC0_ORB1
LA04_P	<b>H10</b>	LA19_P	H22	ADC1_ORA0
LA04_N	<b>H11</b>	LA19_N	H23	ADC1_ORA1
LA05_P	<b>D11</b>	LA20_P	G21	ADC1_ORB0
LA05_N	<b>D12</b>	LA20_N	G22	ADC1_ORB1
LVDS Signal Pairs		Mezzanine Signal name		Stacked FMC134 Function
LA06_P	<b>C10</b>	LA21_P	H25	ADC0_NCOA0
LA06_N	<b>C11</b>	LA21_N	H26	ADC0_NCOA1
LA07_P	<b>H13</b>	LA22_P	G24	ADC0_NCOB0
LA07_N	<b>H14</b>	LA22_N	G25	ADC0_NCOB1
LVDS Signal Pairs		Mezzanine Signal name		Stacked FMC134 Function
LA08_P	<b>G12</b>	LA23_P	D23	ADC1_NCOA0
LA08_N	<b>G13</b>	LA23_N	D24	ADC1_NCOA1
LA09_P	<b>D14</b>	LA24_P	H28	ADC1_NCOB0
LA09_N	<b>D15</b>	LA24_N	H29	ADC1_NCOB1
LVDS Signal Pairs		Mezzanine Signal name		Stacked FMC134 Function
LA10_P	<b>C14</b>	LA25_P	G27	FMC_CPLD_CTRL0_VADJ
LA10_N	<b>C15</b>	LA25_N	G28	FMC_CPLD_CTRL1_VADJ
LA11_P	<b>H16</b>	LA26_P	D26	FMC_CPLD_CTRL2_VADJ
LA11_N	<b>H17</b>	LA26_N	D27	FMC_CPLD_CTRL3_VADJ
LVDS Signal Pairs		Mezzanine Signal name		Stacked FMC134 Function
LA12_P	<b>G15</b>	LA27_P	C26	ADC0_SYNCSE_N
LA12_N	<b>G16</b>	LA27_N	C27	ADC1_SYNCSE_N
LA13_P	<b>D17</b>	LA28_P	H31	ADC0_CALSTAT
LA13_N	<b>D18</b>	LA28_N	H32	ADC1_CALSTAT
LVDS Signal Pairs		Mezzanine Signal name		Stacked FMC134 Function
LA14_P	<b>C18</b>	LA29_P	G30	FPGA_SYNC_OUT_TO_LMK
LA14_N	<b>C19</b>	LA29_N	G31	FIREFLY_INT
LA15_P	<b>H19</b>	LA30_P	H34	
LA15_N	<b>H20</b>	LA30_N	H35	
LVDS Signal Pairs		Mezzanine Signal name		Stacked FMC134 Function
LA16_P	<b>G18</b>	LA31_P	G33	
LA16_N	<b>G19</b>	LA31_N	G34	
LA17_P	<b>D20</b>	LA32_P	H37	
LA17_N	<b>D21</b>	LA32_N	H38	
LA18_P	<b>C22</b>	LA33_P	G36	
LA18_N	<b>C23</b>	LA33_N	G37	

Carrier Connector (Stacked FMC)	Pin	Mezzanine Signal (FMC134)	Pin	Notes
LA19_P	H22	HA00_P	F4	
LA19_N	H23	HA00_N	F5	
<b>Additional HAxx_P/N pairs are sequentially mapped up to LA33_P/N</b>				

# C • FMC134 HSPCe Connector to Carrier Connector Mapping

Carrier Signal (Stacked FMC)	Pin	HSPCe Signal (FMC134)	Pin	Notes
GBTCLK2_M2C_P	L12	GBTCLK6_M2C_P	A1	D-Clock Quad 2
GBTCLK2_M2C_P	L13	GBTCLK6_M2C_P	A2	D-Clock
GBTCLK3_M2C_P	L8	GBTCLK7_M2C_P	X19	D-Clock Quad 3
GBTCLK3_M2C_P	L9	GBTCLK7_M2C_P	X20	D-Clock
GBT Lanes		GBT Lanes		ADCB-Pin Signal Name
DP8_M2C_P	B8	DP24_M2C_P	X3	ADCB-DA0P
DP8_M2C_N	B9	DP24_M2C_N	X4	ADCB-DA0N
DP9_M2C_P	B4	DP25_M2C_P	Y5	ADCB-DA1P
DP9_M2C_N	B5	DP25_M2C_N	Y6	ADCB-DA1N
DP10_M2C_P	Y10	DP26_M2C_P	X7	ADCB-DA2P
DP10_M2C_N	Y11	DP26_M2C_N	X8	ADCB-DA2N
DP11_M2C_P	Z12	DP27_M2C_P	Y9	ADCB-DA3P
DP11_M2C_N	Z13	DP27_M2C_N	Y10	ADCB-DA3N
GBT Lanes		GBT Lanes		ADCB-Pin Signal Name
DP12_M2C_P	Y14	DP28_M2C_P	X11	ADCB-DB0P
DP12_M2C_N	Y15	DP28_M2C_N	X12	ADCB-DB0N
DP13_M2C_P	Z16	DP29_M2C_P	Y13	ADCB-DB1P
DP13_M2C_N	Z17	DP29_M2C_N	Y14	ADCB-DB1N
DP14_M2C_P	Y18	DP30_M2C_P	X15	ADCB-DB2P
DP14_M2C_N	Y19	DP30_M2C_N	X16	ADCB-DB2N
DP15_M2C_P	Y22	DP31_M2C_P	Y17	ADCB-DB3P
DP15_M2C_N	Y23	DP31_M2C_N	Y18	ADCB-DB3N

# D • FMC134 Firefly Interface to Carrier Connector Mapping

Carrier Signal (Stacked FMC)	Pin	Firefly ECUO TX Connector Signal Name	Pin	Notes
GBT Lanes		Firefly Signal Pairs		
DP8_M2C_P	B8	DP8_M2C_P	18B	ADCB-DA0P
DP8_M2C_N	B9	DP8_M2C_N	17B	ADCB-DA0N
DP9_M2C_P	B4	DP9_M2C_P	18A	ADCB-DA1P
DP9_M2C_N	B5	DP9_M2C_N	18B	ADCB-DA1N
DP10_M2C_P	Y10	DP10_M2C_P	15B	ADCB-DA2P
DP10_M2C_N	Y11	DP10_M2C_N	14B	ADCB-DA2N
DP11_M2C_P	Z12	DP11_M2C_P	15A	ADCB-DA3P
DP11_M2C_N	Z13	DP11_M2C_N	15B	ADCB-DA3N
GBT Lanes		Firefly Signal Pairs		
DP12_M2C_P	Y14	TX4_P	12B	ADCB-DB0P
DP12_M2C_N	Y15	TX4_N	11B	ADCB-DB0N
DP13_M2C_P	Z16	TX5_P	12A	ADCB-DB1P
DP13_M2C_N	Z17	TX5_N	11A	ADCB-DB1N
DP14_M2C_P	Y18	TX6_p	9B	ADCB-DB2P
DP14_M2C_N	Y19	TX6_N	8B	ADCB-DB2N
DP15_M2C_P	Y22	TX7_P	9A	ADCB-DB3P
DP15_M2C_N	Y23	TX7_N	8A	ADCB-DB3N
GBT Clock		Firefly Signal Pairs		
		TX8_P	6B	Not used, DC biased and terminated
		TX8_N	5B	Not used, DC biased and terminated
		TX9_P	6A	Not used, DC biased and terminated
		TX9_N	5A	Not used, DC biased and terminated
GBTCLK2_M2C_P	L12	TX10_P	3B	D-Clock Quad 2
GBTCLK2_M2C_P	L13	TX10_N	2B	D-Clock
GBTCLK3_M2C_P	L8	TX11_N	3A	D-Clock Quad 3
GBTCLK3_M2C_P	L9	TX11_P	3B	D-Clock

# Glossary

<b>EEPROM</b>	Electronically Erasable Programmable Read Only Memory
<b>FMC</b>	FPGA Mezzanine Card
<b>FPGA</b>	Field Programmable Gate Array
<b>JTAG</b>	Joint Test Action Group
<b>LDO</b>	Low Dropout (regulator)
<b>LED</b>	Light Emitting Diode
<b>LMK</b>	Refers to LMK04832/LMK04828B
<b>LMX</b>	Refers to LMX2581
<b>LSB</b>	Least Significant Bit(s)
<b>LVDS</b>	Low Voltage Differential Signaling
<b>LVPECL</b>	Low Voltage Positive Emitter Coupled Logic
<b>LVTTL</b>	Low Voltage Transistor Logic Level
<b>MGT</b>	Multi-Gigabit Transceiver
<b>MSB</b>	Most Significant Bit(s)
<b>PCB</b>	Printed Circuit Board
<b>PDF</b>	Phase Detector Frequency
<b>PLL</b>	Phase Lock Loop
<b>PMC</b>	PCI Mezzanine Card
<b>PSRR</b>	Power Supply Rejection Ratio
<b>TTL</b>	Transistor Logic Level

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