Hardware Reference Manual

FMC172 Digital-to-Analog Daughter Card

THE FM172 IS DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTIONS OF HAZARDOUS SUBSTANCE (ROHS) DIRECTIVE (2015/863) CURRENT REVISION.

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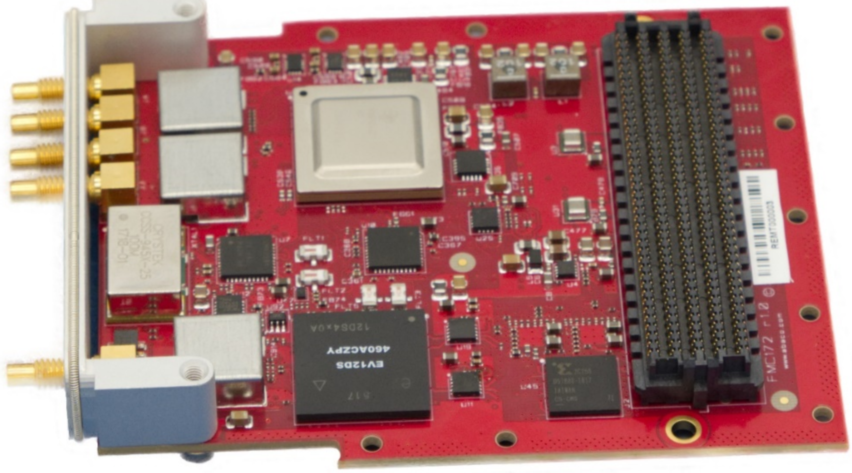

abaco SYSTEMS

Document History

Revision	Date	Changes	Author	Peer Review	Quality Approval
r1.0	2019/10/03	Initial Release	CNS	RTM/ANe	Pko

Waste Electrical and Electronic Equipment (WEEE) Returns

Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

About This Manual

Conventions

Notices

This manual may use the following types of notice:

WARNING
Warnings alert you to the risk of severe personal injury.

CAUTION
Cautions alert you to system danger or loss of data.

NOTE
Notes call attention to important features or instructions.

TIP
Tips give guidance on procedures that may be tackled in a number of ways.

LINK
Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a "D" subscript and binary numbers have a "b" subscript. The prefix "0x" shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers "k", "M" and "G" have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$, respectively, and can be used to define a transfer rate. The only exception to this is in the description of the size of memory areas, when "K", "M" and "G" mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with "#" denote active low signals; all other signals are active high. "N" and "P" denote the low and high components of a differential signal respectively.

Further Information

Abaco Website

You can find information regarding Abaco products on the following website:

LINK
https://www.abaco.com/products

Third-party Documents

- ANSI/VITA 57.1-2010, FPGA Mezzanine Card (FMC) Standard

LINK
https://www.vita.com

- Datasheet ADC12DL3200, 12bit 5.4GSPS Analog to Digital Converter
- Datasheet LMX2594, RF Synthesizer with Integrated VCO

LINK
https://www.ti.com

- Datasheet AD7291, 8 - Channel I^2C 12Bit SAR ADC with Temp Sensor

LINK
https://www.analog.com

- Datasheet EV12DS460A Low Power 12-bit Digital to Analog Converter with 4/2:1 Multiplexer

LINK
https://www.teledyne-e2v.com

NOTE
Technical literature describing components used on the FMC172 is available from the manufacturers' websites.

Technical Support Contact Information

You can find technical assistance contact details on the website Support page.

LINK
https://www.abaco.com/support

Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:

LINK
support@abaco.com

Returns

If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Support page.

LINK
https://www.abaco.com/support

Do not return products without first contacting the Abaco Repairs facility.

EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

Safety

This module presents no hazard to the user.

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1 • General Description

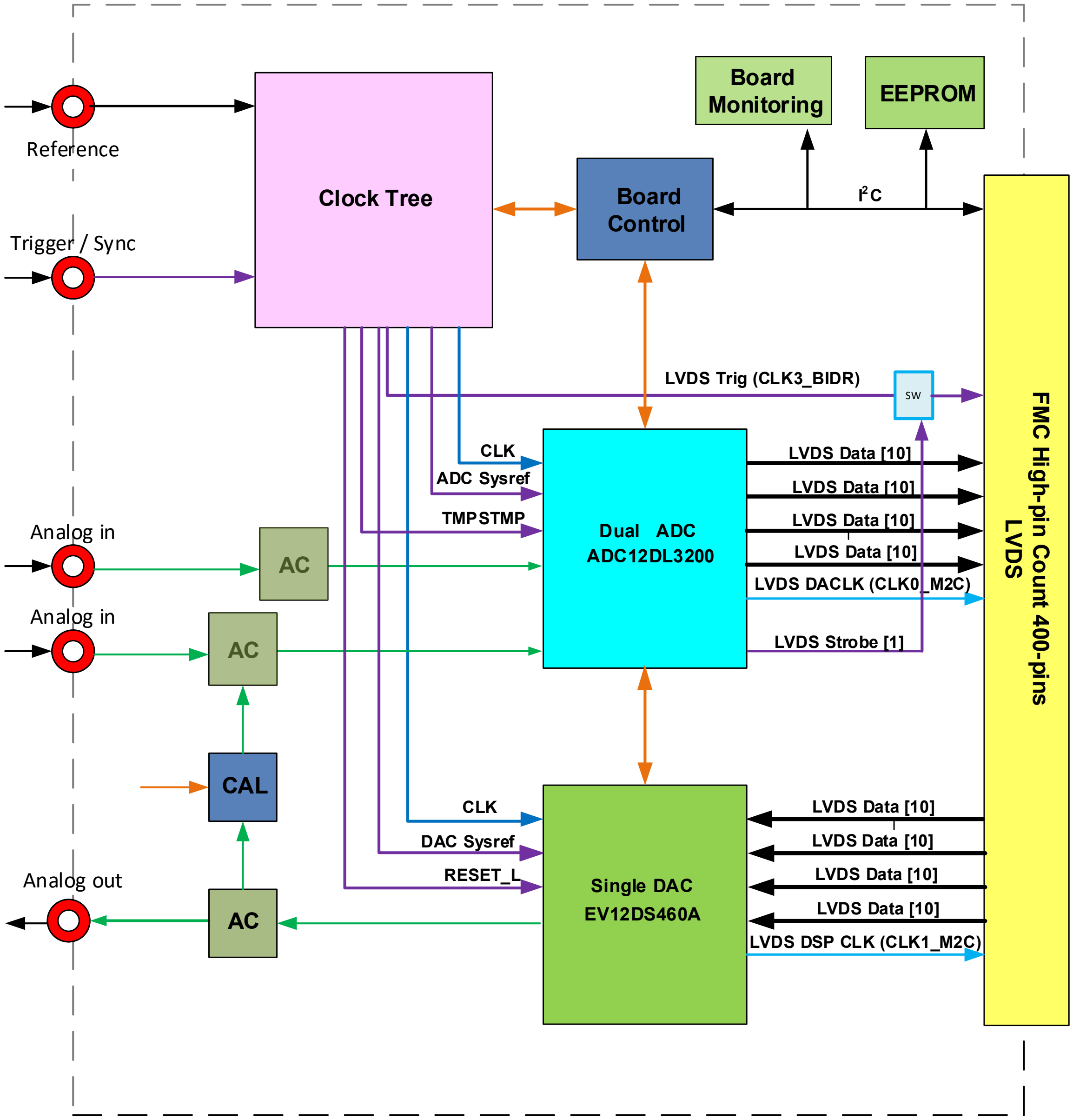
The FMC172 is a single channel 6.4GSPS ADC and 6.0GSPS DAC FMC daughter card. The sample clock is supplied by an internal clock source (optionally locked to an external reference). A trigger input for external synchronization and customized sampling control is available.

The FMC172 daughter card is mechanically and electrically compliant to FMC standard (ANSI/VITA 57.1). The card has a high-pin count connector, front panel I/O, and can be used in a conduction cooled environment.

The design is based on TI's 12-bit ADC12DL3200 ADC and E2V's 12-bit EV12DS460AZP DAC. Due to FMC pin limitations, only 10 bits are used on both converters. The analog input and output signals are available on the front panel on coax connections. The ADC and DAC have individual calibration circuits for fine-tuning of gain, offset, and phase.

The FMC172 allows flexible control on sampling frequency, and calibration through serial I²C communication. Furthermore, the card is equipped with power supply and temperature monitoring via I²C. A high-level block diagram of the FMC172 is shown in Figure 1-1.

Figure 1-1 FMC172 Block Diagram



2 • Installation

2.1 Installation and Handling Instructions

- Prevent electrostatic discharges by observing ESD precautions when handling the card.
- Do not flex the card and do not exceed 2.0 in-lbs on the coax connectors.
- The FMC172 card must be installed on a carrier card compliant to the FMC standard.
- The FMC172 card can support VADJ/VIO_B voltage range of 1.65V to 3.3V.
- The FMC172 is designed to be operated in continuously cooled environment, operation without sufficient cooling for any length of time may damage the device and void the warranty.

2.2 LVDS Requirements

The FMC172 features parallel DDR LVDS inputs and outputs. The DAC has four 10-bit buses running at a maximum of 1.5 Gbit/s. The ADC has four 10-bit buses running at a maximum of 1.6 Gbit/s. The ADC can output a training pattern on the LVDS outputs to enable phase alignment on the carrier card. The ADC and DAC also both provide a DDR clock synchronous with the data words.

2.3 Cabling

Quality coax cables are critical to achieving optimal performance. Mating cables can be ordered online from typical vendors such as Fairview Microwave and Pasternack. Shown below are three examples of a typical 12" long SSMC plug to SMA-male cable.

This is in no way an endorsement of a particular vendor, simply a list of cables that we have used in house in the past.

- Fairview Microwave # FMCA1508-12 (FM-SR086TBJ Coax)
- Fairview Microwave # FMC0234315-12 (RG316 Coax)
- Pasternack # PE3C4422-12 (LMR-100 Coax)
- Pasternack # PE3C4444-12 (SR405 Coax)

For DAC to ADC Loopback a SSMC plug to SSMC plug cable would be used. An example of this is the Pasternack # PE3C4441-6

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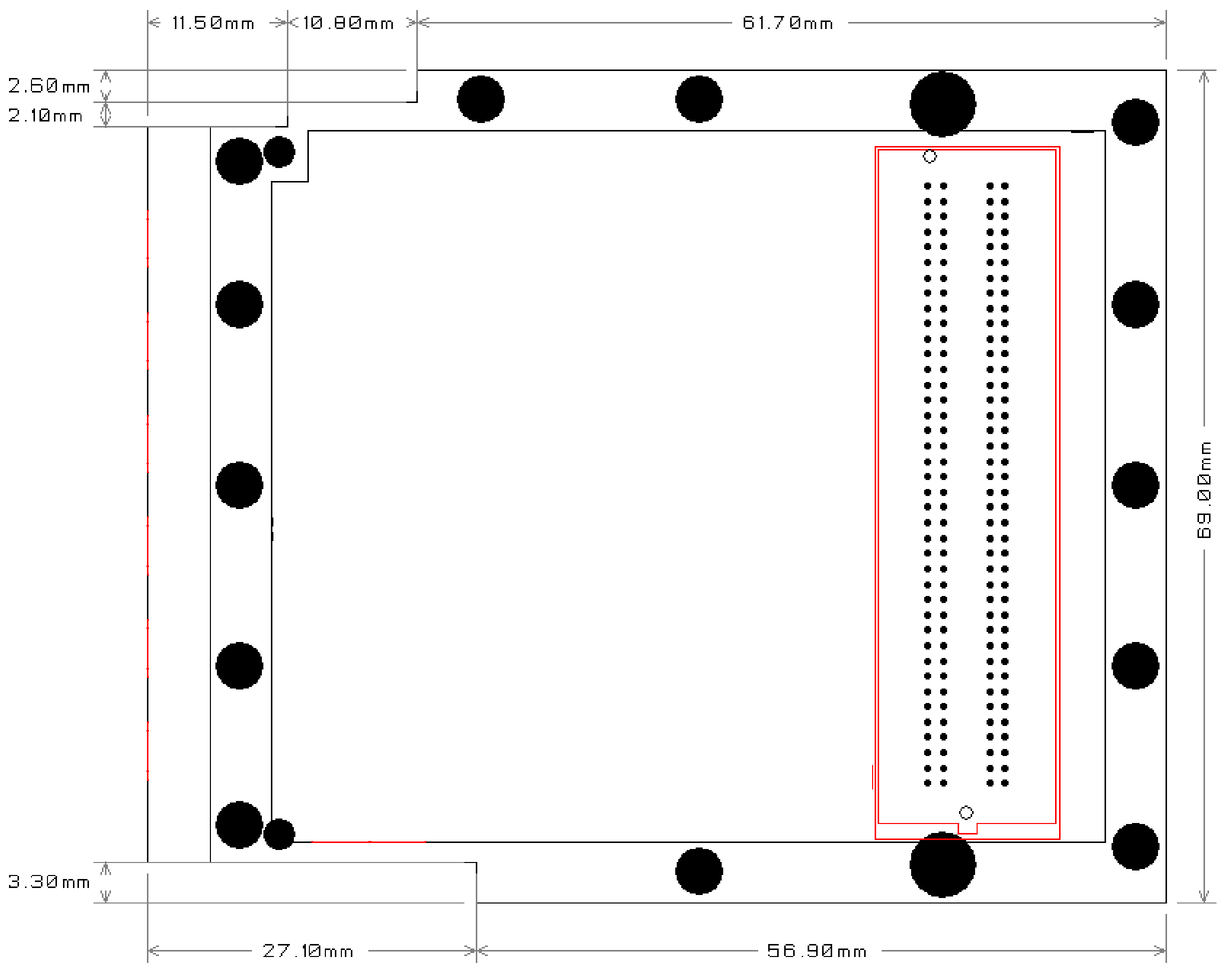
3 • Design

3.1 Physical Specifications

3.1.1 Board Dimensions

The FMC172 card complies with the FMC standard known as VITA 57.1. The card is a single width conduction cooled mezzanine module (with region 1 and front panel I/O). The front Bezel contains five coaxial I/O signals. The stacking height is 10mm and the maximum component height on the bottom layer is 1.3mm. The general outline of the board is shown below in Figure 3-1.

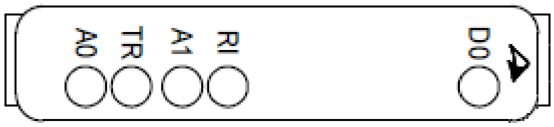
Figure 3-1 FMC172 Dimensions



3.1.2 Front Panel Connectors

The front panel of the FMC172 contains five connectors as shown below, the hole spacing is designed to optimize signal routing path between the analog input/output connectors, the balun, and the ADC input and DAC output. By default, the board is populated with five SSMC connectors.

Figure 3-2 Bezel



The text on the bezel is expanded as follows:

TR Trigger Input

A0 ADC Input 0

A1 ADC Input 1

RI Reference Input

D0 DAC Output

3.2 Main Characteristics

Table 3-1 FMC172 Daughter Card Main Characteristics

FMC172 Main Characteristics	
Analog Inputs (A0, A1)	
Number of channels	2
Channel resolution	10 bits
Input voltage range normal	ADC FS max 2.83 Vp-p +13 dBm @ 500 MHz (max) ADC FS min 1.42 Vp-p +7 dBm @ 500 MHz (min)
Input impedance	50 Ω Single ended
Analog input bandwidth	3 dB BW: 2 MHz to 8000 MHz typical Amplitudes referenced to a 100 MHz input signal at 0 dBm
SFDR	Ain = -1 dBFS, foreground calibration Fin = 347 MHz, -55 dBFS Typ. Fin = 997 MHz, -55 dBFS Typ. Fin = 2482 MHz, -52 dBFS Typ. Fin = 4997 MHz, -49 dBFS Typ. Fin = 6397 MHz, -47 dBFS Typ. Fin = 8197 MHz, -46 dBFS Typ.
Sampling frequency range	1.6 to 6400 GSPS Single channel mode 800 to 3200 MSPS Dual channel mode
Data width	4 x 10 LVDS lanes at 1.6 Gbit/s max
Data format	Offset binary (default) or 2's complement
Analog Output (DO)	
Number of channels	1
Channel resolution	10 bits
Output voltage range	0.45 Vp-p / -3.0 dBm into 50 Ω at 500 MHz typ. in NRZ mode
Output impedance	50 Ω Single ended
Analog output bandwidth	DAC 3dB BW: 2 MHz to 7.5 GHz in addition to sinc roll-off
SFDR	Typical values at 0 dBFS output in NRZ mode: 101 MHz: 67dB 1551 MHz: 57dB 2951 MHz: 50dB
Sampling frequency range	~100 to 6000 MHz using onboard PLL
Data width	4 x 10 LVDS lanes at 1.5 Gbit/s max
Data Format	Offset binary
External Reference Input (RI)	
Frequency range	5 to 100 MHz

FMC172 Main Characteristics	
Input amplitude	-3 to +10 dBm/ ~0.45 to 2.0 Vp-p AC coupled into 50 Ω Recommended input: +10 dBm / 2.0 Vp-p @ 100 MHz Phase noise improves with increasing input level Max +11 dBm @ 100 MHz Nominal PFD is 100 MHz
External Trigger / Timestamp Input (TI)	
Trigger input signal	LVPECL compatible input, 1.8V threshold voltage, DC coupled into 50 Ω
Input impedance	50 Ω
Trigger frequency range	Up to 2 GHz using single ended 50-Ω LVPECL levels
Latency	
ADC input to DAC output	17.2 ns typ. Signal is inputted to the ADC, looped back through a PC820 carrier board and outputted through the DAC. Result includes delay through PC820 carrier.

3.3 Electrical Specifications

The ADC uses 40 (4x10) LVDS lanes operating at a maximum rate of 1.6 GSPS. The DAC uses 40 (4x10) LVDS lanes operating at a maximum rate of 1.5 GSPS.

All control signals are via the I²C bus through the CPLD acting as an I²C to SPI bridge.

A VADJ range of 1.65V to 3.3V is supported. The voltage on the VIO_B pins will follow the voltage on VADJ. All CLK pins are LVDS per the FMC standard.

3.3.1 EEPROM

The FMC172 card carries a 2 Kbit EEPROM (M24C02-RMC6TG) which is accessible from the carrier card through the I²C bus. The EEPROM is powered by 3P3VAUX. The standby current is only 0.01µA when SCL and SDA are kept at 3P3VAUX level. Onboard pull-up resistors allow these signals to be left floating. The EEPROM is write-protected. The EEPROM directly faces the I²C bus, all other devices are on the isolated side of an PCA9517A I²C bus repeater.

3.3.2 FMC Mezzanine Connector

The recommendations from AV57.1 Table 14 have been considered.

- The ADC DACLK is mapped to CLK0_M2C
- The DAC DSP Clock Output signal is mapped to CLK1_M2C
- CLK2_M2C not used, can be left floating
- The trigger signal to the FPGA logic is mapped to CLK3_BIDR

Table 3-2 HPC Signal Utilization

# LVDS Clock Pairs	# LVDS Data Pairs	# Clock Pairs	#GBT Data Pairs M2C	#GBT Data Pairs C2M
CLK0_M2C – ADC DDACLK output		1		
CLK1_M2C – DAC DSP CLK output		1		
CLK3_BIDR – Trigger to FPGA		1		
ADC Data Pairs	40			
DAC Data Pairs	40			

3.3.3 ADC Data Pair Mapping

The ADC is used in its default 12-bit mode, but only the upper 10 bits of the ADC's 12-bit data bus, D11 through D2 are mapped to the LVDS lanes on the respective half of the connector.

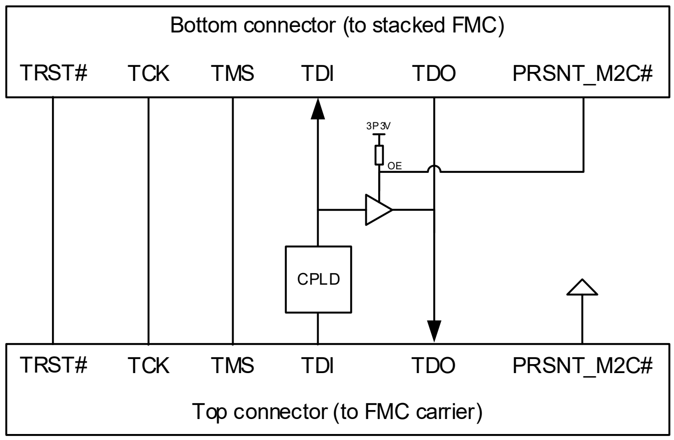
3.3.4 DAC Data Pair Mapping

The upper 10 bits of the DAC's 12-bit data bus, D11 through D2 are mapped to the LVDS lanes on the respective half of the connector.

3.3.5 JTAG Chain

In a stacked environment, the TDI pin will be decoupled from the TDO pin by the PRST_M2C# signal coming from the bottom connector. TRST#, TCK, TMS, TDI and TDO are directly connected between top to bottom connector on the FMC172.

Figure 3-3 JTAG Connection



4 • Analog Inputs

4.1.1 AC Coupling

The FMC172 uses transformer / balun coupling for single-ended to differential conversion. The analog input is AC-coupled at the connector to limit DC biasing of the transformer.

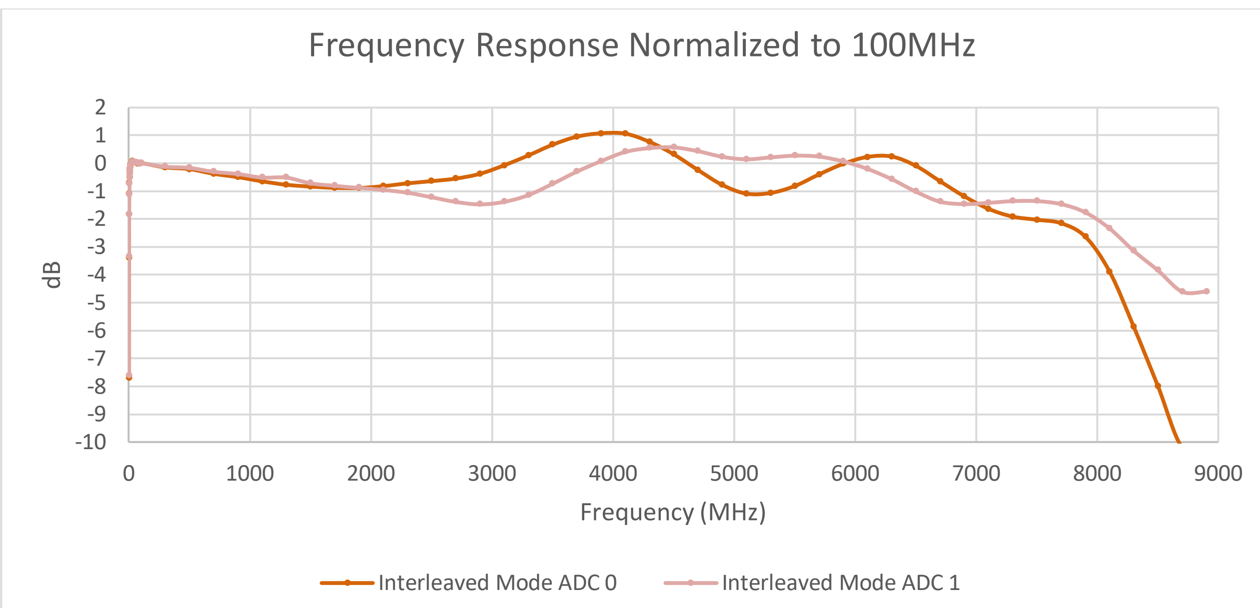
4.1.2 Full Scale Adjustment

Input full-scale voltage adjustment is available by adjusting the FS_RANGE_A and FS_RANGE_B registers in the ADCs. The default value is 0xA000 which provides a nominal full scale of +11dBm. A value of 0xFFF is used in Fmc172APP reference software, which results in a higher SNR and decreased SFDR. Refer to section 7.3.1.2 (Full-Scale Voltage Adjustment) of the TI ADC12DL3200 datasheet for details.

4.1.3 Typical Frequency Response

Below is a plot of the typical ADC response of each channel in interleaved mode. The 3dB roll-off is around 8 GHz.

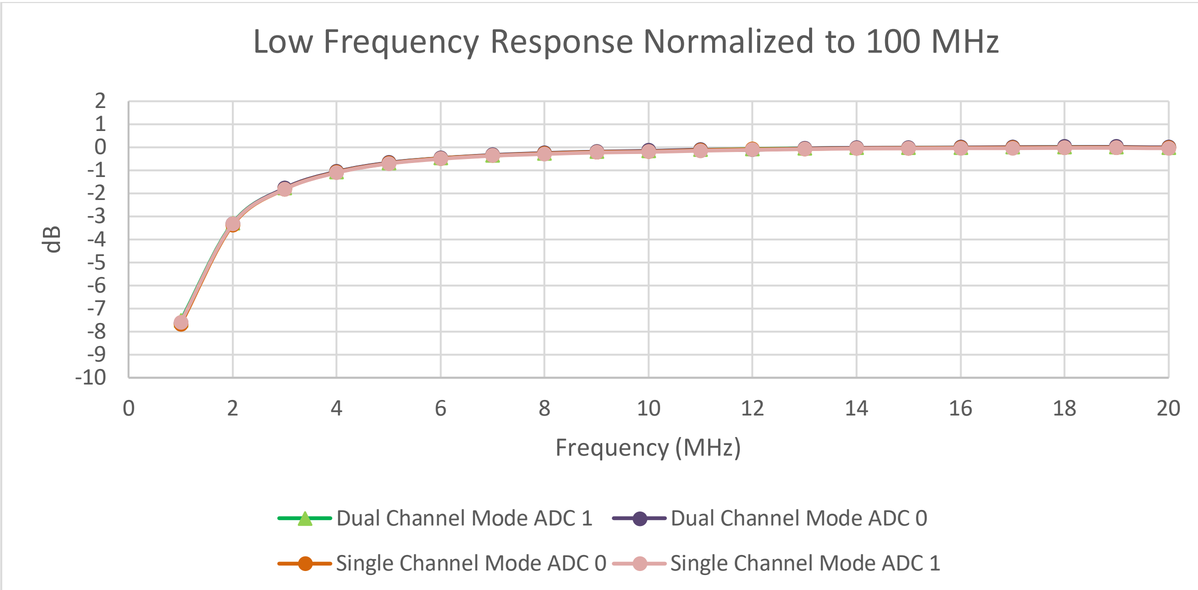
Figure 4-1 Normalized ADC Frequency Response



4.1.4 ADC Low Frequency Response

The typical Low frequency response of ADC is shown below. The -3dB point is around 2 MHz.

Figure 4-2 ADC Low Frequency Response

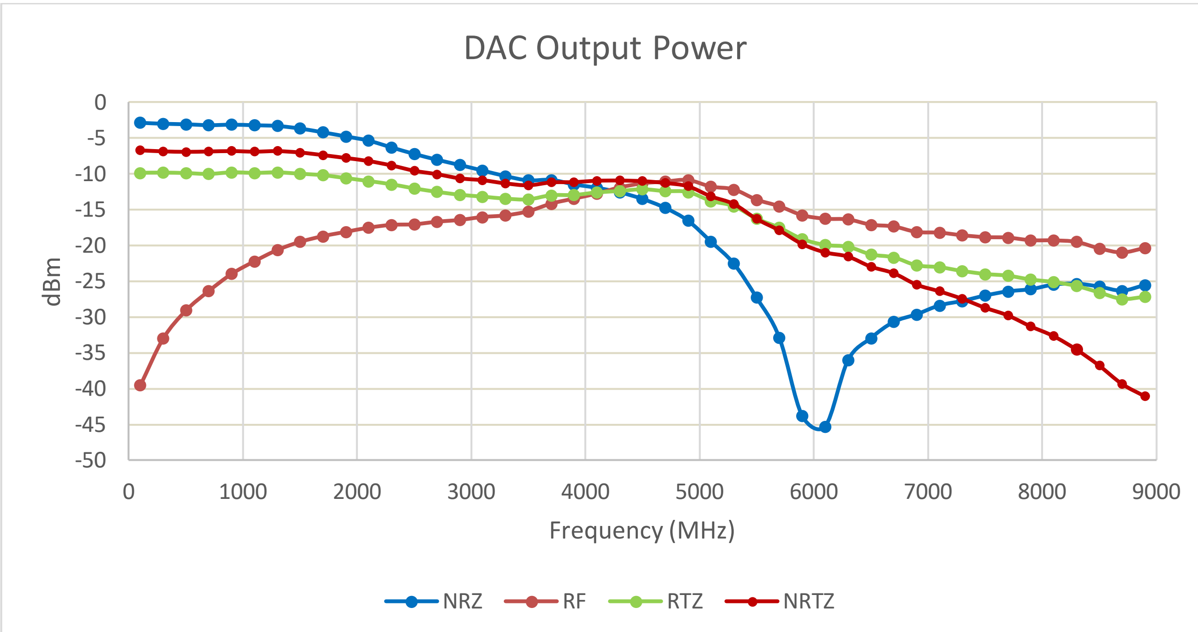


5 • Analog Output

5.1 DAC Power Out

Below is a plot of the typical DAC output power across frequency at 6 GSPS for the four output modes.

Figure 5-1 DAC Output Power



5.2 Analog Output Configuration

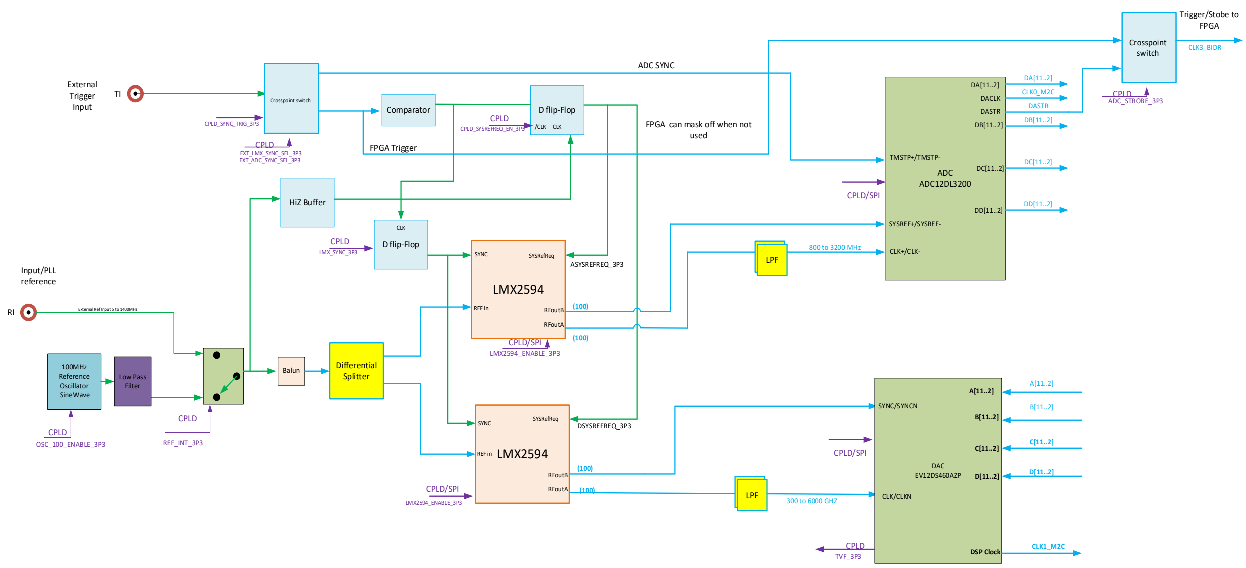
There are two RF switches and a calibration filter between the input connector and the output connector. This is used for adjusting the timing of the data lines to the DAC. See Section 6.6, "DAC – FPGA Synchronization". The switches are controlled by CPLD signals CAL_ENABLE_3P3 and CAL_DISABLE_3P3. For normal operation, the CAL_ENABLE_3P3 signal is set to a 0, and the CAL_DISABLE_3P3 signal is set to a 1.

6 • Clocking

The FMC172 ADC and DAC can be locked to either an onboard 100 MHz oscillator or an external reference source. Onboard reference signals are length matched to aide in synchronization.

A block diagram of the clocking scheme is shown below.

Figure 6-1 FMC172 Clocking Scheme



The sample clocks for the ADC and DAC are generated by their own TI LMX2594 PLL synthesizer. This allows the ADC and DAC to operate at different clock rates.

6.1 PLL 100 MHz Reference Oscillator

The FMC172 uses an ultra-low phase noise sinewave oscillator as its reference. When not used, this oscillator should be powered down by clearing the OSC_100_ENABLE bit in the CPLD to prevent any potential interference.

6.2 PLL External Reference

Per the TI datasheet, optimal performance of the LMX2594 PLL occurs with a PFD frequency of 200 MHz, the FMC172 external reference input will function with any frequency between 10 MHz and 100 MHz, operation below 10 MHz is possible with some degradation.

When using the external reference, the onboard 100 MHz oscillator should be powered down by clearing the CPLD bit OSC_100_ENABLE, and the external reference should be selected by setting the CPLD bit EXT_REF_ENABLE.

6.3 Internal Sample Clock

The FMC172 uses a Texas Instruments LMX2594 High Performance, Wideband N / Frac-N PLL Synthesizer with Integrated VCO to generate the sample clock. The CPLD bit ADC_LMX2594_EN and DAC_LMX2594_EN must be set to enable operation.

Frequency Ranges:
DAC: 300 to 6000 MHz
ADC: 800 to 3200 MHz

6.3.1 LMX2594 Clock Ranges

The upper frequency of the LMX2594 that supplies the DAC is limited by the DAC's maximum clock frequency of 6000 MHz. The upper frequency of the LMX2594 that supplies the ADC is limited by the ADC's maximum clock frequency of 3200 MHz. The lower frequency for the DAC is limited by the coupling capacitors to the DAC. (about 300 MHz) The lower frequency for the ADC is the ADCs minimum clock frequency of 800 MHz.

6.3.2 LMX2594 Noise Considerations with Internal Reference

For the FMC172, the best noise performance will occur when directly using the 100 MHz as the phase detector reference signal with the PLL in Integer-N mode. Lower PFDs will tend to be nosier and have the greatest impact on higher frequency input signals.

6.3.3 LMX2594 Noise Considerations with External Reference

The external reference input on the FMC172 goes to the LMX2594's reference input. This input has a bandwidth of 100 MHz and any additional noise on the external reference will translate to noise on the ADC and DAC signals. The use of a bandpass or low-pass filter on the external reference is strongly recommended. Optimum performance occurs with a PFD frequency of 100 MHz and when the reference frequency is an integer multiple of the PFD frequency. Any phase noise on the external reference signal will be multiplied up by 20log(Fout/Fref)

6.3.4 SYSREF Generation

A SYSREF signal is used to synchronize multiple DACs and ADCs. In order to meet setup and hold times for the ADC, a SYSREF calibration is performed as part of the synchronization process. For a detailed description of this calibration, see the ADC datasheet. The SYSREF signals for the ADC and DAC are each generated by their own LMX2594. The ADC LMX2594 sends continuous pulses to the ADC during the ADC's SYSREF calibration. It is then turned off once the ADC calibration is completed. The DAC LMX2594 simply sends a burst of pulses for synchronization.

The SYSREF pulses may be triggered internally by the CPLD or externally from the TR port. To trigger SYSREF internally, set the signal EXT_LMX_SYNC_SEL_3P3 to a

1 and CPLD_SYSREFREQ_EN_3P3 to a 1. Then set CPLD_SYNC_TRIG_3P3 to a 1 to generate the trigger by setting to a 1, then back to a 0.

To trigger SYSREF externally, the CPLD sets the signal EXT_LMX_SEL_3P3 to a 0 and CPLD_SYSREFREQ_EN_3P3 to a 1. Then send the send the trigger pulse to TR connector (see Table 6-3).

6.3.5 SYSREF Spur Considerations on the LMX2594

After the SYSREF calibration is complete and the SYSREF pulses have been sent, It is recommended to set the SYSREF divider to its maximum value. This is to minimize spurs from the SYSREF divider coupling into the sample clock line. This is recommended even if the LMX2594 output has been disabled.

6.3.6 ADC LMX2594 PLL Loop Filter Design

The loop filter for PLL1 is optimized for a PFD frequency of 100 MHz and a loop filter bandwidth of 379 kHz with a phase margin of 50°.

This gives an estimated jitter of ~58 fs in a 1 kHz to 20 MHz bandwidth, and a ~60 fs of jitter in a 1 Hz to 6400 MHz bandwidth

Using the clock doubler can drop the jitter to ~56 fs but won't allow use of the sync function.

6.3.7 Impact of PFD Frequency on Phase Noise and Loop Bandwidth

The table below shows the effect of changing PFD Frequency by either using the doubler or the reference divider.

Table 6-1 Effect of PFD Frequency on LMX Loop Filter Parameters

PFD Frequency (MHz)	Bandwidth (kHz)	Phase Margin (Deg.)	Phase Noise (fs)
100	379	51	60
50	216	65	73
10	47	82	193
1	5.1	68	1191

As would be expected, this shows that PLL performance is only optimized for a single PFD frequency and the effect of the reference noise being multiplied up by 20log(N).

6.3.8 DAC LMX2594 PLL Loop Filter Design

The default loop filter for PLL1 is optimized for a PFD frequency of 100 MHz and a loop filter bandwidth of 260 kHz and a phase margin of 56°.

This gives an estimated jitter of ~55 fs in a 1 kHz to 20 MHz bandwidth, and a ~56 fs of jitter in a 1 Hz to 6000 MHz bandwidth

Using the clock doubler can drop the jitter to ~51 fs but won't allow use of the sync function.

6.3.9 Impact of PFD on Phase Noise and Loop Bandwidth on DAC PLL

The table below shows the effect of changing PFD frequency by either using the doubler or the reference divider.

Table 6-2 Effect of PFD Frequency on LMX Loop Filter Parameters

PFD Frequency (MHz)	Bandwidth (kHz)	Phase Margin (Deg.)	Phase Noise (fs)
100	260	56	55
50	144	69	69
10	30	82	191
1	3.5	60	1145

As would be expected, this shows that PLL performance is only optimized for a single PFD frequency and the effect of the reference noise being multiplied up by 20log(N).

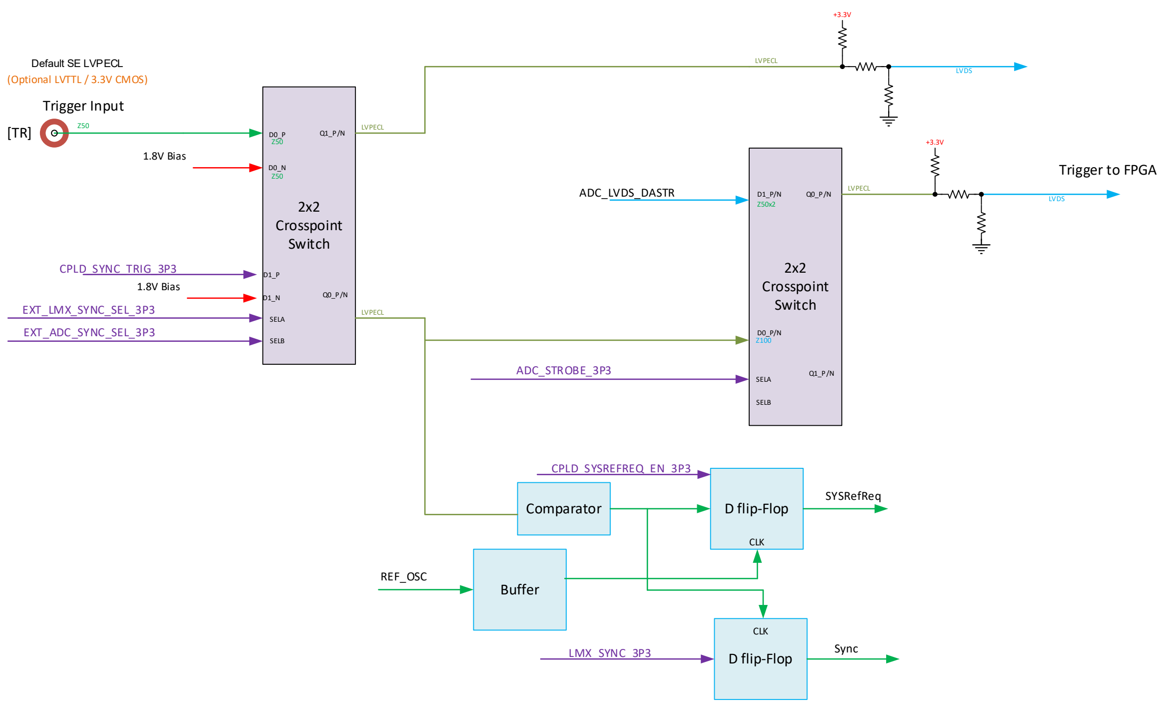
6.4 External Trigger/Synchronization Input

The FMC172 has an external single ended 50-Ω LVPECL trigger input which is converted to LVDS and can be distributed to the ADC, LMX PLLs, and FPGA, either individually or in combination by configuring the control signals listed in Table 6-3.

6.4.1 50-Ω LVPECL Sync /Trigger Signal Path Input

The trigger circuit uses two 2x2 cross point switches to route a SYNC / trigger signal from two possible sources (external and CPLD) to three possible destinations (FPGA trigger input, LMX PLLs, and ADC Timestamp). The external trigger input is biased at ~1.8V to support an LVPECL input. The LMX PLLs and the FPGA can mask off the line when not being used. The SysRefReq and Sync signals to the LMX PLLs are clocked in on the same reference clock used for the PLLs. The simplified block diagram below shows the trigger paths.

Figure 6-2 Trigger / Synchronization Signal Path



The Sync / Trigger source is selected by four bits in the CPLD as outlined in the table below.

Table 6-3 Sync / Trigger Control Bits

Trigger / Sync Source Selection Multiplexer Settings							
Function	External Trigger Input	CPLD_SYNC_TRIG_3P3	EXT_LMX_SYNC_SEL_3P3	EXT_ADC_SYNC_SEL_3P3	ADC_STROBE_3P3	CPLD_SYSREFREQ_EN_3P3	LMX_SYNC_3P3
Passive EXT Trigger	0	0	1	1	X	x	0
Passive CPLD	0	0	0	0	X	x	0
CPLD Syncs LMX Reference	0	2 Pulses	1	0	X	0	1 then 0
CPLD triggers SYSREF	0	Pulse	1	0	X	1	0
CPLD Triggers FPGA	0	Pulse	1	0	0	0	0
CPLD Timestamp ADC	0	Pulse	0	1	X	0	0
EXT Trigger Syncs LMX	2 Pulses	0	0	1	X	0	1 then 0
EXT Trigger SYSREF	Pulse	0	0	1	X	1	0
EXT Triggers FPGA	Pulse	0	0	1	0	0	0
EXT Timestamp ADC	Pulse	0	1	0	X	0	0
ADC Strobe triggers FPGA	X	X	X	X	1	0	0

6.5 ADC – DAC Phase Detector

The FMC172 has phase detector that outputs from 1.24V to 2.30V. This may be used to verify that the phase between the ADC and DAC clock outputs are deterministic.

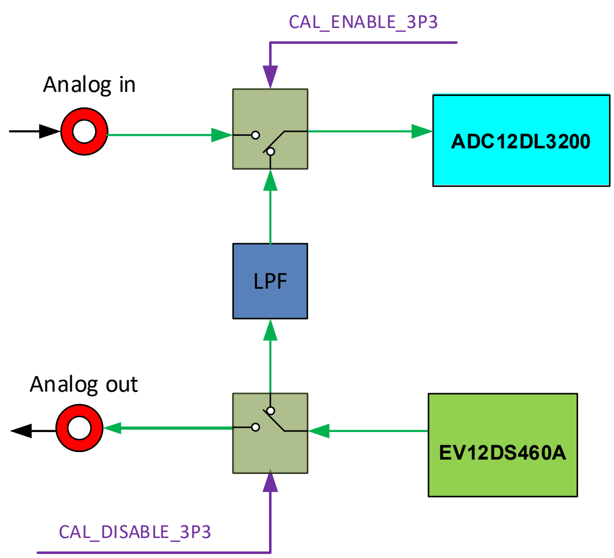
6.6 DAC – FPGA Synchronization

The DAC provides the DSP clock to the FPGA for the FPGA to clock the digital data at the DAC sample rate. However, due to the propagation delay to the FPGA and back to the DAC, the data will be delayed some amount that may violate system level timing requirements between the FPGA and DAC. The DAC is able to delay the DSP clock in relation to the sample clock (and by relation the clock/4 that clocks the data in) in 8 half sample clock increments. Please refer to the EV12DS460 datasheet for details. Additionally, the FPGA may have the ability to delay the data presented to the DAC in order to meet system level timing requirements.

6.6.1 Analog Calibration Path

The analog calibration path can be used to examine the output of the DAC. If the data is clocked in incorrectly, the DAC output can be examined by the ADC to help determine the cause. Figure 6-3 shows the DAC calibration path. To enable calibration, the CAL_ENABLE_3P3 signal is set to a 1, and the CAL_DISABLE_3P3 signal line is set to a 0. This sends the DAC output into the ADC input through a bandpass filter allowing the system to be calibrated.

Figure 6-3 DAC Calibration Path



6.7 Multiple Card Synchronization

For systems that use multi-board synchronization, care must be taken in the choice of sample clock frequencies. The LMX2594 has a minimum N divide value of 28. When the sync is enabled, an additional divide by 4 or divide by 6 is added inside the loop, making the divide by N smaller. This limits the max PFD frequency that can be used with synchronization enabled. This can be compensated by reducing the phase detector frequency at the expense of phase jitter performance. TI's design tool PLLatinum Sim can be used for estimating phase noise on the clocks.

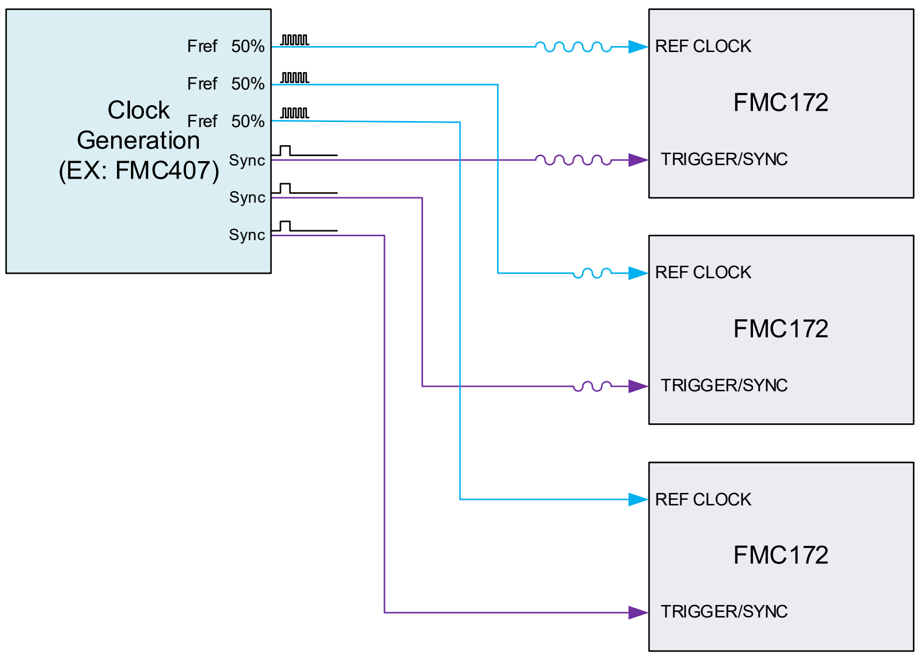
For synchronization to work across multiple cards, the cards need to be supplied with phase-matched reference signals. In addition, external synchronization pulses are required. Match the cable length between the clock/sync generator and each FMC172. With a 6GHz sample clock, a reference signal mismatch of 83ps will introduce an error in the synchronization of ½ of the sample clock. With LMR-100 cables, 83ps corresponds to approximately 16mm.

The clock generator needs to be able to tune the phase relationship between the clock and sync pulses to satisfy the setup/hold timing requirements. The sync pulse must occur no later than 2ns prior to the next rising edge of the reference clock. It is important that the clock can cleanly drive the 50-Ω cables used to connect to the FMC172 boards.

Close attention should be paid to the trigger signal and the trigger input impedance and best performance will be achieved when the trigger source, interconnect cable, and trigger input impedance are all 50Ω. Anything with a slower rise time than LVPECL will probably not work very well.

The reference clock should be as spectrally clean as possible. Any noise on the reference will degrade the performance of the FMC172. This is especially evident close in, at high input frequencies. The basic concept of clock and trigger distribution for multiple card synchronization is shown below.

Figure 6-4 Synchronizing Multiple Cards

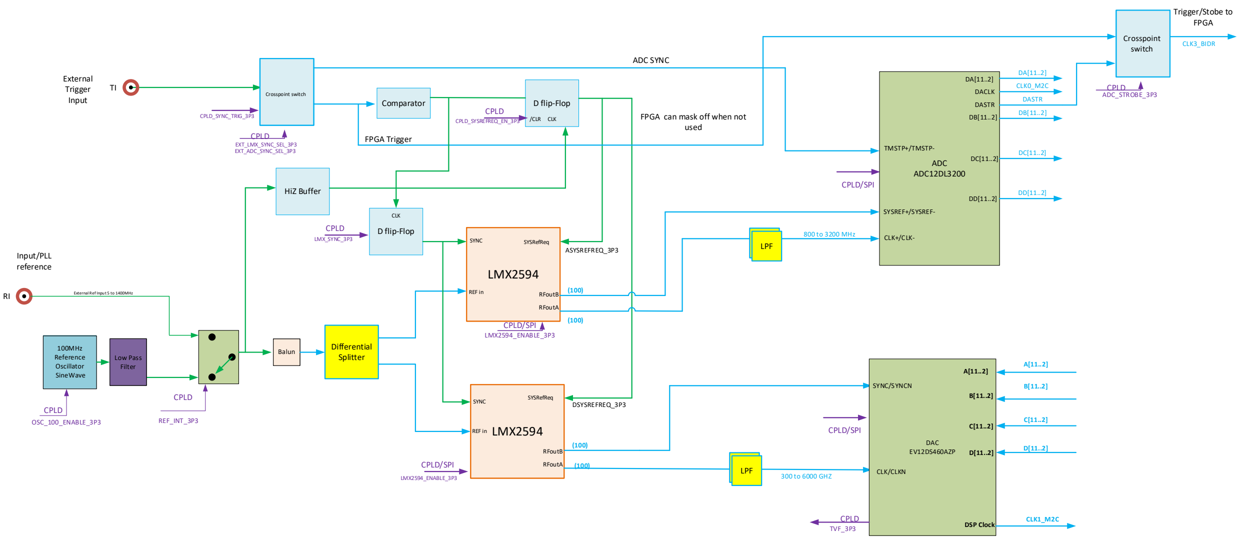


6.7.1 Synchronization Procedure

Once the reference clocks and triggers are provided to the FMC172, the following are steps to synchronize the boards. Refer to Figure 6-5 for the following steps.

1. Program the PLL in SYNC mode.
2. Configure the FMC172s to accept and external sync pulse.
3. Set CPLD bit lmx_sync_edge high.
4. Send an external pulse to the FMC on the TR input. This pulse will assert the SYNC on the LMX2594 to synchronize the FMC172s' PLLs.
5. Set CPLD bit lmx_sync_edge low.
6. Send an external pulse to the FMC172s. This will de-assert the SYNC on the LMX2594.
7. Use the FMC172 software to configure the FMC172s to accept an external SYSREF start pulse.
8. Send an external pulse to the FMC172s. This pulse will cause the FMC172s' LMX2594s to generate SYSREF pulses. The DAC LMX2594 is set to send two SYSREF pulses when triggered. The ADC LMX2594 is set to send a continuous stream of pulses and is turned off when ADC SYSREF calibration is complete. At this point, the ADC and DAC are synchronized.
9. Use the FMC172 software to configure the FMC172s to route triggers to the FPGAs and configure the FPGAs to reset internal clock dividers based on the trigger events.
10. Use the FMC172 software to configure the FPGAs to accept external triggers for data acquisition and data generation.
11. Send an external pulse to the FMC172s. This pulse will cause the FPGAs to acquire ADC data and send DAC data.

Figure 6-5 System Clocking



6.8 Power Supply

The available input power, through the HPC connector, along with typical and maximum current consumption is shown below.

Table 6-4 FMC Available Power and Power Consumption

Power Plane	Maximum Available	Typical Current (mA)	Maximum Current (mA)	Typical Power (W)	Maximum Power (W)
VADJ	4000 mA	20	-	-	-
3P3V	3000 mA	1818	2009	6.029	6.63
12P0V	1000 mA	632	741	7.824	9.108
VIOB	1mA				
3P3VAUX (Operating) 3P3VAUX (Standby)	20 mA 1 μA	1.8 mA	5.8 mA	5.9 mW	19 mW

7 • Controlling the FMC172

7.1 I²C Devices

The devices shown in the table below are directly connected to the I²C bus, The EEPROM is powered by VAUX and directly faces the I²C bus, the other devices including the I²C for a stacked FMC are behind an I²C level translator for isolation until full power is applied.

Table 7-1 I²C Slave Addresses

Device	I²C Address	GA1	GA0	Address Binary	Address Hex
M24C02 (EEPROM)	10100XX	0 0 1 1	0 1 0 1	1010000 1010010 1010001 1010011	0x50 0x52 0x51 0x53
AD7291 (ADC Monitor)	010XXXX	0 0 1 1	0 1 0 1	0101111 0101100 0100011 0100000	0x2F 0x2C 0x23 0x20
AD7291 (Voltage Monitor)	010XXXX	 0 0 1 1	 0 1 0 1	See Table 7-2	(Translated) 0x2E 0x2B 0x28 0x22
CPLD (Board Control)	00111XX	0 0 1 1	0 1 0 1	0011100 0011101 0011110 0011111	0x1C 0x1D 0x1E 0x1F

NOTES

- The CPLD reads the GA0 and GA1 lines, and provides 2 buffered output signals CPLD_GA0_OUT_3P3 and CPLD_GA1_OUT_3P3
- To allow operation of a stacked card, the CPLD reads the GA0 and GA1 lines and provides 2 buffered output signals CPLD_GA0_OUT_CC_3P3 and CPLD_GA1_OUT_CC_3P3, by default the CPLD should read the numeric value of the GA0 and GA1 and increment this by 1 (firmware permitting) if not, an address can be hardcoded based on the carrier card used.
- To allow a second AD7291 to exist on the FMC172 address re-mapping is used as described in Section 7.1.1.

7.1.1 I²C Address Translation for Second AD7291

To monitor all the supply voltages as well as the ADC's temperature a second AD7291 is located on the FMC172 with an alternate set of addresses provided by the CPLD. The CPLD drives the XGA0 and XGA1 pins based on the lookup table shown in the table below.

Table 7-2 AD7291 #2 Address Translation

FMC Signal		CPLD Output		Final Address	
GA 1	GA 0	XGA1/AS 1	XGA0/AS 0	Binary	Hex
0	0	0	Tri-State	010 1110	0x2E
0	1	Tri-State	1	010 1011	0x2 B
1	0	Tri-State	0	010 1010	0x28
1	1	1	Tri-State	010 0010	0x22

7.2 Controlling the CPLD

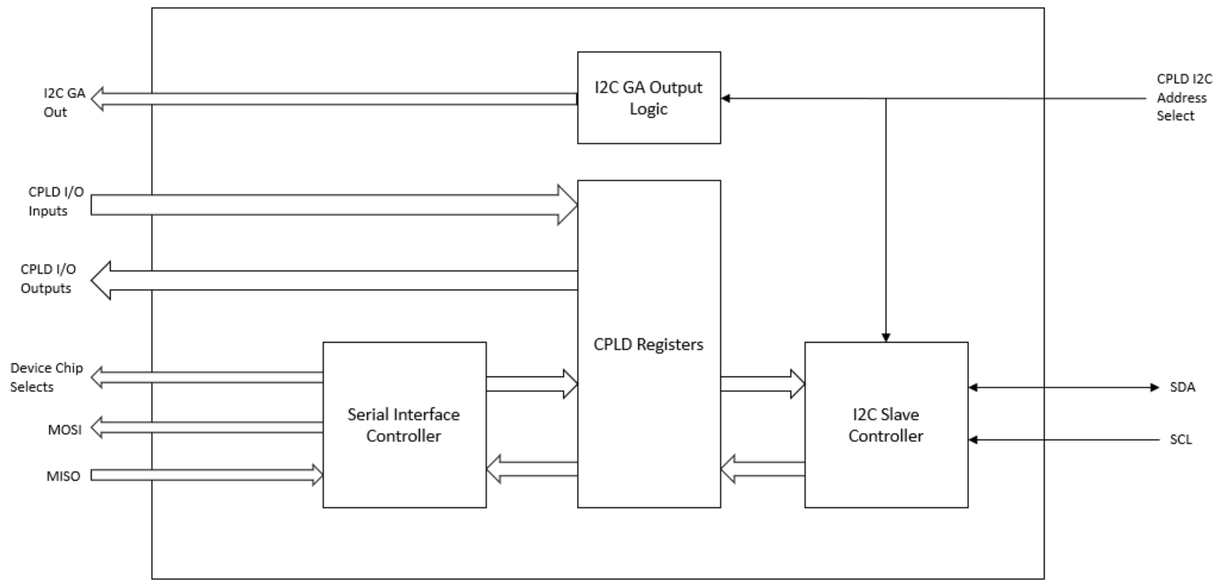
The CPLD is implemented as an I²C device with registers that are used to control devices, read status bits, and perform I²C to SPI transactions.

Good knowledge of the internal structure and communication protocol of relevant onboard devices is required for controlling the FMC172. For detailed information, it is recommended to refer to the datasheets mentioned in the related documents section of this document. In addition, Abaco may be contacted for support.

7.2.1 CPLD Simplified Block Diagram

A Xilinx XC2C256 CPLD is used to implement the control logic between the host I²C bus and the FMC172. See Table 7-4 for a full list of signals connected to the CPLD. Refer to the simplified block diagram of the CPLD below.

Figure 7-1 CPLD Architecture



7.2.2 CPLD Register Map

Table 7-3 CPLD Register Map

Register	Address	R/W	Description
ADDR_COMMAND	0x00	W	Selects which device to communicate with. **BIT 0**: adc_dval, default = 0 **BIT 1**: dac_dval, default = 0 **BIT 2**: adc_lmx_dval, default = 0 **BIT 3**: dac_lmx_dval, default = 0 **BIT 4-7: Reserved**
ADDR_CONTROL0	0x01	R/W	**BIT 0**: osc_100_en, default = 1 **BIT 1**: ext_ref_en, default = 0 **BIT 2**: adc_lmx_en, default = 0 **BIT 3**: dac_lmx_en, default = 0 **BIT 4**: ext_lmx_sync_sel, default = 1 **BIT 5**: ext_adc_sync_sel, default = 0 **BIT 6**: cal_disable, default = 1 **BIT 7**: cal_en, default = 0
ADDR_CONTROL1	0x02	R/W	**BIT 0**: sync_cpld, default = 0 **BIT 1**: lmx_sync_edge, default = 0 **BIT 2**: adc_strobe_sel, default = 0 **BIT 3**: adc_syncse, default = 0 **BIT 4**: ad7291_reset, default = 1 **BIT 5**: reserved **BIT 6**: cpld_led, default = 1 **BIT 7**: RESERVED, must write 1
ADDR_CONTROL2	0x03	R/W	**BIT 0**: adc_pd, default = 0 **BIT 1**: adc_caltrig, default = 0 **BIT 2**: cpld_sysrefreq_en, default = 1 **BIT 3**: dac_spi_reset, default = 1 **BIT 4**: dac_phase_sel<0>, default = 0 **BIT 5**: dac_phase_sel<1>, default = 0 **BIT 6**: dac_phase_sel<2>, default = 0 **BIT 7**: dac_clk_div_sel, default = 0
ADDR_STATUS0	0x04	R	**BIT 0**: tvf **BIT 1**: adc_calstat **BIT 2**: alarm_ad7291<0> Temperature ALARM **BIT 3**: alarm_ad7291<1> Voltage ALARM **BIT 4**: RESERVED **BIT 5**: ps_pg **BIT 6**: ga0_mod_in **BIT 7**: ga1_mod_in
ADDR_VERSION	0x05	R	0x10
ADDR_I2C _DATA_0	0x06	W	LSB byte to send to the selected SPI device
ADDR_I2C _DATA_1	0x07	W	2nd byte to send to the selected SPI device
ADDR_I2C _DATA_2	0x08	W	3rd byte to send to the selected SPI device
ADDR_I2C _READ_0	0x0E	R	LSB byte read from SPI device
ADDR_I2C _READ_1	0x0F	R	MSB byte read from SPI device

7.2.3 CPLD Signals Functional Description

All banks of CPLD will be referenced to 3.3V (RED) or 1.8V (GREEN). I/O's will be level shifted as required. The signal direction is as follows:

- Output signals from the CPLD are identified with an 'O'
- Input Signals to the CPLD are identified with an 'I'
- Bidirectional Signals are identified with an 'I/O'
- The address (ADR header) is formatted as x.x (Address.Bit)

The signal names and functions are listed below.

Table 7-4 CPLD Control Signals

Signal Name (Schematic Net Name)	Initial State	I/O	ADR	
adc_dval (ADC1_SPI_SCS_3P3#)	1	O	0.0	Chip select output for ADC0 SPI
dac_dval (DAC_SPI_CS_3.3#)	1	O	0.1	Chip select output for DAC0 SPI
adc_lmx_dval (ALMX2594_SPI_CS_3P3#)	1	O	0.2	Chips select output for ADC LMX2594 SPI
dac_lmx_dval (DLMX2594_SPI_CS_3P3#)	1	O	0.3	Chips select output for DAC LMX2594 SPI
osc_100_en (OSC_100_ENABLE_3P3)	1	O	1.0	A logic 1 enables the power supply to the onboard 100 MHz reference oscillator
ext_ref_en (EXT_REF_ENABLE_3P3)	0	O	1.1	A logic 0 routes the 100 MHz reference oscillator to the LMX PLL clock input
adc_lmx_en (ADC_LMX2594LMX_EN)	0	O	1.2	A logic 1 enables the LMX2594 PLL synthesizer via CE pin
dac_lmx_en (DAC_LMX2594LMX_EN_3P3)	0	O	1.3	A logic 1 enables the LMX2594 PLL synthesizer via CE pin
ext_lmx_sync_sel (EXT_LMX_SYNC_SEL_3P3)	1	O	1.4	A logic 0 selects external input for the SYSREFReq
ext_adc_sync_sel (EXT_ADC_SYNC_SEL_3P3)	0	O	1.5	A logic 0 transmits the FPGA synchronization pattern on data lines
cal_disable (CAL_DISABLE_3P3)	1	O	1.6	A logic 1 disables the analog loopback
cal_enable (CAL_ENABLE_3P3)	0	O	1.7	A logic 0 disables the analog loopback
sync_cpld (CPLD_SYNC_TRIG_3P3)	0	O	2.0	Trigger from CPLD
lmx_sync_edge (LMX_SYNC_3P3)	0	O	2.1	Sync pulse to sync LMX PLLs to sync to the rising edge of the reference input.

Signal Name (Schematic Net Name)	Initial State	I/O	ADR	
adc_strobe_sel (ADC_STROBE_3P3)	0	O	2.2	A logic 1 Selects adc strobe output to FPGA
adc_syncse (ADC_SYNCESE#_3P3)	0	O	2.3	A logic 1 sets to output digital interfaces test patterns from ADC
ad7291_reset- (AD7291_RESET_3P3#)	1	O	2.4	A logic 0 resets both AD7291 Devices 10k external pull up to vcc, this line must default to a 1, do not hold this line at a logic 0
Reserved	x	x	2.5	
cpld_led (LED_ENABLE_3P3)	1	O	2.6	Software controllable LED 1 = ON
Reserved	1	O	2.7	Always set to 1
adc_pd (ADC_PD_3P3)	0	O	3.0	A logic 1 causes the ADC to enter low power mode.
adc_caltrig (ADC_CALTRIG_3P3)	0	O	3.1	A logic 1 triggers ADC foreground calibration.
cpld_sysrefreq_en (CPLD_SYSREFREQ_EN_3P3)	1	O	3.2	A logic 1 enables SYSREFReq pulse
dac_spi_reset (DAC_SPI_RESET_3P3#)	1	O	3.3	A logic 0 resets the DAC
dac_phase_sel<0> (DAC_PHASE_SEL0_3P3)	0	O	3.4	DAC_PHASE_SEL<0> (DAC_PHASE_SEL0_3P3)
dac_phase_sel<1> (DAC_PHASE_SEL1_3P3)	0	O	3.5	DAC_PHASE_SEL<1> (DAC_PHASE_SEL1_3P3)
dac_phase_sel<2> (DAC_PHASE_SEL2_3P3)	0	O	3.6	DAC_PHASE_SEL<0> (DAC_PHASE_SEL0_3P3)
dac_clk_div_sel (DAC_CLK_DIV_SEL_3P3)	0	O	3.7	Logic 0 selects OCDS0 Logic 1 select OCDS2
tvf (TVF_3P3)	x	I	4.0	DAC timing violation flag
adc_calstat (ADC_CALSTAT_3P3)	x	I	4.1	ADC alarm output (1.8V)
alarm_ad7291<0> (ALARM_AD7291_0_3P3)	x	I	4.2	AD7291 Alarm output mostly temp and Voltage
alarm_ad7291<1> (ALARM_AD7291_1_3P3)	x	I	4.3	AD7291 Alarm output mostly voltages
RESERVED	x	I	4.4	
ps_pg (PS_PG)	x	I	4.5	Power supply power good.
ga0_mod_in (GA0_MOD_IN_3P3)	x	I	4.6	Input state of GA0

Signal Name (Schematic Net Name)	Initial State	I/O	ADR	
ga1_mod_in (GA1_MOD_IN_3P3)	x	I	4.7	Input state of GA1
SPI_SCLK (SPI_SCLK_3P3)	0	O		3.3V SPI serial clock to LMXs, ADC, DAC
SPI_MOSI (SPI_MOSI_3P3)	0	O		3.3V SPI data to LMXs, ADC, DAC
SPI_LMX_MISO (SPI_DLMX_MISO_3P3)	x	I		3.3V DAC LMX SPI data output
SPI_ADC_MISO (ADC_SPI_MISO_3P3)	x	I		3.3V ADC SPI data output
I2C_SCL (ISO_I2C_SCL_3P3)	x	I		I^2C clock input to CPLD, on isolated side of PCA9517
I2C_SDA (ISO_I2C_SDA_3P3)	x	I/O		I^2C data i/o CPLD, on isolated side of PCA9517
CPLD_XGA0_OUT (CPLD_XGA0_OUT_3P3)	x	O		Alternate address controls for AD7291 (LUT output from GA0:GA1)
CPLD_XGA1_OUT (CPLD_XGA1_OUT_3P3)	x	O		(LUT output from GA0:GA1)
GA0_CC_OUT (GA0_CC_OUT_3P3)	x	O		GA0…GA1_CC = (GA0…GA1) +1
GA1_CC_OUT (GA1_CC_OUT_3P3)	x	O		(Read input and increment by 1)
CPLD_GA0_OUT (CPLD_GA0_OUT_3P3)	x	O		Tracks GA0, provides isolated buffered signal
CPLD_GA1_OUT (CPLD_GA1_OUT_3P3)	x	O		Tracks GA1, provides isolated buffered signal
CLK4 (CPLD_4M_CLK_3P3_4)	x	I		4 MHz clock input to CPLD
STACKED_PG_M2C (STACKED_CARD_PG_M2C)	x	I		Connection only CPLD vision to stacked card present

7.3 Controlling the Clock Tree

7.3.1 Oscillators and Switches

The FMC172 has an RF switch that selects whether an internal or external reference is used. These switches must be configured via I²C register writes to the CPLD for various configurations. The following table lists the CPLD bits that are required to be modified for a specific mode of operation.

Table 7-5 Supported Clock Modes

Function	osc_100_en	adc_lmx2594_en	dac_lmx2594_en	ext_ref_en
Power down	0	0	0	0
LMX PLL with Internal reference	1	1	1	0
LMX PLL with External reference	0	1	1	1

7.4 Guidelines for Controlling Onboard Voltage and Temp Monitoring

The FMC172 includes 2 AD7291 '8-channel I²C 12-bit SAR ADCs with temperature monitor' devices for monitoring power supply voltages as well as local and remote temperatures. The device can be programmed and read through the I²C bus at the address defined in Section 8.1.

1. At powerup, the application software should write a '1' to the Reset bit in the Command Register to initialize the part to a known state.
2. All measured values must be multiplied by a constant to convert to the actual analog level. Formulas are included in the associated tables and text.
3. Continuously operating the I²C bus might interfere with the A/D conversion process resulting in signal distortion. It is recommended to program the minimum and maximum thresholds in the monitoring device and only read from the device when the interrupt line is asserted.

7.4.1 AD7291 (ADC Monitor)

The first device is configured to monitor the DAC voltages and temperatures shown in the table below. To convert the ADC reading to voltage or temperature multiply the ADC value by the scaling factor listed in the table. For the ADCs 2 onboard temperature monitors see Section 7.4.2.

Table 7-6 AD7291 Voltage Parameters

Parameter:	Voltage	Formula
Channel 0	VP1P1_ADC_ANA	ADC0 * .00061035V
Channel 1	VP1P9_ADC_ANA	ADC1 * .00061035V
Channel 2	VP1P9_ADC_LVDS	ADC2 * .00061035V
Channel 3	VP3P3_DAC_DIG	ADC3 *. 0012207V
Channel 4	VP_5P0VA	ADC4 *.00183105V
Channel 5	VP5V5VA	ADC5 * .00183105V
Channel 6	ADC_TEMP	(ADC6) 1.6mV / °C, see text
Channel 7	DAC_TEMP	(ADC7) 1.17mV / °C, see text
Temperature	(internally generated)	AD7921 ADC TEMP * .0625 °C

7.4.2 ADC Temperature Measurement

Texas Instruments specifies a maximum die temperature of 105C for the ADCDL3200 ADC IC, and notes that operation above this point will degrade the life expectancy of the ADC. The ADC die temperature requires calibration of the temperature diodes to ensure the maximum die temperature is not exceeded.

On the FMC172, the ADC has a temperature diode, (TDIODE) which can be used to monitor the ADC's temperature. The FMC172 forward biases the TDIODE with a 100uA current source and the resulting temperature dependent voltages can be monitored on channel 6 of the AD7291 described above.

The temperature diode should be measured at a known ambient temperature to get an accurate offset voltage. This offset is used in a linear equation with the diode voltage slope of 1.6mV/°C

To accurately measure the diode temperature, the board should be stable at room temperature, with proper ventilation applied, the software application should then perform the following:

- At powerup hold the ADC and DAC in reset. Measure the ambient temperature on the AD7291, and save this value as the ambient temperature offset as the baseline temperature in °C.
- Measure the temperature diode.
- Save this as the ambient temperature offset voltage.

- This voltage is board and ADC specific and should be used in the individual boards end application.
- Continue with normal power-up sequencing.

On subsequent temperature readings:

- Measure the ADC's internal TDIODE voltage
- Subtract out the ambient temperature reference voltage
- Multiply the result by .00061035V (convert to volts)
- Divide this result by .0016 (convert to °C)
- Add this result to the ambient temperature offset to get the die temperature in °C.

Use this result to program into the AD7291 for alarm. Once the ADC temperature is accurately calibrated, further temperature testing can proceed. If the actual ADC die temperature is at or above 105°C, you should take additional measures to further cool the board.

7.4.3 DAC Temperature Measurement

- At powerup, hold the DAC in reset, measure the ambient temperature on the AD7291 and save this as the baseline temperature in °C.
- Measure each respective temperature diode.
- Save this value as the ambient temperature reference
- Continue with normal power up sequencing.

On subsequent temperature readings:

- Measure the DAC's internal TDIODE voltage
- Subtract out the ambient temperature reference
- Multiply the result by .00061035V (convert to volts)
- Divide this result by .00117 (convert to °C)
- Add this result to the ambient temperature reference to get the die temperature in °C.

NOTE
The hottest spot on the die is 6 °C hotter than read by the diode.

Use this result to program into the AD7291 for alarm. Once the DAC temperature is accurately calibrated, further temperature testing can proceed. If the actual DAC die temperature is at or above 105°C the user should take additional measures to further cool the board.

7.4.4 AD7291 (Voltage Monitor)

The second device, identified in paragraph 4.1 as temperature monitor, is configured to monitor the voltages that are shown in the table below. To convert the ADC reading to a voltage or temperature, multiply the ADC value by the scaling factor listed in the table.

Table 7-7 AD7291 Temperature and Voltage Parameters

Parameter:	Voltage	Formula
Channel 0	PHASE_DET_OUT	ADC0 * .00061035V
Channel 1	VP3P3_CLOCK_ADC	ADC1 * .0012207V
Channel 2	VP3P3_CLOCK_DAC	ADC2 * .0012207V
Channel 3	CPLD_VCC_CORE_1P8	ADC3 * .00061035V
Channel 4	VADJ	ADC4 * .0012207V
Channel 5	VCC_3P3	ADC5 * .0012207V
Channel 6	VCC_12P0	ADC6 * .0036621V
Channel 7	VP3P3_DAC_ANA	ADC7 * .0012207V
Temperature	(internally generated)	AD7921 ADC TEMP * 0.0625 °C

8 • Specifications

8.1 Environmental Specifications

Operating temperature:

- Dependent upon incoming airflow provided by end user as illustrated in Figure 8-1. The VITA AV47 AC2 ruggedness condition can be met by 400 LFM of mean airflow within 9 mm of the entrance to the heatsink.

Storage temperature:

- -40 ˚C to +85 ˚C

8.2 Cooling

The FMC172 has an integral heatsink, and the board should not be operated without its heatsink. Furthermore, benchtop operation requires a fan to be used to maintain a safe operating temperature. In all cases, the temperature should be monitored and steps taken to limit the temperature rise of the board.

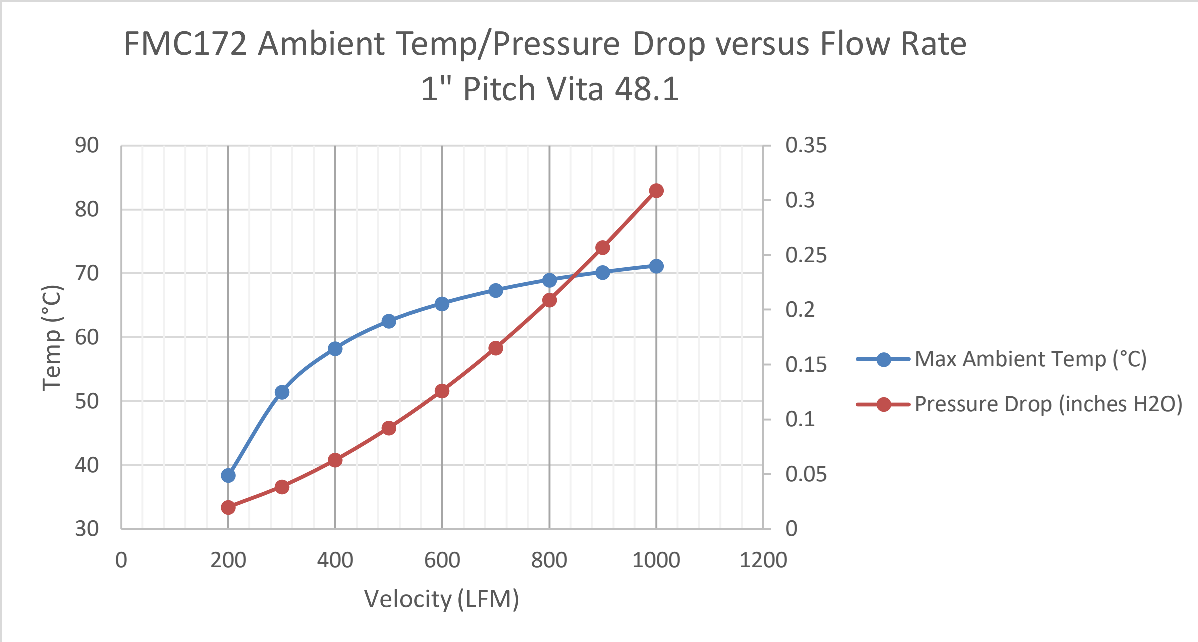
Two different types of cooling will be available for the FMC172.

8.2.1 Convection Cooling

The air flow provided by the chassis fans where the FMC172 operates, must be able to dissipate the heat generated by the onboard components. At the VITA AV47 AC2 ruggedness condition of 55 °C incoming airflow, a minimum mean airflow of 400 LFM entering the FMC172 heatsink is required. Additionally, the 400 LFM mean airflow must be met within 9 mm of the entrance to the FMC172 heatsink, otherwise acceptable thermal performance of the FMC172 cannot be guaranteed.

If the end user provides airflow which is cooler than the VITA AV57 AC2 55C ruggedness condition, then the end user may be able to achieve acceptable thermal performance with lower airflow. Conversely, if the end user provides airflow which is warmer than the VITA AV57 AC2 55C, then acceptable thermal performance could be achieved with higher airflow rates. These trade-offs and required pressure drops are illustrated in Figure 8-1.

Figure 8-1 Temperature, Velocity and Pressure Trade-offs



For standalone operations (such as on a Xilinx development kit), it is strongly recommended to blow air across the FMC and ensure that the temperature of the devices is within the allowed range. Additionally, if the FMC is operated without a carrier board, it is helpful to add ducting around the FMC heatsink and fan to contain the airflow to prevent boundary layer formation from negatively affecting thermal performance. Abaco's warranty does not cover boards on which the maximum allowed temperature has been exceeded

8.2.2 Conduction Cooling

In demanding environments, the ambient temperature inside a chassis could be close to the operating temperature defined in this document. It is very likely that in these conditions, the junction temperature of power-consuming devices will exceed the operating conditions recommended by the devices' manufacturers (mostly +85 °C). While a low-profile heatsink coupled with sufficient air flow might be sufficient to maintain the temperature within operating boundaries, some active cooling would yield better results and would certainly help with resuming operations much faster in the case the devices were disabled because of a temperature "over range".

A • FMC172 FMC Mezzanine and Carrier Connector Pinout Tables

Table Notes:

- All power and ground pins are connected to their common nets on both mezzanine and carrier connectors for stacked operation
- All pins not explicitly noted in the table are passed through between the mezzanine and carrier connectors for stacked operation
- Mezzanine (module) connector exclusive pins are noted in **RED**
- Carrier connector exclusive pins are noted in **BLUE**
- Common (pass through pins) are noted in **GREEN**

Table A-1 Control Signal Mapping

AV57.4	Pin	FMC172 Signal	Notes
GA0	**C34**	GA0_MOD_IN_3.3	Card Global Address 0 from mezzanine connector
GA1	**D35**	GA1_MOD_IN_3.3	Card Global Address 1 from mezzanine connector
PRSNT_M2C#	**H2**	PRSNT_M2C#	Tied to GND (FM172 is present)
PG_M2C	**F1**	PG_M2C	Indicate FMC172 power good status to carrier
CLK_DIR	**B1**	CLK_DIR_MODULE	Driven by mezzanine, tied low
FMC172 Signals Exclusive to Carrier Card			
GA0	**C34**	GA0_CC_OUT_3.3	Card Global Address 1 from CPLD to carrier connector
GA1	**D35**	GA0_CC_OUT_3.3	Card Global Address 1 from CPLD to carrier connector
PRSNT_M2C#	**H2**	PRESENT_M2C_CC#_3P3	Indicates that a stacked card is present (from carrier connector to CPLD)
PG_M2C	**F1**	STACKED_CARD_PG_M2C	Power good status from stacked card (from carrier connector to CPLD)
FMC172 Signals Used that are also Passed Through to the Carrier Connector			
TSRT#	**D34**	TRST#	JTAG Port (also passed through)
TCK	**D29**	TCK	JTAG Port (also passed through)
TMS	**D33**	TMS	JTAG Port (also passed through)
TDI	**D30**	TDI	JTAG Port (also passed through)
TDO	**D31**	TDO	JTAG Port (also passed through)
PG_C2M	**D1**	PG_C2M	Carrier power is OK (also passed through)
I2C_SCL	**C30**	I2C_SCL	I^2C Bus Clock (also passed through)
I2C_SDA	**C31**	I2C_SDA	I^2C Bus Data (also passed through)
RES0	**B40**	RES0	System Reset (also passed through)

The following clock signals are used by the FMC172.

Table A-2 Clock Signal Usage

AV57 Signal	FMC Connector Pin	FMC172 Signal Function
CLK0_M2C+	H4	ADC_DACLK+
CLK0_M2C-	H5	ADC_DACLK-
CLK1_M2C+	G2	DAC_DSP+
CLK1_M2C-	G3	DAC_DSP-
CLK3_BIDR+CLK2_BIDR+	J2	Trigger Output to FPGA
CLK3_BIDR-CLK2_BIDR-	J3	Trigger Output to FPGA

The first eight GBT lanes are reserved for the high-resolution version of the product, disabled in the default build and listed in the table below.

NOTE

All of the DAC pairs are intentionally inverted to optimize the DAC RF output path.

Table A-3 Reserved GPT Lanes

AV57 Signal	FMC Connector Pin	FMC172 Signal Function
DP0_M2C-	C7	DAC_D00+
DP0_M2C+	C6	DAC_D00-
DP1_M2C-	A3	DAC_D01+
DP1_M2C+	A2	DAC_D01-
DP2_M2C-	A7	DAC_C00+
DP2_M2C+	A6	DAC_C00-
DP3_M2C-	A11	DAC_A01+
DP3_M2C+	A10	DAC_A01-
DP4_M2C-	A15	DAC_B00+
DP4_M2C+	A14	DAC_B00-
DP5_M2C-	A19	ADC_A0-
DP5_M2C+	A18	ADC_A0+
DP6_M2C-	B17	DAC_A00+
DP6_M2C+	B16	DAC_A00-
DP7_M2C-	B13	DAC_B01+
DP7_M2C+	B12	DAC_B01-
DP0_C2M-	C3	DAC_C01+
DP0_C2M+	C2	DAC_C01-
DP1_C2M-	A23	ADC_B0-
DP1_C2M+	A22	ADC_B0+
DP2_C2M-	A27	ADC_B1-
DP2_C2M+	A26	ADC_B1+
DP3_C2M-	A31	ADC_A1-
DP3_C2M+	A30	ADC_A1+

AV57 Signal	FMC Connector Pin	FMC172 Signal Function
DP4_C2M-	A35	ADC_C1-
DP4_C2M+	A34	ADC_C1+
DP5_C2M-	A39	ADC_D0-
DP5_C2M+	A38	ADC_D0+
DP6_C2M-	B37	ADC_C0-
DP6_C2M+	B36	ADC_C0+
DP7_C2M-	B33	ADC_D1-
DP7_C2M+	B32	ADC_D1+

All 80 LVDS pairs are mapped to the ADC and DAC. The LA bank is shown in the table below.

NOTE

All of the DAC pairs are intentionally inverted to optimize the DAC RF output path.

Table A-4 LVDS LA Bank LVDS Pair Mapping

AV57 Signal	FMC Connector Pin	FMC172 Signal Function
LA00-_CC	G7	DAC_C06+
LA00+_CC	G6	DAC_C06-
LA01-_CC	D9	DAC_C09+
LA01+_CC	D8	DAC_C09-
LA02-	H8	DAC_C11+
LA02+	H7	DAC_C11-
LA03-	G10	DAC_B10+
LA03+	G9	DAC_B10-
LA04-	H11	DAC_B04+
LA04+	H10	DAC_B04-
LA05-	D12	DAC_B09+
LA05+	D11	DAC_B09-
LA06-	C11	DAC_B11+
LA06+	C10	DAC_B11-
LA07-	H14	DAC_D04+
LA07+	H13	DAC_D04-
LA08-	G13	DAC_B05+
LA08+	G12	DAC_B05-
LA09-	D15	DAC_D03+
LA09+	D14	DAC_D03-
LA10-	C15	DAC_B02+
LA10+	C14	DAC_B02-
LA11-	H17	DAC_D11+
LA11+	H16	DAC_D11-
LA12-	G16	DAC_D08+
LA12+	G15	DAC_D08-
LA13-	D18	DAC_A05+
LA13+	D17	DAC_A05-
LA14-	C19	DAC_A07+
LA14+	C18	DAC_A07-
LA15-	H20	DAC_A04+
LA15+	H19	DAC_A04-
LA16-	G19	DAC_A11+

AV57 Signal	FMC Connector Pin	FMC172 Signal Function
LA16+	G18	DAC_A11-
LA17-_CC	D21	DAC_A09+
LA17+_CC	D20	DAC_A09-
LA18-_CC	C23	ADC_B2-
LA18+_CC	C22	ADC_B2+
LA19-	H23	ADC_D10-
LA19+	H22	ADC_D10+
LA20-	G22	ADC_B5-
LA20+	G21	ADC_B5+
LA21-	H26	ADC_C5-
LA21+	H25	ADC_C5+
LA22-	G25	ADC_C6-
LA22+	G24	ADC_C6+
LA23-	D24	ADC_D8-
LA23+	D23	ADC_D8+
LA24-	H29	ADC_C4-
LA24+	H28	ADC_C4+
LA25-	G28	ADC_C10-
LA25+	G27	ADC_C10+
LA26-	D27	ADC_B6-
LA26+	D26	ADC_B6+
LA27-	C27	ADC_D7-
LA27+	C26	ADC_D7+
LA28-	H32	ADC_C3-
LA28+	H31	ADC_C3+
LA29-	G31	ADC_C9-
LA29+	G30	ADC_C9+
LA30-	H35	ADC_C2-
LA30+	H34	ADC_C2+
LA31-	G34	ADC_C8-
LA31+	G33	ADC_C8+
LA32-	H38	ADC_D5-
LA32+	H37	ADC_D5+
LA33-	G37	ADC_B11-
LA33+	G36	ADC_DB11+

All 80 LVDS pairs are mapped to the ADC and DAC. The HA bank is shown in the table below.

NOTE
All of the DAC pairs are intentionally inverted to optimize the DAC RF output path.

Table A-5 LVDS HA Bank LVDS Pair Mapping

AV57 Signal	FMC Connector Pin	FMC172 Signal Function
HA00-_CC	F5	DAC_C03+
HA00+_CC	F4	DAC_C03-
HA01-_CC	E3	DAC_C02+
HA01+_CC	E2	DAC_C02-
HA02-	K8	DAC_C10+
HA02+	K7	DAC_C10-
HA03-	J7	DAC_C08+
HA03+	J6	DAC_C08-
HA04-	F8	DAC_C07+
HA04+	F7	DAC_C07-
HA05-	E7	DAC_C04+
HA05+	E6	DAC_C04-
HA06-	K11	DAC_B07+
HA06+	K10	DAC_B07-
HA07-	J10	DAC_B08+
HA07+	J9	DAC_B08-
HA08-	F11	DAC_B03+
HA08+	F10	DAC_B03-
HA09-	E10	DAC_C05+
HA09+	E9	DAC_C05-
HA10-	K14	DAC_D06+
HA10+	K13	DAC_D06-
HA11-	J13	DAC_D02+
HA11+	J12	DAC_D02-
HA12-	F14	DAC_D07+
HA12+	F13	DAC_D07-
HA13-	E13	DAC_B06+
HA13+	E12	DAC_B06-
HA14-	J16	DAC_D09+
HA14+	J15	DAC_D09-
HA15-	F17	DAC_D10+
HA15+	F16	DAC_D10-
HA16-	E16	DAC_D05+

AV57 Signal	FMC Connector Pin	FMC172 Signal Function
HA16+	E15	DAC_D05-
HA17-_CC	K17	DAC_A06+
HA17+_CC	K16	DAC_A06-
HA18-	J19	DAC_A02+
HA18+	J18	DAC_A02-
HA19-	F20	DAC_A08+
HA19+	F19	DAC_A08-
HA20-	E19	DAC_A03+
HA20+	E18	DAC_A03-
HA21-	K20	DAC_A10+
HA21+	K19	DAC_A10-
HA22-	J22	ADC_A11-
HA22+	J21	ADC_A11+
HA23-	K23	ADC_A5-
HA23+	K22	ADC_A5+

Table A-6 LVDS HB Bank LVDS Pair Mapping

AV57 Signal	FMC Connector Pin	FMC172 Signal Function
HB00-_CC	K26	ADC_A4-
HB00+_CC	K25	ADC_A4+
HB01-	J25	ADC_A10-
HB01+	J24	ADC_A10+
HB02-	F23	ADC_B4-
HB02+	F22	ADC_B4+
HB03-	E22	ADC_B3-
HB03+	E21	ADC_B3+
HB04-	F26	ADC_C11-
HB04+	F25	ADC_C11+
HB05-	E25	ADC_D9-
HB05+	E24	ADC_D9+
HB06-_CC	K29	ADC_A3-
HB06+_CC	K28	ADC_A3+
HB07-	J28	ADC_A9-
HB07+	J27	ADC_A9+
HB08-	F29	ADC_D11-
HB08+	F28	ADC_D11+
HB09-	E28	ADC_B7-
HB09+	E27	ADC_B7+
HB10-	K32	ADC_A2-
HB10+	K31	ADC_A2+
HB11-	J31	ADC_A8-
HB11+	J30	ADC_A8+
HB12-	F32	ADC_B9-
HB12+	F31	ADC_B9+
HB13-	E31	ADC_B8-
HB13+	E30	ADC_B8+
HB14-	K35	ADC_D4-
HB14+	K34	ADC_D4+
HB15-	J34	ADC_A7-
HB15+	J33	ADC_A7+
HB16-	F35	ADC_B10-
HB16+	F34	ADC_B10+
HB17-_CC	K38	ADC_D6-
HB17+_CC	K37	ADC_D6+
HB18-	J37	ADC_A6-
HB18+	J36	ADC_A6+
HB19-	E34	ADC_D2-

AV57 Signal	FMC Connector Pin	FMC172 Signal Function
HB19+	E33	ADC_D2+
HB20-	F38	ADC_C7-
HB20+	F37	ADC_C7+
HB21-	E37	ADC_D3-
HB21+	E36	ADC_D3+

Glossary

EEPROM	Electronically Erasable Programmable Read Only Memory
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
JTAG	Joint Test Action Group
LDO	Low Dropout (regulator)
LED	Light Emitting Diode
LMX	Refers to LMX2581
LSB	Least Significant Bit(s)
LVDS	Low Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor Logic Level
MSB	Most Significant Bit(s)
PCB	Printed Circuit Board
PDF	Phase Detector Frequency
PLL	Phase Lock Loop

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