Re: CookieBox Data pipes

Weaver, Matt <weaver@slac.stanford.edu>
Fri 10/12/2018 7:30 PM

To: Therrien, Audrey C. <therria@slac.stanford.edu>; Coffee, Ryan <coffee@slac.stanford.edu>; O'Grady, Paul Christopher <cpo@slac.stanford.edu>
Cc: Weninger, Clemens <weninc@slac.stanford.edu>

I think we have several options for a PCIe board with at least 16 fiber optic lanes:

(1) ABACO PC821 with two dual QSFP+ FMC cards.
This would be double wide because of the two mezzanine cards. It is the same board that we use as the carrier for the digitizer. It only has 8 Gen3 PCIe lanes. $10K

(2) HiTechGlobal HTG-K805
This card has 4 QSFP+ modules on board and 16 Gen3 PCIe lanes. $??

Both offer similar FPGAs (Kintex Ultrascale 085 - 115).

(3) HiTechGlobal HTG-710.
This card has 2 CXP modules = 24 fiber optic lanes and 8 Gen3 PCIe lanes. $??
Virtex Ultrascale FPGA (embedded processor).

(4) ABACO PC821 with 1 dual CXP FMC cards and 1 dual QSFP+ FMC.
Double wide; 32 fiber optic lanes. 8 Gen3 PCIe lanes. ~$14k

From: Therrien, Audrey C.
Sent: Tuesday, October 9, 2018 2:45 PM
To: Coffee, Ryan; O'Grady, Paul Christopher; Weaver, Matt
Cc: Weninger, Clemens
Subject: CookieBox Data pipes
When: Friday, October 12, 2018 4:00 PM-5:00 PM.
Where: 901-122 Kite Conference Room

When: Friday, October 12, 2018 4:00 PM-5:00 PM (UTC-08:00) Pacific Time (US & Canada).
Where: 901-122 Kite Conference Room

Note: The GMT offset above does not reflect daylight saving time adjustments.

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The meeting was pushed forward an hour to accommodate schedules.

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Hi!

Following last Friday's meeting about the TMO data reduction, we thought it may be a good idea to meet and brainstorm/discuss how we are going to direct all the cookiebox data in a single node/fpga to do some math on it.

Sorry about putting it on a Friday afternoon, it is the only time I found that we were mostly free.

Audrey