Lab 4: Schematic, Layout and Post-Layout simulation of a 2-Input AND Gate

In this lab, we designed a 2-input AND gate using xschem using the previously designed NAND gate and inverter. Then we verified it using ngspice. Then we designed the AND layout using magic. I don't have a specific format in mind. So if you want to include more information, that's okay too.

Lab tasks:

- We built a two-input AND schematic and symbol using NAND and inverter. Did verification with ngspice.
- Designed layout using NAND and inverter layout.
- Verified that the layout is drc free
- LVS matches
- Did a post-layout simulation

Report guideline:

There needs to be 4 sections.

Introduction: In a few words, describe what this lab is about

Methodology: Describe briefly how you built the AND. Then how you built the layout. Briefly describe what layers you used to get the NAND. Provide screenshots of your schematic, symbol, testbench schematic and layout.

Result: Show me the result of your verification of schematic. From layout, give me screenshots showing it's drc clean and LVS matches. **Also show the results from post-layout simulation.**

Discussion: Describe in a few words what you learned from this analysis, and the challenges you faced.