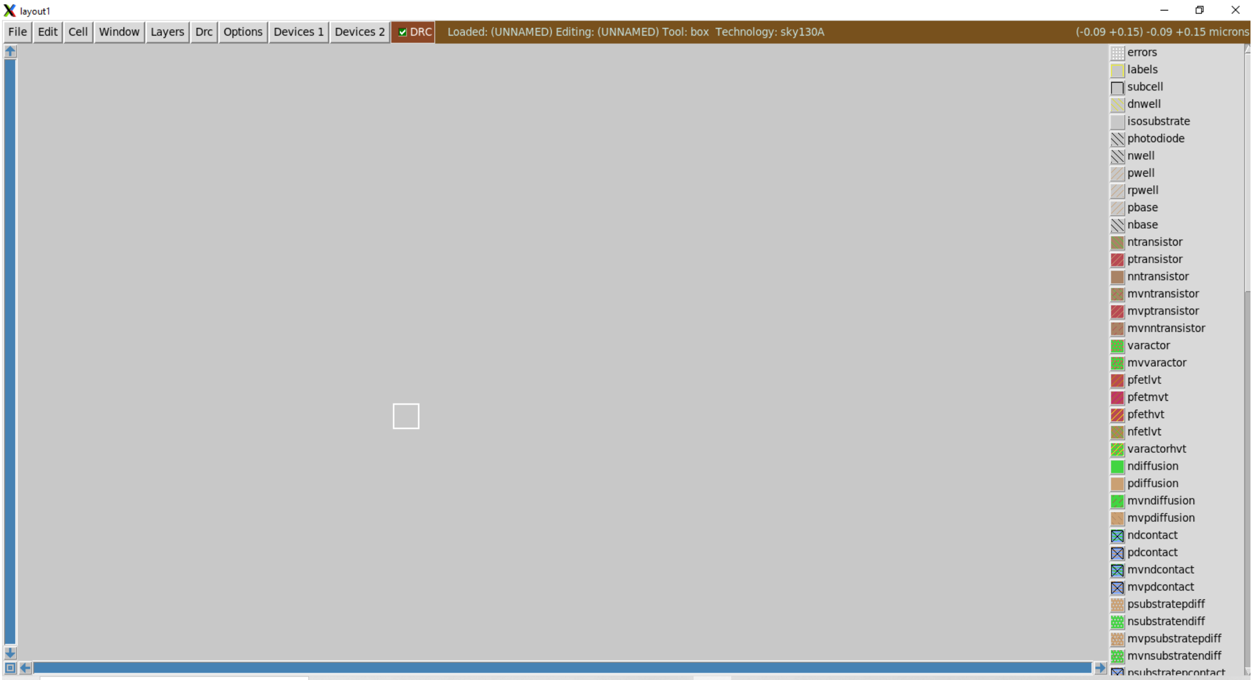
CMOS Inverter Layout Design using Magic and Skywater 130nm PDK

1. Since the skywater tech files are not installed in magic's library, we need to create a symbolic link to use the tech files for drawing layout.

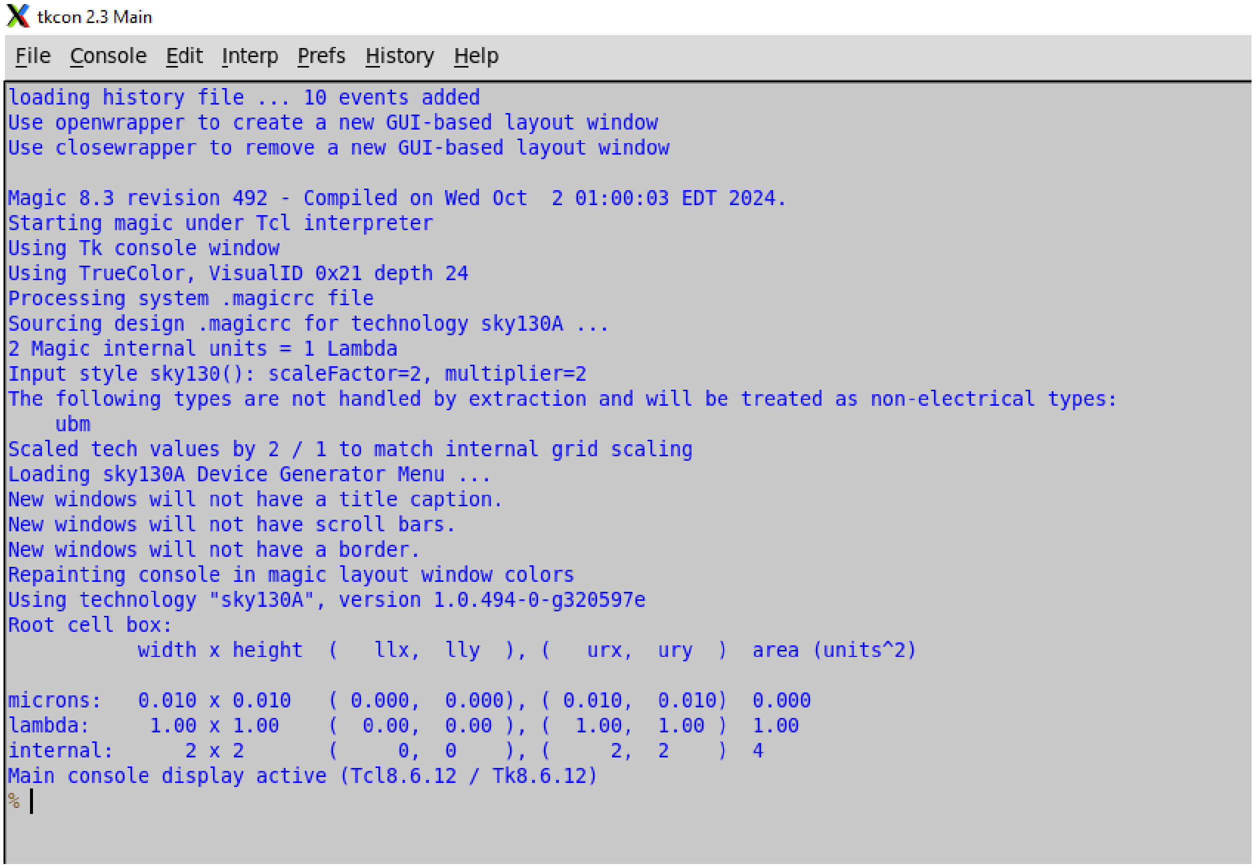
   ```
   sudo ln -s $PDK_ROOT/sky130A/libs.tech/magic/* $CAD_ROOT/magic/sys/
   ```

   where: $PDK_ROOT is /home/<username>/share/pdk
   $CAD_ROOT is /home/<username>/opt/magic/lib
2. Create a directory using mkdir <name>
3. Go to the directory using cd <name>
4. Copy sky130A.magicrc file to the directory.
5. Open magic using: magic -rcfile sky130A.magicrc. Your gui and command window for magic will look like the following two.



Loaded: (UNNAMED) Editing: (UNNAMED) Tool: box Technology: sky130A

(-0.09 +0.15) -0.09 +0.15 microns

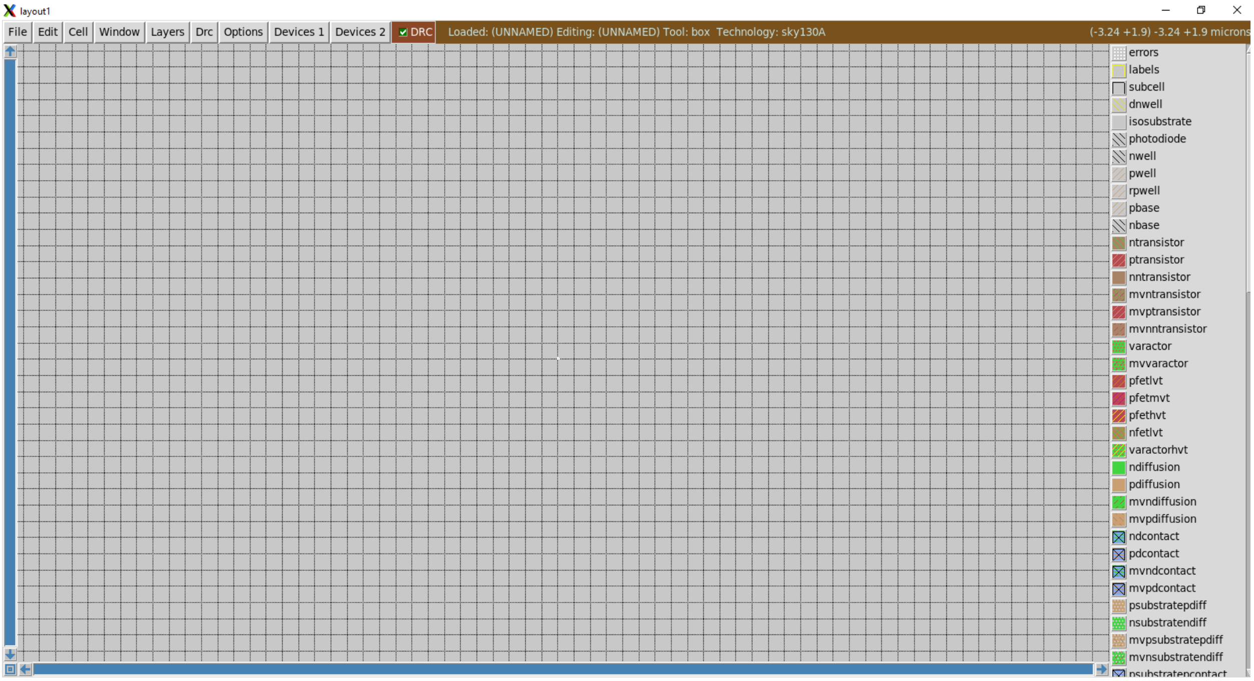


```
loading history file ... 10 events added
Use openwrapper to create a new GUI-based layout window
Use closewrapper to remove a new GUI-based layout window

Magic 8.3 revision 492 - Compiled on Wed Oct  2 01:00:03 EDT 2024.
Starting magic under Tcl interpreter
Using Tk console window
Using TrueColor, VisualID 0x21 depth 24
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
    ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
New windows will not have a title caption.
New windows will not have scroll bars.
New windows will not have a border.
Repainting console in magic layout window colors
Using technology "sky130A", version 1.0.494-0-g320597e
Root cell box:
           width x height  (   llx,  lly  ), (   urx,  ury  )  area (units^2)

microns:   0.010 x 0.010   ( 0.000,  0.000), ( 0.010,  0.010)  0.000
lambda:     1.00 x 1.00    (  0.00,  0.00 ), (  1.00,  1.00 )  1.00
internal:      2 x 2       (     0,  0    ), (     2,  2    )  4
Main console display active (Tcl8.6.12 / Tk8.6.12)
% 
```

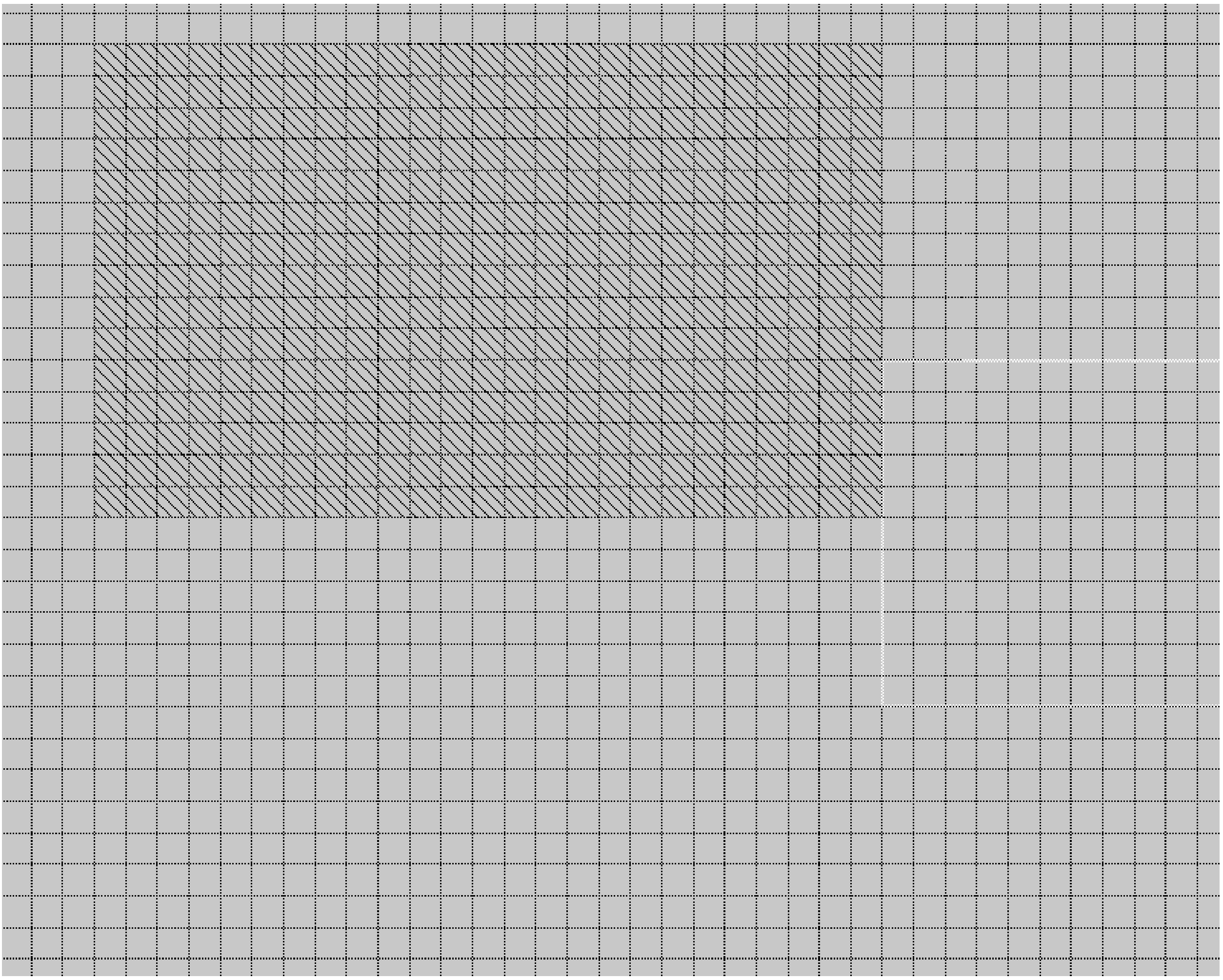
6. Use **grid 100nm 100nm** to set the grid. Use the command in the command window. Also use **snap user**. You will see the grid, and the squares will always start at the edge of the boxes.



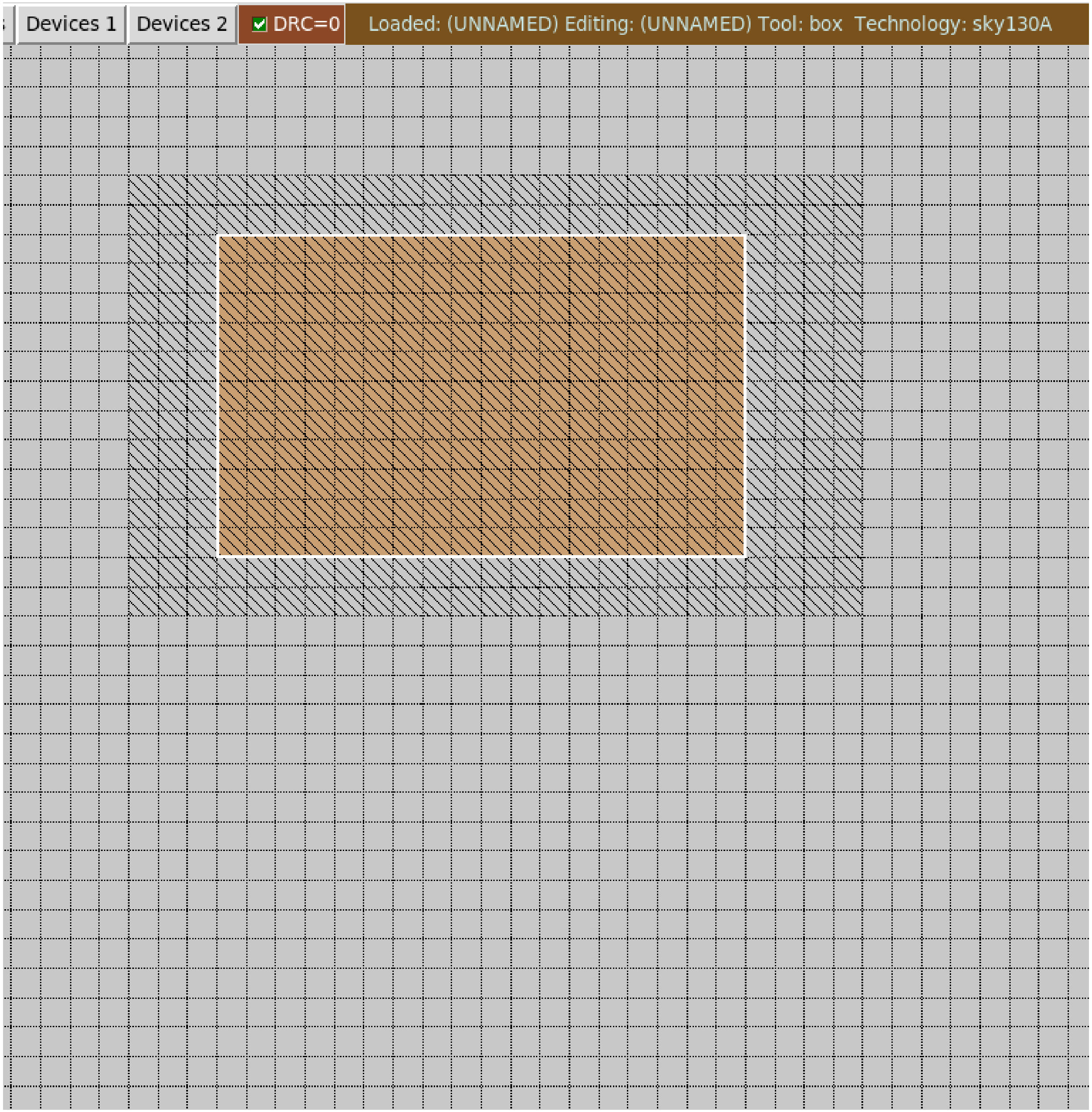
Loaded: (UNNAMED) Editing: (UNNAMED) Tool: box Technology: sky130A

(-3.24 +1.9) -3.24 +1.9 microns

7. Let’s draw nwell first. To do that left click on one edge of your desired box, and then right click on the other edge of your desired box. That other edge is diagonal from the first edge. Middle click on your mouse on the **nwell** layer on the right. You can also use the command **paint nwell** in the command window.

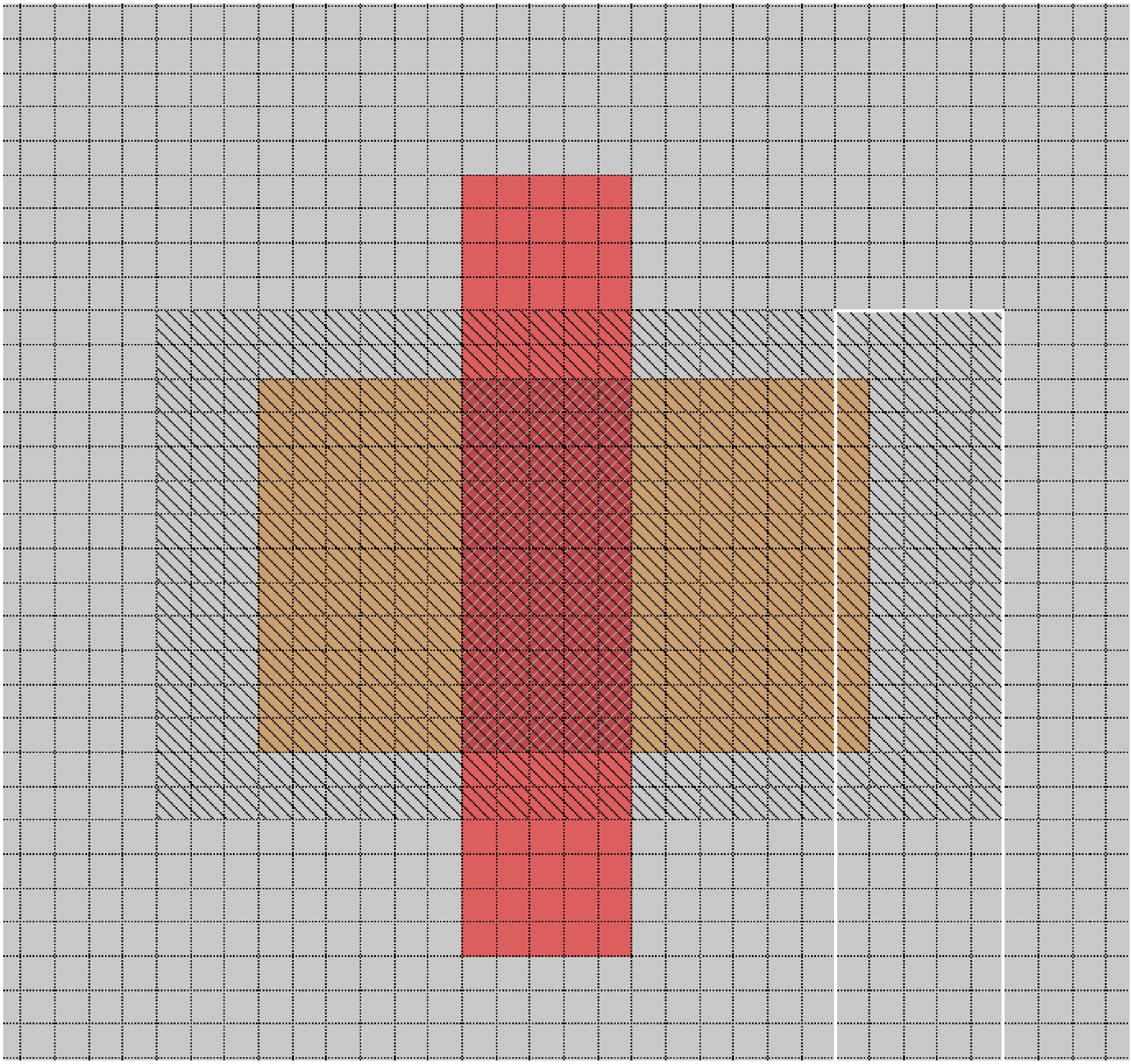


8. Draw the pdiffusion similarly

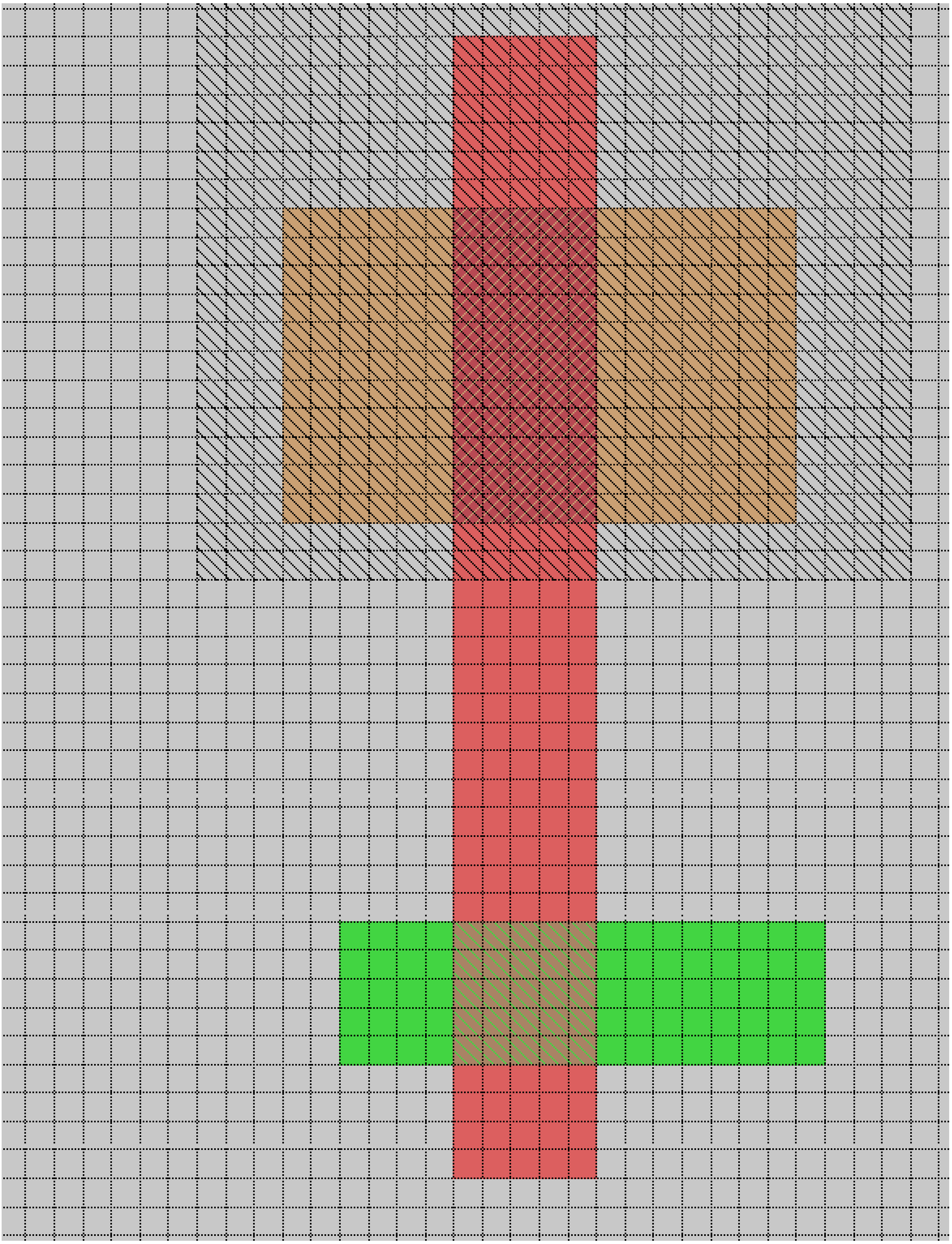


Loaded: (UNNAMED) Editing: (UNNAMED) Tool: box Technology: sky130A

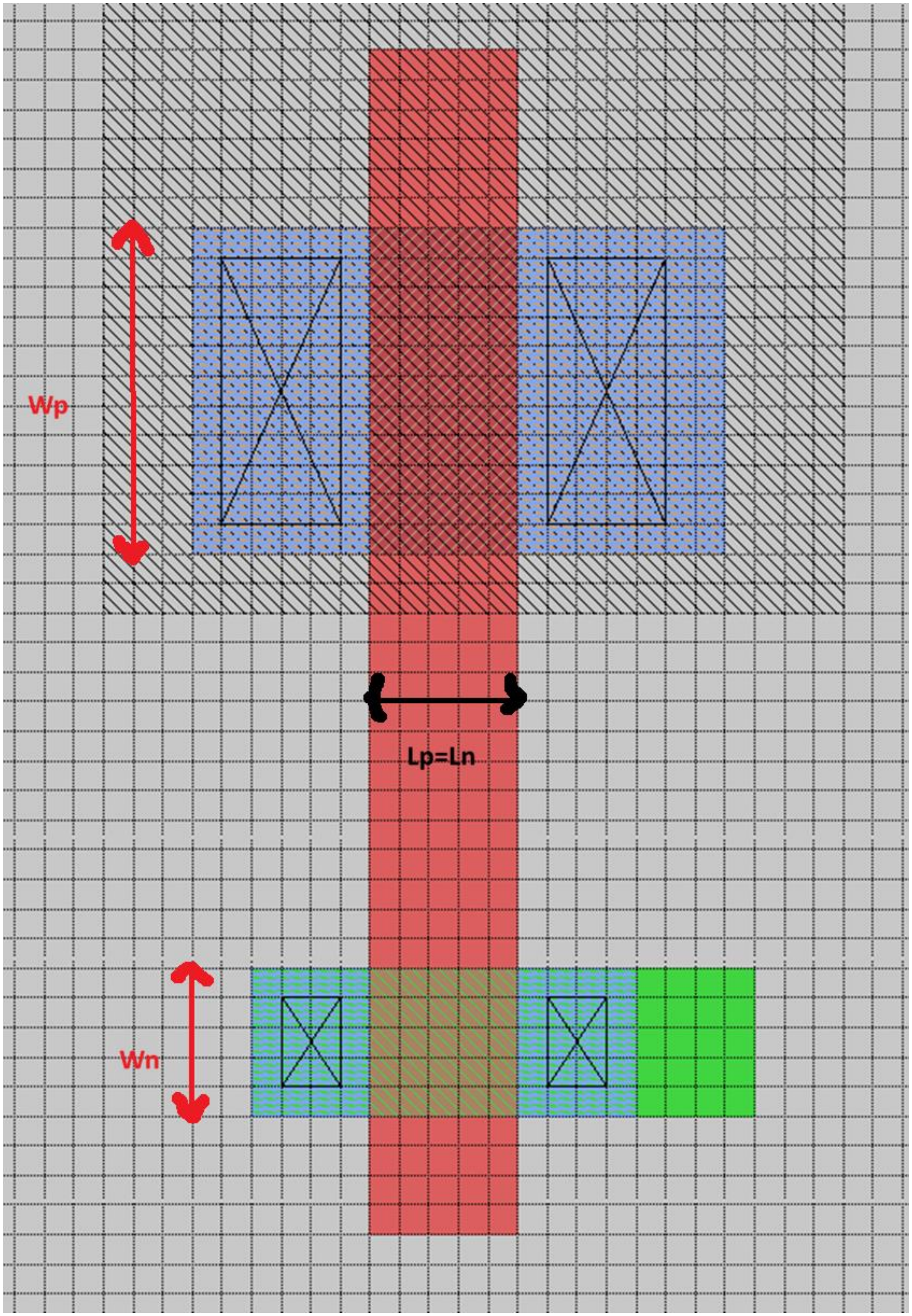
9. Draw polysilicon gate similarly like below. Use **paint poly**.



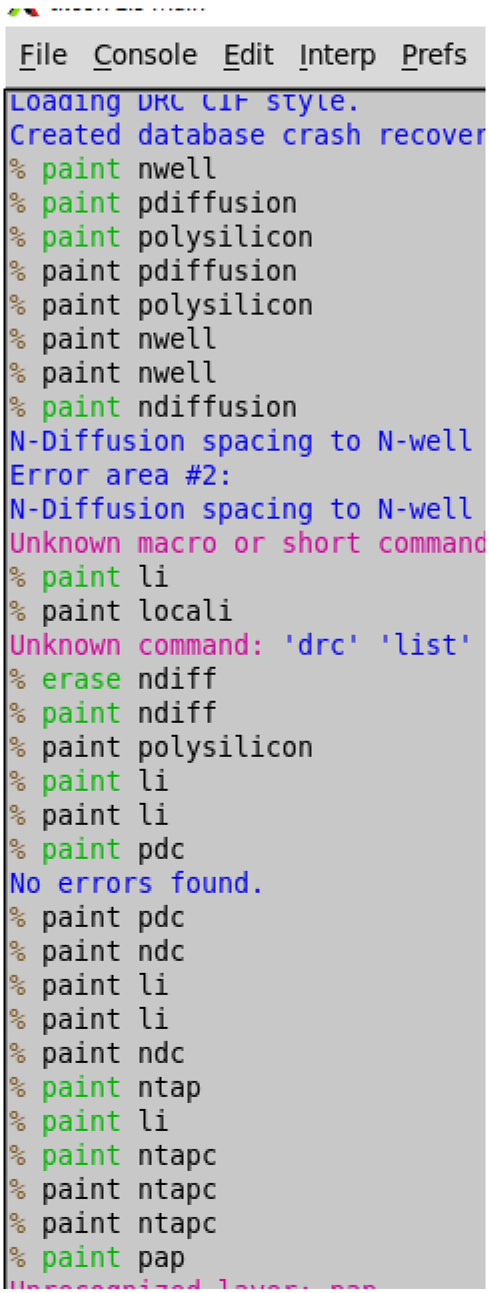
10. Now draw the ndiffusion for the nmos: **paint ndiff**



11. Draw contacts for the sources and drains. To do that, add the local metal layer first using : **paint li.** Then use **paint pdc** and **paint ndc** for the pmos and nmos contacts respectively.

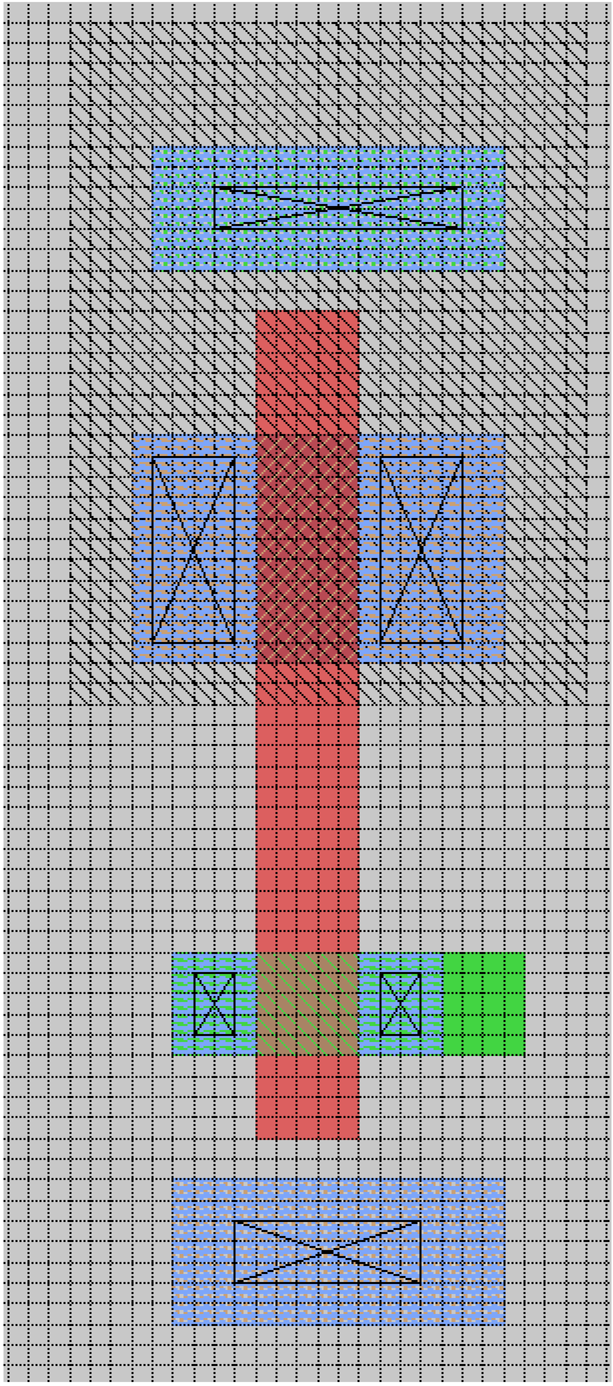


Below is some of the commands I used for my layout.

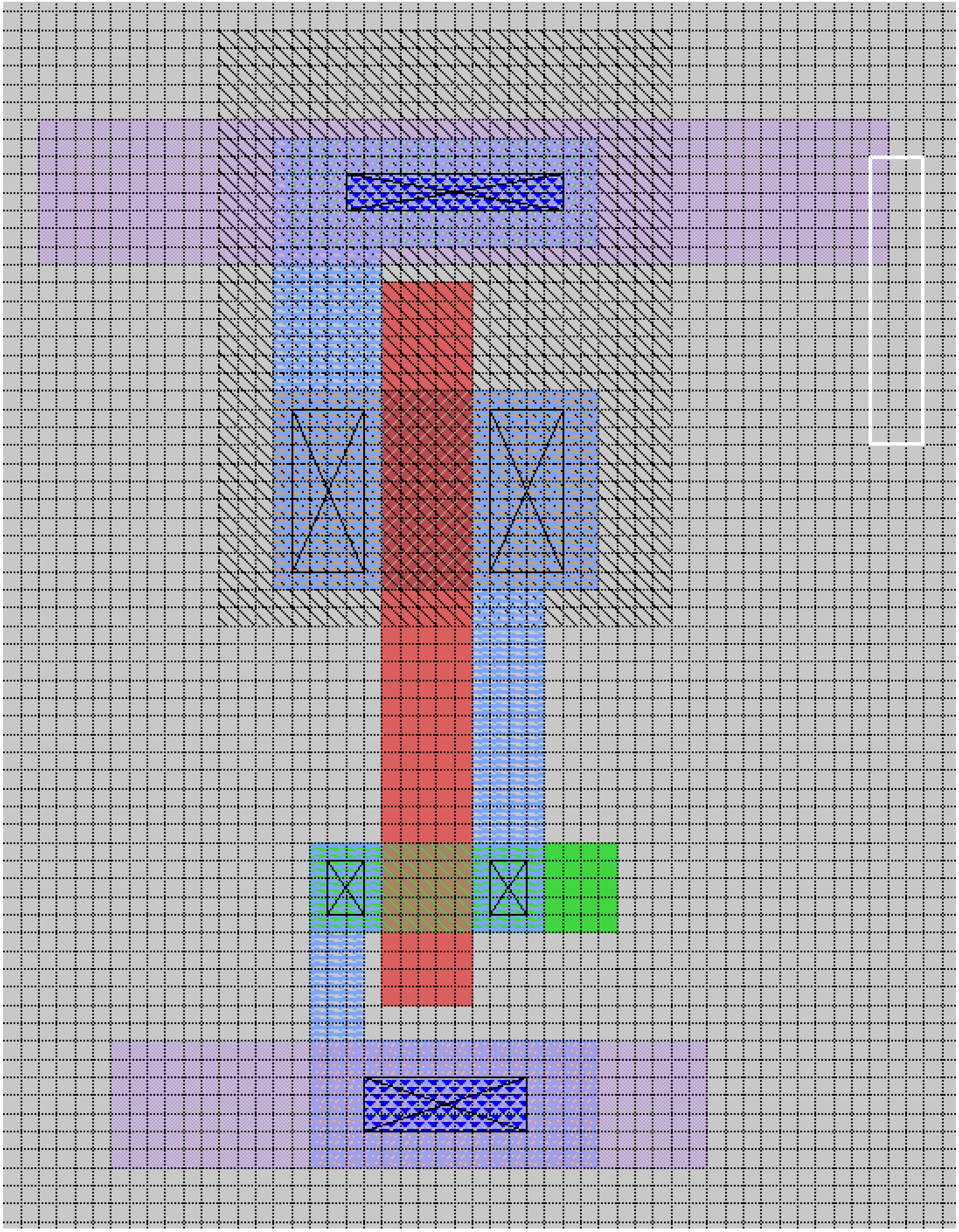


```
Loading DRC CIF style.
Created database crash recover
% paint nwell
% paint pdiffusion
% paint polysilicon
% paint pdiffusion
% paint polysilicon
% paint nwell
% paint nwell
% paint ndiffusion
N-Diffusion spacing to N-well
Error area #2:
N-Diffusion spacing to N-well
Unknown macro or short command
% paint li
% paint locali
Unknown command: 'drc' 'list'
% erase ndiff
% paint ndiff
% paint polysilicon
% paint li
% paint li
% paint pdc
No errors found.
% paint pdc
% paint ndc
% paint li
% paint li
% paint ndc
% paint ntap
% paint li
% paint ntapc
% paint ntapc
% paint ntapc
% paint pap
Unrecognized layer: pap
```

12. Now let’s add the body terminals for the pmos and nmos. For pmos, use **paint ntap**, and for nmos, **paint ptap.** Add contacts by adding li, and the using **paint ntapc** and **paint ptapc**.



13. Add VDD and Gnd rails by using metal1. Make sure to add li layer, and mcon for that. Connect the terminals using li.

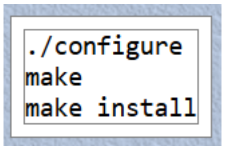


14. Now let's attach the ports. We will attach ports to VDD, GND, input and outputs. Make sure it matches the schematic. To add ports, left and right click on the same spot on the layer layer you want to add the ports to, thenuse the following commands. We want A on the poly layer, Y on the li layer on the right. VDD on top metal1 layer and GND on the bottom metal1 layer.

```
% label A w
% port make 1
% label Y e
 % port make 2
% label VDD w
% port make 3
% label GND w
% port make 4
```

Here, we use the label command with the pin name and then specify where it will be using w or e (west or east). Then we declare it as a port using port make ‘index’. The index specifies the port number in the spice file.

15. Save your layout. Then extract the layout using : extract all. Then extract it to a spice file using : ext2spice. After that, you will see a .spice file in your working directory.
16. To run LVS (Layout vs schematic), you need to install netgen. **DO NOT install it using sudo apt install netgen.**
17. Install netgen from here: http://opencircuitdesign.com/netgen/
18. Use the following commands to install:



```
./configure
make
make install
```

You may have to use sudo make install.

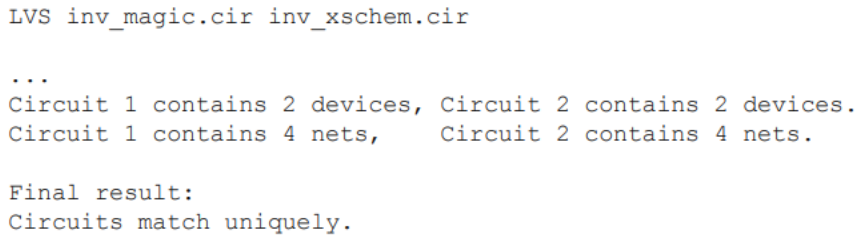
19. Launch netgen. I had to copy the setup.tcl file to the directory from where I launched netgen. The file can be found in “~/share/pdk/sky130A/libs.tech/netgen/” folder.
20. Then use: lvs inverter.spice inv_xschem.spice. The first file one is from magic layout, the last one is from ngspice. The one from ngspice can be found in your .xschem folder in your home directory.
21. If lvs passes, you will see:

```
…
Final result:
Circuits match uniquely.
```

However, you may also see: The following cells had property errors: inv_magic.cir (Although I didn’t see it).
The detailed results of the lvs comparison are saved in the file: comp.out

22. The reason for the property errors is that in the xschem’s spice netlist inv_xschem.cir many of the MOS quantities are given in parametric form rather than as absolute values. The PDK provides a tcl script to solve this issue. The script is located at: ~/share/pdk/sky130A/libs.tech/netgen/sky130A_setup.tcl To take advantage of this script, instead of running netgen and lvs interactively we run netgen in batch mode: netgen -batch lvs inv_magic.cir inv_xschem.cir ~/share/pdk/sky130A/libs.tech/netgen/sky130A_setup.tcl

23. Run lvs again. You will see the fllowing:



```
LVS inv_magic.cir inv_xschem.cir

...
Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets,    Circuit 2 contains 4 nets.

Final result:
Circuits match uniquely.
```