CAL POLY
SAN LUIS OBISPO

EE 431: COMPUTER-AIDED DESIGN OF VLSI DEVICES

Device and Circuit Basics

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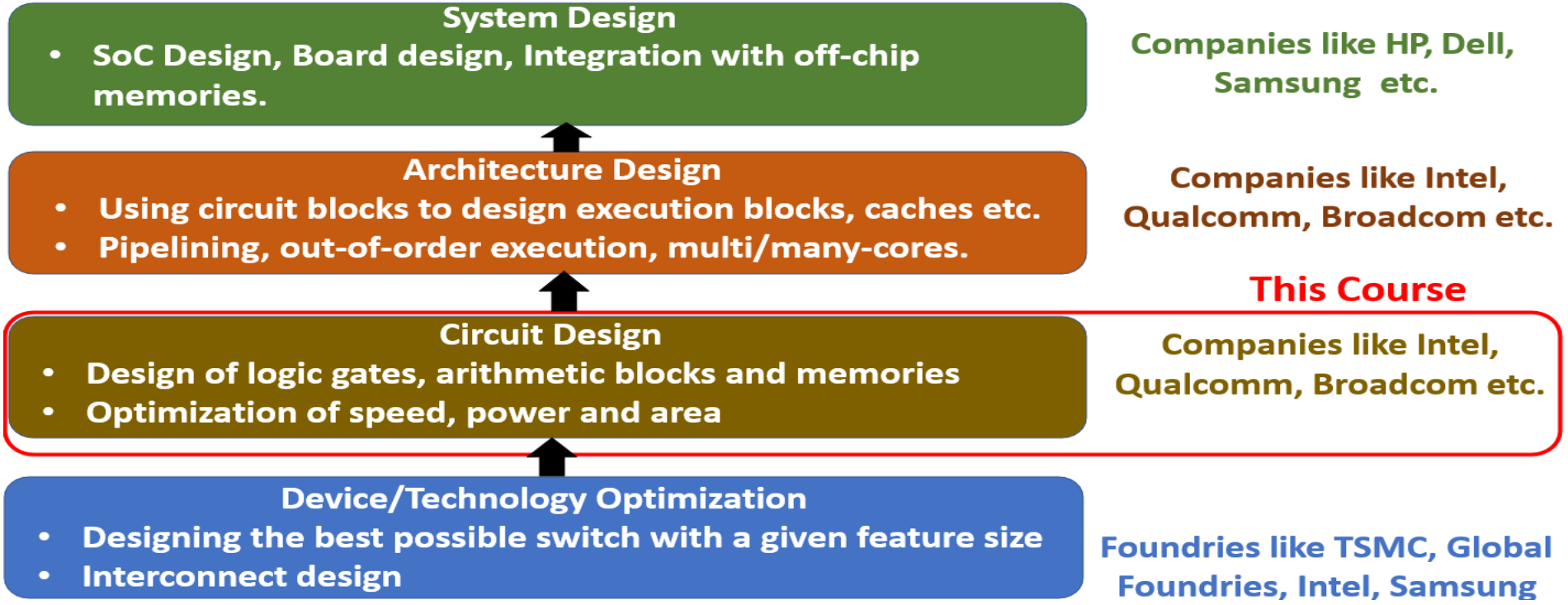
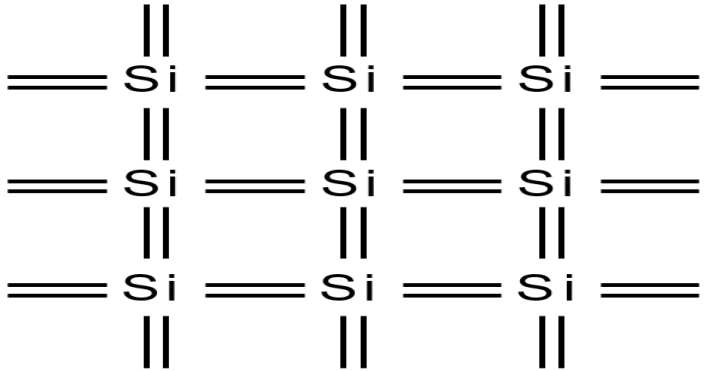
DIGITAL DESIGN: A PERSPECTIVE ON ABSTRACTION



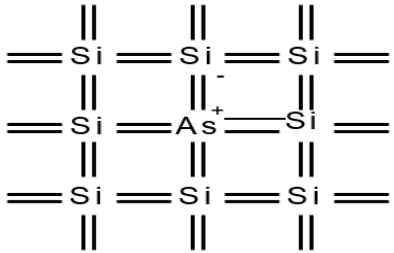
SILICON LATTICE

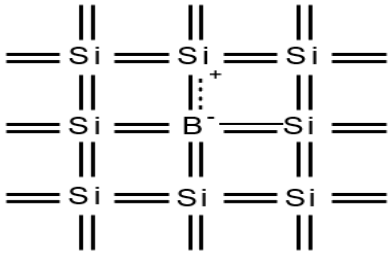
- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



DOPED SEMICONDUCTOR

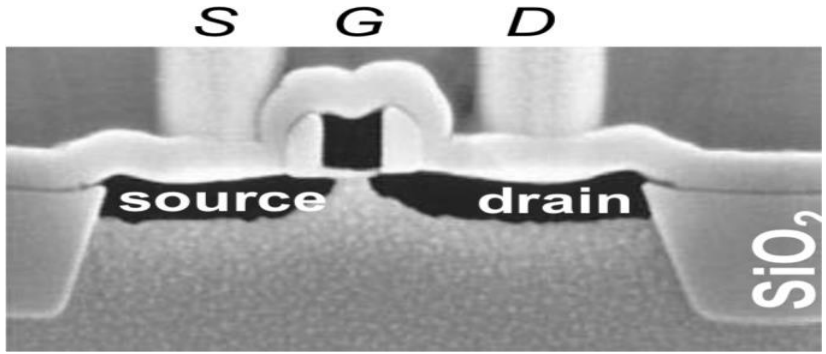
- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)



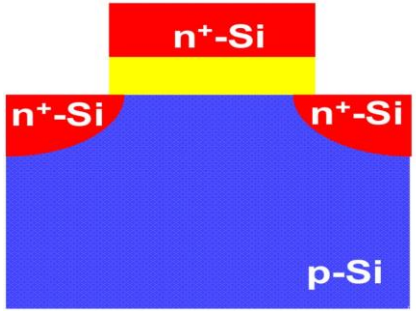


MOSFETS DEVICE STRUCTURE

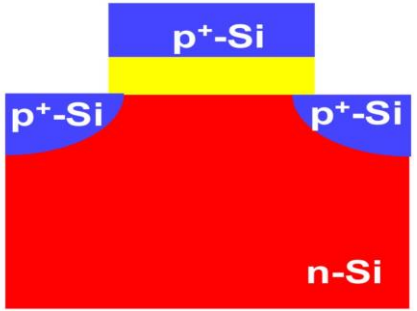
- The MOSFET is the most important device for digital integrated circuits today.
- It is a unipolar device, that is, electrical current is carried predominantly by the drift of one type of carrier: electrons in the n-MOS transistor and holes in the p-MOS device.
- It is a field effect, or voltage-controlled, device, which makes the standby power consumption low.
- The ease with which the MOSFET geometry can be scaled down in size, make it very attractive for VLSI.



NMOS/ NFET/ n-MOS



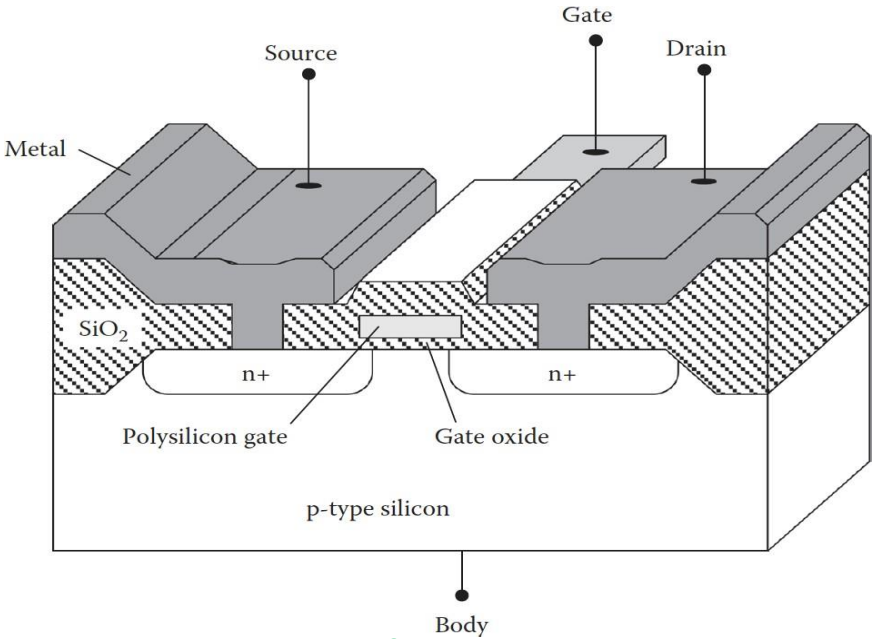
PMOS/ PFET/ p-MOS



MOSFETS DEVICE STRUCTURE

Enhancement-Type MOSFET: No conducting channel between the drain and source unless a positive voltage is applied between the gate and source (so it is a normally-off)

- **The name enhancement type reflects the fact that a gate bias is required to enhance a conducting channel**
- **Some MOS transistors are designed to conduct with zero gate-source bias, and these are referred to as depletion type devices.**
- **However, enhancement type devices are preferred in digital circuits for low standby power.**



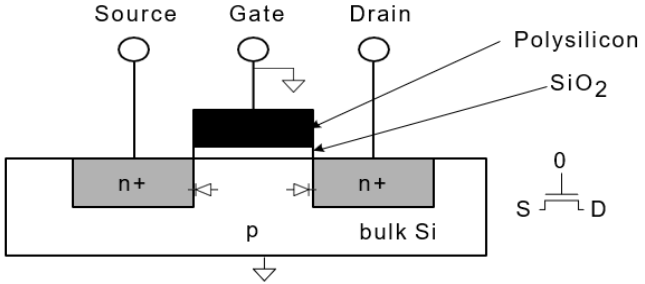
Enhancement Type NMOS

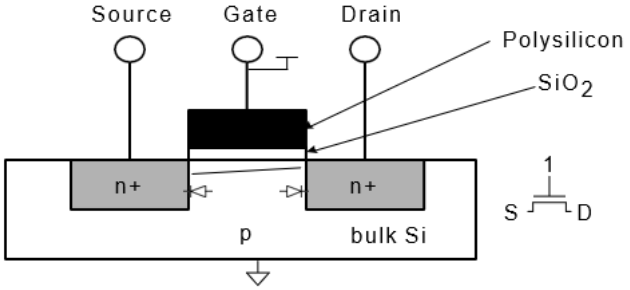
Source: Digital Integrated Circuits : Analysis and Design, Second Edition, by John E. Ayers

NMOS OPERATION

- When gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF

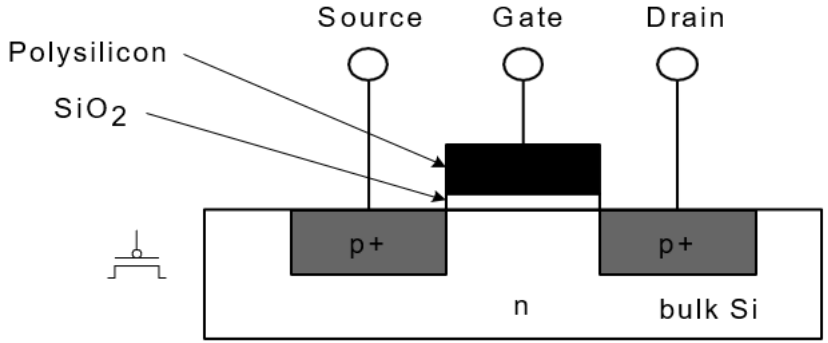
- When gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON





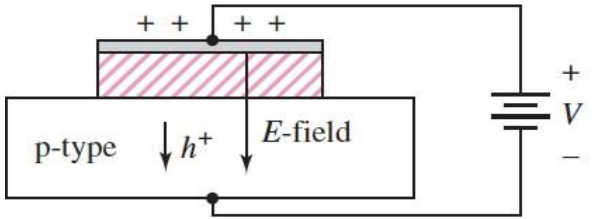
PMOS OPERATION

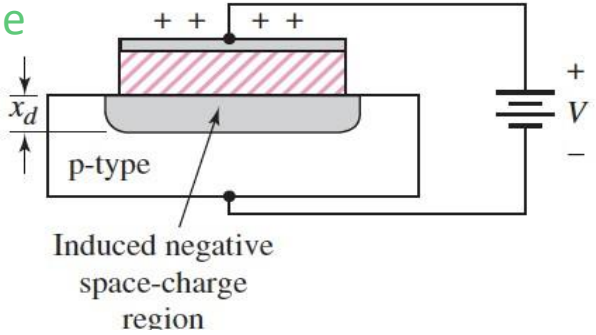
- Body tied to high voltage (VDD)
- Gate low: transistor ON
- Gate high: transistor OFF
- Bubble indicates inverted behavior

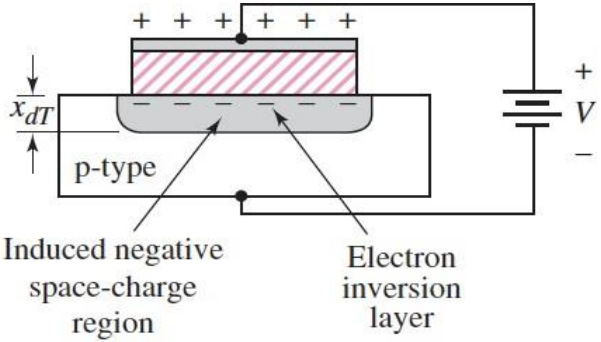


THE MOS CAPACITOR

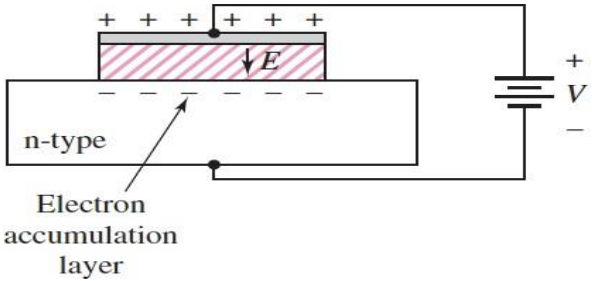
The MOS capacitor with p-type substrate

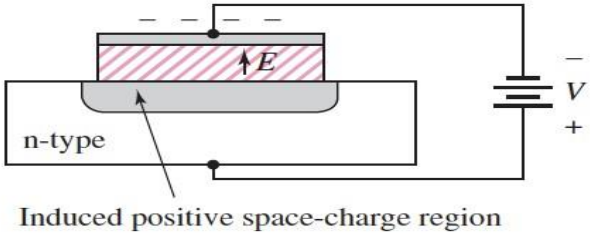


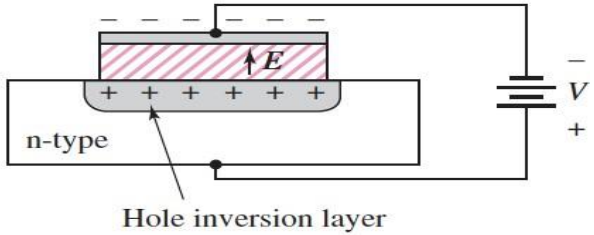




The MOS capacitor with n-type substrate







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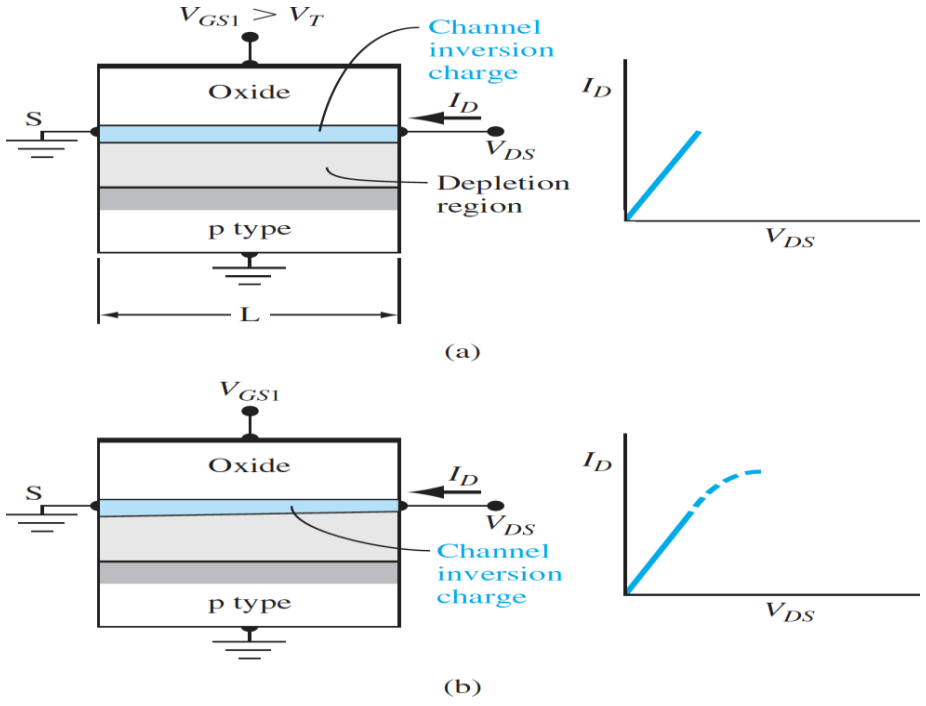
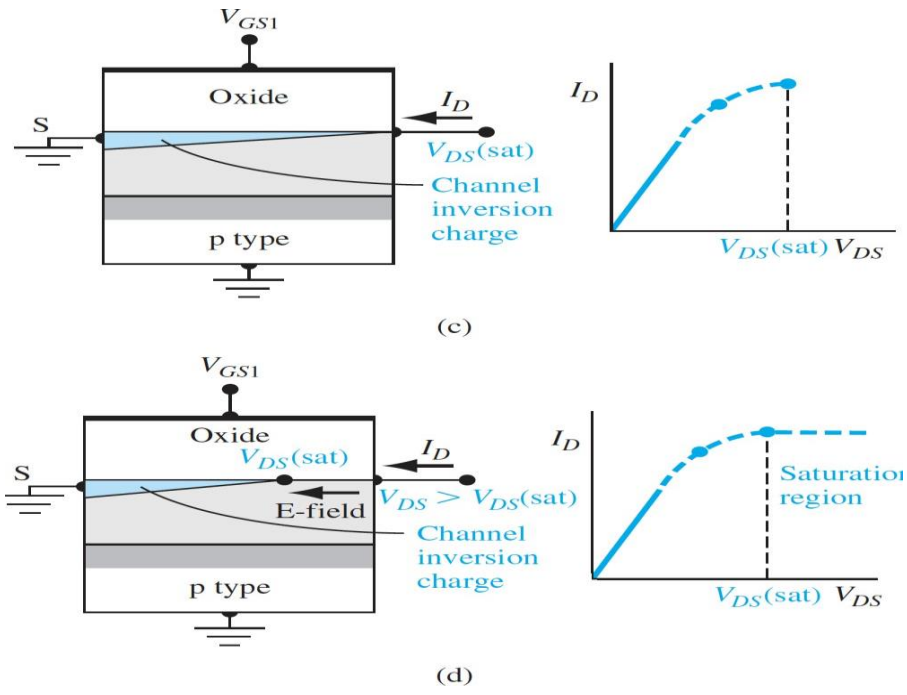
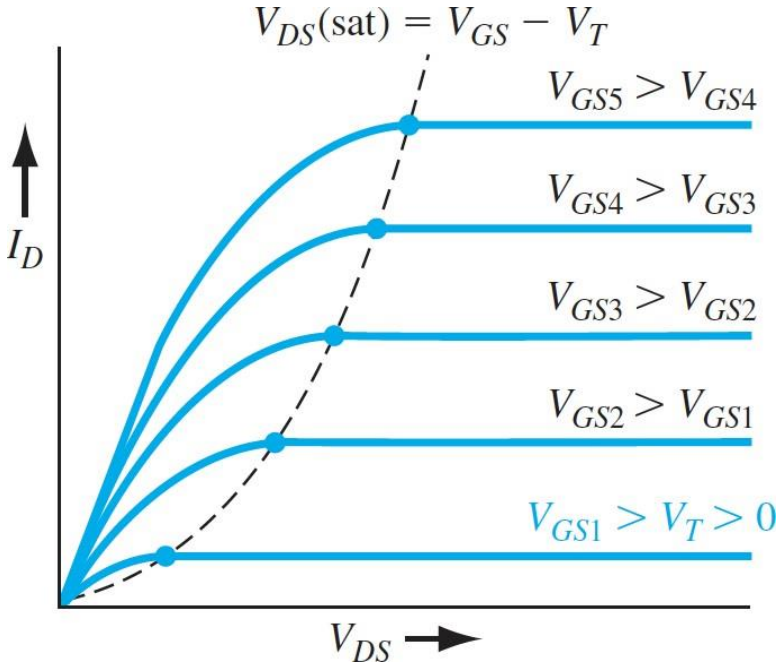
MOSFET I-V CHARACTERISTICS

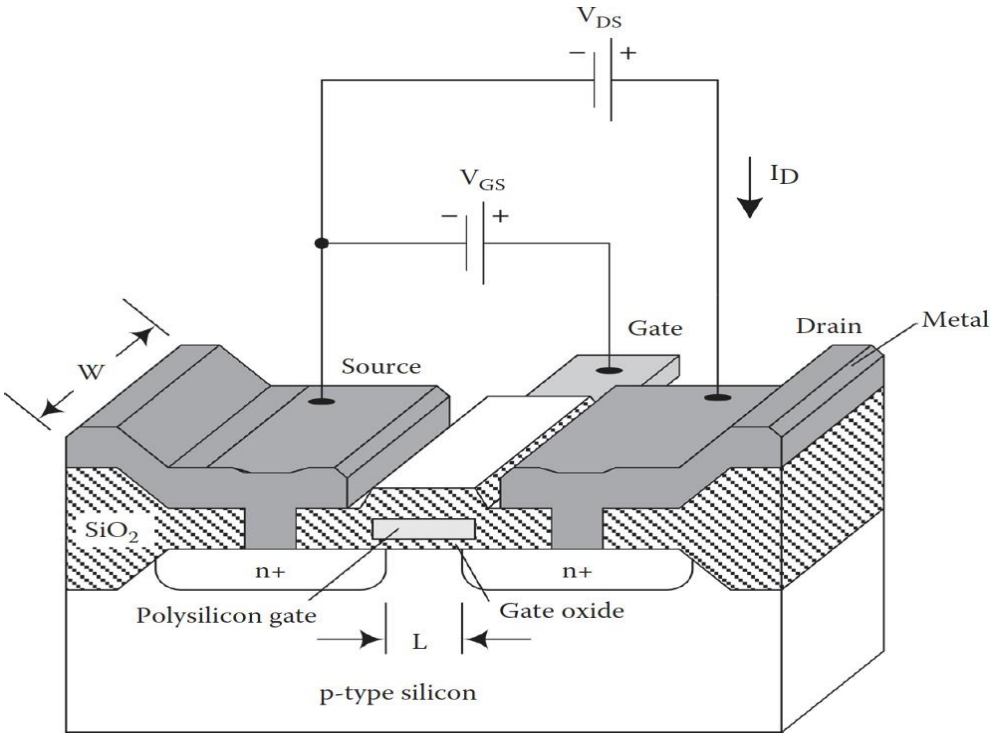




MOSFET I-V CHARACTERISTICS



Output Characteristics of an NMOS



MOSFET I-V CHARACTERISTICS

- **The drain current is assumed to be entering the drain terminal.**
- **Normally, V_{DS}, V_{GS}, and V_{TN} are all positive.**

Drain Current Equations for a Long-Channel n-MOS Transistor

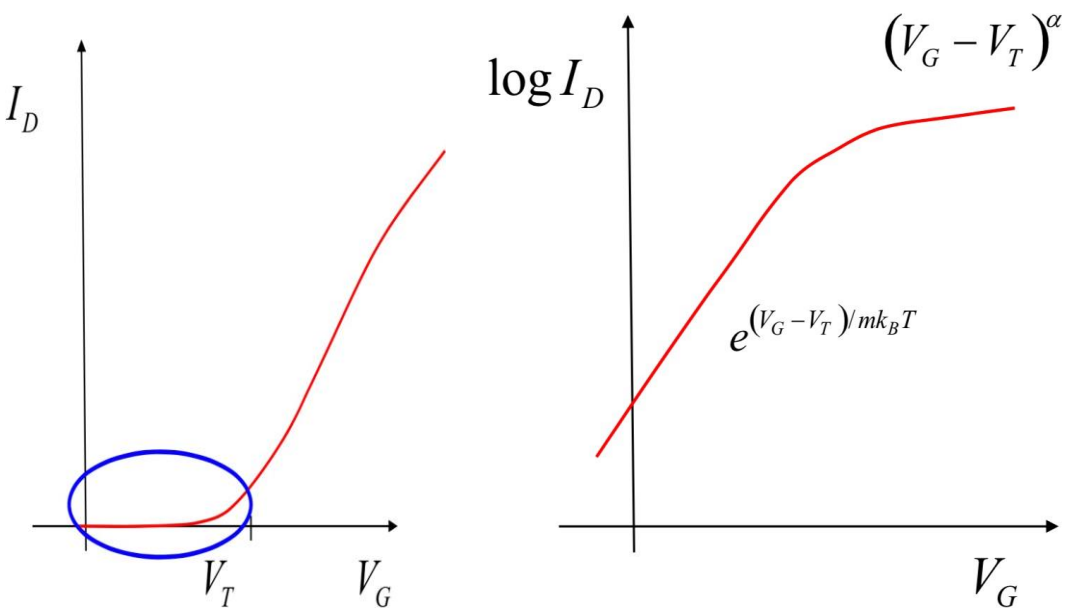
Mode	Drain current equation	Voltage conditions
Cutoff	$I_D \approx 0$	$(V_{GS} - V_{TN}) \le 0$
Linear	$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right]$	$V_{DS} \le (V_{GS} - V_{TN})$
Saturation	$I_D = \mu_n C_{ox} \frac{W}{L}\frac{(V_{GS} - V_{TN})^2}{2}$	$0 \le (V_{GS} - V_{TN}) \le V_{DS}$

- **The drain current is assumed to be leaving the drain terminal.**
- **Normally, V_{DS}, V_{GS}, and V_{TP} are all negative.**

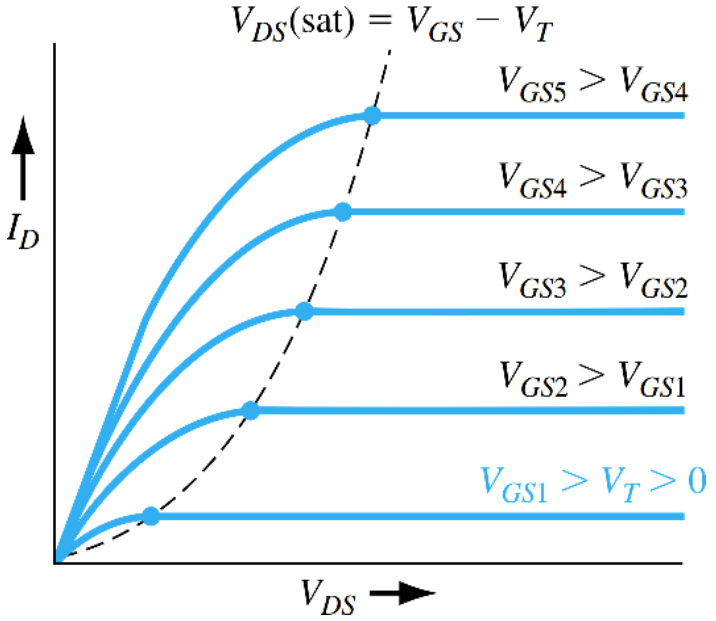
Drain Current Equations for a Long-Channel p-MOS Transistor

Mode	Drain current equation	Voltage conditions
Cutoff	$I_D \approx 0$	$(V_{GS} - V_{TP}) \ge 0$
Linear	$I_D = \mu_p C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TP})V_{DS} - \frac{V_{DS}^2}{2}\right]$	$V_{DS} \ge (V_{GS} - V_{TP})$
Saturation	$I_D = \mu_p C_{ox} \frac{W}{L}\frac{(V_{GS} - V_{TP})^2}{2}$	$0 \ge (V_{GS} - V_{TP}) \ge V_{DS}$

MOSFET I-V CHARACTERISTICS



Transfer Characteristics



Output Characteristics

SUBTHRESHOLD DRAIN CURRENT

Drain current in Subthreshold condition:

$$I_D = \mu_{eff} C_{ox} \left(\frac{W}{L}\right)(m-1)\left(\frac{k_B T}{q}\right)^2 e^{q(V_{GS}-V_T)/mk_BT}\left(1-e^{-qV_{DS}/k_BT}\right)$$

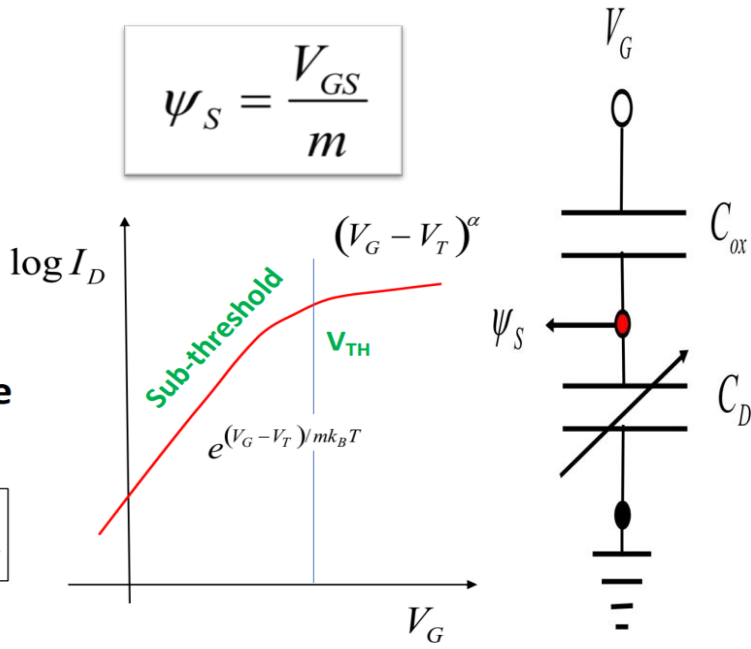
Subthreshold Slope = $\frac{\partial(\log_{10} I_D)}{\partial V_{GS}}$

Subthreshold Swing (S)= $\left[\frac{\partial(\log_{10} I_D)}{\partial V_{GS}}\right]^{-1}$ **= 1/ Subthreshold Slope**

$$S = \left(\frac{\partial(\log_{10} I_D)}{V_{GS}}\right)^{-1} = 2.3m(k_BT/q)\ \frac{\text{mV}}{\text{dec}}$$

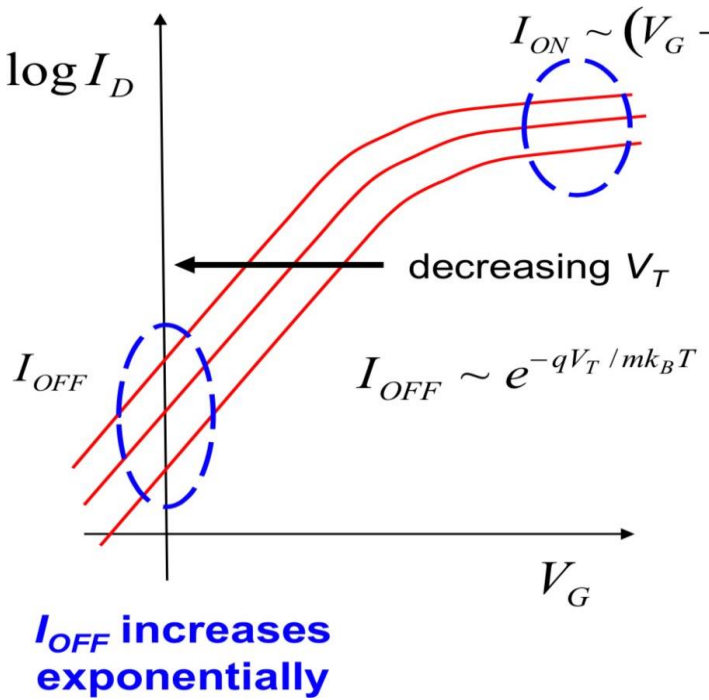
$$m = 1 + C_D / C_{ox}$$

$$\psi_S = \frac{V_{GS}}{m}$$



Sminimum **= 60 mV/dec → Boltzmann Limit**

OFF CURRENT, SUBTHRESHOLD SLOPE & V_{TH}



I_{ON} increases ~ linearly

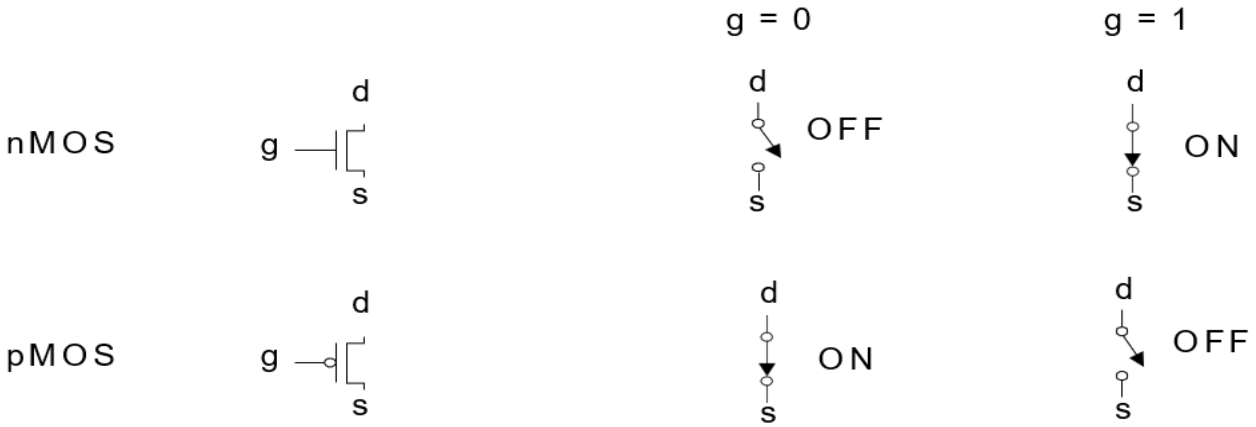
Small increase in I_{ON} leads to large increase in I_{OFF}

POWER SUPPLY VOLTAGE

- Ground (GND) = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny (sub 100 nm) transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

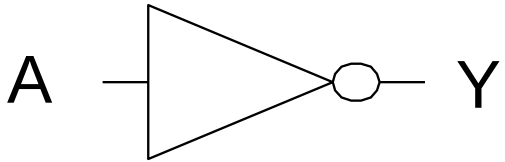
TRANSISTORS AS SWITCHES

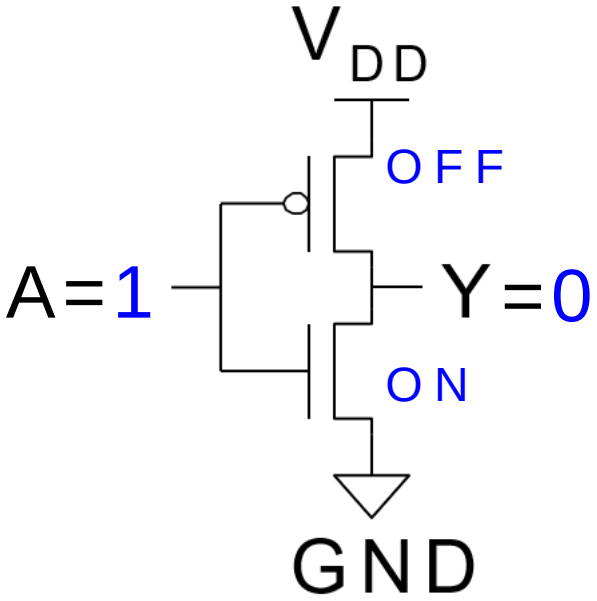
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS INVERTER (NOT GATE)

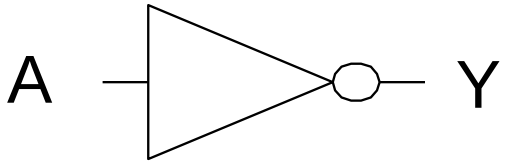
A	Y
0	
1	0

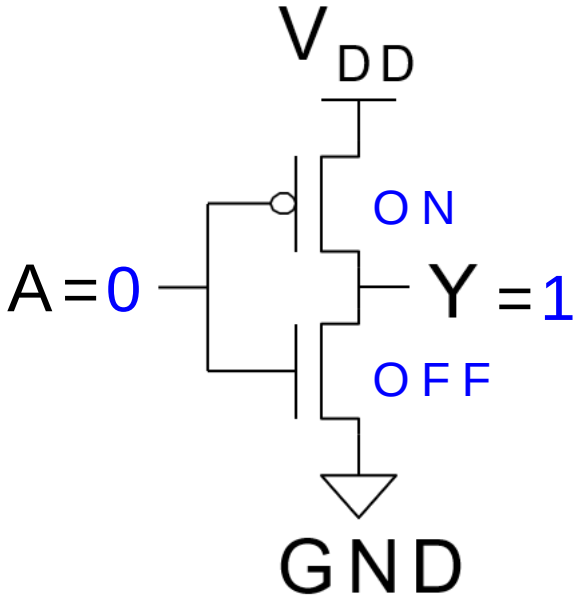




CMOS INVERTER (NOT GATE)

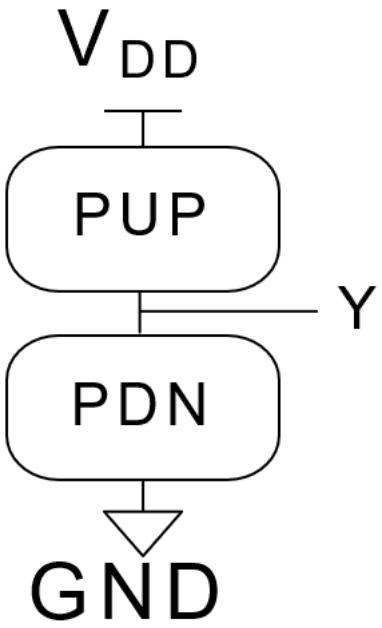
A	Y
0	1
1	0





MORE COMPLEX CIRCUITS: PUP AND PDN

- Pull-up net (PUP) off when pull-down (PDN) on
- PUP implemented as complement of PDN (Complementary MOS)
- If two FETs in parallel in PDN, counterparts in series in PUP
- Output (Y) connected to VDD or GND, never both



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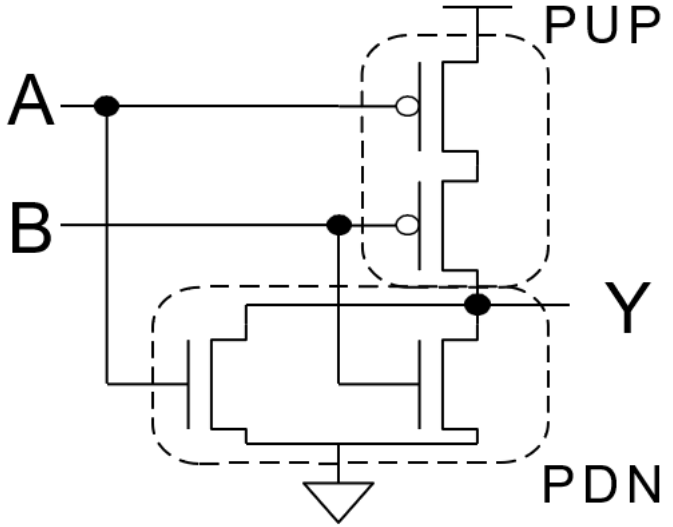
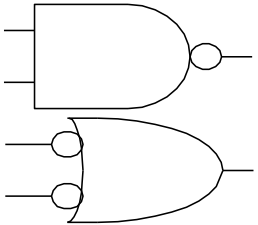
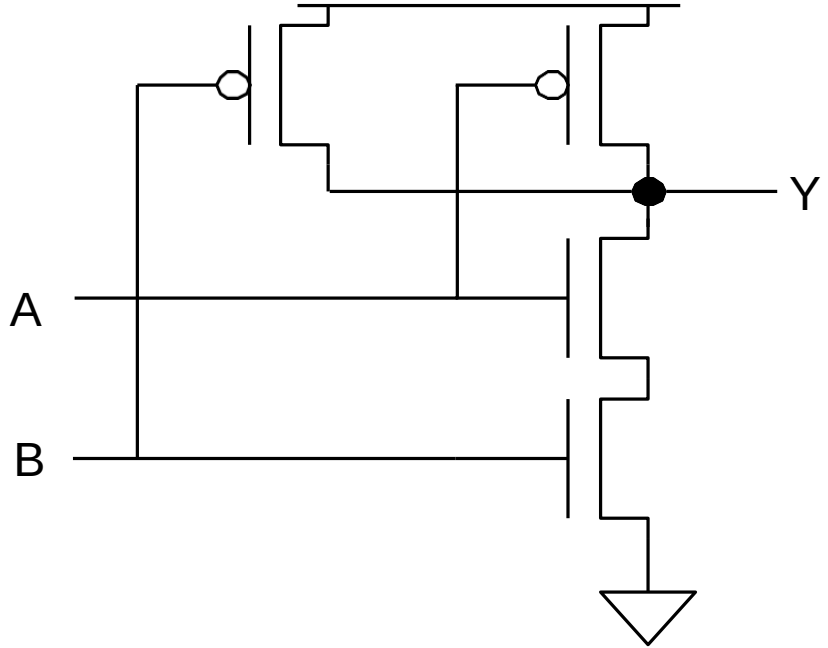


CMOS NAND GATE

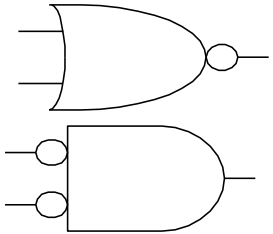
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

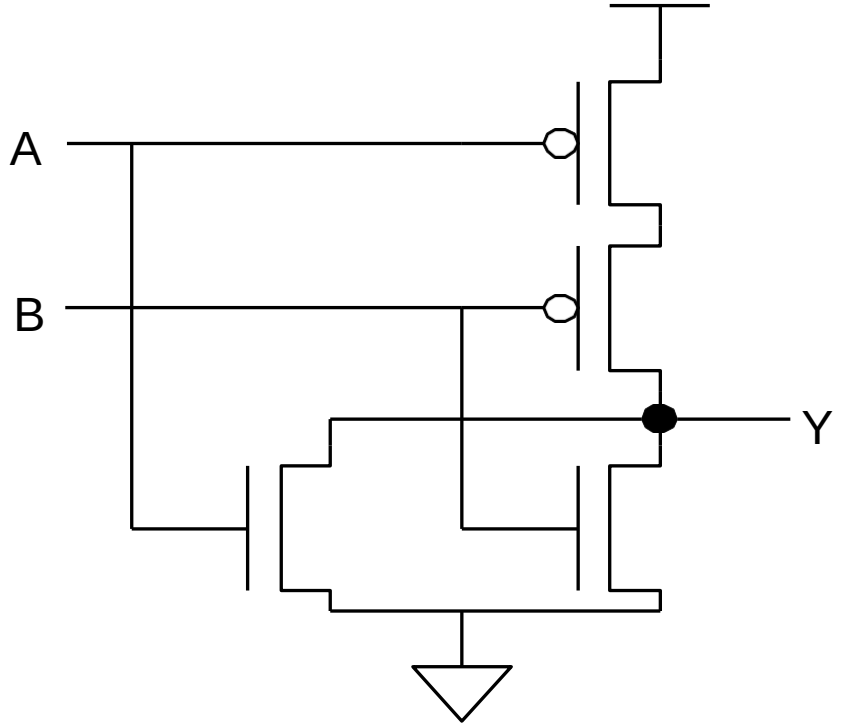




CMOS NOR GATE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





Thank you!