CAL POLY
SAN LUIS OBISPO

EE 531: ADVANCED VLSI DESIGN

Chip Finishing and Signoff

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March, 2025

Sign Off Timing

ADDITIONAL TIMING MARGINS

- Remember those pesky timing margins, we mentioned in the lecture about static timing analysis?

$$T + \delta_{skew} > t_{CQ} + t_{logic} + t_{setup} + \delta_{margin}$$

$$t_{CQ} + t_{logic} - \delta_{margin} > t_{hold} + \delta_{skew}$$

  - Well, we discussed skew and jitter, but is that all?
  - If it was, there's a good chance that all the CAD engineers could retire…

- So what/why/how do we apply additional timing margins?

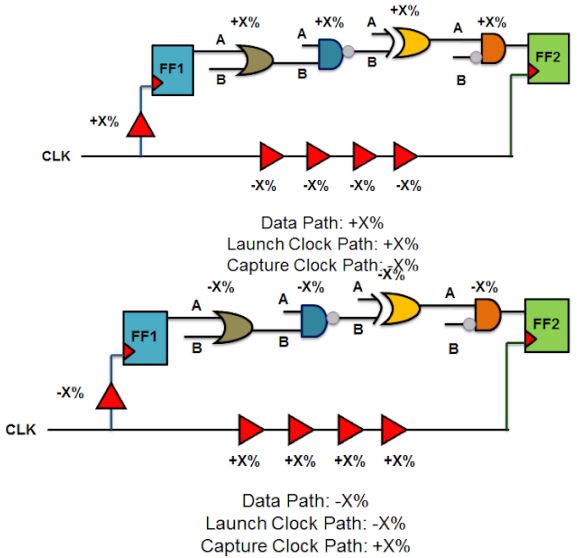
BEST CASE-WORST CASE (BC-WC) TIMING

- This is the straightforward and traditional way to run STA:
  - Max-delay (setup) checks are run on worst-case (slow) conditions.
  - Min-delay (hold) checks are run on best-case (fast) conditions.
- However, it doesn't take into account variation that can occur across the chip, for example, due to a temperature variance.

ON CHIP VARIATION

- Spatial variation
  - Chips are “big” and delay elements can be far from each other.
  - Process/Voltage/Temperature (PVT) variation can affect different parts of the timing path in opposite directions.
  - So, why don’t we just assume the worst possible case
- During setup:
  - The launch (data) path is extra slow.
  - The capture (clock) path is super fast.

```
set_timing_derate –max -early 0.9 -late 1.2
```



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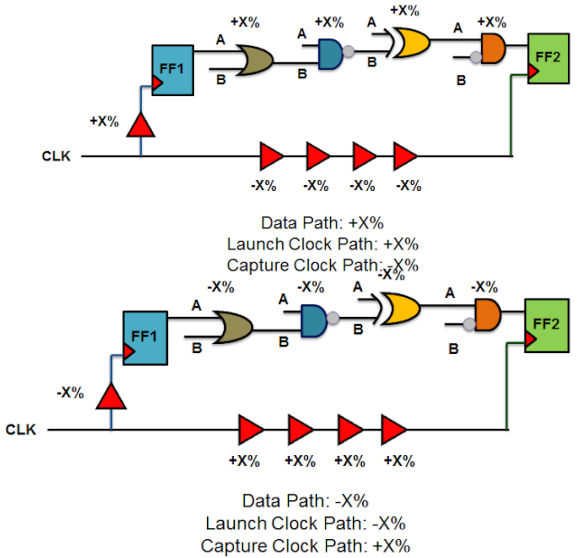
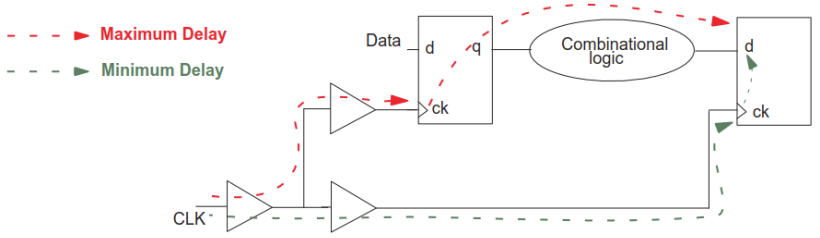


ULTRA PESSIMISM…

- A common practice in VLSI design implementation is to be over pessimistic.
  - If you are optimistic, your chip may not work.
  - If you over-design, your yield will go up.
- But over pessimism is painful
  - Time-to-market increases
  - Performance is hindered
  - Less efficient in all parameters: size, power, performance



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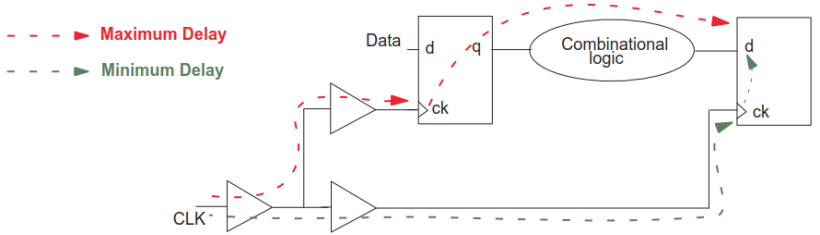
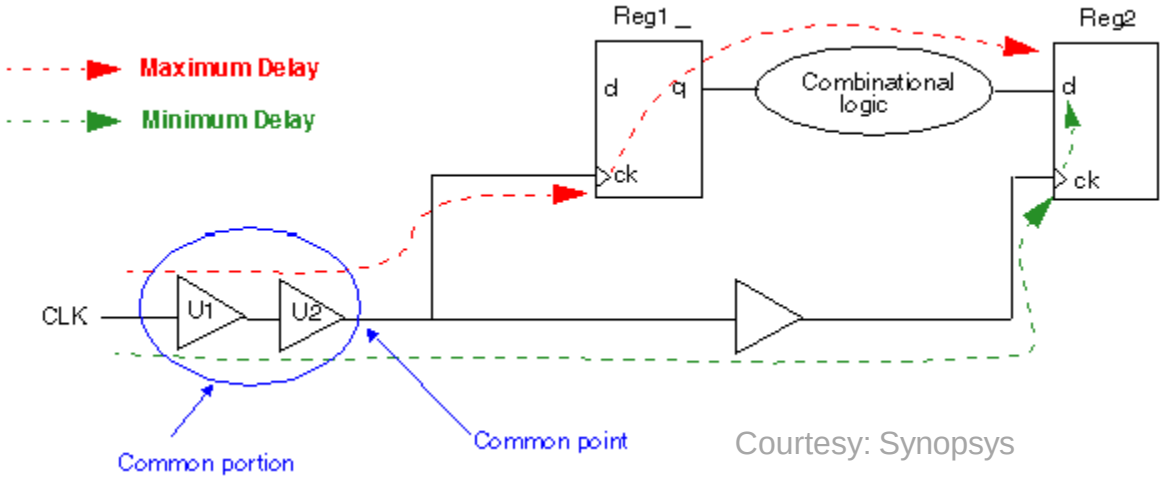


- So, we have to ask, can the defined OCV methodology actually occur?
  - We choose one library (slow/fast) for data and another (fast/slow) for clock…
  - We then add derating on top of that!
- Well, that's too harsh… let's recover some of our pessimism!

CLOCK RECONVERGENCE PESSIMISM REMOVAL

- To limit the pessimism of OCV, apply CRPR
  - This basically removes the derating from the clock path shared by both the launch and capture paths.



ADVANCED ON-CHIP VARIATION (AOCV)

- Well, CPPR helped, but those derates are gruesome.
  - Do all paths derate the same?
- No, variation is statistical…
  - But statistical behavior is hard to compute.
  - So, let's do something easier.

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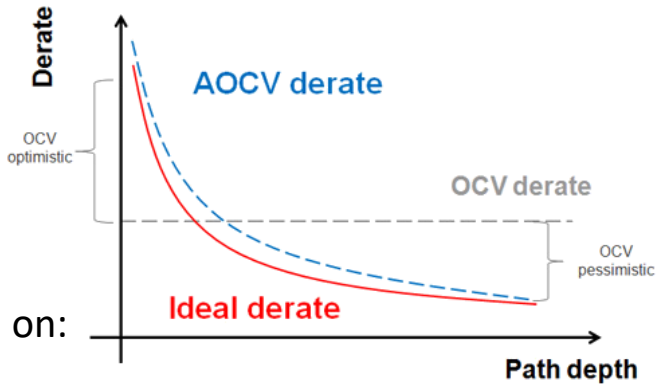
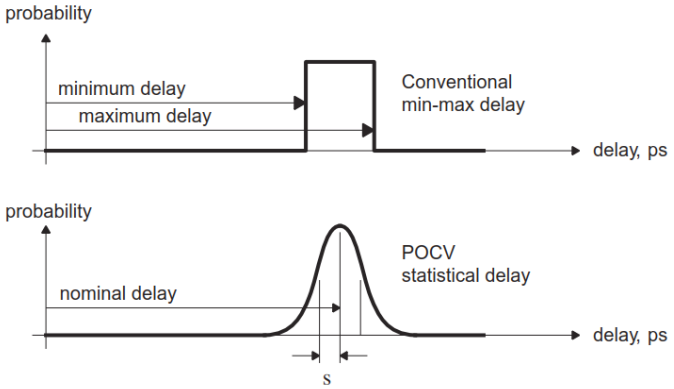
  - Do all paths derate the same?
- No, variation is statistical…
  - But statistical behavior is hard to compute.
  - So, let's do something easier.
- Someone noticed that worst-case conditions in a path depend on:
  - Distance between gates on the path
  - Depth (number of stages) of the path
- So let's provide libraries with new derating factors based on these factors.
  - We'll call it "Advanced On-Chip Variation"!



PARAMETRIC ON-CHIP VARIATION (POCV)

- AOCV is cool!
  - But still too pessimistic…
  - Remember, variation is statistical.
  - And is different for each gate.
- Well, let's just run Monte Carlo simulations for every path!
  - Yeah… that's known as Statistical STA (SSTA)
  - But it's really computationally intensive.



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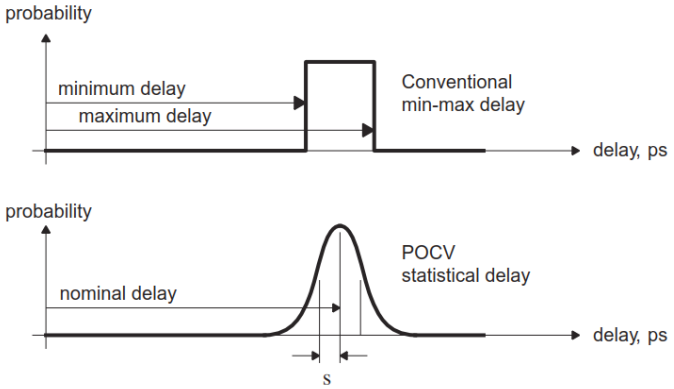
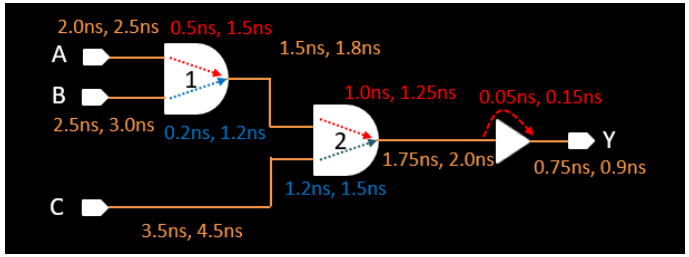
- Well, let's just run Monte Carlo simulations for every path!
  - Yeah… that's known as Statistical STA (SSTA)
  - But it's really computationally intensive.
- So, I guess we'll have to be more realistic.
  - Let's just provide a distribution for each gate in the library.
  - Then calculate the delay according to the gates in the path.
  - This is known as Parametric OCV (POCV) or Statistical OCV (SOCV)



PATH-BASED ANALYSIS

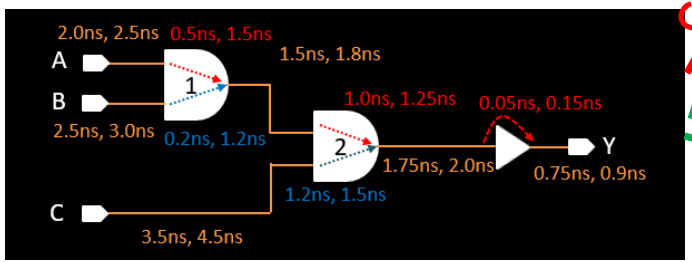
- Another point of pessimism removal is to run Path-based Analysis (PBA)
- Due to long runtimes, STA is usually run with Graph-based Analysis (GBA)



source:
vlsi-expert.com

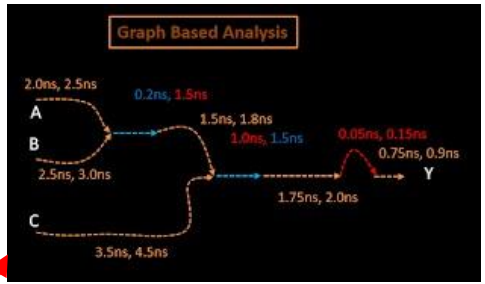
PATH-BASED ANALYSIS

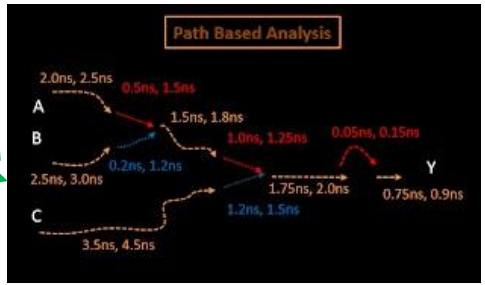
- Another point of pessimism removal is to run Path-based Analysis (PBA)
- Due to long runtimes, STA is usually run with Graph-based Analysis (GBA)
- What is the difference?
  - GBA chooses the worst-case propagation from all inputs through a gate
  - PBA chooses the propagation of the specific path
  - This results in a 10X longer run time but highly reduced pessimism



GBA

PBA





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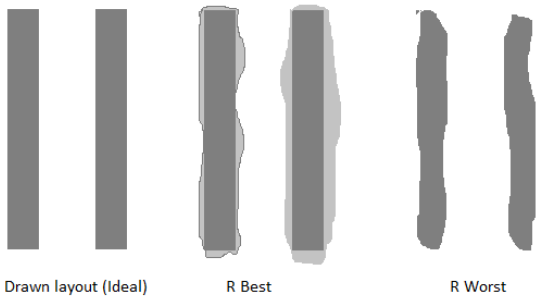
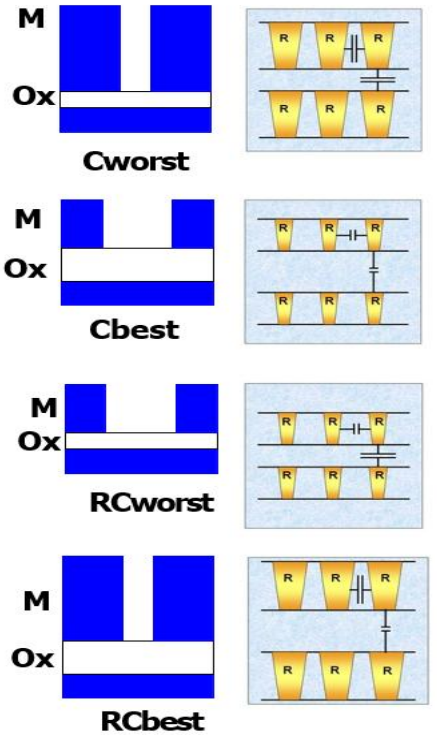
RC EXTRACTION

- Usually done with several extraction options:
  - Cworst
    - Min metal spacing, Tall wires, Max surface area
  - Cbest
    - Max metal spacing, Short wires, Min surface area



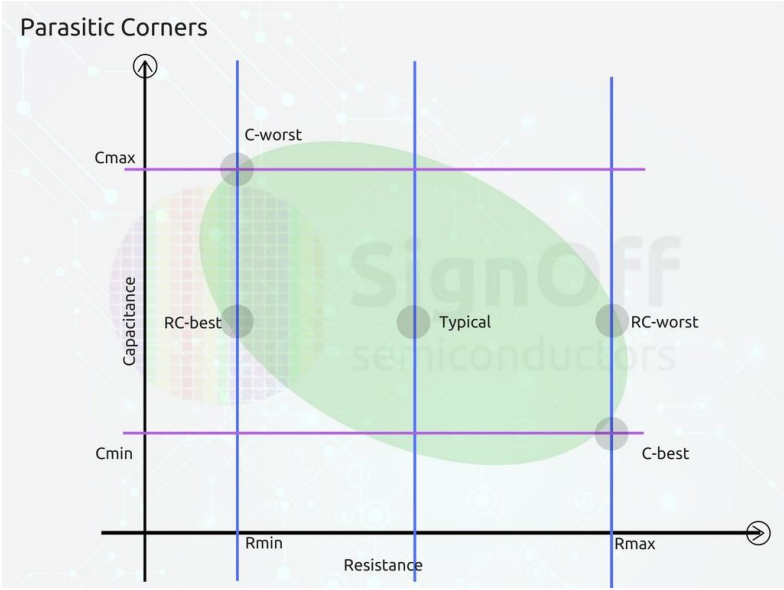
RC EXTRACTION

- Usually done with several extraction options:
  - Cworst
    - Min metal spacing, Tall wires, Max surface area
  - Cbest
    - Max metal spacing, Short wires, Min surface area
  - RCworst
    - Min Inter-layer metal spacing, Max Intra-layer spacing
    - Long wires, Min surface area
  - RCbest
    - Max Inter-layer metal spacing, Min Intra-layer spacing
    - Short wires, Max surface area



RC EXTRACTION

- How do these affect RC values?
  - **Cworst**: Max C, Min R
  - **Cbest**: Min C, Max R
  - **RCworst**: Max R, Wide wires: Max C, Narrow wires: Min C
  - **RCbest**: Min R, Wide wires: Min C, Narrow wires: Max C



Source: signoffsemi.com

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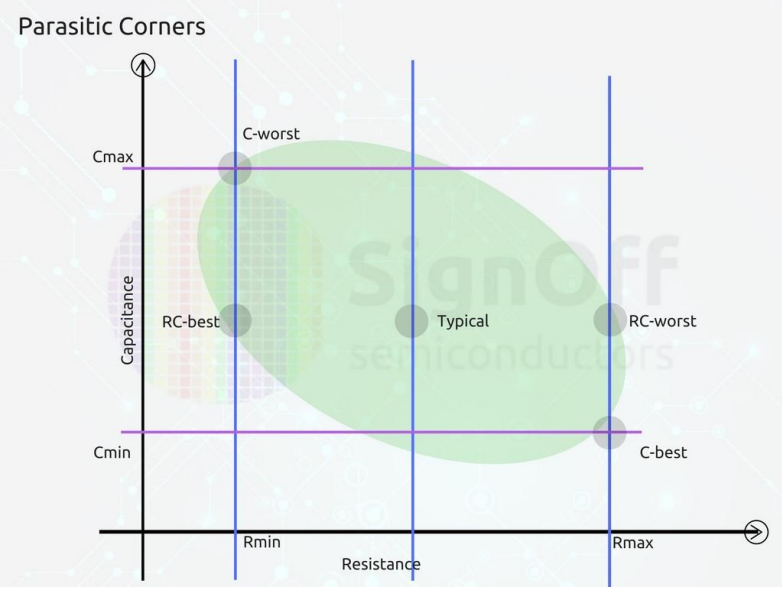
  - **Cworst**: Max C, Min R
  - **Cbest**: Min C, Max R
  - **RCworst**: Max R, Wide wires: Max C, Narrow wires: Min C
  - **RCbest**: Min R, Wide wires: Min C, Narrow wires: Max C
- Which corner to use?
  - Only C affects the cell delay…
  - Maybe use Cworst for setup, Cbest for hold.
  - RCbest, RCworst for long interconnects



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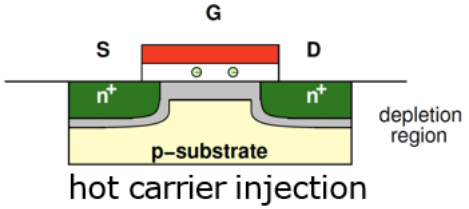
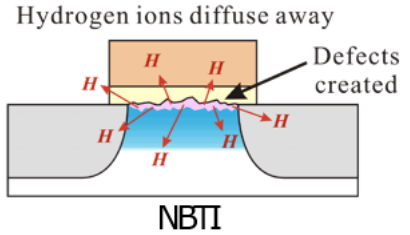
A NOTE ABOUT AGING

- Another big issue in modern VLSI design is aging
  - Device characteristics change over time.
  - Hot Carrier Injection (HCI)
  - Negative Bias Temperature Instability (NBTI)
  - Time Dependent Dielectric Breakdown (TDDB)
  - Electromigration



hot carrier injection



NBTI

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  - Device characteristics change over time.
  - Hot Carrier Injection (HCI)
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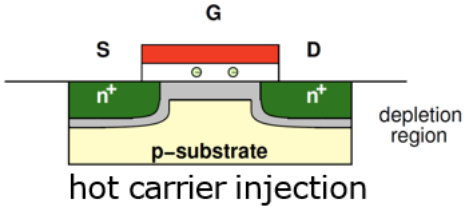
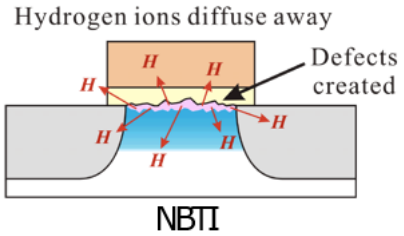
  - Electromigration
- Dealing with aging effects:
  - Operate with low VDD.
  - Model aging as an additional timing margin.
  - Use aged library models for signoff timing.
  - Add aging sensors and adjust frequency/voltage for compensation.





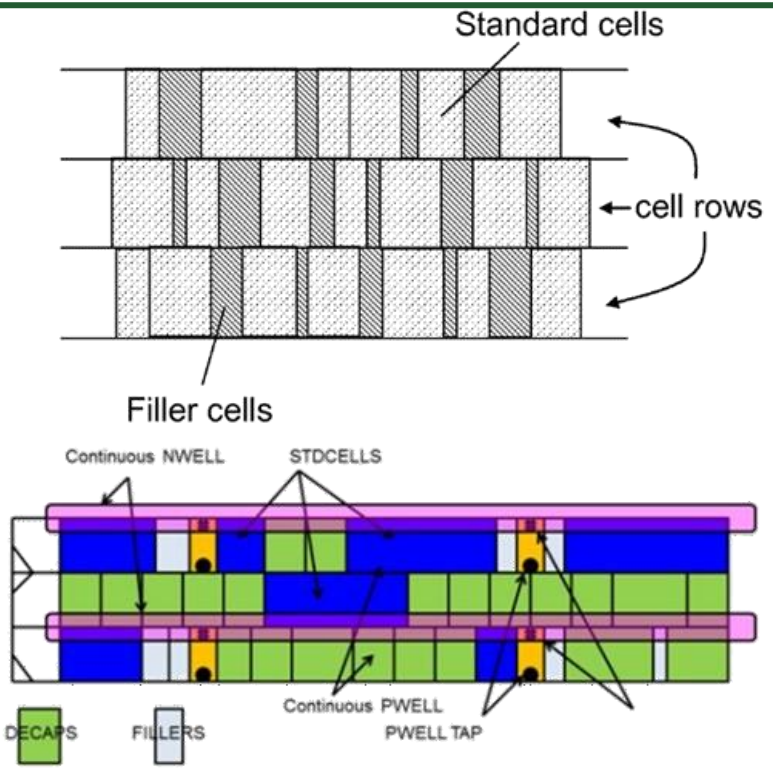
Chip Finishing and Sign-off

CHIP FINISHING OVERVIEW

- Chip Finishing for Signoff includes, at the very least:
  - Insertion of fillers and DeCaps.
  - Application of Design for Manufacturing (DFM) and Design for Yield (DFY) rules.
  - Antenna checking.
  - Metal filling and slotting for metal density rules.
  - IR Drop and Electromigration Analysis
  - Logic Equivalence
  - Layout (Physical) Verification
  - Add Sealring

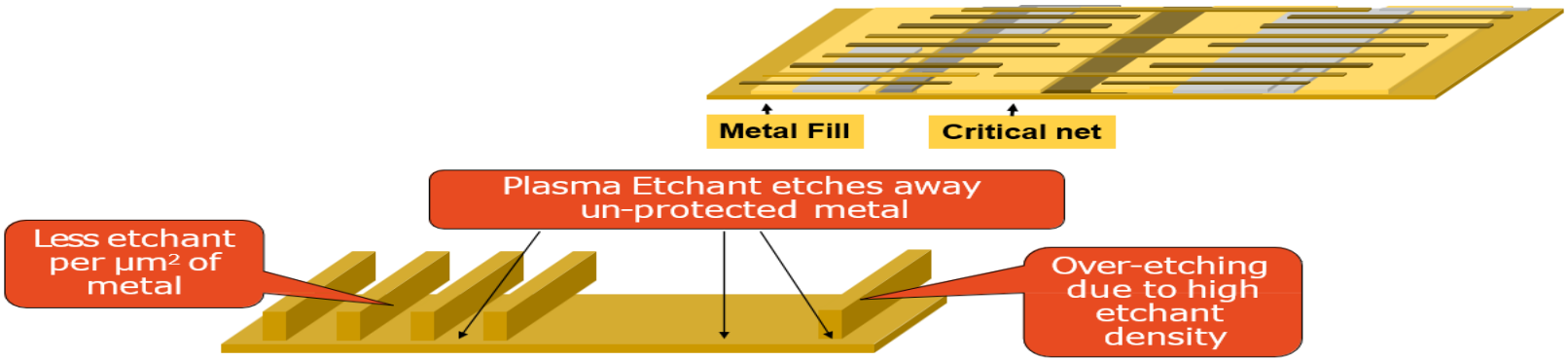
FILLER CELL INSERTION

- Standard cell placement never reaches 100% utilization.
- We need to “fill in the blanks”
  - Ensure continuous wells across the entire row.
  - Ensure VDD/GND rails (follow pins) are fully connected.
  - Ensure proper GDS layers to pass DRC.
  - Ensure sufficient diffusion and poly densities.
  - In scaled processes, provide regular poly/diffusion patterning.
- We can also add DeCap cells as fillers.



METAL DENSITY FILL

- Density issues due to etching:
  - A narrow metal wire separated from other metal receives a higher density of etchant than closely spaced wires, such that the narrow metal can get over-etched.
- Solution:
  - Minimum metal density rules
  - But, be aware of critical nets!



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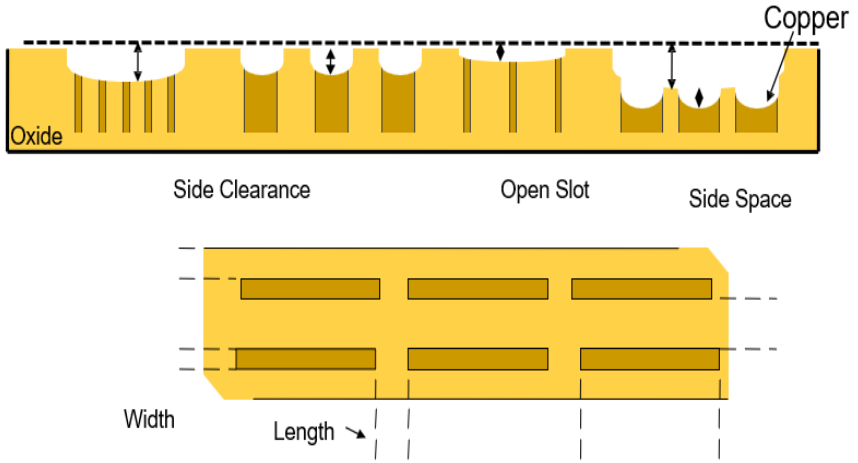
- Density issues due to CMP:
  - Chemical Mechanical Polishing (CMP) is the stage during which the wafer is planarized.
  - Since metals are mechanically softer than dielectrics, metal tops are susceptible to "dishing", and very wide metals become thin (erosion).



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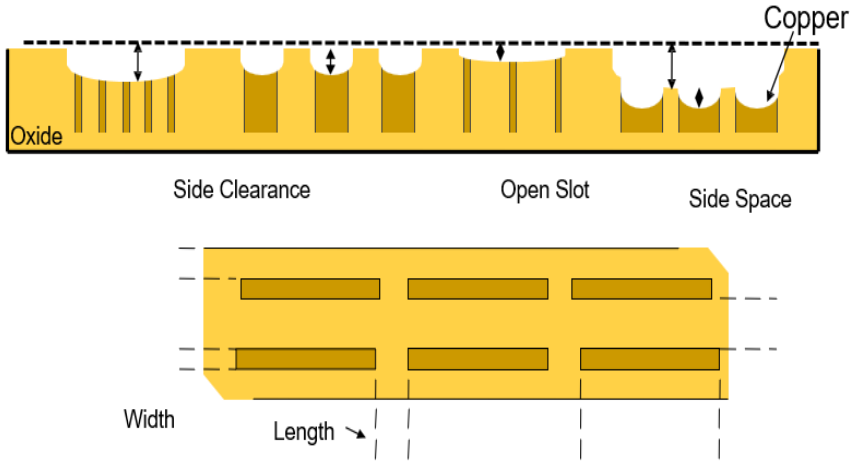
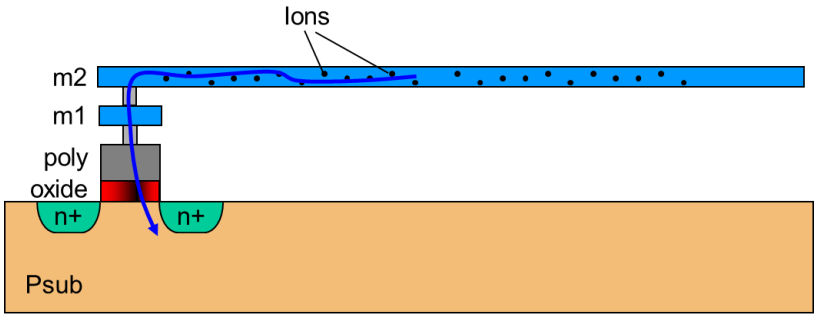
  - Since metals are mechanically softer than dielectrics, metal tops are susceptible to "dishing", and very wide metals become thin (erosion).
- Solution:
  - Maximum metal density rules
  - Apply "Slotting"
  - Also solves "metal liftoff" problems.



ANTENNA FIXING

- Antenna Hazards:
  - During metal etch, strong EM fields are used to stimulate the plasma etchant resulting in voltage gradients at MOSFET gates that can damage the thin oxide
  - Antenna hazards occur when the ratio of the metal area to gate area during a process step is large.

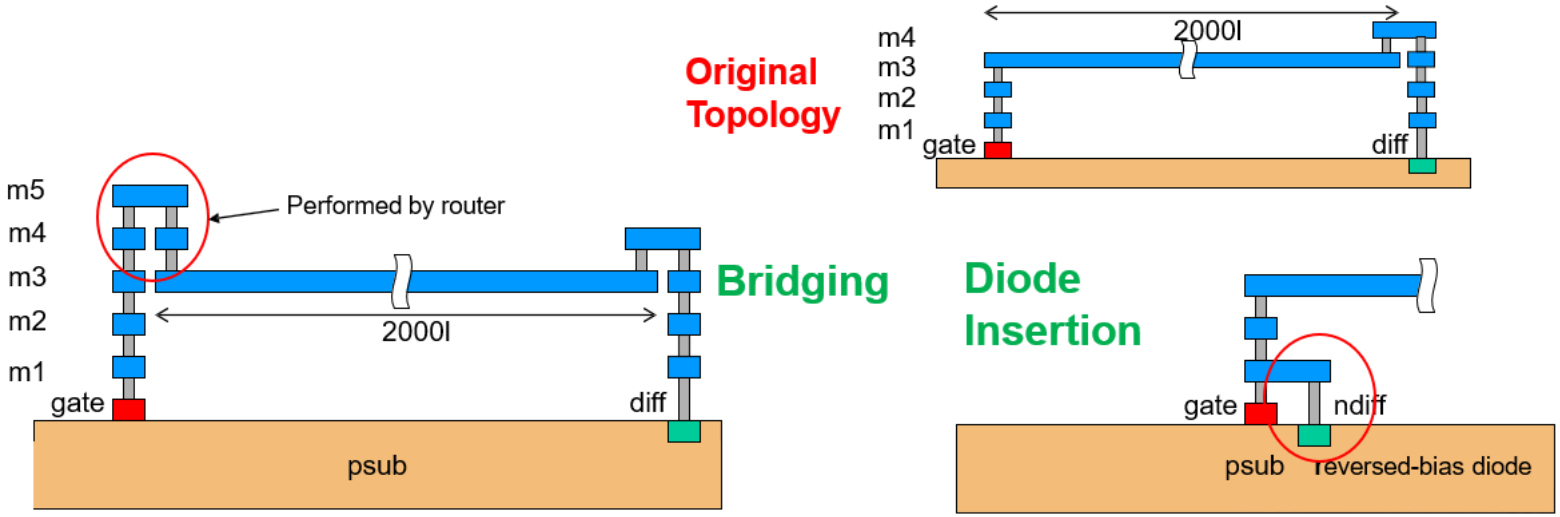


Antenna Ratios:

Area of Metal Connected to Gate
Combined Area of Gate
Or
Area of Metal Connected to Gate
Combined Perimeter of Gate

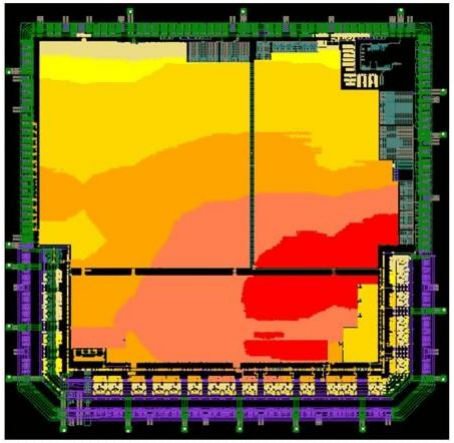
ANTENNA FIXING

- Fixing Antenna Problems:

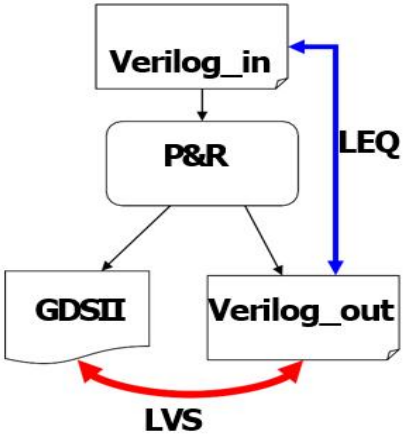


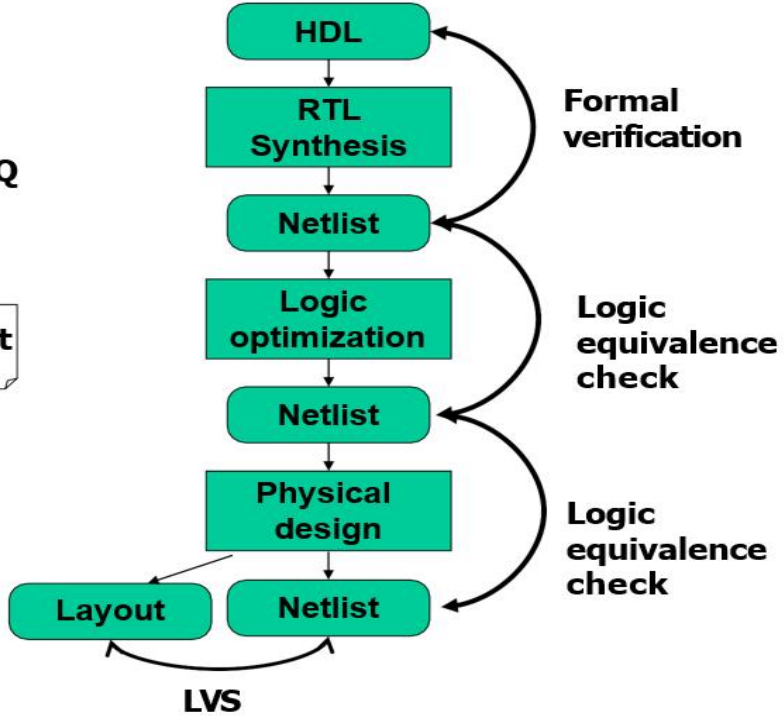
IR DROP AND EM ANALYSIS

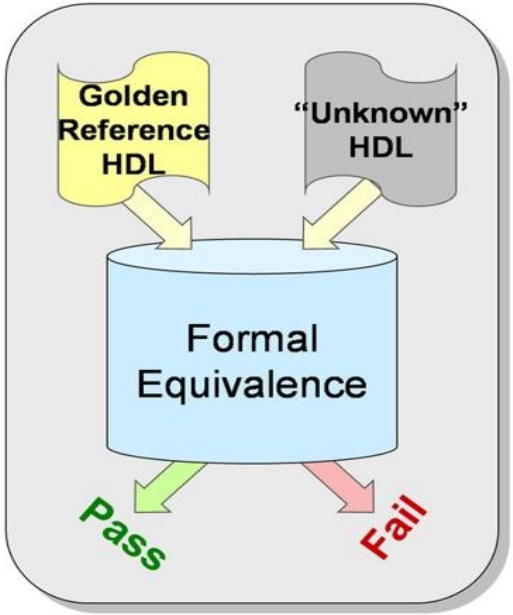
- Static IR drop analysis:
  - Average voltage drop assuming constant current.
  - Insufficient for modern technologies.
- Dynamic IR drop analysis:
  - Depends on switching activity of the logic.
  - Is vector dependent, using VCD files produced with SDF timing data.
  - Analyzes peak current demand.
  - Often run at FF corner, high VDD, high temp, RCWorst extraction.
- Electromigration Analysis
  - Check current density.
  - Focuses on power lines, but “Signal EM” is also required nowadays.



LOGIC EQUIVALENCE







LAYOUT (PHYSICAL) VERIFICATION

- Design Rule Check (DRC)
  - DRC run at the fullchip level on a sign-off DRC Tool.
  - Extra checks for fullchip are considered, including DFM recommended rules.
  - Applied to GDS streamed out from P&R tool with the addition of bonding pads, density fillers, top-level markings, sealring, and labels.

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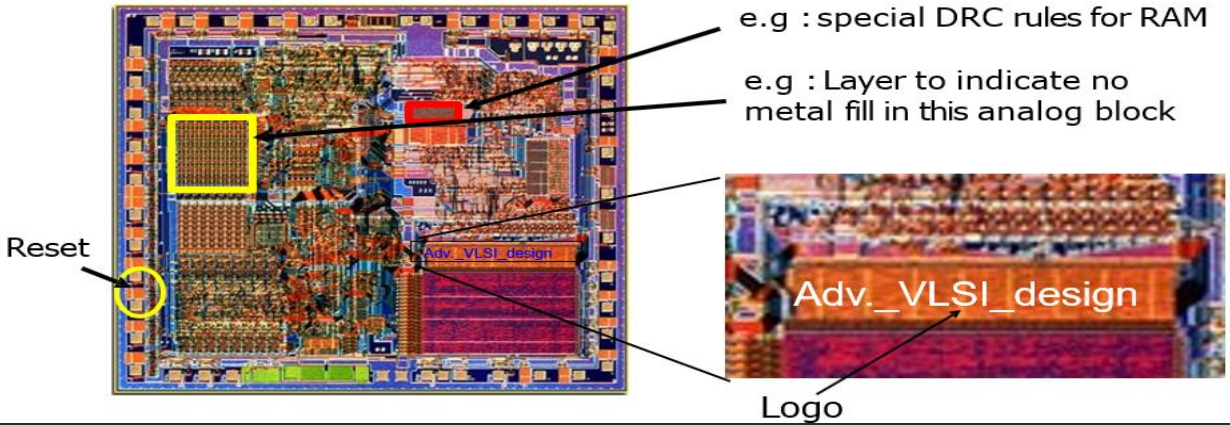
- Layout vs Schematic (LVS)
  - Extract layout (GDS) and build Spice netlist
  - Sometimes need to black-box sensitive layouts.
  - Export Verilog and translate into Spice netlist
  - Compare the two with a sign-off LVS tool.
- Electrical Rule Check (ERC)
  - Part of LVS. Checks for shorts, floating nets, well biasing.

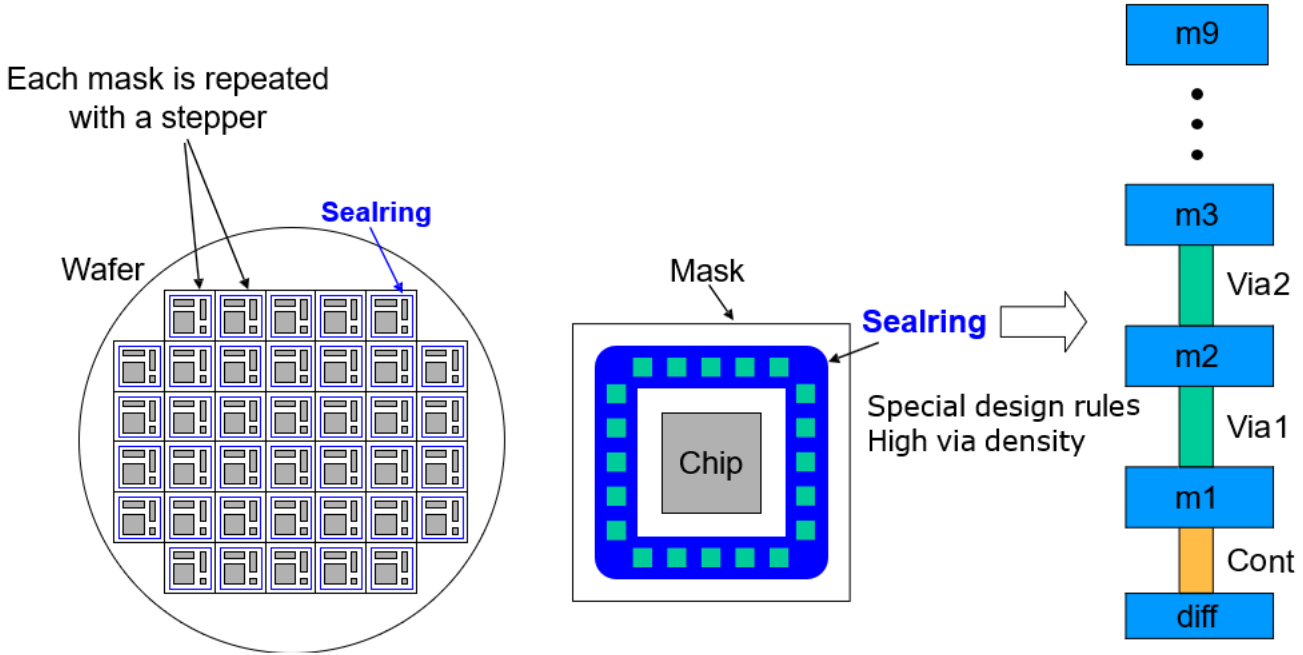
LAYOUT (PHYSICAL) VERIFICATION

- Special GDS additions for tapeout:
  - Special marker layers are used by DRC and LVS
  - Text labels are used for LVS and for commenting
  - Chip logo added in top-layer for identification
  - Reticle alignment or “fiducial” markings for alignment.



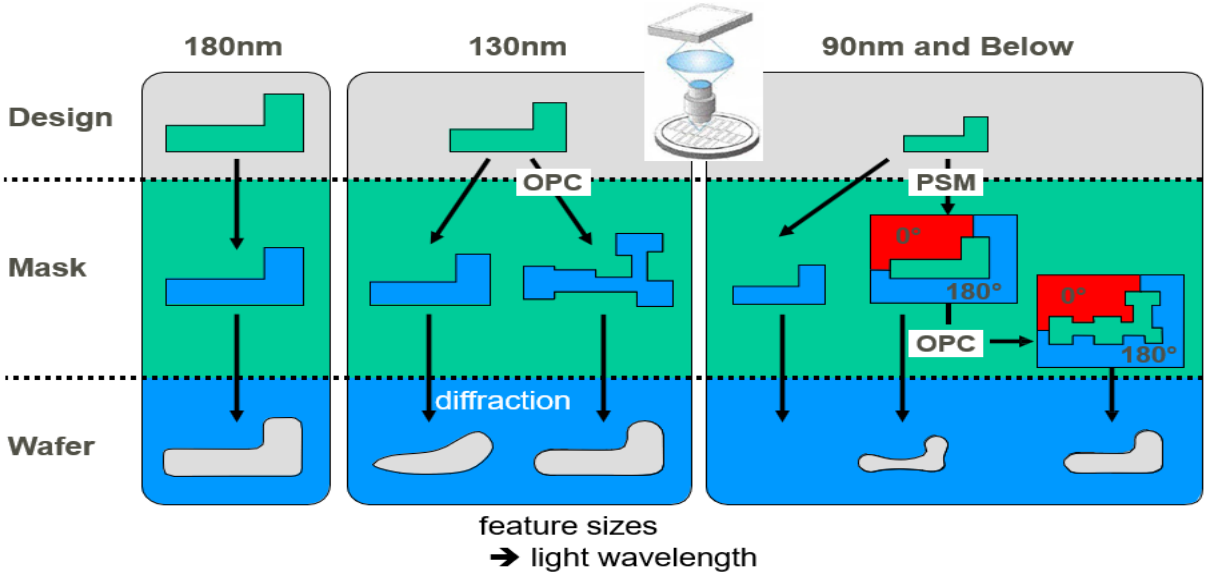
ADDING A SEALRING

- To protect the chip from damaging during dicing (sawing), a sealring is added around the periphery.



RESOLUTION ENHANCEMENT TECHNIQUES (RET)

- Before writing the mask, additional transformations are applied to the GDS:
  - Optical Proximity Correction (OPC)
  - Phase Shift Masks (PSM)



Thank you!