

Lab1- Introduction to UMS GH15 PDK

Joe Schultz & Anurag Bhargava

Jan. 8, 2026

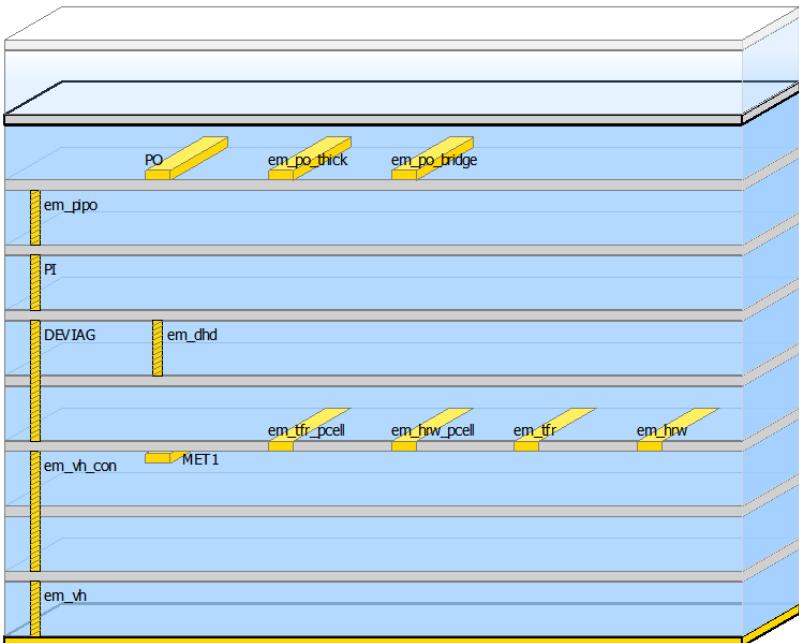
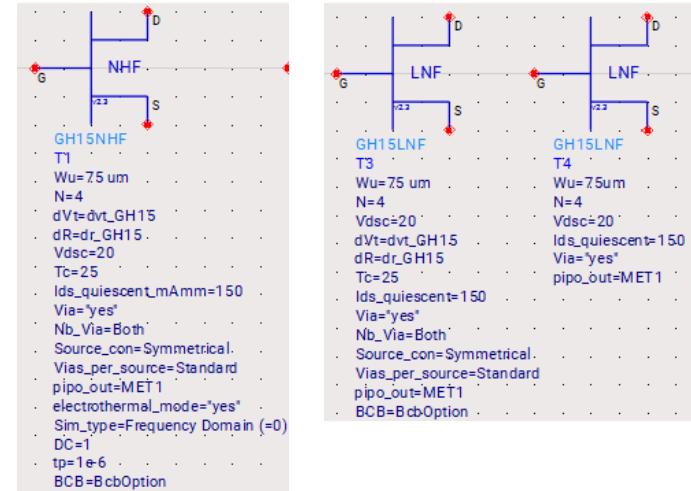
Lab 1 Overview

Objectives and Purpose

- Lab 1 will introduce the United Monolithic Semiconductors (UMS) 150nm GaN Process Design Kit (PDK) in Keysight's Advance Design System (ADS)
 - UMS website: <https://www.ums-rf.com/>
 - UMS Product Examples: <https://www.ums-rf.com/products/>
 - UMS Design Kits: <https://my.ums-rf.com/login/>
- Lab1 steps are:
 1. Create an ADS workspace “pdk_analysis” and install the PDK
 2. Inspect the component palette & parameters; place components (schematic & layout)
 3. Simulate Passive components: a)Spiral, b) MIM Cap, c) Thin Film Resistors, d) MLIN,
- Students should follow along the best they can. The lab will be recorded allowing students to return to the video and follow through the steps.

UMS GH15-1x Process and Device Model *

- Process Used: UMS GH15-11 (v2.3) 150 nm gate length AlGaN/GaN process
- Active Devices Used:
 - LNA = GH15LNF_NOFP & GH15NHF_NOFP; Linear noise model & non-linear model of transistor without field plate for low noise amplifier applications.
 - PA=GH15NHF: " non-linear transistor model for power amplifier applications
- The substrate technology used includes BCB



MSub

```
MSUB  
MSub_MET1  
H=70 um  
Er=10.42  
Mur=1  
Cond=2.5e7  
Hu=3.9e+34 um  
T=2 um  
TanD=0.0015  
Rough=0 um  
FreqForEpsrTanD=2.1 GHz  
LowFreqForTanD=2 GHz  
HighFreqForTanD=8 GHz  
Bbase=  
Dpeaks=
```

GH15LNF noise capability validation domain	
Maturity level	Confirmed
Technology versions	All
Number of gate fingers	4, 6, 8 fingers
Unit gate width	20 µm to 50 µm
Frequency	6 GHz – 40 GHz
Drain voltage bias	5V to 20V
Drain current operating point	50 to 150 mA/mm
Temperature (SiC substrate)	25 °C

* Ref: UMS_GH15-1x_Design_manual_v3.0 - SP_30S_Electrical_Models_GH15-1x.pdf

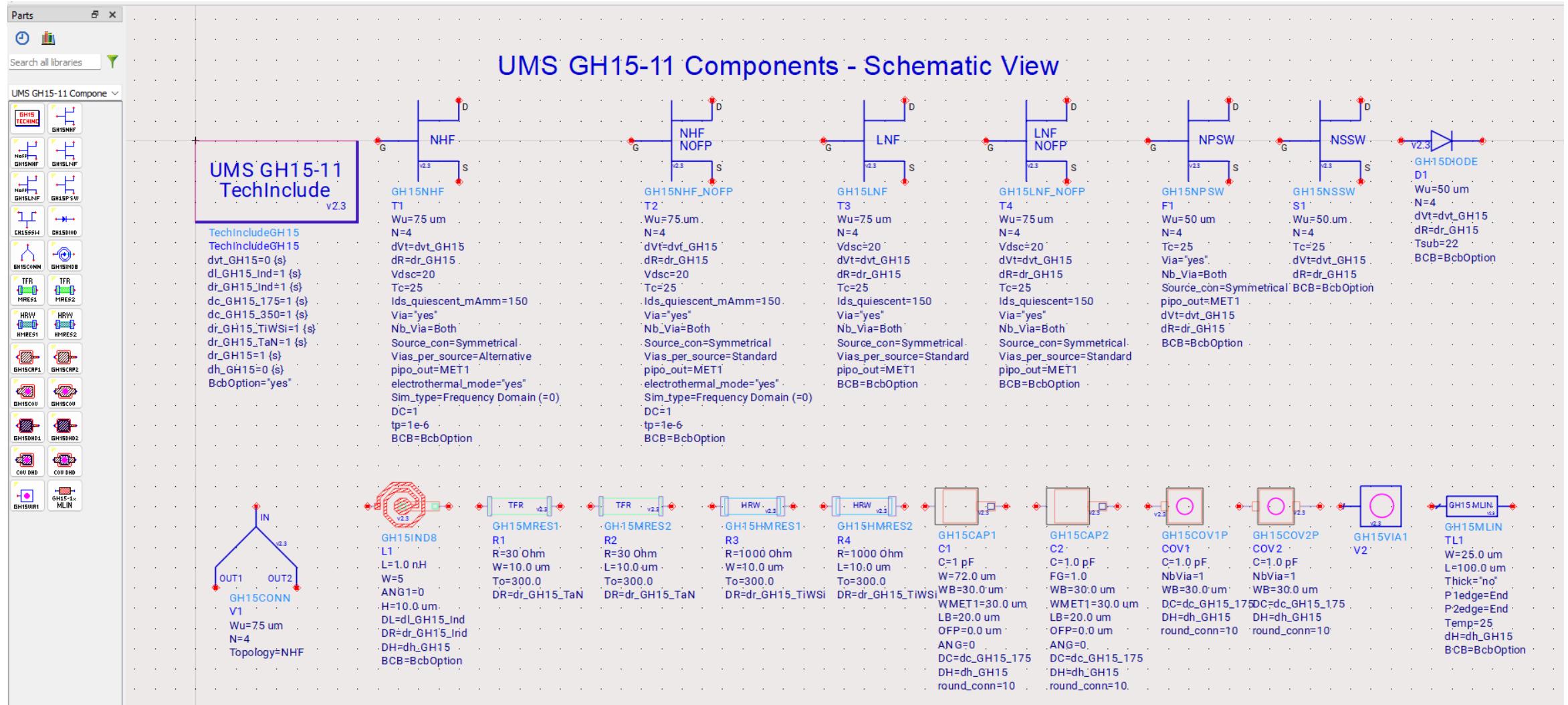
Lab 1, Steps 1 & 2

Create Workspace and Review PDK

UMS PDK install, schematic, layout, 2-to-3D

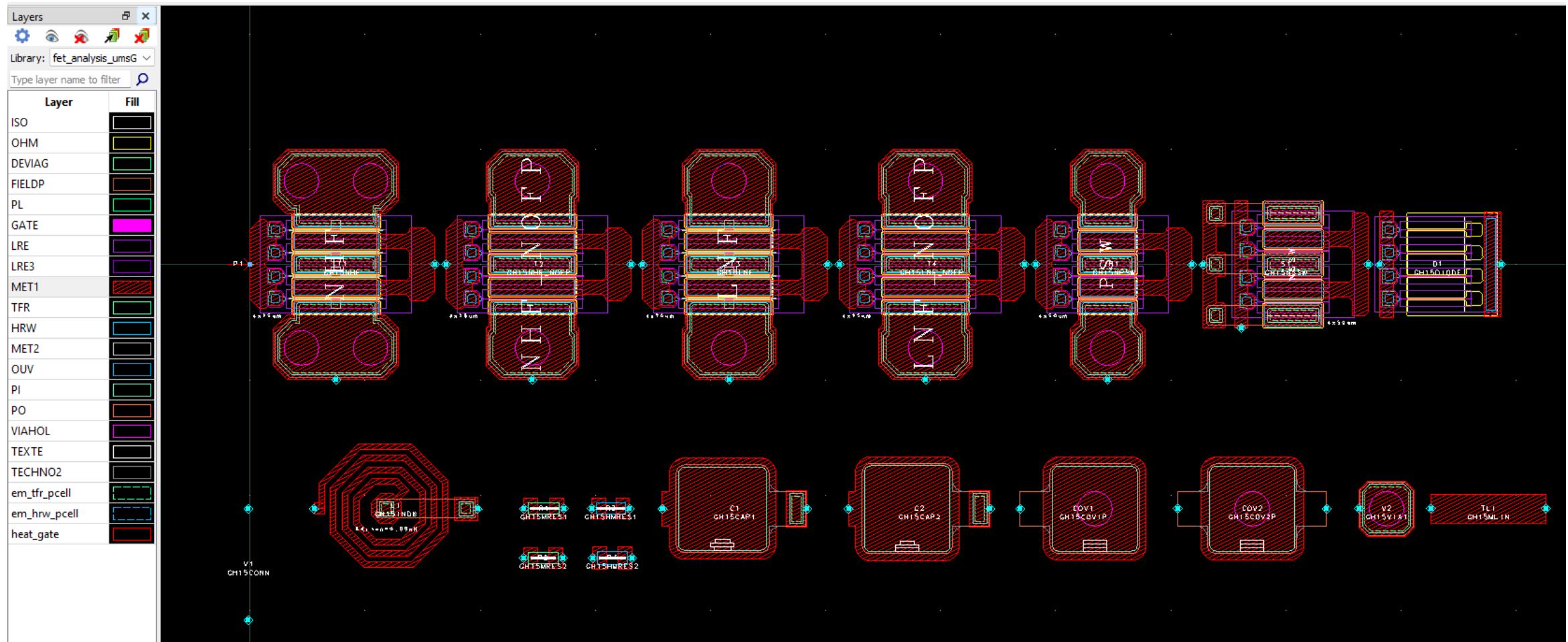
UMS GH15-11 ADS Components

Schematic View



UMS GH15-11 ADS Components

Layout View



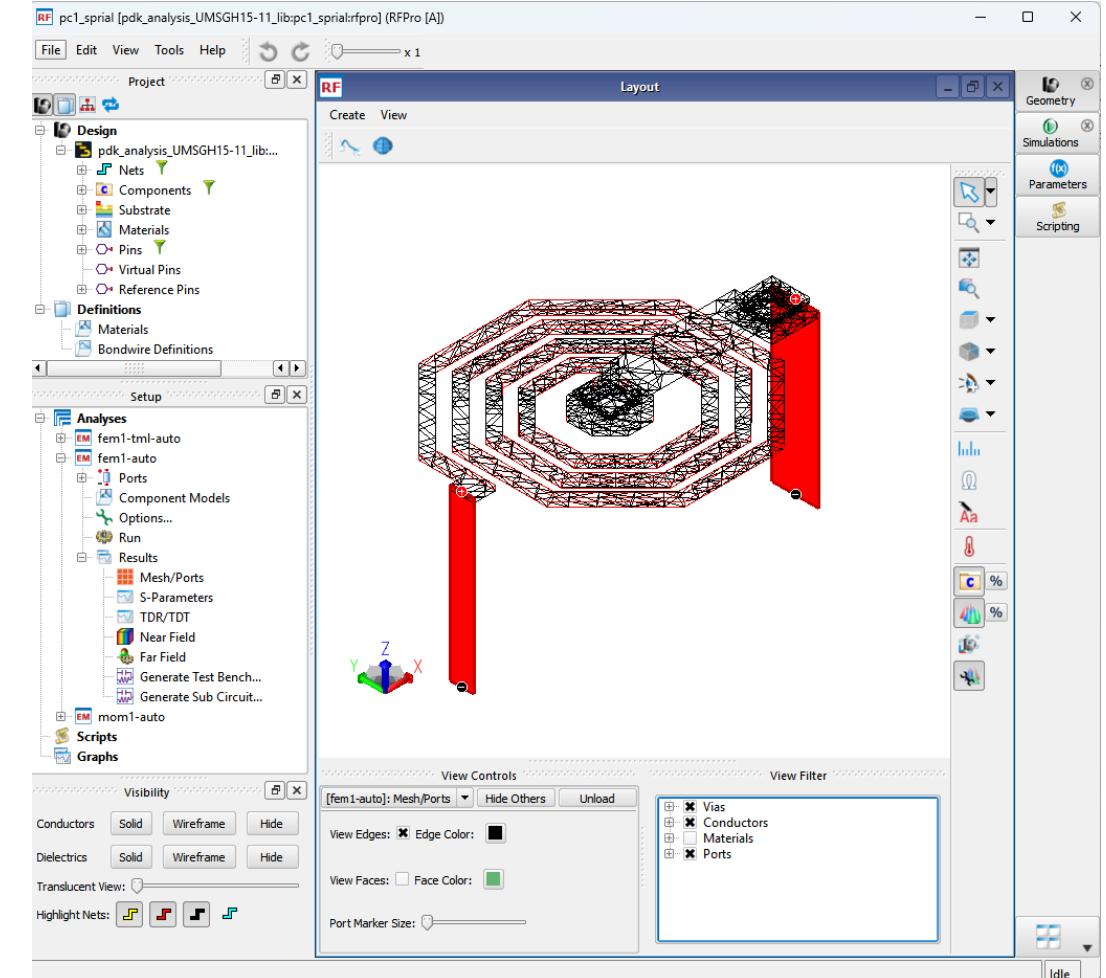
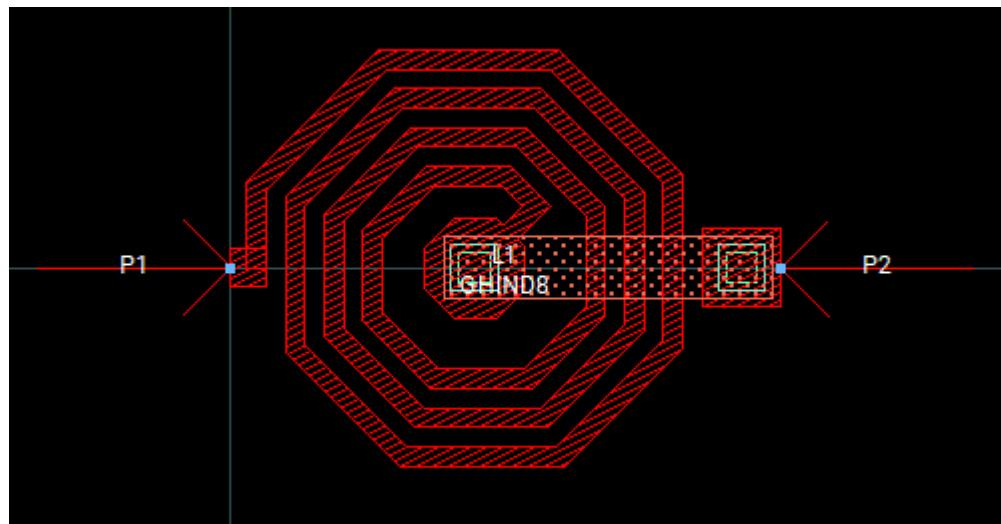
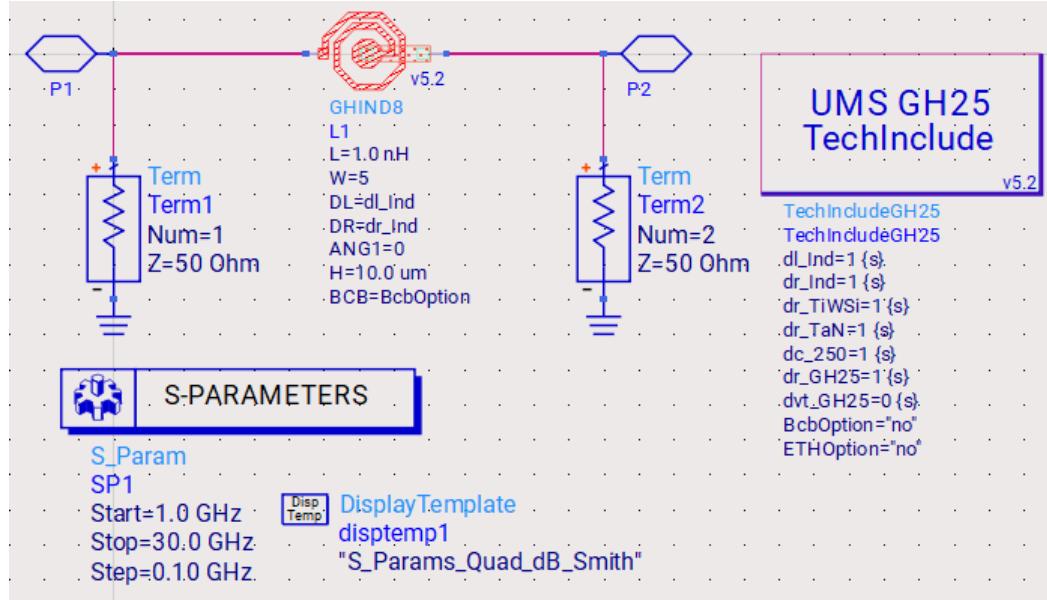
Lab 1, Steps 3a, b, c

Simulate Passive components

Simulate L, C, R, MLIN in Schematic and EM with RFPro

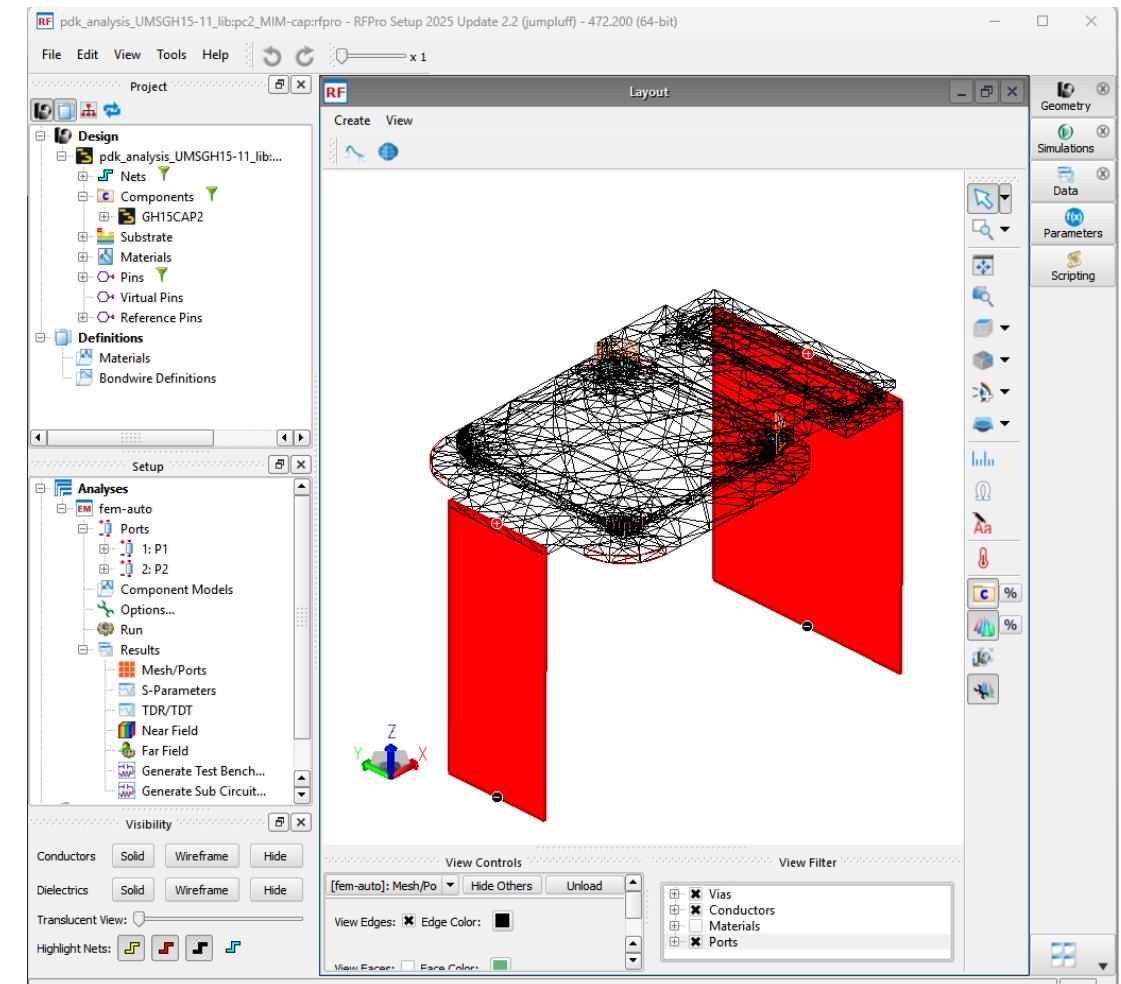
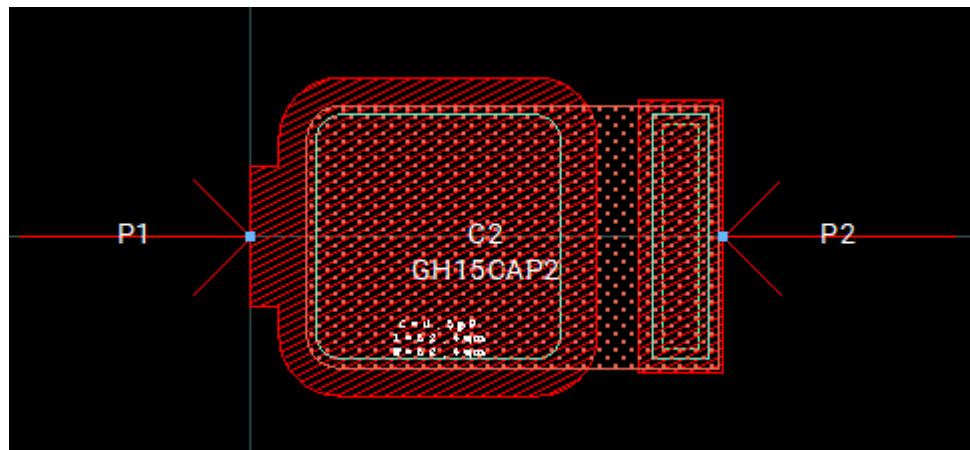
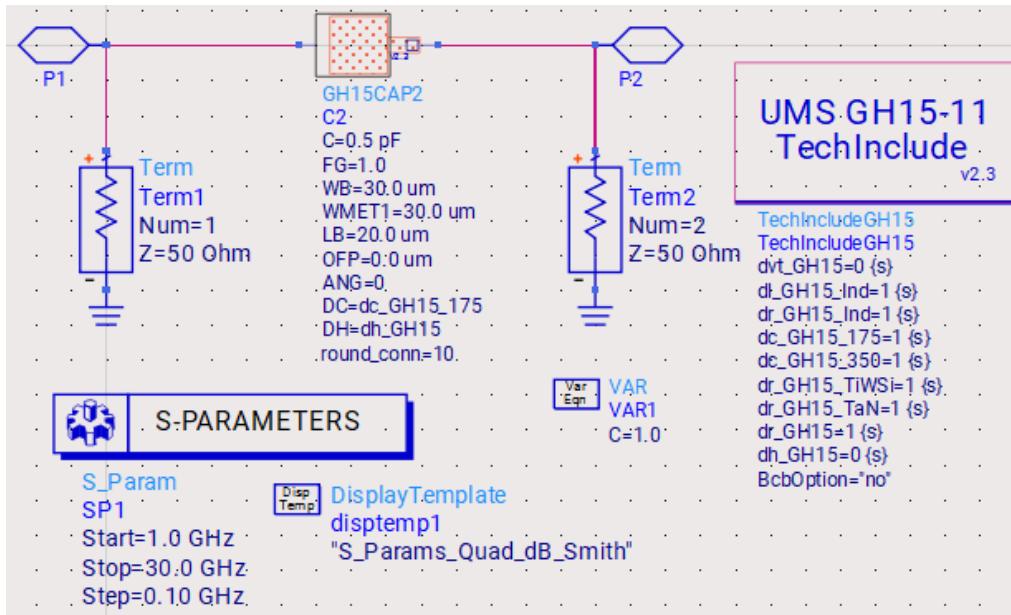
Spiral

Schematic and EM simulations



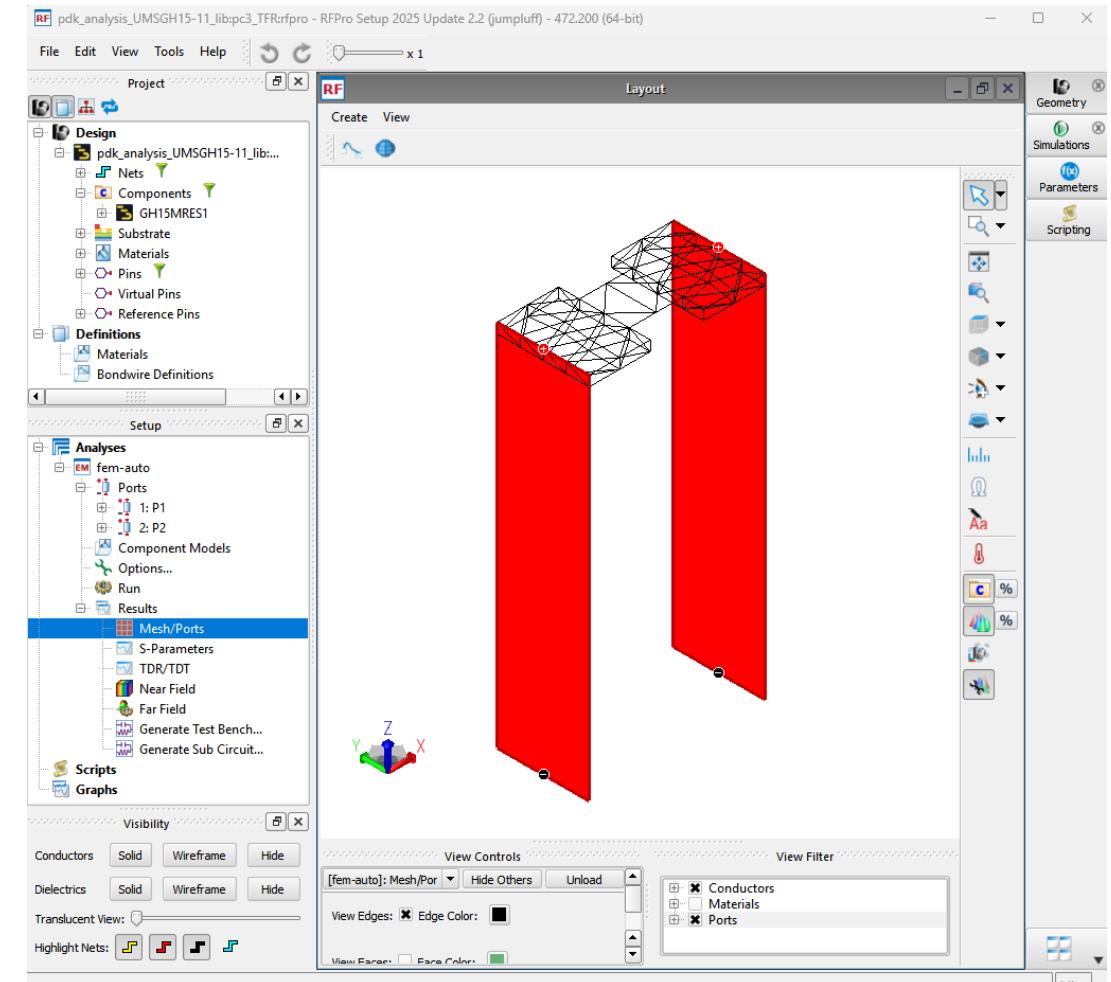
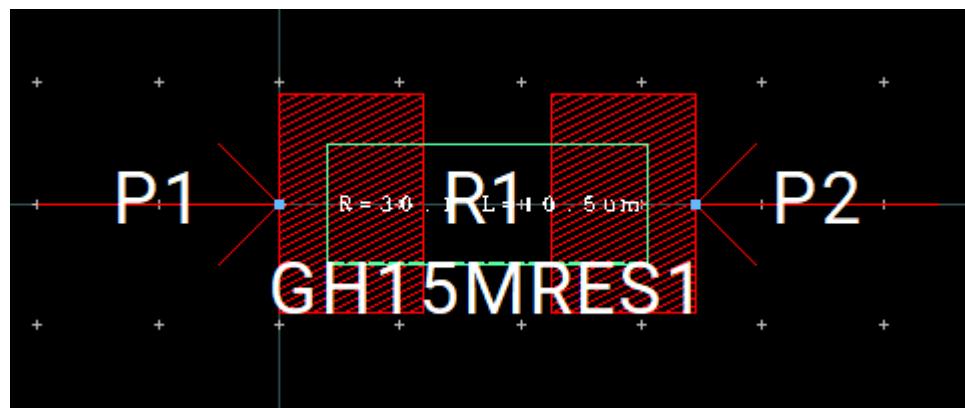
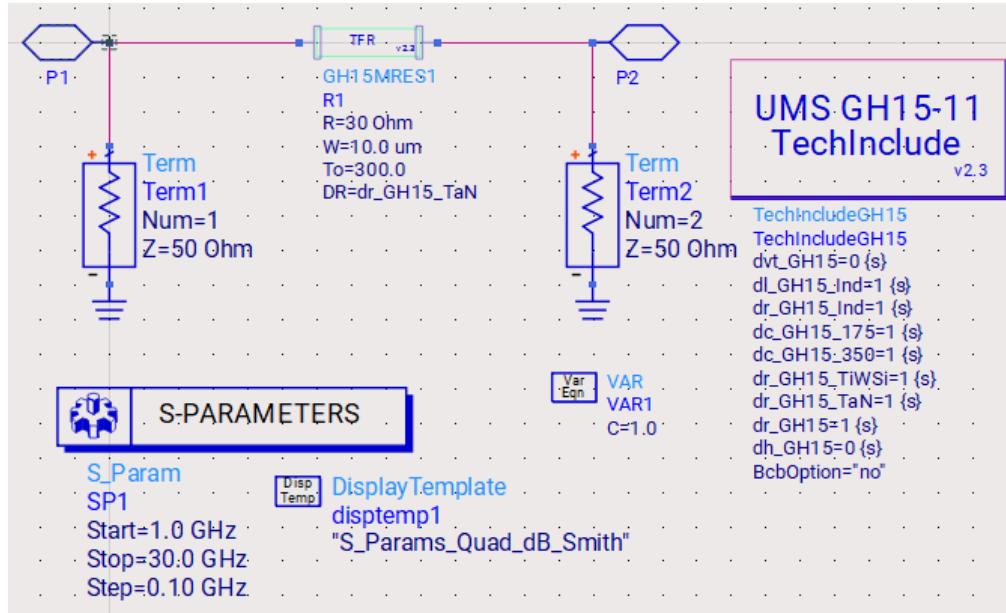
MIM Cap

Schematic and EM simulations



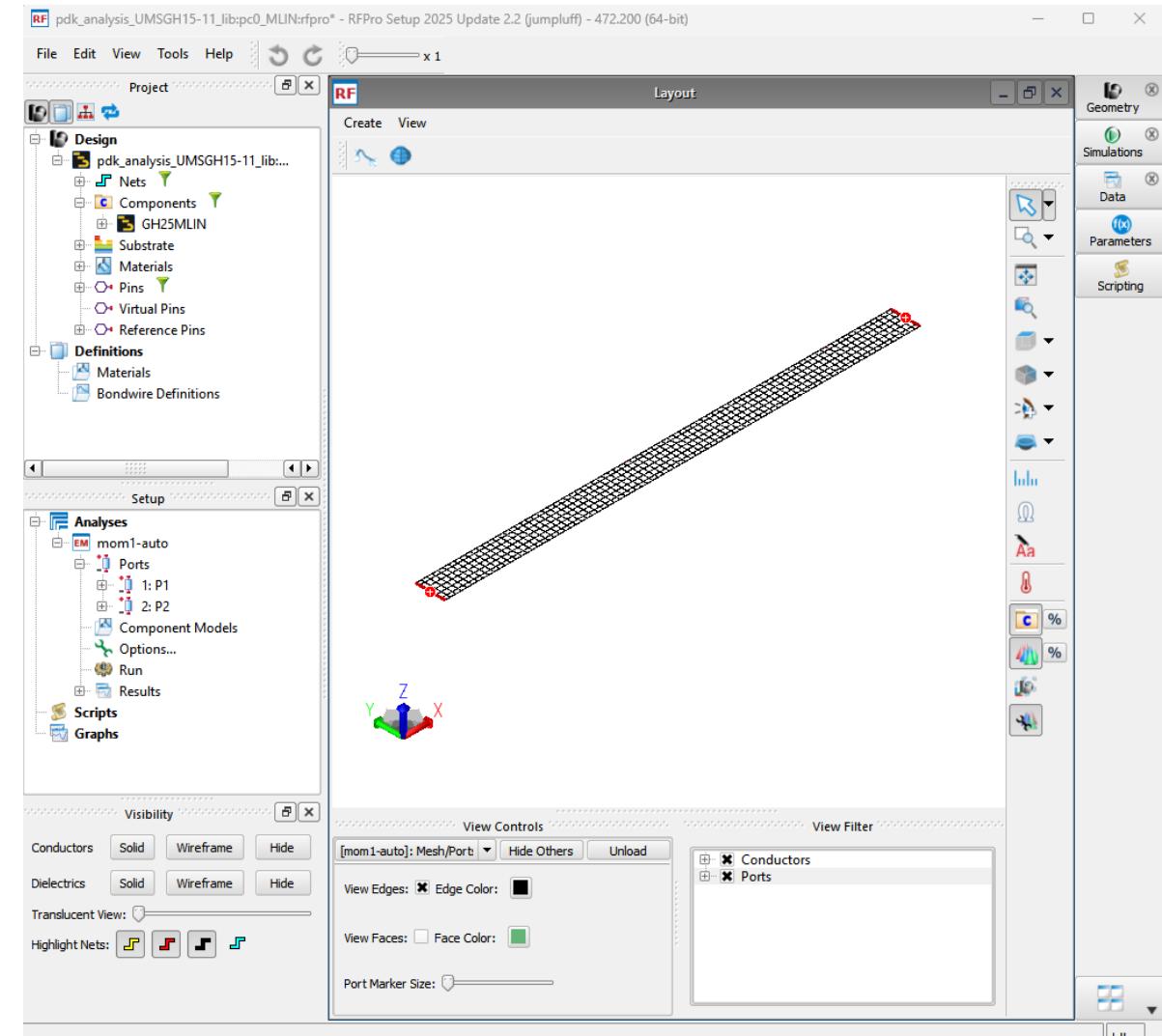
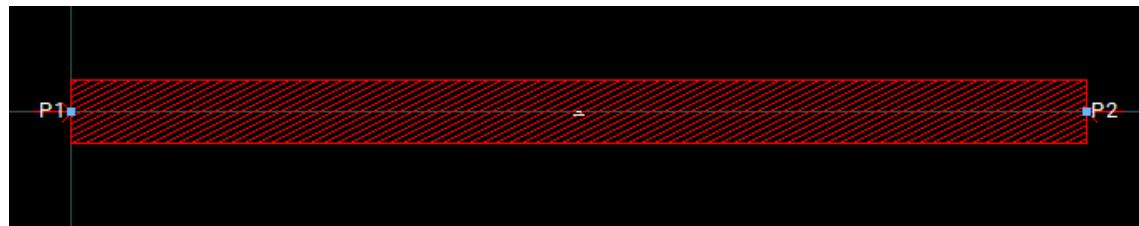
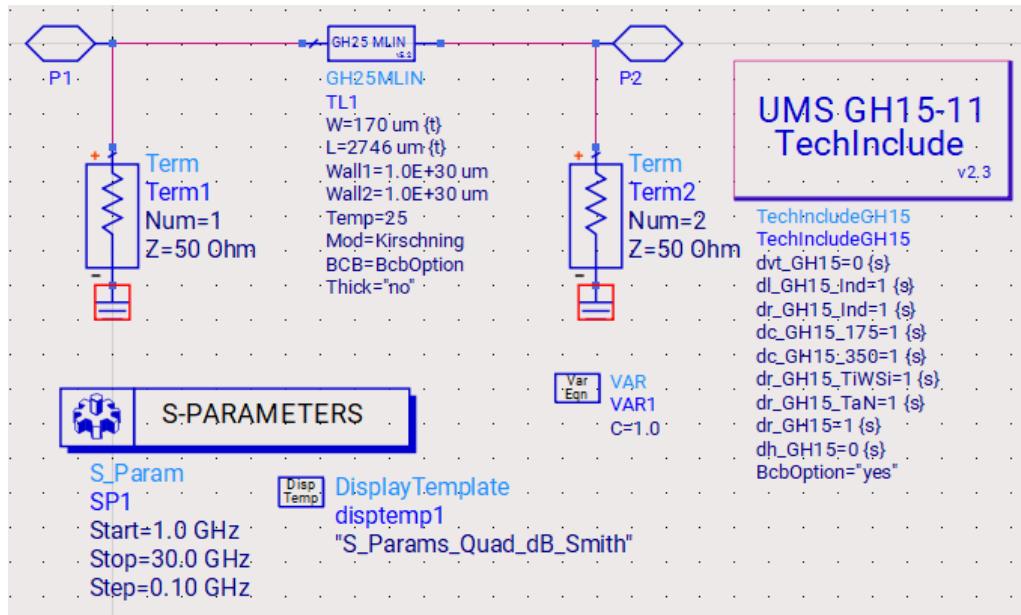
Thin Film Resistor

Schematic and EM simulations



Microstrip Transmission Line

Schematic and EM simulations



Line Calculator & Controlled Impedance Designer

Layout Substrate tool to calculate Line Impedances

