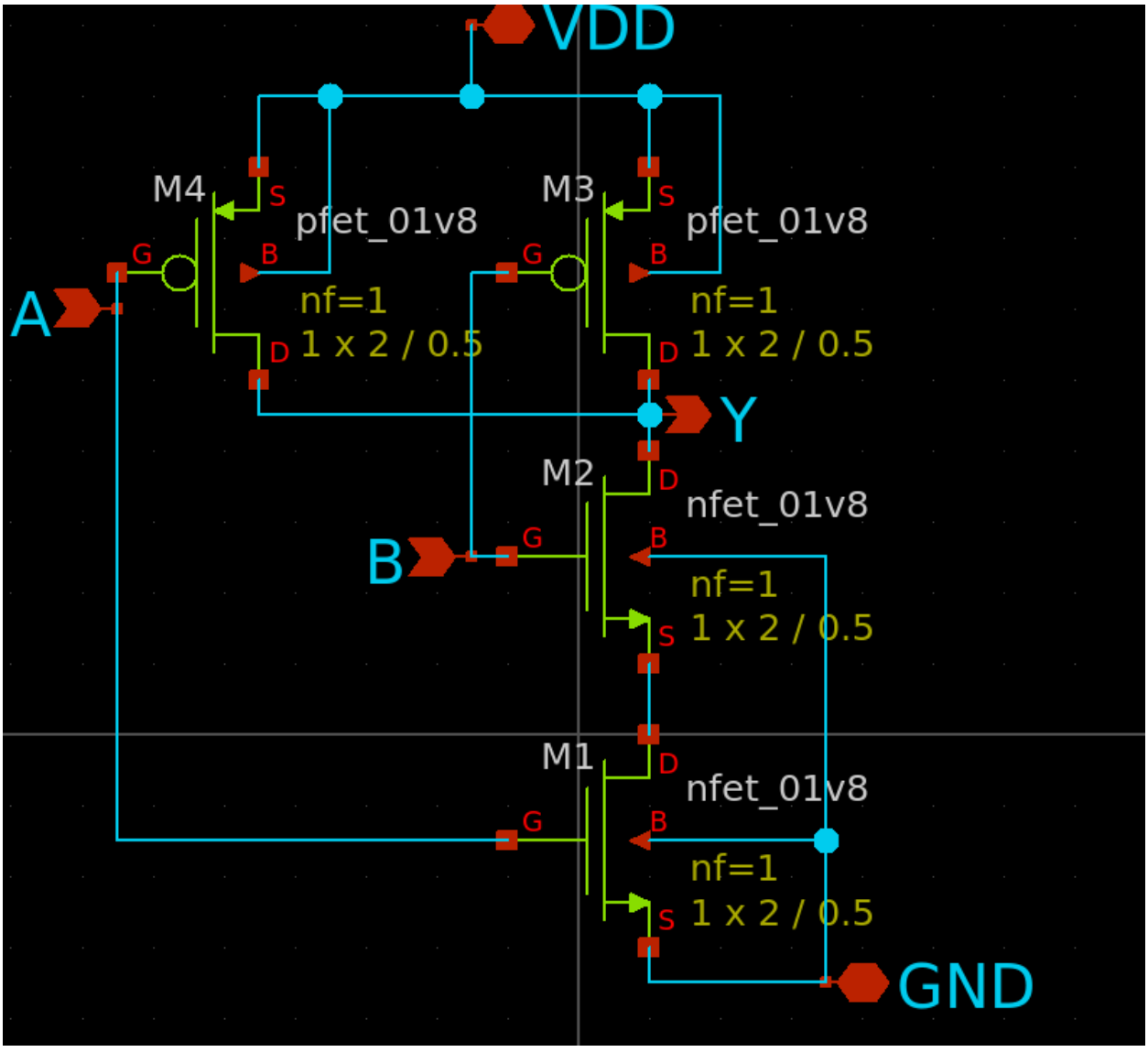
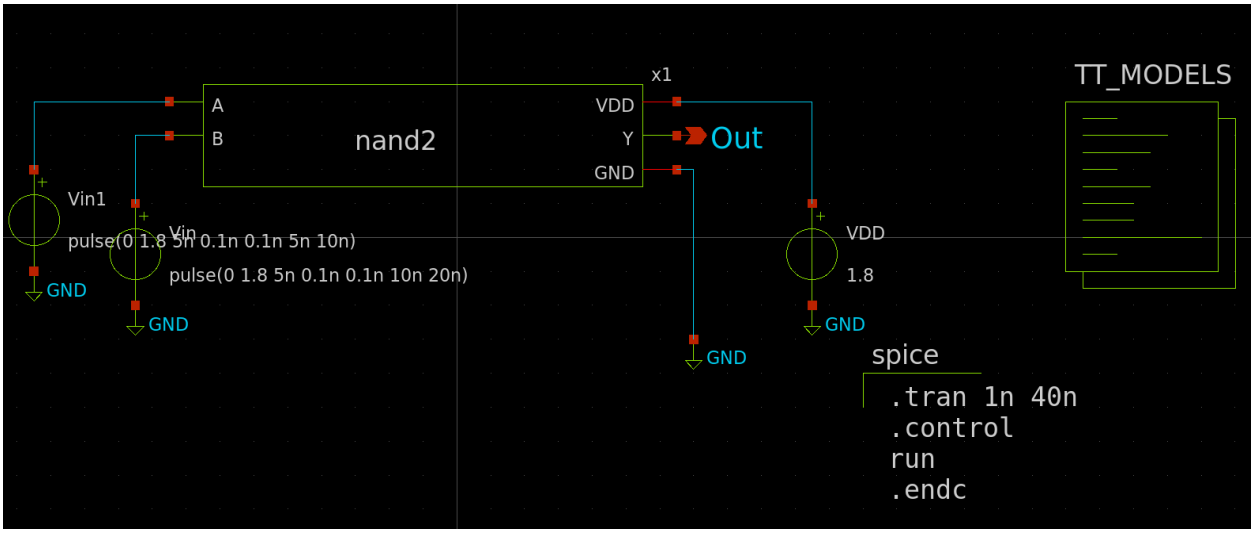
Designing the schematic and the layout of a2-input NAND gate using Skywater 130nm process

For this week's lab, we will design a 2-input NAND gate. First design the schematic, which will look like following. Then create a symbol.



Then verify the functionality using a testbench like following.



Then design the layout. Make sure that it is DRC clean. Finally, check LVS. The detailed tutorials are already posted for the inverter. We will also do a parasitic extraction and do post-layout simulation. I will update this file for that on Wednesday.