CAL POLY
SAN LUIS OBISPO

EE 431: COMPUTER-AIDED DESIGN OF VLSI DEVICES

Introduction to VLSI System Design

Nishith N. Chakraborty

December, 2024

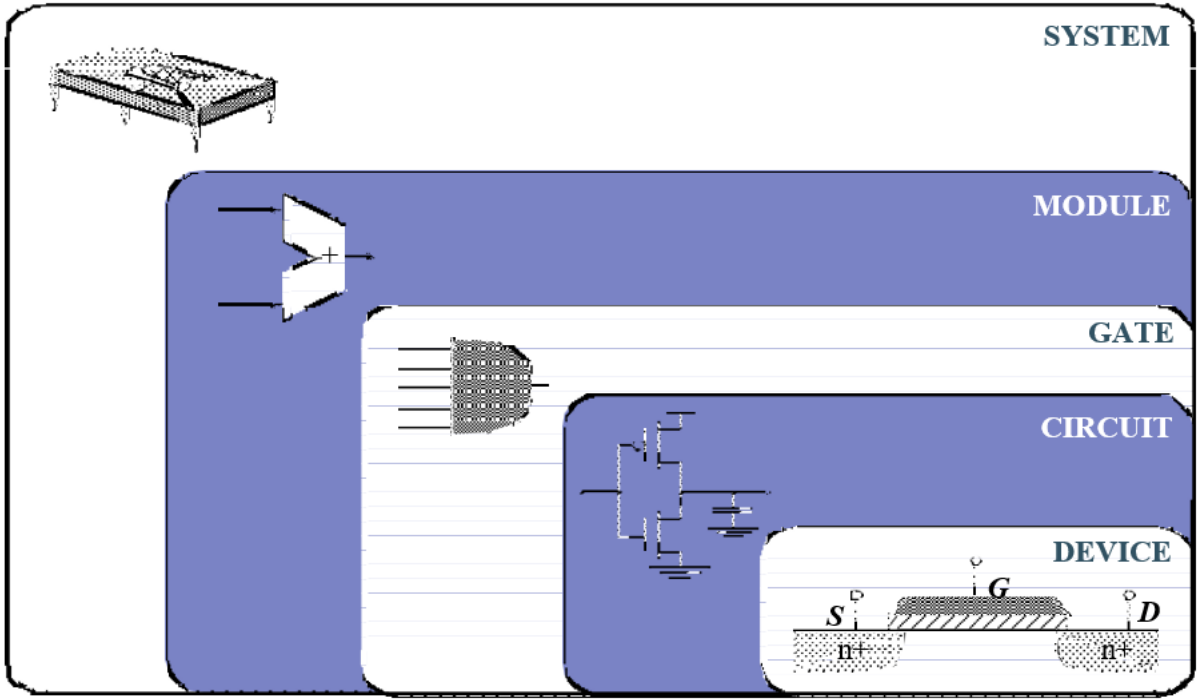
STRUCTURED DESIGN

- Hierarchy
  - Recursively divide the system into modules
- Regularity
  - Reuse modules wherever possible
  - Ex: Standard cell library
- Modularity
  - Allows modules to be treated as black boxes

DESIGN PARTITIONING

- Architecture: User's perspective, what does it do?
  - Instruction set, registers
  - MIPS, x86, Alpha, PIC, ARM, …
- Microarchitecture
  - Single cycle, multi-cycle, pipelined ?
- Logic: how are functional blocks constructed
  - Ripple carry, carry lookahead, carry select adders
- Circuit: how are transistors used
  - Complementary CMOS, pass transistors, domino
- Physical: chip layout
  - Datapaths, memories, random logic

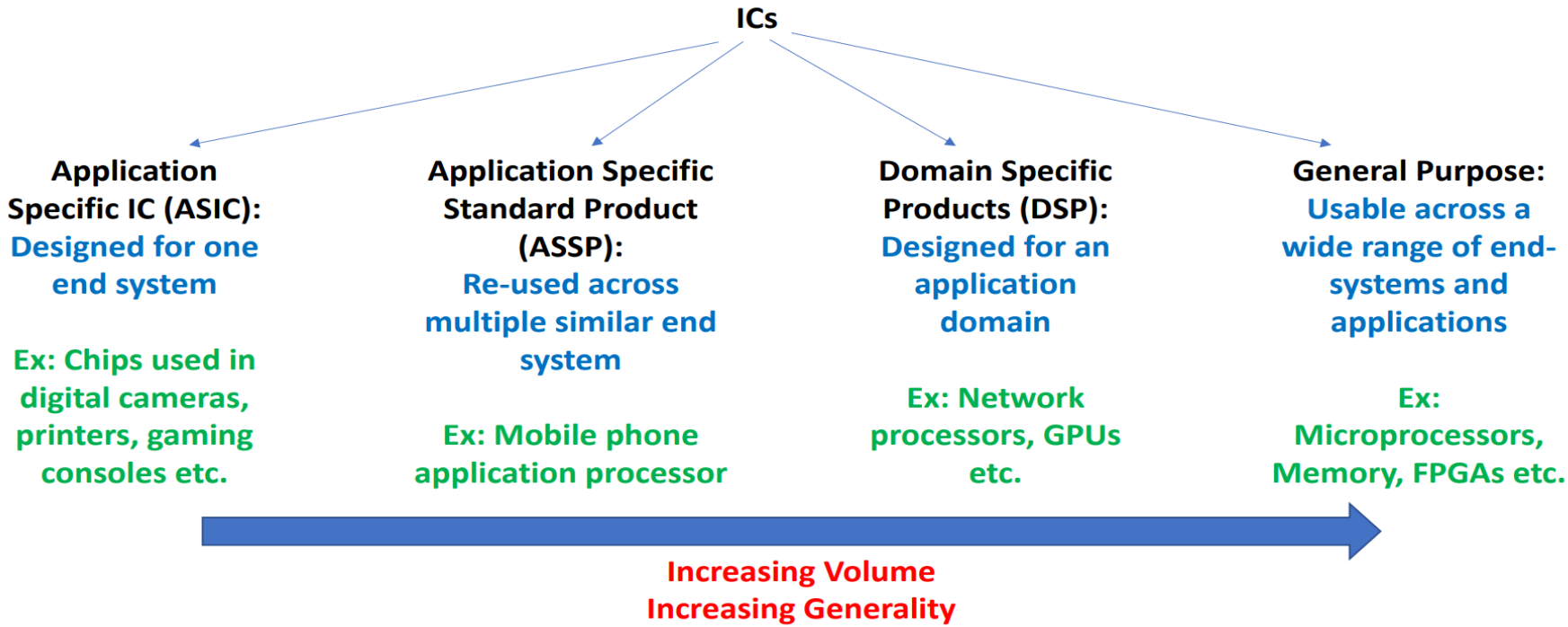
DESIGN ABSTRACTION LEVELS



VLSI DESIGN APPROACHES

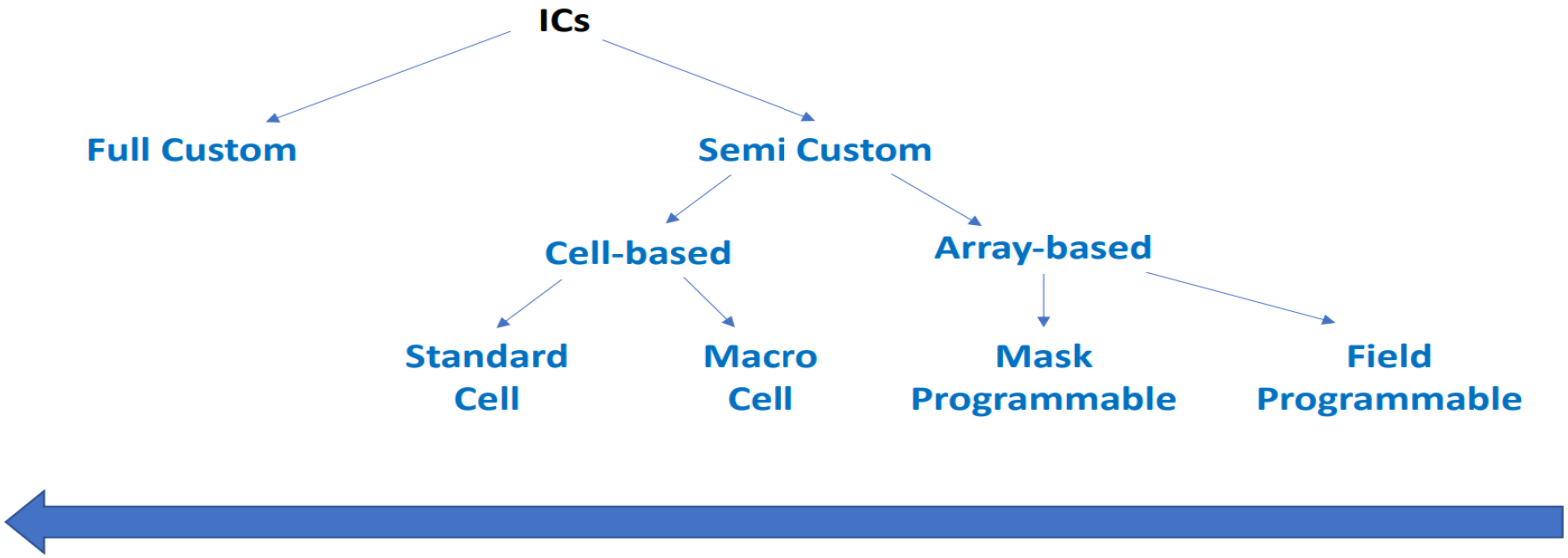
- **Custom:** A design that has been carefully crafted by the designer including manual layout.
- **Semi-custom:** Some custom crafted blocks including custom blocks using automation (i.e., SKILL) along with some fully automated blocks. Usually makes use of predefined, well optimized blocks that cannot be changed.
- **Automated:** The use of a hardware description language (VHDL, Verilog, SystemC, etc.) and CAD tools to synthesize a design from code to Silicon.

TAXONOMY OF INTEGRATED CIRCUITS (BY SCOPE OF USE)



Adapted from Prof. Anand Raghunathan, Purdue University

TAXONOMY OF INTEGRATED CIRCUITS (BY DEGREE OF CUSTOMIZATION)



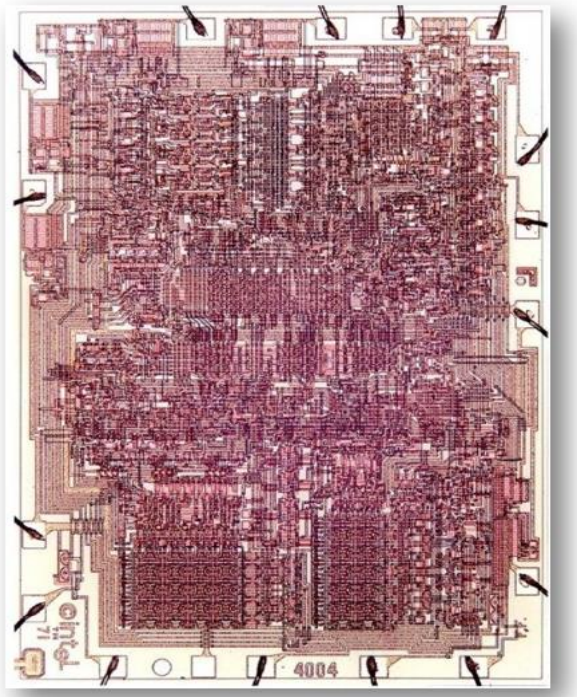
- Increasing design complexity and design cost
- More scope for optimization

Adapted from Prof. Anand Raghunathan, Purdue University

FULL CUSTOM DESIGN

- Very high level of customization – down to layout
- High design effort
- Maximum efficiency

Intel 4004



SEMI-CUSTOM: CELL BASED DESIGN

- A cell library (gates/latches/flip-flops) is pre-designed and pre-characterized
- Library contains different views of each cell (logic/transistor/physical)
- Circuits constructed by instantiating, connecting cells from library
- Design rules ensure that such circuits will work

COMBINATIONAL CELLS

Cell Name	*#In*	*Boolean Function*	*Drive Strengths*
BUF	1	$O = A$	X1, X2, X4, X8, X12 and X16
INV	1	$O = !A$	X1, X2, X4, X8, X12 and X16
AND2	2	$O = A * B$	X1 and X2
AND3	3	$O = A * B * C$	X1 and X2
AND4	4	$O = A * B * C * D$	X1 and X2
OR2	2	$O = A + B$	X1 and X2
OR3	3	$O = A + B + C$	X1 and X2
OR4	4	$O = A + B + C + D$	X1 and X2
NAND2	2	$O = !(A * B)$	X1 and X2
NAND3	3	$O = !(A * B * C)$	X1 and X2
NAND4	4	$O = !(A * B * C * D)$	X1 and X2
NOR2	2	$O = !(A + B)$	X1 and X2
NOR3	3	$O = !(A + B + C)$	X1 and X2
NOR4	4	$O = !(A + B + C + D)$	X1 and X2
MUX2	3	$O = A * !Sel + B * Sel$	X1
XOR2	2	$O = A \oplus B$	X1
XNOR2	2	$O = !(A \oplus B)$	X1
AOI21	3	$O = !((A * B) + C)$	X1 and X2
AOI22	4	$O = !((A * B) + (C + D))$	X1 and X2
OAI21	3	$O = !((A + B) * C)$	X1 and X2
OAI22	4	$O = !((A + B) * (C + D))$	X1 and X2
FA	3	$S = A \oplus B \oplus Cin$, $Cout = A \oplus B * Cin + A * B$	X1
HA	2	$S = A \oplus B$, $Cout = A * B$	X1

SEQUENTIAL CELLS

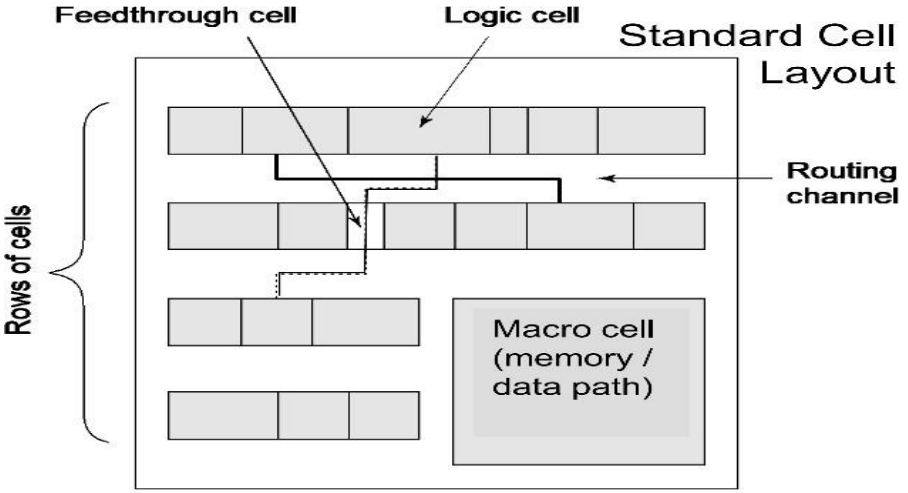
Cell Name	*#In*	*Description*	*Drive Strengths*
DFFRNQ	3	D flip-flop with asynchronous $!reset$	X1
DFFSNQ	3	D flip-flop with asynchronous $!set$	X1
SDFFRNQ	5	D flip-flop with scan and asynchronous $!reset$	X1
SDFFSNQ	5	D flip-flop with scan and asynchronous $!set$	X1
LHQ	2	High enable Latch	X1

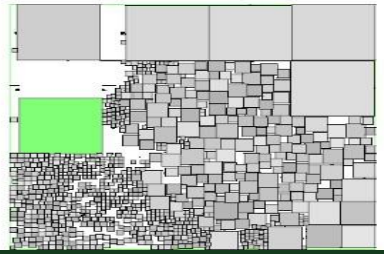
ADDITIONAL CELLS

Cell Name	*#In*	*Description*	*Drive Strengths*
CLKBUF	2	Clock buffer	X1, X2, X4, X8, X12 and X16
TBUF	2	Tri-state buffer	X1, X2, X4, X8, X12 and X16
FILL	-	Filler cell	X1, X2, X4, X8 and X16
CLKGATETST	3	Clock gate with test pin	X1
ANTENNA	-	Antenna cell	-
FILLTIE	-	Cell to tie the wells	-
TIEH	-	Tie-high cell	-
TIEL	-	Tie-low cell	-

SEMI-CUSTOM: CELL BASED DESIGN (CONTINUED)

- Standard cells must have the same height
  - Eases physical design
  - Layout organized into rows of cells with routing channels in between them
- Macro cells do not have this restriction.
- It is common to mix both macro cells (e.g. memories and Datapath components) with standard cells (random logic).

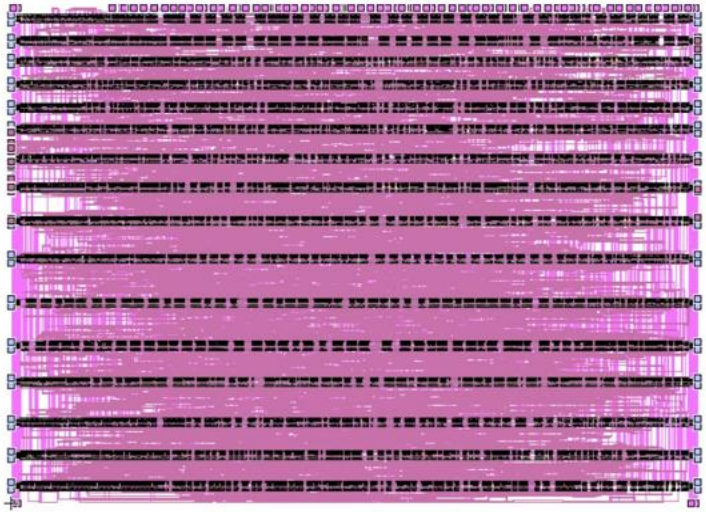




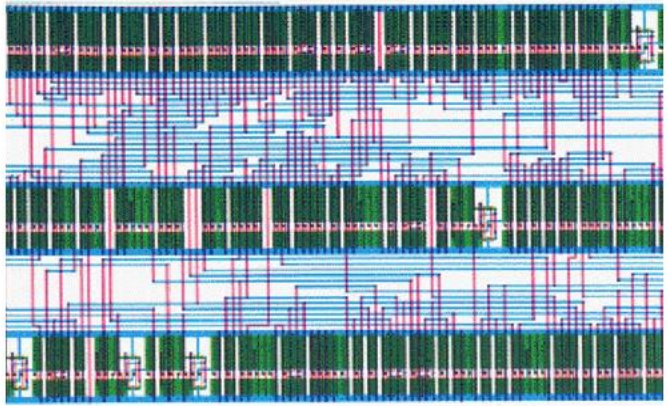
Macro Cell Layout

STANDARD CELL BASED DESIGN (EXAMPLES)

32-bit ALU standard cell layout



Three rows of standard cells



Adapted from Prof. Anand Raghunathan, Purdue University

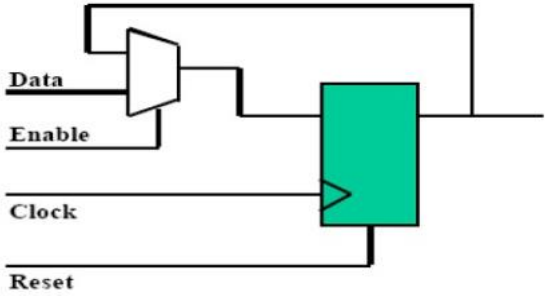
LOW POWER TECHNIQUES

- Dynamic Voltage Scaling (DVS)
- Frequency Scaling
- Clock Gating
- Sleep Mode Transistors/ Power Gating/ Header -Footer Transistors

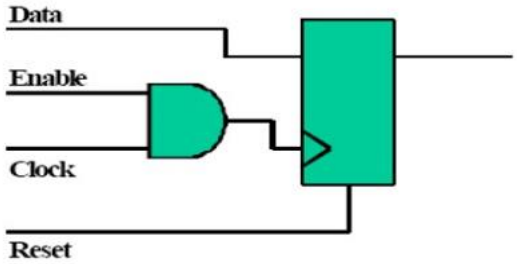
➢ All these are targeted to reducing dynamic power. As technology scales, static power is becoming more of a concern

CLOCK GATING

- Dynamic power control through synthesis typically due to clock gating
- Usually this means shutting off the clock to flip-flop
- Example to the right:
  - Conceptually the same
  - Implementation 1 clocks the ff every cycle
  - Implementation 2 only clocks the ff when enabled
    - Hence the lower power design



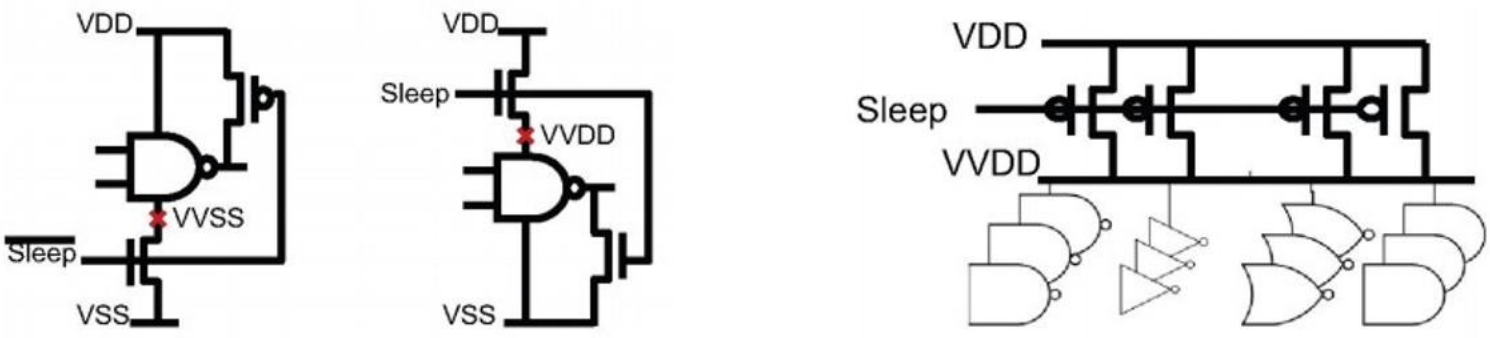
Implementation 1



Implementation 2

POWER GATING/ SLEEP MODE

- Use transistors to cut-off connection with VDD and/or GND, to reduce power consumption.
- Selectively turns off unused blocks/segments of the system



K. Shi and D. Howard, "Sleep Transistor Design and Implementation - Simple Concepts Yet Challenges To Be Optimum," 2006 International Symposium on VLSI Design, Automation and Test, Hsinchu, 2006, pp. 1-4.

THERMAL-AWARE DESIGN

- Temperature is more of a concern as technology continues to scale well below 100 nm
- As temperature is related to power density, low-power techniques can be used to reduce temperature
  - DVS → Dynamic Voltage Scaling
  - Frequency Scaling
  - Use of sleep mode
- A thermal-aware design responds to temperature by:
  - Actively monitoring “hot spots” with sensors
  - Monitoring the activity factor

Thank you!