CAL POLY
SAN LUIS OBISPO

EE 531: ADVANCED VLSI DESIGN

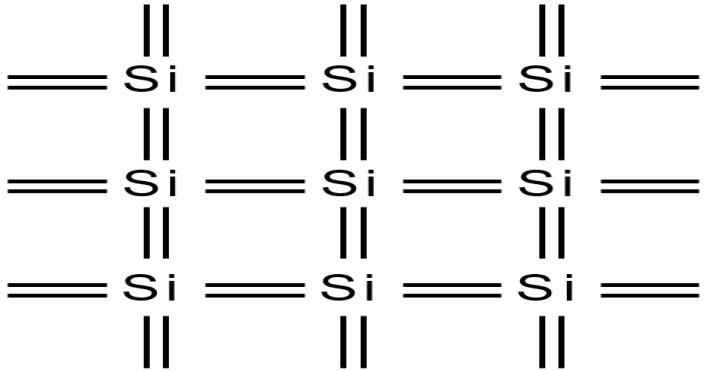
Crash Course: VLSI Devices & Circuits

Nishith N. Chakraborty

January, 2025

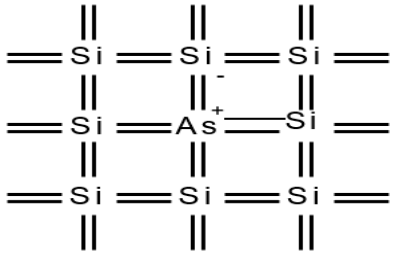
SILICON LATTICE

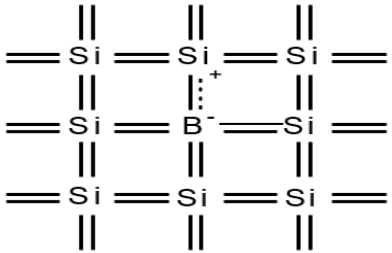
- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



DOPED SEMICONDUCTOR

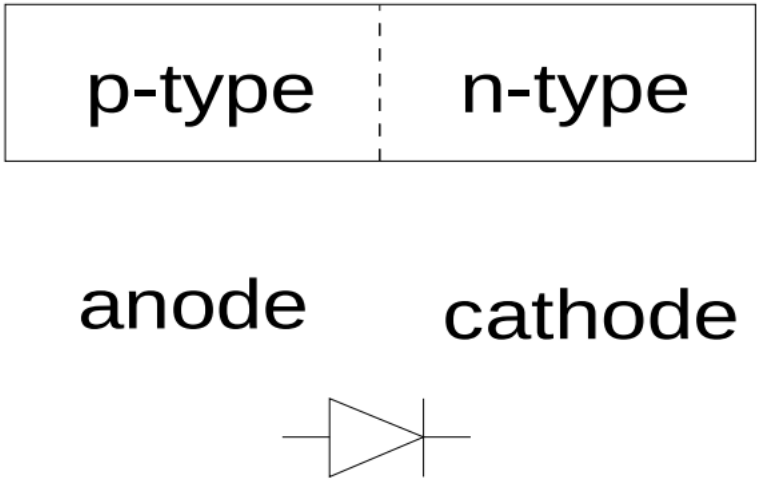
- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)





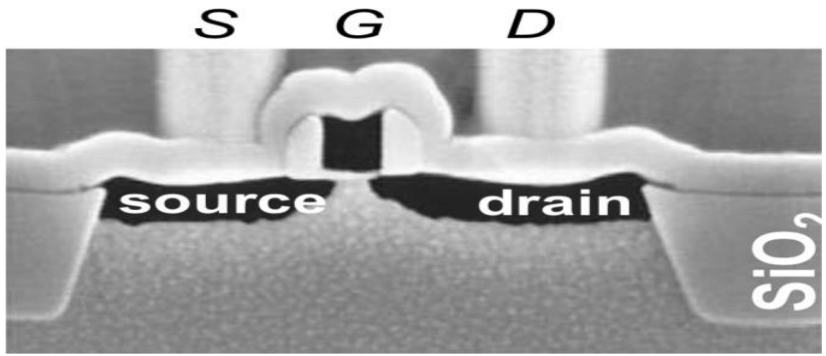
THE P-N JUNCTION

- Junction between p-type & n-type semiconductor forms diode.
- Current flows only in one direction

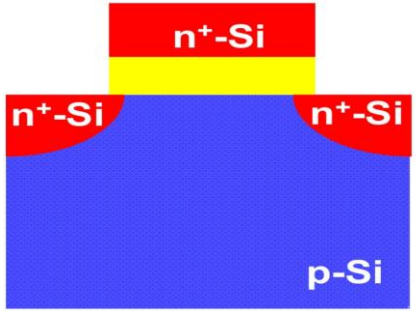


MOSFETS DEVICE STRUCTURE

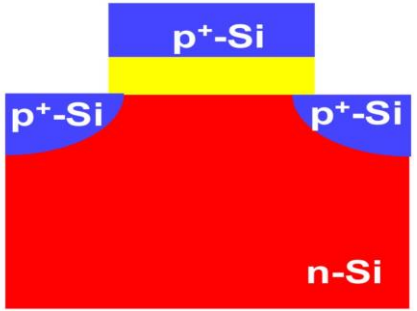
- The MOSFET is the most important device for digital integrated circuits today.
- It is a unipolar device, that is, electrical current is carried predominantly by the drift of one type of carrier: electrons in the n-MOS transistor and holes in the p-MOS device.
- It is a field effect, or voltage-controlled, device, which makes the standby power consumption low.
- The ease with which the MOSFET geometry can be scaled down in size, make it very attractive for VLSI.



NMOS/ NFET/ n-MOS



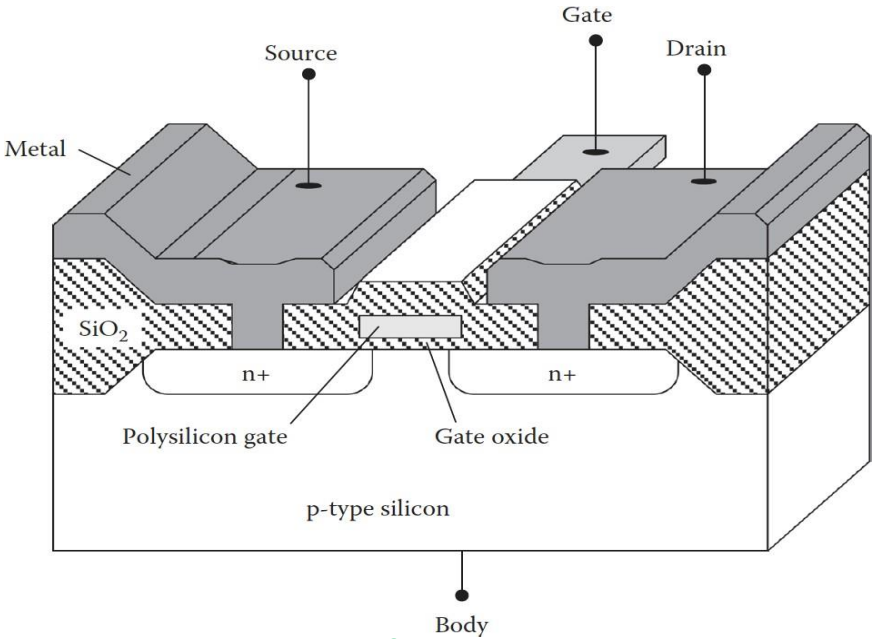
PMOS/ PFET/ p-MOS



MOSFETS DEVICE STRUCTURE

Enhancement-Type MOSFET: No conducting channel between the drain and source unless a positive voltage is applied between the gate and source (so it is a normally-off)

- **The name enhancement type reflects the fact that a gate bias is required to enhance a conducting channel**
- **Some MOS transistors are designed to conduct with zero gate-source bias, and these are referred to as depletion type devices.**
- **However, enhancement type devices are preferred in digital circuits for low standby power.**



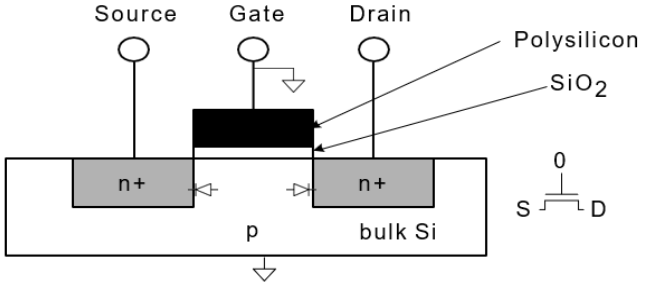
Enhancement Type NMOS

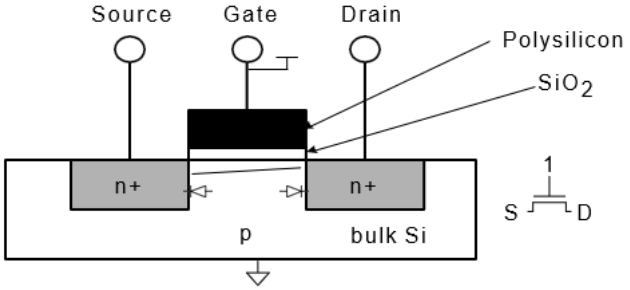
Source: Digital Integrated Circuits : Analysis and Design, Second Edition, by John E. Ayers

NMOS OPERATION

- When gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF

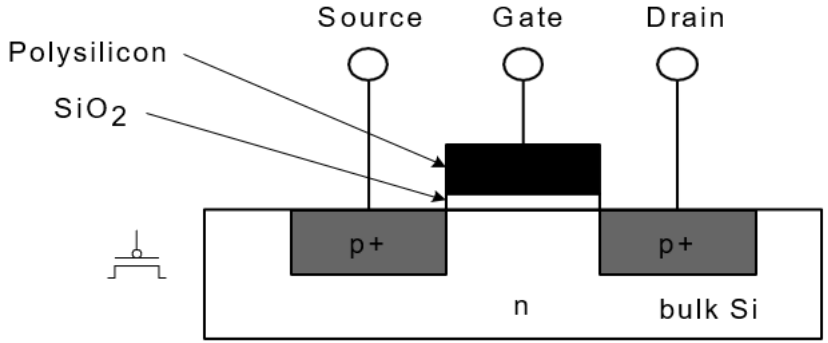
- When gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON





PMOS OPERATION

- Body tied to high voltage (VDD)
- Gate low: transistor ON
- Gate high: transistor OFF
- Bubble indicates inverted behavior

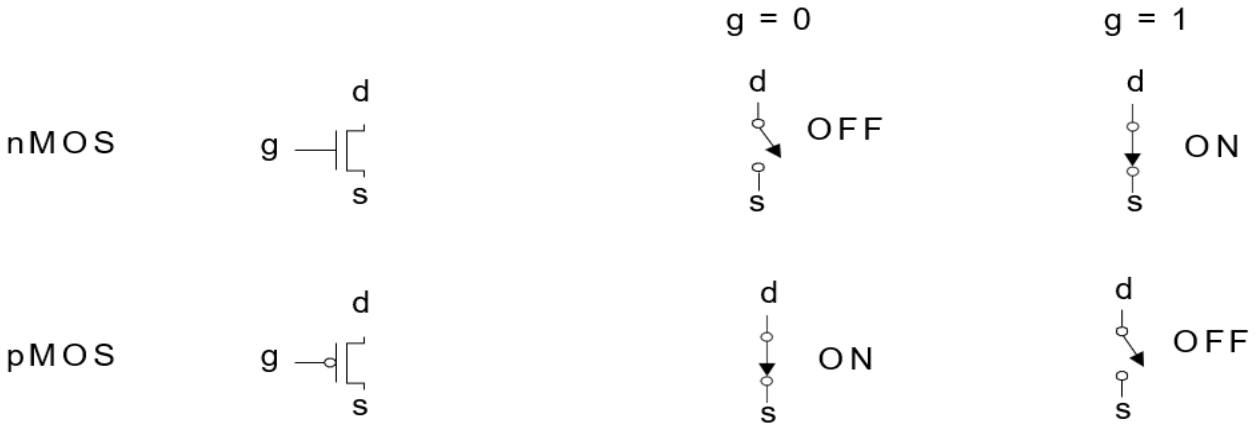


POWER SUPPLY VOLTAGE

- Ground (GND) = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny (sub 100 nm) transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

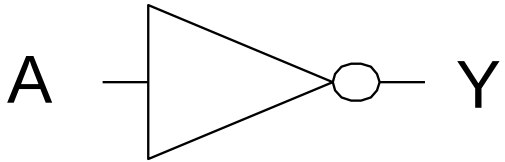
TRANSISTORS AS SWITCHES

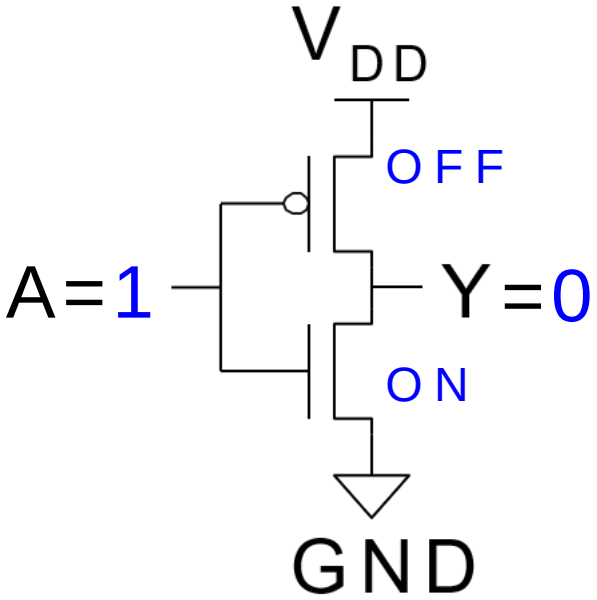
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS INVERTER (NOT GATE)

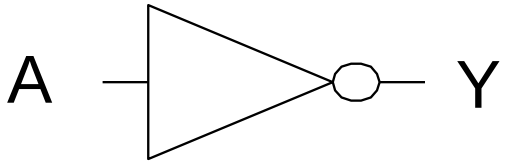
A	Y
0	
1	0

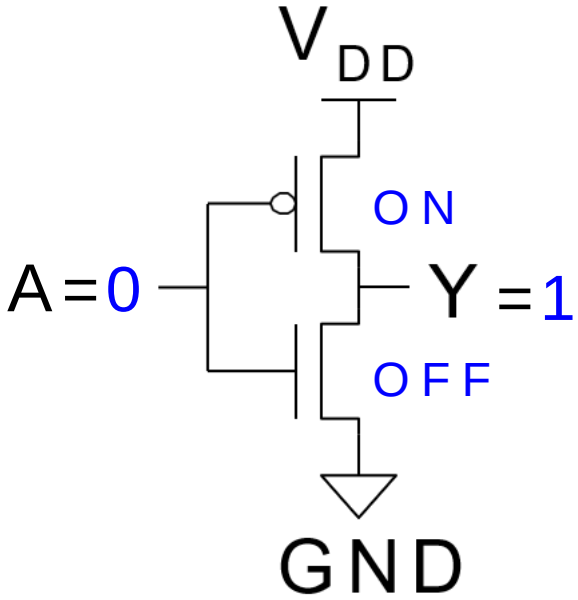




CMOS INVERTER (NOT GATE)

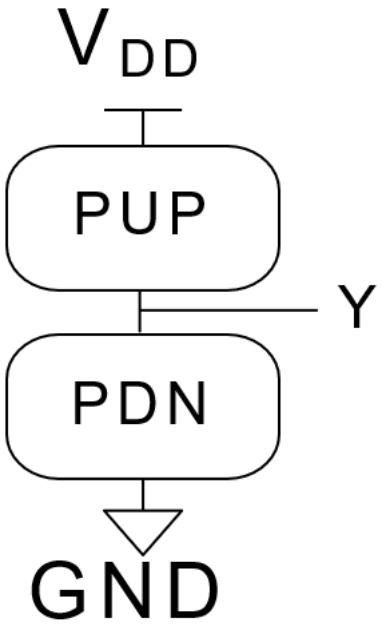
A	Y
0	1
1	0





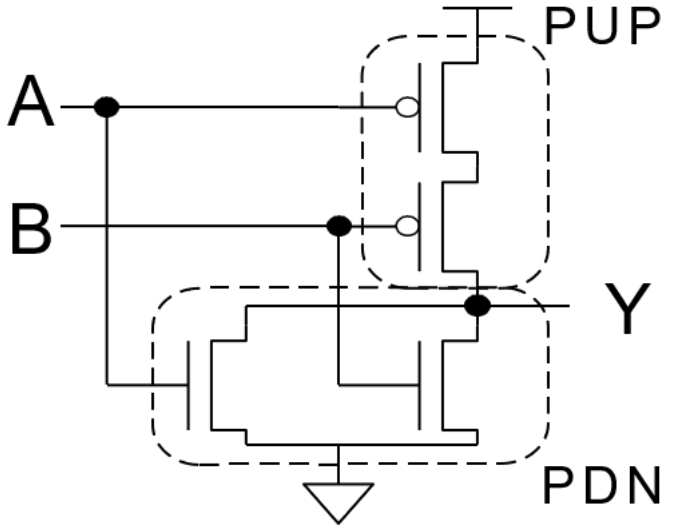
MORE COMPLEX CIRCUITS: PUP AND PDN

- Pull-up net (PUP) off when pull-down (PDN) on
- PUP implemented as complement of PDN (Complementary MOS)
- If two FETs in parallel in PDN, counterparts in series in PUP
- Output (Y) connected to VDD or GND, never both



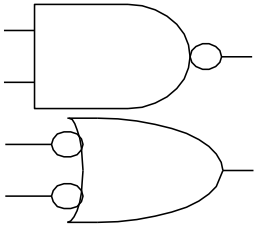
MORE COMPLEX CIRCUITS: PUP AND PDN

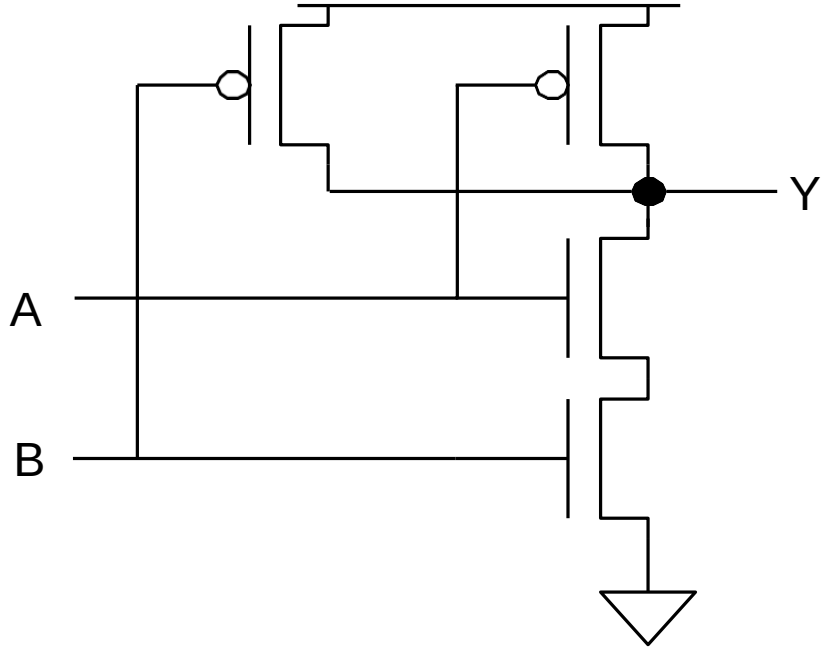
- Pull-up net (PUP) off when pull-down (PDN) on
- PUP implemented as complement of PDN (Complementary MOS)
- ***If two FETs in parallel in PDN, counterparts in series in PUP***
- Output (Y) connected to VDD or GND, never both



CMOS NAND GATE

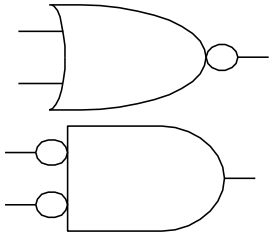
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

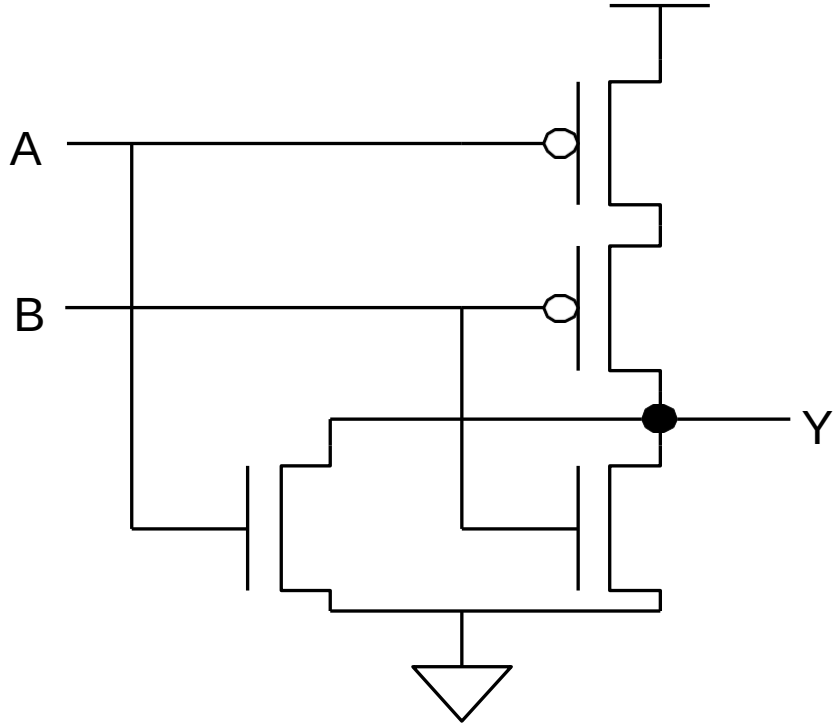




CMOS NOR GATE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



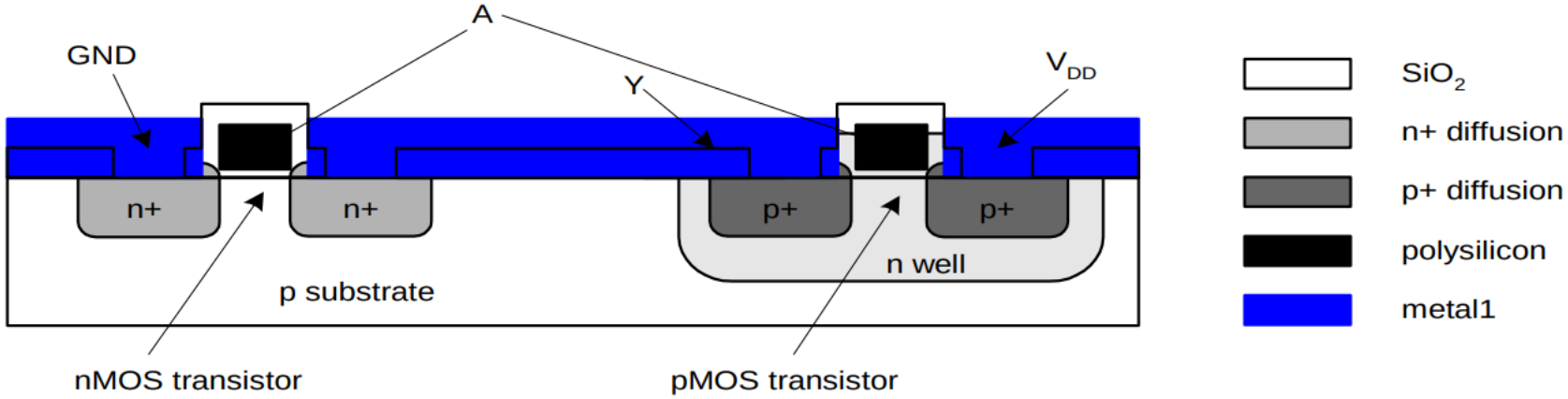


CMOS FABRICATION

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

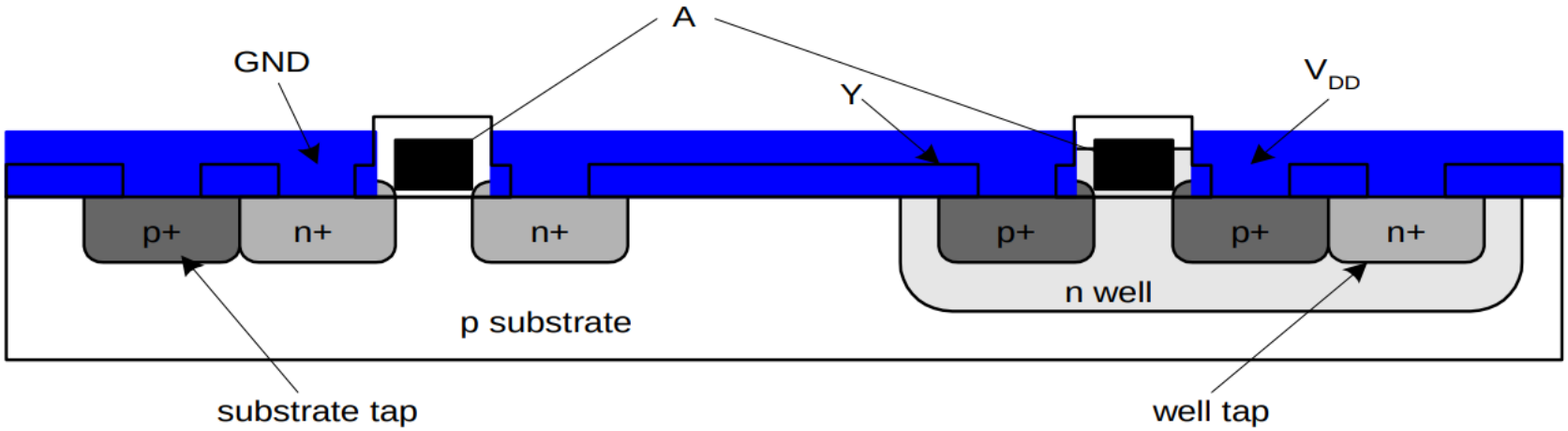
INVERTER CROSS-SECTION

- Typically use p-type substrate for NMOS transistors
- Requires n-well for body of PMOS transistors



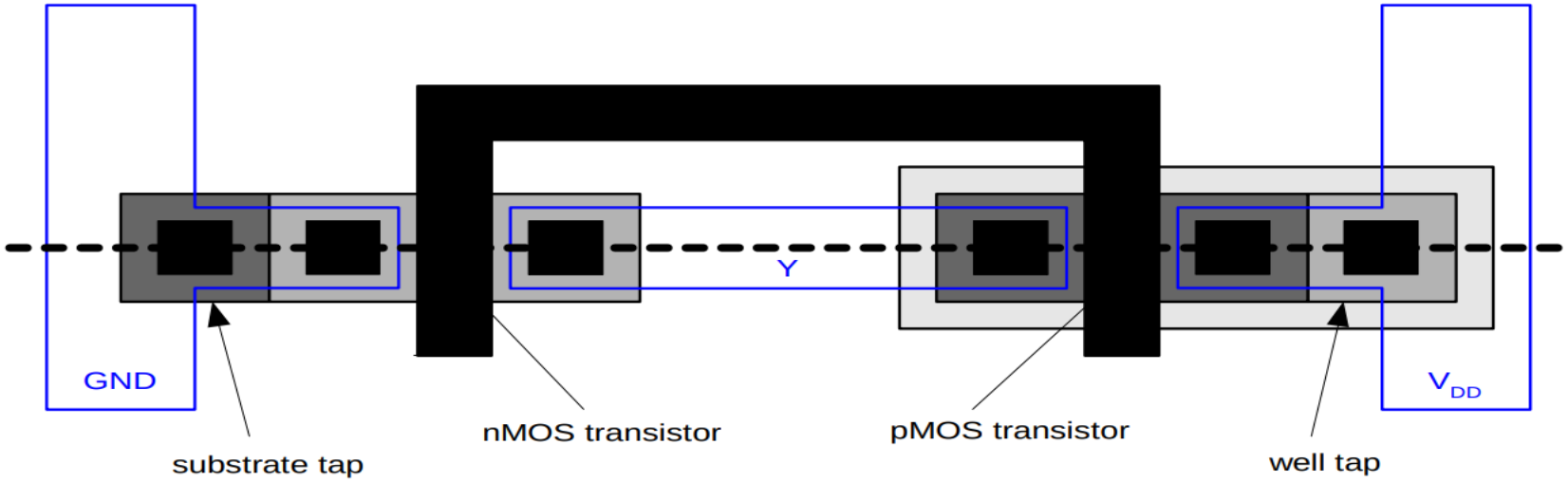
WELL AND SUBSTATE TAPS

- Substrate must be tied to GND and n-well to VDD
- Metal to lightly-doped semiconductor forms poor connection called Schottky Diode
- Use heavily doped well and substrate contacts / taps



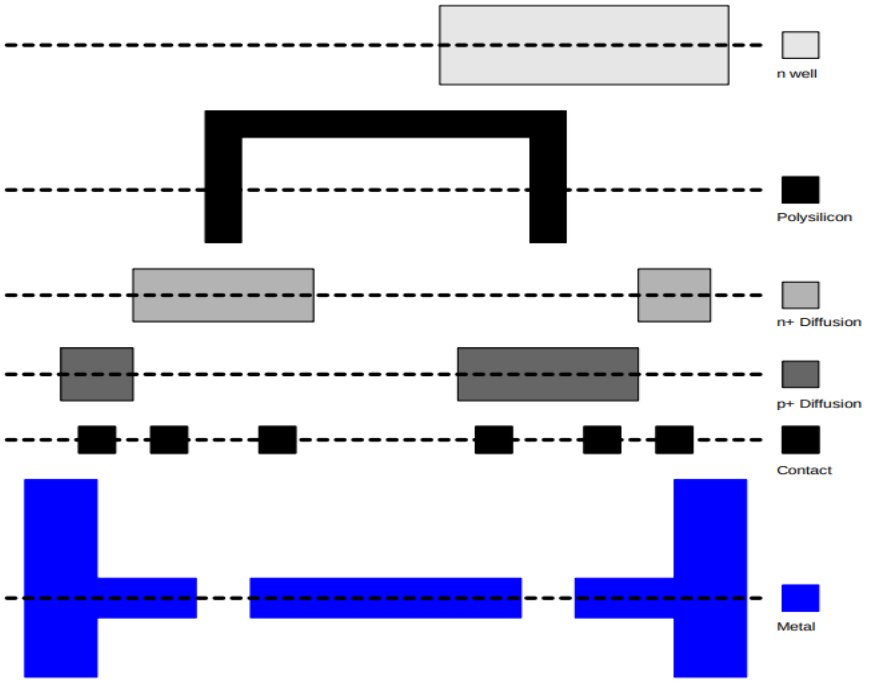
INVERTER MASK SETS

- Transistors and wires are defined by masks
- Cross-section taken along dashed line



DETAILED MASK VIEWS

- Six masks (old process)
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal

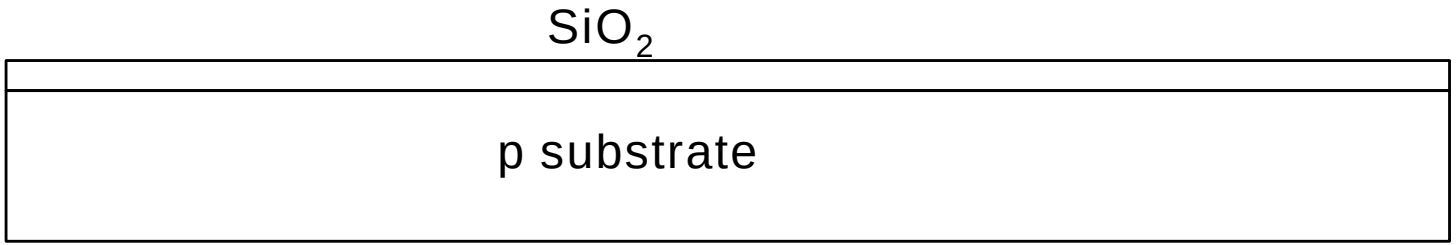


FABRICATION STEPS

- Start with blank wafer (cut from ingot of crystalline silicon)
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

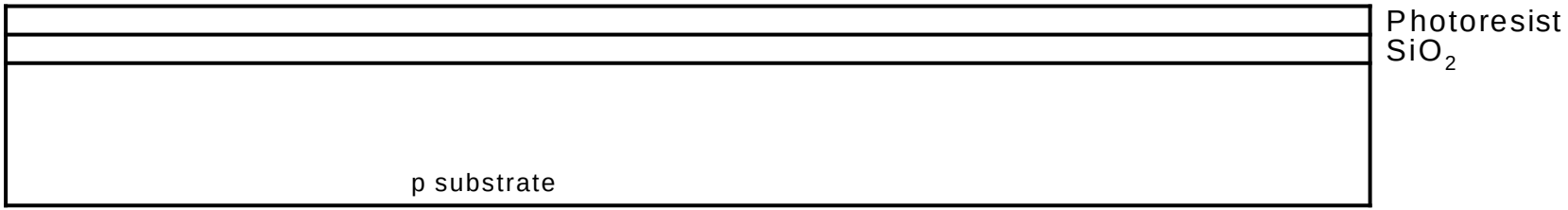
OXIDATION

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



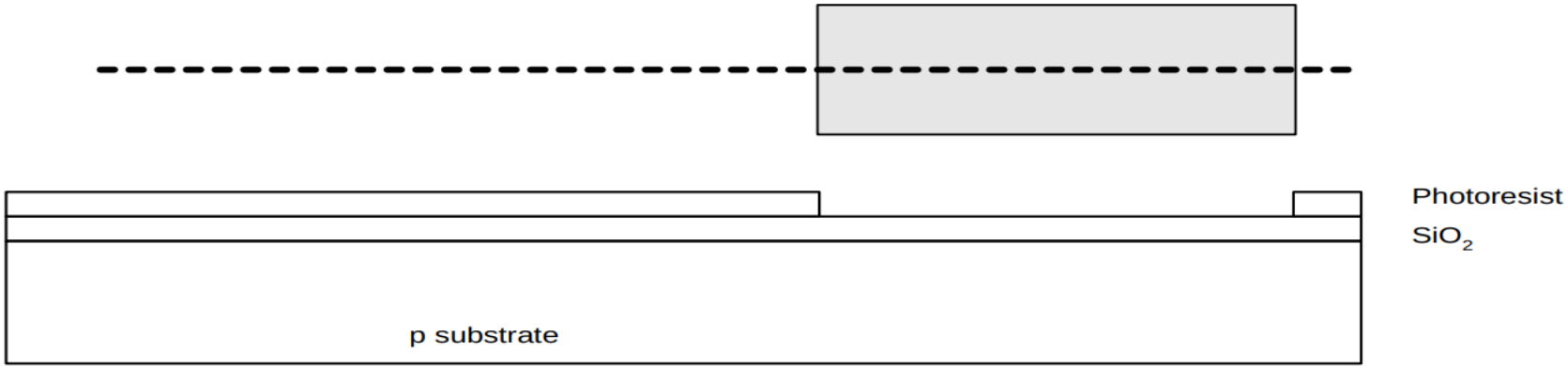
PHOTORESIST

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



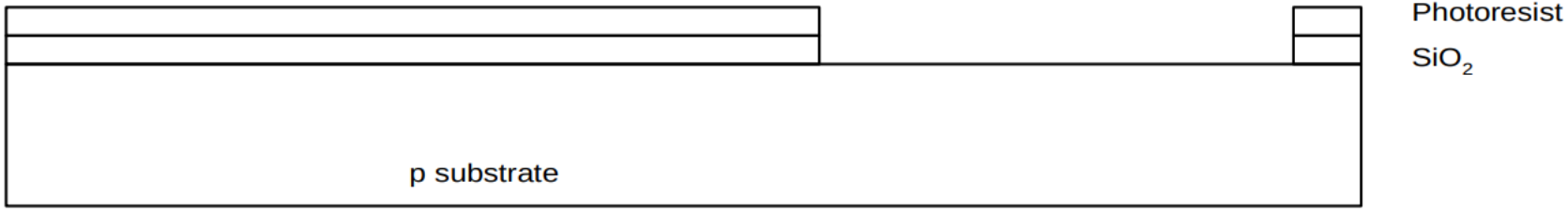
LITHOGRAPHY

- Expose photoresist through n-well mask
  - Older processes use visible light
  - For features below 14 nm, X-rays or EUV (extreme ultraviolet) used
- Strip off exposed photoresist



ETCH

- Etch oxide with something like hydrofluoric acid (HF)
  - ➢ Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed

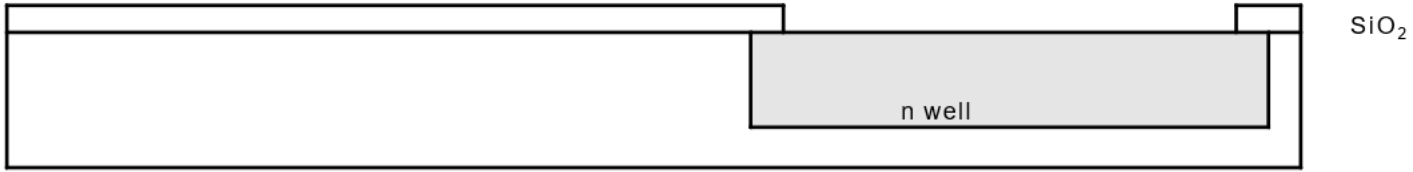


STRIP PHOTORESIST

- Strip off remaining photoresist
  - ➢ Use mixture of acids called piranha etch
- Necessary so resist doesn't melt in next step

N-WELL

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



STRIP OXIDE

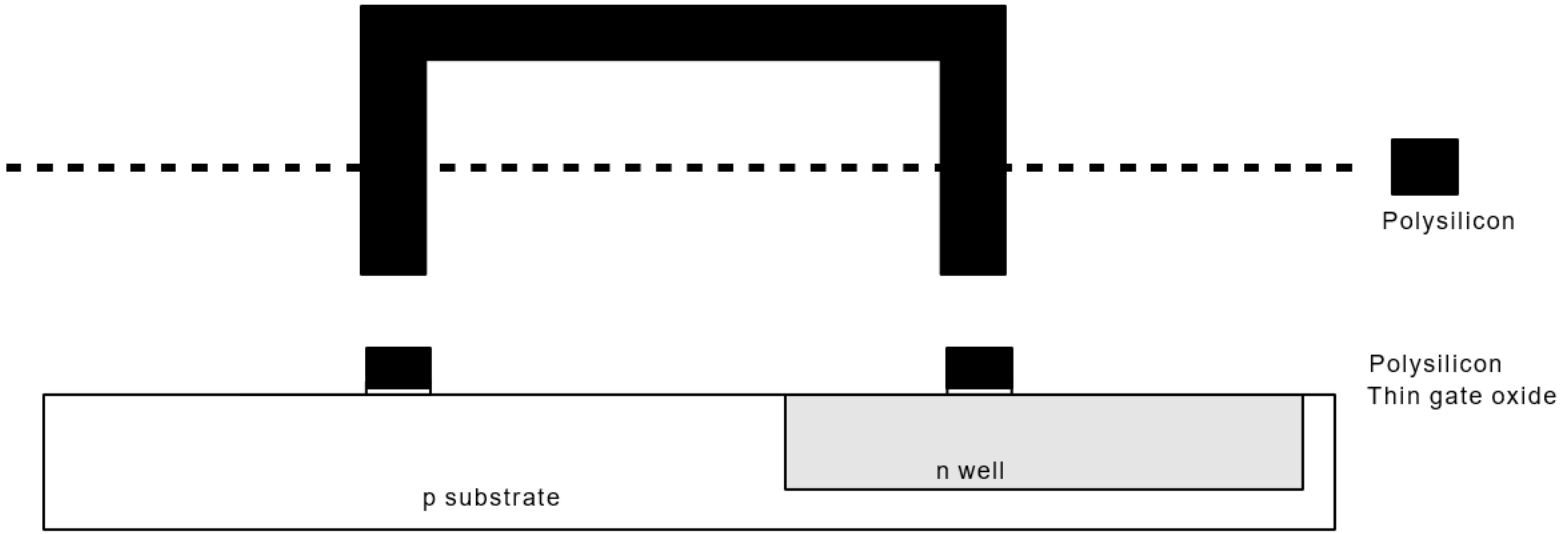
- Strip off the remaining oxide using something like HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

POLYSILICON (OR OTHER METAL) GATE

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers) for silicon dioxide
  - Thicker for hafnium oxide (high-k dielectric)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor

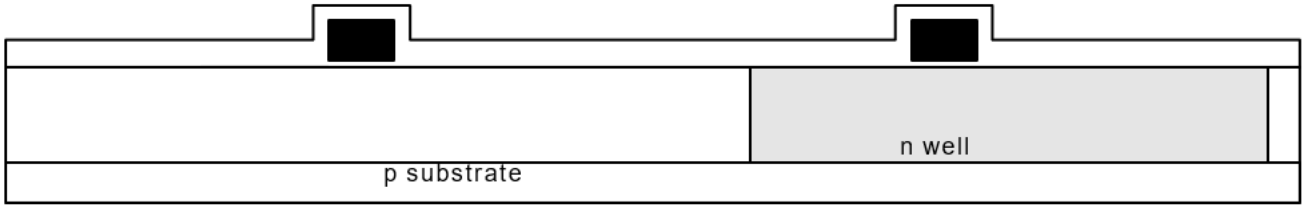
POLYSILICON PATTERNING

- Use same lithography process to pattern polysilicon



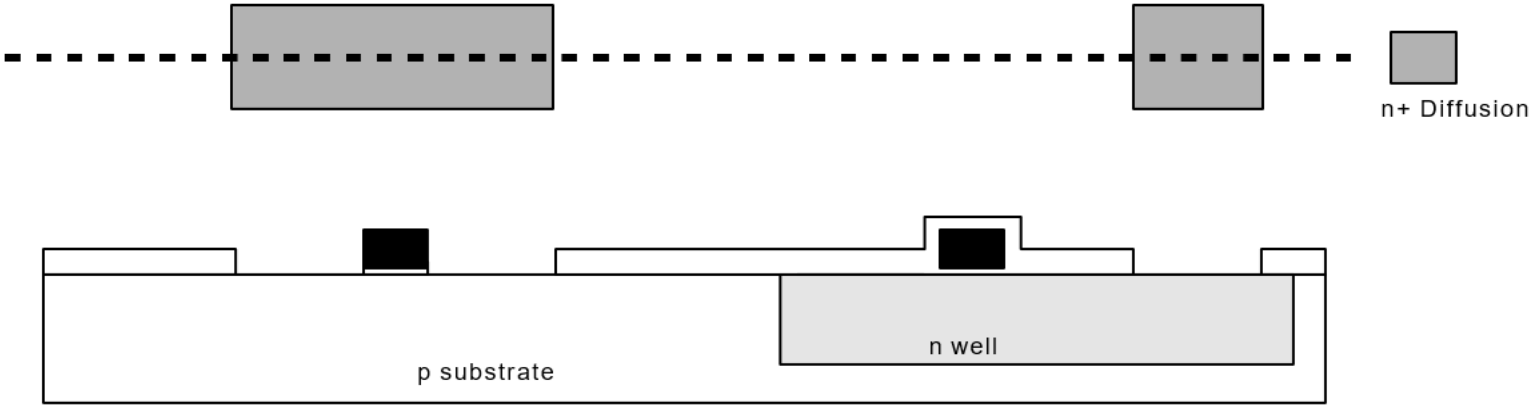
SELF-ALIGNED PROCESS

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms NMOS source, drain, and n-well contact
- Polysilicon gate structures will be used as “self-aligned” mask for drain/source



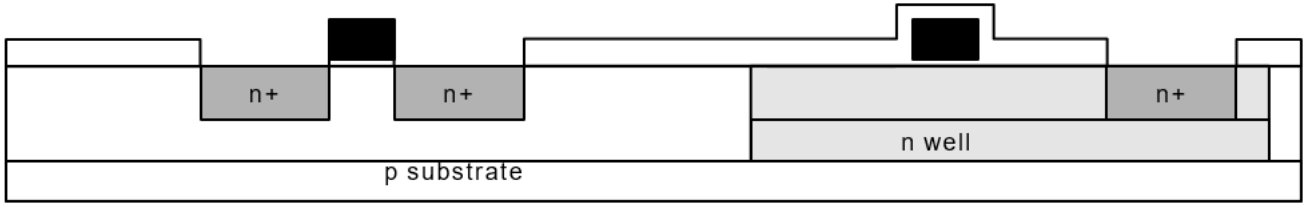
N-DIFFUSION (SOURCE, DRAIN AND N-WELL CONTACTS)

- Pattern oxide and form n+ regions
- Self-aligned process where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



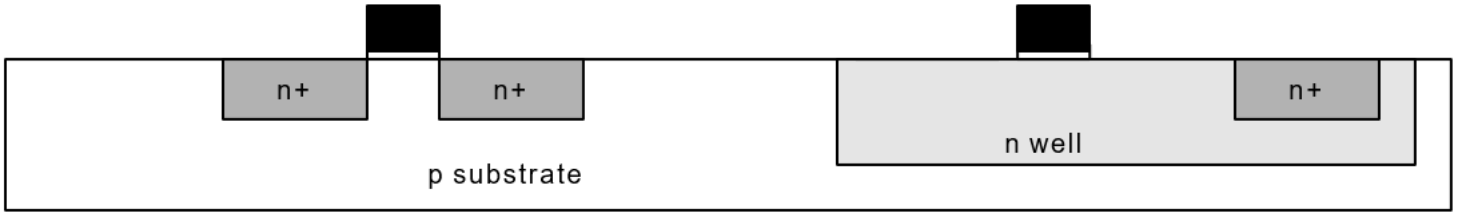
N-DIFFUSION CONTINUED

- Historically, dopants were diffused
- More often, ion implantation is used today
- But regions (source, drain, etc.) are still called “diffusion”



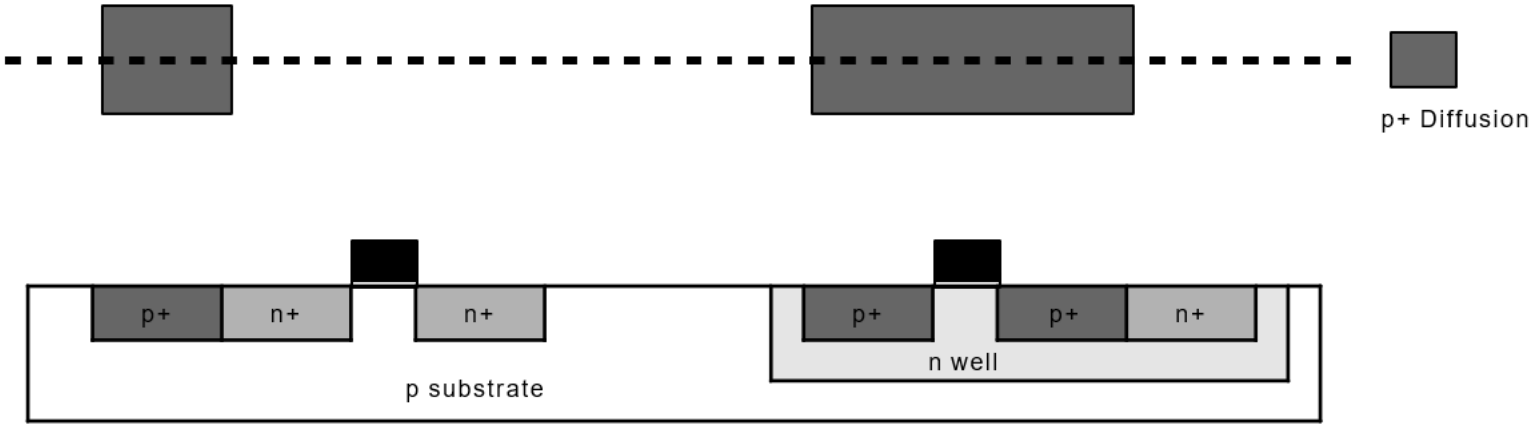
N-DIFFUSION CONTINUED

- Strip off oxide to complete patterning step



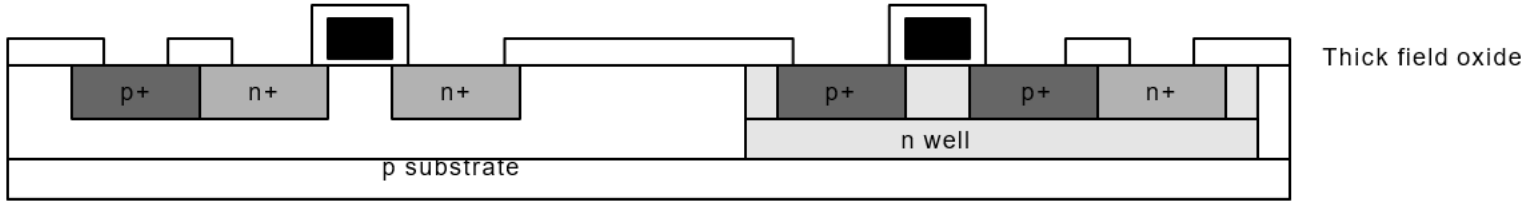
P-DIFFUSION

- Similar set of steps form p+ diffusion regions for PMOS source and drain and substrate contact



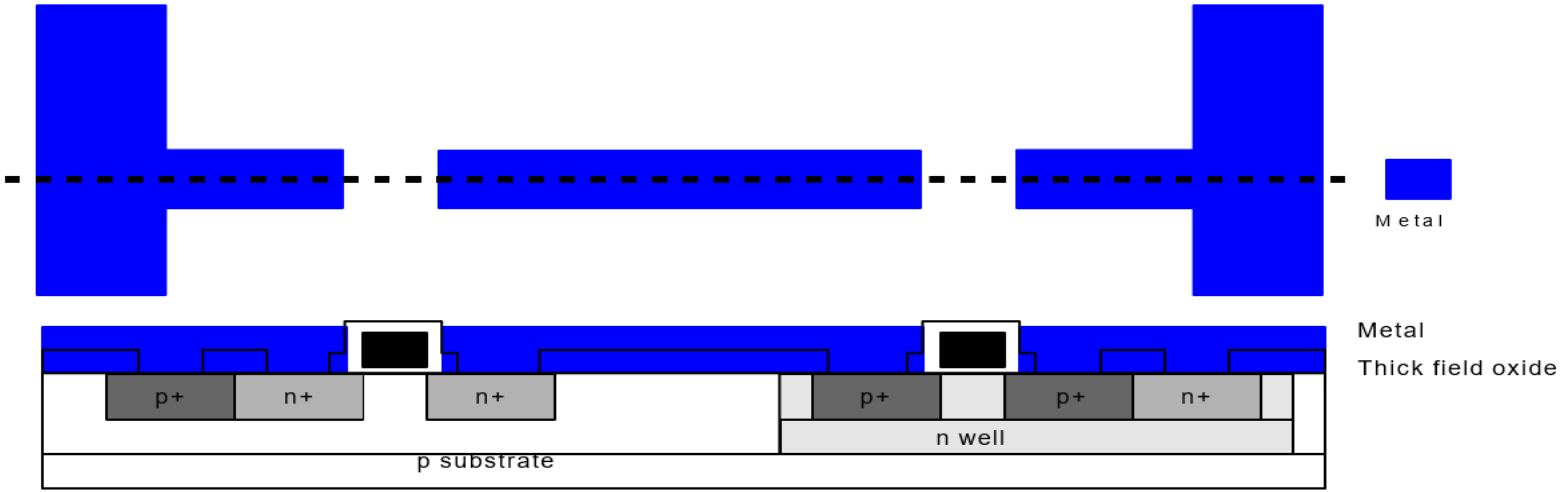
CONTACTS

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



METALIZATION

- Sputter on aluminum over whole wafer (may be copper, depending on process)
- Pattern to remove excess metal, leaving wires

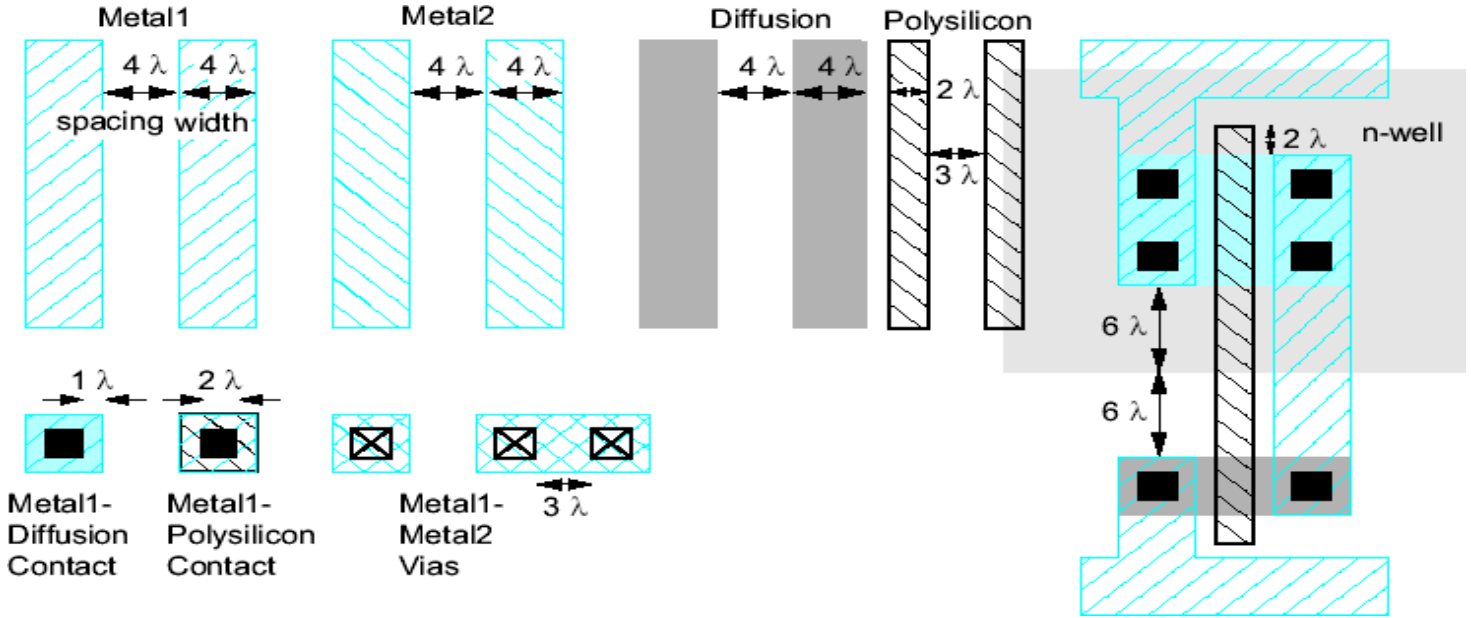


LAYOUT – CUSTOM PHYSICAL DESIGN

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain (gate length)
  - Set by minimum width of polysilicon
  - A little different for FinFETs (fin width)
- Historically, feature size has improved 30% every 3 years or so
- Normalize for feature size when describing design rules

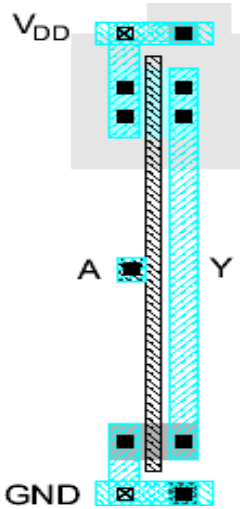
SIMPLIFIED DESIGN RULES FOR LAYOUT

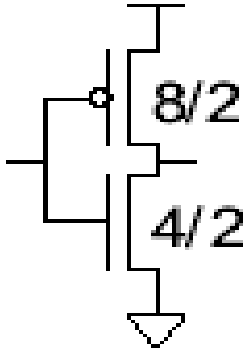
- Conservative rules are useful to get you started
- Older process use λ rules, where λ = f/2

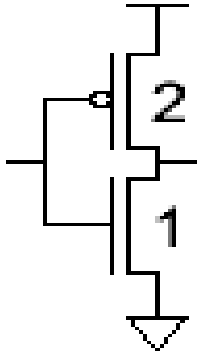


INVERTER LAYOUT

- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In *f* = 0.6 µm process (old!), this is 1.2 µm wide, 0.6 µm long







Thank you!