EE 431 - Lab 3 Report

Author: Ryan Cramer

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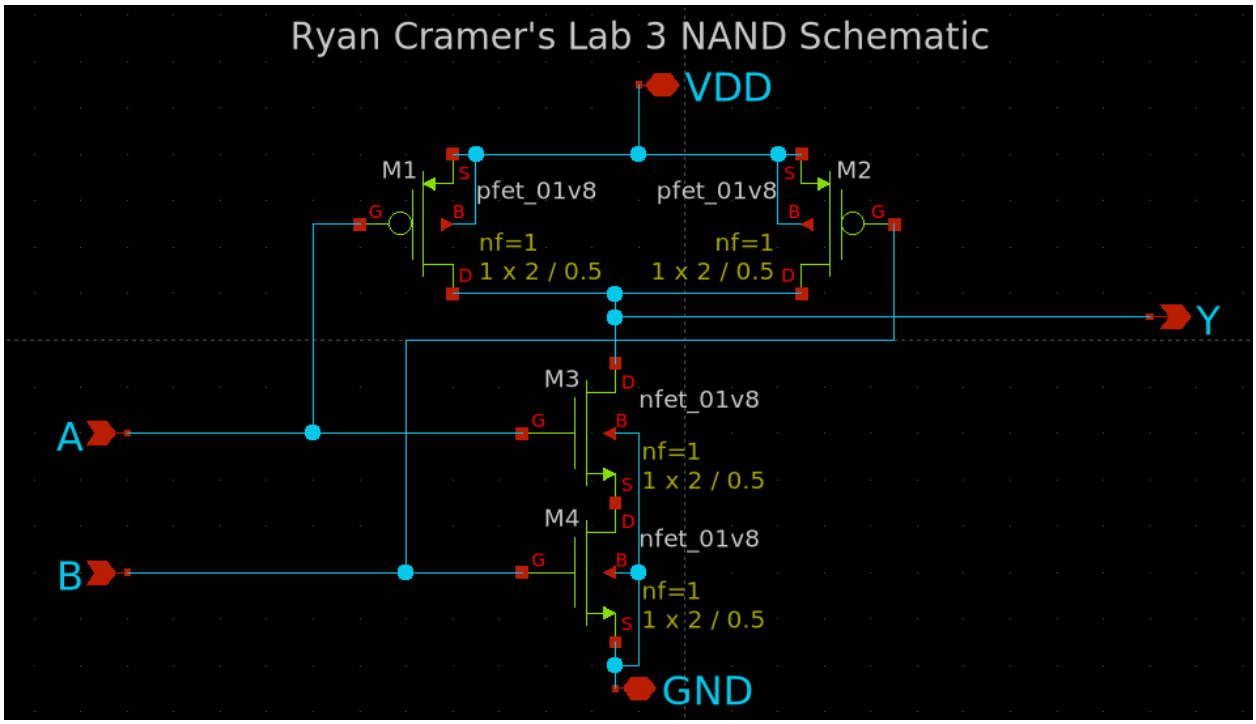
I. Introduction

In this lab we design, simulate, and physically lay out a 2-input NAND gate using the open-source CAD tools Xschem, Ngspice, and Magic. This extends the concepts learned in Lab 2 (the inverter layout) by implementing a slightly more complex CMOS logic gate that combines multiple pull-up and pull-down devices in parallel and series configurations. Through schematic capture, simulation, and physical layout, we verified the functional correctness and electrical integrity of the gate while ensuring that all Design-Rule-Check (DRC) and Layout-Versus-Schematic (LVS) conditions were satisfied.

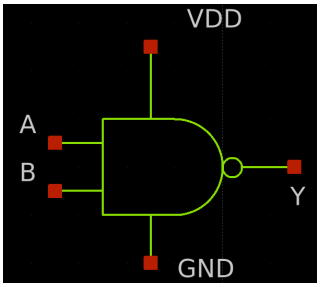
II. Methodology:

We first generate the transistor level schematic of the 2-input NAND using Xschem, which we use to generate our xschem netlist. Then, we generate a circuit symbol, as well as a testbench to verify that the NAND we designed works as intended before we do layout.

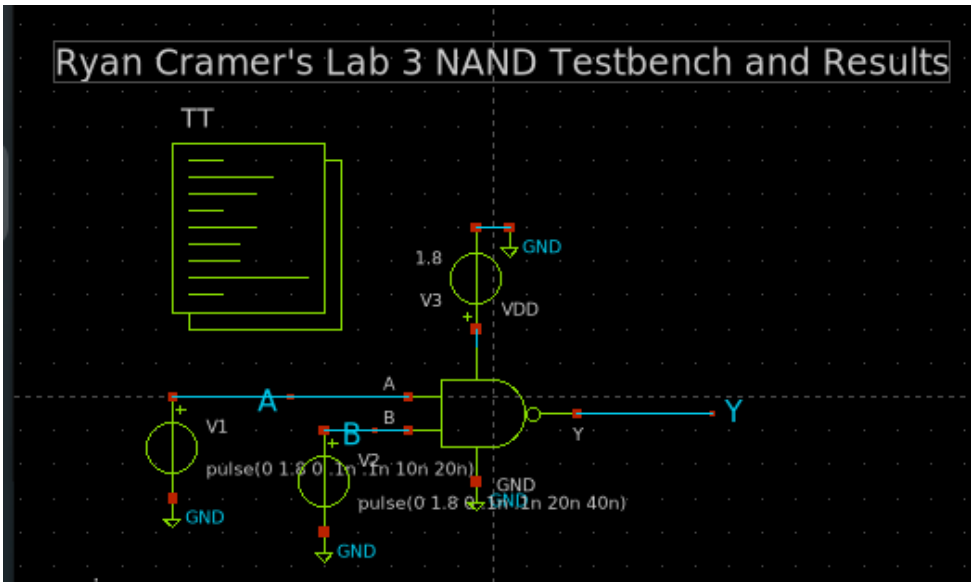
NAND Schematic (Xschem)

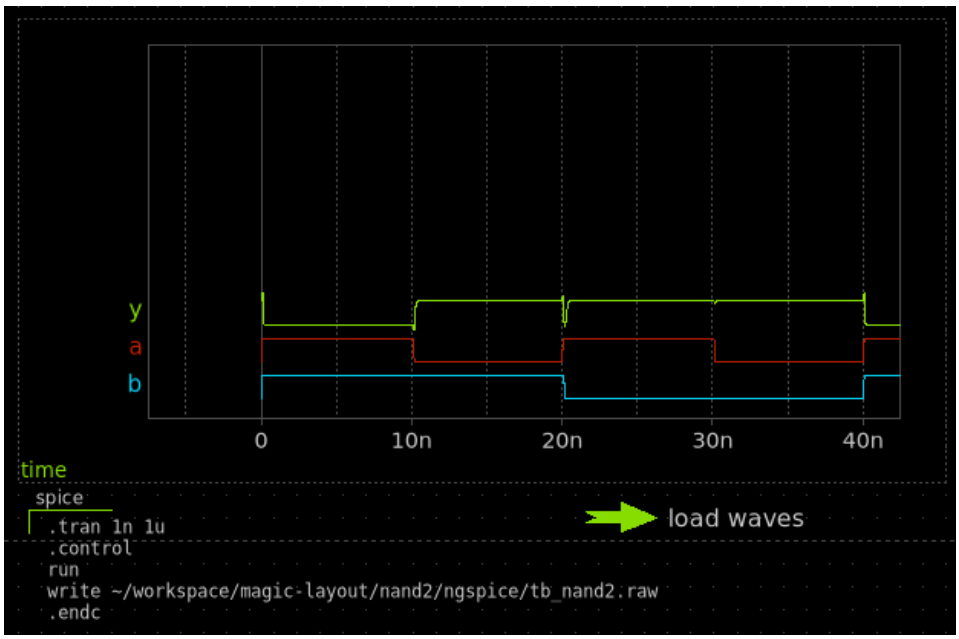


NAND Symbol (Xschem)



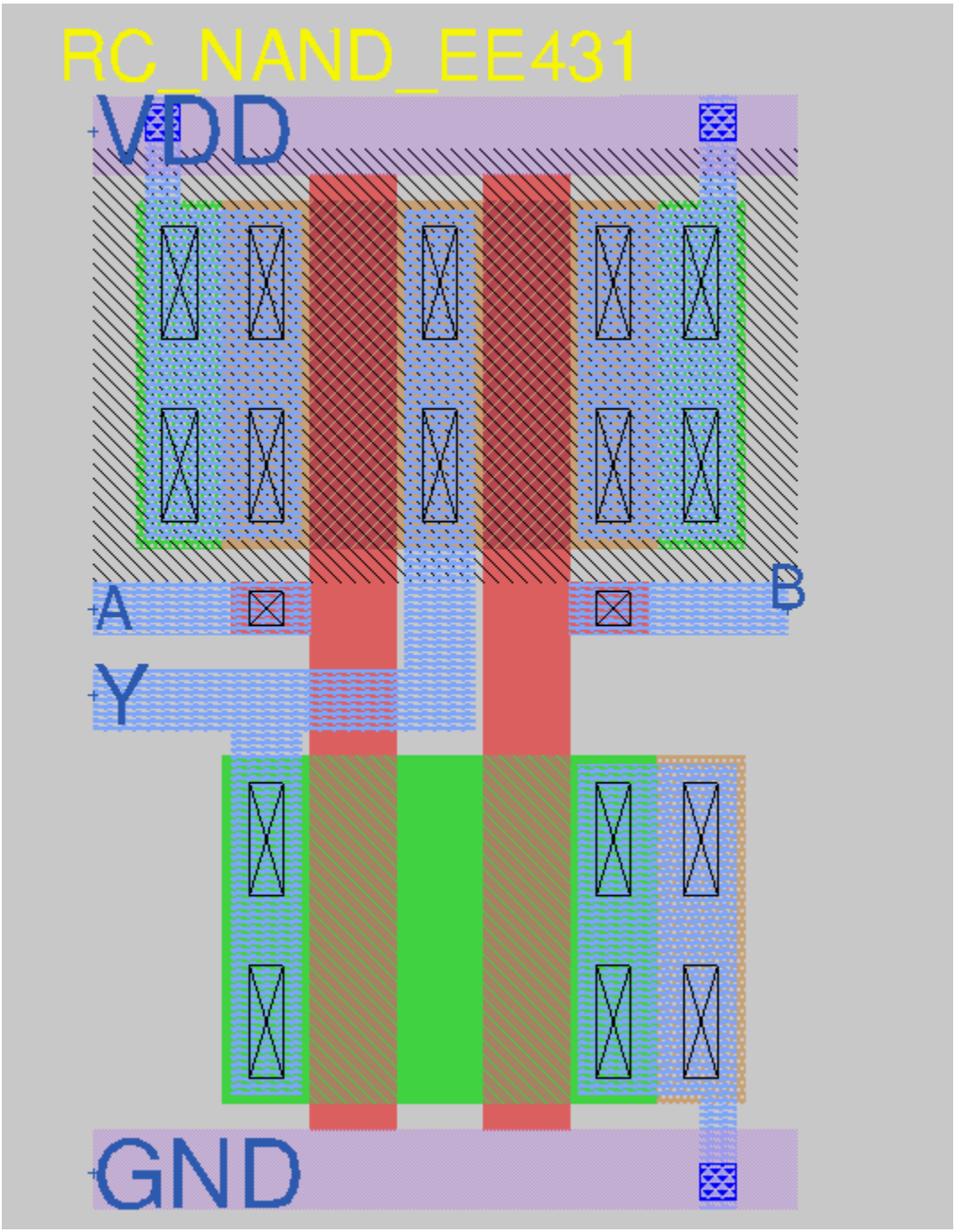
NAND Testbench Schematic and Results (Ngspice)





Now that we've verified that our transistor schematic is right: let's attempt layout:

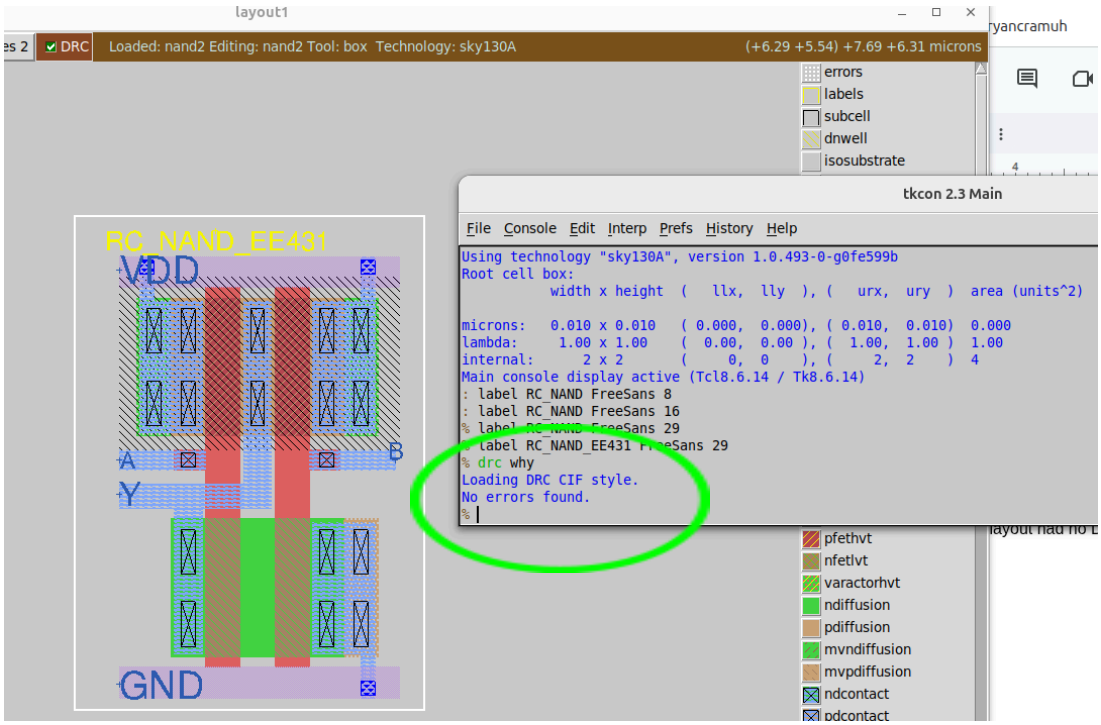
NAND Magic Layout:



As you can see, the pull-up network consists of two parallel PMOS feeding the input of two series NMOS. This accurately captures our intent, but let's check DRC and LVS.

III. Results

As you can see from the following screenshot, the layout had no DRC errors:



And we pass LVS against our extracted netlist Magic and our spice netlist from Xschem:

```
Logging to file "comp.out" enabled
Circuit sky130_fd_pr__nfet_01v8 contains no devices.
Circuit sky130_fd_pr__pfet_01v8 contains no devices.

Contents of circuit 1:  Circuit: 'netgen/mnand2.spice'
Circuit netgen/mnand2.spice contains 4 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   2
  Class: sky130_fd_pr__pfet_01v8 instances:   2
Circuit contains 6 nets.
Contents of circuit 2:  Circuit: 'netgen/xnand2.spice'
Circuit netgen/xnand2.spice contains 4 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   2
  Class: sky130_fd_pr__pfet_01v8 instances:   2
Circuit contains 6 nets.

Circuit 1 contains 4 devices, Circuit 2 contains 4 devices.
Circuit 1 contains 6 nets,    Circuit 2 contains 6 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
ubuntu@asic:~/workspace/magic-layout/nand2$
```

IV. Discussion

This lab reinforced the hierarchical design process from schematic to physical layout for a slightly more complex logic gate than the inverter. I learned how series and parallel MOS configurations implement Boolean functions and how transistor placement directly influences the final mask geometry.

The main challenge was routing the internal node between the two NMOS transistors. Originally, I connected the bulk of the PMOS connected NMOS to the drain of the next NMOS, but that doesn't work because it must be connected to ground. Once I fixed my schematic, DRC passed.

Once the layout passed both DRC and LVS checks, it confirmed that my understanding of transistor-level NAND design and CMOS layout practices had improved significantly. This exercise demonstrated how logical expressions are realized physically and prepared me for more advanced standard-cell and full-custom designs.