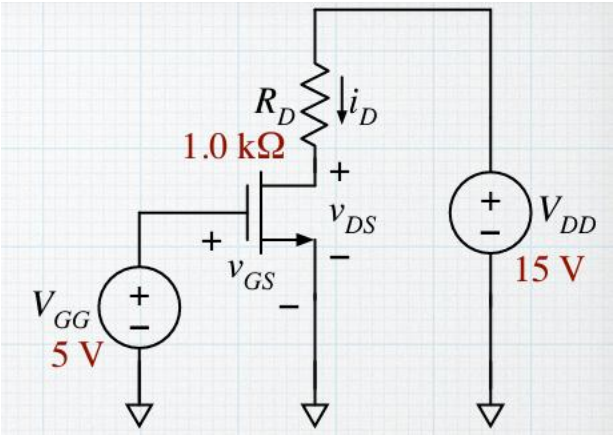
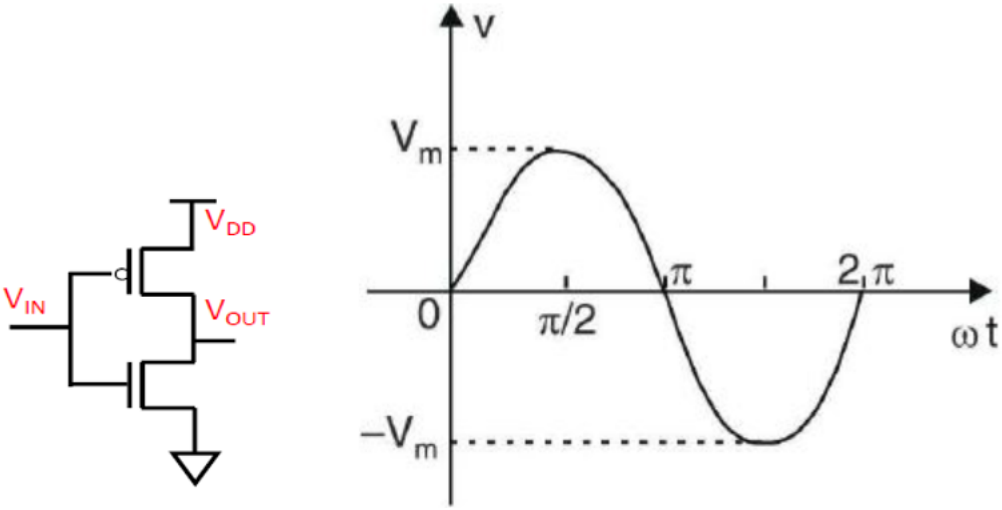
Problem 1: For the circuit below, find the value of i_d and v_{DS}. Assume that the MOSFET threshold voltage is 1V, and $\beta_n=\mu_n C_{ox}\frac{W}{L}=1$ mA/V². What region of operation is the NMOS operating in?



Problem 2: Consider a CMOS inverter with the following parameters: VDD=3V, V_{TN} = 0.6V V_{TP} = -0.82 V. $\mu_n C_{ox}$=100 μA/V², μ_n=2.2 μ_p.

i. Determine the β-ratio (β_n/β_p) for a switching threshold of V_M = 1.3V.
ii. Determine the PMOS device width and length if the NMOS device width is 1μm and length is 500nm.

Problem 3: Consider a CMOS inverter as follows, where VDD is 5V, and GND is 0. Assume that there is a sinusoidal voltage at the input, V_{IN} as below, where V_m=5V. Sketch the output voltage V_{OUT} assuming a switching threshold V_M of 2.5V. Clearly show the points where the output voltage transitions.



Problem 4: Sketch a 3-input NOR gate with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).