EE 431 - Lab 1 Report

Introduction to Bottom Up Design

Author: Ryan Cramer

I. Introduction

In this lab, we start by building the most foundational CMOS devices, the Inverter, 2-input NAND, and 2-input NOR. We then use our primitive logic gates to construct other logic gates, such as AND/OR, and eventually scale to build transmission devices such as a 2:1 Mux and 4:1 Mux.

II. Methodology

We scale from Inverter to 4-1 Mux by leveraging DeMorgan's law and modular design. First we build a CMOS inverter which can perform the simplest logical operation: inversion. From there, we build CMOS NAND and NOR devices using 4 transistors. By leveraging DeMorgan's law:

NAND + inverted inputs = OR

~(~A & ~B) = (A + B)

NOR + inverted inputs = AND

~(!A + ~B) = (A & B)

…we can use our NOR, NAND, and inverter to build the AND and OR gate. To build the 2:1 multiplexor, we use two AND gates, an OR gate, and one inverter, so that we can make sure we have (A&~SEL) + (B&SEL), the proper 2:1 Mux function. Once we have constructed our 2:1 Mux, we can go to 4:1 easily. We use three 2-1 Mux, by configuring two with SEL0 as their SEL, and one with SEL1 to get the proper 4:1 Mux function:

(A & ~SEL0 & ~SEL1) + (B & SEL0 & ~SEL1) + (C & ~SEL0 & SEL1) + (D & SEL0 &SEL1)

Since SEL1 controls the leading Mux, which takes in the output of the two prior Muxes, being controlled by SEL0, SEL1 selects whether we are using A and B or C and D. For A and B, SEL0 controls whether we are using A (0) or B (1). For C and D, SEL0 controls whether we are using C (0) or D(1).

Figure 1.1 - CMOS Inverter Schematic and Symbol

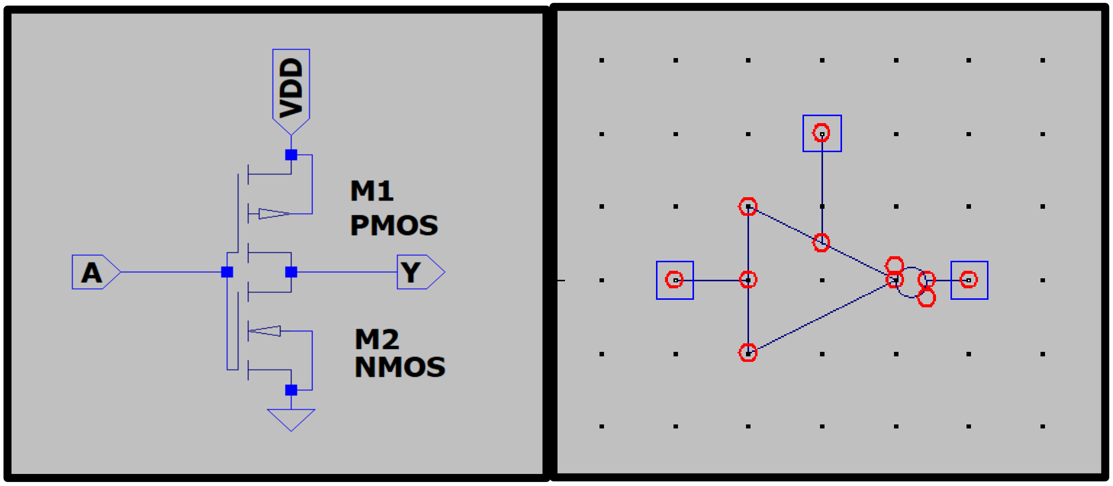


Figure 1.2 - CMOS 2-Input NAND Schematic and Symbol

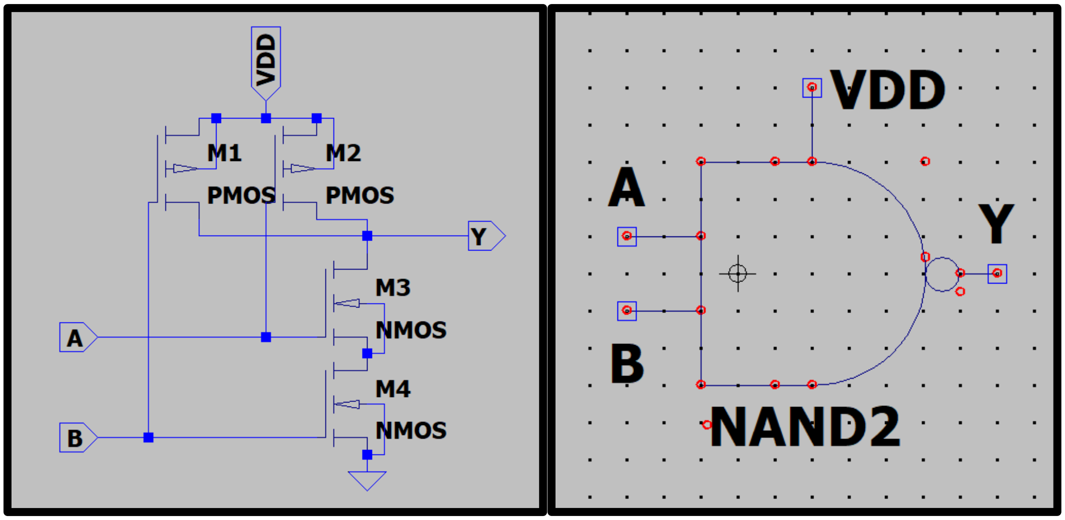


Figure 1.3 - CMOS 2-Input NOR Schematic and Symbol

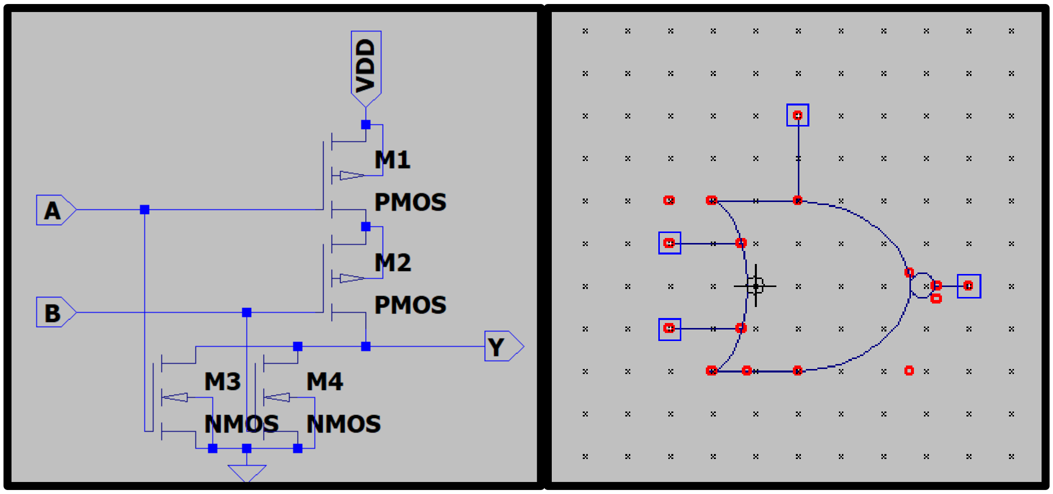


Figure 1.5 - 2:1 Mux using NAND, NOR, and Inverter - Schematic and Symbol

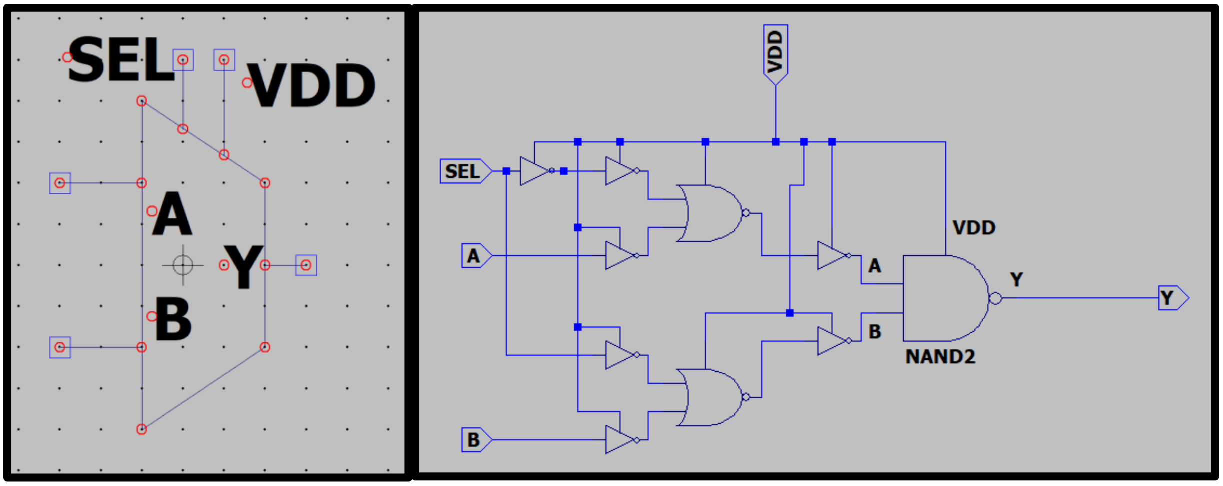
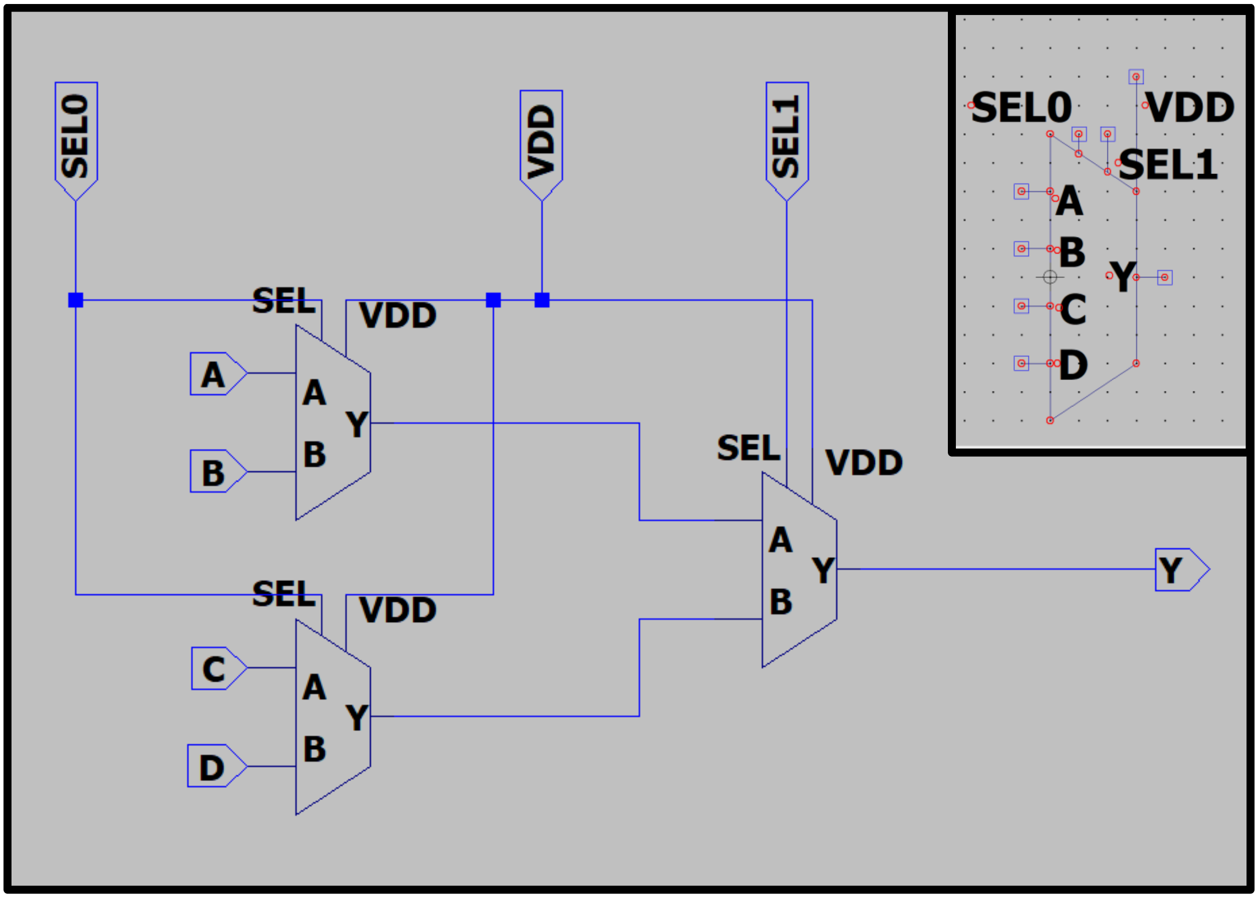
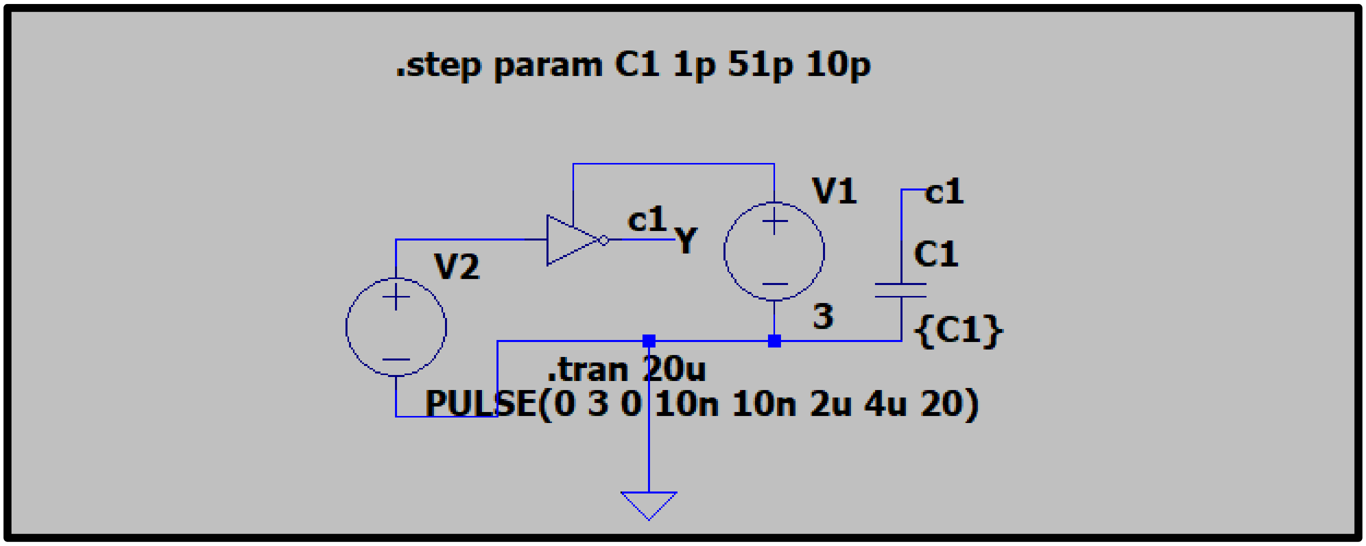


Figure 1.6 - 4:1 Mux Schematic and Symbol

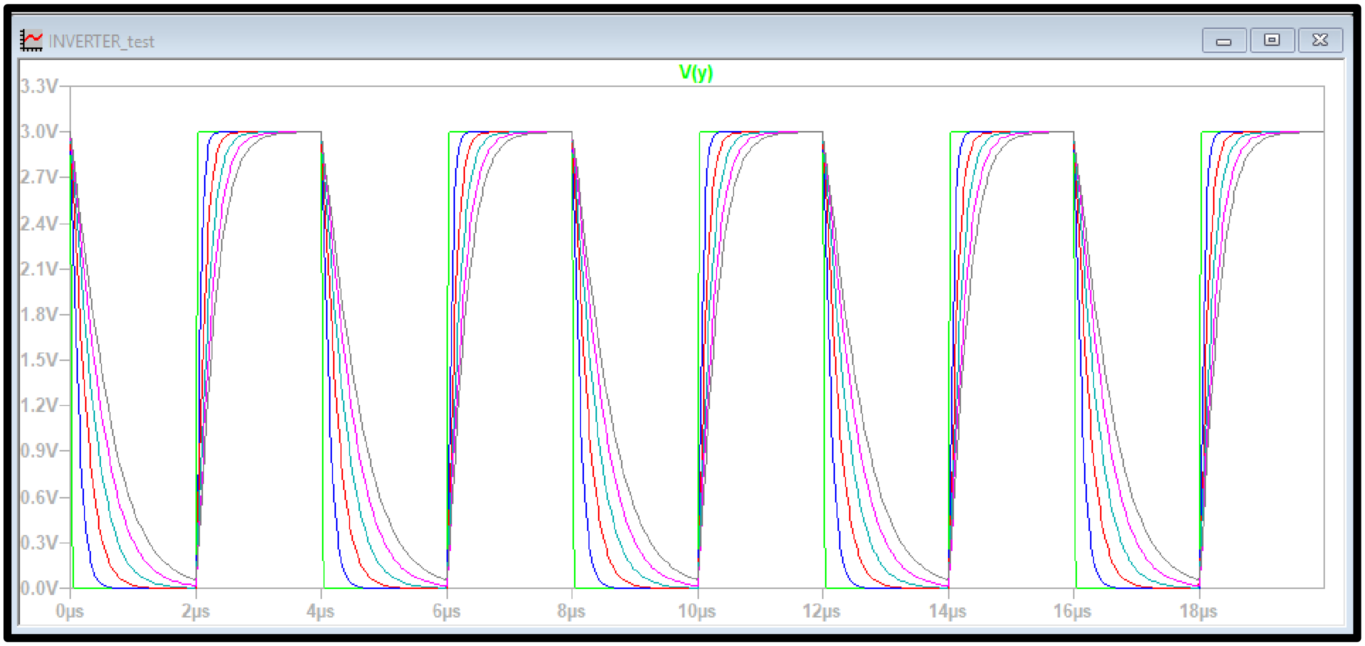


III. Result

Figure 2.1 - Inverter with Parametric Capacitor



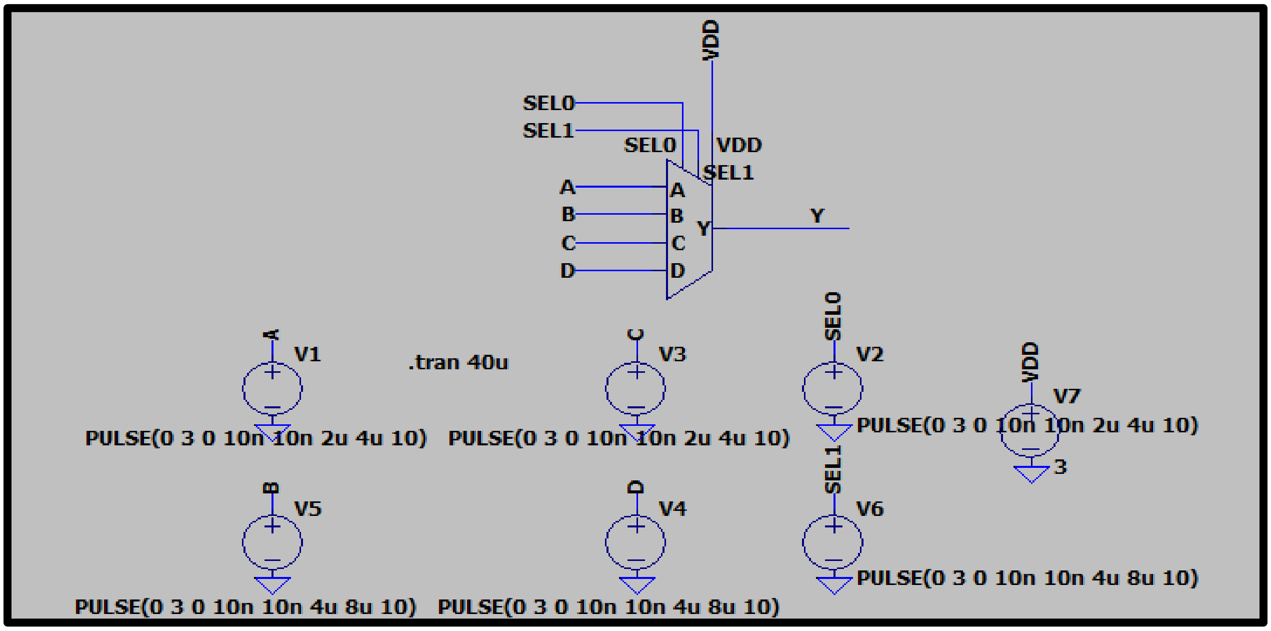
```
.step param C1 1p 51p 10p
.tran 20u
PULSE(0 3 0 10n 10n 2u 4u 20)
```

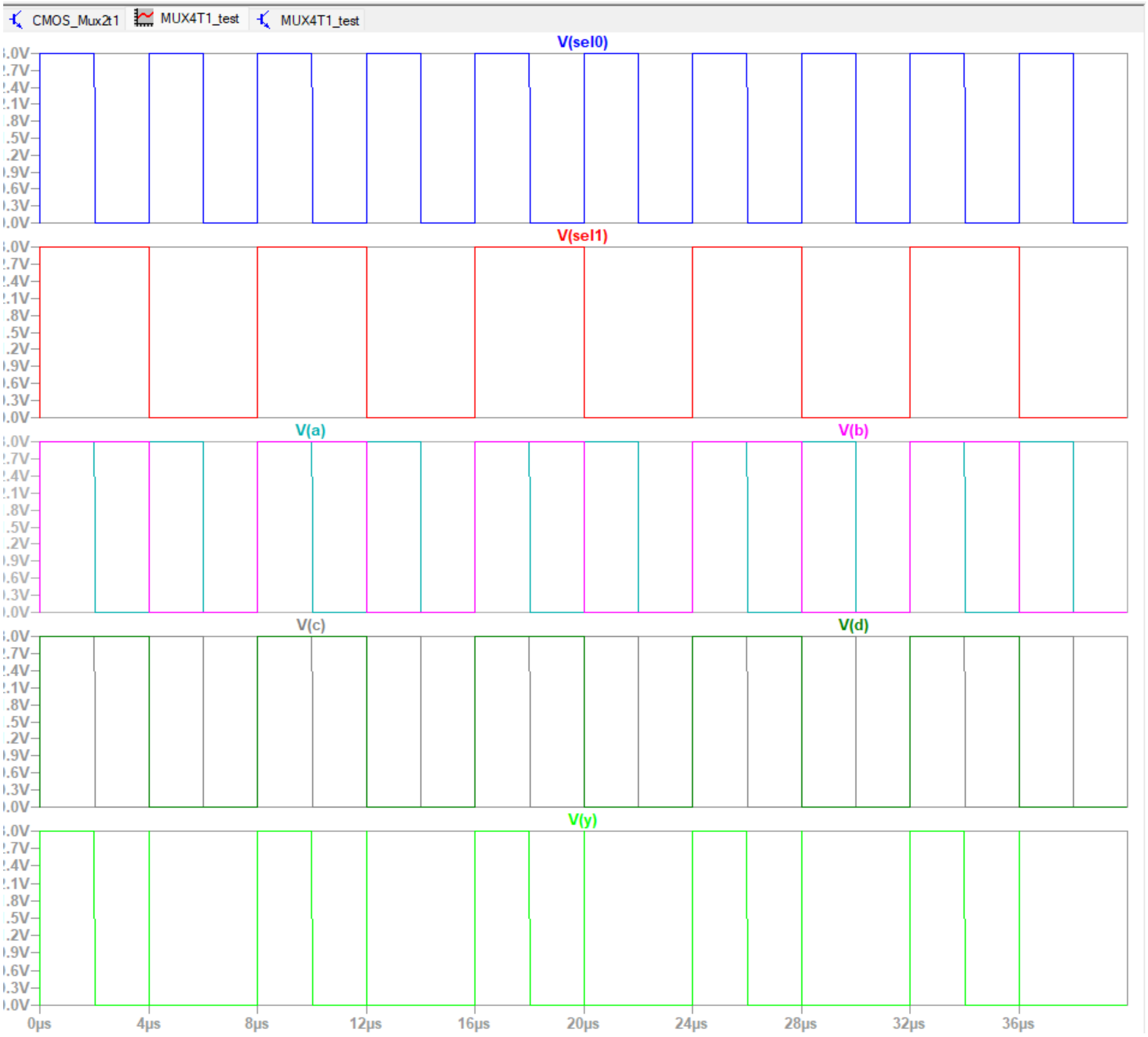


Analysis of Inverter with Parametric Capacitive Load:

The results show us that as the load-capacitor's capacitance increases, the transitions from 0 to 3 volts take approximately 1ns longer at 51pf. During the inverter's transition from '1' to '0', the capacitor drains, and the extra energy causes high-low transitions to take much longer (about 2ns at 51pf). This shows us that by attaching a capacitive load, we can affect the transition of our inverter, so we want to reduce or remove the load capacitance to have our inverter have cleaner transitions

Figure 2.2 - 4:1 Mux Final Simulation Schematic and Waveform


VDD
SEL0
SEL1
SEL0
VDD
SEL1
A
B
C
D
A
B
C
D
Y
Y
A
V1
.tran 40u
C
V3
SEL0
V2
VDD
V7
PULSE(0 3 0 10n 10n 2u 4u 10)
PULSE(0 3 0 10n 10n 2u 4u 10)
PULSE(0 3 0 10n 10n 2u 4u 10)
3
B
V5
D
V4
SEL1
V6
PULSE(0 3 0 10n 10n 4u 8u 10)
PULSE(0 3 0 10n 10n 4u 8u 10)
PULSE(0 3 0 10n 10n 4u 8u 10)



0-2ns: SEL[1:0] = 2’b11 (SEL0 and SEL1 are “high”), D is active, D is high, so Y is high
2-4ns: SEL[1:0] = 2’b10 (SEL0 is “low”, SEL1 is “high”, C is active, C is low, so Y is low
4-6ns: SEL[1:0] = 2’b01 (SEL1 is “low”, SEL0 is “high”), B is active, B is low, so Y is low
6-8ns: SEL[1:0] = 2’b00 (SEL0 and SEL1 are “low”), A is active, A is low, so Y is low

By combining inverter, Nor, and Nand gates, we are able to leverage DeMorgan’s law to construct AND and OR gates for the 2:1 Mux and then use the 2:1 Mux to construct a 4:1 Mux. For the 4:1 Mux, SEL0 toggles SEL for the 2:1 Muxes receiving A, B, C, and D. When SEL0 is low, A or C is active, SEL0 is high, B or D is active. The leading bit of the 4:1 Mux, SEL1, toggles between the upper Mux: A and B, and the lower Mux: C and D. Treating SEL1 and SEL0 as a bit pairing {SEL1,SEL0}, A=2’b00, B=2’b01, C=2’b10, D=2’b11.

IV. Discussion

Through analyzing the various CMOS devices, I learned how to use modular design practice to scale CMOS technology to larger and larger devices, as well as learned the effects of load-capacitance on our switching networks, and how that can affect the timing of our transitions. One thing I had to remember was that to make an OR gate from a NOR gate, you have to use DeMorgan’s law. Originally, I built and tested my Inverter, NAND, and NOR, and then constructed AND and OR gates. I forgot to apply DeMorgan’s law, so I tried making an AND gate with two Inverters and a NAND, which is logically an OR. Once I corrected the convention, and used DeMorgan’s law, I was easily able to scale my design to the 4:1 Mux, by first making a 2:1 Mux using 7 Inverters, 2 NANDs, and 1 OR, so 26 transistors. Afterwards, I scaled to the 4:1 Mux using SEL1 to control the output 2:1 Mux, and SEL0 to control the two input 2:1 Mux, I was able to construct the 4:1 Mux using 78 transistors.