Problem 1: Consider the design of a 3-input AND-OR-INVERT (AOI) gate. The function is $Y = \overline{AB + C}$. (8 points)

i. Sketch a transistor-level schematic with transistor widths chosen to approximate the effective rise and fall resistances equal to a unit inverter (assuming pmos width is double the nmos width).

ii. Compute the rising and falling delays of the AOI gate driving h identical unit sized NOR gates using the Elmore delay model for specific inputs. For rising delay, assume A=C=0, B=1, and for falling delay, assume A=B=1, C=0. Assume that every source/drain has fully contacted diffusion and contacted diffusions are shared wherever possible.

Problem 2: Let a 4x inverter have transistors four times as wide as those of a unit inverter. If a unit inverter has three units of input capacitance and parasitic delay of p_{inv}, what is the input capacitance of the 4x inverter? What is the logical effort? What is the parasitic delay? (3 points)

Problem 3: Consider a 7-stage ring-oscillator (7 inverters in a loop). Each inverter is unit sized but also drives a total of 4 inverters (one in the oscillator and 3 off-path). Using logical effort, estimate the period of oscillation in units of τ (3RC) and the frequency f of the ring-oscillator. (3 points)

Problem 4: You are given the following multistage logic circuit built from static CMOS gates. Determine the sizing values for x and y that minimize the delay through the path from input A to output F. NOTE: Values written on gates represent the input capacitance of the respective gate. Assume load capacitance at F is 20C. (Also, the first gate in the picure is an AOI gate as Problem 1) (6 points)