Lab 3: Schematic and Layout Design of a 2-Input NAND Gate

In this lab, we designed a 2-input NAND gate using xschem by drawing a schematic and making a symbol. Then we verified it using ngspice. Then we designed the NAND layout using magic. I don't have a specific format in mind. So if you want to include more information, that's okay too.

Lab tasks:

- We built a two-input NAND schematic and symbol. Did verification with ngspice.
- Designed layout
- Verified that the layout is drc free
- LVS matches

Report guideline:

There needs to be 4 sections.

Introduction: In a few words, describe what this lab is about

Methodology: Describe briefly how you built the NAND. Then how you built the layout. Briefly describe what layers you used to get the inverter. Provide screenshots of your schematic, symbol, testbench schematic and layout.

Result: Show me the result of your verification of schematic. From layout, give me screenshots showing it's drc clean and LVS matches. **Also copy the content of both spice files in your report.**

Discussion: Describe in a few words what you learned from this analysis, and the challenges you faced.