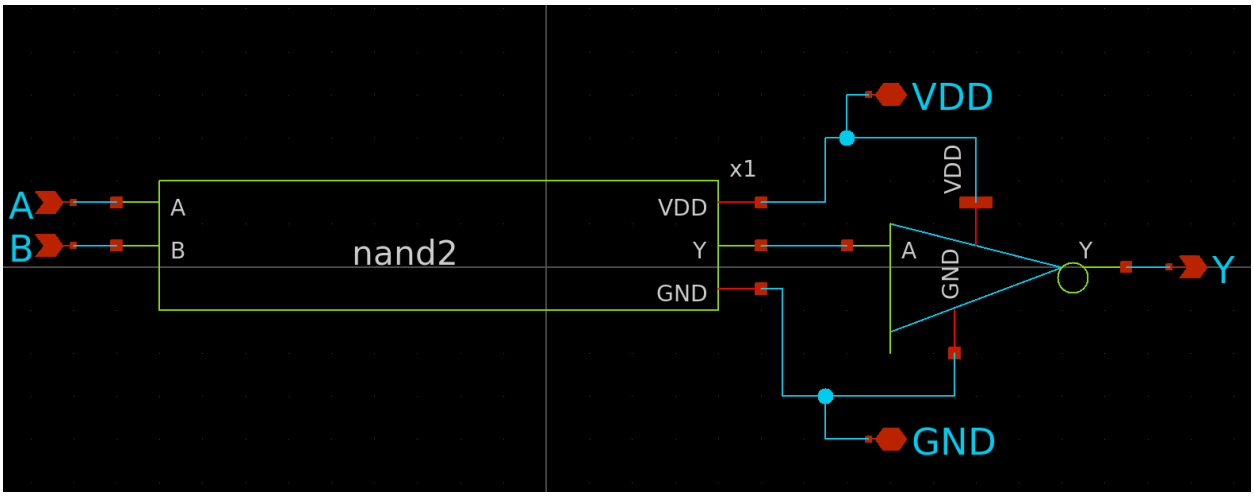
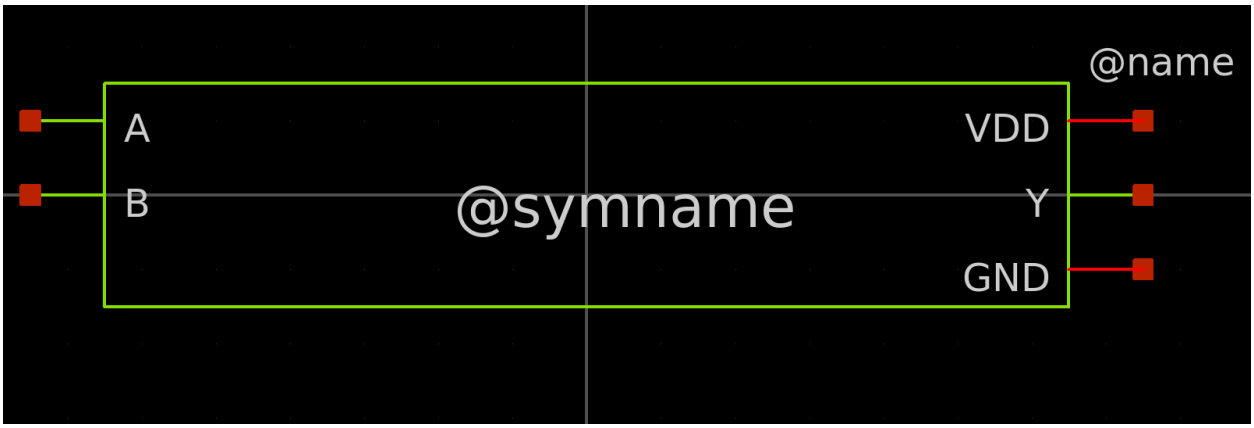
Designing the schematic and the layout of a 2-input AND gate using Skywater 130nm process

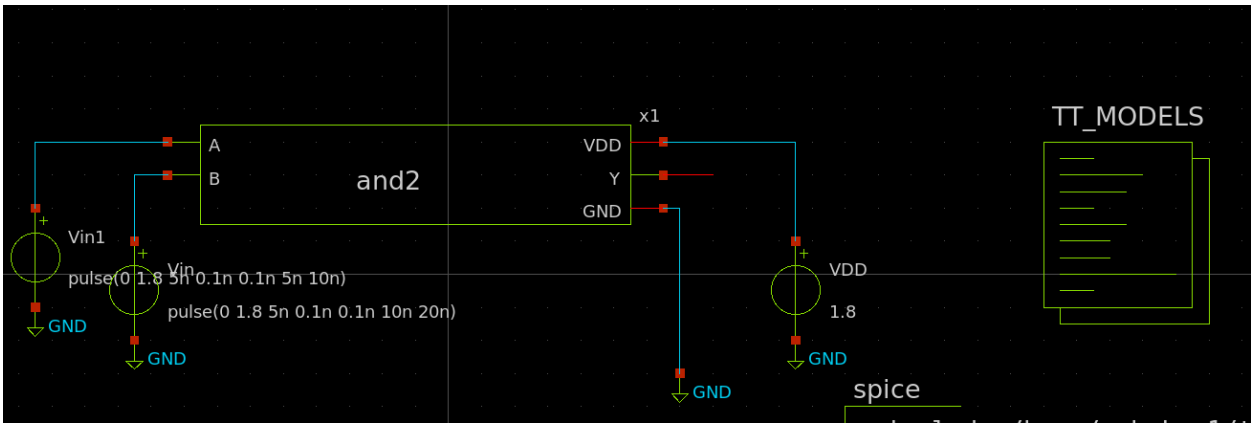
For this week's lab, we will design a 2-input AND gate. First design the schematic using the nand gate and the inverter you designed before, which will look like following.



Then create a symbol.



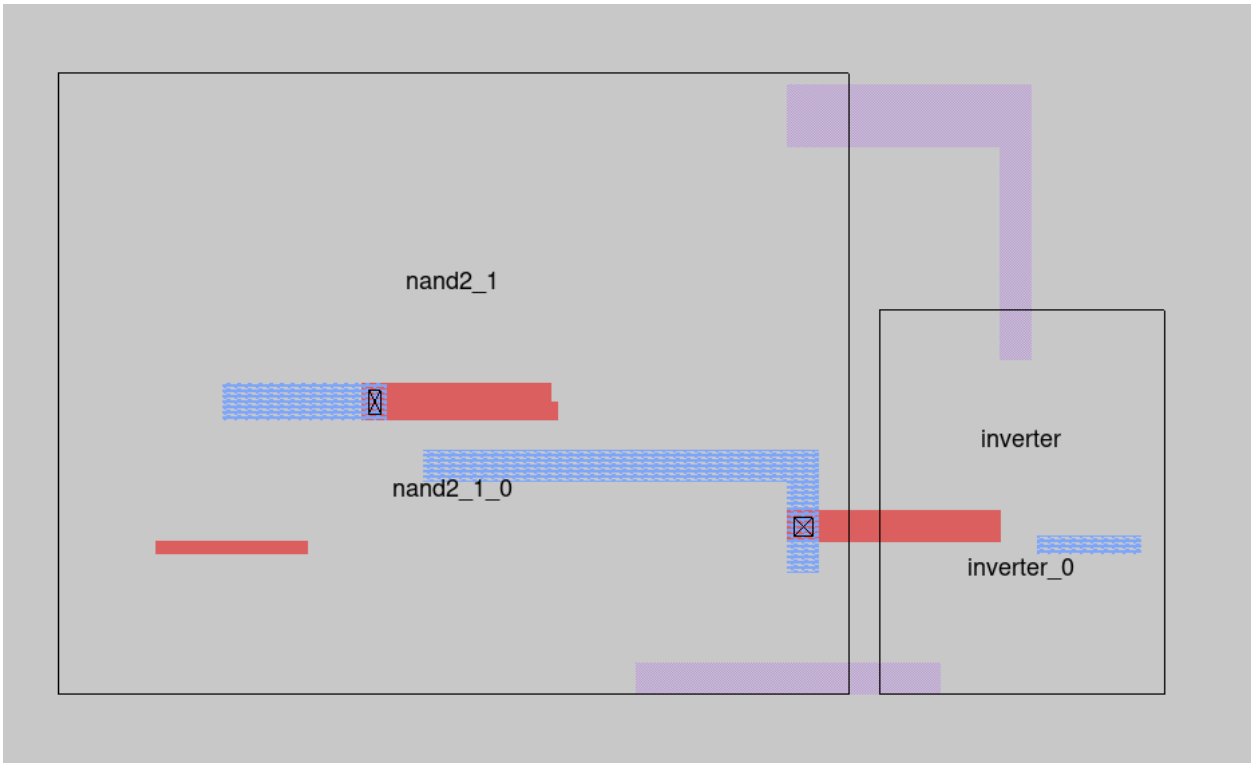
Then verify the functionality using a testbench like following.



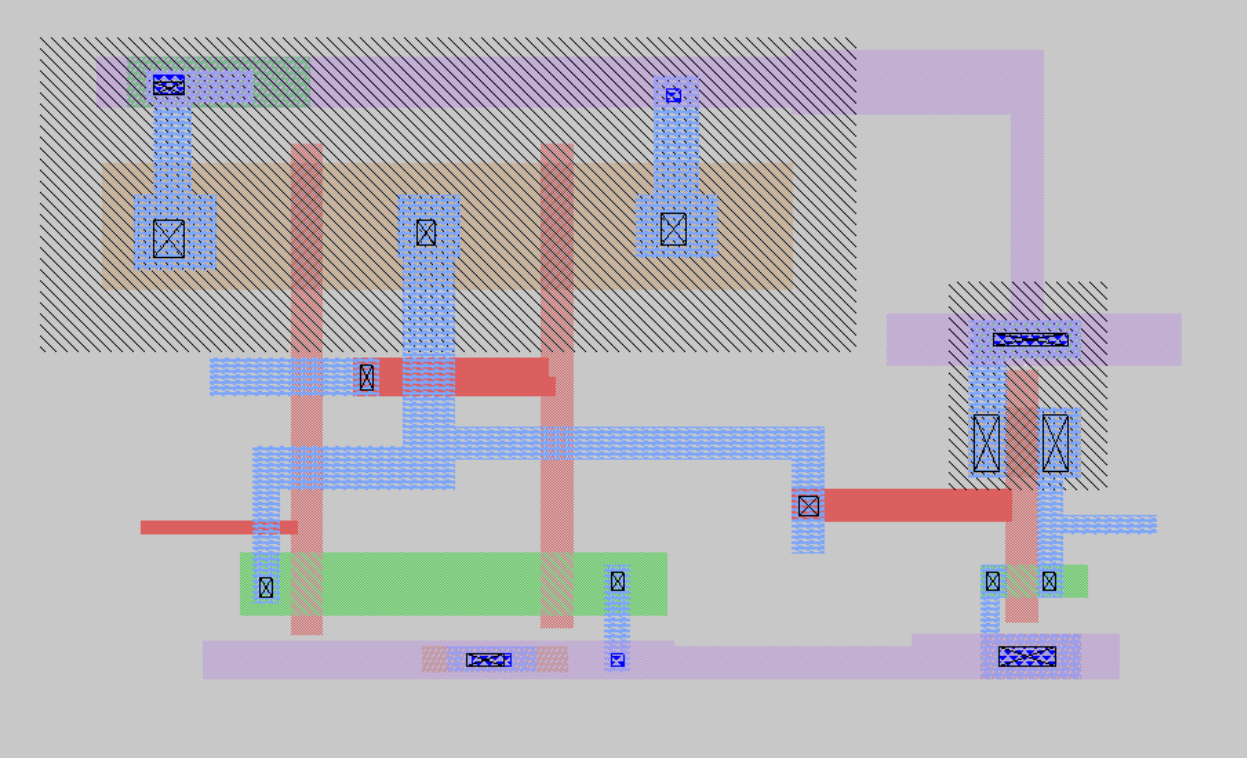
Then design the layout. You can do it by using NAND and inverter layouts. To do that, use the commands:

getcell nand2

getcell inverter



You will see the names, but not the gates. To do that, click on the boxes where the components layout will be, press the key “x”. The components will be visible after that. Then connect the VDDs and GNDs of both gates. Connect the output of Nand2 to the input of inverter.



Add labels and ports. One thing to keep in mind is that, add labels and ports to the parts that you added in this particular layout. For example, don't define a port on the VDD of nand, define it between the connection where you connected both vdds, as this is something you drew in this layout, not imported. The filename should be the same as the schematic. Also make sure the port order matches the one from the schematic. Otherwise it will create problems for post-layout simulation.

Make sure that it is DRC clean. Finally, check LVS. The detailed tutorials are already posted for the inverter. In this case, you can also use

ext2spice lvs

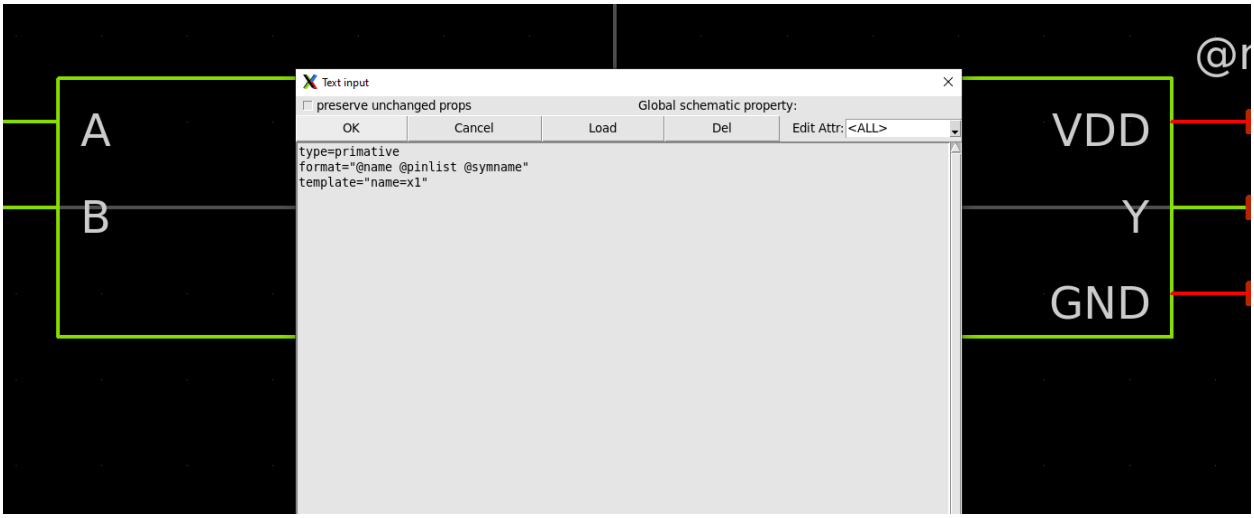
ext2spice hierarchy on

Depending on what you need.

Post-layout simulation:

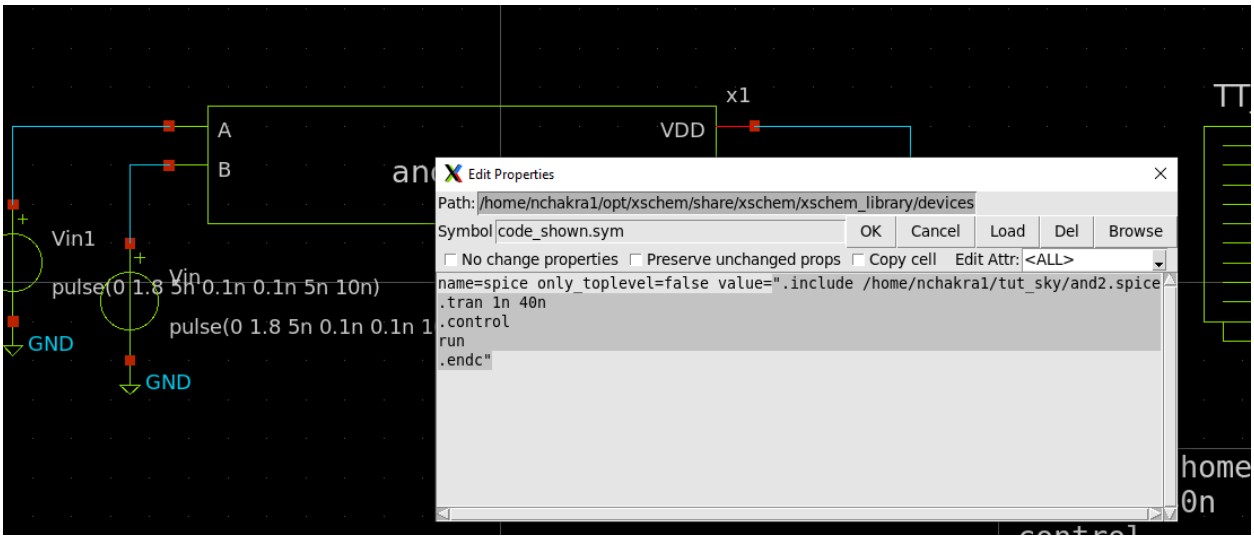
We will use the spice file from magic for post-layout simulation. To do that, open your and.sym symbol. Then press Q on the symbol. Then change the type from subcircuit to primative.

Save it.



Then open testbench, in your spice directive, include the path to your layout spice file.

.include “path_to_spice”



Then run netlist, followed by simulation.