

Lab1- Introduction to UMS GH15 PDK

Joe Schultz & Anurag Bhargava

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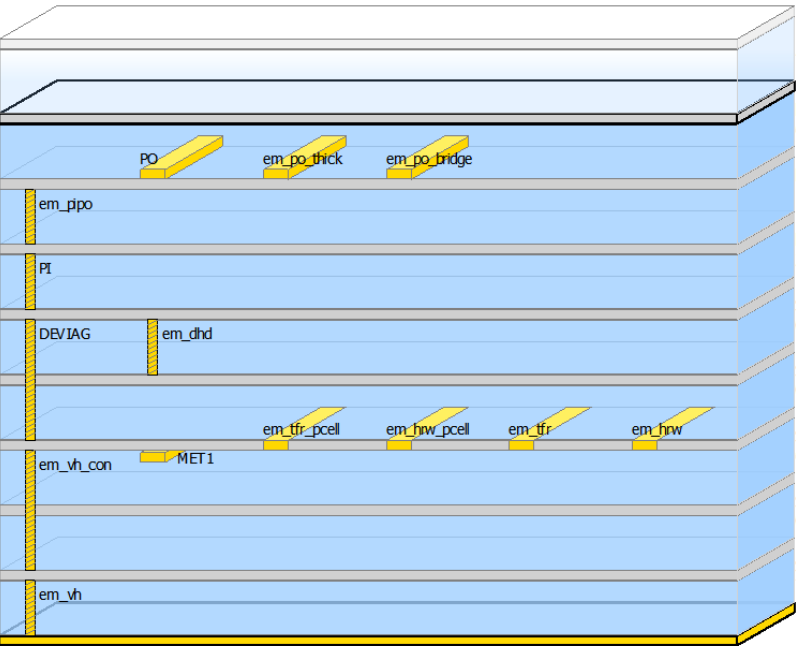
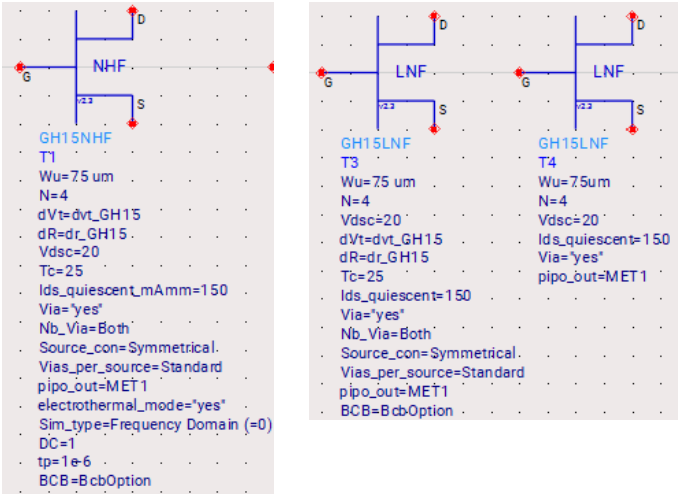
Lab 1 Overview

Objectives and Purpose

- Lab 1 will introduce the United Monolithic Semiconductors (UMS) 150nm GaN Process Design Kit (PDK) in Keysight's Advance Design System (ADS)
 - UMS website: <https://www.ums-rf.com/>
 - UMS Product Examples: <https://www.ums-rf.com/products/>
 - UMS Design Kits: <https://my.ums-rf.com/login/>
- Lab1 steps are:
 1. Create an ADS workspace "pdk_analysis" and install the PDK
 2. Inspect the component palette & parameters; place components (schematic & layout)
 3. Simulate Passive components: a)Spiral, b) MIM Cap, c) Thin Film Resistors, d) MLIN,
- Students should follow along the best they can. The lab will be recorded allowing students to return to the video and follow through the steps.

UMS GH15-1x Process and Device Model *

- Process Used: UMS GH15-11 (v2.3) 150 nm gate length AlGaN/GaN process
- Active Devices Used:
 - LNA = GH15LNF_NOFP & GH15NHF_NOFP; Linear noise model & non-linear model of transistor without field plate for low noise amplifier applications.
 - PA=GH15NHF: " non-linear transistor model for power amplifier applications
- The substrate technology used includes BCB



MSub
MSUB
MSUB_MET1
H=70 um
Er=10.42
Mur=1
Cond=2.5e7
Hu=3.9e+34 um
T=2 um
TanD=0.0015
Rough=0 um
FreqForEpsrTanD=2.1 GHz
LowFreqForTanD=2 GHz
HighFreqForTanD=8 GHz
Bbase=
Dpeaks=

GH15LNF noise capability validation domain	
Maturity level	Confirmed
Technology versions	All
Number of gate fingers	4, 6, 8 fingers
Unit gate width	20 µm to 50 µm
Frequency	6 GHz – 40 GHz
Drain voltage bias	5V to 20V
Drain current operating point	50 to 150 mA/mm
Temperature (SiC substrate)	25 °C

* Ref: UMS_GH15-1x_Design_manual_v3.0 - SP_30S_Electrical_Models_GH15-1x.pdf

Lab 1, Steps 1 & 2

Create Workspace and Review PDK

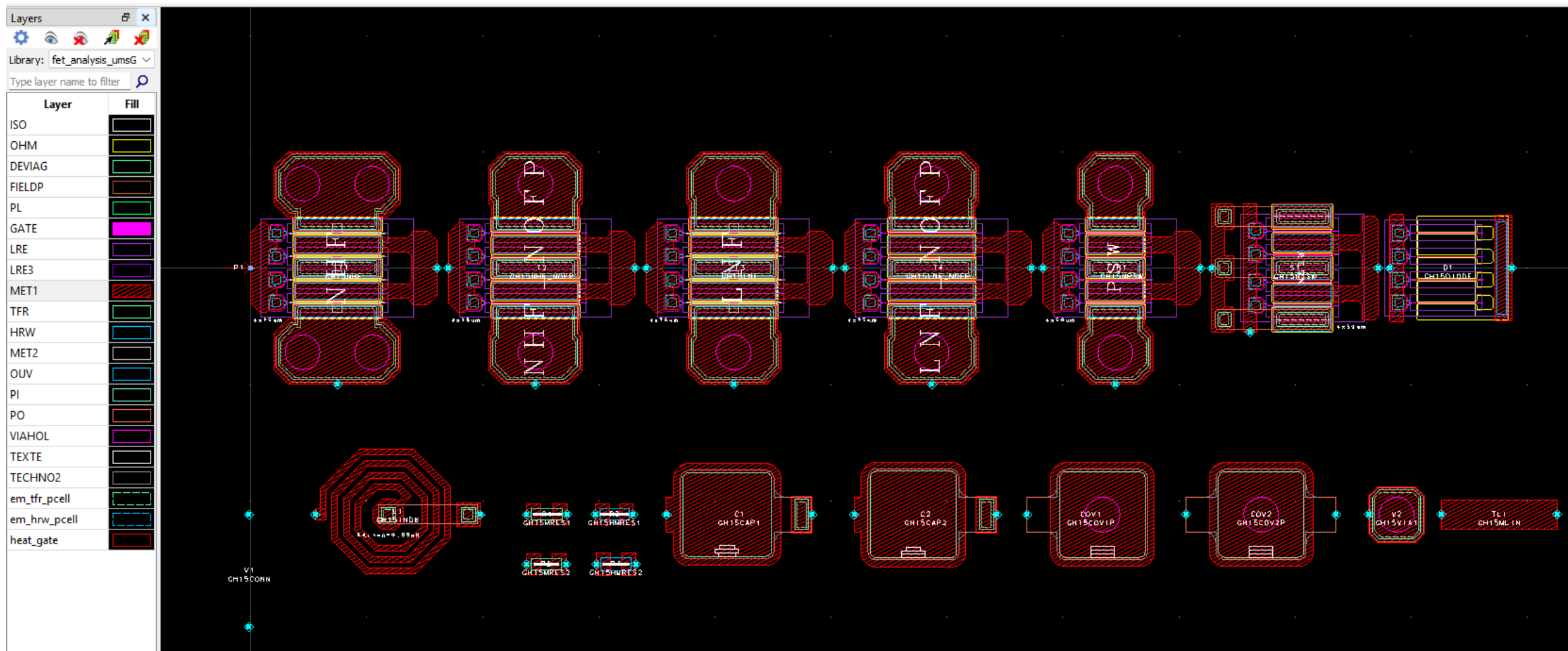
UMS PDK install, schematic, layout, 2-to-3D

Schematic View



UMS GH15-11 ADS Components

Layout View



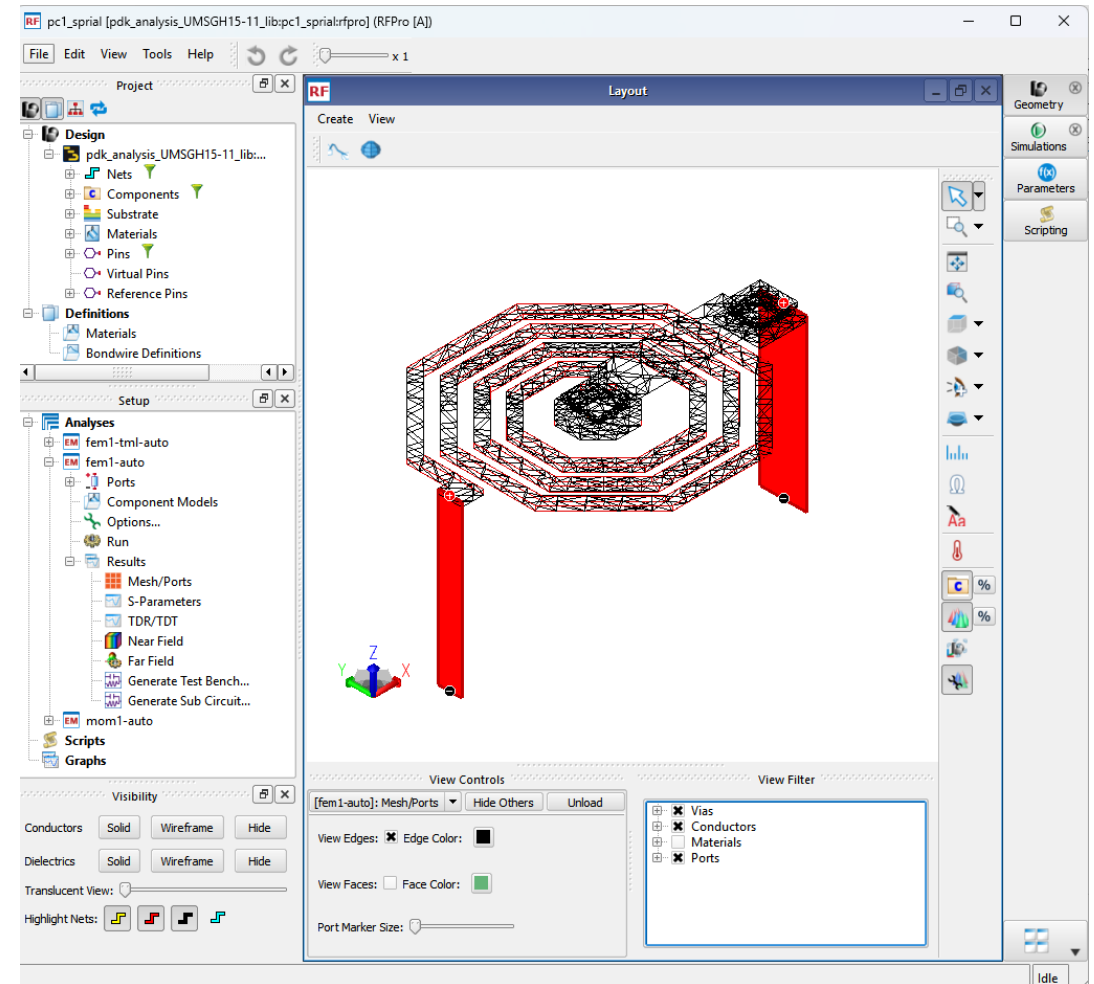
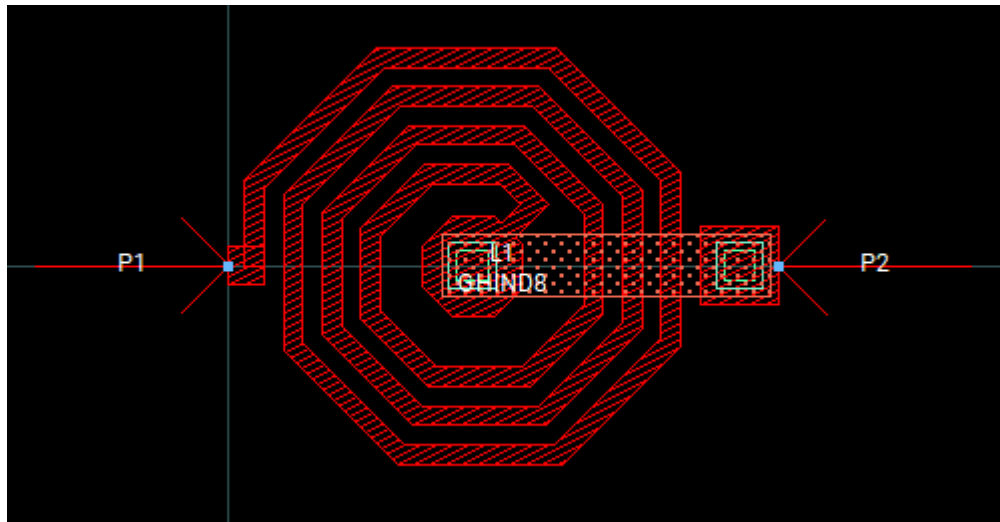
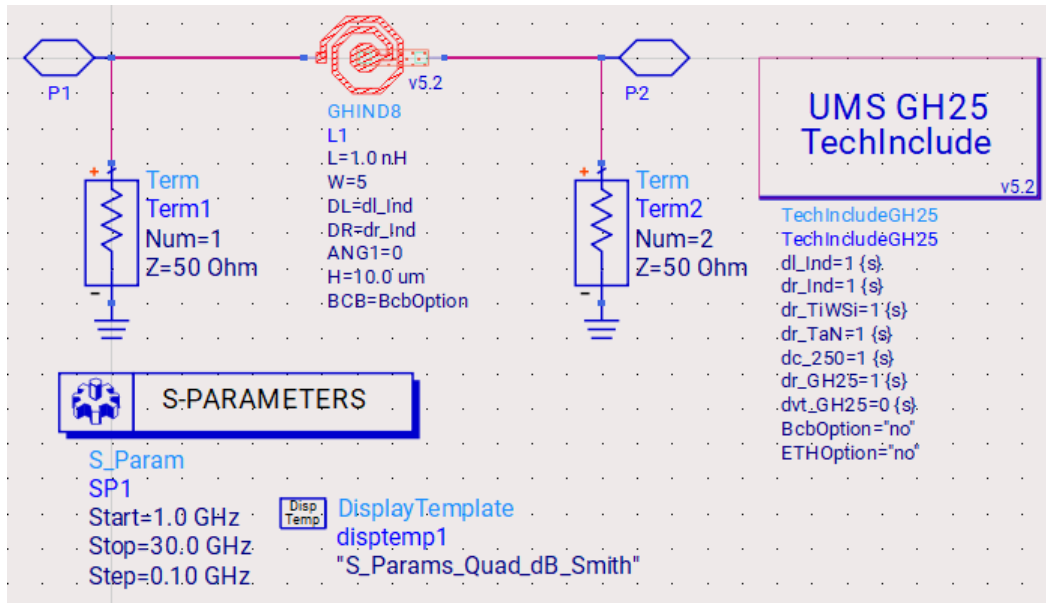
Lab 1, Steps 3a, b, c

Simulate Passive components

Simulate L, C, R, MLIN in Schematic and EM with RFPro

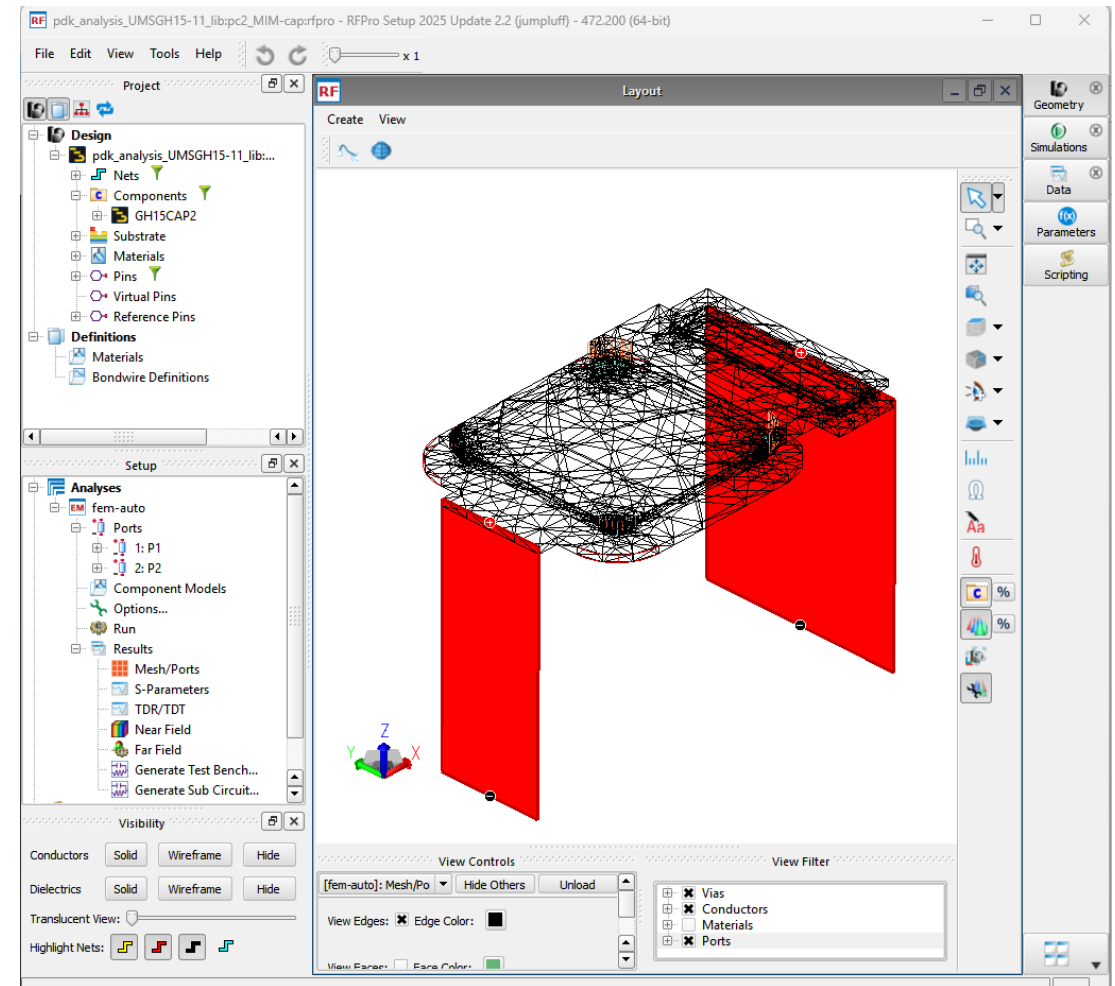
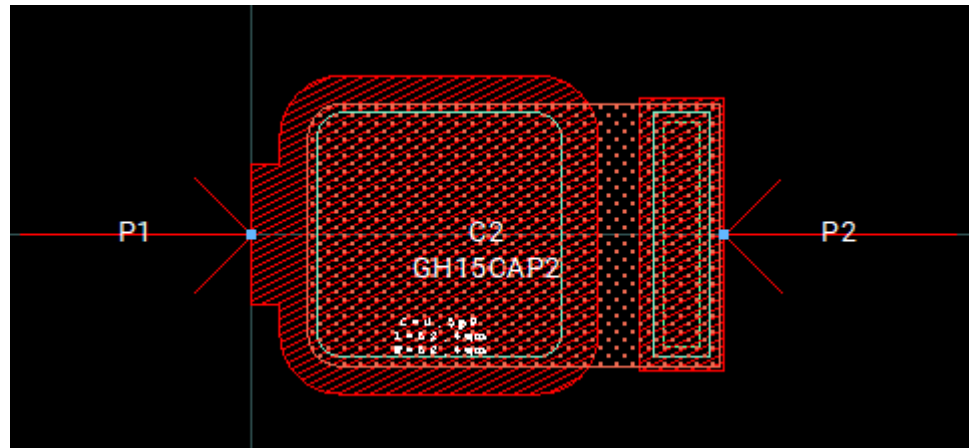
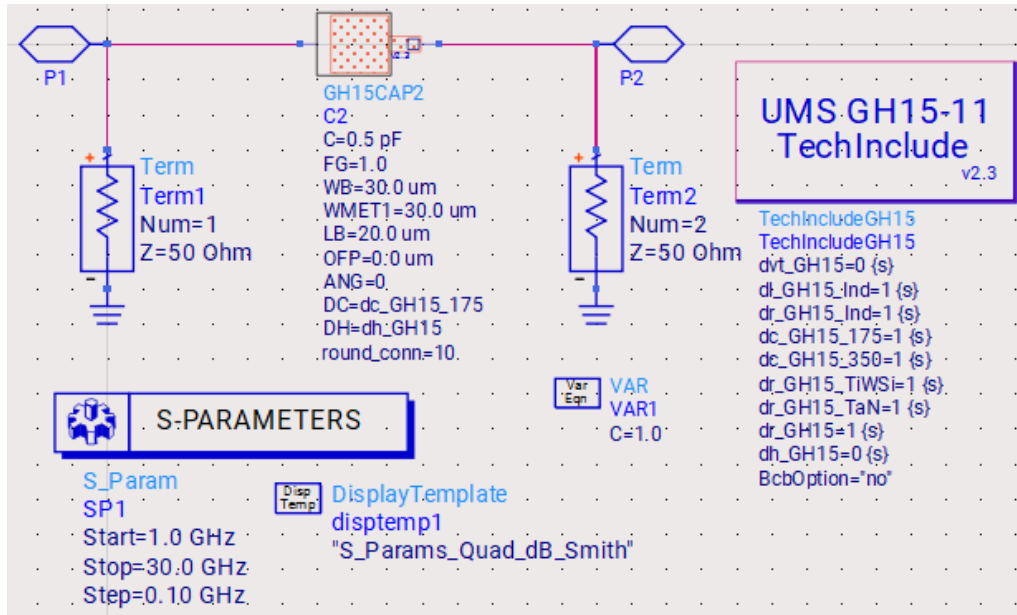
Spiral

Schematic and EM simulations



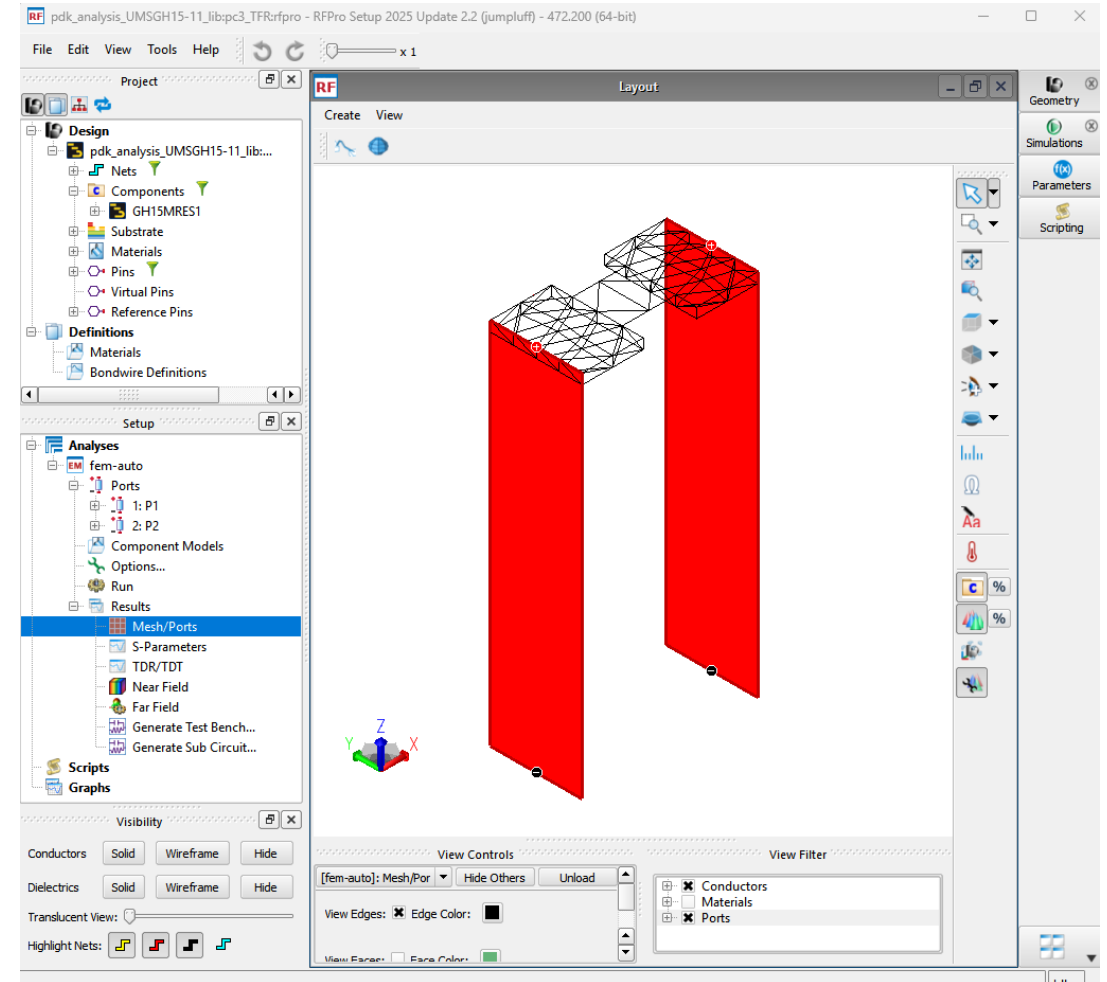
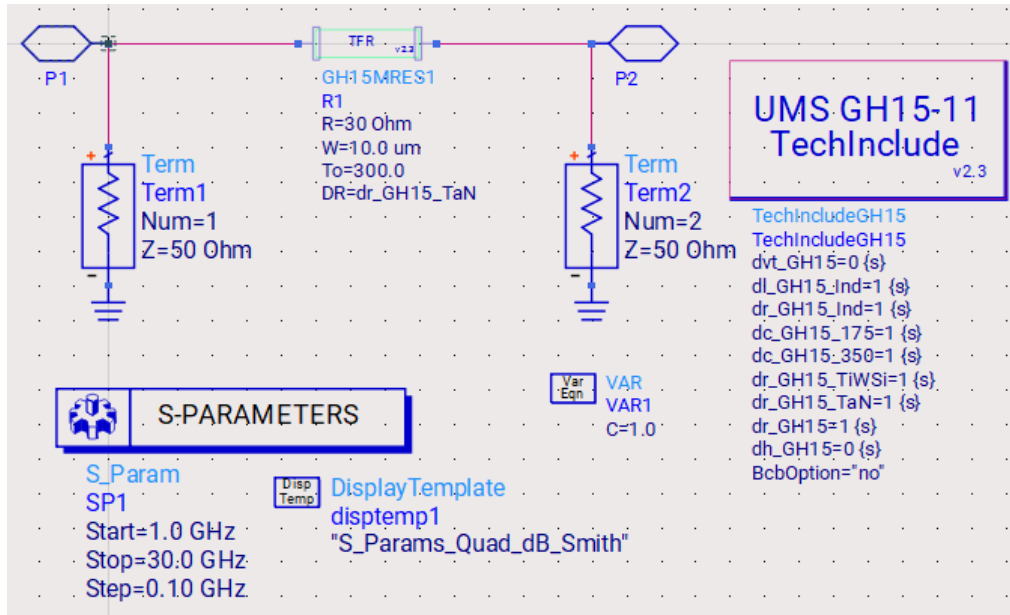
MIM Cap

Schematic and EM simulations



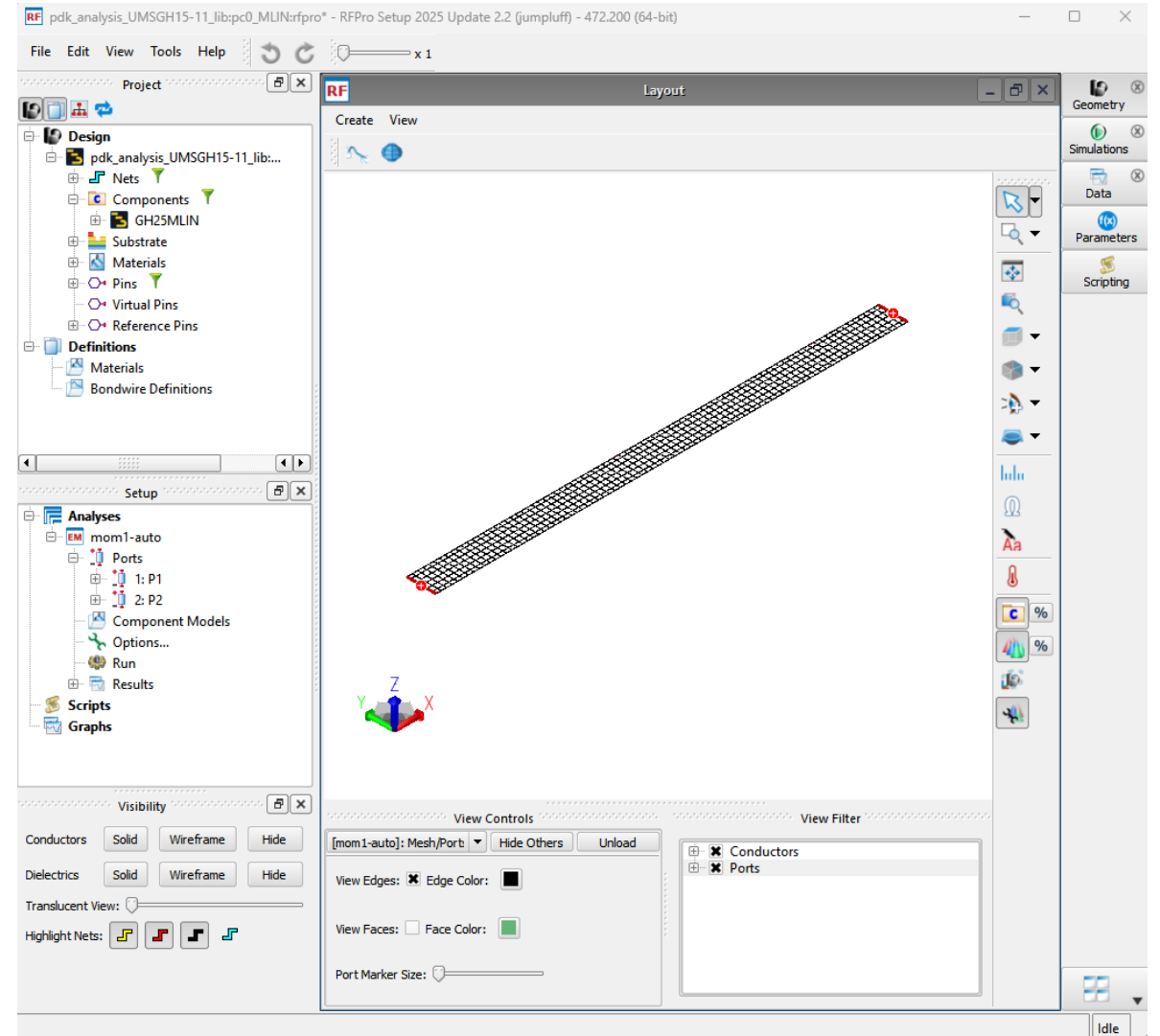
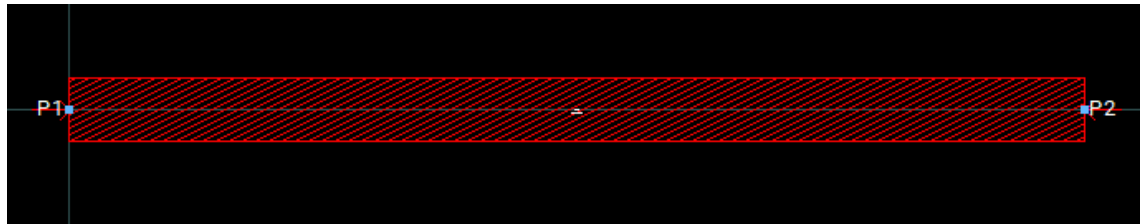
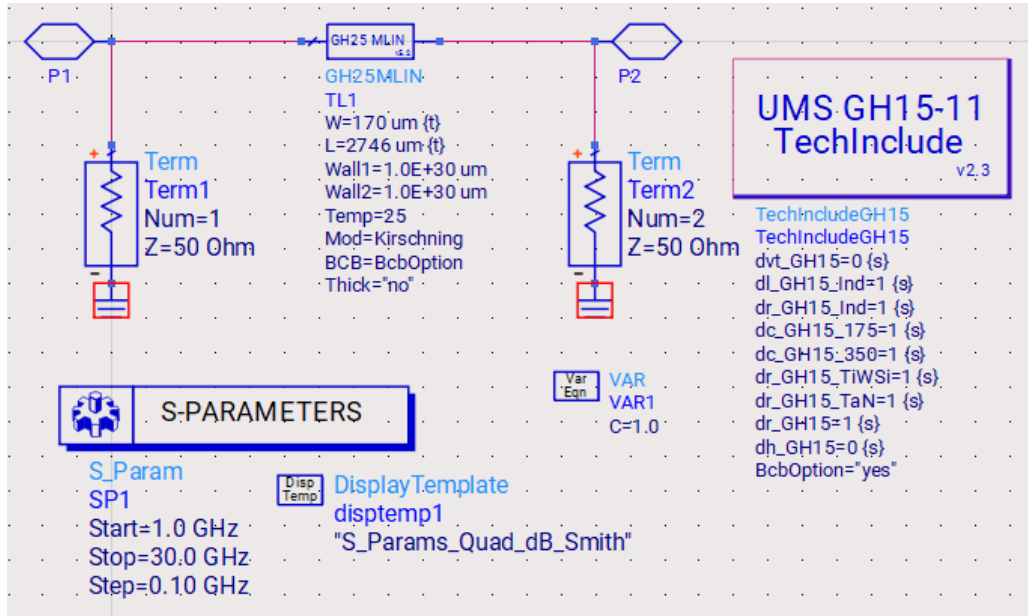
Thin Film Resistor

Schematic and EM simulations



Microstrip Transmission Line

Schematic and EM simulations



Line Calculator & Controlled Impedance Designer

Layout Substrate tool to calculate Line Impedances

LineCalc/untitled

File Simulation Options Help

Component

Type MLIN ID MLIN: MLIN_DEFAULT

Substrate Parameters

ID MSUB_DEFAULT

Er	10.2	N/A
Mur	1	N/A
H	70	um
Hu	3.9e+34	mil
T	2	um
Cond	570000000	N/A
TanD	0.001	N/A
Rough	0	mil
DielectricLossModel	1	N/A
FreqForEpsrTanD	1000000000	N/A
LowFreqForTanD	1000	N/A
HighFreqForTanD	1000000000000	N/A

Physical

W 61.42 um

L 2836 um

Synthesize Analyze

Electrical

Z0 50.718900 Ohm

E_Eff 87.691800 deg

Calculated Results

K_Eff = 6.63044

A_DB = 0.0346628

SkinDepth = 0.008299

Diagram: A 3D perspective view of a microstrip line on a substrate. The substrate has a thickness 'H'. The microstrip has a width 'W' and a length 'L'. The top surface of the substrate is labeled '1' and the bottom surface is labeled '2'.

Component Parameters

Freq 10 GHz

Wall1 0 mil

Wall2 0 mil

Values are consistent

cild_5 [UMS_GH15_11_tech] * (Controlled Impedance Line Designer)

File View Technology Options Help

Analyze Optimize Sweep Statistical

Variables

Name	Nominal
freq	10 GHz
Length	2836 um
Width	61.4183 um

Show: ☒ Line Type Vars ☐ Substrate Vars ☐ Material Vars

Electrical

TML Properties RLGC

	Real	Imag
Zc (ohm)	49.9986	-0.37901
Gamma (1/m)	4.24656	553.851
Attenuation (dB/um)	3.68851e-05	0
Attenuation (dB)	0.104606	0
Delay (ns/um)	8.81481e-06	0
Delay (ns)	0.0249988	0
Propagation Velocity (m/s)	1.13445e+08	0
Effective Dielectric Constant	6.9834	0
Effective Electrical Length (deg)	89.9957	0

Diagram: A cross-sectional view of a microstrip line. The layers are labeled from top to bottom: AIR, BCB (Thickness_1: 4.7 + 5 um), BCB (Thickness_2: 1 um), BCB (Thickness_3: 2 um), SIN2 (Thickness_4: 0.1925 um), SIN2 (Thickness_5: 0.1925 um), MET1/em_tfr_pcel/em_hrw_pcel/em_tfr/em_hrw (Thickness_6: 0.025 + 2 um), SIN1 (Thickness_7: 0.375 um), and SIC2 (Thickness_8: 70 um). The substrate is labeled "0 micron".

Substrate UMS_GH15_11_tech:UMS_GH15_11_with_BCB

Type Microstrip Single-Ended

Top plane <None>

Signal MET1