CAL POLY
SAN LUIS OBISPO

EE 531: ADVANCED VLSI DESIGN

Packaging

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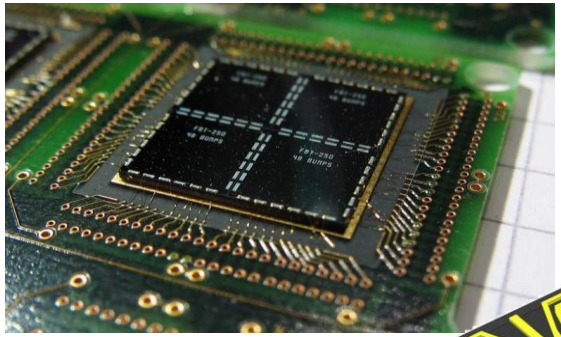
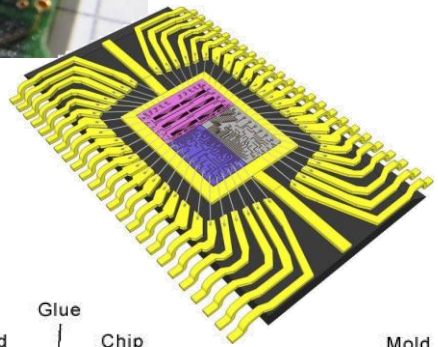
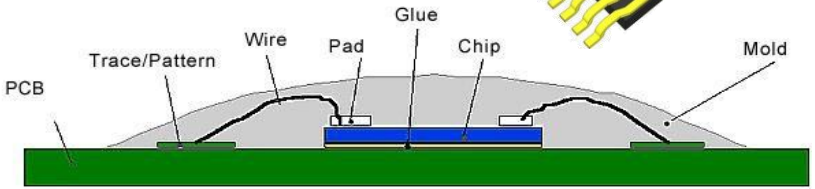
HOW DO WE GET OUTSIDE THE CHIP?

- It's actually a pretty long road…
  - I/O Circuits
  - Bonding
  - Package
  - Board
- Once we get out of the chip
  - Long wires mean a lot of delay, capacitance, inductance.
  - We can use fat wires for low resistance.
  - But we have a lot more room to play around.
- The interface between the chip and the outer world is the IC package.

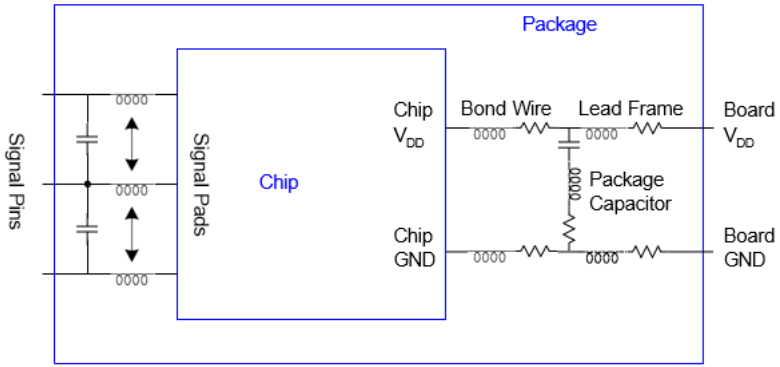






MAIN PROPERTIES OF PACKAGE

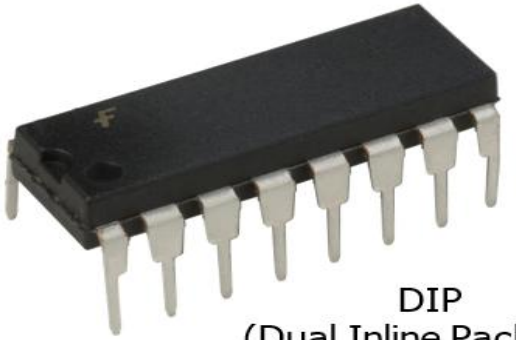
- The package provides the physical, temperature and electrical protection.
  - Electrical connection from chip to board
  - Physical connection from chip to board
  - Protection from high voltages (outside)
  - Physical protection
  - Thermo isolation



MAIN PROPERTIES OF PACKAGE

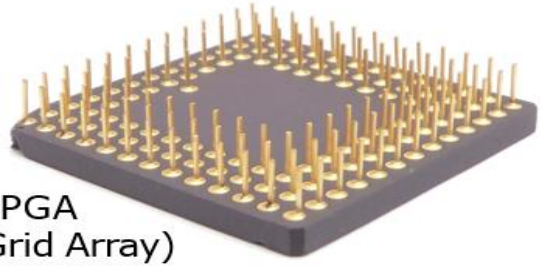
- Requirements of a package are:
  - Electrical: Capacitance, Resistance, Inductance, Impedance Tuning
  - Interface: A large number of I/O pins
  - Mechanical: Die/Bond protection, Compatibility with PCB
  - Thermal: Heat Removal
  - Cost: As low cost as possible (without fan, heat sink, etc.)

PACKAGE TO BOARD CONNECTION

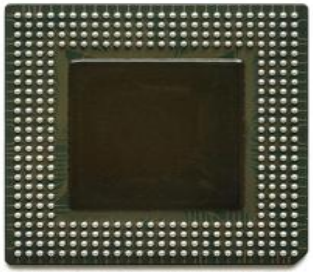


DIP
(Dual Inline Package)

QFP
(Quad Flat Package)



PGA
(Pin Grid Array)

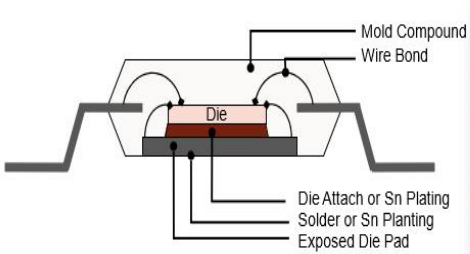


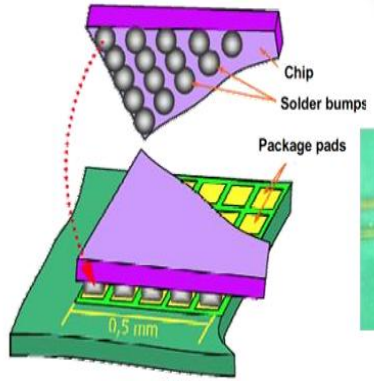
BGA (Ball Grid Array)

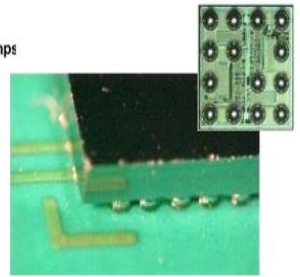
IC TO PACKAGE CONNECTION

Two main approaches:

- Wire bonding
  - All pads are around chip edges (~100um pitch).
  - Slow, serial bonding process.
  - Long, high RLC wires (~5nH, 1pF per wire).
- Flip Chip
  - Pads on top of IC core.
  - High pin count.
  - Short, low RLC bonds (0.1nH)
  - Fast parallel bonding process.
  - But… Expensive!





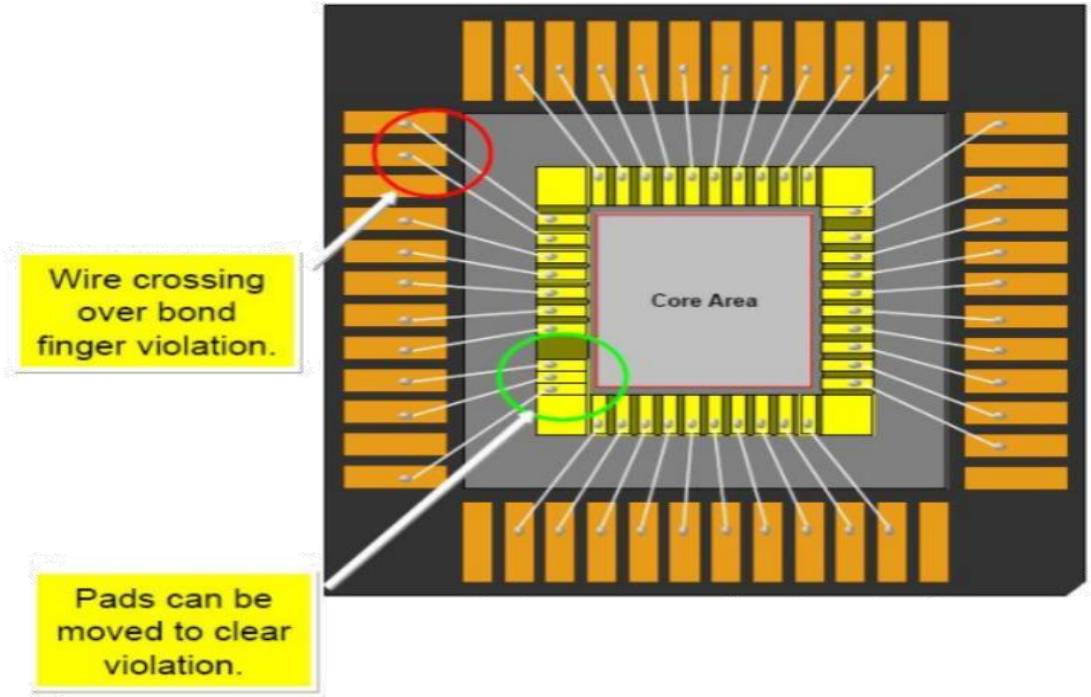


Controlled Collapse Chip Connection, C4

SOME BOND WIRE REQUIREMENTS

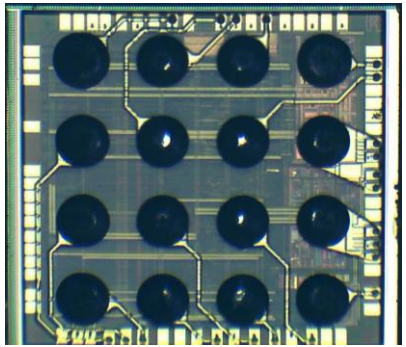
When designing a wire bond package, you need to pay attention to:

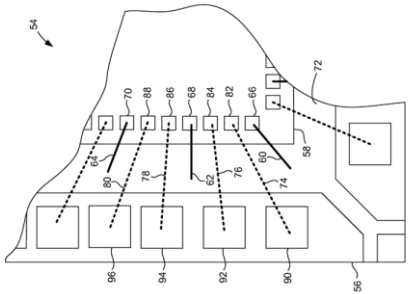
- No crossing of bond wires
- Minimum spacing
- Maximum angle of wires
- Maximum length of wires

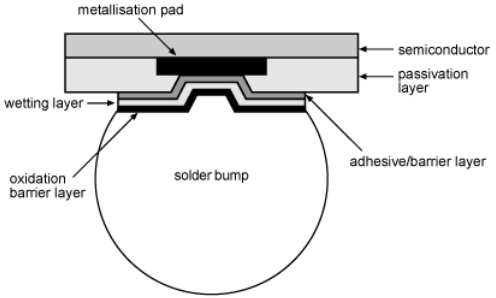


SO HOW DO WE INTERFACE TO THE PACKAGE?

- We need to create a physical connection to the bonding wire.
- For wire bond packaging:
  - Use a landing pad.
  - Basically a big (100µm X 100µm) piece of metal.
  - Many stacking layers for physical robustness.
- For flip chip packaging:
  - Use solder bumps.
  - Route to bumps with Redistribution Layer (RDL)







BUT WHAT CONNECTS TO THE BONDING PADS?

- I/O Circuits!
- Requirements of I/O Circuits:
  - Availability to drive big loads
    - Due to package and transmission lines
  - Voltage Consistency
    - Due to different supply voltages on the board
  - Low switching noise
    - Due to package and transmission line inductance
  - ESD protection
    - Due to high potential difference of external devices

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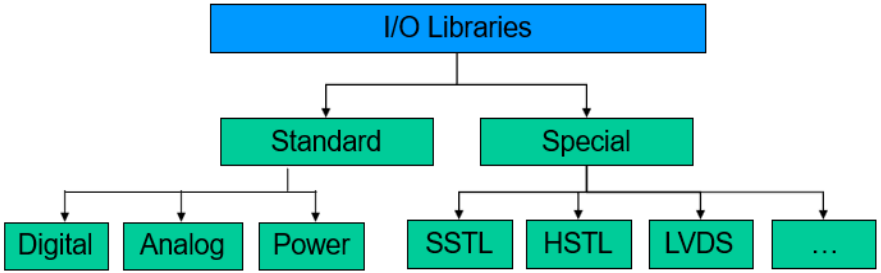
Goals of I/O Design:

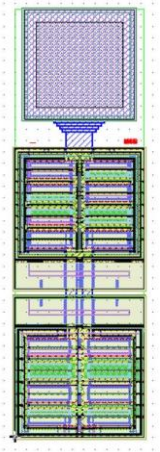
- Reduce delay to and from outside world (PCB)
- High drive current capability
- Match impedance to load
- ESD Protection
- Level shifting of voltages (i.e.1.2V inside/3.3V outside)
- Meet specifications of Interfaces
- Reduce power (short circuit current through output buffers)
- High voltage tolerance

TYPES OF I/O CELLS

There are several types of basic I/O cells:

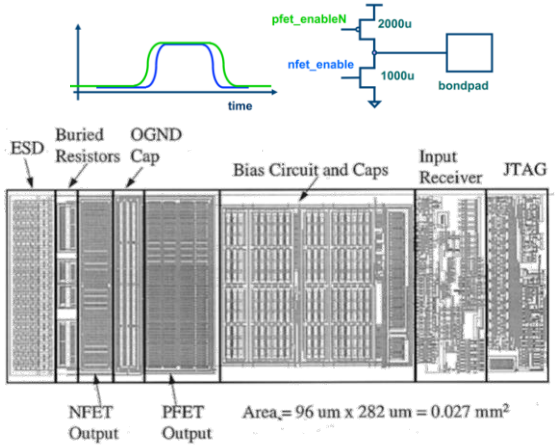
- Digital I/O Buffers
  - Provide high drive up-level shifting output
  - Provide down-level shifting and ESD protection for inputs
- Analog I/O Cells
  - Provide ESD protected analog inputs/outputs
- Power supplies
  - Provide power to the I/O and Core supplies
  - Provide the basis for ESD protection

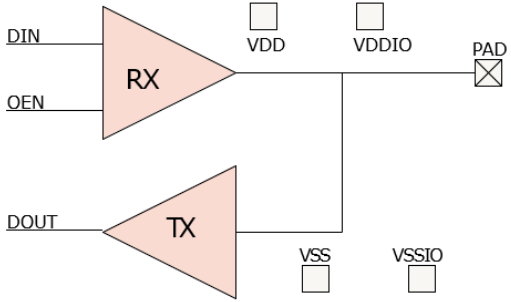


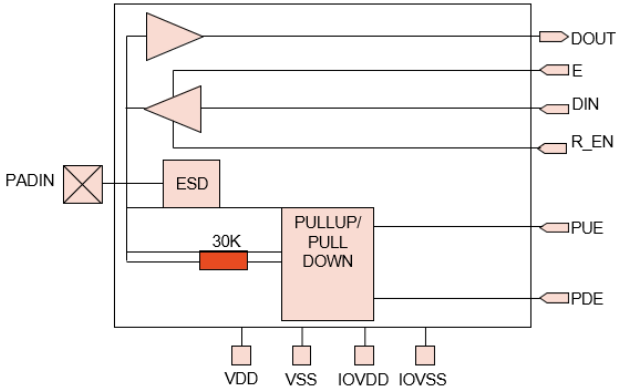


DIGITAL I/O BUFFER

- Digital I/O
  - Output buffer needs to drive pF, not fF
  - Requires increasing fanout inverter chain
  - Short circuit current is unacceptable!

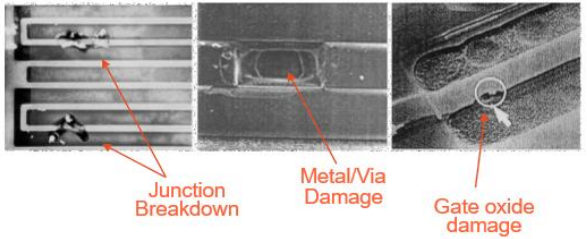


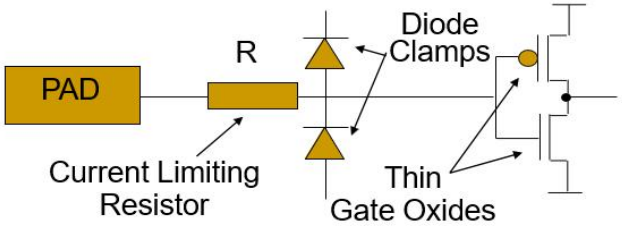


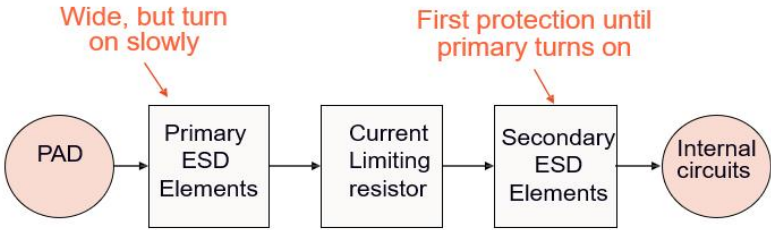


ESD PROTECTION

- Electrostatic discharge (ESD)
  - One of the most important reliability problems in the IC industry.
  - ESD protection circuits divert high currents away from the internal circuitry and clamp high voltages during an ESD stress.
- Diode clamps
  - Diodes turn on if pad voltage:
    - Exceeds VDD +0.7V
    - Drops below VDD -0.7V
  - Formation:
    - P+ diffusion in n-well
    - N+ diffusion in p-substrate

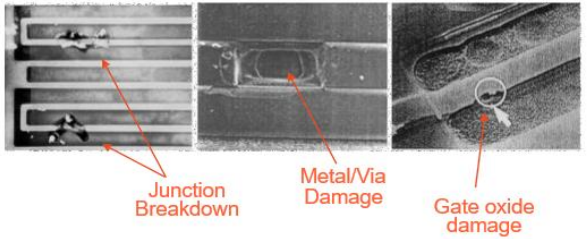


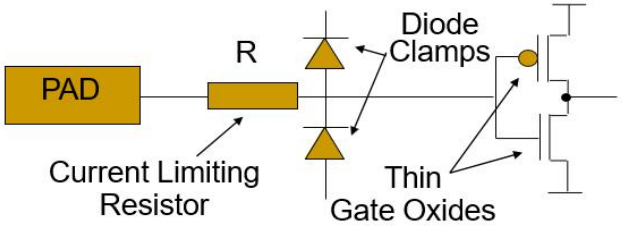


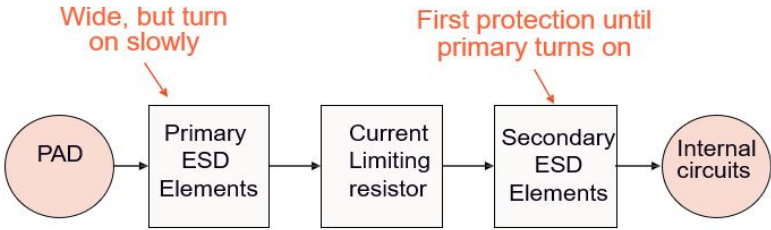


ESD PROTECTION

- Electrostatic discharge (ESD)
  - One of the most important reliability problems in the IC industry.
  - ESD protection circuits divert high currents away from the internal circuitry and clamp high voltages during an ESD stress.
- Resistor
  - Limits the current
  - Protects secondary protection
  - Formation:
    - Diffusion
    - Polysilicon

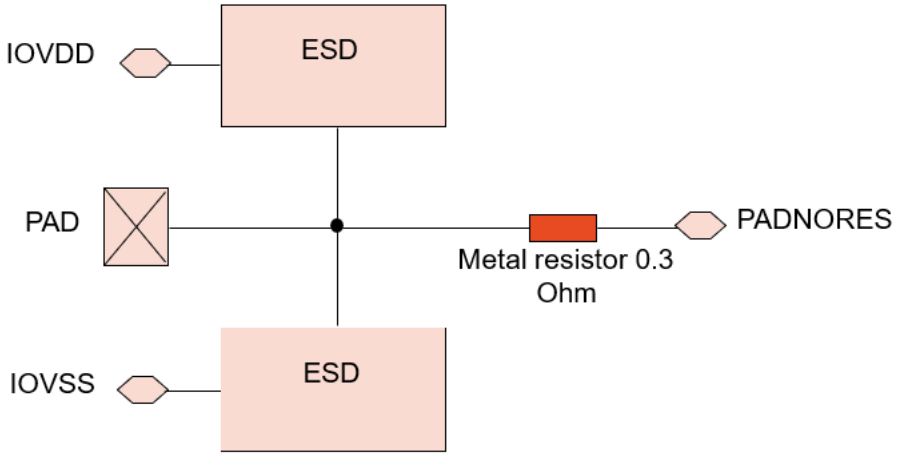






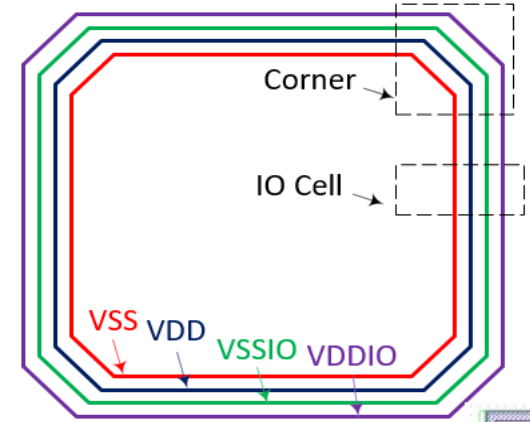
ANALOG I/O CELL

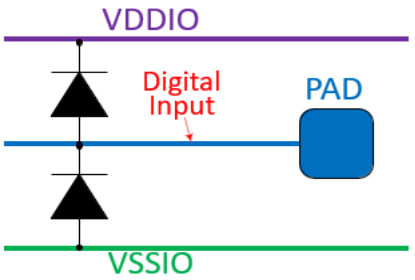
- Analog I/O
  - Used for passing “analog” signals to/from the chip.
  - Basically, “a wire”, but should have some degree of ESD protection.

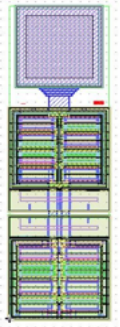


POWER SUPPLY CELLS AND ESD PROTECTION

- Power supply cells are analog cells (i.e., just a wire).
- But these cells supply the I/O rings for:
  - Power distribution
  - ESD Protection
- Generally, digital (core) and I/O power/ground supplies are separate:
  - I/Os sink a lot of current → Power supply noise
  - I/Os usually run at a higher voltage level (i.e., 2.5V vs. 1.2V)
  - All (four) types of supplies connect to rings under the I/O circuits.

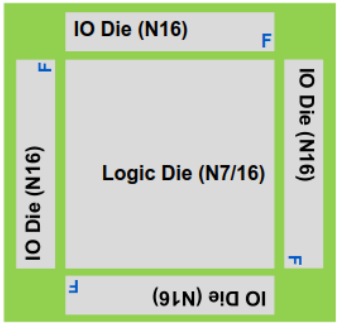


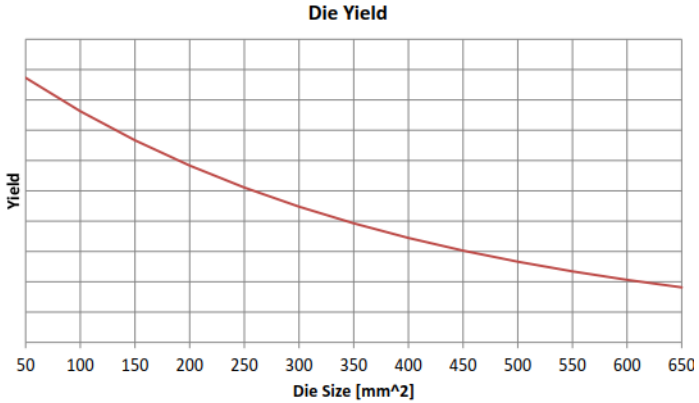




SYSTEM IN PACKAGE (SIP)

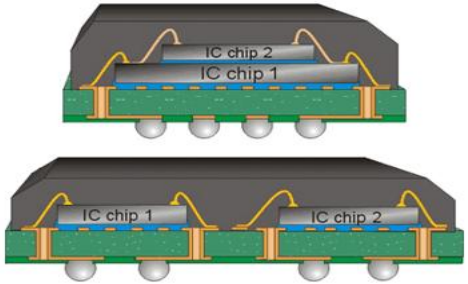
- SoC – System-on-Chip
  - Integration of several IPs on a single silicon substrate.
- SiP – System-in-Package
  - Integration of several silicon devices (chips) in a single package.
- Why SiP?
  - ➢ Smaller chips → Improved yield
  - ➢ Mix several process nodes
    - i.e., 7nm for high speed logic, 45nm for analog.
  - ➢ Close integration with non-CMOS device
    - Flash
    - Silicon Photonics
    - SiGe
    - High Bandwidth Memory (HBM DRAM)



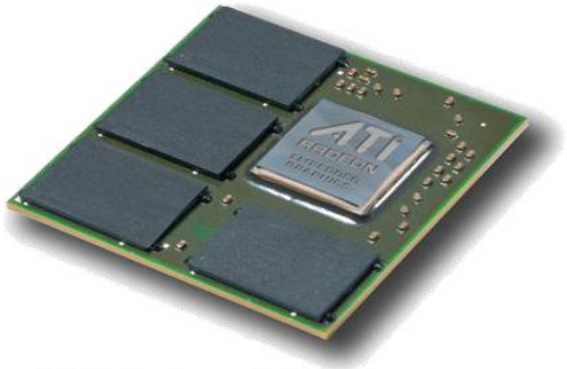


MCM – MULTI CHIP MODULE

- Assembly of several silicon devices on Organic Substrate (PCB)
  - Very mature technology
  - Routing pitch ~30um
  - Bump Pitch > 160um



Source: PC Magazine



AMD Radeon E4690:
GPU + DRAM in MCM

Source: AnandTech

Thank you!