EE271 – Introduction to VLSI Systems

Final Examination

December 10, 2008

Name: _____

(Please Print)

SCPD Student: Yes / No

You may not collaborate in any manner on this exam. This exam is closed notes, closed book, except that you are permitted two sheets (four sides) of notes. You have 180 minutes to complete the exam. Please do all of your work on the exam itself. Attach any additional pages as necessary. Before starting, please check to make sure that you have all 16 pages including the cover page.

No:	Total Points	Score
1.	15	____
2.	10	____
3.	10	____
4.	15	____
5.	12	____
6.	15	____

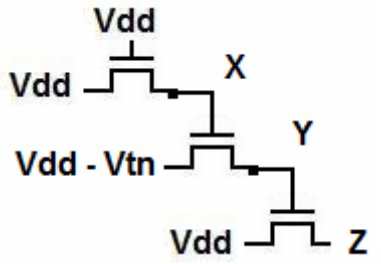
Total: _____ / 77

In recognition of and in the spirit of the Stanford University Honor Code, I certify that I will neither give nor receive unpermitted aid on this examination.

Signature: _____

Question 1: Short Questions (15 points)

a) (6 points) In the figure below, state the voltages at node x, y and z. The threshold voltage of all the three transistors is Vtn. Initial voltage at X, Y and Z is 0V.

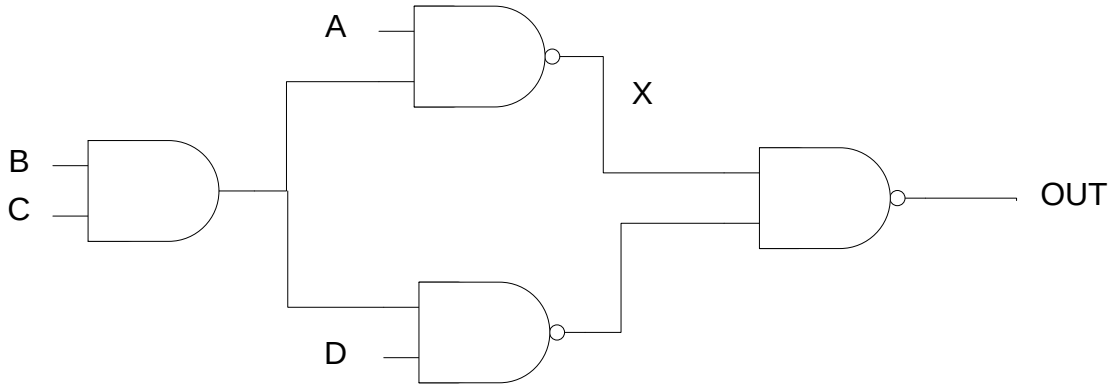


X = Vdd – Vtn

Y = Vdd – 2Vtn

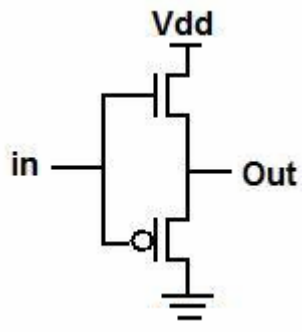
Z = Vdd – 3Vtn

b) (4 points) For the circuit below, give all the test patterns that test for SA-1 fault at node X.

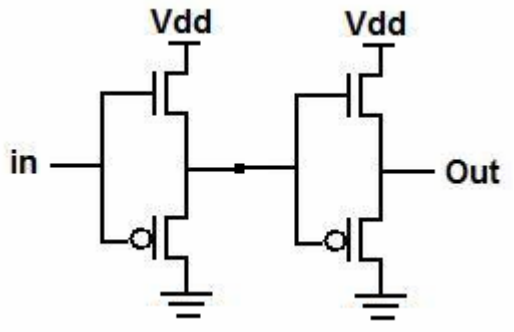


ABCD: 1110

c) (5 points) Draw the voltage transfer characteristic of the circuit in (ii). The voltage transfer characteristic of the circuit in (i) is given for your reference. Assume |Vtn|=|Vtp|= 0.25Vdd and 'Out' is initially at 0V.



(i)



(ii)

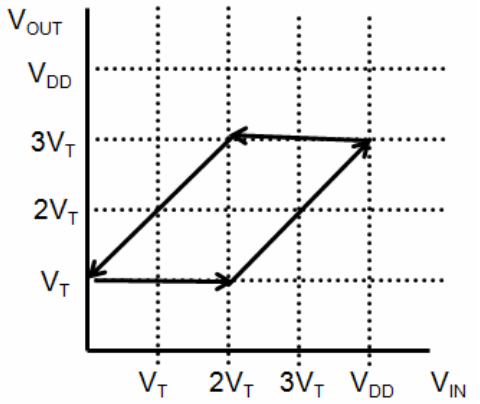
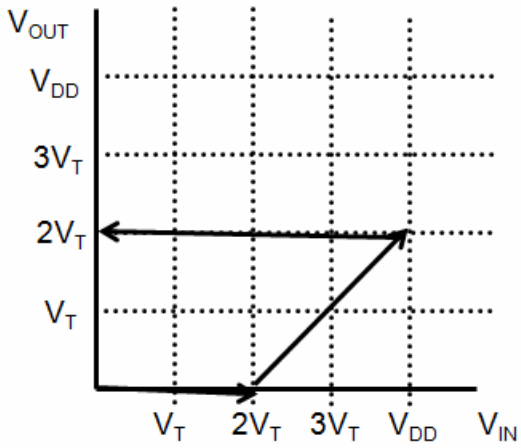
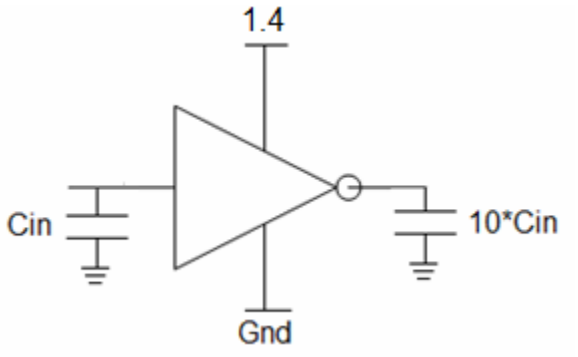


Figure: Voltage Transfer Characteristic of the circuit in (i)

Answer:



Question 2: Logical Effort (10 points)



In class, we found out the resistances of the transistors using the formula, R= Rsq. L/W. Suppose now, we model the resistance in the following way, R = 80*(L/W)*(Vdd) / (Vdd – Vt)^2.

Assume the following for this problem.

- Nominal Vdd = 1.2V, Nominal |Vtn| = |Vtp| = 0.5V
- The pull up and pull down network resistances are equal.
- The reference inverter used to calculate LE is an inverter gate (of W/L =2) at NOMINAL Vdd and NOMINAL Vt.
- The inverter in the figure is sized, W/L = 2.
- The inverter in the figure uses a 1.4V power supply.
- The total fanout(CL/Cin) of this chain is 10.
- The threshold voltage is constant (at nominal Vt) and is not bias dependent.

a) (5 points) Give the logical effort of the inverter.

LE = R(inverter) / R(reference inverter) (Capacitance is the same so it cancels out)

= (1.4 / (1.4 – 0.5) ^2) / (1.2 / (1.2 – 0.5) ^2

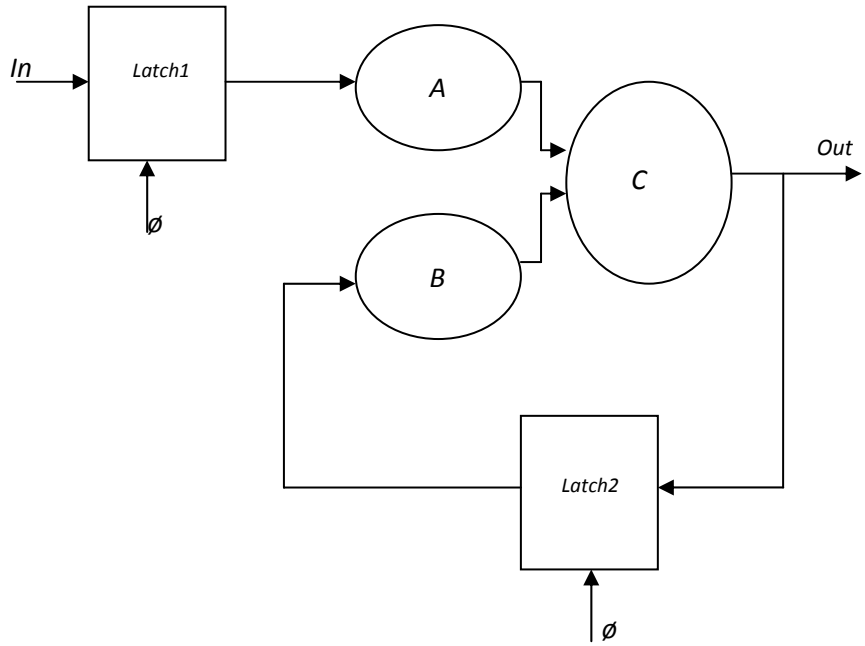
= 0.71

b) (5 points) Suppose now we have the flexibility of choosing a power supply voltage anywhere between 0.8V and 2V. What is the most optimal power supply voltage (between 0.8V and 2V) you would choose so as to minimize the energy delay product.

Note: The energy delay product is given by RC * ½ CV^2. Neglect leakage power. (Hint : Think of differentiating something)

- First substitute the value of R in the energy delay product and differentiate it.
- Equate the differentiation to zero and solve for V
- Differentiation gives, $2V^3(V - 0.5) - 3V^2(V - 0.5) = 0$
- Solving for V gives V = 1.5 V

Question 3: Timing (10 points)



Consider the simple state machine shown above. A, B and C represent combinational logic blocks with the following properties:

t_{cd}(A) = 200ps; t_{pd}(A) = 1ns;

t_{cd}(B) = 300ps; t_{pd}(B) = 2ns;

t_{cd}(C) = 100ps; t_{pd}(C) = 0.5ns;

Both the latches (they are latches, not flip-flops) are clocked by the same clock ø and have equal ***setup time of 150ps*** and $t_{d\text{-}q}$ ***delay of 250ps***. The clock to output delay $t_{clk\text{-}q}$ ***is 100ps*** and t_{hold} ***is 100ps*** for both the latches. The clock ø has a period T_{clk} and is high for a duration of T_{on} i.e. the duty cycle of the clock is T_{on}/T_{clk}

a) (4 points) Determine range of T_{on} necessary to avoid hold time violations.

$$t_{cd} \geq t_{hold} - t_{ccq} + t_{pw}$$

$$200 + 100 \geq 100 - 100 + t_{pw}$$

$$t_{pw} \leq 300ps$$

b) (6 points) For this part, let's assume T_{on} = ***200ps***. Determine the absolute minimum clock period for the circuit to work correctly.

$$t_{pd} \leq T_c - t_{pdq}$$

$$2.5 \leq T_c - 0.25$$

$$T_{cmin} = 2.75\,ns$$

Question 4: Timing Analysis and Optimization (15 points)

In this problem we will look at one of the optimization techniques for improving the clock period (usually performed by synthesis tools) called register retiming.

a) (5 Points) First verify that the two circuits shown below have the same functionality (suppose clock period is long enough so that no timing violations happen). Briefly explain why such transformation can help improve clock speed. *(This is called retiming technique and can be used to increase the clock speeds during synthesis)*

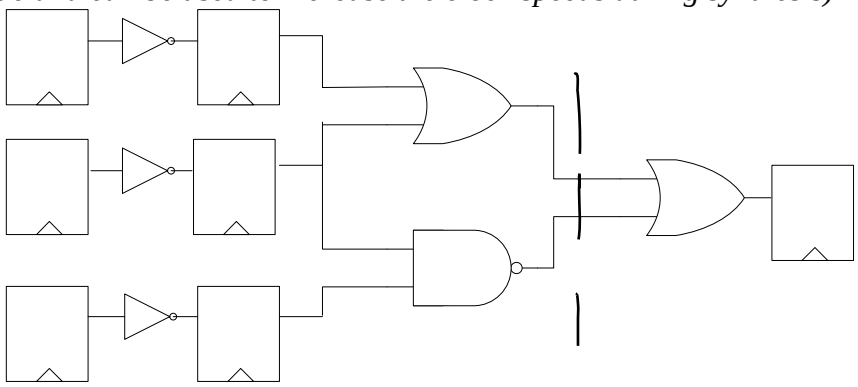


Fig (a)

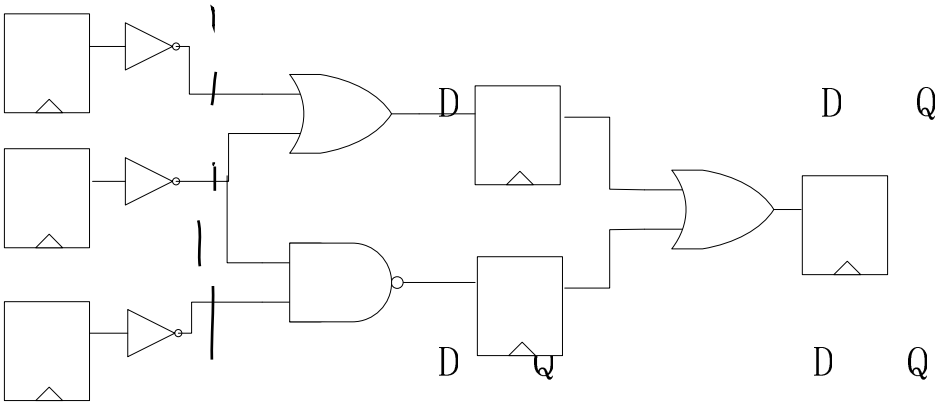


Fig (b)

D Q D Q

D Q

3 lvls of flops, clean graph cut between orig + retimed so all data stays together

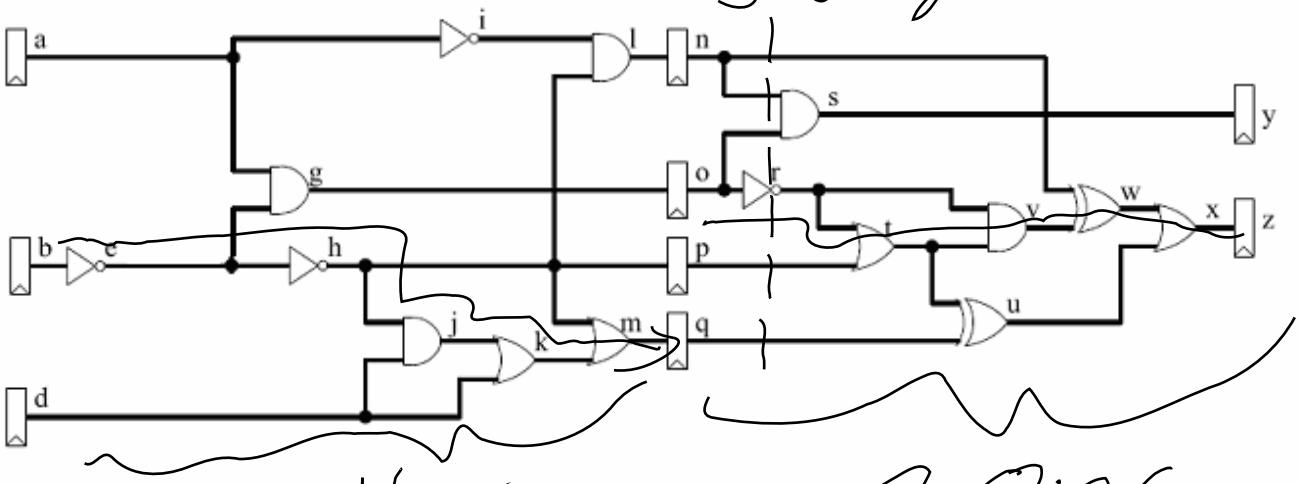
The rest of the question is concerned with the timing analysis and optimization of the circuit below.

Delay and Timing Parameters

INV	2ns
AND	4ns
OR	4ns
XOR	6ns

Setup	2ns
Hold	1ns
Clk-q	3ns

move flops here



16ns 20ns

b) (5 points) What is the critical path in the circuit, and what is the minimum clock period at which the circuit will operate correctly? You do not have to perform a full STA using graphs, as long as you are sure the path you found is actually the most critical one.

$t_{crit} = 20ns$, $T_{clk} = 20+3+2$

$= 25ns$

c) (5 points) Using the retiming technique introduced in part a), describe a small change that you can make to the circuit in order to shorten its critical path (and increase clock speed). Describe any tradeoffs related to this change.

move flops to dashed line on diagram. costs 2 extra flops & saves 2 ns on tcyc.

Question 5: Clock Gating (12 points)

a) (4 points) Prove within 5 lines that the two flip-flops F1 and F2 (only consider the parts inside the boxes) shown below behave the same way.

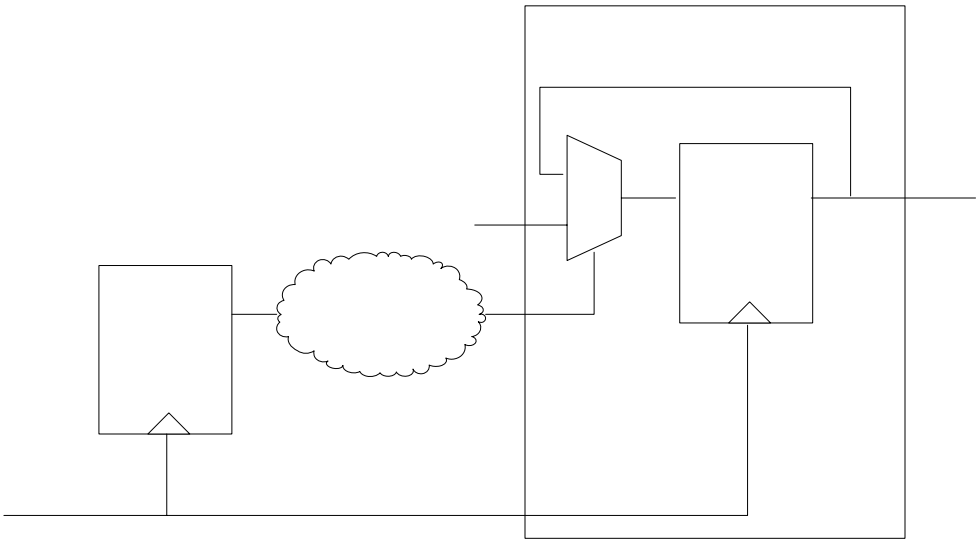


Fig (a)

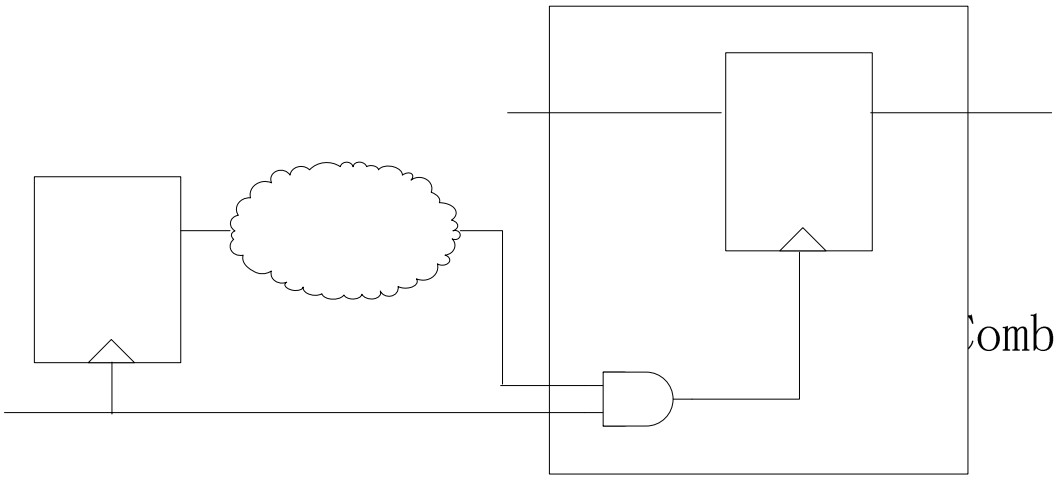


Fig (b)

Divide the discussion into two cases. EN is low, … EN is high, …All reasonable interpretations get full points.

CLK

b) (8 points) The flip-flop F2 is called a clock-gated flip-flop. In practice, an additional latch (as shown below in F3) is often added when implementing such flip-flops. Can you explain the function of this latch? (Hint: draw waveforms of DIN, COUT, EN and CLK signals for both clock-gated flip-flops. Find out cases when they perform differently.)

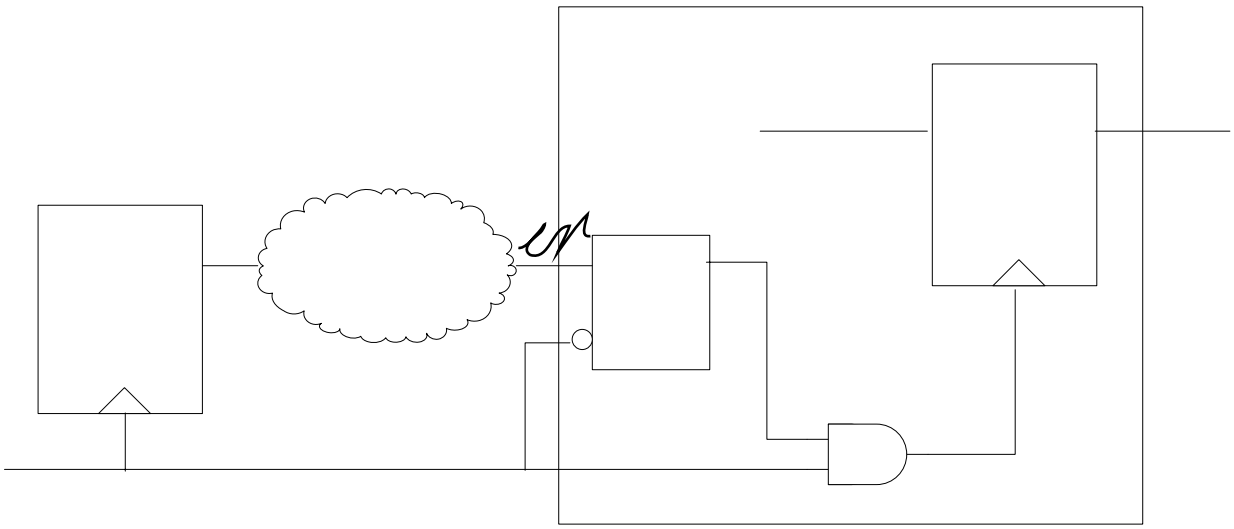
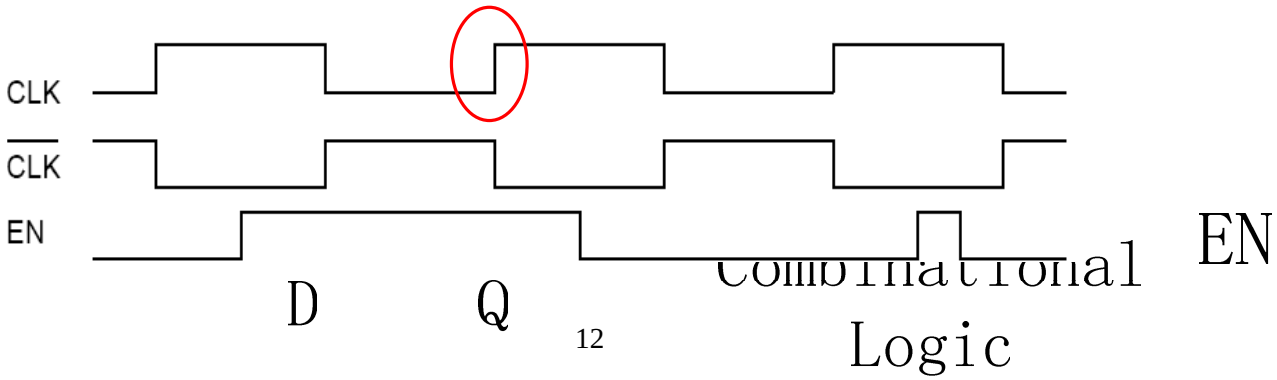


Fig (c)

The major problem of Fig (b) architecture is undesirable glitches. Consider the input waveforms below. Only one rising edge (circled in red) is intended to be enabled by EN, but you should figure out that architecture (b) results in two undesirable clock glitches. Architecture (c) avoid this problem.



c) (**Optional: Only considered for borderline cases**) How would you incorporate testability into the clock gated flip-flop F3 so that all stuck-at faults can be detected? Note that the combinational logic that generates the EN signal needs to be tested as well.

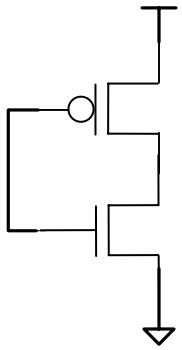
Several issues need to be considered.

1. Make the original flip-flop scannable.
2. Make sure we can overpower the EN signal in controlling the clock to the flip-flop. Because otherwise EN may disable the flip-flop and break the scan chain.
3. Make sure the output of the combinational “cloud” is testable, which is currently not.

There may be a few ways to fix each of these problems.

Question 6: Skewed Gates (15 points)

Sometimes, people intentionally "skew" logic gates so that one type of transition is faster than the other. For example, the following inverter favors falling transition at the output against rising transition.



a) (4 points) What is the logical effort (LE) of the above inverter (with respect to a normal un-skewed inverter where PMOS is twice as wide as NMOS)? You need to solve LE for both rising and falling transitions (at the output) for this part.

LE (rising) = 4/3

LE (falling) = 2/3

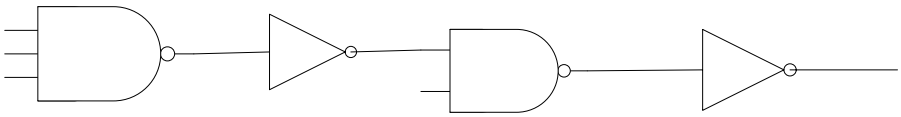
b) (5 points) Following this idea, design skewed inverters, 2 input NAND gates, and 3 input NAND gates, where one type of transition is twice as fast as the other type. There should be a total of 3*2 = 6 possible combinations; since we already covered one of them in part (a), you only need to find the rest five of them. Find the logical efforts of ONLY the fast edge of transition for these gates.

	NMOS	PMOS	LE
Inverter (rising)	1	4	5/6
NAND2 (rising)	1	2	1
NAND2 (falling)	2	1	1

NAND3 (rising)	3	4	7/6
NAND3 (falling)	3	1	4/3

c) (6 points) For this part of the question, you will design a decoder using the skewed logic gates which you just designed. The decoder takes 6 address bits and gives 64 outputs as select signals. The load presented at each output node is 40fF. You are given each address and its complement (i.e. A and ~A), each can drive 5fF. The decoder structure will be structured such that the pre-decoder combines three of address lines each time and the final stage combines the output of pairs of pre-decoder stages (Note that this structure is slightly different from the one we used in Homework 3!).

Below shows one of the paths for this decoder. For simplicity, we will neglect the wire load between the pre-decoder and final decoder stage (not shown on the plot) and ALL parasitic capacitances.



The goal of our decoder is to make the <u>rising edge of the decoder outputs</u> as fast as possible. Out of the 6 logic gates you designed in part b), which ones would you choose for each of the four gates shown above? Calculate the total path effort from the input to the output given your choice of gates. Remember that you need to take into account branch efforts.

NAND3-F, INV-R, NAND2-F, INV-R

Total BE = 32. (BE0 = 4 before the first stage, BE2 = 8, finding these BE's counts for 2 out of the 6 points in the second part).

Total path effort = (4/3 * 5/6 * 1 * 5/6) * (40 / 5) * 32

= 237