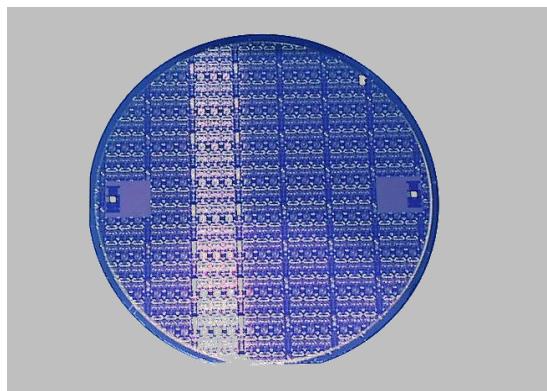


Foundry Process Data Sheet



BES

Schottky Diode

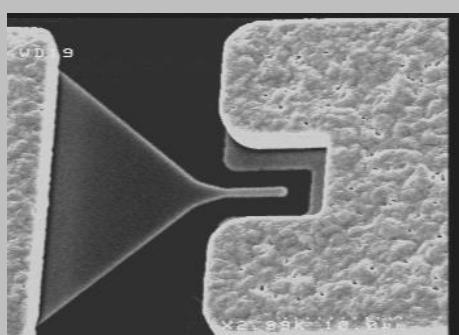
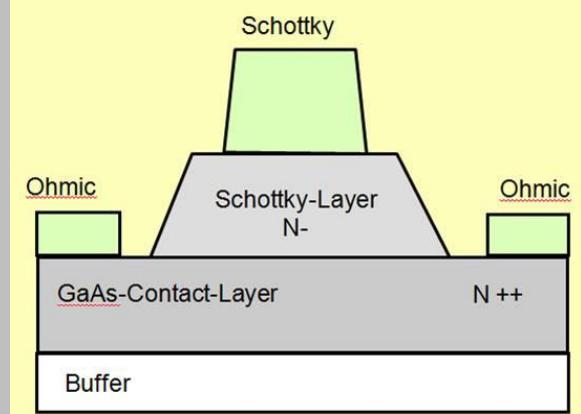


Description

The 1 μm Schottky diode process is optimized for very high frequency mixers or switches up to several hundred of GHz. The process includes two metal interconnect layers, precision TaN resistors, high values TiWSi resistors, MIM capacitors, air-bridges and via-holes through the substrate.

Main Features

- 1.0 μm Schottky diode
- Fully optical process
- Typical F_t : 3THz
- TaN and TiWSi resistors
- GaAs resistors
- M.I.M. capacitors
- Air bridges
- Via-holes
- Wafer thickness: 100 μm
- Wafer diameter: 100mm
- Space evaluated process according to ESA (EPPL)



One 5 μm finger BES Schottky diode

Design Kit Characteristics

- Available for ADS from Keysight, MwO from AWR and Nexxim from Ansoft
- Schematic entry with autolayout generation
- Scalable models for passive devices
- Scalable non-linear diode models
- Data for spread analysis

Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
Diode (1x5µm)					
Ideality factor n	1.0	1.2	1.3	-	Vdiode = 0.55V
J0 diode	-	3e-6	1e-4	A/cm ²	
Series resistance Rs	3	5	8	Ω	Idiode = 15mA
Breakdown voltage V_bd	-10	-6.5	-5	V	Idiode = -20µA
Forward voltage V_on	-	0.65	0.8	V	Idiode = 20µA
Coplanar diode (1x5µm)					
equivalent circuit					
Cut-off frequency	3			THz	
Intrinsic capacitance Cj	8			fF	
Parasitic capacitance Cp	6			fF	
TaN RESISTOR /					
sheet resistance	26	30	34	Ω/square	
MIM CAPACITOR /					
density	290	330	370	pF/mm ²	@1MHz
TiWSi RESISTOR /					
sheet resistance	800	1000	1200	Ω/square	
GaAs RESISTOR					
Ohmic contact resistance	-	0.05	0.3	Ω.mm	
GaAs sheet resistance	7	9	11	Ω/square	

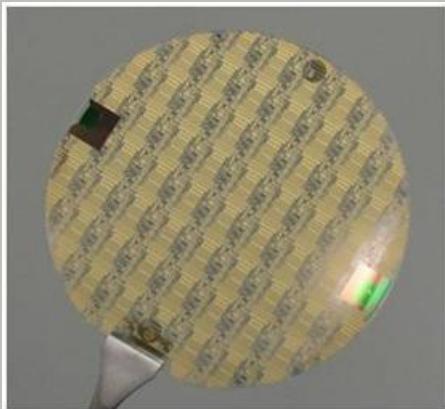
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GH15-1x



Description

This 0.15µm HEMT process is optimized for high power applications up to 45GHz. The good HEMT noise performance allows also LNA design.

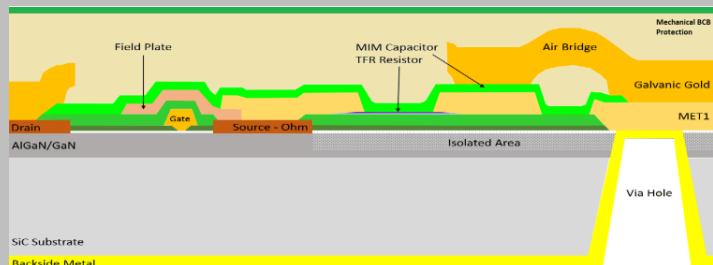
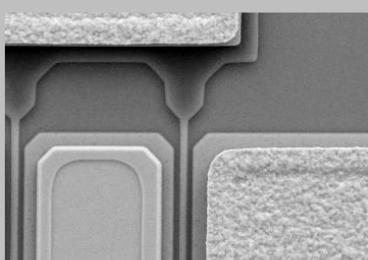
The process includes two metal interconnect layers, precision TaN resistors, high values TiWSi resistors, MIM capacitors with standard and high density, air-bridges and via-holes through the substrate.

GH15 is available in four technology versions:

- GH15-10, Space evaluated
- GH15-11, providing additional options, such as High Density MIM 355pF/mm² and BCB mechanical protection for compatibility with plastic molded packaging.
- GH15-12, providing mechanical and humidity protection
- GH15-13, with thinner substrate specially optimized for Q-band applications

Main Features

- 0.15µm GaN on SiC HEMT process
- Power density: 4.2 W/mm
- TaN and TiWSi resistors
- M.I.M. capacitors & inductors
- Air bridges
- Via-holes
- Operation Vds= 25V
- Vbds > 60V
- Wafer thickness: 70/50 µm
- Wafer diameter: 100mm
- Schottky diodes



Design Kit Characteristics

- Available for ADS by Keysight, MwO by CADENCE
- Non-linear electro-thermal model for source grounded FET
- Noise model for LNA design
- Switch and diode models
- Scalable models for passive and active devices.

Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
FET /					
Threshold voltage V _p	-3.7	-3.0	-2.3	V	V _{ds} =7.0V I _{ds} =I _{dss} /100
Transconductance G _m	325	405	-	mS/mm	V _{ds} =7.0V, V _{gs} =V _{GMMax}
Saturation current I _{dss}	1350	1450	1550	mA/mm	V _{ds} =7.0V, V _{gs} =3V

Coplanar FET (2x75µm)
equivalent circuit

Transconductance G _{me}	23	30	38	mS	
Input capacitance C _{in}	105	125	145	fF	
Feedback capacitance C _f	13	18	23	fF	

TaN RESISTOR /

sheet resistance	26	30	34	Ω/square	
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MIM CAPACITOR /

Standard Density	160	175	190	pF/mm ²	
High Density (GH15-11/-13)	330	355	380		

TiWSi RESISTOR /

sheet resistance	800	1000	1200	Ω/square	
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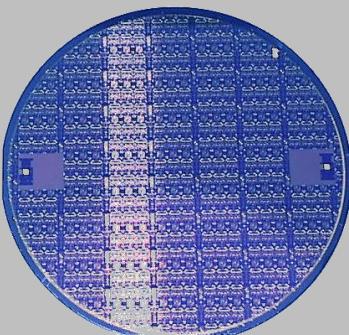
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Foundry Process Data Sheet



HB20M

VCO HBT



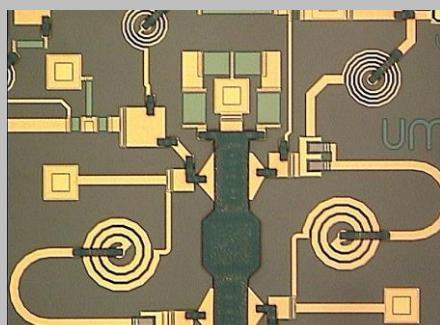
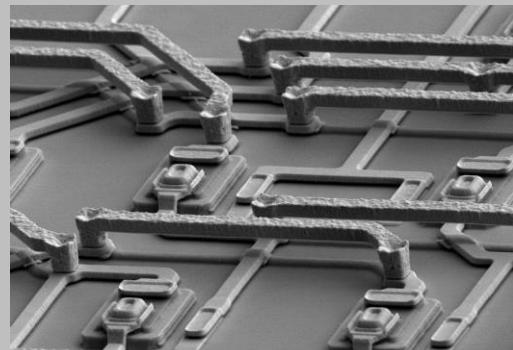
Main Features

- 2µm emitter HBT
- Typical F_t : 30GHz
- TaN and TiWSi resistors
- M.I.M. capacitors
- Via-holes
- Operation V_{ce} = 6V
- Wafer thickness: 100µm
- Wafer diameter: 100mm
- Space evaluated process according to ESA (EPPL)

Description

The HB20M 2µm emitter length HBT process is optimized for VCO application up to 25GHz. The process includes two metal interconnect layers, precision TaN resistors, high values TiWSi resistors, MIM capacitors, air-bridges and via-holes through the substrate.

HB20M is a fully passivated HBT process.



Design Kit Characteristics

- Available for ADS from Keysight
- Schematic entry with autolayout generation (passive)
- Scalable models for passive devices
- Scalable non-linear transistor model including 1/f noise.
- Temperature effect
- Data for spread analysis

Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
Base sheet resistance	150	200	250	Ω/square	Measured on TLM
Base contact resistance	-	15e-6	3e-6	Ω/cm ²	Measured on TLM
Breakdown voltage Vce	14	18	-	V	Ib=0, Ic=Ie=500μA

Coplanar transistor (2x30μm²) equivalent circuit

Feedback capacitor Cbc	28	35	42	fF	Vce=3.0V, Ic=20mA
Emitter resistance Re	2	2.5	4	Ω	Vce=3.0V, Ic=20mA
Gmo x Rbe product (β)	30	45	70	-	Vce=3.0V, Ic=20mA
Offset voltage (Vce_sat)	-	0.15	0.3	V	Ib=Ie=1mA , Ic=0

TaN RESISTOR /

sheet resistance	26	30	34	Ω/square
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MIM CAPACITOR /

density	220	260	280	pF/mm ²	@1MHz
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TiWSi RESISTOR /

sheet resistance	800	1000	1200	Ω/square
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Ordering Information

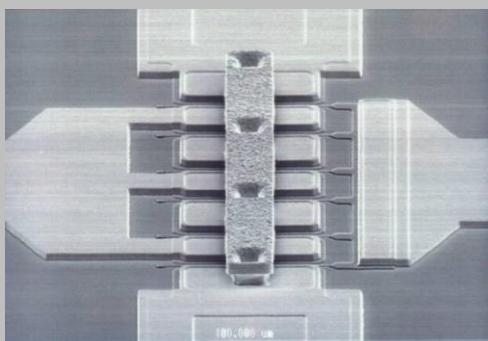
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HP07

0.7µm MESFET

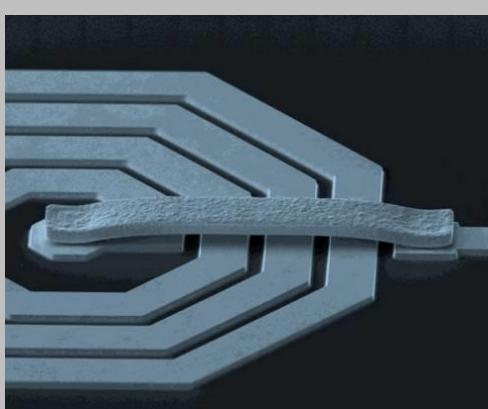
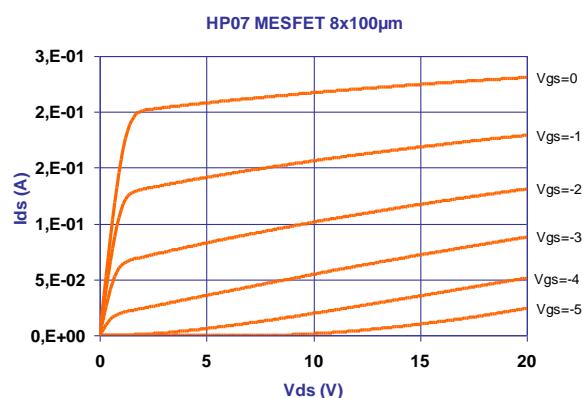


Description

The 0.7µm optical gate MESFET process is optimized for multipurpose operation up to 20GHz. The process includes two metal interconnect layers, precision TaN resistors, MIM capacitors, air-bridges and via-holes through the substrate.

Main Features

- 0.7µm MESFET process
- Typical F_t : 15GHz
- TaN and TiWSi resistors
- GaAs resistors
- M.I.M. capacitors
- Air bridges
- Via-holes
- Operation V_{ds} = 10V
- Wafer thickness: 100µm
- Wafer diameter: 100mm
- Space evaluated process according to ESA (EPPL)



Design Kit Characteristics

- Available for ADS from Keisight
- Schematic entry with autolayout generation
- Scalable models for passive devices
- Scalable non-linear models for FET
- Scalable linear and noise model for FET
- Scalable models for series and parallel switch configuration
- Scalable non linear models for reversed (varactors) and forwarded diodes (mixers)
- Data for spread analysis

Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
FET /					
Threshold voltage V _p	-5.0	-4.1	-3.3	V	V _{ds} =3.0V, I _{ds} =I _{dss} /100
Transconductance G _m	85	110	-	mS/mm	V _{ds} =3.0V, V _{gs} =0V
Saturation current I _{dss}	240	300	360	mA/mm	V _{ds} =3.0V, V _{gs} =0V
Breakdown voltage V _{bds}	14	15	-	V	I _{ds} = I _{dss} /100
Coplanar FET (2x75µm) equivalent circuit					
Transconductance G _{me}	9	12	18	mS	V _{ds} =3.0V, V _{gs} =0V
Input capacitance C _{in}	85	130	175	fF	V _{ds} =3.0V, V _{gs} =0V
Feedback capacitance C _f	9	14	17	fF	V _{ds} =3.0V, V _{gs} =0V
Output resistance R _{out}	400	600	950	Ω	V _{ds} =3.0V, V _{gs} =0V
TaN RESISTOR /					
sheet resistance	26	30	34	Ω/square	
MIM CAPACITOR /					
density	220	260	280	pF/mm ²	@1MHz
TiWSi RESISTOR /					
sheet resistance	800	1000	1200	Ω/square	
GaAs RESISTOR					
Ohmic contact resistance	-	0.10	0.3	Ω.mm	
GaAs sheet resistance	135	158	180	Ω/square	

Ordering Information

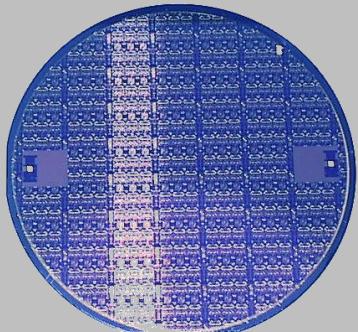
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PH10-10

0.1µm very low noise pHEMT



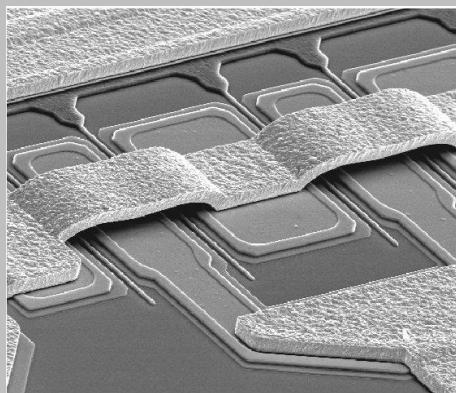
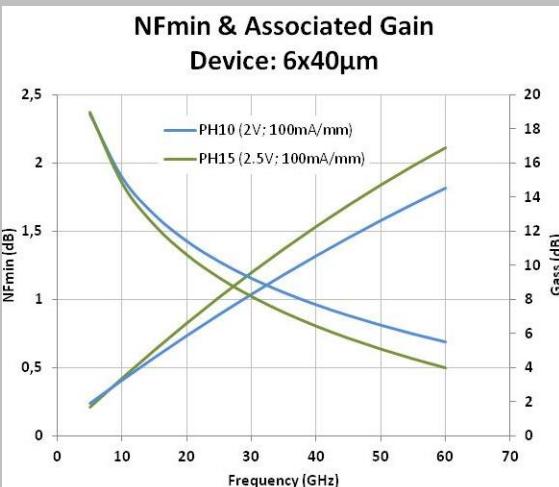
Description

The 0.1µm pHEMT process is optimized for very low noise up to 110GHz. The process includes two metal interconnect layers, precision TaN resistors, high values TiWSi resistors, MIM capacitors, air-bridges and via-holes through the substrate.

Overcoating layer is available as an option.
Hot-vias are available as an option

Main Features

- 0.1µm pHEMT process
- Typical F_t : 130GHz
- TaN and TiWSi resistors
- GaAs resistors
- M.I.M. capacitors
- M.I.M. capacitors over via-hole
- Air bridges
- Via-holes
- Operation V_{ds} = 2V to 3V
- Wafer thickness: 70µm
- Wafer diameter: 100mm



Design Kit Characteristics

- Available for ADS from Keysight.
- DRC on line with ADS DK
- Scalable non-linear model for FET with noise
- Scalable models for passive devices
- Scalable non-linear models for FET (2 & 3 ports)
- Scalable models for series and parallel switch configuration
- Scalable non linear models for diodes (mixers)
- Data for spread analysis

Foundry Process Data Sheet



Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
FET /					
Threshold voltage V _p	-0.7	-0.45	-0.2	V	V _{ds} =2.0V, I _{ds} =I _{dss} /100
Transconductance G _{mmax}	625	750	-	mS/mm	V _{ds} =2.0V, G _m _max
Saturation current I _{dmax}	200	280	-	mA/mm	V _{ds} =2.0V, G _{mmax}
Breakdown voltage V _{bds}	5.0	6.0	-	V	I _{ds} = I _{dss} /100
Coplanar FET (2x75μm) equivalent circuit					
Transconductance G _{me}	85	100	115	mS	V _{ds} =3.0V, V _{gs} =0V
Input capacitance C _{in}	90	110	125	fF	V _{ds} =3.0V, V _{gs} =0V
Feedback capacitance C _f	23	28	33	fF	V _{ds} =3.0V, V _{gs} =0V
Output resistance R _{out}	80	110	140	Ω	V _{ds} =3.0V, V _{gs} =0V
TaN RESISTOR /					
sheet resistance	26	30	34	Ω/square	
MIM CAPACITOR /					
density	300	330	360	pF/mm ²	@1MHz
TiWSi RESISTOR /					
sheet resistance	800	1000	1200	Ω/square	
GaAs RESISTOR					
Ohmic contact resistance	-	0.13	0.2	Ω.mm	
GaAs sheet resistance	100	120	130	Ω/square	

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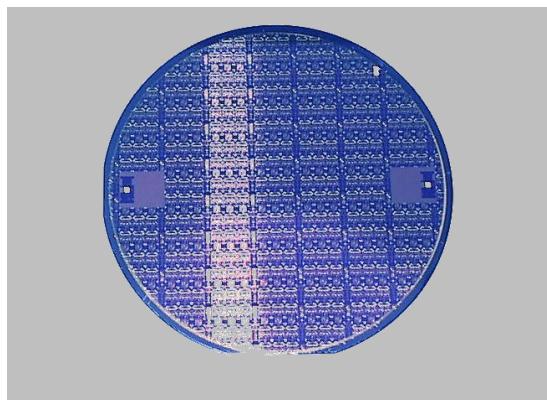
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PH10-20

0.1µm very low noise pHEMT



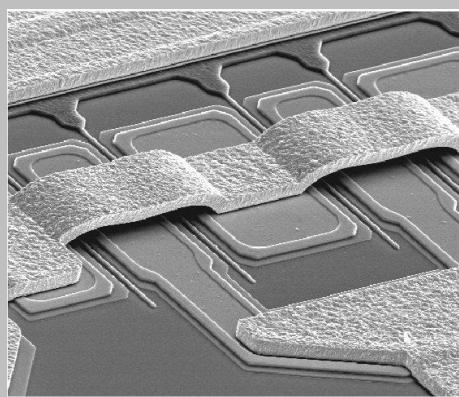
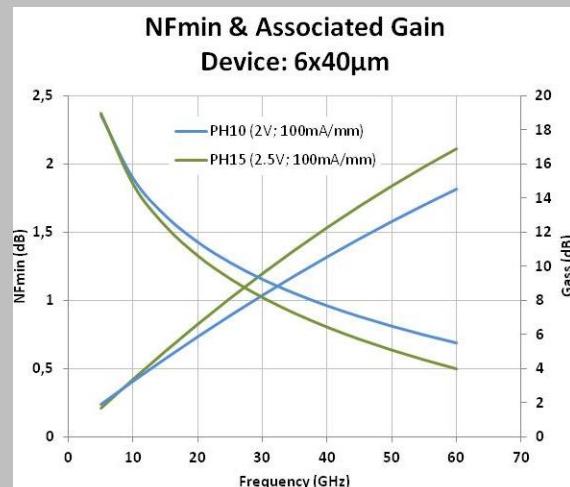
Description

The 0.1µm pHEMT process is optimized for very low noise up to 110GHz. The process includes two metal interconnect layers, precision TaN resistors, high values TiWSi resistors, two densities of MIM capacitors and MIM over via capacitors, air-bridges, hot-vias and via-holes through the substrate.

Overcoating layer is available as an option.
Hot vias are available as an option

Main Features

- 0.1µm pHEMT process
- Typical F_t : 130GHz
- TaN and TiWSi resistors
- GaAs resistors
- M.I.M. capacitors
- M.I.M. capacitors over via-hole
- Air bridges
- Via-holes
- Operation V_{ds} = 2V to 3V
- Wafer thickness: 70µm
- Wafer diameter: 100mm



Design Kit Characteristics

- Available for ADS from Keysight.
- DRC on line with ADS DK
- Scalable non-linear model for FET with noise
- Scalable models for passive devices
- Scalable non-linear models for FET (2 & 3 ports)
- Scalable models for series and parallel switch configuration
- Scalable non linear models for diodes (mixers)
- Data for spread analysis

Electrical Characteristics

Process Data Sheet

0.1µm very low noise pHEMT PH10-20

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
FET /					
Threshold voltage V _p	-0.7	-0.45	-0.2	V	V _{ds} =2.0V, I _{ds} =I _{dss} /100
Transconductance G _{mmax}	625	750	-	mS/mm	V _{ds} =2.0V, G _m _max
Saturation current I _{dmax}	200	280	-	mA/mm	V _{ds} =2.0V, G _{mmax}
Breakdown voltage V _{bds}	5.0	6.0	-	V	I _{ds} = I _{dss} /100
Coplanar FET (2x75µm) equivalent circuit					
Transconductance G _{me}	85	100	115	mS	V _{ds} =3.0V, V _{gs} =0V
Input capacitance C _{in}	90	110	125	fF	V _{ds} =3.0V, V _{gs} =0V
Feedback capacitance C _f	23	28	33	fF	V _{ds} =3.0V, V _{gs} =0V
Output resistance R _{out}	80	110	140	Ω	V _{ds} =3.0V, V _{gs} =0V
TaN RESISTOR /					
sheet resistance	26	30	34	Ω/square	
MIM CAPACITOR /					
Standard density	230	250	270	pF/mm ²	@1MHz
High density (DHD)	550	625	700	pF/mm ²	@1MHz
TiWSi RESISTOR /					
sheet resistance	800	1000	1200	Ω/square	
GaAs RESISTOR					
Ohmic contact resistance	-	0.13	0.2	Ω.mm	
GaAs sheet resistance	100	120	130	Ω/square	

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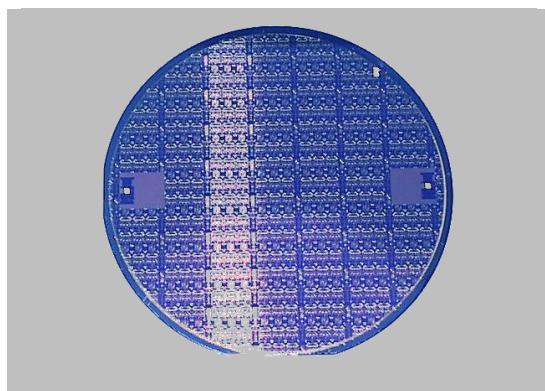
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Foundry Process Data Sheet



PH15



0.15µm very low noise pHEMT

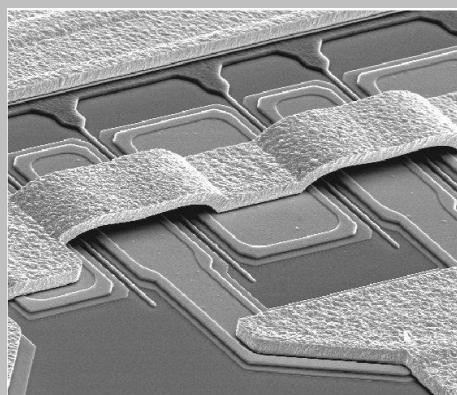
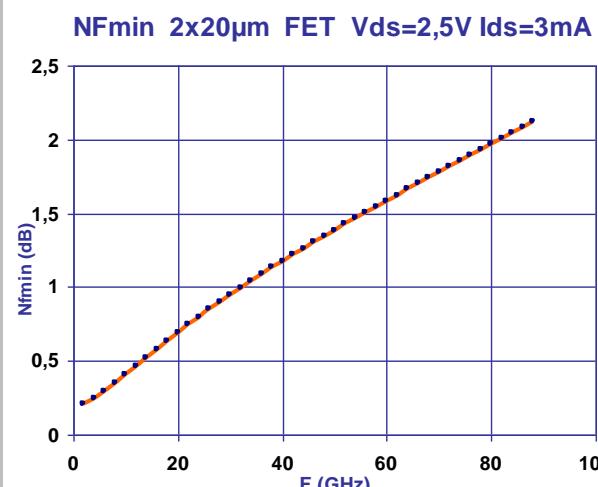
Description

The 0.15µm pHEMT process is optimized for very low noise up to 60GHz. The process includes two metal interconnect layers, precision TaN resistors, high values TiWSi resistors, MIM capacitors, air-bridges and via-holes through the substrate.

Overcoating layer is available as an option.

Main Features

- 0.15µm pHEMT process
- Typical F_t : 110GHz
- TaN and TiWSi resistors
- GaAs resistors
- M.I.M. capacitors
- Air bridges
- Via-holes
- Operation V_{ds} = 2.5V
- Wafer thickness: 100µm
- Wafer diameter: 100mm
- Space evaluated process according to ESA (EPPL)



Design Kit Characteristics

- Available for ADS from Keysight, MwO from AWR and Nexxim from Ansoft
- DRC on line with ADS DK
- Schematic entry with autolayout generation
- Scalable models for passive devices
- Scalable non-linear model for FET with noise
- Scalable non linear model forwarded diodes (mixers and detectors)
- Data for spread analysis

Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
FET /					
Threshold voltage V _p	-1.0	-0.75	-0.5	V	V _{ds} =2.0V, I _{ds} =I _{dss} /100
Transconductance G _{mmax}	580	650	-	mS/mm	V _{ds} =2.0V, G _m _max
Saturation current I _{dmax}	220	280	-	mA/mm	V _{ds} =2.0V, G _{mmax}
Breakdown voltage V _{bds}	4.5	6	-	V	I _{ds} = I _{dss} /100
Coplanar FET (2x75µm) equivalent circuit					
Transconductance G _{me}	80	95	110	mS	V _{ds} =3.0V, V _{gs} =0V
Input capacitance C _{in}	80	110	140	fF	V _{ds} =3.0V, V _{gs} =0V
Feedback capacitance C _f	20	25	30	fF	V _{ds} =3.0V, V _{gs} =0V
Output resistance R _{out}	130	160	190	Ω	V _{ds} =3.0V, V _{gs} =0V
TaN RESISTOR /					
sheet resistance	26	30	34	Ω/square	
MIM CAPACITOR /					
density	290	330	370	pF/mm ²	@1MHz
TiWSi RESISTOR /					
sheet resistance	800	1000	1200	Ω/square	
GaAs RESISTOR					
Ohmic contact resistance	-	0.13	0.3	Ω.mm	
GaAs sheet resistance	100	120	140	Ω/square	

Ordering Information

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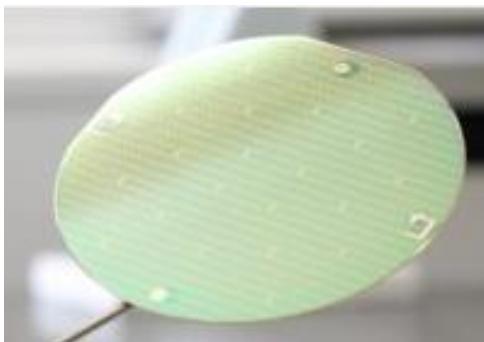
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Foundry Process Data Sheet



PH25-20

0.25µm low noise pHEMT



Description

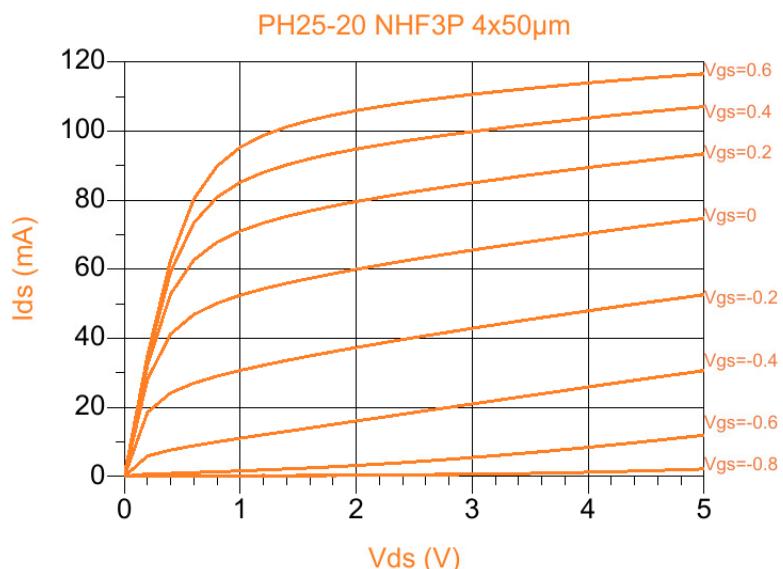
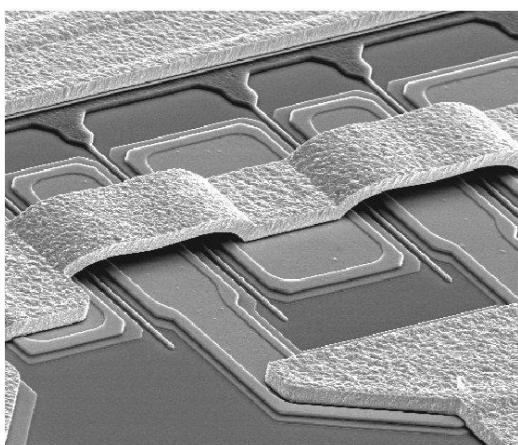
The 0.25µm pHEMT process is optimized for low noise up to 60GHz. The second generation PH25-20 features a thinner substrate (70 µm instead of 100 µm), which allows additional 2-ports transistor topologies with individual source vias. The process includes two metal interconnect layers, precision TaN resistors, high values TiWSi resistors, two densities of MIM capacitors and MIM over via capacitors, air-bridges, hot-vias and via-holes through the substrate.

Overcoating layer is available as an option.

Hot vias are available as an option

Main Features

- 0.25µm pHEMT process
- Typical F_t : 90GHz
- TaN and TiWSi resistors
- GaAs resistors
- M.I.M. capacitors
- M.I.M capacitors over via-hole
- D.H.D capacitors
- D.H.D capacitors over via-hole
- Air bridges
- Via-holes
- Hot-vias
- Operation V_{ds} = 3V
- Wafer thickness: 70µm
- Wafer diameter: 100mm



Design Kit Characteristics

- Available for ADS from Keysight
- e-DRC with ADS DK
- Schematic entry with autolayout generation
- Scalable models for passive devices
- Scalable non-linear models for FET (2 & 3 ports)
- Scalable linear and noise model for FET
- Scalable models for series and parallel switch configuration
- Scalable non linear models for reversed (varactors) and forwarded diodes (mixers)
- Data for spread analysis

Foundry Process Data Sheet



Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
FET /					
Threshold voltage V _p	-1.0	-0.75	-0.5	V	V _{ds} =2.5V, I _{ds} =I _{dss} /100
Transconductance G _m	400	530	-	mS/mm	V _{ds} =2.5V, V _{gs} =0V
Saturation current I _{dss}	200	340	460	mA/mm	V _{ds} =2.5V, V _{gs} =0V
Breakdown voltage V _{bds}	6	7.5	-	V	I _{ds} = I _{dss} /100
Coplanar FET (2x75μm) equivalent circuit					
Transconductance G _{me}	70	85	100	mS	V _{ds} =3.0V, V _{gs} =0V
Input capacitance C _{in}	120	150	180	fF	V _{ds} =3.0V, V _{gs} =0V
Feedback capacitance C _f	20	25	30	fF	V _{ds} =3.0V, V _{gs} =0V
Output resistance R _{out}	160	220	300	Ω	V _{ds} =3.0V, V _{gs} =0V
MIM CAPACITOR /					
Standard Density	230	250	270	pF/mm ²	@1MHz
High Density (DHD)	550	625	700	pF/mm ²	@1MHz
TaN RESISTOR /					
Sheet resistance	26	30	34	Ω/square	
TiWSi RESISTOR /					
Sheet resistance	800	1000	1200	Ω/square	
GaAs RESISTOR /					
Ohmic contact resistance	-	0.15	0.3	Ω.mm	
GaAs sheet resistance	100	120	140	Ω/square	

Ordering Information

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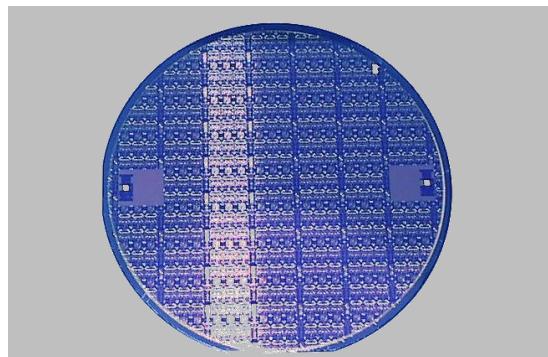
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Foundry Process Data Sheet



PPH15X-20



0.15µm power pHEMT

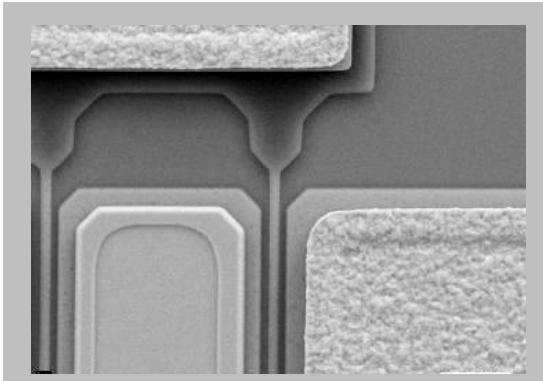
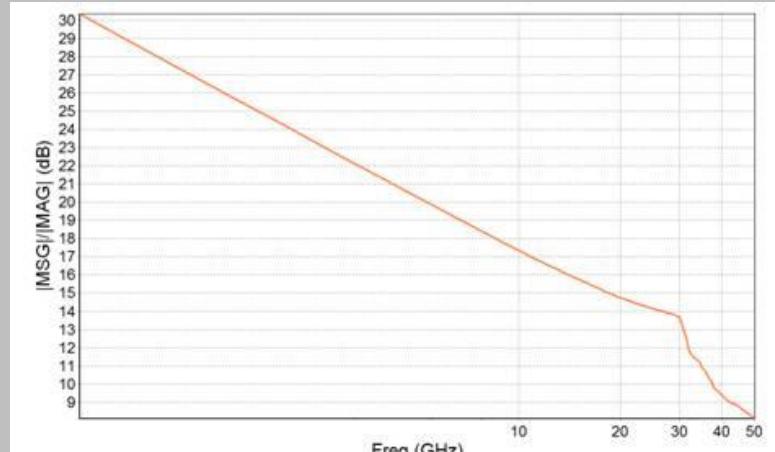
Description

This 0.15µm pHEMT process is optimized for wideband high power amplification up to 45GHz. The process includes two metal interconnect layers, precision TaN resistors, high values TiWSi resistors, MIM capacitors, air-bridges and via-holes through the substrate.

Overcoating layer is available as an option.

Main Features

- 0.15µm pHEMT process
- Typical F_t : 70GHz
- Power density: 800mW/mm
- TaN and TiWSi resistors
- GaAs resistors
- M.I.M. capacitors (standard & high density)
- Air bridges
- Via-holes
- Operation V_{ds} = 6.0V
- $V_{bds} > 12.0V$
- Wafer thickness: 70µm
- Wafer diameter: 100mm



Design Kit Characteristics

- Available for ADS from Keysight, MwO from AWR
- Scalable models for passive devices
- Non-linear model for source grounded FET

Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
FET /					
Threshold voltage V _p	-1.2	-0.95	-0.7	V	V _{ds} =2.0V, I _{ds} =I _{dss} /100
Transconductance G _m	430	-	-	mS/mm	V _{ds} =2.0V, V _{gs} =0V
Saturation current I _{dss}	270	-	-	mA/mm	V _{ds} =2.0V, V _{gs} =0V
Breakdown voltage V _{bds}	12	14	18	V	I _{ds} = I _{dss} /100

Coplanar FET (2x75µm)

equivalent circuit

Transconductance G _{me}	45	60	75	mS	V _{ds} =3.0V, V _{gs} =0V
Input capacitance C _{in}	100	130	160	fF	V _{ds} =3.0V, V _{gs} =0V
Feedback capacitance C _f	12	15	18	fF	V _{ds} =3.0V, V _{gs} =0V
Output resistance R _{out}	300	400	500	Ω	V _{ds} =3.0V, V _{gs} =0V

TaN RESISTOR /

sheet resistance	26	30	34	Ω/square	
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MIM CAPACITOR /

Standard Density	240	250	280	pF/mm ²	@1MHz
	550	625	700		@1MHz

TiWSi RESISTOR /

sheet resistance	800	1000	1200	Ω/square	
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GaAs RESISTOR

Ohmic contact resistance		0.12	0.3	Ω.mm	
GaAs sheet resistance	85	95	105	Ω/square	

Ordering Information

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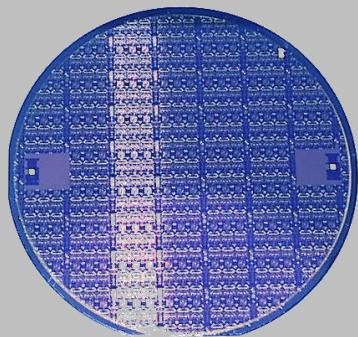
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Foundry Process Data Sheet



PPH25

0.25µm power pHEMT



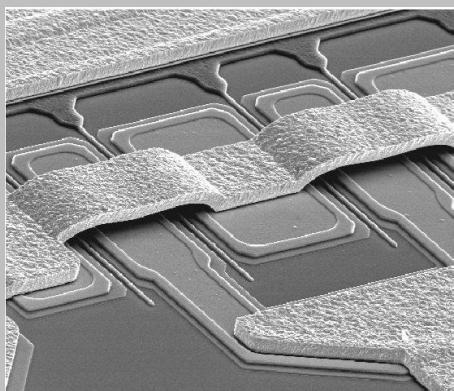
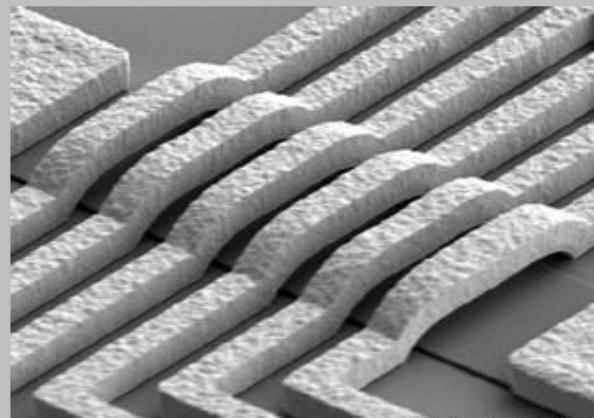
Description

The 0.25µm pHEMT process is optimized for power and multipurpose up to 40GHz. The process includes two metal interconnect layers, precision TaN resistors, high values TiWSi resistors, MIM capacitors, air-bridges and via-holes through the substrate.

Overcoating layer is available as an option.

Main Features

- 0.25µm pHEMT process
- Typical Ft: 50GHz
- TaN and TiWSi resistors
- GaAs resistors
- M.I.M. capacitors
- Air bridges
- Via-holes
- Operation Vds= 6V
- Wafer thickness: 100µm
- Wafer diameter: 100mm



Design Kit Characteristics

- Available for ADS from Keysight and MwO from AWR
- DRC on line with ADS DK
- Schematic entry with autolayout generation
- Scalable models for passive devices
- Scalable non-linear models for FET
- Scalable models for series and parallel switch configuration
- Data for spread analysis

Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
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FET /

Threshold voltage V _p	-1.2	-0.9	-0.7	V	V _{ds} =2.5V, I _{ds} =I _{dss} /100
Transconductance G _m	370	430	-	mS/mm	V _{ds} =2.5V, V _{gs} =0V
Saturation current I _{dss}	250	325	400	mA/mm	V _{ds} =2.5V, V _{gs} =0V
Breakdown voltage V _{bds}	12	13	-	V	I _{ds} = I _{dss} /100

Coplanar FET (2x75µm)

equivalent circuit

Transconductance G _{me}	50	60	75	mS	V _{ds} =3.0V, V _{gs} =0V
Input capacitance C _{in}	140	170	200	fF	V _{ds} =3.0V, V _{gs} =0V
Feedback capacitance C _f	9	12	15	fF	V _{ds} =3.0V, V _{gs} =0V
Output resistance R _{out}	550	750	950	Ω	V _{ds} =3.0V, V _{gs} =0V

TaN RESISTOR /

sheet resistance	26	30	34	Ω/square	
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MIM CAPACITOR /

density	220	250	280	pF/mm ²	@1MHz
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TiWSi RESISTOR /

sheet resistance	800	1000	1200	Ω/square	
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GaAs RESISTOR

Ohmic contact resistance	-	0.15	0.3	Ω.mm	
GaAs sheet resistance	85	95	105	Ω/square	

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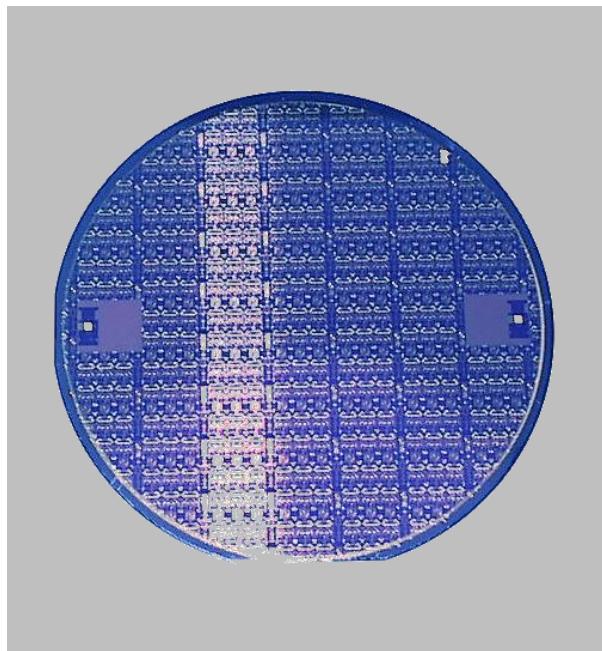
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Foundry Process Data Sheet



ULRC-20

Passive process



Description

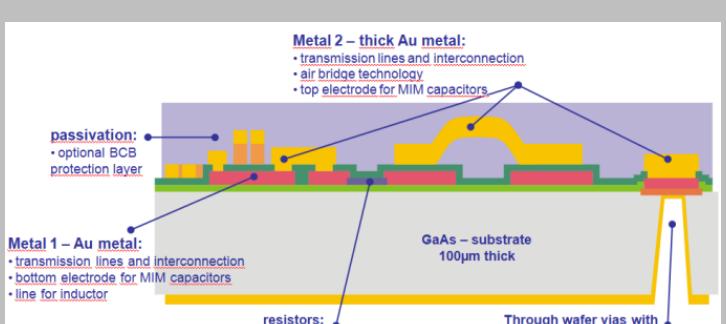
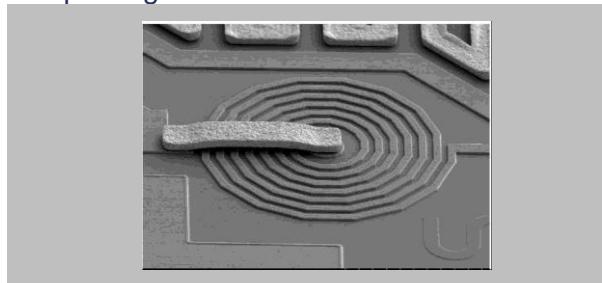
ULRC-20 is a GaAs passive process gathering GaAs properties: high resistivity, good isolation and high dielectric constant. These advantages are associated with high voltage MIM capacitors and high current density metal lines. This process is optimized for reproducibility, power handling, low losses, up to high frequency and for high volume / high yield production.

ULRC-20 allows very diverse passive circuit design including accurate microwave filters, RF power combiners, microwave baluns, matching elements, low losses lines; power bar input and output matching circuits.

ULRC-20 is widely recommended to design hybrid microwave circuits for amplifier modules used into antenna transmitters and receivers such as Radars, Telecom and Space Communication systems.

Main Features

- Fully optical process
- M.I.M. capacitors
- Inductors
- Metallic resistors
- TaN and TiWSi resistors
- Via holes through the GaAs substrate
- Thick Au lines
- Wafer thickness: 100µm
- Wafer diameter: 4"
- Optional coating compatible with plastic package



Design Kit Characteristics

- Available for ADS from Keysight,
- Schematic entry with autolayout generation
- Scalable models
- Data for spread analysis

Process Data Sheet

Passive process
ULRC-20

Electrical Characteristics

ELEMENT / Parameters	Min	Typ	Max	Units	Conditions
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INDUCTOR

Inductance	0.1		12.7	nH	
Via hole diameter		30x30		um	
Substrate thickness		100		μm	

TaN RESISTOR /

sheet resistance	26	30	34	Ω/square	
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TiWSi RESISTOR /

sheet resistance	800	1000	1200	Ω/square	
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MIM CAPACITOR /

Density	160	175	190	pF/mm ²	@1MHz
Voltage	150			V	

Ordering Information

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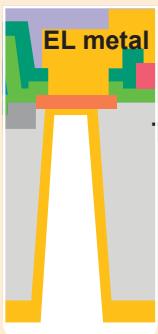
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FOUNDRY INNOVATION BY UMS

At UMS we constantly innovate to make our open III-V foundry technologies more and more efficient for our customers, facilitating frequency rise and assembly in innovative ad-hoc solutions (BGA, etc.). Check out our new generations PH10-20 and PH25-20.

I.S.V.

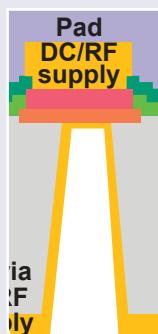


Individual Source Vias

Thanks to thinner substrate, FET via-holes for grounding can be directly below FET sources to reduce parasitic source inductance. The FET is more compact:

- Higher Ft, Fmax
- Higher Gain
- Easier matching

H.V.



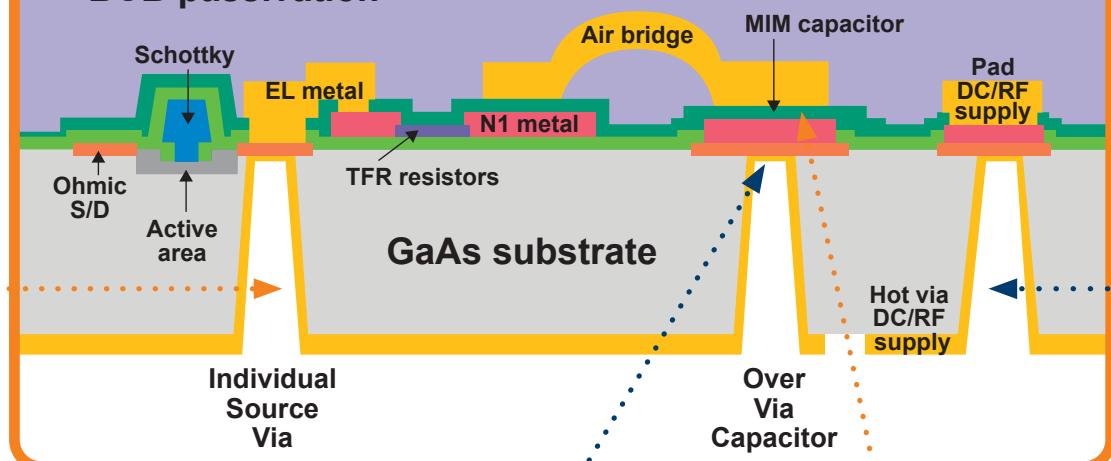
Hot Vias

That new option allows RF signal or DC biasing to be handled through a back side patterning.

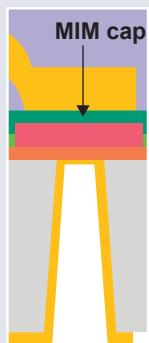
Die may be assembled with a flip-chip process in BGA solutions, shortening connections for DC & RF.

Very efficient solution for high frequency MMICs, reducing the parasitics of assembly (no more long wires needed).

BCB passivation



C.O.V.

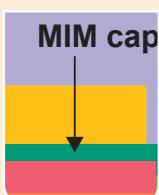


Capacitor over Via

Small via-holes directly connected to the bottom electrode of shunt MIM capacitor make it better for high frequency design, strongly reducing the series inductance:

Design is more compact and efficient, wideband design is also simplified.

H.D.M.C.



High density MIM Capacitor

Specific dielectric layers, optimized to support high voltages, define two capacitor density options.

In particular, the new $625\text{pF}/\text{mm}^2$ capacitor density allows more compact design by significantly reducing the size of the decoupling network.



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