CPE 523 - Homework 2

Technology Info:

For all problems, please use the following values where needed (based on 45nm tech)

- $\lambda = 0.0225\,\mu m$
- $R_{sqp} = 26\,k\Omega/sq$
- $R_{sqn} = 26\,k\Omega/sq$
- $C_{gate} = 1.2\,fF/\mu m$
- $C_{d} = 1.2\,fF/\mu m$
- $C_{wire} = 0.3\,fF/\mu m$
- $V_{DD} = 1.0\,V$
- All transistors have minimum length 2λ

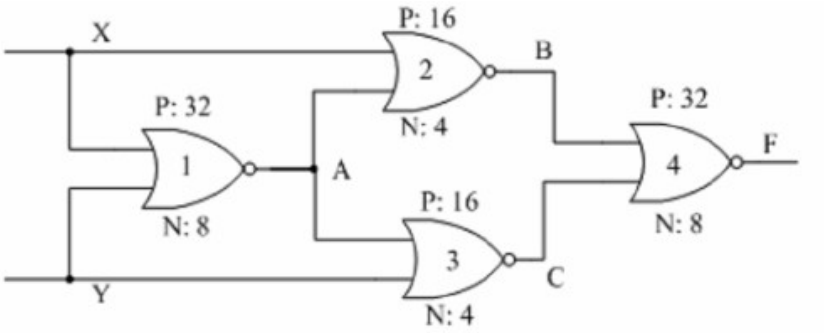
1. Gate Design

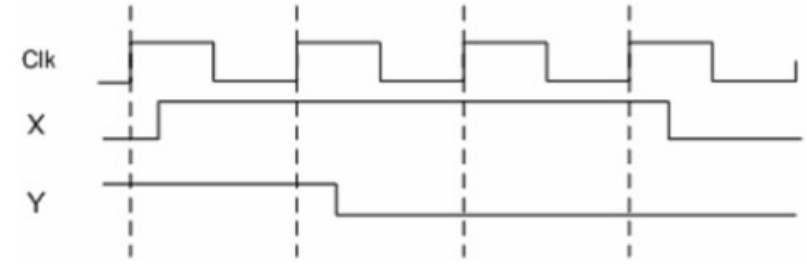
Implement the following functions using a single CMOS gate (transistor level diagram). Assume inputs and their complements are available.

a) F = (AB) + (C)
b) F = ((A + B)(C' + D')E)'

2. Energy and Power Calculation

Consider the combinational logic block below. It works inside a big sequential circuit (not shown in the figure) which is operating at 1Ghz (1ns cycle time). In this problem, we will look at energy consumption of this combinational block during four clock cycles, All the gate sizes are marked on the schematic. The N:4 notation means that EACH of the nMOS in a particular gate has size 4λ. The waveforms of the inputs are given in the figure below the circuit. The vertical gridlines in the figure represent one clock cycle. Assume the clock cycle time is long enough for any change at the inputs (X or Y) to propagate through this whole circuit.





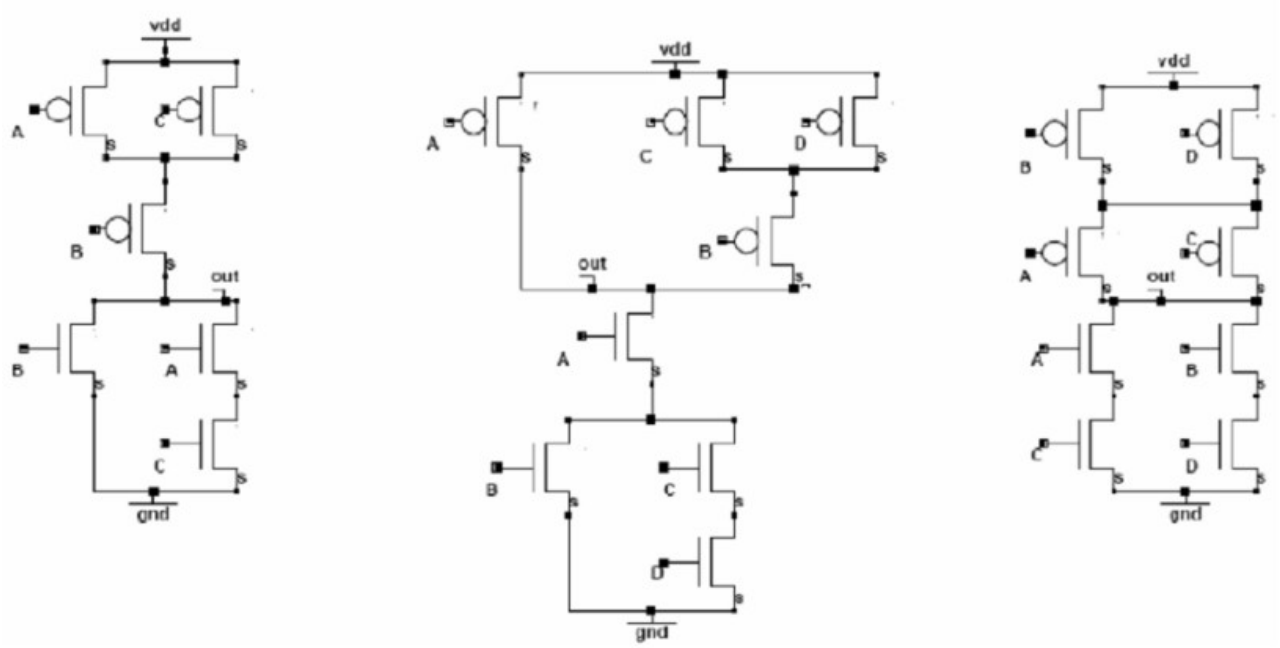
a) draw the waveforms for the rest of the nodes marked in this circuit (A,B,C,F)

b) Calculate the total number of transistions as well as the activity factors of each node (X,Y,A,B,C,F). Activity factors are the per-cycle-transitions averaged across the 4 cycles we consider.

c) Calculate the energy and average power dissipation for each node (X,Y,A,B,C,F). Assume all wires in this circuit are 200 λ long. You will also need to add the capacitance from the gates loading the output, and the internal parasitic capacitance from the diffusion capacitance. To simplify the calculation, only consider the parasitic capacitance directly on the output node of a logic gate. You do not need to consider any capcitance outside this circuit, Also, consider clock period T = 1ns for this equation

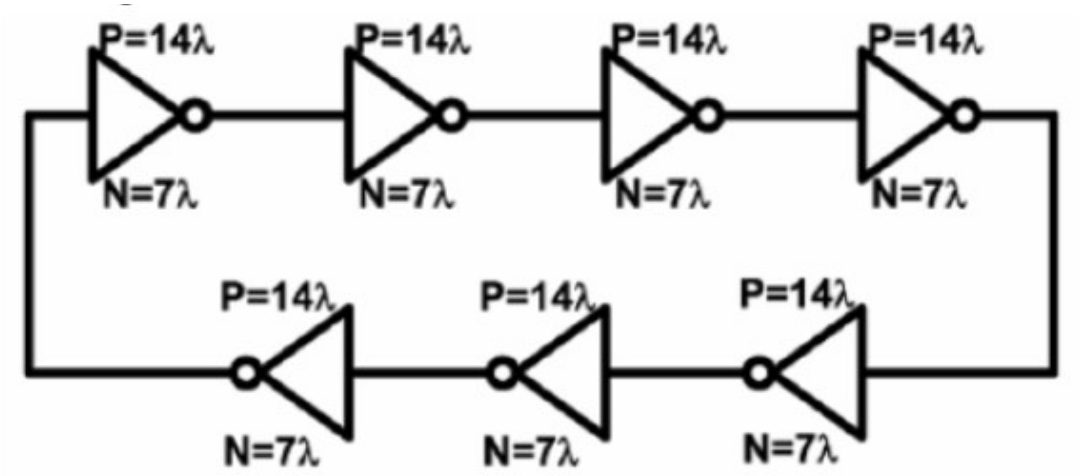
3. **Transistor Sizing**

For the gates shown below, find the transistor sizes (in terms of λ) so that the pull-up and pull-down resistance in the worst case is 2.6K. In some of these circuits you will have transistors in series, so there will be many ways to make the total equal to 2.6K. Your goal will be to choose the best sizes for each of the transistors, which usually means trying to keep the capacitance of each input close to each other. This generally means that you make the resistance of the series devices the same (but not always)



4. **Ring Oscillator**

Consider the ring oscillator shown below:



a) Find the RC delay of one of the inverters in the ring. What are the contributions from fanout delay (RC load) and parasitic delay (RC parasitic), respectively?

b) What is the period of oscillation of the ring in picoseconds? What is the frequency?

5. **Static Timing Analysis**

Consider the logic network defined by the following structural Verilog expressions:

```
inv ginv1(k, a);
or gor1(e, k, b);
nor gor1(e, k, b);
and gand1(f, a, g);
and gand2(h, a, b);
xnor gxnor1(i, f, d);
or gor2(j, d, s);
xor gxor1(x, e, I)
or gor3(y, j, h)
```

Inputs are {a,b,c,d,s} and outputs are {x,y}

a) Draw and label a gate level schematic diagram for this network

b) Assume that the delay of each INV, AND, and OR gate is 1, and the delay of each NOR, XOR, and XNOR gate is 2. Neglect all wire delays. Compute the arrival time and slacks for all vertices in this network. Assume that the input arrival times are zero except for input s, where arrivals(s) = 4. The required arrival time at the output is 7.

c) Determine the critical path of this network