Problem 1: Consider a unit sized two-input NOR gate. (5 points)

i. Determine the activity factor $\alpha_{0\to1}$ for this gate.

ii. Calculate the dynamic power consumption of the gate that drives a total $C_{out} = C_{int} + C_L$ = 12fF capacitance, at 100MHz from a 2V power supply.

Solution:

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

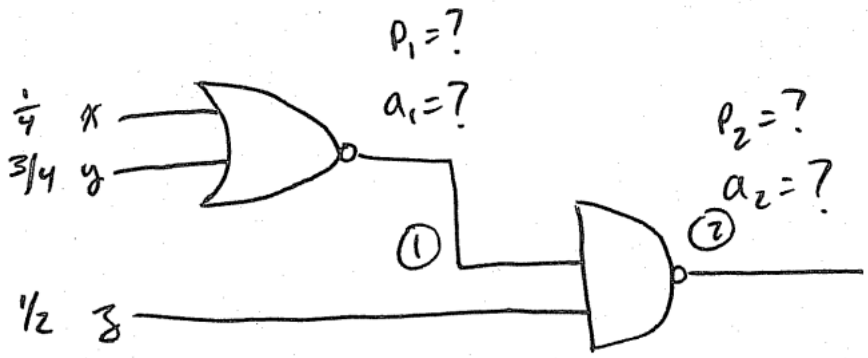
i. From the truth table, $P_1 = \overline{P_A}.\overline{P_B}$=1/4

P_0= (1-1/4) = ¾

$\alpha_{0\to1}$=P_0.P_1= 3/16 = 0.1875

ii. $P_{dyn}= \alpha_{0\to1}C_{out}V_{DD}^2f = 0.1875 * 12*10^{-15}*2^2*100*10^6=0.9*10^{-6}$ W = 0.9μW

Problem 2: Calculate the signal probabilities P1, P2 and activity factors a1, a2. Here a represents $\alpha_{0\to1}$. The values of P_x,P_y and P_z are given in the figure as ¼, ¾ and ½. (4 points)



Solution:

P_x= ¼, that makes $\overline{P_x} = \left(1 - \frac{1}{4}\right) = \frac{3}{4}$

Similarly, $\overline{P_y} = \left(1 - \frac{3}{4}\right) = \frac{1}{4}$

From the NOR truth table from Problem 1 solution, we find

$$P_1 = \overline{P_x}.\overline{P_y} = (3/4).(1/4) = 3/16 = 0.1875$$

$$\overline{P_1} = \left(1 - \frac{3}{16}\right) = \frac{13}{16}$$

$$a_1 = \overline{P_1}.P_1. = \frac{39}{256} = 0.1523$$

Now let's see a NAND truth table.

Q = A NAND B

Truth Table

Input A	Input B		Output Q
0	0		1
0	1		1
1	0		1
1	1		0

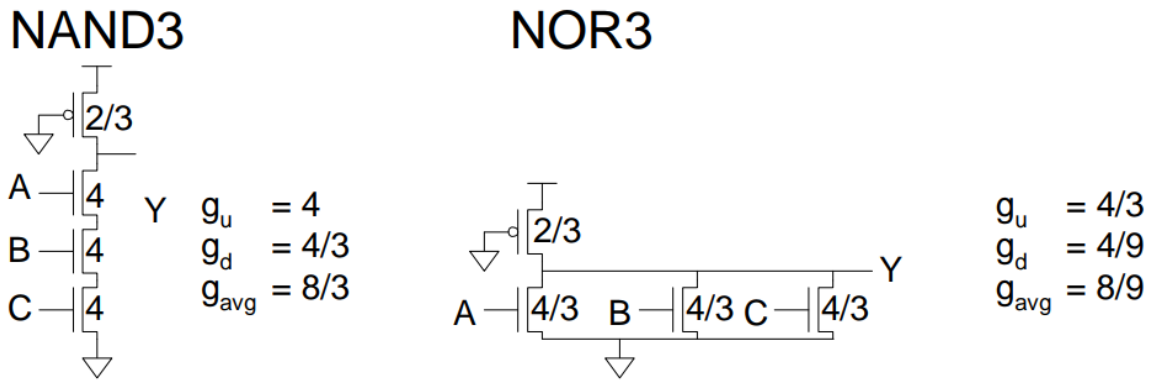
From the truth table, we see that $\overline{P_2}. = P_1.P_z = \left(\frac{3}{16}\right).\left(\frac{1}{2}\right) = \frac{3}{32}$

That makes P_2= 1-$\overline{P_2} = 1 - \frac{3}{32} = \frac{29}{32}$ = 0.9063

$a_2 = \overline{P_2}.P_2 = \frac{87}{1024}$ = 0.085

Problem 3: Sketch pseudo-nMOS 3-input NAND and NOR gates. Label the transistor widths so that it is equivalent to the pseudo-nMOS inverter shown in Lecture 7, slide 8. What are the rising, falling, and average logical efforts of each gate? (6 points)

Solution:

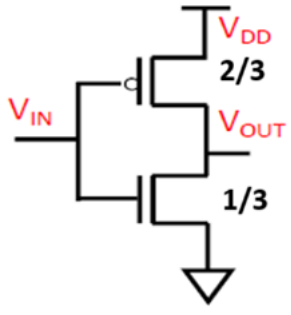


The inverter has nMOS aspect ration of 4/3, pMOS aspect ratio of 2/3. For both gates, pMOS aspect ratio remain the same. For nMOS aspect ratio, the calculation is following:

For NAND3:

R/k + R/k + R/k = R/(4/3), we get k=4.

To calculate g_u: we need to make an equivalent unskewed inverter with pMOS aspect ratio 2/3.



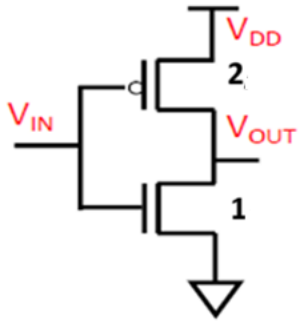
C_{in} = 4, C_{inv} = (1/3 + 2/3) =1

$g_u = C_{in}/C_{inv} = 4$

To calculate g_d: we need to calculate the current through nMOS, and then make an equivalent unskewed inverter.

Current through nMOS = 4I/3-I/3=I

So, the equivalent unskewed inverter looks like following:



$g_u = C_{in}/C_{inv} = 4/3$

$g_{avg} = 8/3$

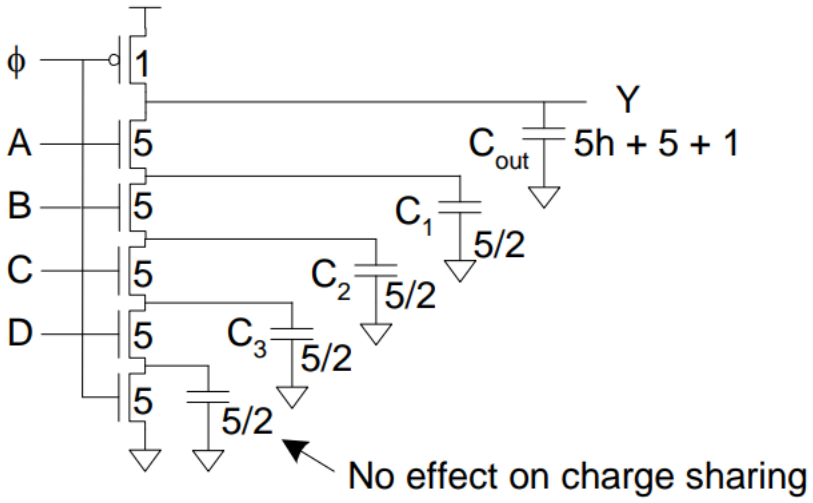
For NOR3:

R/k = R/(4/3), we get k=4/3

Using the same process as the NAND gate, $g_u = 4/3$, $g_d = 4/9$, $g_{avg} = 8/9$

Problem 4: Design a 4-input footed dynamic NAND gate driving an electrical effort of 1. Estimate the worst charge-sharing noise as a fraction of VDD assuming that diffusion capacitance on uncontacted nodes is about half of gate capacitance and on contacted nodes it equals gate capacitance. (5 points)

Solution: The worst case is when A is low on one cycle, B, C, and D are high, and all the internal nodes become predischarged to 0. Then D falls low during precharge. Then A goes high during evaluation. The NAND has 11 units of capacitance on C_{out} precharged to VDD and 7.5 units of internal capacitance (C_1, C_2, C_3) that will be initially low. The output will thus drop to 11/(11+7.5) VDD = 0.59 VDD.


ϕ
A
B
C
D
1
5
5
5
5
5
Y
C_{out}
5h + 5 + 1
C_1
5/2
C_2
5/2
C_3
5/2
5/2
No effect on charge sharing