MMU
MULTIMEDIA UNIVERSITY

TUTORIAL 3
LOGIC GATES

PDS0101: INTRODUCTION TO DIGITAL SYSTEMS
TRI 2, 2022-2023

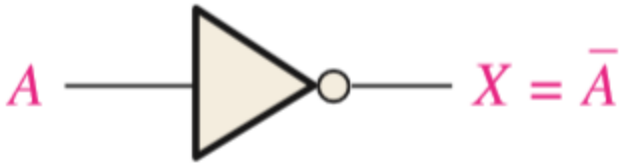
QUESTION 1

Draw the LOGIC SYMBOL and construct the TRUTH TABLES and TIMING DIAGRAM for the following gates showing all possible input combinations

LOGIC SYMBOL

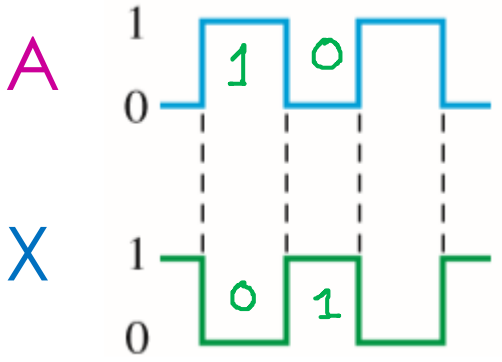
1-input inverter

2^n ← input $= 2^1 = 2$ < 1, 0



TRUTH TABLES

INPUT	OUTPUT	
A	$\bar{A}$	A′
0	1	
1	0	

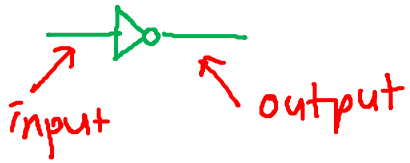


TIMING DIAGRAM

inverter

NOT

only ONE input



AND

OR

NAND

NOR

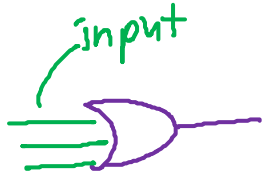
XOR

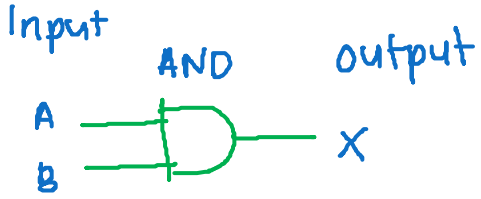
XNOR

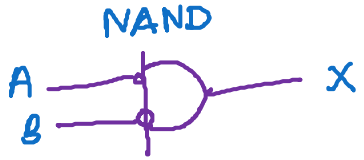
negative AND

negative OR

at least two input





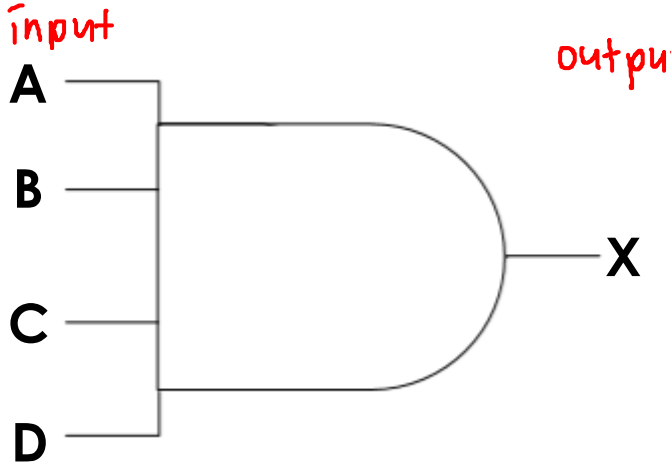


QUESTION 2

Draw the LOGIC SYMBOL and construct the TRUTH TABLES and TIMING DIAGRAM for the following gates showing all possible input combinations

LOGIC SYMBOL

4-input (quad input)AND gate

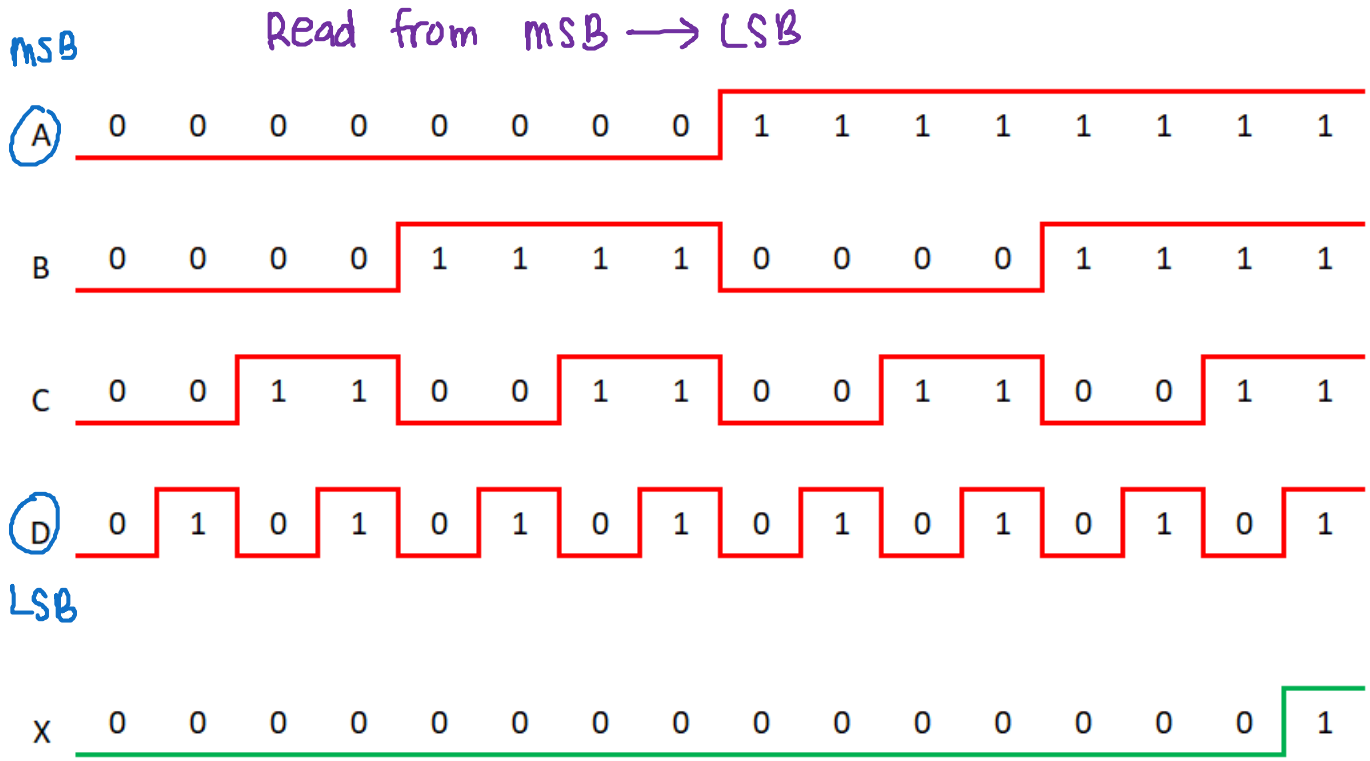


$2^n = 2^4 = 16$ possible input combination

Example : 0010 , 1101 , 0001

4-input (quad input)AND gate

INPUT				OUTPUT
A	B	C	D	X = ABCD
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



TIMING DIAGRAM

If ALL input ONE ;

output = ONE

6 input AND gate

Input | Output

11 111 → 1

111 101 → 0

011111 → 0

7 input AND gate

input | output

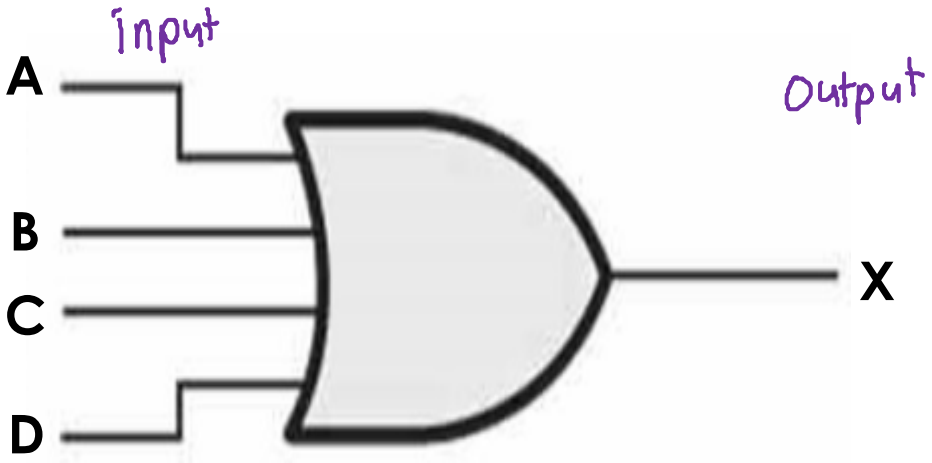
1111 1111 → 1

QUESTION 3

Draw the LOGIC SYMBOL and construct the TRUTH TABLES and TIMING DIAGRAM for the following gates showing all possible input combinations

LOGIC SYMBOL

4-input OR gate

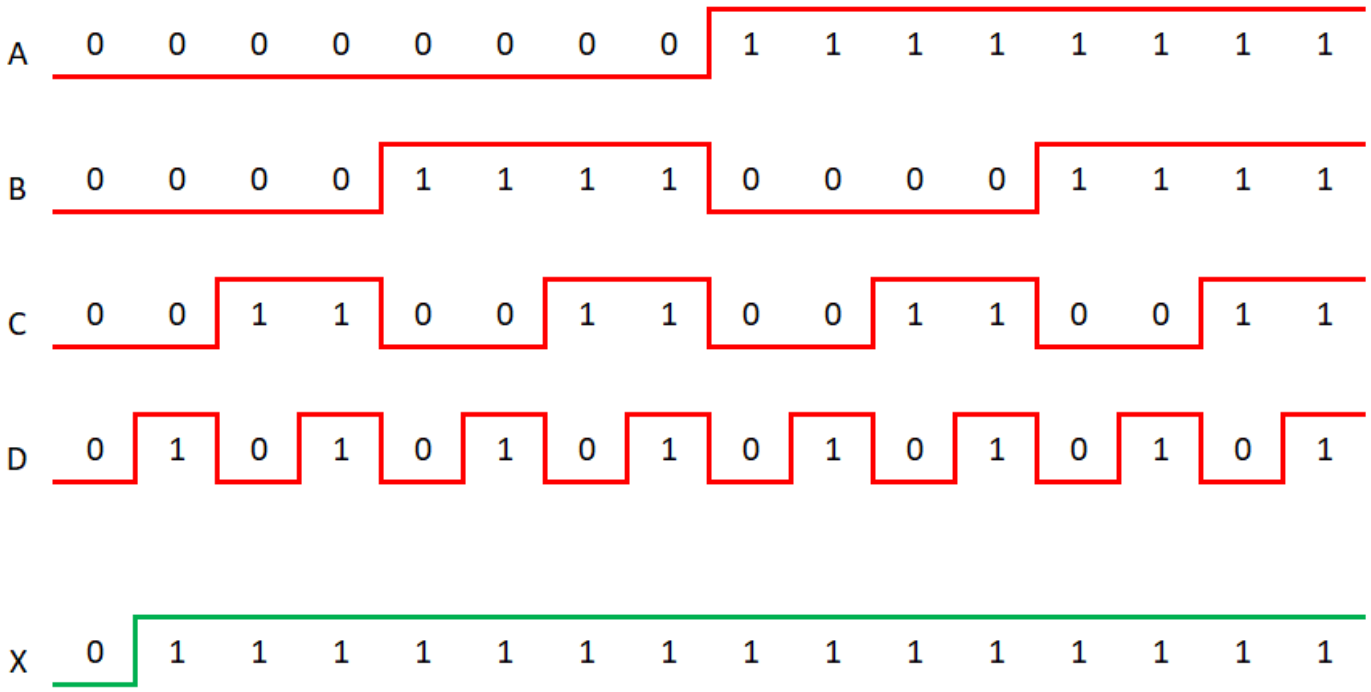


$2^n = 2^4 = 16$ possible input combination

Example : 0010 , 0011 , 1110 ,
Input 1111 , 1010, 0000 ...

4-input OR gate

TRUTH TABLES	INPUT			OUTPUT
A	B	C	D	X = A+B+C+D
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



TIMING DIAGRAM

If ALL input ZERO ;
output = ZERO

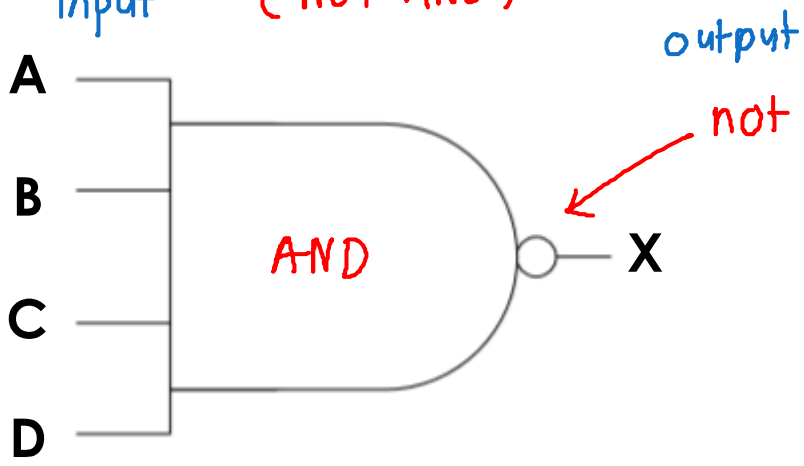
QUESTION 4

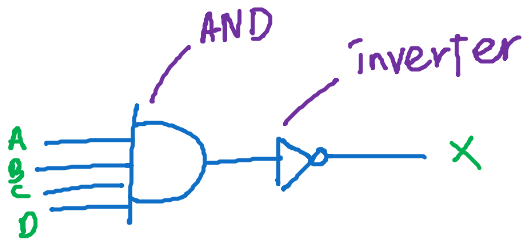
Draw the LOGIC SYMBOL and construct the TRUTH TABLES and TIMING DIAGRAM for the following gates showing all possible input combinations

LOGIC SYMBOL

4-input NAND gate

(NOT AND)

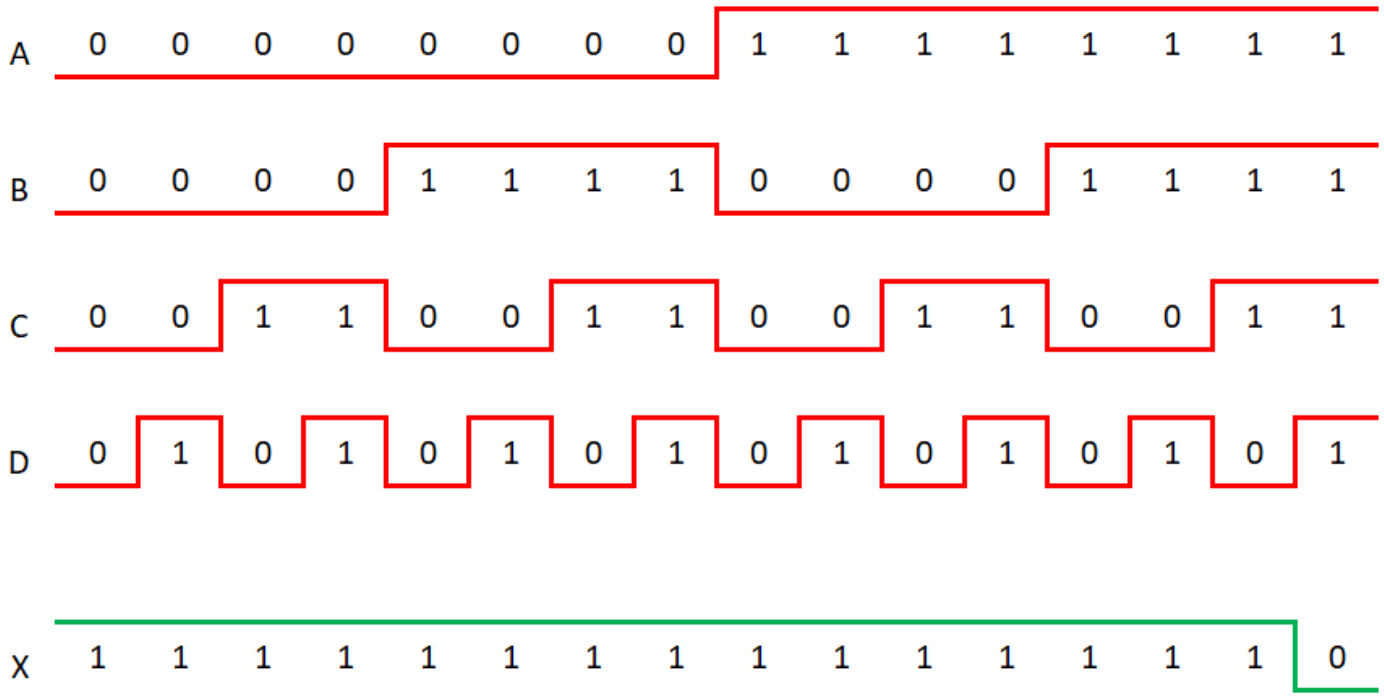




$2^n = 2^4 = 16$ possible input combination

4-input NAND gate

TRUTH TABLES	INPUT			OUTPUT
A	B	C	D	X = (ABCD)'
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



TIMING DIAGRAM

AND
If All input ONE, output ONE
invert
NAND (Not And)
If All input ONE, output ZERO

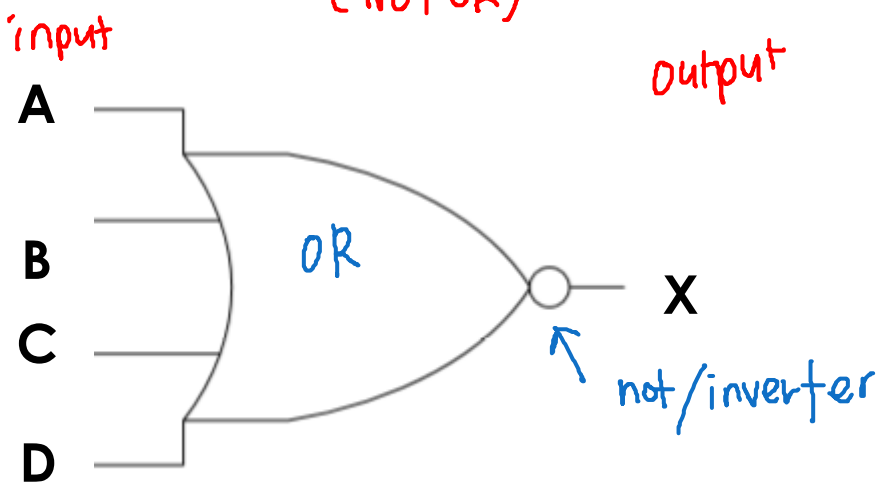
QUESTION 5

Draw the LOGIC SYMBOL and construct the TRUTH TABLES and TIMING DIAGRAM for the following gates showing all possible input combinations

LOGIC SYMBOL

4-input NOR gate

(NOT OR)

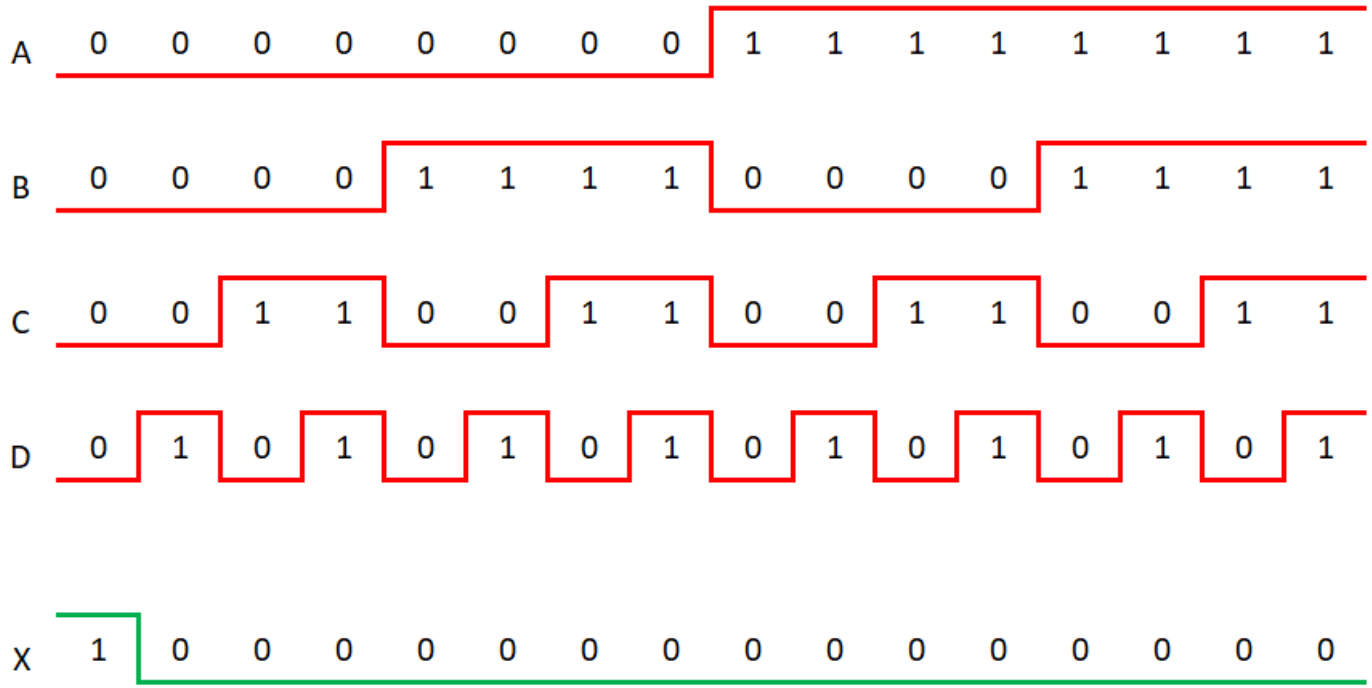


2^n ← input

$2^4 = 16$ possible input combination

TRUTH TABLES	INPUT			OUTPUT
A	B	C	D	$X = \overline{A+B+C+D}$
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

4-input NOR gate



TIMING DIAGRAM

OR $(A+B+C+D)$
if ALL input ZERO, output ZERO

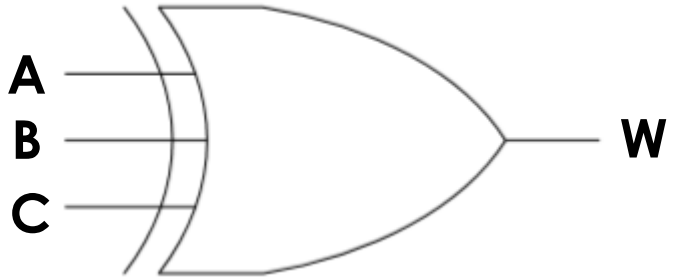
NOR $(\overline{A+B+C+D})$ ↓ invert
if ALL input ZERO; output ONE

QUESTION 6

Draw the LOGIC SYMBOL and construct the TRUTH TABLES for the following gates showing all possible input combinations

LOGIC SYMBOL

3-input XOR gate



$2^3 = 8$ possible input combination

total number of input high (one) is ODD number ; then output ; ONE

TRUTH TABLES

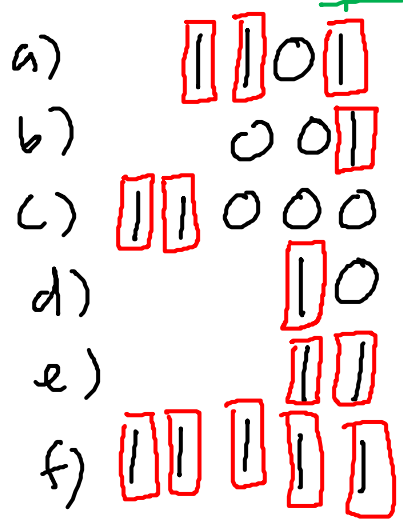
INPUT			OUTPUT
A	B	C	W = A⊕B⊕C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

XOR gate

1, 3, 5, 7 ....

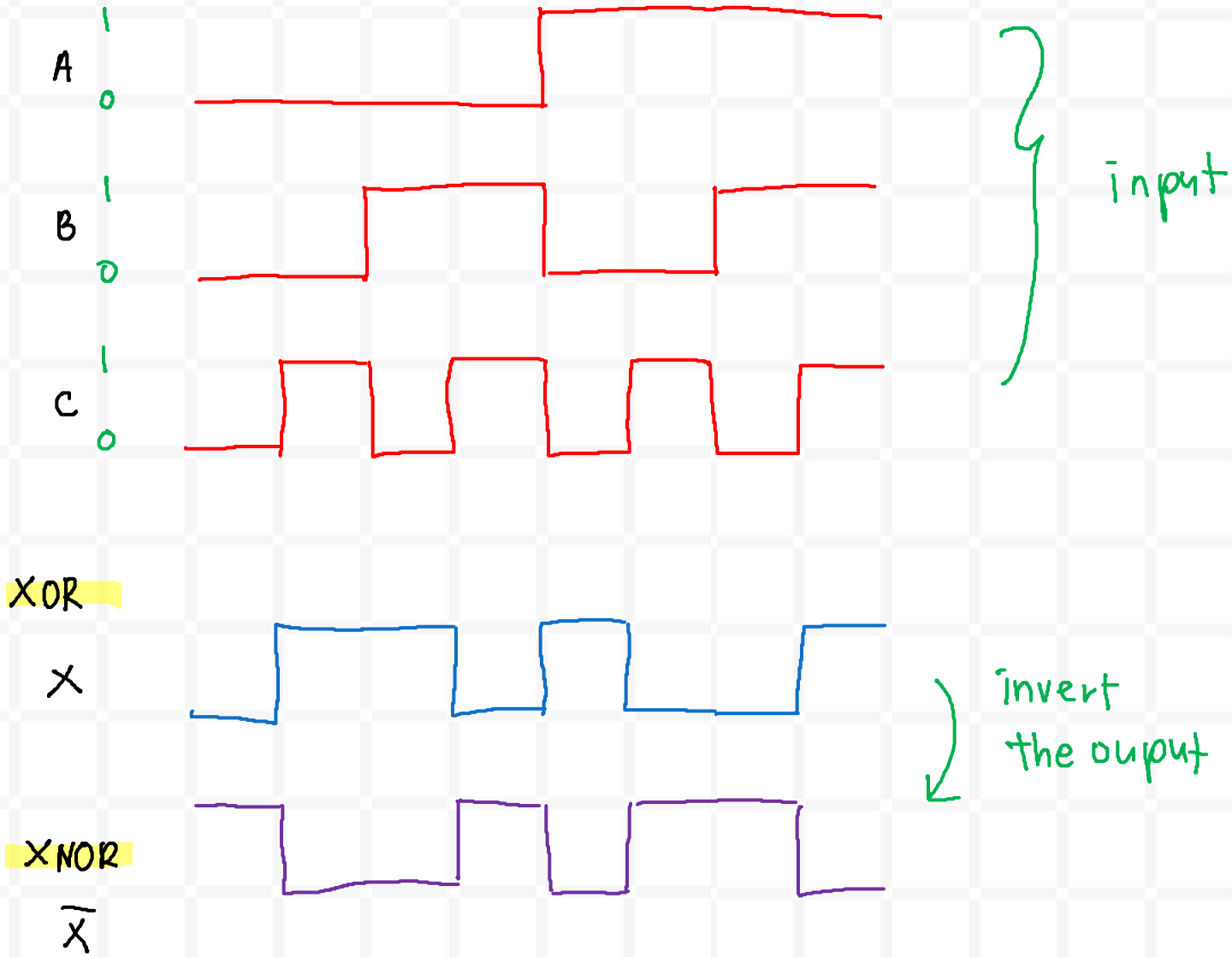
total number of input high (ONE) is ODD number, then OUTPUT = ONE

Example



total number of input high	XOR output	XNOR
3 input high	1	0
1 input high	1	0
2 input high	0	1
1 input high	1	0
2 input high	0	1
5 input high	1	0

TIMING DIAGRAM



QUESTION 7

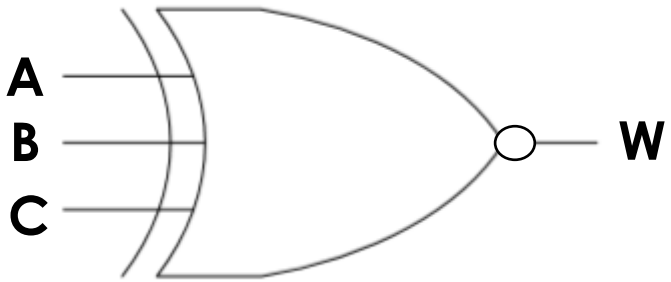
Draw the LOGIC SYMBOL and construct the TRUTH TABLES for the following gates showing all possible input combinations

$W = A \oplus B \oplus C$

$\bar{W} = \overline{A \oplus B \oplus C}$

LOGIC SYMBOL

3-input XNOR gate



$2^n = 2^3 = 8$ possible input combination

TRUTH TABLES

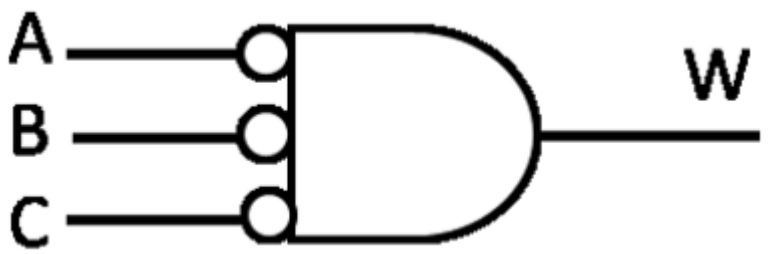
INPUT			XOR OUTPUT XNOR	
A	B	C	$W = A \oplus B \oplus C$	$\bar{W} = (A \oplus B \oplus C)'$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

QUESTION 10

Draw the LOGIC SYMBOL and construct the TRUTH TABLES for the following gates showing all possible input combinations

LOGIC SYMBOL

3-input negative-AND gate



If ALL input ONE, output = ONE

$\overline{ABC}$ X

$2^3 = 8$ possible input combination

TRUTH TABLES

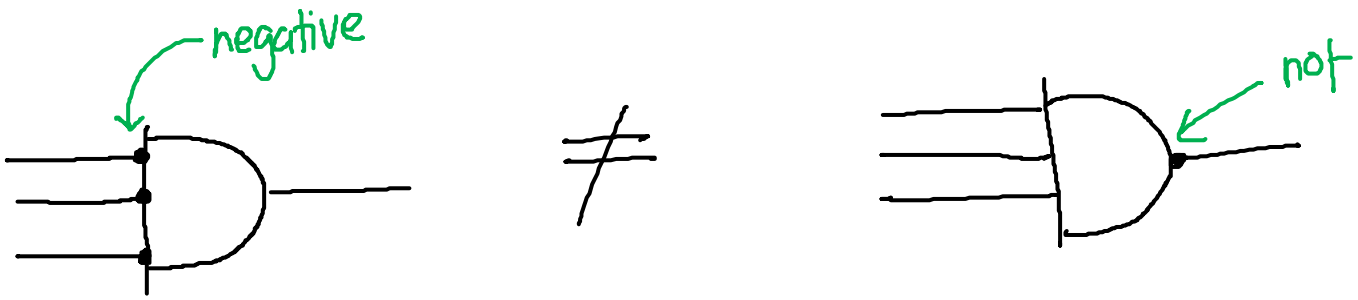
$\bar{A}\bar{B}\bar{C}$

INPUT						OUTPUT
A	B	C	A'	B'	C'	A'B'C'
0	0	0	1	1	1	1
0	0	1	1	1	0	0
0	1	0	1	0	1	0
0	1	1	1	0	0	0
1	0	0	0	1	1	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	0

Invert Invert Invert

negative AND gate $\neq$ NOT AND gate (NAND)

$\bar{A}\,\bar{B}\,\bar{C}$ $\neq$ $\overline{A\,B\,C}$



DeMorgan

negative AND gate = NOR gate (NOT OR)

$\bar{A}\bar{B}\bar{C}\bar{D} = \overline{A+B+C+D}$

QUESTION 10

3-input negative-AND gate equivalent with 3-input NOR gate

3-input negative-AND gate

TRUTH TABLES

$\bar{A}\bar{B}\bar{C} = \overline{A+B+C}$

INPUT			OUTPUT			
A	B	C	A'	B'	C'	A'B'C'
0	0	0	1	1	1	1
0	0	1	1	1	0	0
0	1	0	1	0	1	0
0	1	1	1	0	0	0
1	0	0	0	1	1	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	0

3-input NOR gate (NOT OR)

TRUTH TABLES

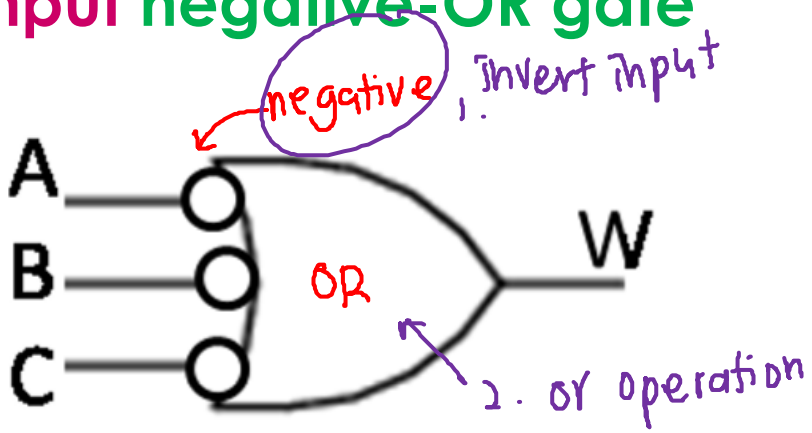
INPUT			OR OUTPUT NOR	
A	B	C	A+B+C	(A+B+C)'
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

QUESTION 11

Draw the LOGIC SYMBOL and construct the TRUTH TABLES for the following gates showing all possible input combinations

LOGIC SYMBOL

3-input negative-OR gate



$2^3 = 8$ possible input combination

TRUTH TABLES

INPUT						OUTPUT
A	B	C	A'	B'	C'	A'+B'+C'
0	0	0	1	1	1	1
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	1	0	0	1
1	0	0	0	1	1	1
1	0	1	0	1	0	1
1	1	0	0	0	1	1
1	1	1	0	0	0	0

QUESTION 11

3-input negative-OR gate equivalent with 3-input NAND gate

3-input negative-OR gate

TRUTH TABLES

$\bar{A}+\bar{B}+\bar{C} = \overline{ABC}$

INPUT			OUTPUT			
A	B	C	A'	B'	C'	A'+B'+C'
0	0	0	1	1	1	1
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	1	0	0	1
1	0	0	0	1	1	1
1	0	1	0	1	0	1
1	1	0	0	0	1	1
1	1	1	0	0	0	0

3-input NAND gate

TRUTH TABLES

INPUT			OUTPUT	
A	B	C	ABC	(ABC)'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

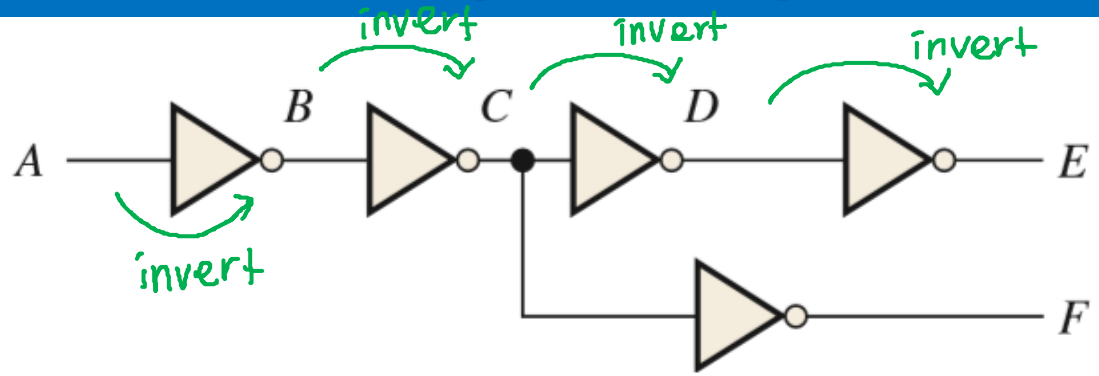
negative OR gate = NOT AND (NAND) gate

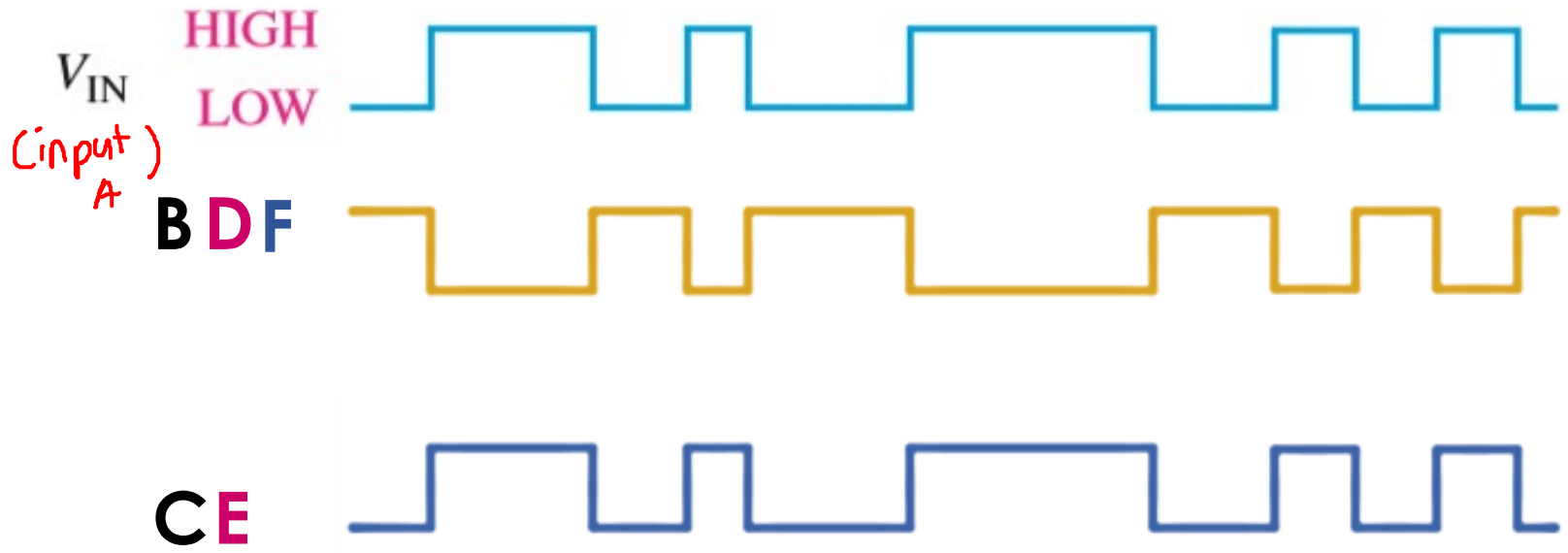
$\bar{A} + \bar{B} + \bar{C} + \bar{D} = \overline{ABCD}$

APPLIED KNOWLEDGE QUESTIONS 1

A series of cascaded inverters is shown in the figure below. Determine the logic level outputs at B, C, D and F if the Vin signal at A is given as shown.

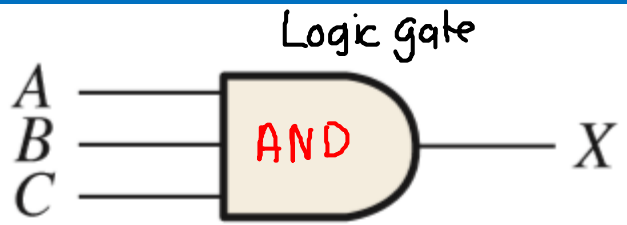
$\bar{\bar{A}} = A$





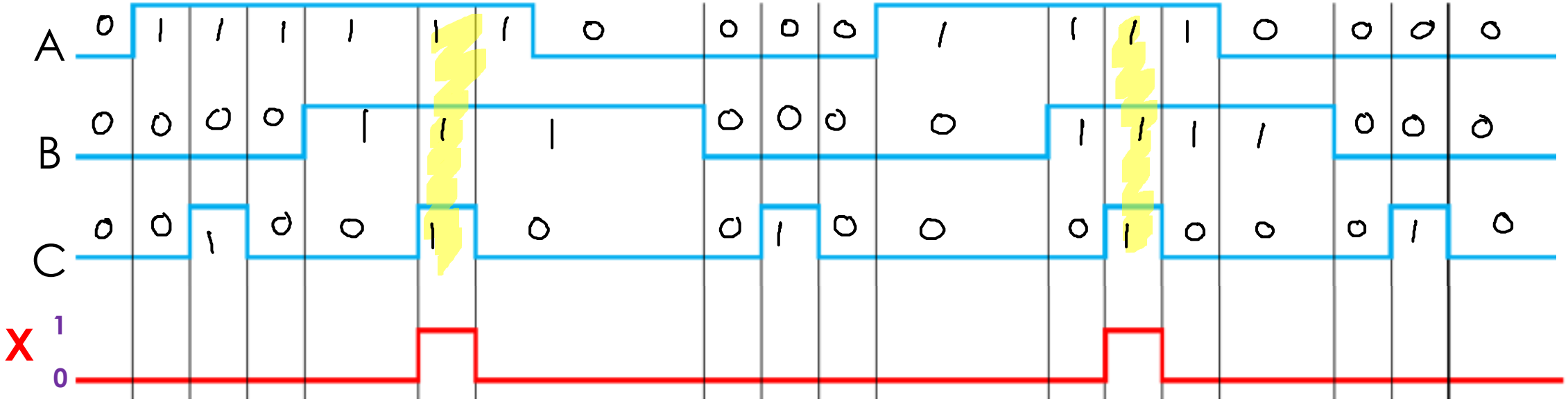
APPLIED KNOWLEDGE QUESTIONS 2 (i)

Determine the individual outputs of X to the tri-input gates below based on the timing diagrams shown for inputs A, B and C



If ALL input ONE, output = ONE

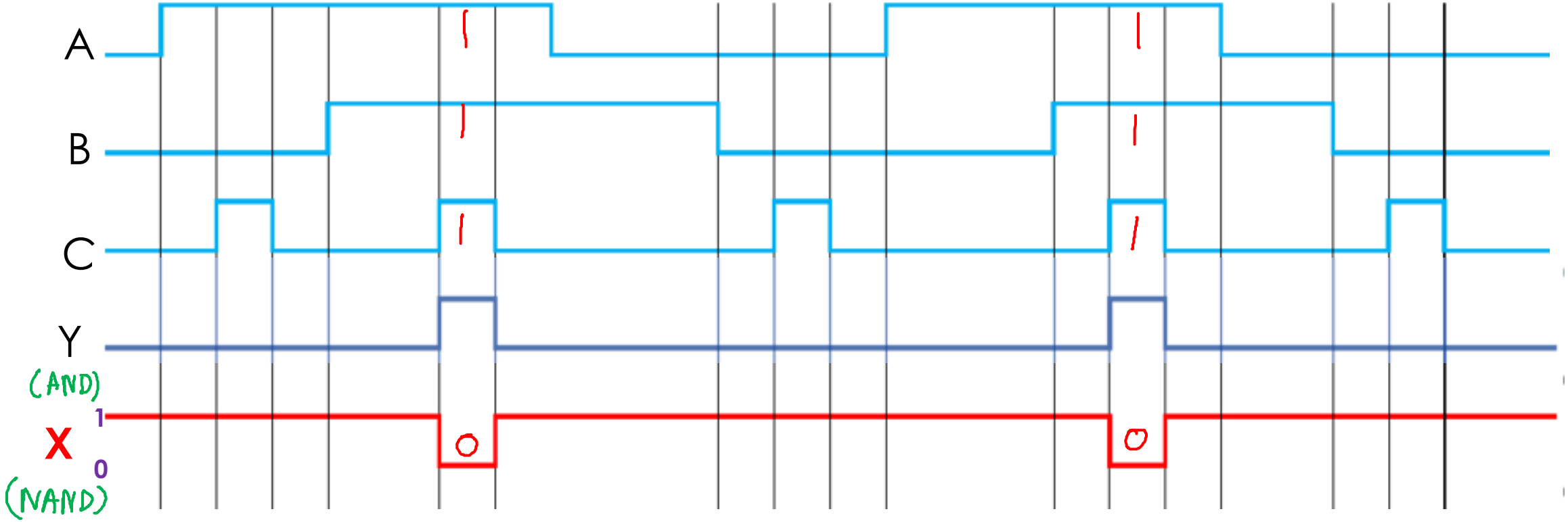
timing diagram



APPLIED KNOWLEDGE QUESTIONS 2 (ii)

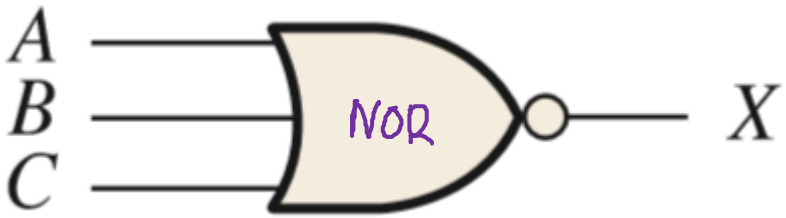
Determine the individual outputs of X to the tri-input gates below based on the timing diagrams shown for inputs A, B and C

AND
if All input ONE, output ONE → invert
NAND
if All input ONE, output ZERO

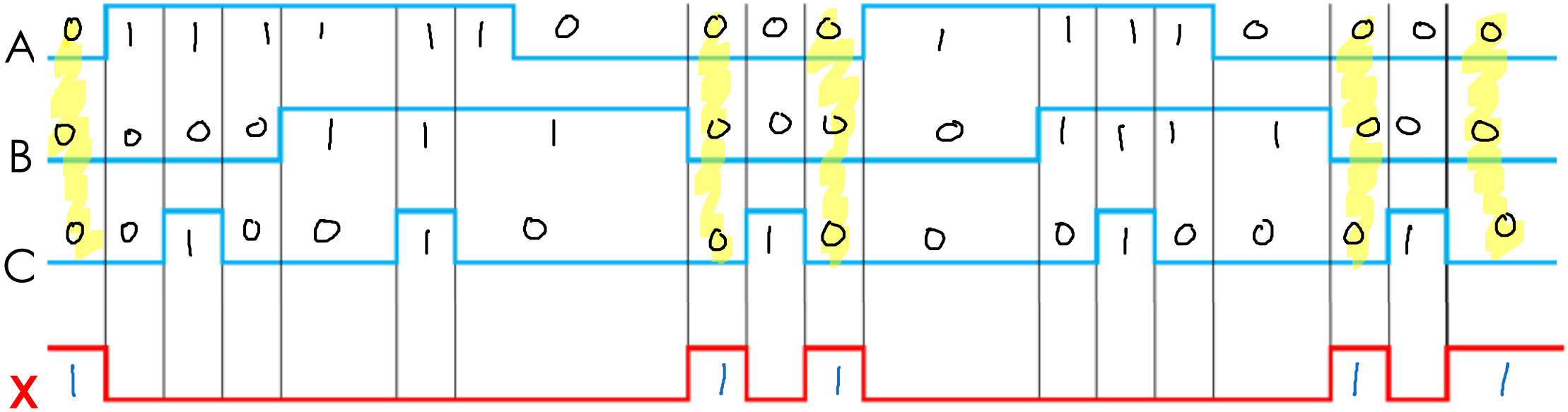


APPLIED KNOWLEDGE QUESTIONS 2 (iii)

Determine the individual outputs of X to the tri-input gates below based on the timing diagrams shown for inputs A, B and C

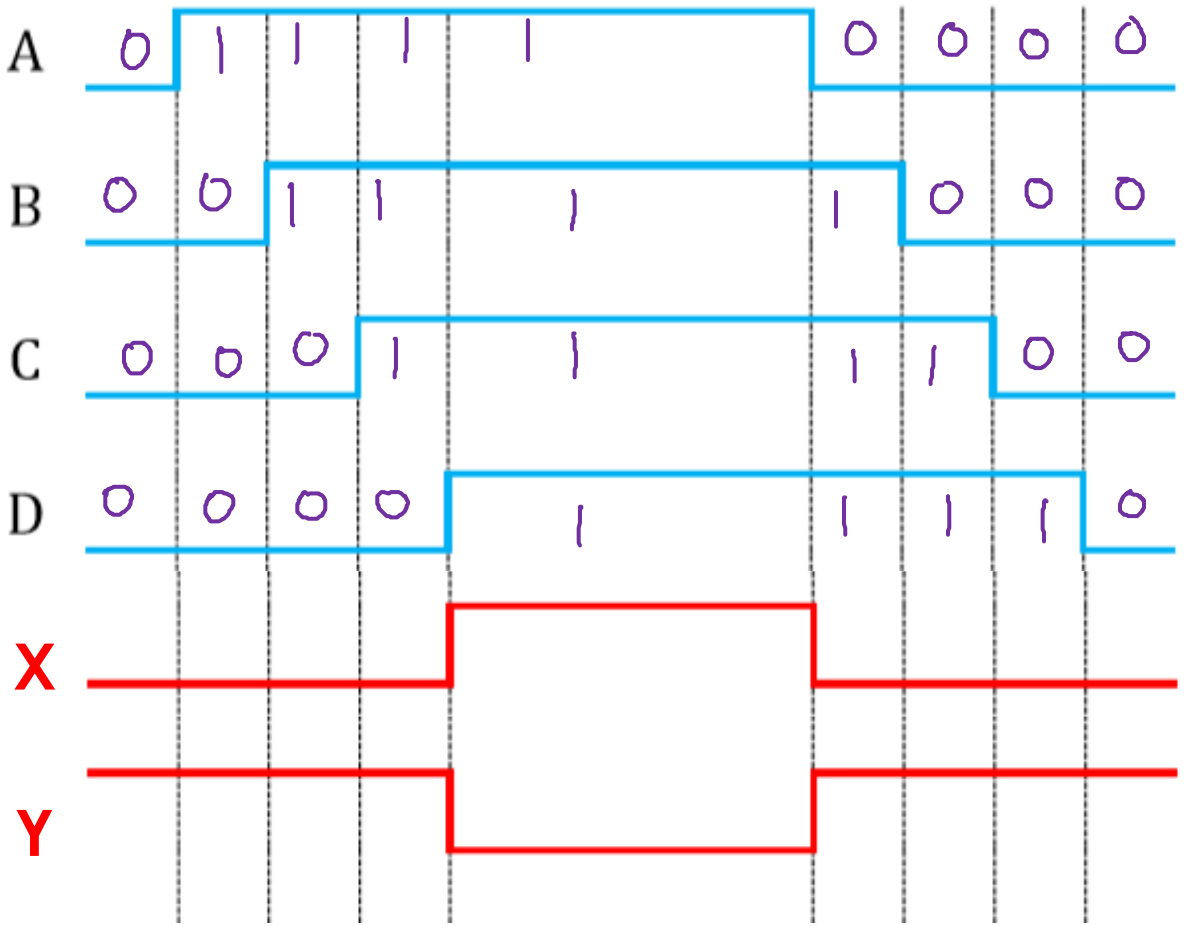


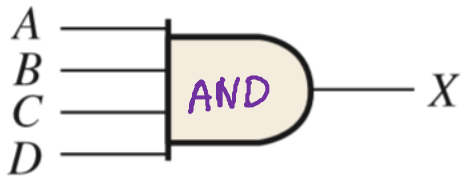
OR
IF All Input ZERO, output ZERO
↓ invert
NOR (NOT OR)
IF All Input ZERO, output ONE

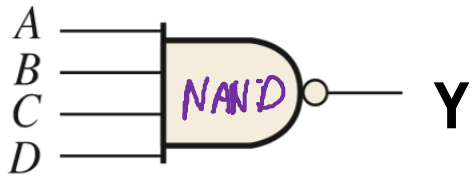


QUESTION 3 (i and ii)

Determine the individual outputs of X / Y to the quad-input gates below based on the timing diagrams shown for inputs A, B, C and D



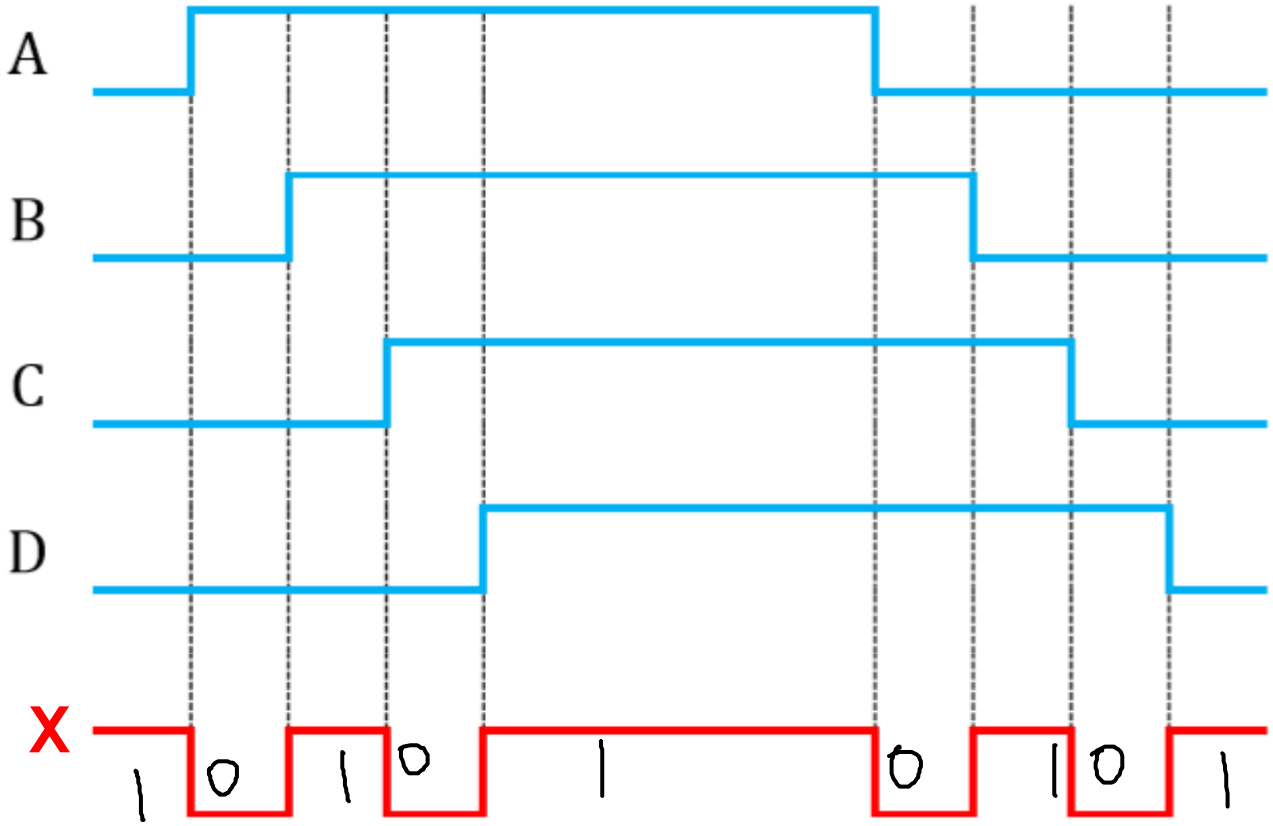


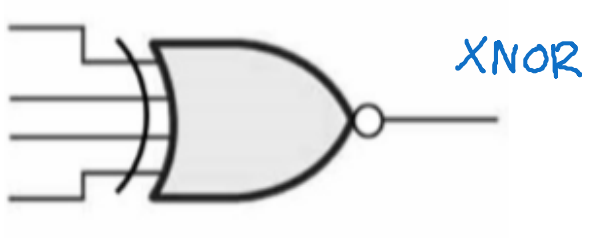


INPUT				OUTPUT	
A	B	C	D	X = ABCD	Y = X'
0	0	0	0	0	1
1	0	0	0	0	1
1	1	0	0	0	1
1	1	1	0	0	1
1	1	1	1	1	0
0	1	1	1	0	1
0	0	1	1	0	1
0	0	0	1	0	1
0	0	0	0	0	1

QUESTION 3 (iii)

Determine the individual outputs of X / Y to the quad-input gates below based on the timing diagrams shown for inputs A, B, C and D



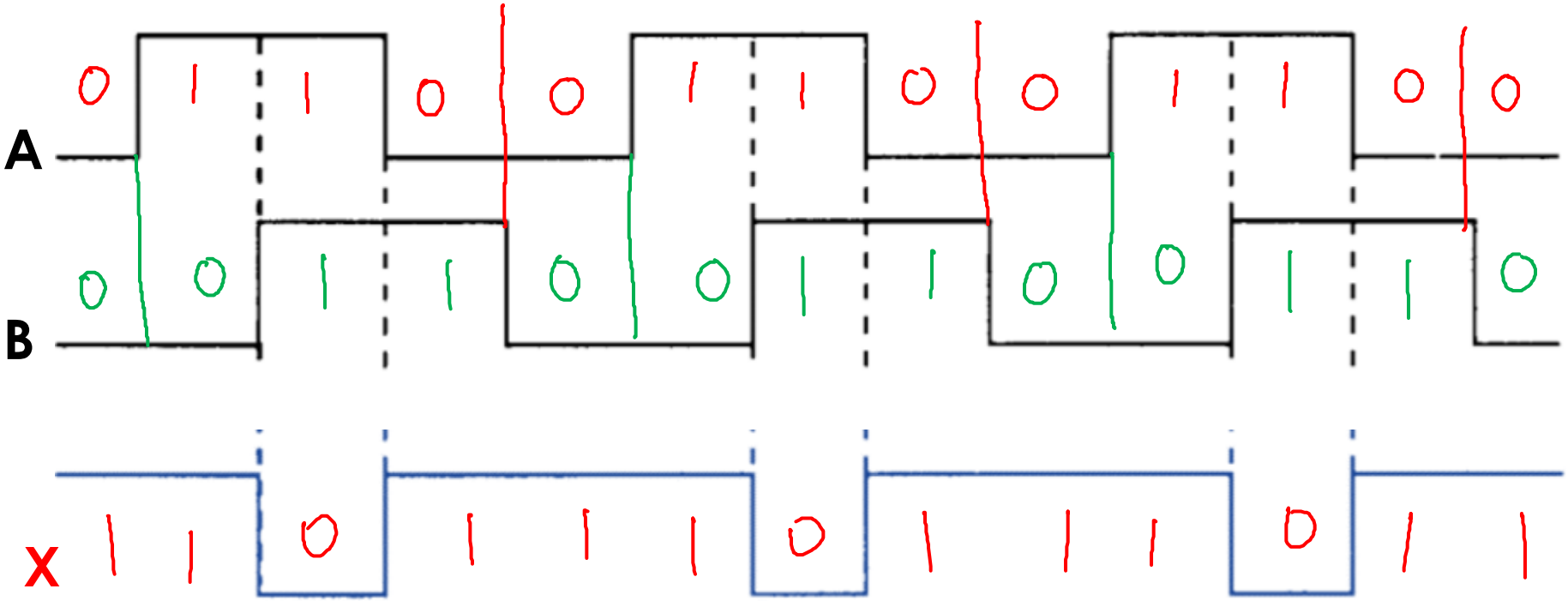


INPUT				XOR OUTPUT XNOR	
A	B	C	D	Y = A⊕B⊕C⊕D	X = Y'
0	0	0	0	0	1
1	0	0	0	1	0
1	1	0	0	0	1
1	1	1	0	1	0
1	1	1	1	0	1
0	1	1	1	1	0
0	0	1	1	0	1
0	0	0	1	1	0
0	0	0	0	0	1

QUESTION 4

Complete the timing diagram for the two gates below based on the inputs A and B shown. What conclusions can you derive from the output of the gates?

INPUT		OUTPUT	
A	B	X=(AB)'	X=A'+ B'
0	0	1	1
1	0	1	1
1	1	0	0
0	1	1	1



Conclusion :

input < A, B

$2^n = 2^2 = 4$ possible input combination

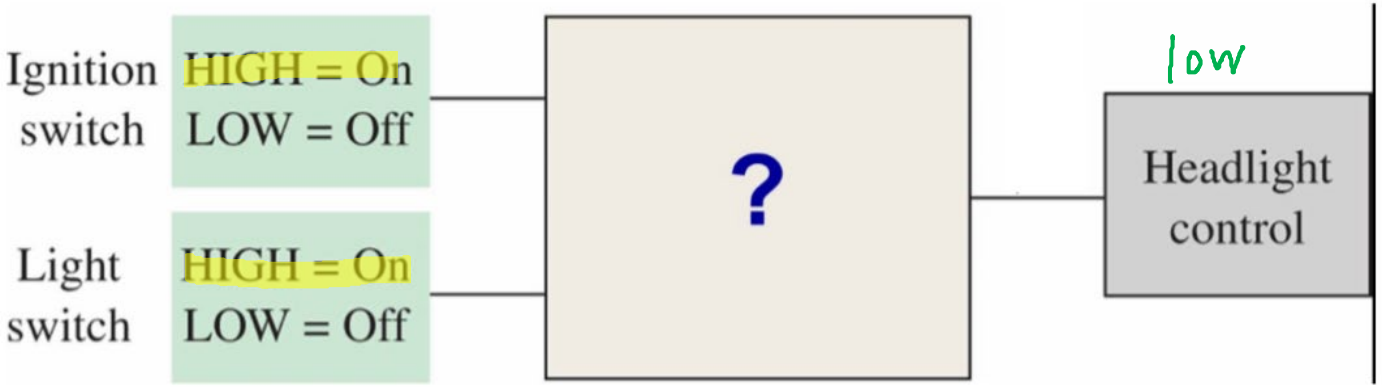
NAND gate — negative OR

A	B	AB	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	0	1	1	1	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0
0	1	0	1	1	0	1

$\overline{AB} = \overline{A}+\overline{B}$

QUESTION 5

The headlights of a car only turn on (light up) when the car's ignition is turned ON with the key and the headlight switch is turned ON. Assuming that the headlight requires a LOW signal to turn it ON, what gate would be suitable to fit in the blank below to complete the circuit? Explain your answer.



Input
1 1

Output
→ 0

NAND gate
Negative OR

Both inputs need to be **high (ON)** to activate its output. (**AND gate**)
The headlight is activated upon a **LOW signal**, inverse of the output.
Hence the **NAND gate** is used. (optional **negative-OR**)

END DISCUSSIONS

ANY QUESTIONS ??