MULTIMEDIA UNIVERSITY

PDS0101 Introduction to Digital Systems

Tutorial 8

Tutorial outcomes

By the end of today's tutorial, you should be able to

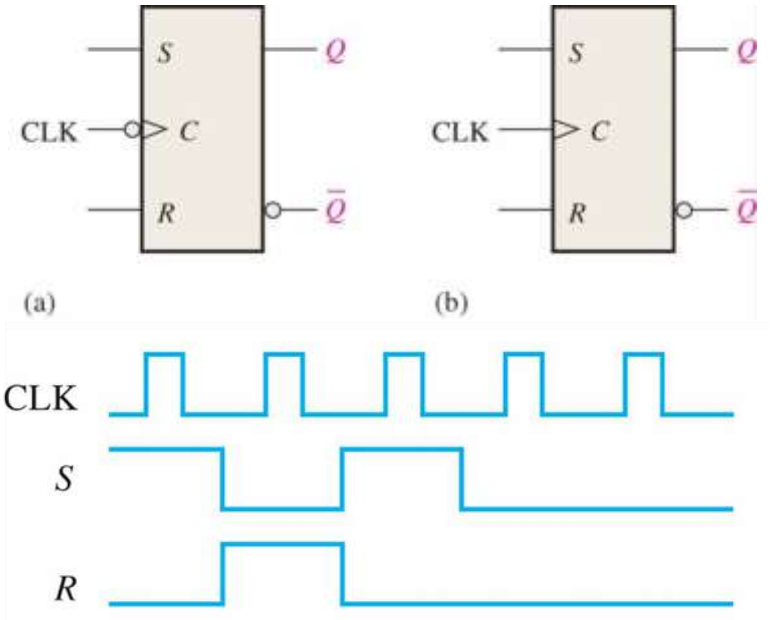
- recognize the difference between latches and flip-flops
- explain how ET S-R, D and J-K flip-flops work
- identify ET flip-flops by its symbols
- distinguish between positive and negative ET FFs

Theory based questions

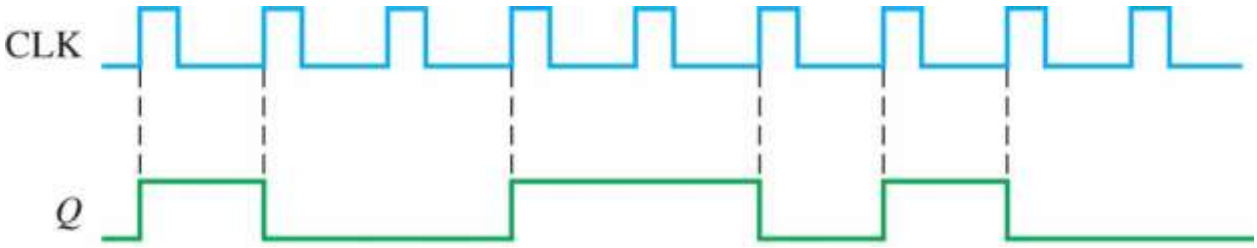
1. Draw the logic symbols for positive going edge-triggered S-R, D and J-K flip-flops
2. Draw the logic symbols for negative going edge-triggered S-R, D and J-K flip-flops
3. How does the J-K flip-flop avoid having any invalid state outputs?
4. How does the D flip-flop avoid having any invalid state outputs?
5. What are the differences/similarities between a J-K and D flip-flop?

Applied knowledge based questions

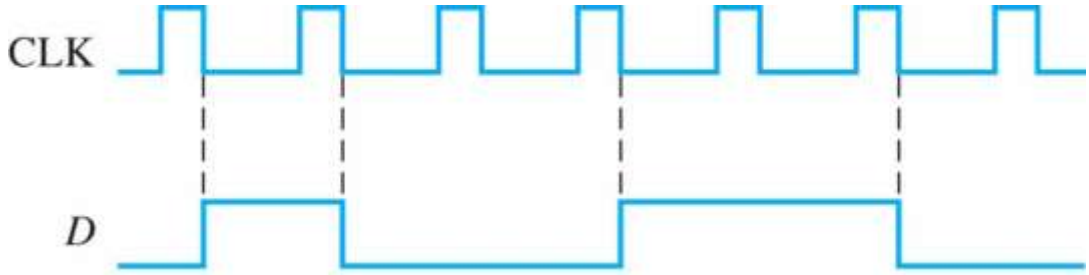
1. Identify the two flip-flops shown below and draw their respective timing diagrams for their Q outputs based on the inputs shown. The FF are initially RESET.



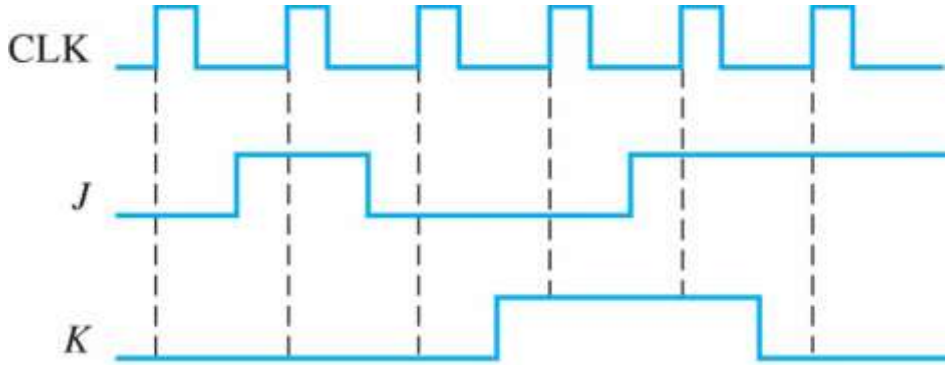
2. The Q output of a positive going ET S-R flip-flop is shown in the timing diagram below. Determine the correct inputs to S and R that are required to produce the this output.



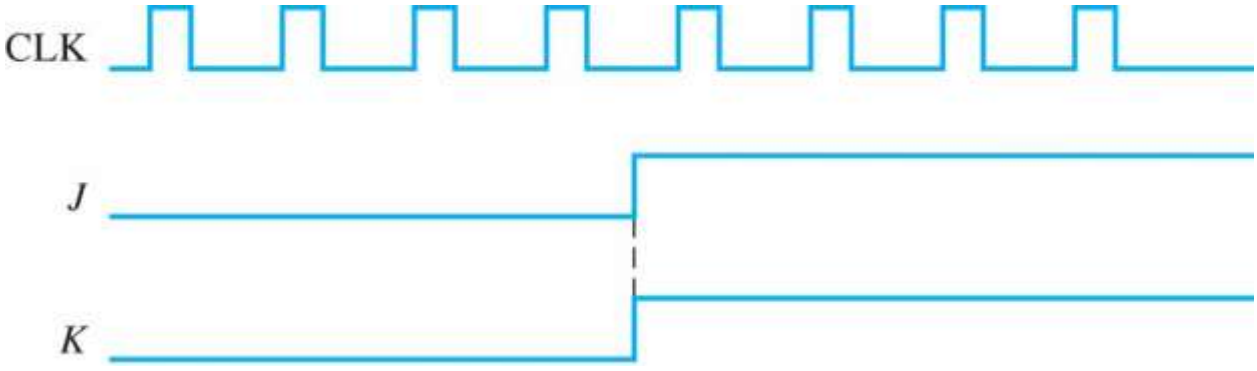
3. Draw the Q output of the a D flip-flop with the inputs shown in the timing diagram below. You may assume that the FF is positive going triggered and Q is initially LOW



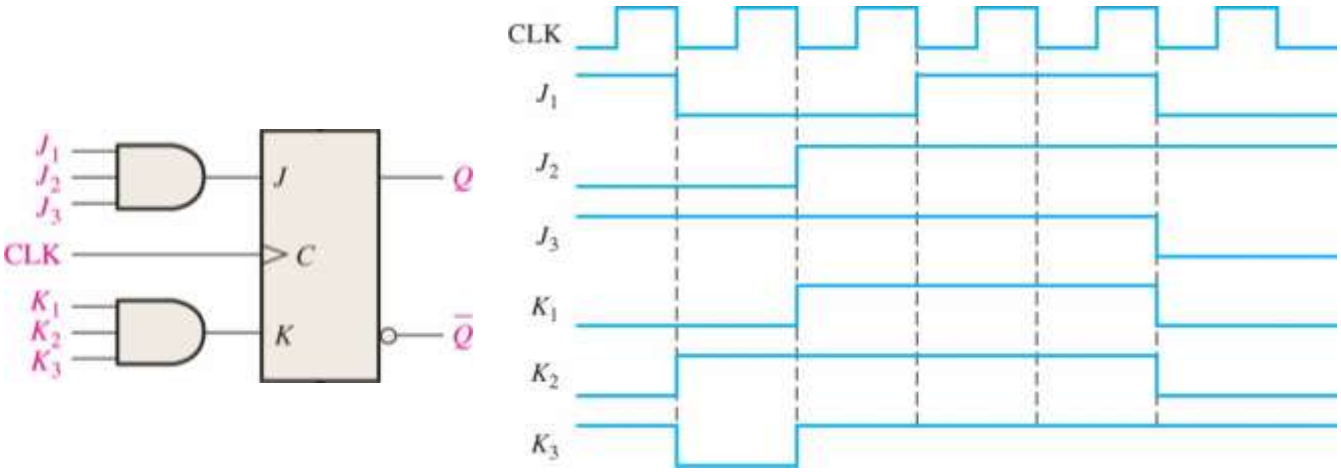
4. For a positive going ET J-K flip-flop with inputs as shown below, determine the Q output relative to the CLK assuming that Q starts out LOW



5. With the same conditions from (4), determine the Q output with the following inputs



6. For the circuit shown below, determine the output of Q (which starts out LOW) based on the inputs shown the in the timing diagram



7. For a negative going ET J-K FF with the inputs shown below, determine the Q output waveform relative to the CLK if Q is initially RESET