MULTIMEDIA UNIVERSITY

PDS0101 Introduction to Digital Systems

Tutorial 1

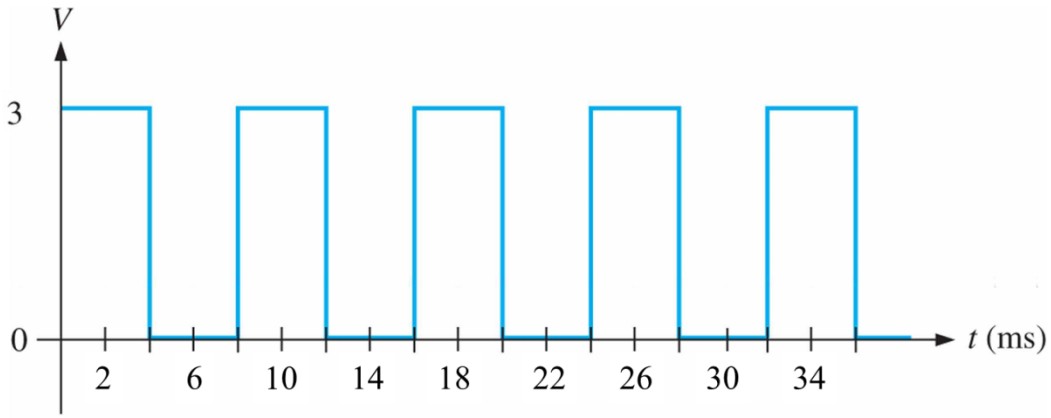
Tutorial outcomes

By the end of today's lab, you should be able to

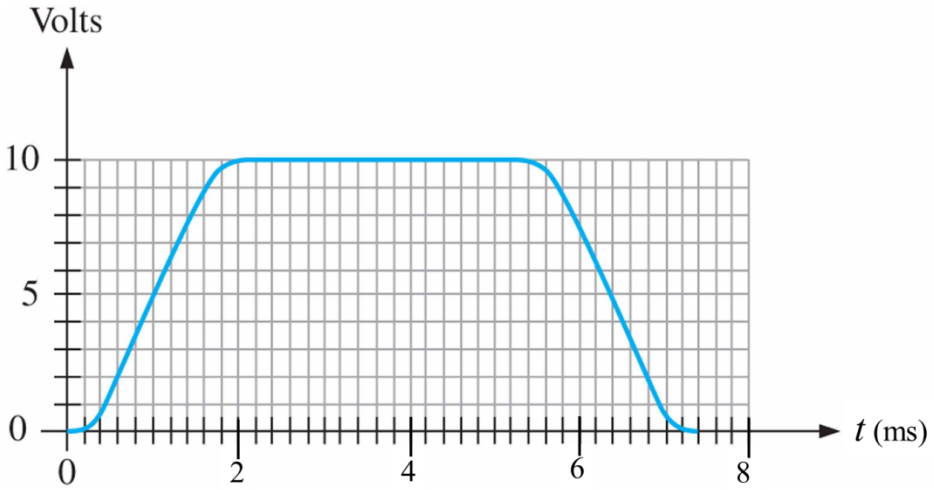
- identify differences between digital and analog quantities
- show how voltage levels can be used to represent digital quantities
- describe various waveform properties

Theory based questions

Identify and indicate the amplitude, period and pulse width components in the timing diagram below and their respective values.



Identify and indicate the amplitude, period, rise time, fall time and pulse width components in the timing diagram below and their respective values.



Knowing the period of a periodic waveform, how do you find the frequency?

What is the meaning of the term *binary*?

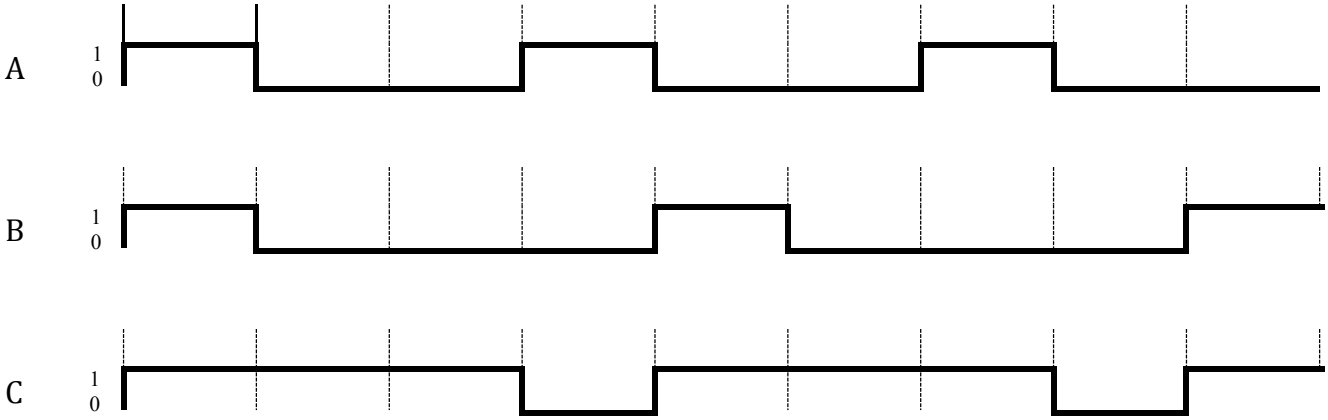
Define the following storage words in terms of its capacity

a) bit
b) byte
c) tayste
d) nybble
e) kilobyte
f) word
g) doubleword
h) playte
i) dynner

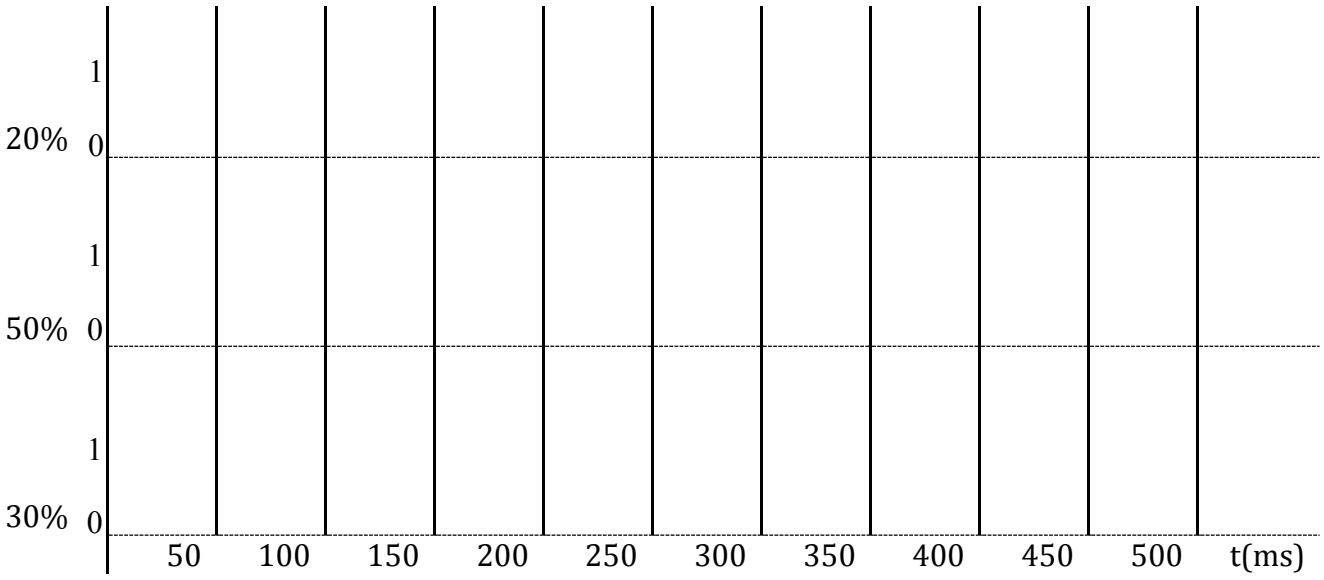
What are the advantages and disadvantages of the digital domain over analog?

Applied knowledge questions

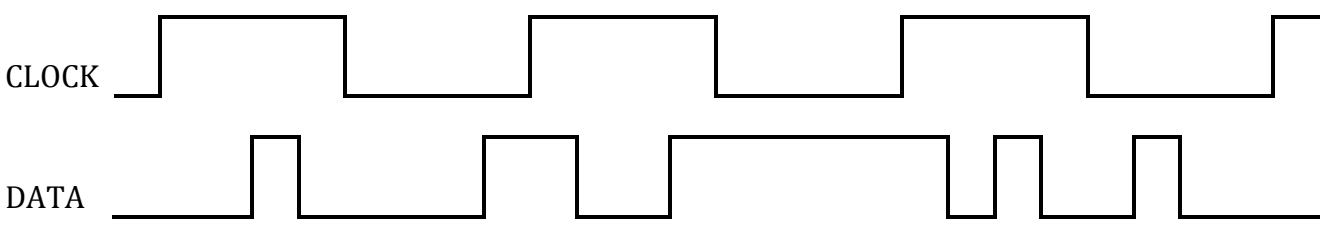
Identify the pulse width and period then calculate the *duty cycle* of the signals in the timing diagram shown below



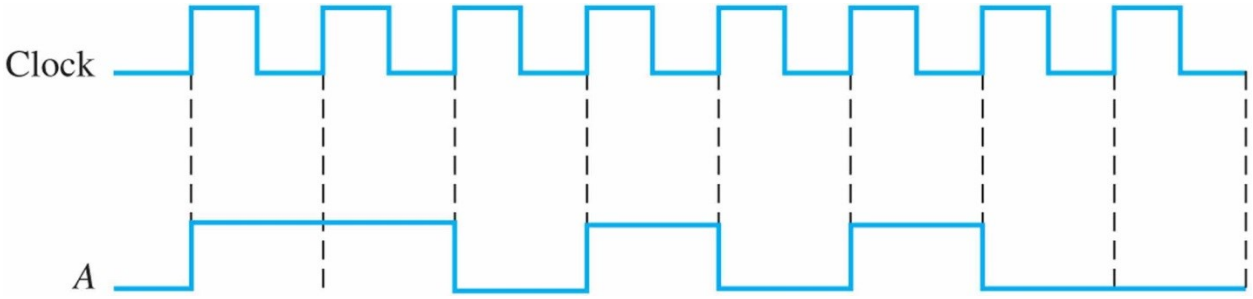
If given the frequency of a periodic signal is at 4Hz, use the following timing diagram scale to draw a signal when the duty cycle is at (a) 20%, (b) 50% and (c)30%



If binary data is transferred on a USB2.0 connection at a rate of 480Mbps, how long will it take (in theory) to transfer 4MB of data?

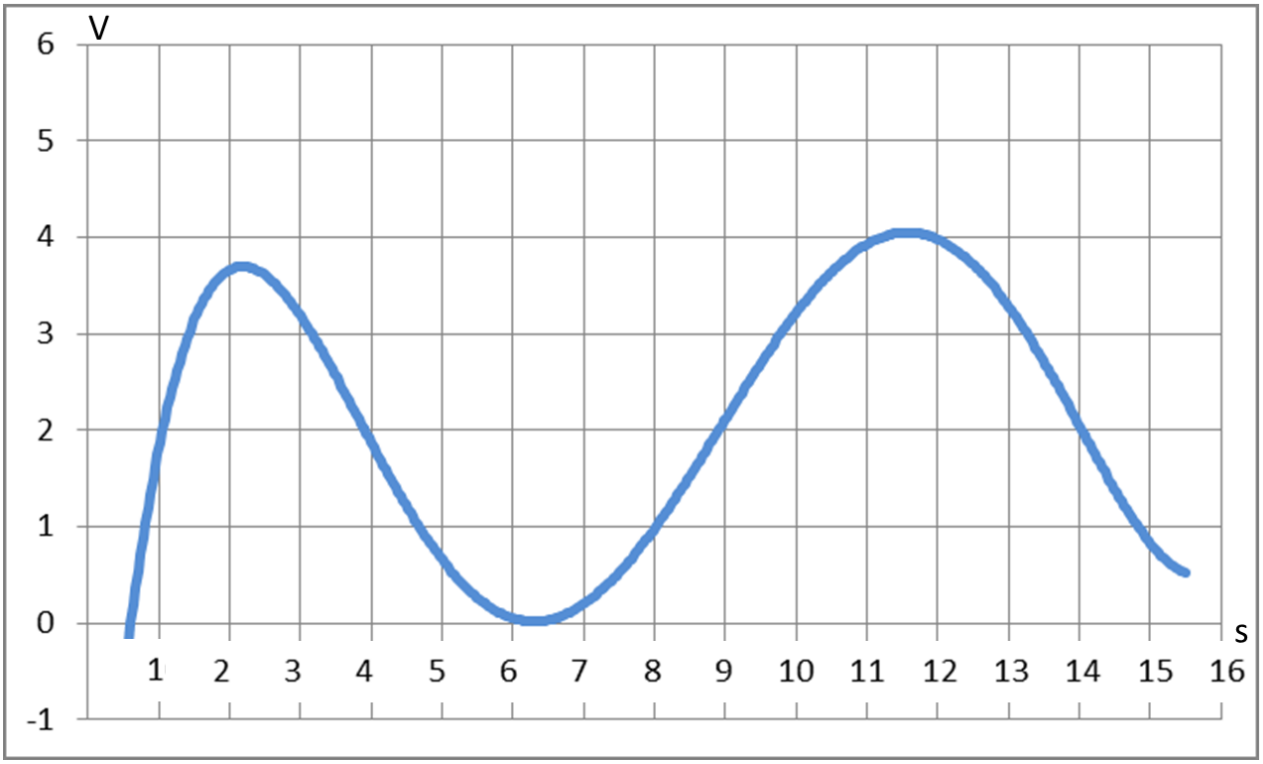


Using the timing diagram above, what is the bit sequence transmitted above if given that the sampling is done upon the *rising edge* of the clock signal



Based on the waveform above, determine

- The bit time if given the reference clock is running at 500Hz
- The bit sequence transferred by A
- The total time to transfer the bits serially
- The total time to transfer the same bits in parallel



The waveform diagram above shows a recorded analog signal of voltage against time in seconds. Draw the resulting binary digital waveform assuming that an ADC samples this signal once (1) every second at the rising edge of its clock signal and given that TTL levels for high are between 2-4V and low between 0-1V. It can be assumed that any values in the *unacceptable range* fall to low.
