LAB A-06 (Week 7) Construction and Implementation of Flip-flops, Counters, and Shift Registers

Objectives

a. To get familiarity with the flip-flops, asynchronous counters, and shift registers by the construction of the circuit and studying the operation.

b. To design and construct the synchronous counter and verify the counting sequence.

Tasks

1. a. Verify the function table for 7476 Dual Negative Edge Triggered JK Flip-flop

   b. Construct the following flip-flops using JK Flip-Flop andverify their truth tables

   - D (Data) Flip-Flop
   - T (Toggle) Flip-Flop

2. Design a 2-bit synchronous counter that can go through the following sequence in binary.

   1, 3, 2, 0 and repeat

   Use J-K Flip-flops for the design. Verify your design experimentally.

3. Construct and explain the operation of the following ripple counters with positive edge triggered D Flip-flops.

   - 4 bit binary asynchronous UP counter
   - 4 bit binary asynchronous DOWN counter
   - Asynchronous BCD Counter
   - Asynchronous MOD-12 Counter
   - Ripple divide by 14 Counter

4. Design and Construct a parallel counter that has the following sequence.
   If the input (UP)/(DOWN)' = 1, it will count up, 000-010-100-110 and then recycle to 000
   If the input (UP)/(DOWN)' = 0, it will count down, 110-100-010-000 and then recycle to 110.
   Undesired states are don't care states.

   (i) Use T flip-flops for the design.
   (ii) Use D flip-flops for the design.

Report Format

Show all steps for each question and be self explanatory.

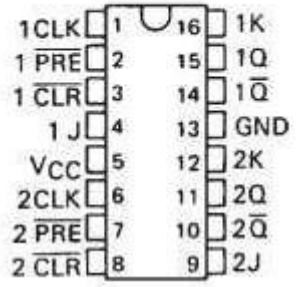
Assessment:

Total marks = 20/10=2%

Construction/Connections of the Circuit and Result during lab session= Tutor to pick questions for students to do and submit via CircuitVerse = 10 marks,
Report =5 Questions × 2 marks = 10 marks

Pin Configurations:

SN5476, SN54LS76A . . . J PACKAGE
SN7476 . . . N PACKAGE
SN74LS76A . . . D OR N PACKAGE
(TOP VIEW)



'LS76A
FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

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