MULTIMEDIA UNIVERSITY

PDS0101 Introduction to Digital Systems

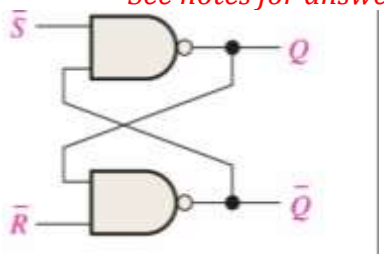
Tutorial 7 SAMPLE SOLUTIONS

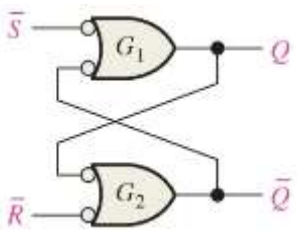
NOTE

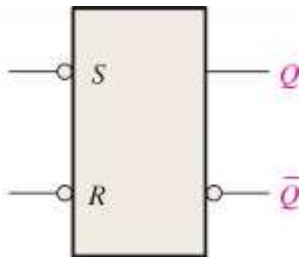
Answers shown may be only one of many possibilities available. Please approach your tutor if you have an alternative answer of which you are not sure of. Any errors and omissions in the answers are deeply regretted.

Theory based questions

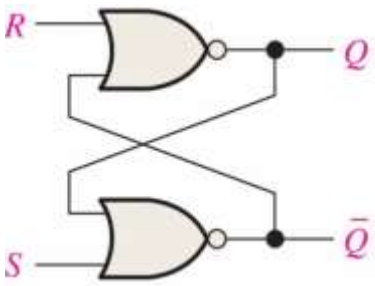
1. What are the differences between combinational and sequential circuits?
   Combinational logic refers to circuits whose output is a function of the present value of the inputs only. As soon as inputs are changed, the information about the previous inputs is lost, that is, combinational logic circuits have no memory
   Sequential logic current output values depend on current input and past state values (input and/or output). Thus the output of a sequential circuit may depend upon its previous outputs and so in effect has some form of "memory"
   Both combinational and sequential circuits remain built up from basic logic gates and apply the same design techniques.
2. How many 'states' can a S-R latch transition into?
   4 – resting/stable, set, reset and invalid/meta-stable
3. Draw the logic circuit and block diagram for an active-LOW S-R latch – show the alternatives possible in the logic circuit diagram
   - What is an alternative name for the active-LOW S-R latch? *NAND S-R latch / negative-OR S-R latch*
   - Complete the truth table for the active-LOW S-R latch
     See notes for answer

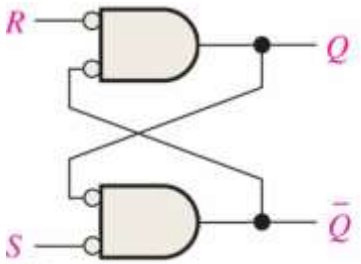


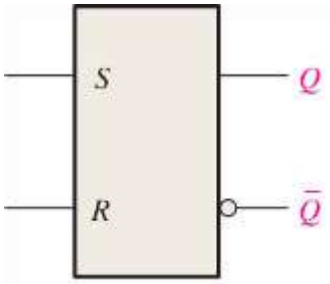




4. Draw the logic circuit and block diagram for an active-HIGH S-R latch – show the alternatives possible in the logic circuit diagram
   - What is an alternative name for the active-HIGH S-R latch? *NOR S-R latch / negative AND S-R latch*
   - Complete the truth table for the active-HIGH S-R latch
     See notes for answer



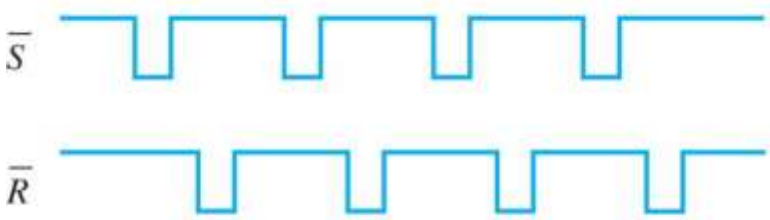




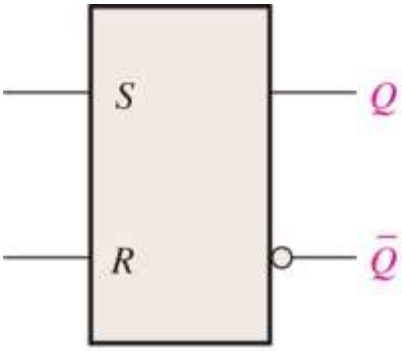
5. Explain how an active-LOW S-R latch transitions from resting/stable state into set state and then into reset state.
   See notes for answer
6. What happens when both inputs to the NAND S-R latch are set to HIGH?
   NAND S-R latch is active LOW. When both inputs are set to HIGH, the latch remains in rest state and retains the outputs is was generating
7. What happens when both inputs to the negative-AND S-R latch are set to HIGH?
   Negative-AND S-R latch is active HIGH. When both inputs are set high, the latch will attempt to generate a 1 (high) output for Q and Q' which goes against the nature of the complemented outputs thus resulting in an invalid state
8. Why is it not possible for a gated D-latch to fall into an invalid state?
   The input to a gated D latch are always opposed to each other thus making it not possible to achieve both HIGH (or LOW depending on latch type) inputs which may possibly result in an invalid state

Applied-knowledge based questions

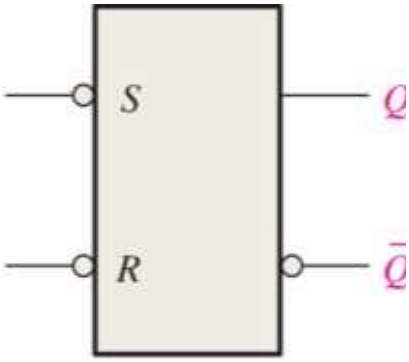
1. The waveforms in the timing diagram are applied to the latches shown below. Draw the resulting output waveform at Q in relation to the inputs assuming that Q starts low.

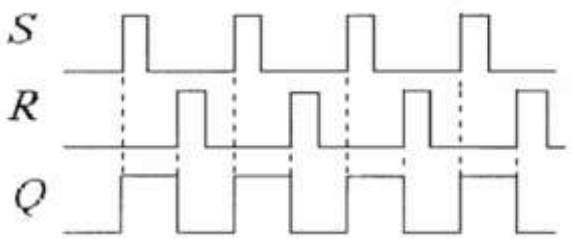


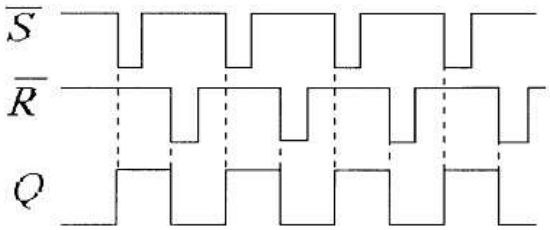
a)



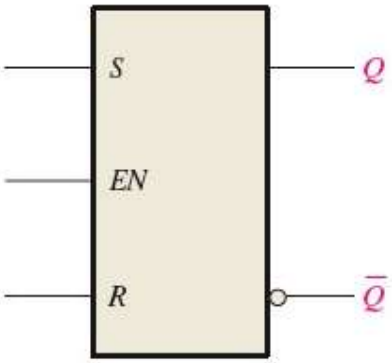
b)



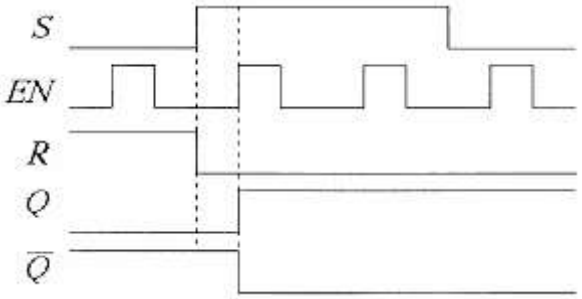




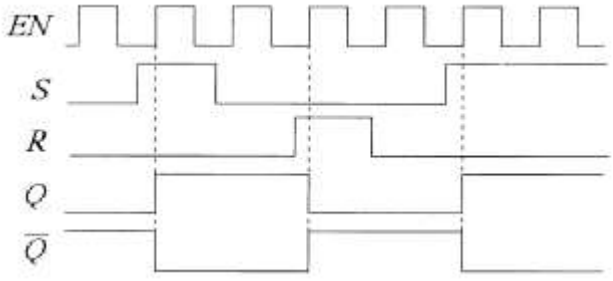
2. Determine the Q and Q' inputs for the inputs of S and R to the following latch given that the Q output is initially LOW



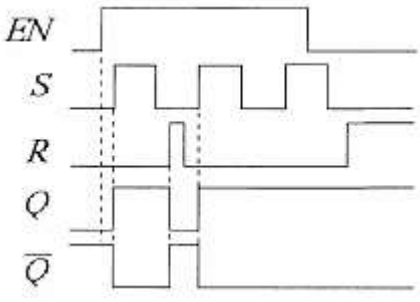
a)



b)



c)



3. Given the following latch, determine the outputs for Q and Q' with the inputs shown if given that the Q output for the latch is initially LOW