MMU
MULTIMEDIA UNIVERSITY

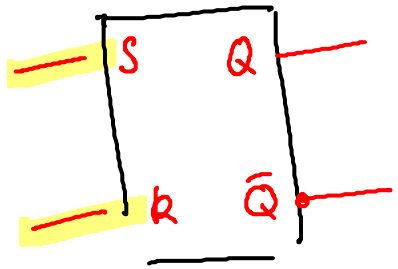
TUTORIAL 7
SEQUENTIAL LOGIC : LATCH

PDS0101: INTRODUCTION TO DIGITAL SYSTEMS
TRI 2, 2022-2023

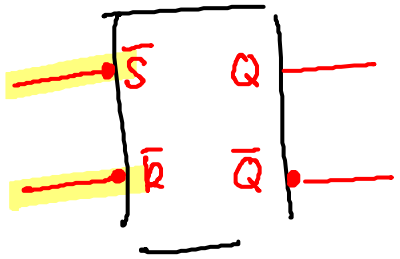
Latch

S-R latch

Active High Input

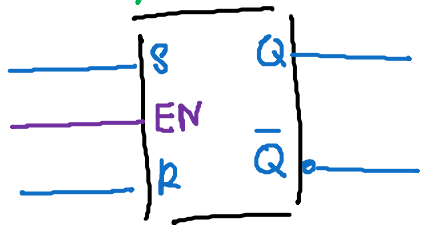


Active Low Input

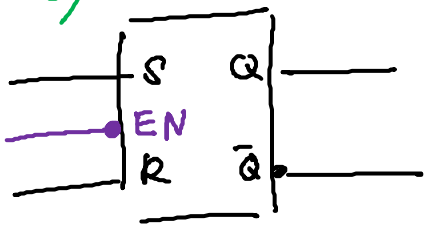


Gated S-R Latch

a) EN = 1



b)

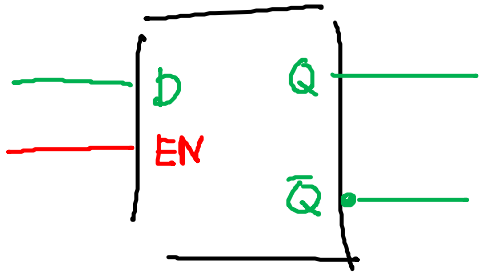


EN = 0

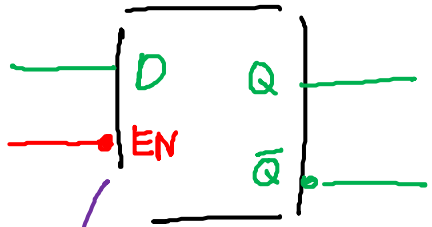
Gated D Latch

(D Latch)

Active when EN = 1



Active when EN = 0



EN = 0

Truth table

Active High SR Latch

$2^2 = 4$ possible input combination

Q follow S

S	R	Output	State
0	0	follow previous output	Rest
0	1	Q = 0	Reset
1	0	Q = 1	Set
1	1	follow previous output	Invalid

Active Low $\bar{S}$ - $\bar{R}$ latch

Q follow $\bar{R}$

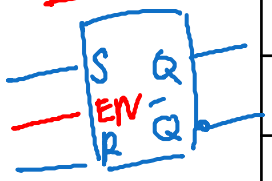
$\bar{S}$	$\bar{R}$	Output	State
0	0	follow previous output	invalid
0	1	Q = 1	set
1	0	Q = 0	reset
1	1	follow previous output	rest

Gated SR Latch (Active EN = 1)

Q follow S

EN	S	R	Output	State
1	0	0	follow previous output	rest
1	0	1	Q = 0	reset
1	1	0	Q = 1	set
1	1	1	follow previous output	invalid
0	X	X	follow previous output	rest

Logic Symbol



EN = 1

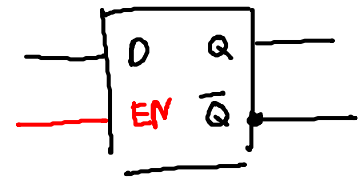
Gated D latch

input

$2^1 = 2$

EN	D	Output	State
1	0	0	reset
1	1	1	set
0	X	follow previous	rest

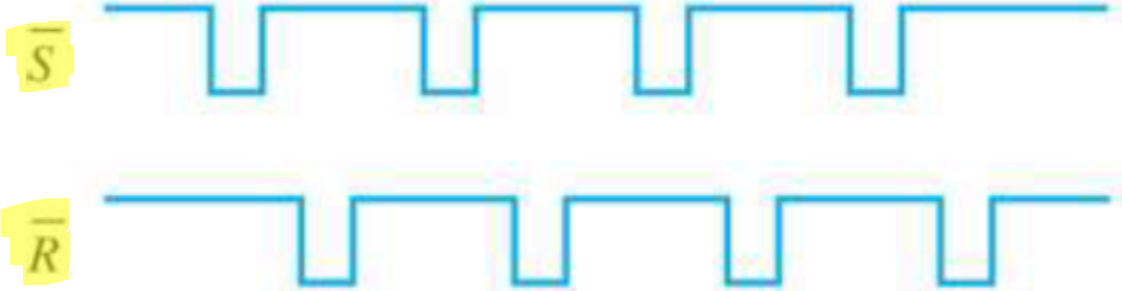
Q follow D when EN = 1



APPLIED-KNOWLEDGE BASED QUESTIONS

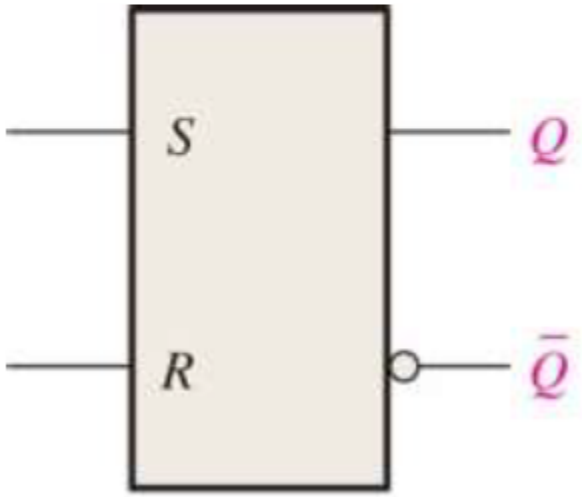
1. The waveforms in the timing diagram are applied to the latches shown below. Draw the resulting output waveform at Q in relation to the inputs assuming that Q starts low. Q = 0

Timing Diagram



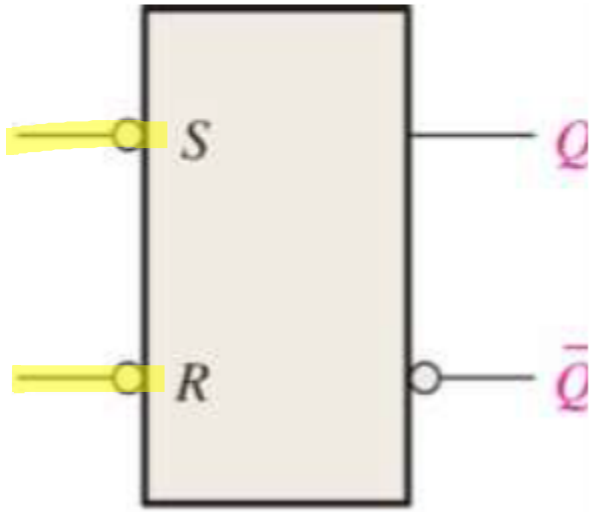
Active High Input

a)



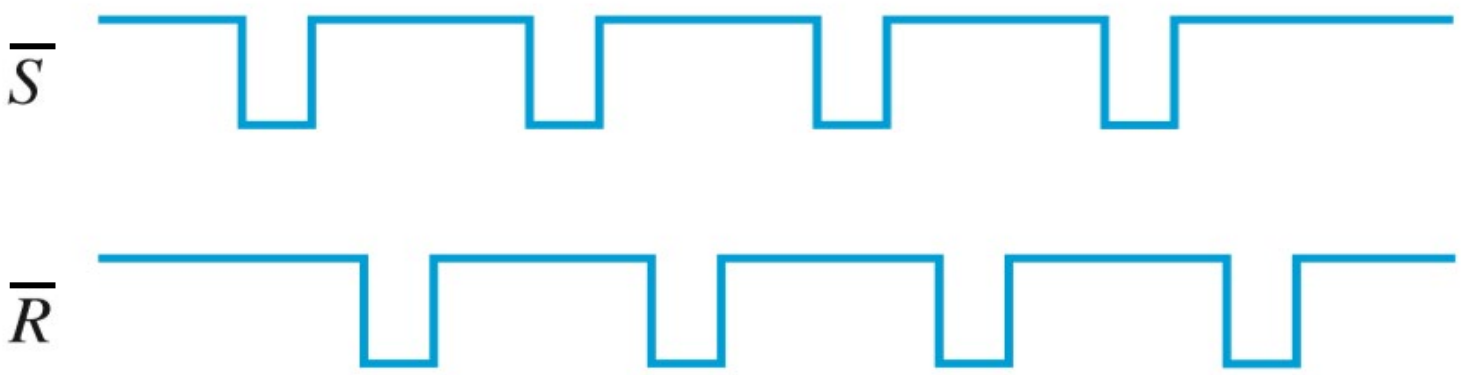
Active Low Input

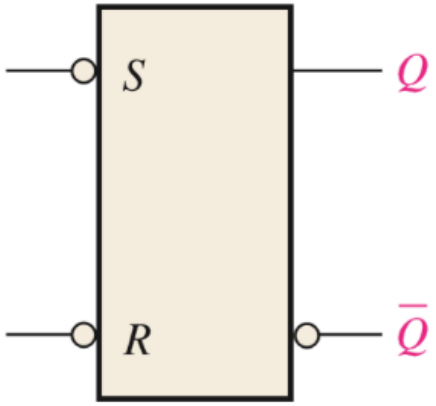
b)



QUESTION 1(b)

The waveforms in the timing diagram are applied to the **latches** shown below. Draw the resulting **output** waveform at Q in relation to the inputs assuming that **Q starts low**.

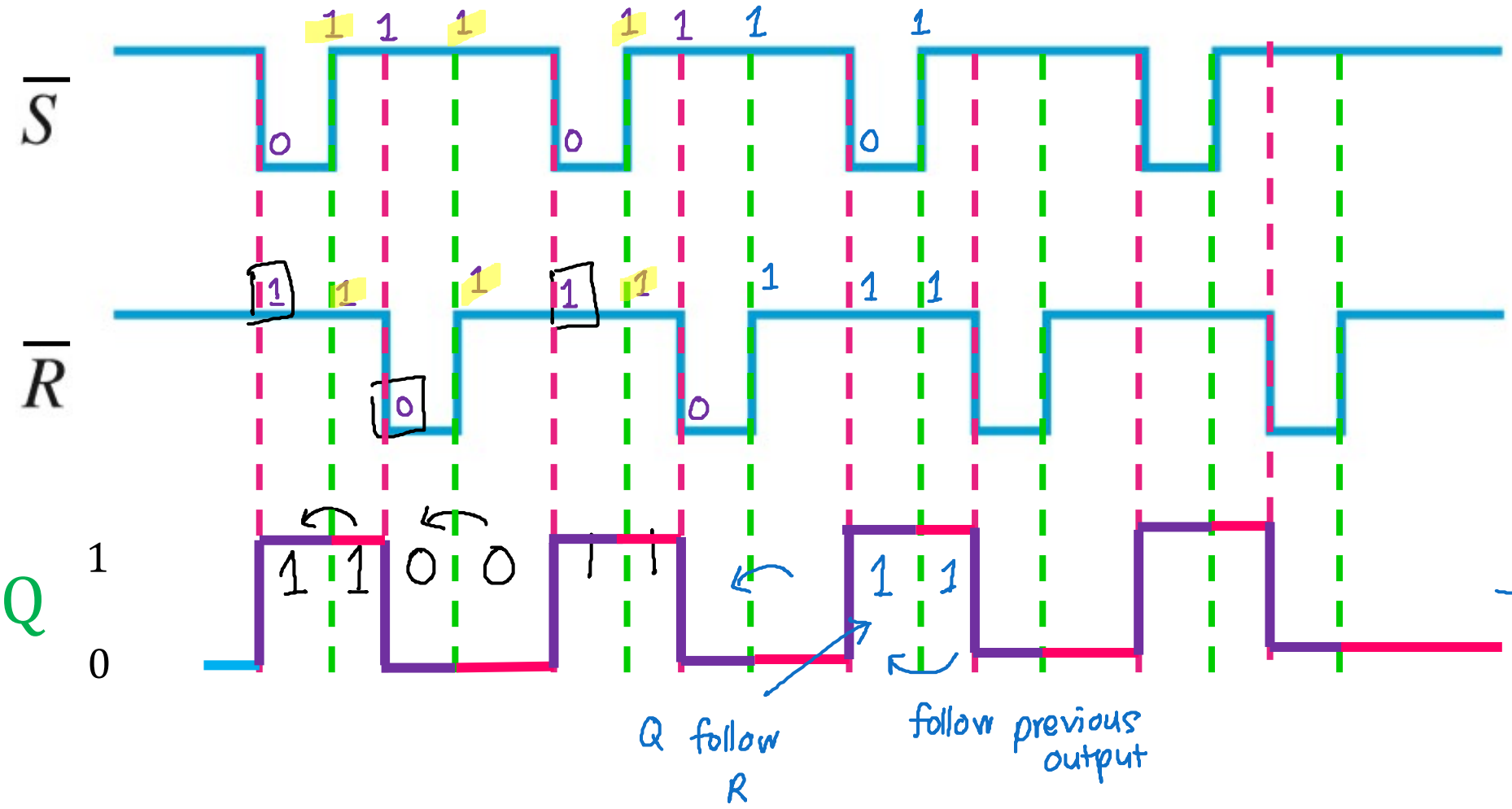


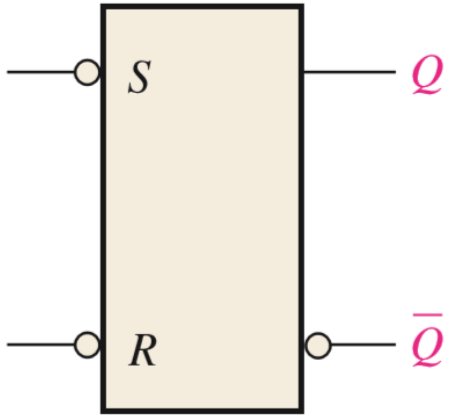


Active-LOW input $\overline{S}$-$\overline{R}$ latch

S	R	Q	STATE
0	0	No change	Invalid
1	0	Q = 0	Reset
0	1	Q = 1	Set
1	1	No change	Resting

1(b) LATCHES | Q STARTS LOW | ACTIVE LOW INPUT S-R LATCH



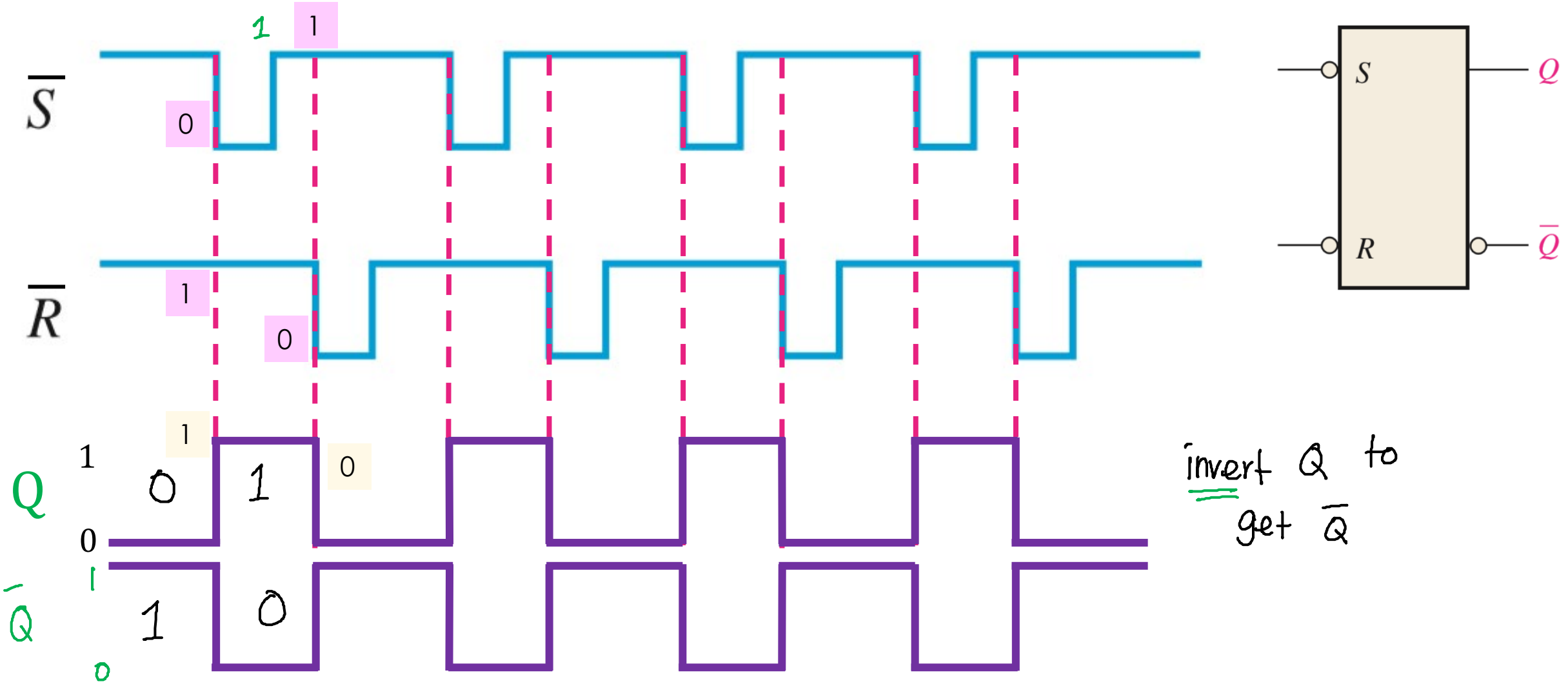


Q follow R

$\overline{S}$	$\overline{R}$	output
0	1	1
1	0	0

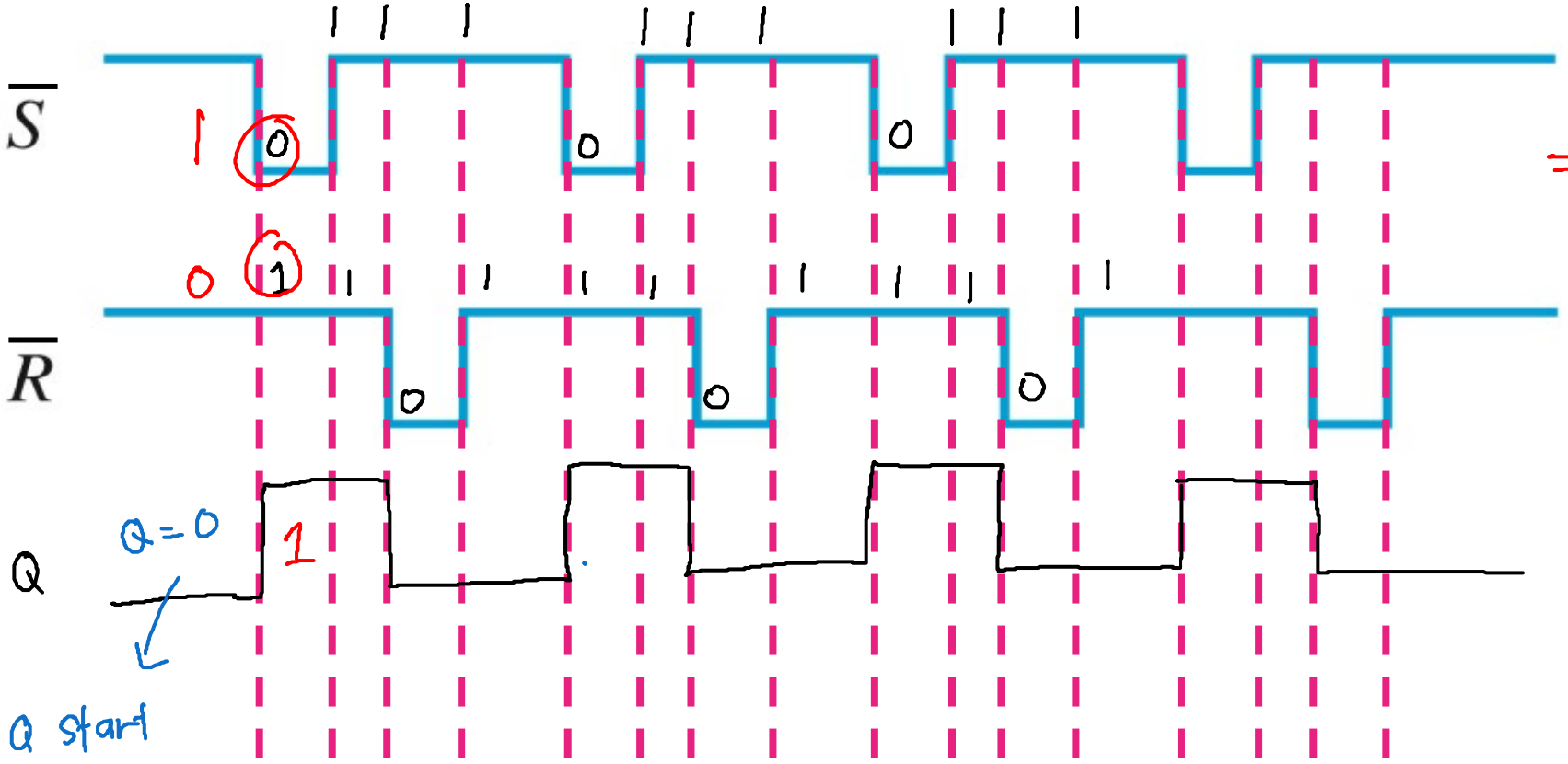
$\overline{S}$	$\overline{R}$	output
0	0	} follow previous output
1	1	

1(b) LATCHES | Q STARTS LOW | ACTIVE LOW INPUT S-R LATCH

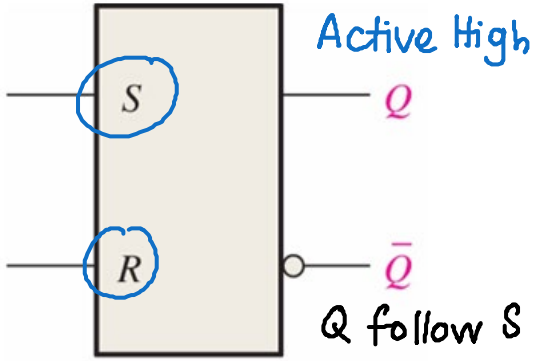


QUESTION 1(a)

The waveforms in the timing diagram are applied to the latches shown below. Draw the resulting **output** waveform at Q in relation to the inputs assuming that **Q starts low**.



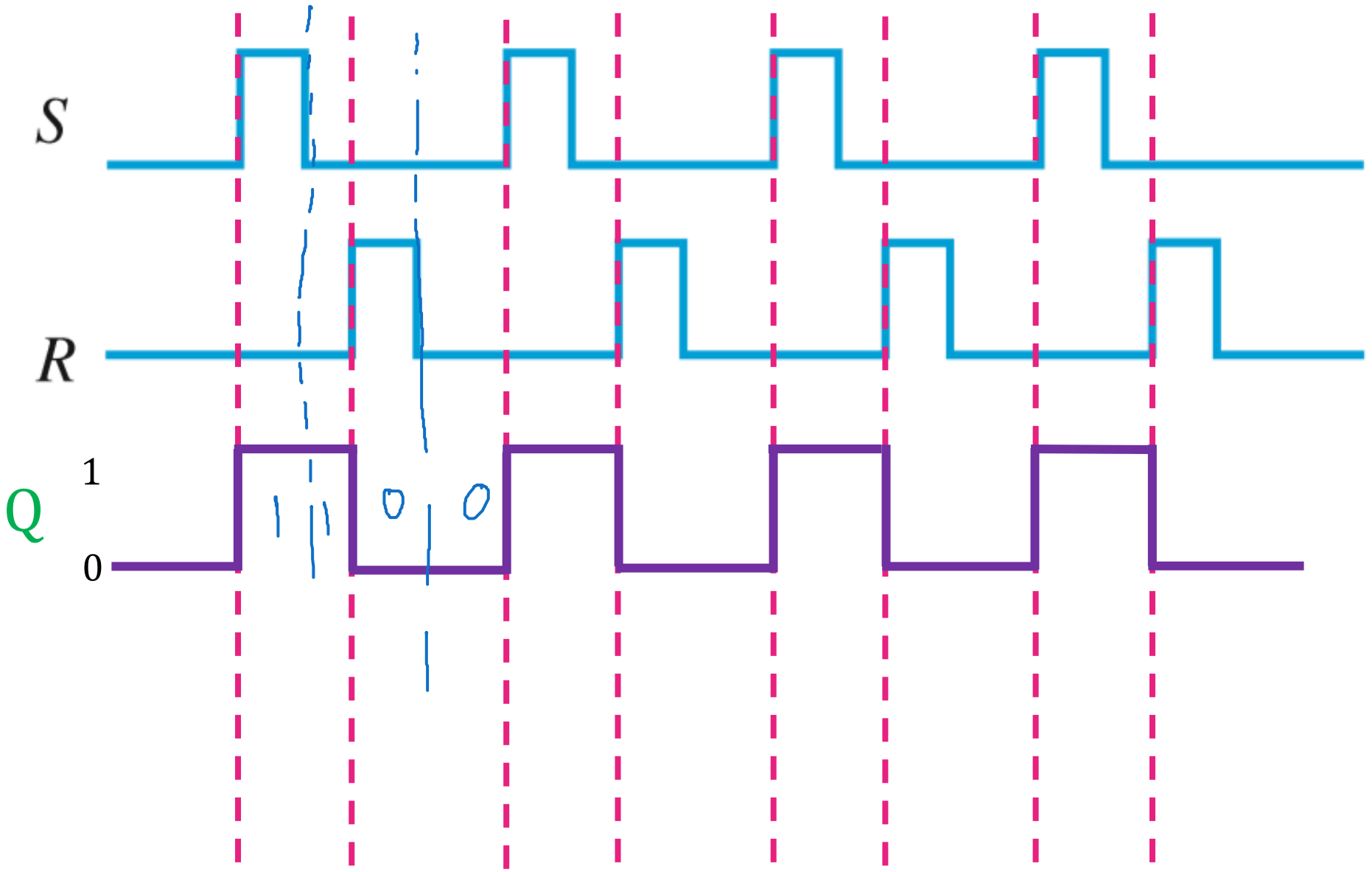
invert timing digram

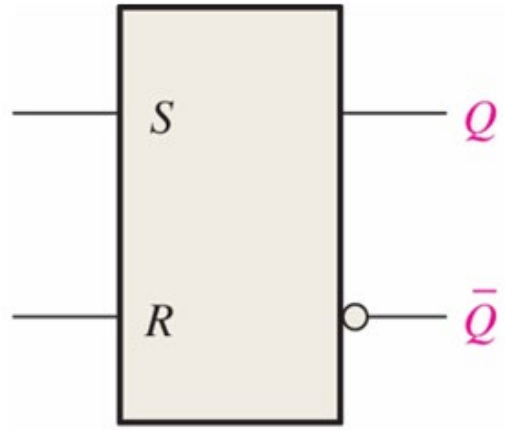


S	R	Output
1	0	1
0	0	1
0	1	0
0	0	0
1	0	1
0	0	1
0	1	0
0	0	0
1	0	1
0	0	1
0	1	
0	0	

follow previous output

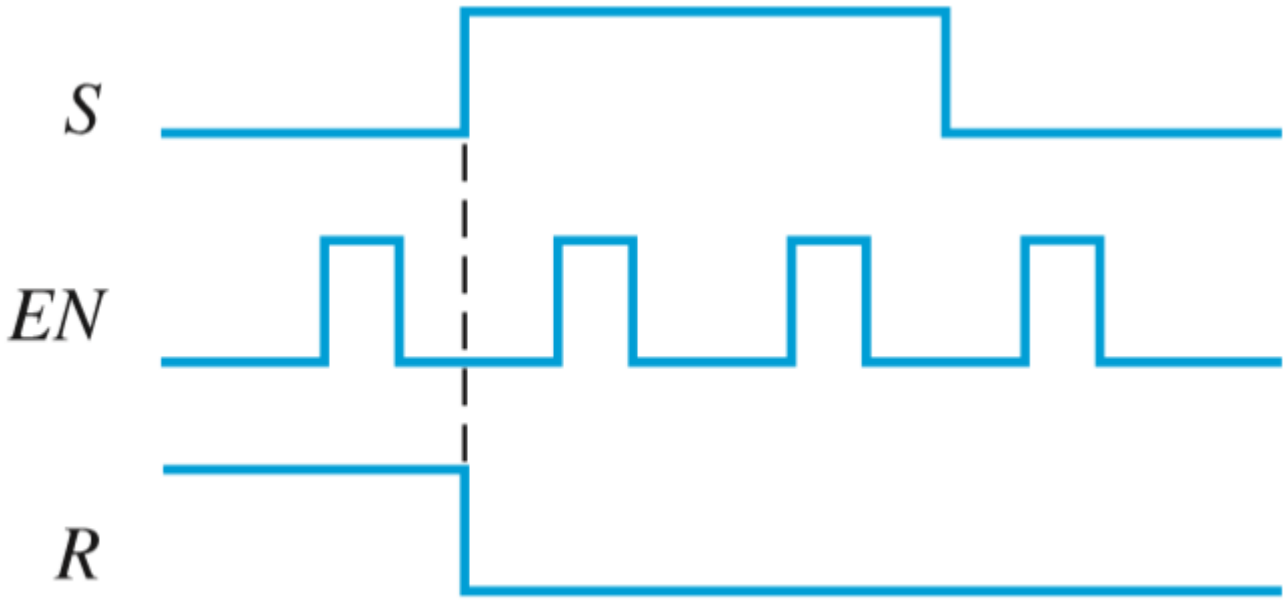
1(a) LATCHES | Q STARTS LOW | ACTIVE HIGH INPUT S-R LATCH

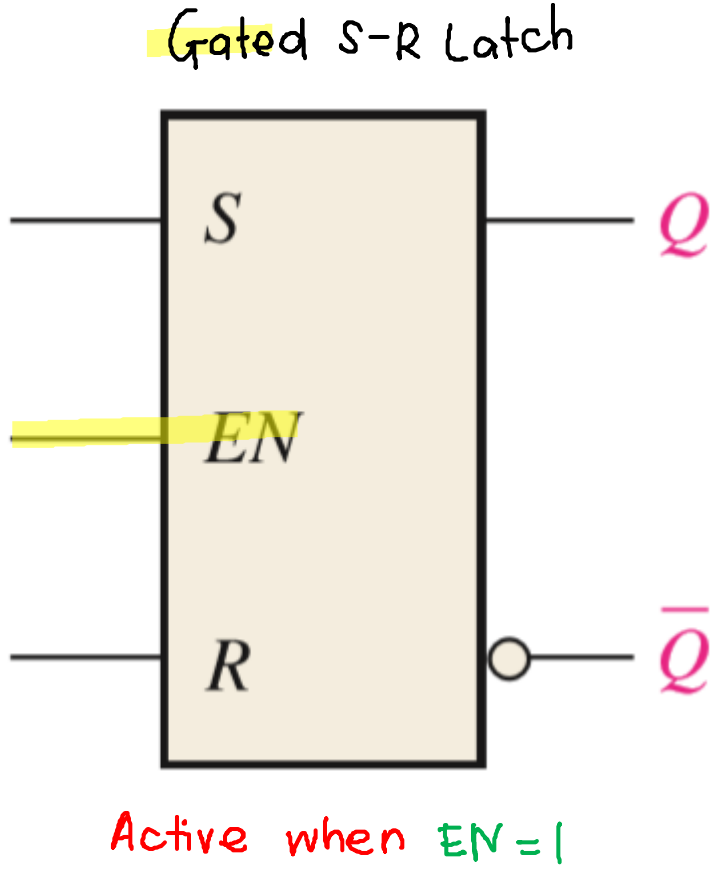




QUESTION 2(a)

Determine the **Q** and $\overline{\mathbf{Q}}$ output for the inputs of **S** and **R** to the following latch given that the Q output is initially **LOW**



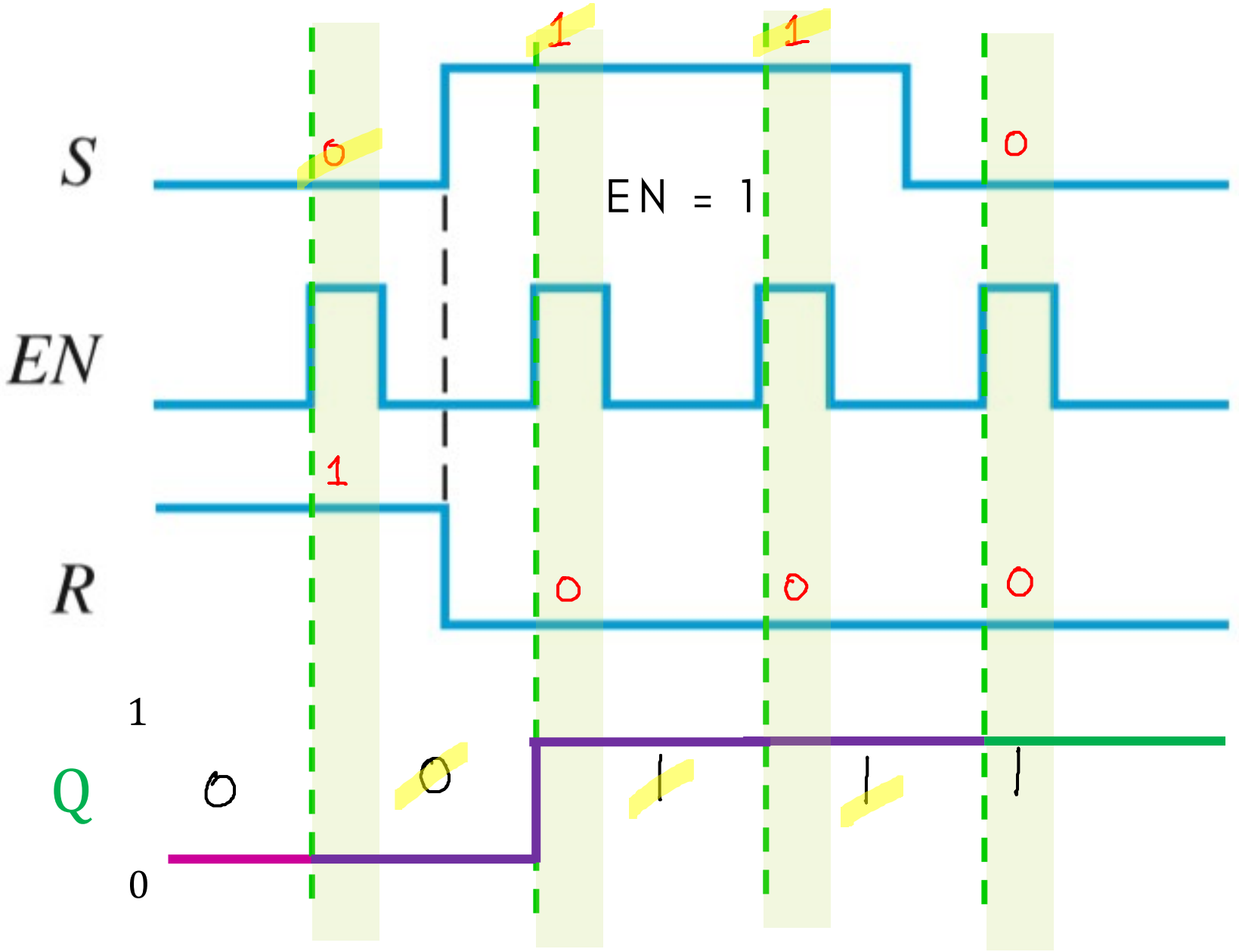


TRUTH TABLE FOR GATED S-R LATCH

Gated S-R latch

E	S	R	Q
1	0	0	No change
1	0	1	Q = 0
1	1	0	Q = 1
1	1	1	No change
0	x	x	No change

2(a). LATCHES | Q STARTS LOW | GATED S-R LATCH



0	0	1	1
1	0	0	0

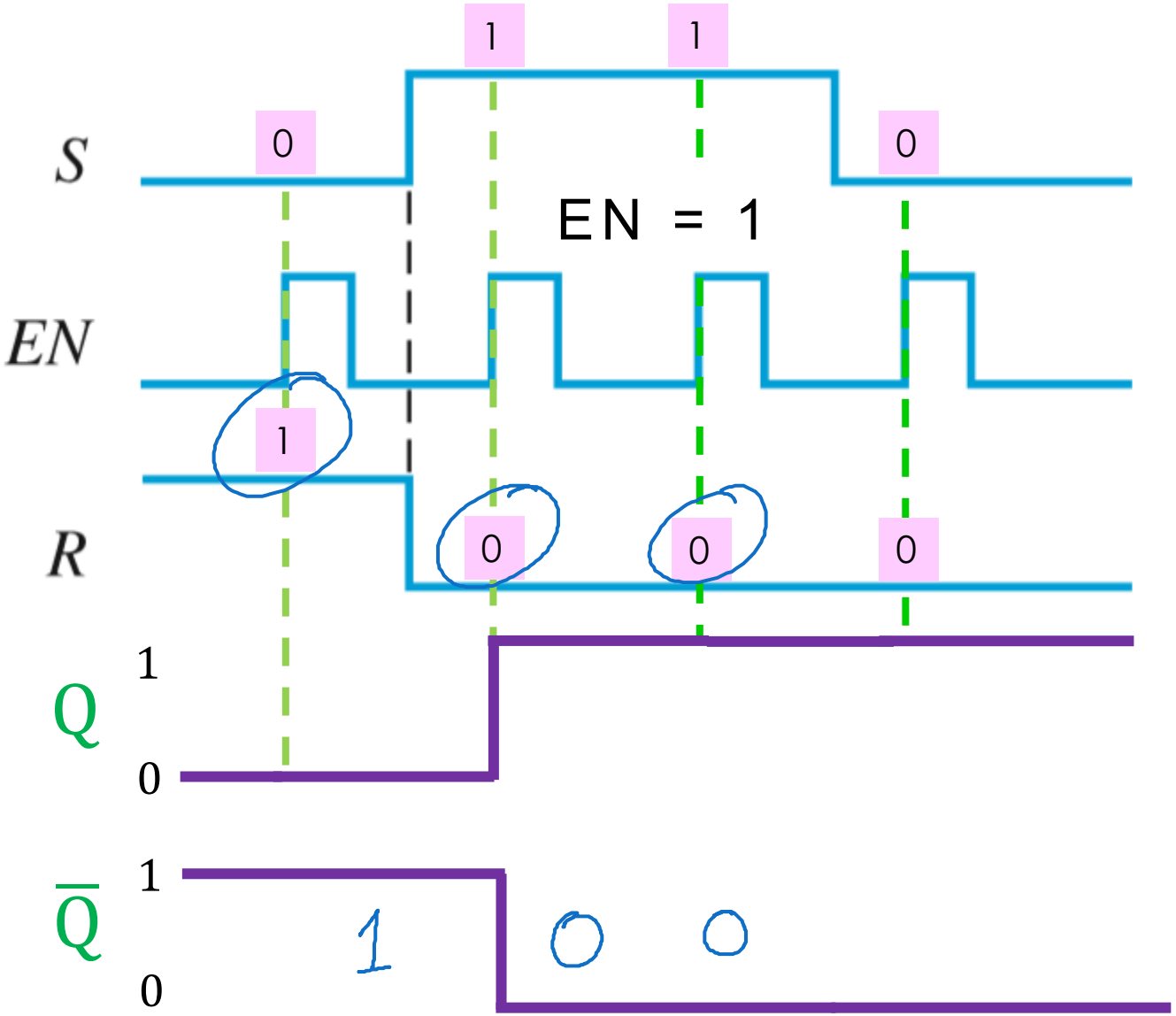
Q follow S

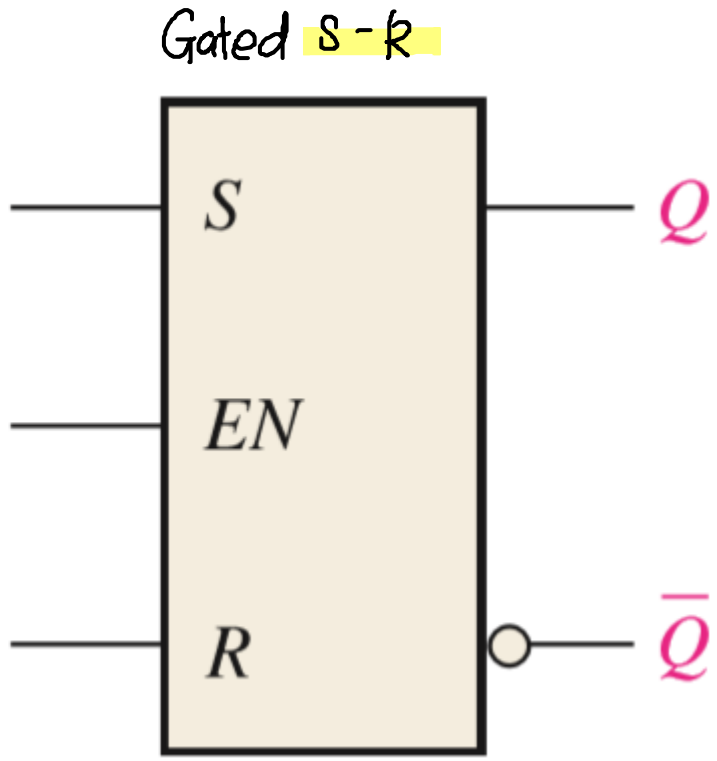
S	R	Q
0	1	0
1	0	1

Q follow previous output

S	R
0	0
1	1

2(a). LATCHES | Q STARTS LOW | GATED S-R LATCH



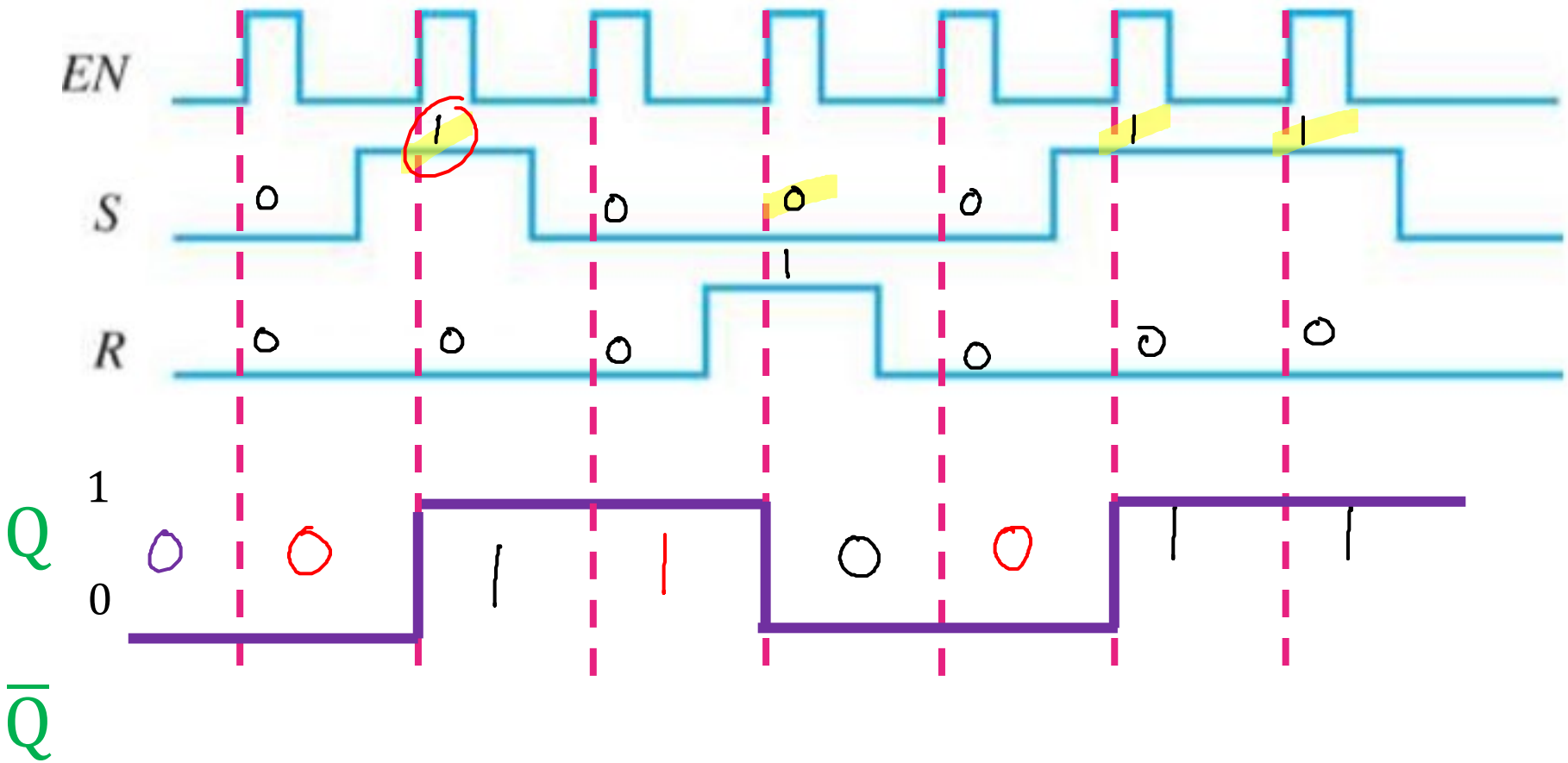


Q follow S

$\overline{Q}$ follow R

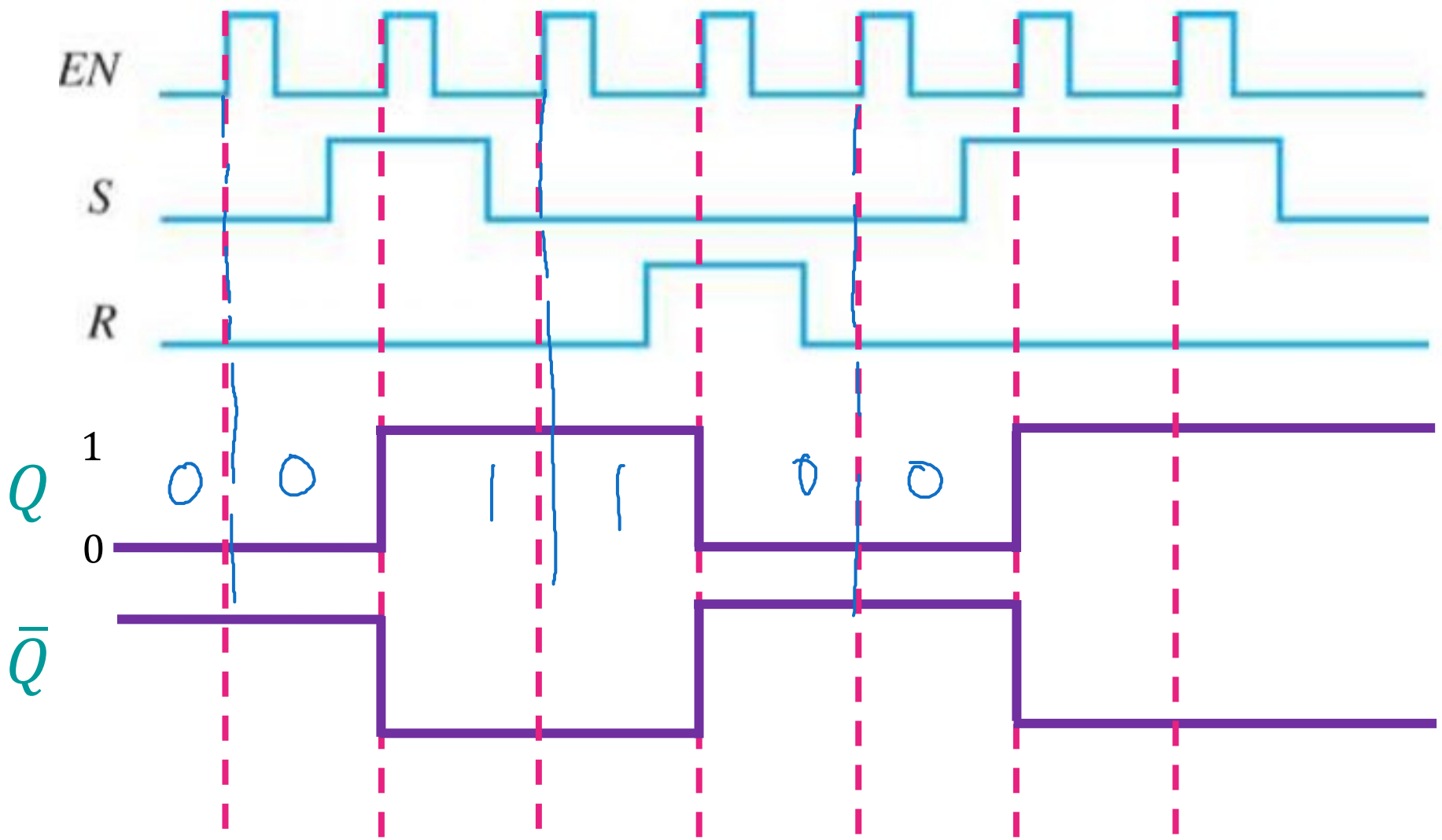
QUESTION 2(b)

Determine the **Q** and $\overline{\mathbf{Q}}$ output for the inputs of **S** and **R** to the following latch given that the **Q** output is initially **LOW** Q = 0



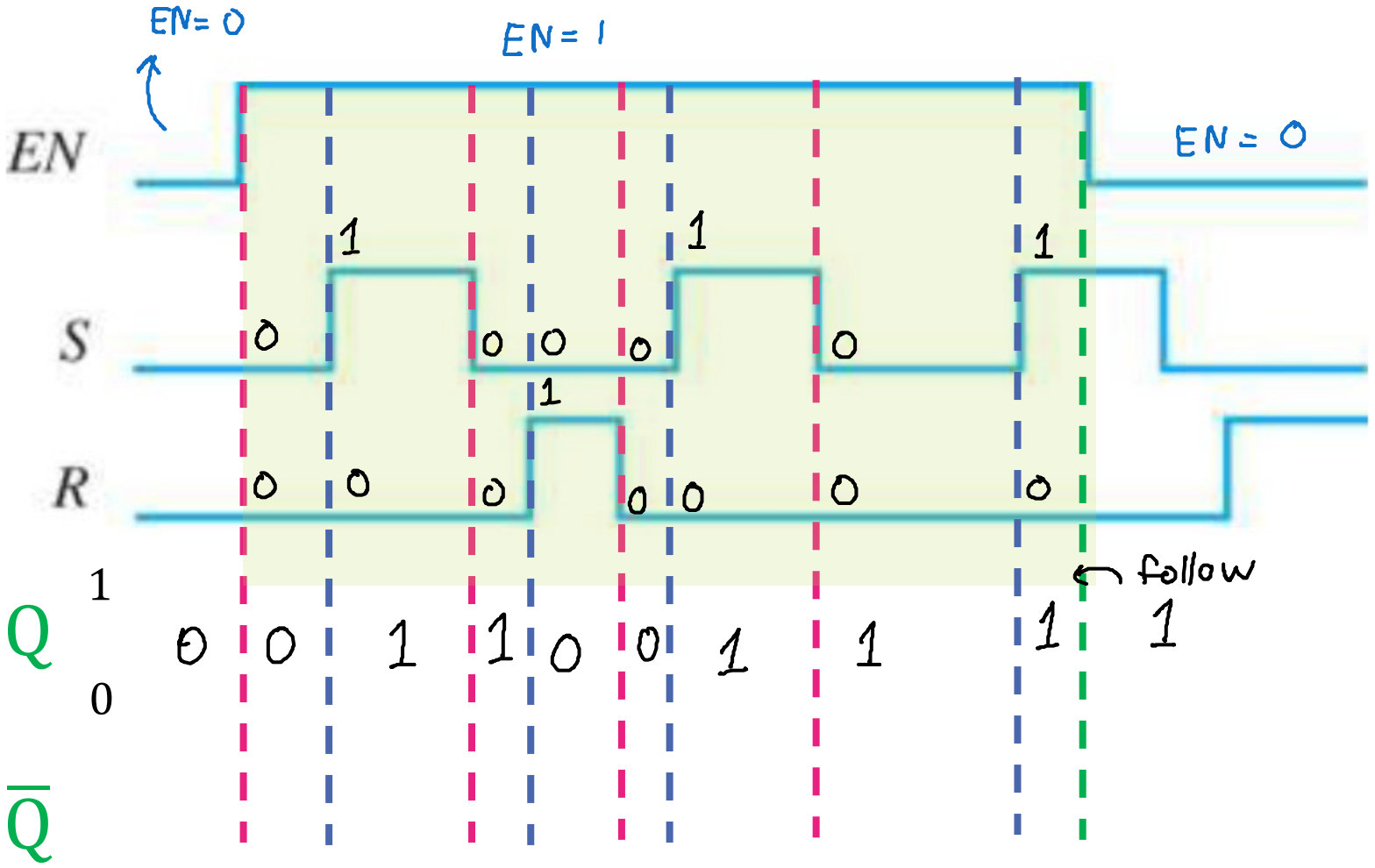
Q follow S

2(b). LATCHES | Q STARTS LOW | GATED S-R LATCH

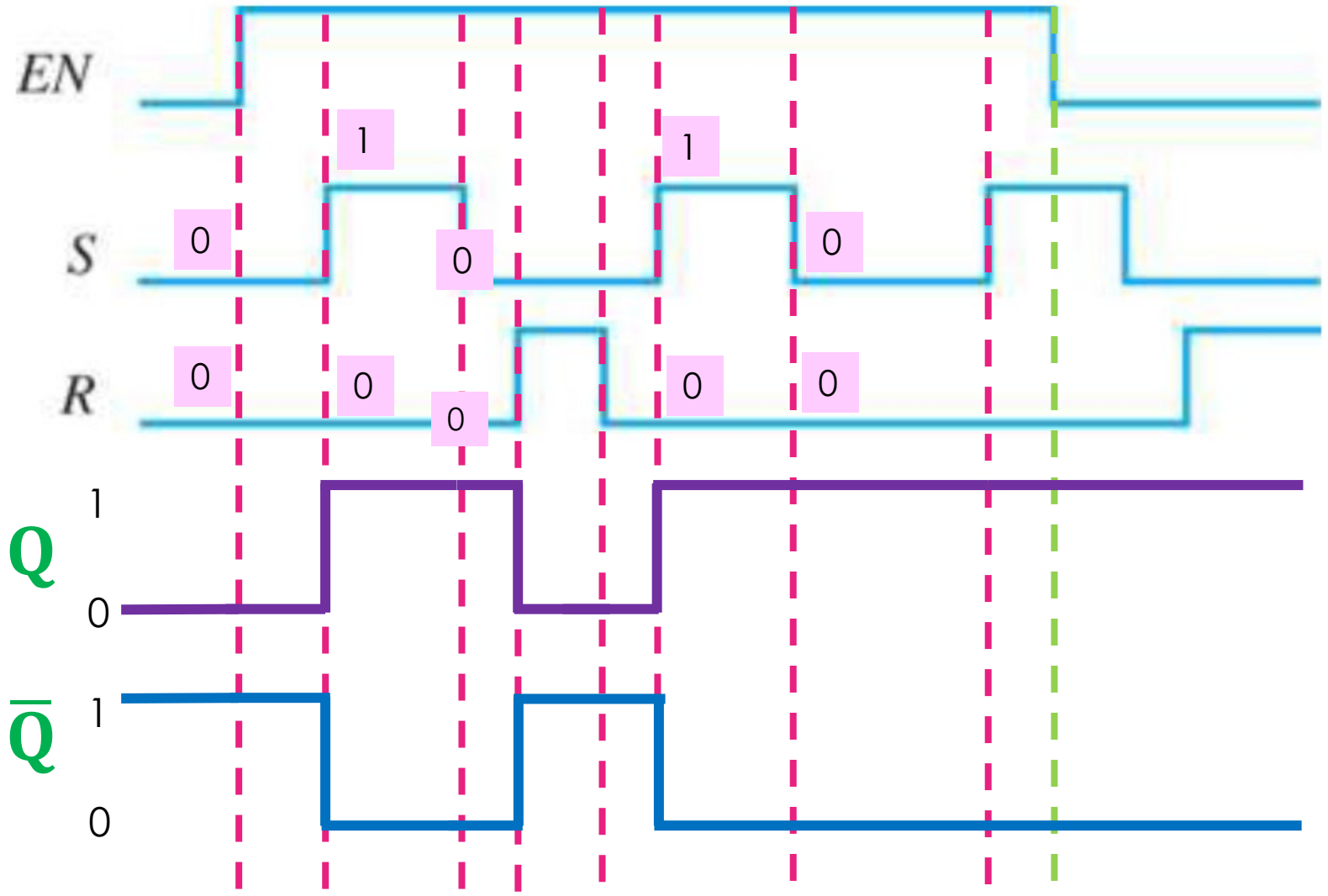


QUESTION 2(c)

Determine the **Q** and $\overline{\mathbf{Q}}$ output for the inputs of S and R to the following latch given that the Q output is initially LOW

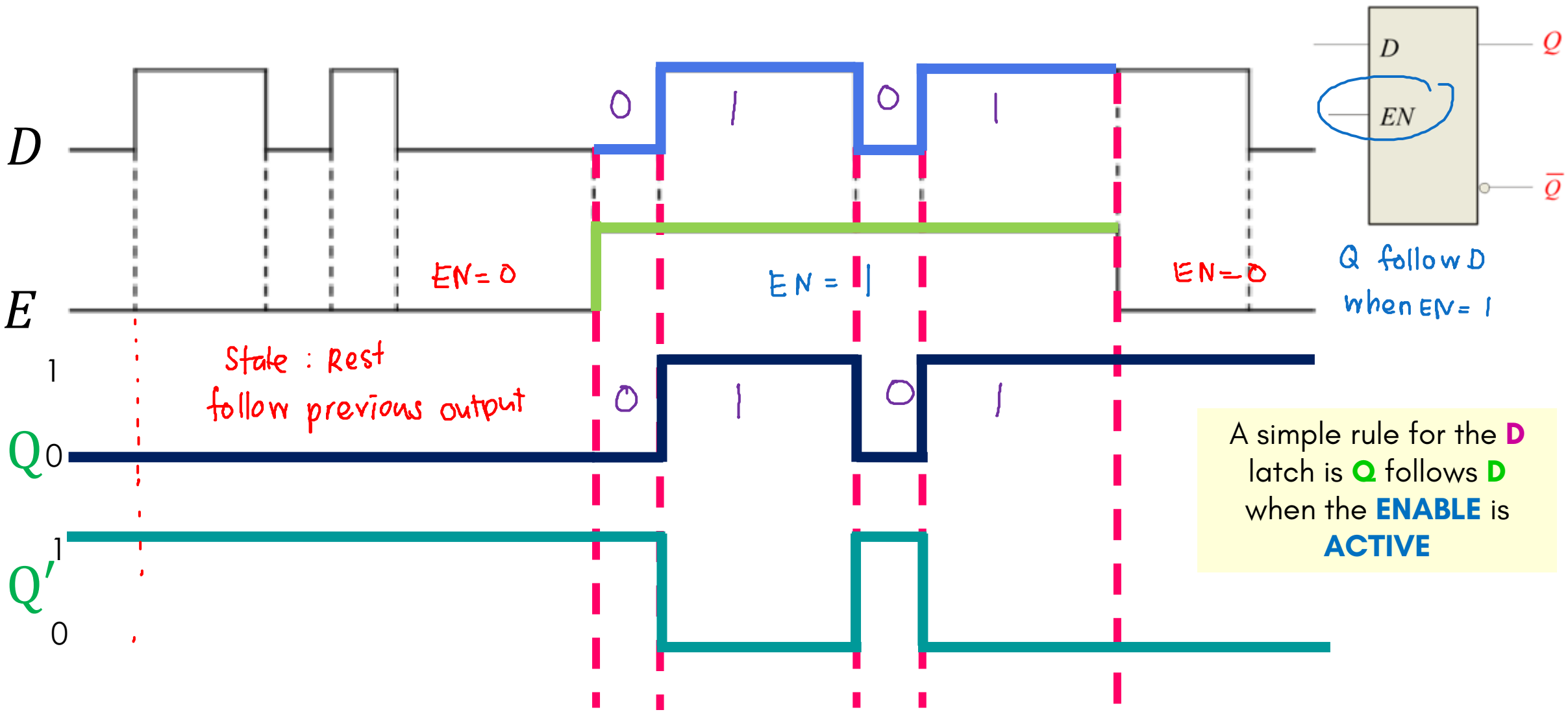


2(c). LATCHES | Q STARTS LOW | GATED S-R LATCH



QUESTION 3(a)

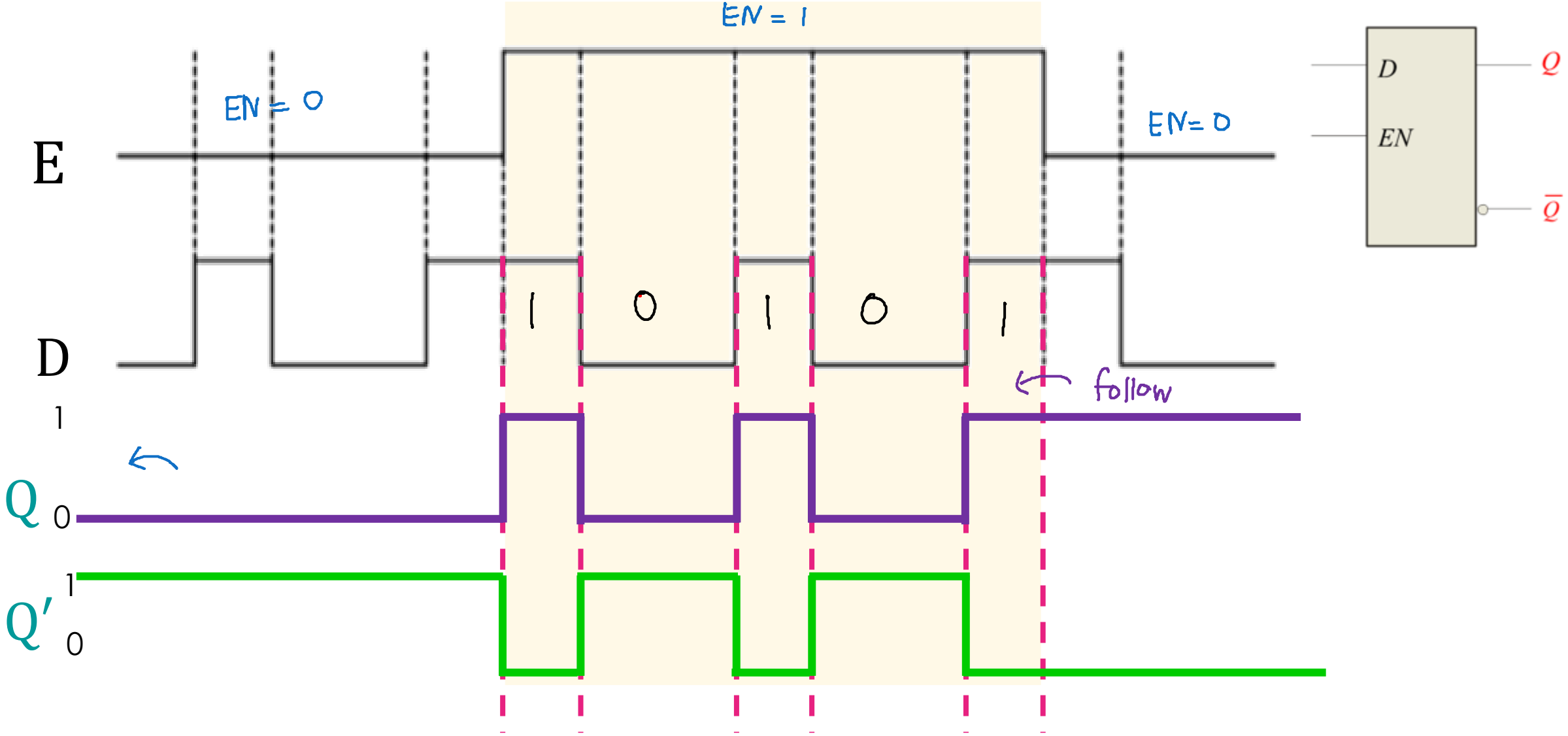
Given the following latch, determine the outputs for **Q** and $\overline{Q}$ with the inputs shown if given that the Q output for the latch is **initially LOW**.



A simple rule for the **D** latch is **Q** follows **D** when the **ENABLE** is **ACTIVE**

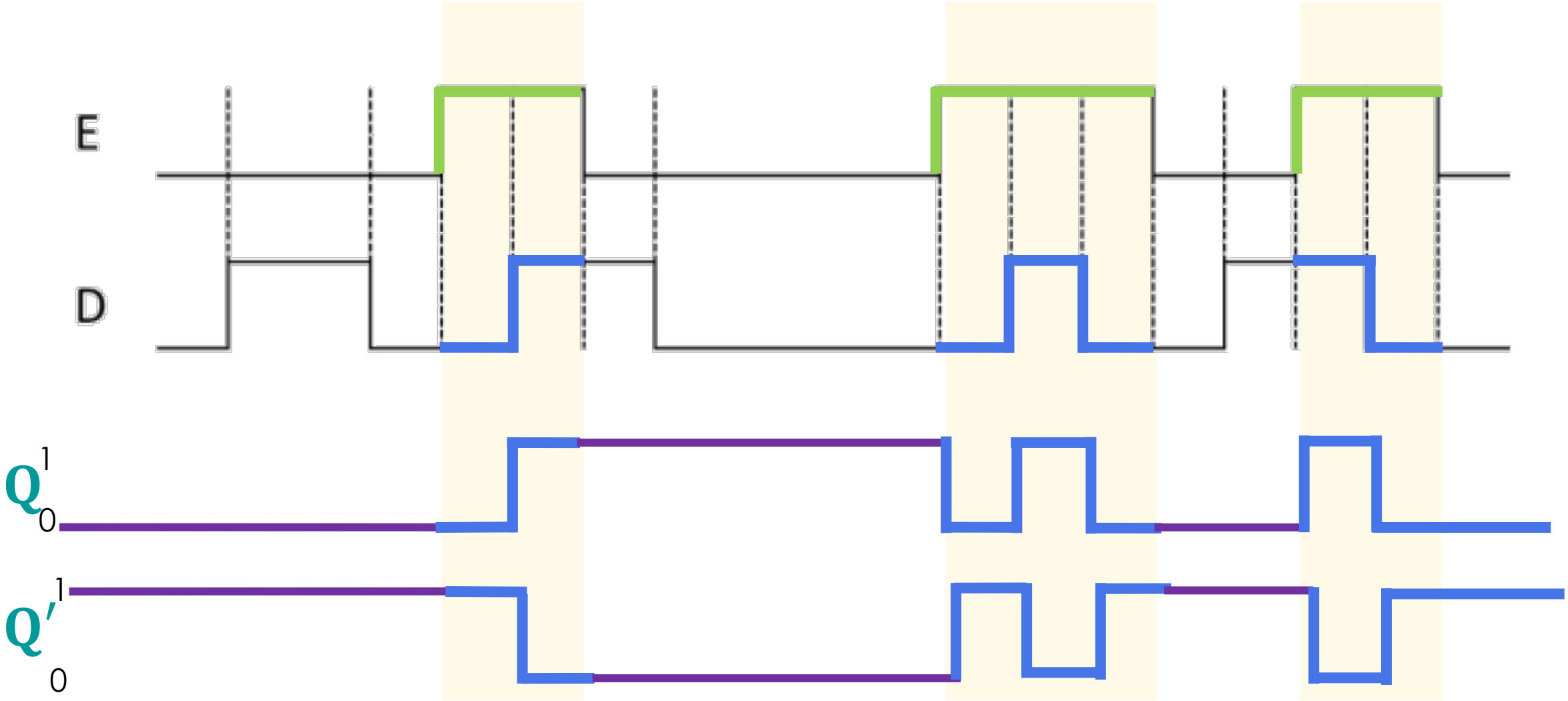
QUESTION 3(b)

Given the following latch, determine the outputs for **Q** and $\overline{\mathbf{Q}}$ with the inputs shown if given that the Q output for the latch is **initially LOW**.



QUESTION 3(c)

Given the following latch, determine the outputs for **Q** and $\overline{\mathbf{Q}}$ with the inputs shown if given that the Q output for the latch is **initially LOW**.



END DISCUSSIONS
ANY QUESTIONS ??