MULTIMEDIA UNIVERSITY

PDS0101 Introduction to Digital Systems

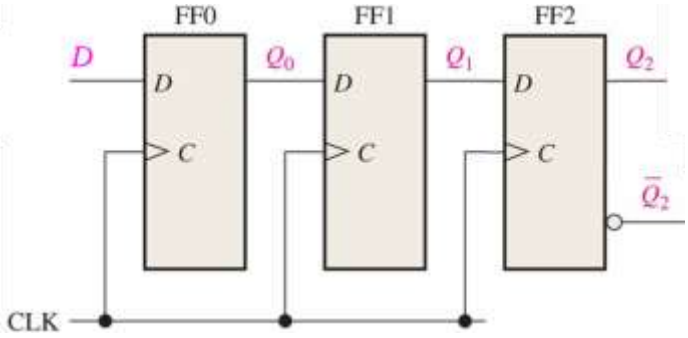
Tutorial 10 SAMPLE SOLUTIONS

NOTE

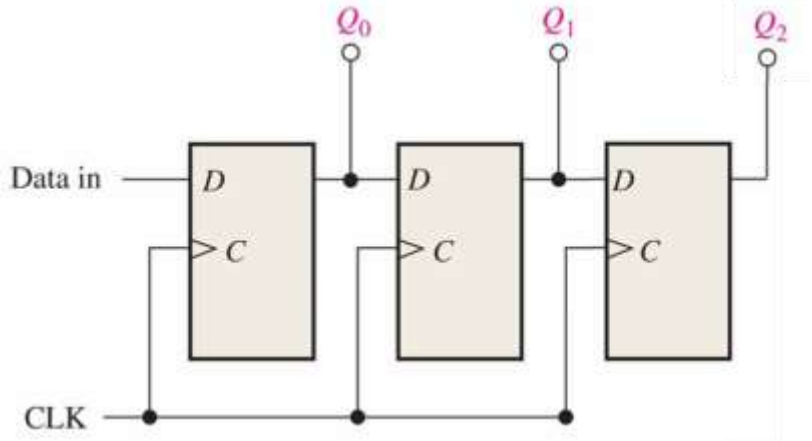
Answers shown may be only one of many possibilities available. Please approach your tutor if you have an alternative answer of which you are not sure of. Any errors and omissions in the answers are deeply regretted.

Theory based questions

1. Draw the logic circuit diagram for a 3-bit serial in/serial out shift register – what FFs do you use?



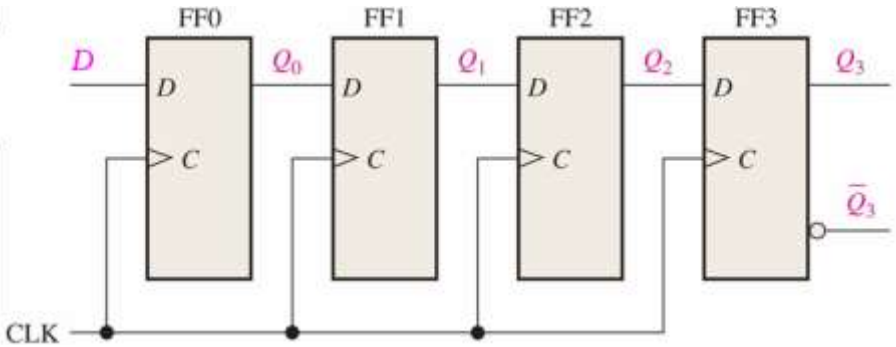
2. Revise the circuit from (1) to create a 3-bit serial in/parallel out shift register



3. The sequence 1011 is applied to the input line of a 4-bit serial shift register. If the register is initially cleared, what is the state of the register after 3 clock pulses?

Initially: 0000
1st CLK: 1000 ← Note that the LSB goes in first!
2nd CLK: 1100
3rd CLK: 0110

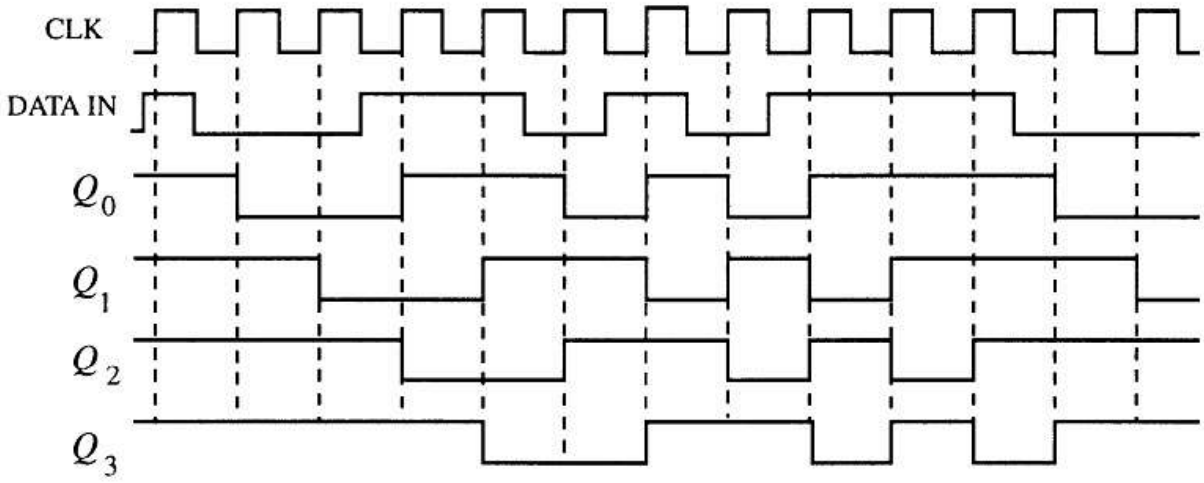
4. Identify the shift register shown in the diagram below. Then identify which is the input and output for the register



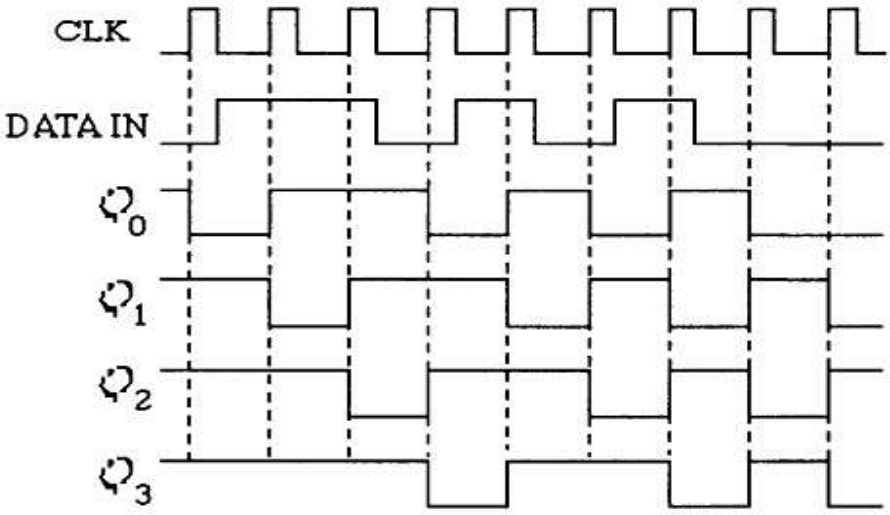
4-bit serial in/out register. Input D, output Q3

5. Using the register above in (4), determine the state of each flip-flop and show the Q waveforms in with the data inputs and clock timing diagrams shown below. The register has all 1's in each FF when it begins.

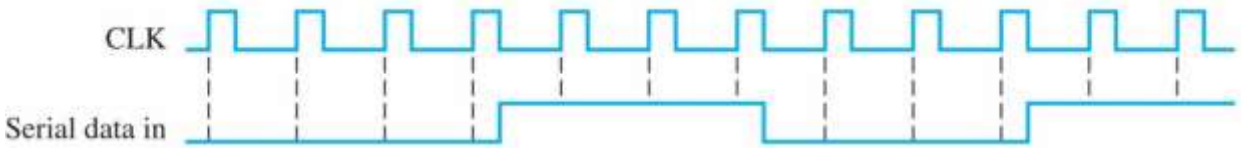
a)



b)



6. What is the state of the register below after each clock pulse if it starts in the 101001111000 state?

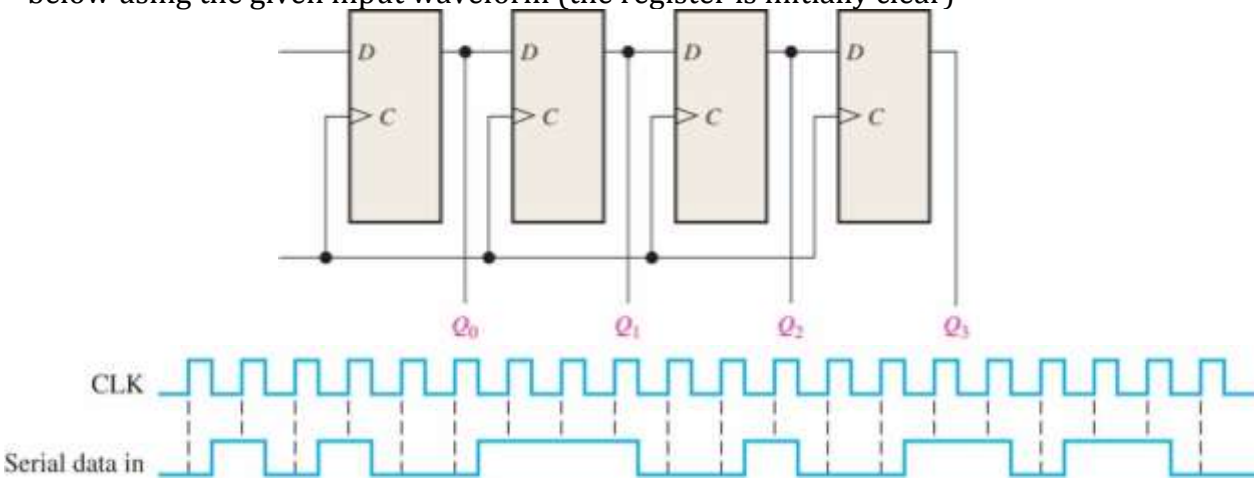


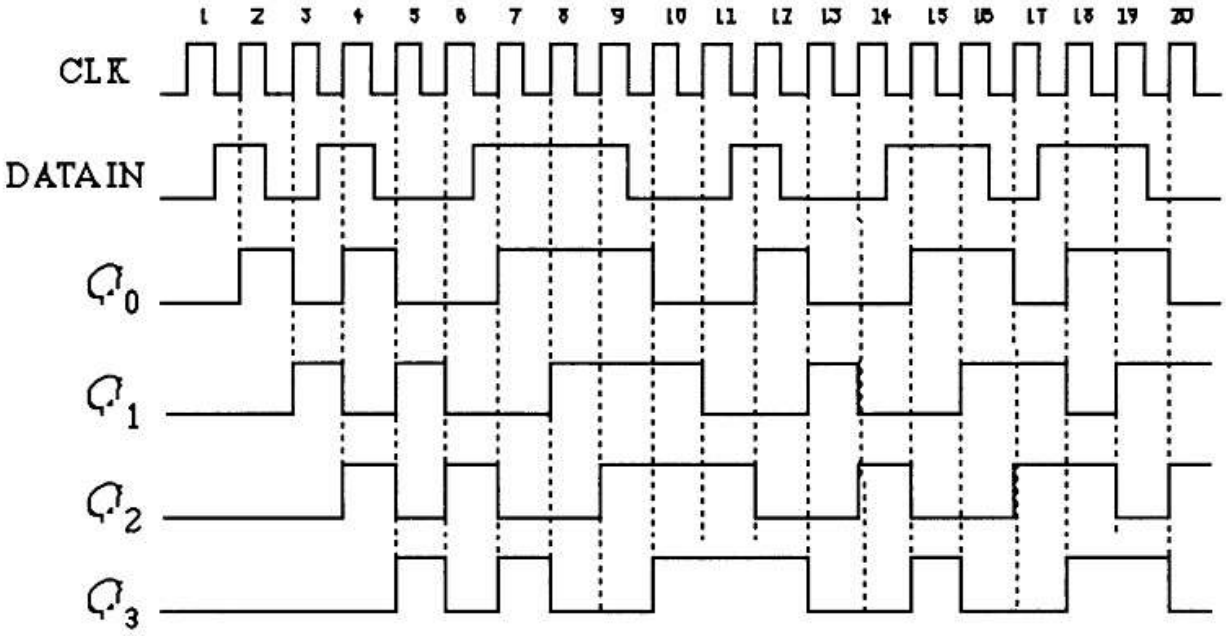
Initially	101001111000
CLK 1	010100111100
CLK 2	001010011110
CLK 3	000101001111
CLK 4	000010100111
CLK 5	100001010011
CLK 6	110000101001
CLK 7	111000010100
CLK 8	011100001010
CLK 9	001110000101
CLK 10	000111000010
CLK 11	100011100001
CLK 12	110001110000

CLK 1 – 4 the register proceeds as normal and 'shifts' the bits it already has towards the output (i.e. to right)

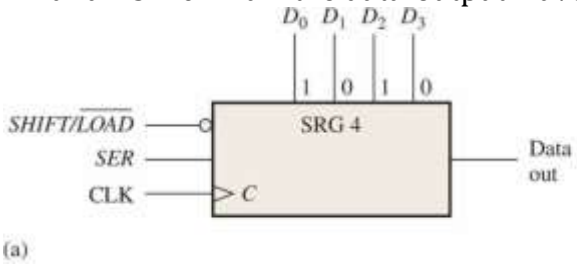
At CLK 5, the data in is HIGH so a new bit is 'added'
This process repeats at CLK 6 and 7
At CLK 8, the data in is LOW so a '0' is added instead

7. Identify and show the timing diagram including the parallel outputs for the shift register below using the given input waveform (the register is initially clear)

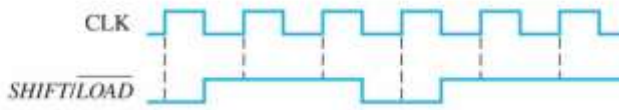




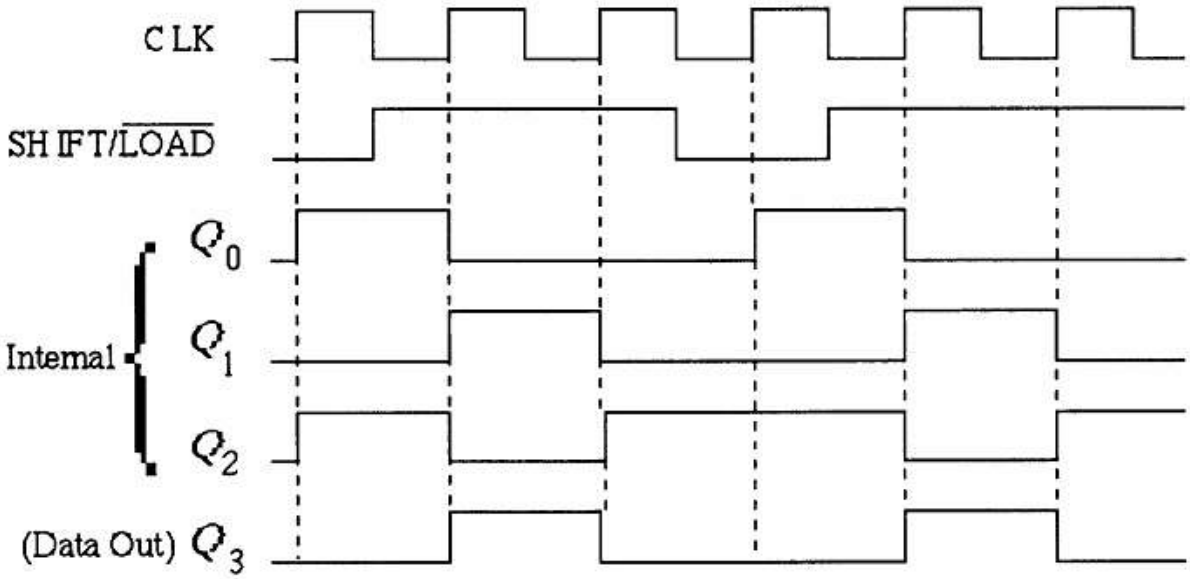
8. The parallel in/serial out register below has the SHIFT/LOAD and CLK inputs as shown in the timing diagram below. The parallel data inputs are constant at D0 = 1, D1 = 0, D2 = 1 and D3 = 0. Draw the data-output waveform of the register in relation to the inputs



(a)



(b)

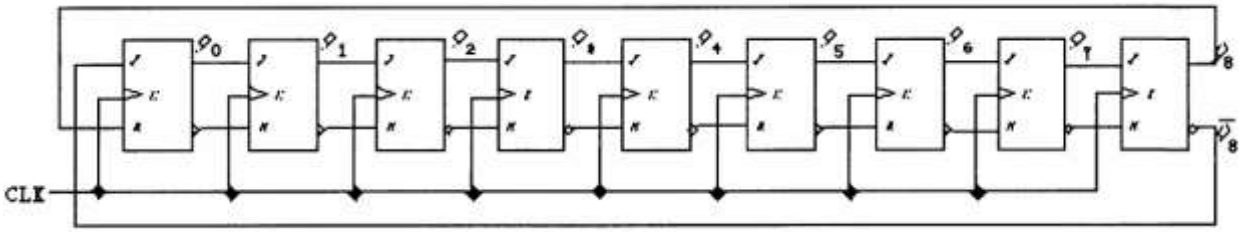


9. Determine the number of flip-flops required to implement each of the following in a Johnson counter configuration
   a. modulus-6 → 2n=6 therefore number of FF, n=3 (DO NOT MIX THIS UP WITH THE MODULUS IN EARLIER COUNTERS!!)
   b. modulus-10 → n=5

c. modulus-14 → n = 7
d. modulus-16 → n=8

10. Draw the logic diagram for a modulus-18 Johnson counter using J-K flip-flops and show the timing sequence of its flip-flops in tabular form. How would the sequence change if it were a ring counter instead?

    2n = 18, n=9 The counter requires 9 FFs. In Johnson, the complement is fedback to the initial FF



Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0
1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1
0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0