

TUTORIAL 1

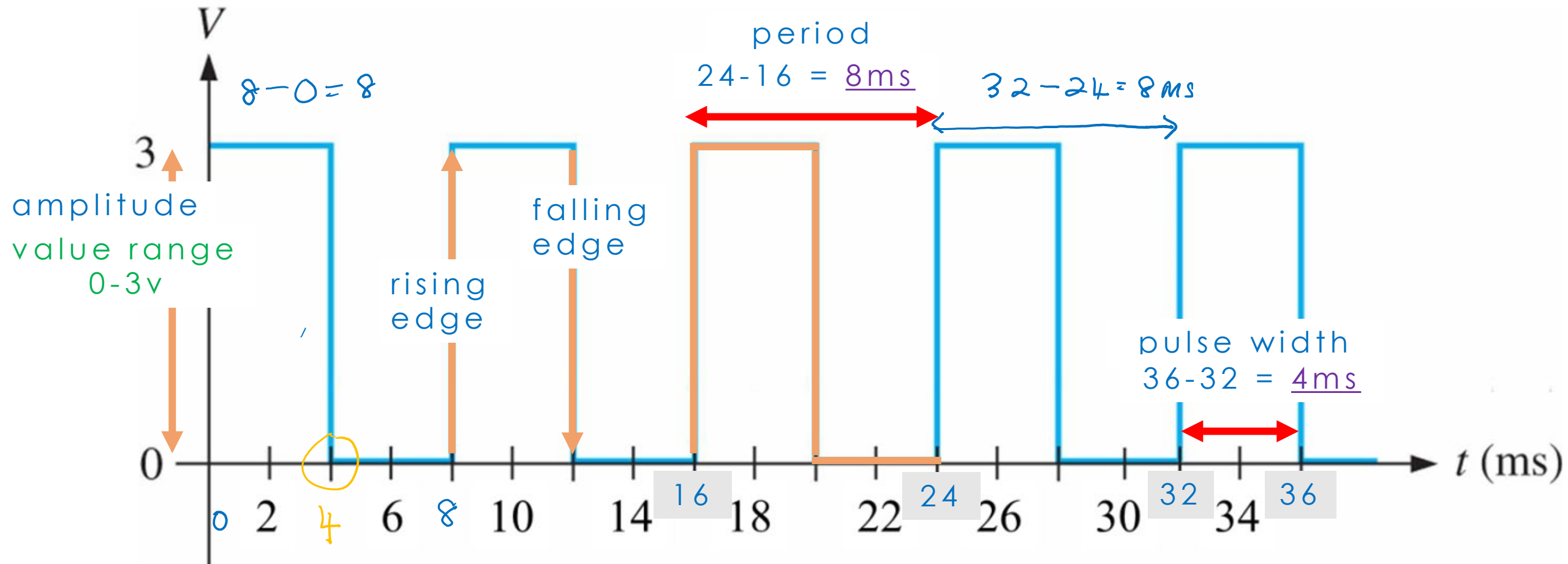
INTRO TO DIGITAL CONCEPTS

PDS0101: INTRODUCTION TO DIGITAL SYSTEMS
TRI 2, 2022-2023



THEORY BASED QUESTIONS : QUESTION 1

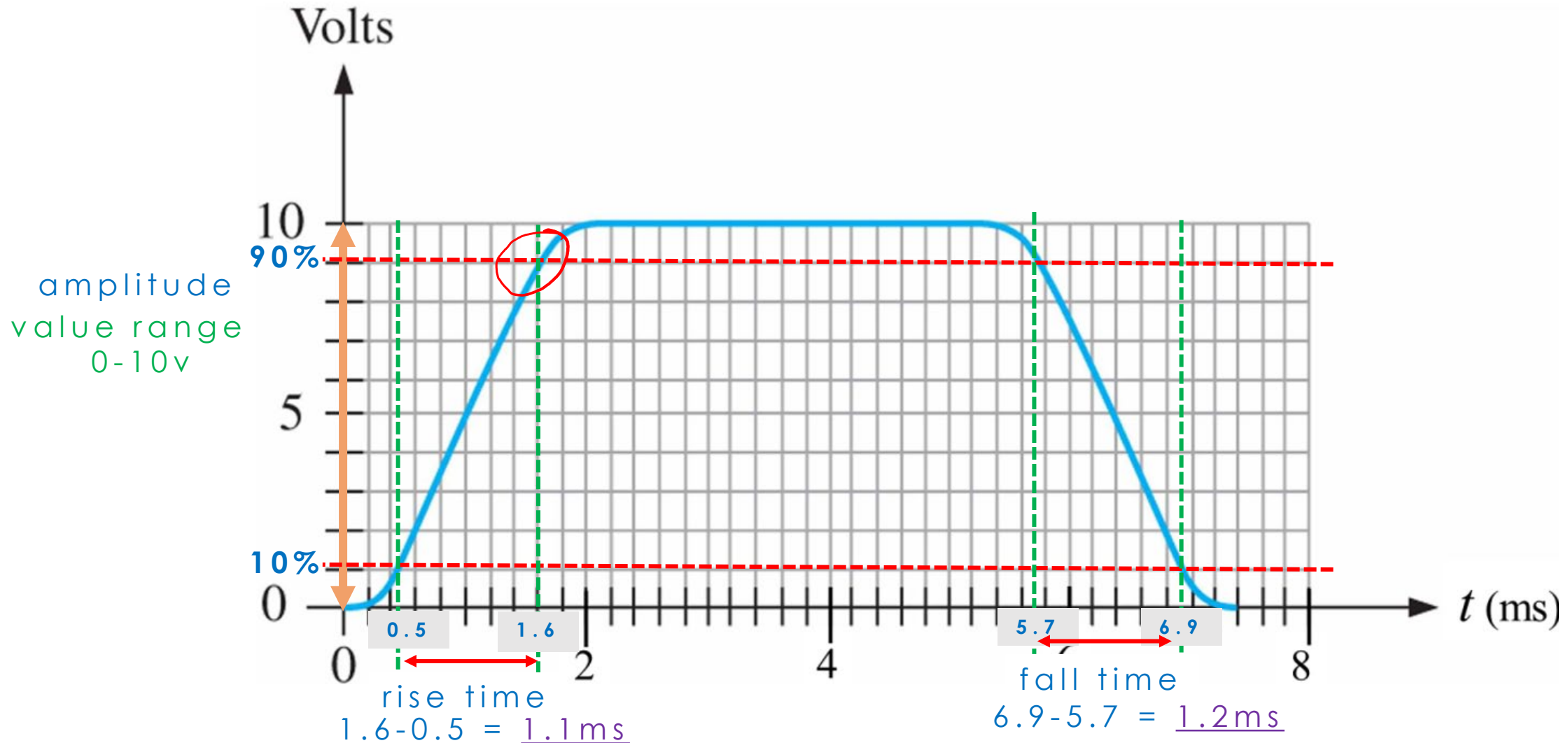
Identify and indicate the amplitude, rising/falling edge, period and pulse width components in the timing diagram below and their respective values.



IDEAL PULSES | PERIODIC TYPE

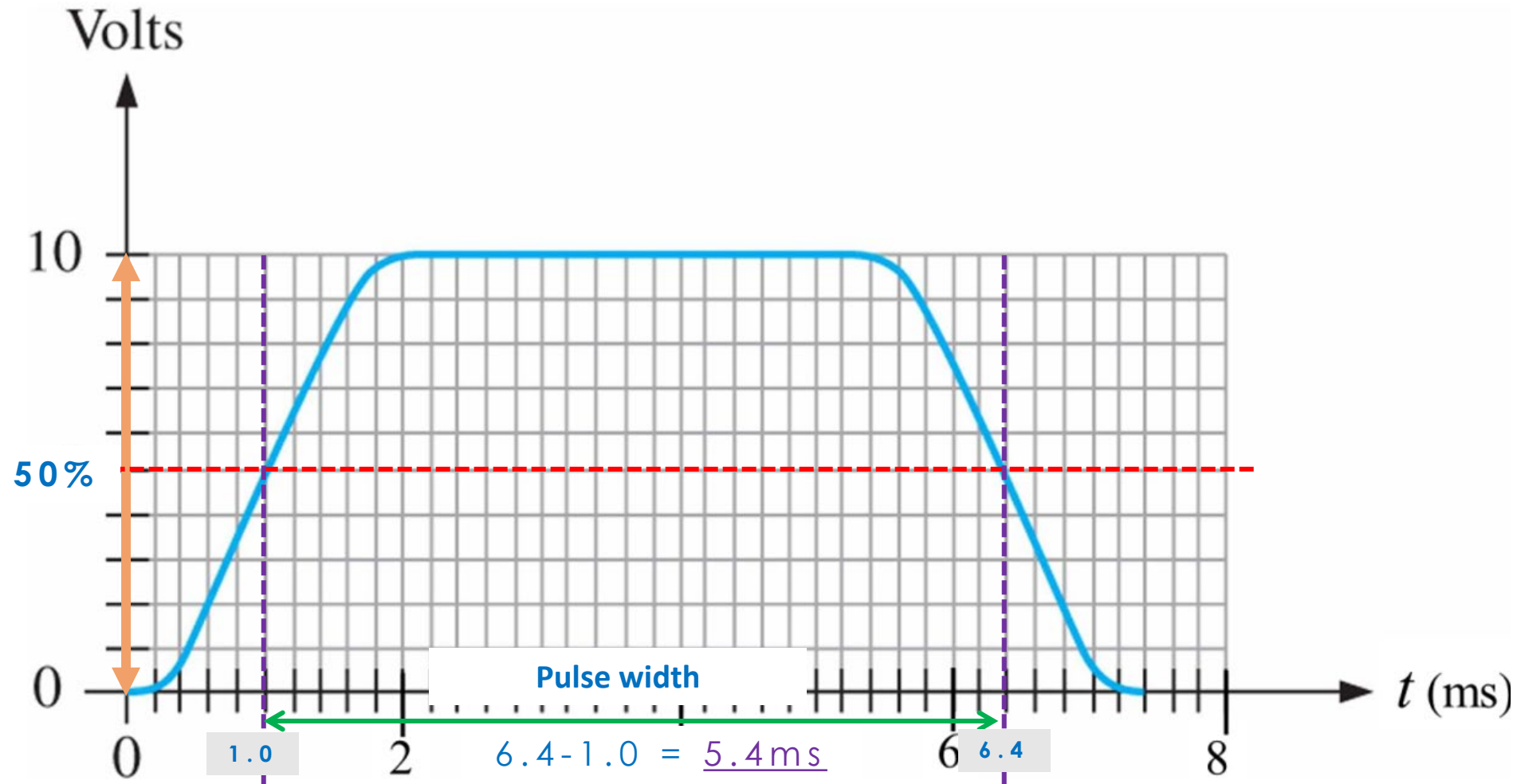
THEORY BASED QUESTIONS : QUESTION 2

Identify and indicate the amplitude, rise time, fall time, and pulse width components in the timing diagram below and their respective values.



THEORY BASED QUESTIONS : QUESTION 2

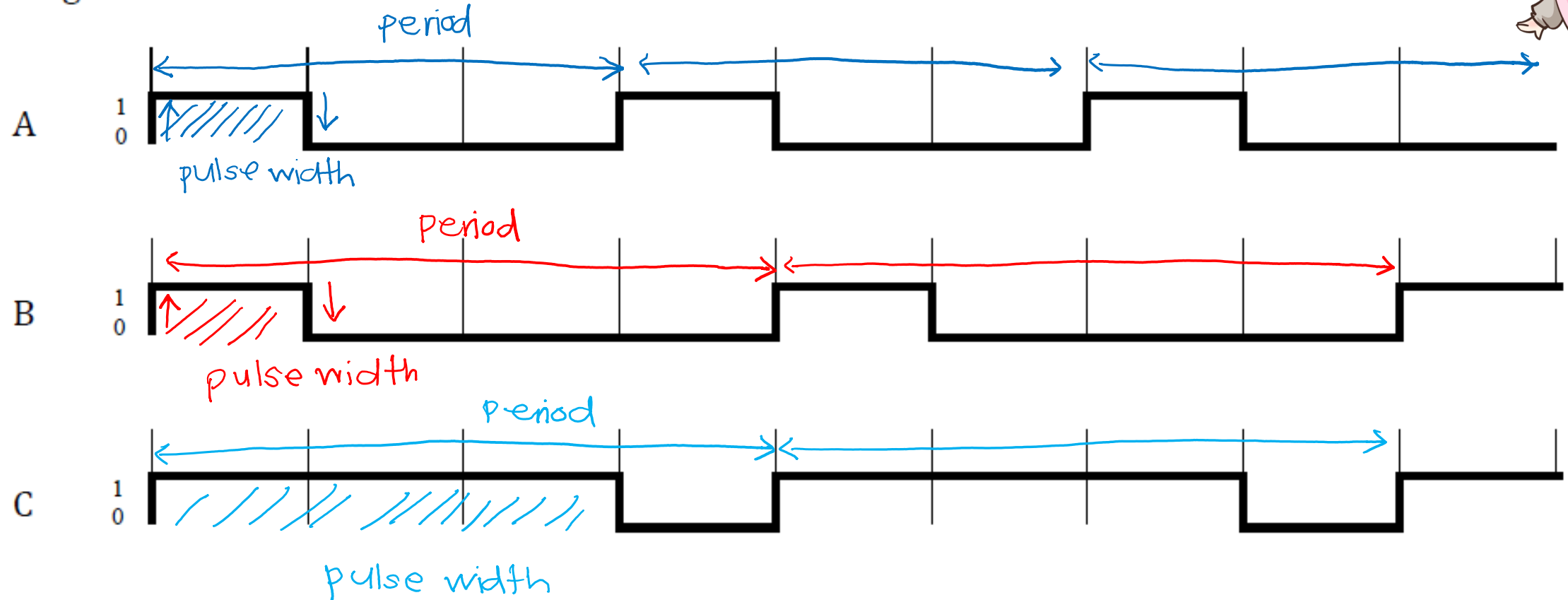
Identify and indicate the amplitude, rise time, fall time, and pulse width components in the timing diagram below and their respective values.



APPLIED KNOWLEDGE QUESTIONS : QUESTION 1

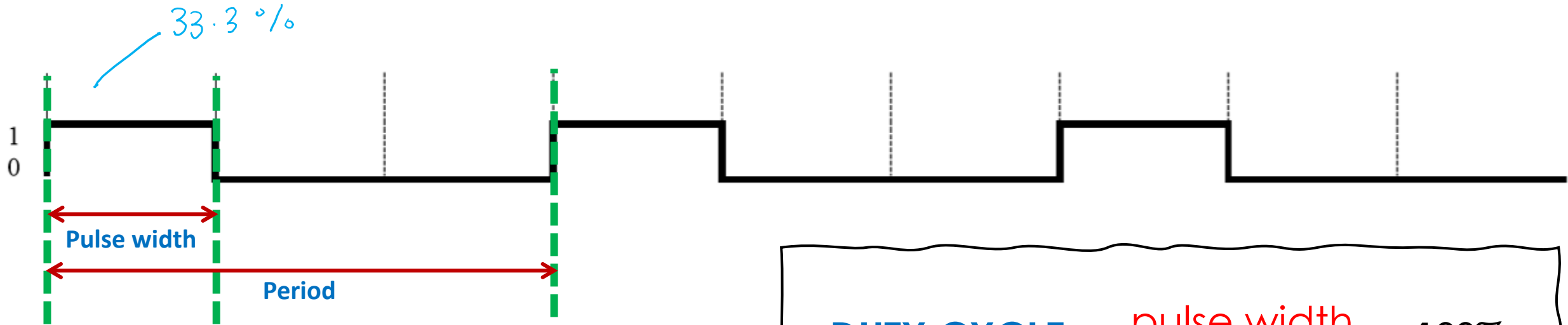


Identify the pulse width and period then calculate the *duty cycle* of the signals in the timing diagram shown below



APPLIED KNOWLEDGE QUESTIONS : QUESTION 1 (A)

Identify the **pulse width** and **period** then calculate the **duty cycle** of the signals in the timing diagram shown below.



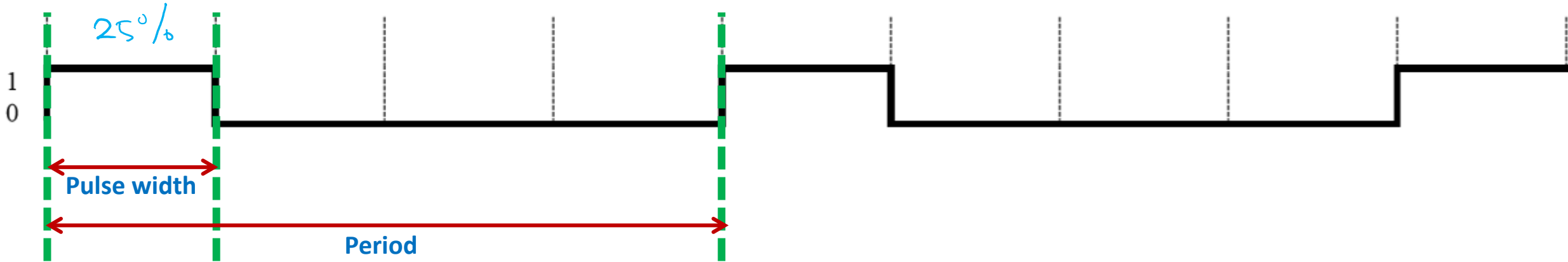
$$\begin{aligned}\text{Duty cycle} &= \frac{t_w}{T} \times 100\% \\ &= \frac{1}{3} \times 100\% \\ &= 33.3\%\end{aligned}$$

$$\begin{aligned}\text{DUTY CYCLE} &= \frac{\text{pulse width}}{\text{period}} \times 100\% \\ &= \frac{t_w}{T} \times 100\%\end{aligned}$$



APPLIED KNOWLEDGE QUESTIONS : QUESTION 1 (B)

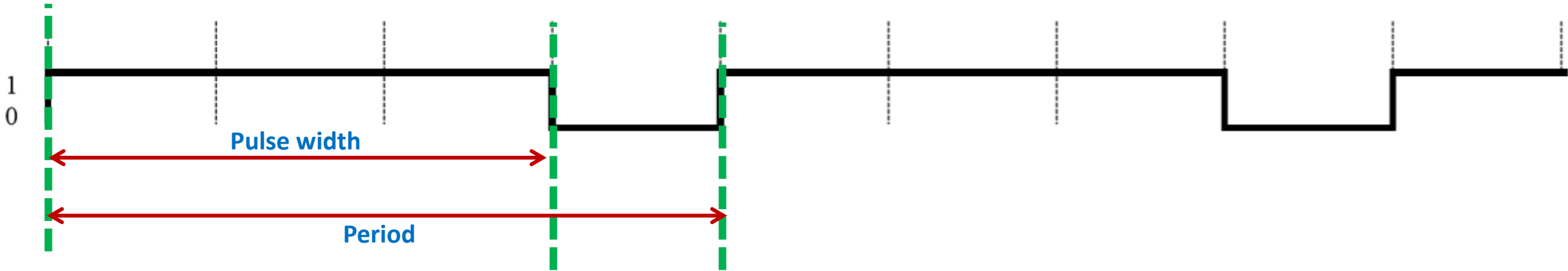
Identify the **pulse width** and **period** then calculate the **duty cycle** of the signals in the timing diagram shown below.



$$\begin{aligned}\text{Duty cycle} &= \frac{t_w}{T} \times 100\% \\ &= \frac{1}{4} \times 100\% \\ &= 25\%\end{aligned}$$

APPLIED KNOWLEDGE QUESTIONS : QUESTION 1 (C)

Identify the **pulse width** and **period** then calculate the **duty cycle** of the signals in the timing diagram shown below.

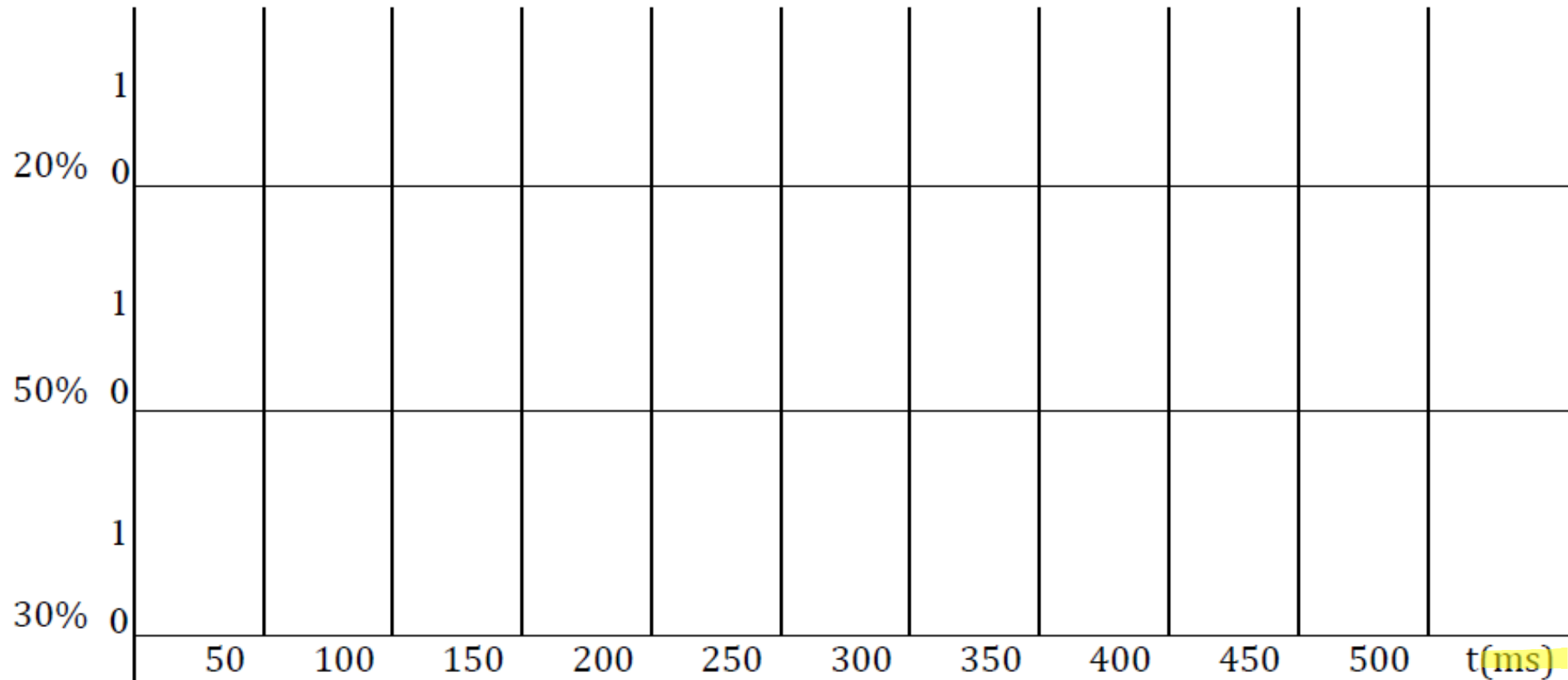


$$\begin{aligned}\text{Duty cycle} &= \frac{t_w}{T} \times 100\% \\ &= \frac{3}{4} \times 100\% \\ &= 75\%\end{aligned}$$

APPLIED KNOWLEDGE QUESTIONS : QUESTION 2



If given the frequency of a periodic signal is at 4Hz, use the following timing diagram scale to draw a signal when the duty cycle is at (a) 20%, (b) 50% and (c) 30%



APPLIED KNOWLEDGE QUESTIONS : QUESTION 2 (A)

If given the **FREQUENCY** of a periodic signal is at **4Hz**, use the following timing diagram scale **to draw** a signal when the **duty cycle is at 20%**



To draw a signal, you need PERIOD and PULSE WIDTH

Calculate PERIOD based on FREQUENCY given

$$\text{Period} = 1/\text{frequency}$$

$$\begin{aligned} T &= 1/f \\ &= 1/4 \\ &= 0.25 \text{ second} \times 1000 \\ &= 250\text{ms} \end{aligned}$$



APPLIED KNOWLEDGE QUESTIONS : QUESTION 2 (A)

To draw a signal, you need PERIOD and PULSE WIDTH

Period = 250ms | Duty cycle = 20%

$$\text{Duty cycle} = \frac{t_w}{T}$$

$$20/100 = \frac{t_w}{250}$$

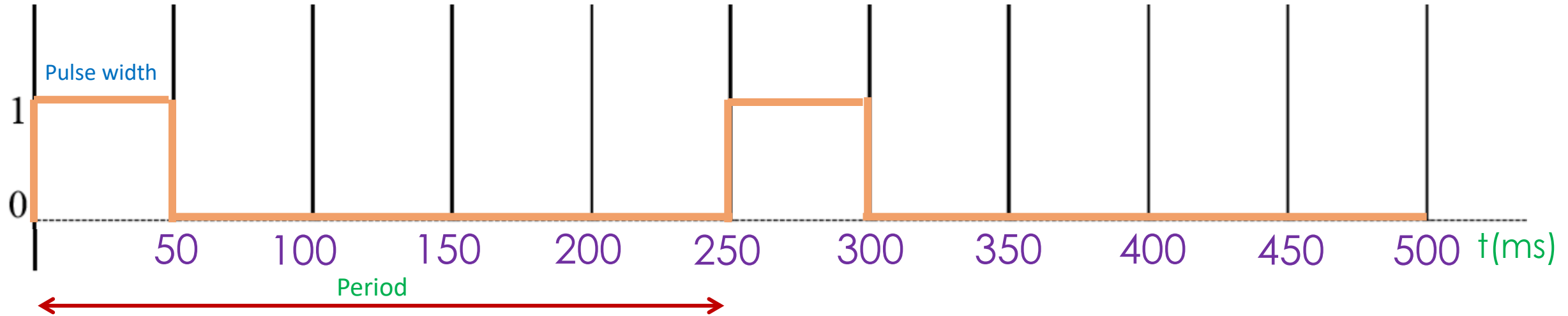
$$t_w = \frac{20}{100} \times 250$$

$$\text{pulse width} = 50\text{ms}$$

APPLIED KNOWLEDGE QUESTIONS : QUESTION 2 (A)

To draw a signal, you need PERIOD and PULSE WIDTH

Period = 250ms | Pulse width = 50ms





APPLIED KNOWLEDGE QUESTIONS : QUESTION 2 (B)

To draw a signal, you need PERIOD and PULSE WIDTH

Period = 250ms | Duty cycle = 50%

$$\text{Duty cycle} = \frac{t_w}{T}$$

$$50/100 = \frac{t_w}{250}$$

$$t_w = \frac{50}{100} \times 250$$

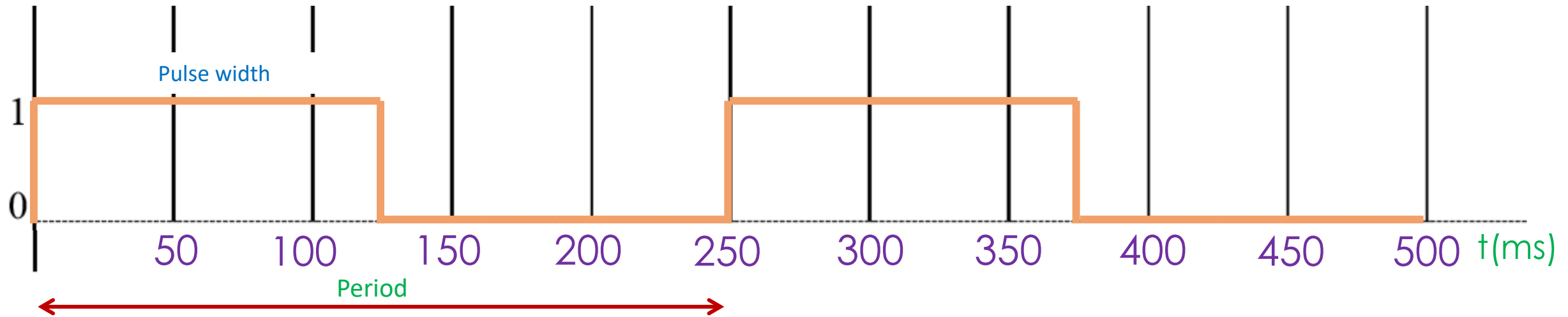
$$\text{pulse width} = 125\text{ms}$$



APPLIED KNOWLEDGE QUESTIONS : QUESTION 2 (B)

To draw a signal, you need PERIOD and PULSE WIDTH

Period = 250ms | Pulse width = 125ms





APPLIED KNOWLEDGE QUESTIONS : QUESTION 2 (C)

To draw a signal, you need PERIOD and PULSE WIDTH

Period = 250ms | Duty cycle = 30%

$$\text{Duty cycle} = \frac{t_w}{T}$$

$$30/100 = \frac{t_w}{250}$$

$$t_w = \frac{30}{100} \times 250$$

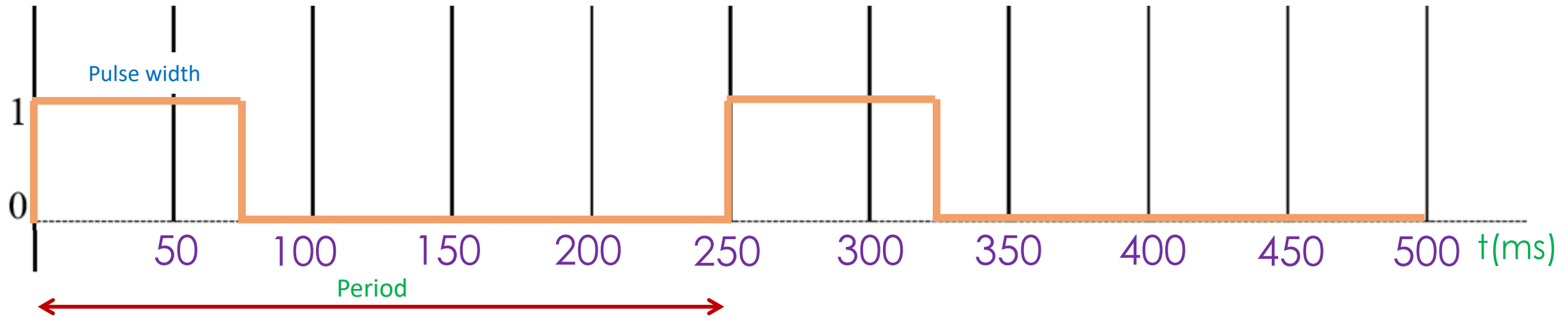
$$\text{pulse width} = 75\text{ms}$$



APPLIED KNOWLEDGE QUESTIONS : QUESTION 2 (C)

To draw a signal, you need PERIOD and PULSE WIDTH

Period = 250ms | Pulse width = 75ms



APPLIED KNOWLEDGE QUESTIONS : QUESTION 3

If binary data is transferred on a USB2.0 connection at a rate of 480Mbps, how long will it take (in theory) to transfer 4MB of data?

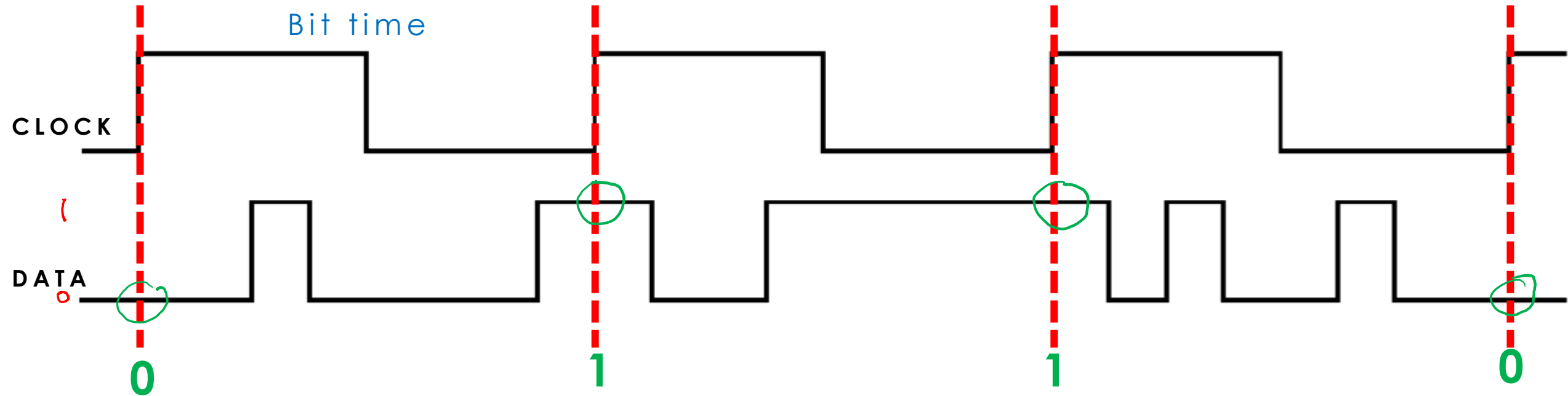
Transfer rate of USB2.0 = 480Mbps $\times 1000 \times 1000$
= 480 000 000 bits per second

File size = 4MB
= $4 \times 1024 \times 1024$ Bytes
= 4 194 304 Bytes $\times 8$
= 33 554 432 bits

Time to transfer file = 33 554 432 / 480 000 000
= 0.06 seconds

APPLIED KNOWLEDGE QUESTIONS : QUESTION 4

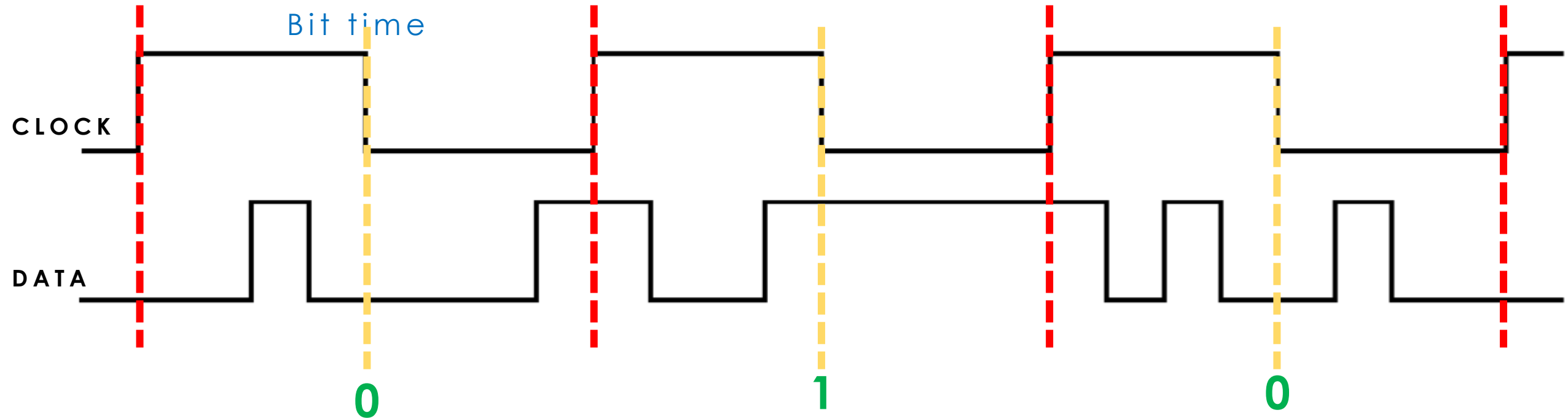
Using the timing diagram given, what is the BIT SEQUENCE transmitted if given that the sampling is done upon the RISING EDGE of the clock signal



Bit sequence = 0110

APPLIED KNOWLEDGE QUESTIONS : QUESTION 4 (EXTRA)

Using the timing diagram given, what is the BIT SEQUENCE transmitted if given that the sampling is done upon the **FALLING EDGE** of the clock signal



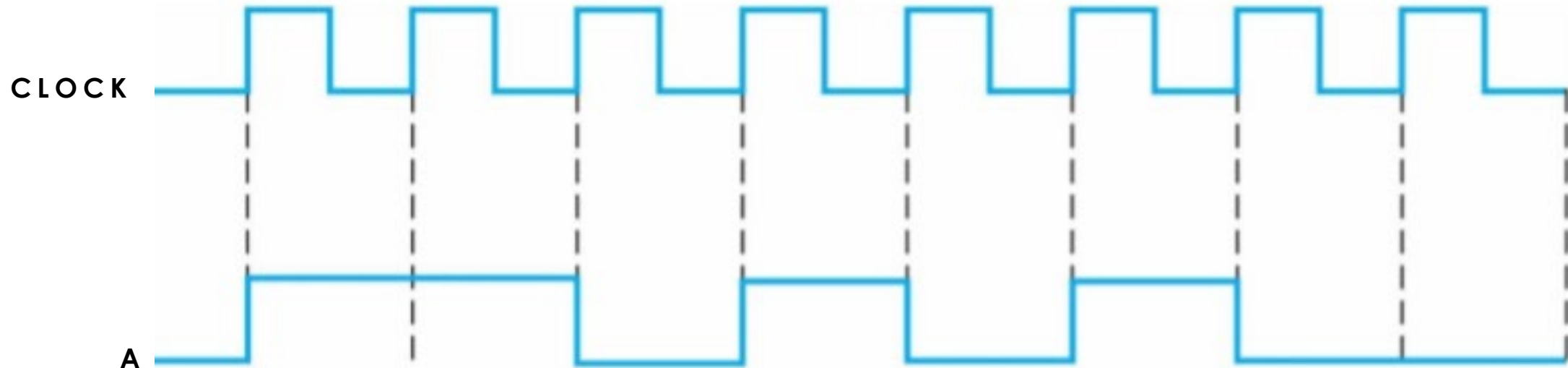
Bit sequence = 010



APPLIED KNOWLEDGE QUESTIONS : QUESTION 5

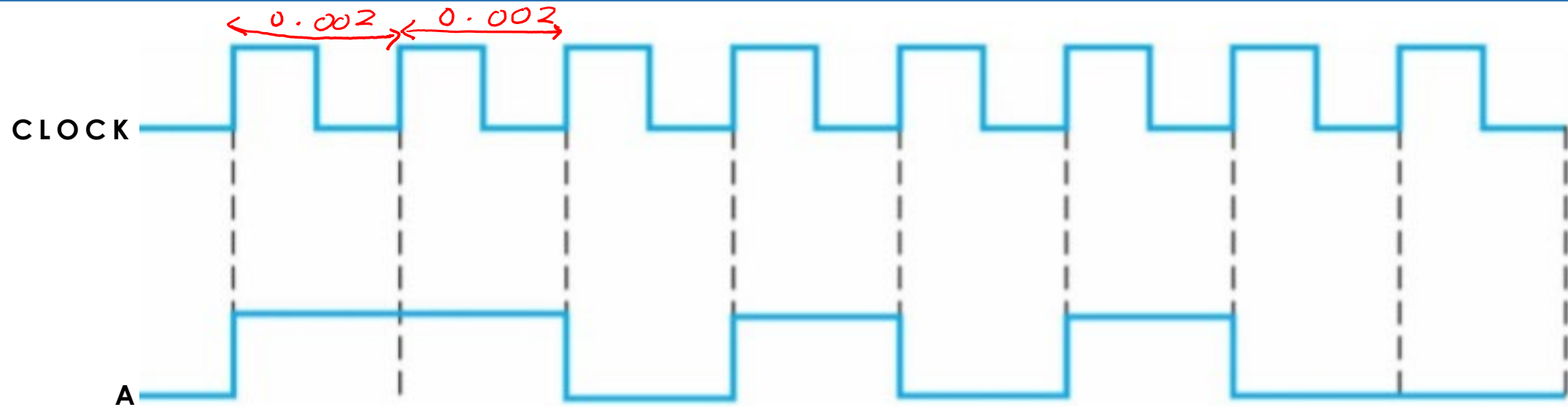
Based on the waveform above, determine

- a) The bit time if given the reference clock is running at 500Hz
- b) The bit sequence transferred by A
- c) The total time to transfer the bits serially
- d) The total time to transfer the same bits in parallel



APPLIED KNOWLEDGE QUESTIONS : QUESTION 5 (a)

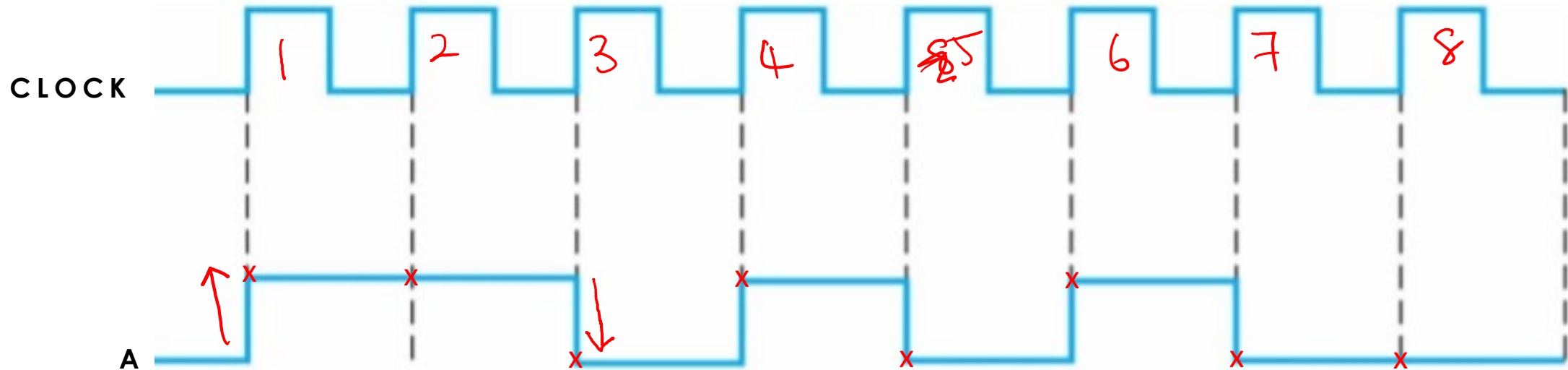
Determine the bit time if given the reference clock is running at 500Hz



$$\begin{aligned}\text{Bit time} &= \text{PERIOD of clock} \\ &= 1/\text{frequency} \\ &= 1/500 \\ &= 0.002 \text{ second} \times 1000 \\ &= 2 \text{ milliseconds} / 2\text{ms}\end{aligned}$$

APPLIED KNOWLEDGE QUESTIONS : QUESTION 5 (b)

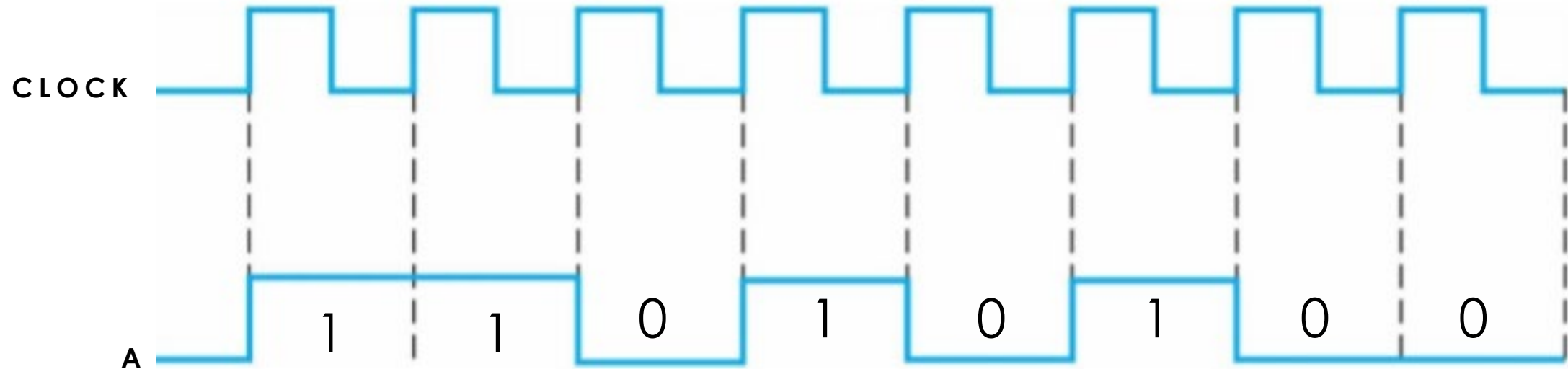
Determine the bit sequence transferred by A



Bit sequence = 11010100

APPLIED KNOWLEDGE QUESTIONS : QUESTION 5 (c)

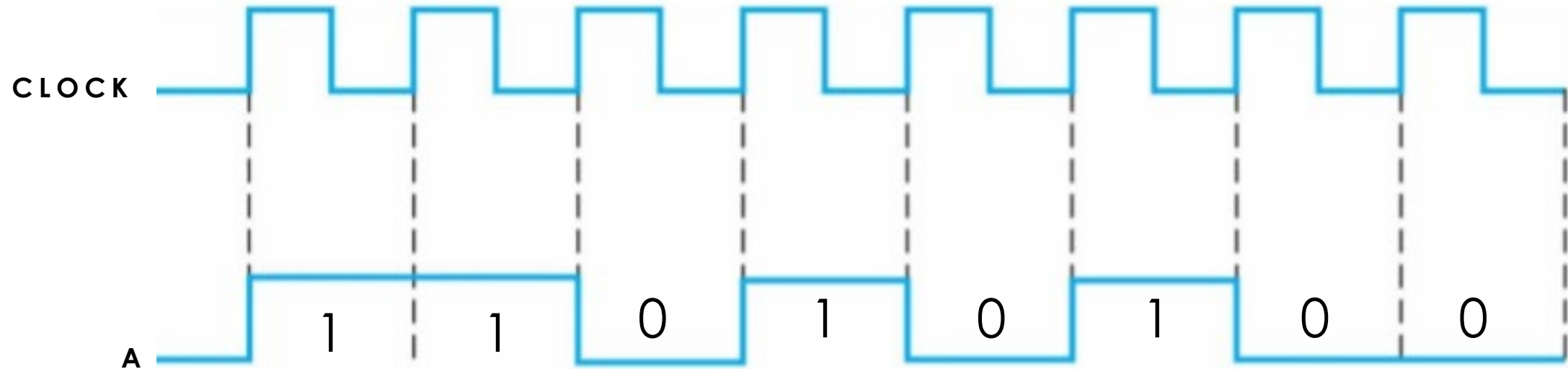
Determine the total time to transfer the bits serially



$$\begin{aligned}\text{Transfer time} &= 8 \text{ bits} \times 2\text{ms} \\ &= 16\text{ms}\end{aligned}$$

APPLIED KNOWLEDGE QUESTIONS : QUESTION 5 (d)

Determine the total time to transfer the same bits in parallel



2 ms

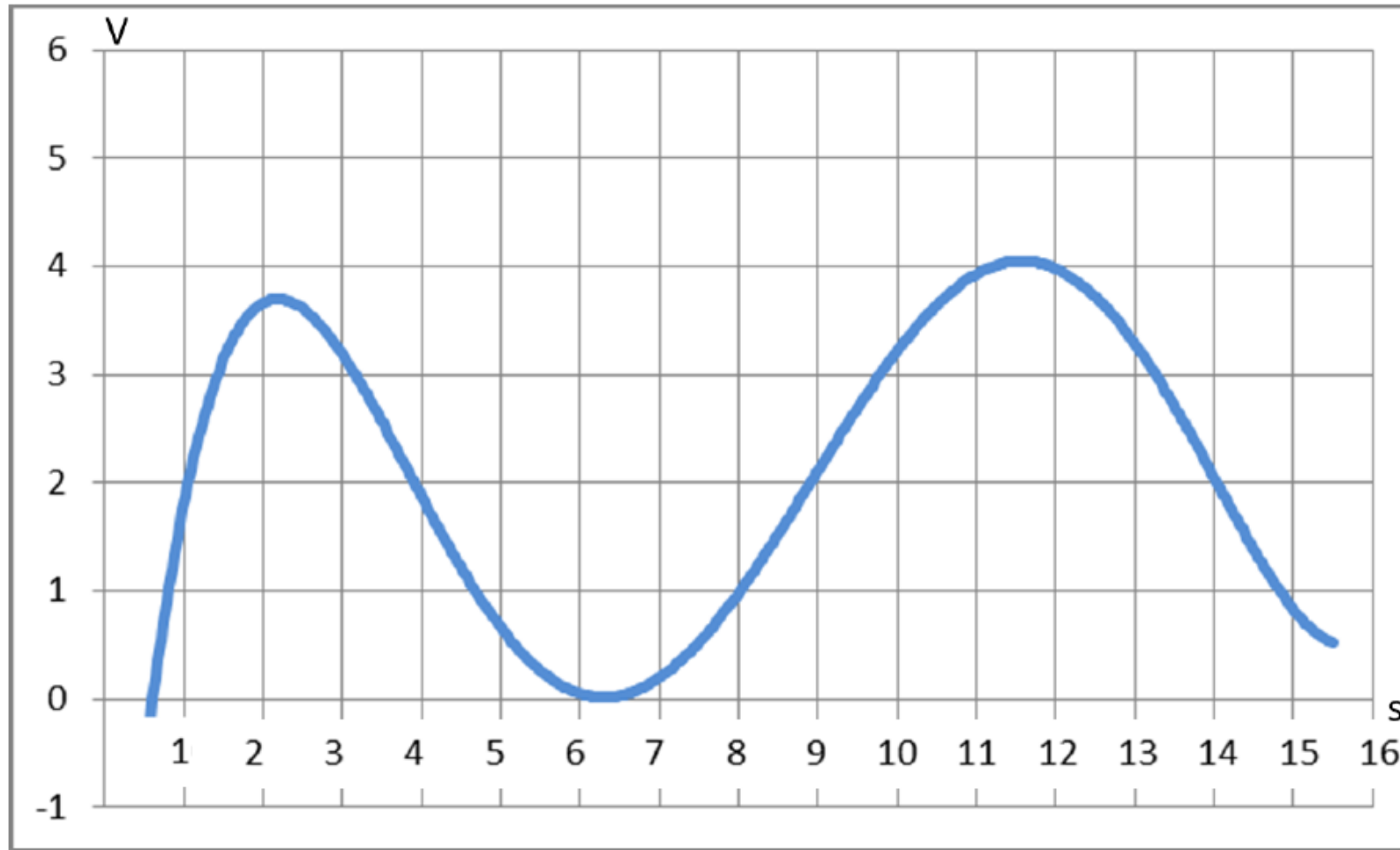
~~0.02~~

|||||

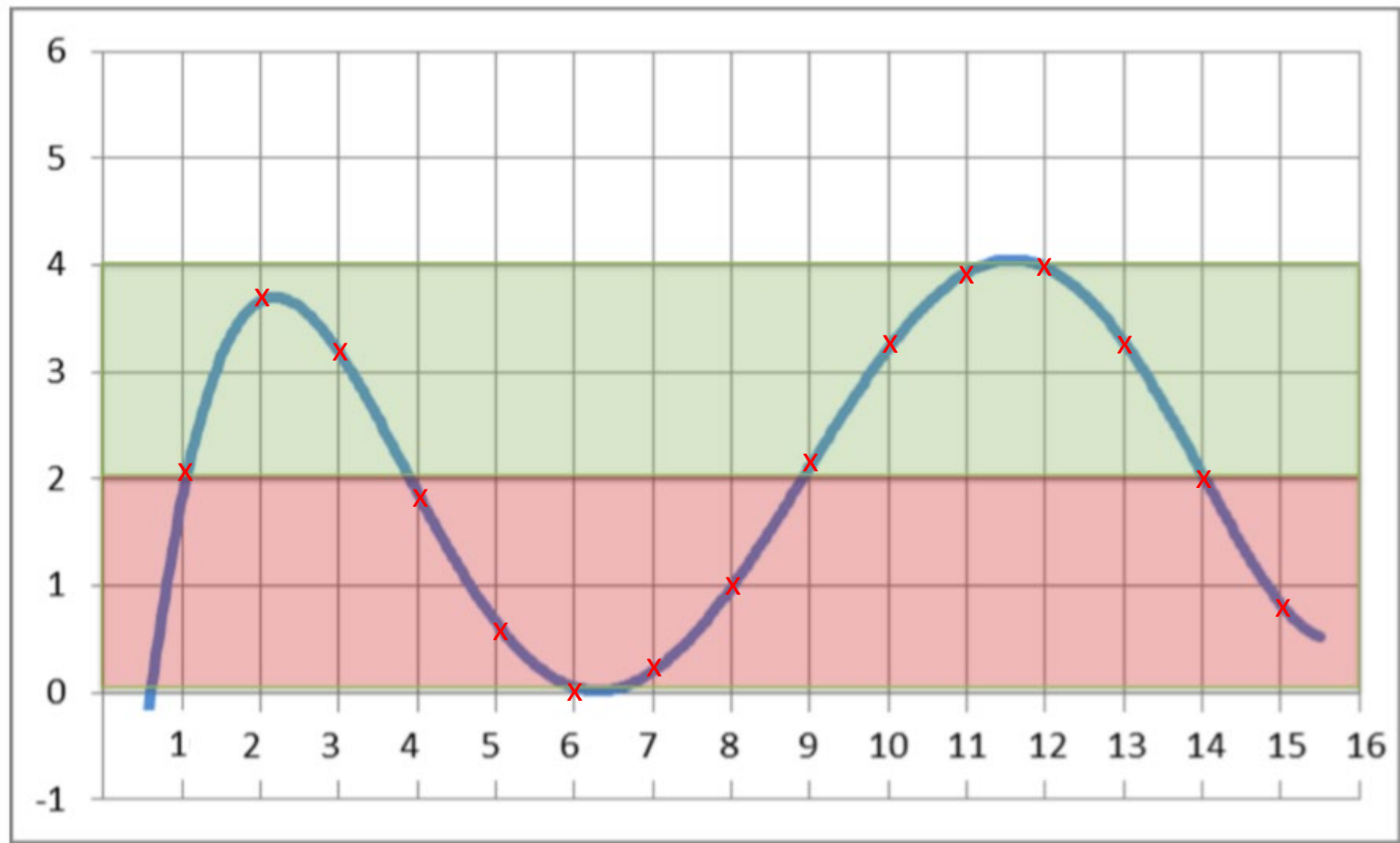
parallel

Parallel transfer time = 2ms

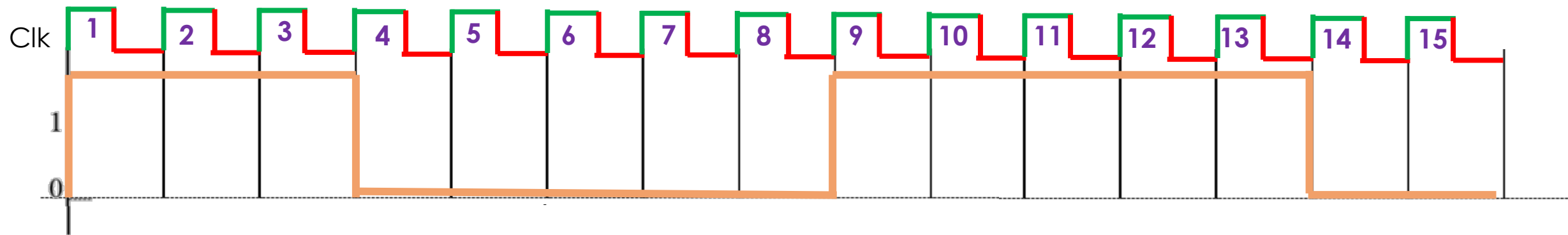
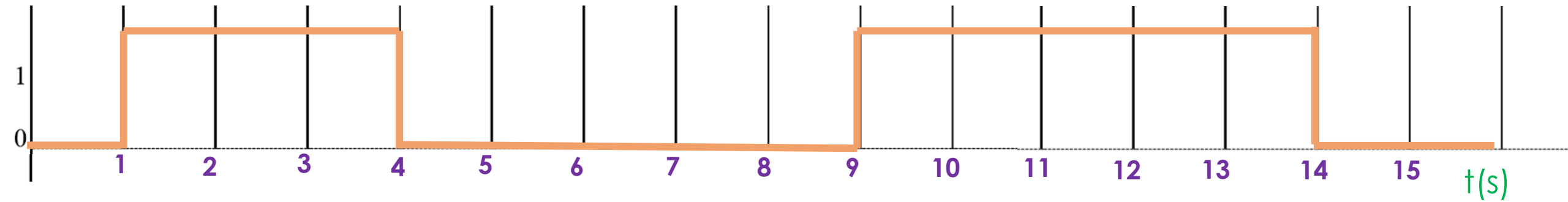
APPLIED KNOWLEDGE QUESTIONS : QUESTION 6



The waveform diagram above shows a recorded analog signal of voltage against time in seconds. Draw the resulting binary digital waveform assuming that an ADC samples this signal once (1) every second at the rising edge of its clock signal and given that TTL levels for high are between 2-4V and low between 0-1V. It can be assumed that any values in the *unacceptable range* fall to low.



APPLIED KNOWLEDGE QUESTIONS : QUESTION



END DISCUSSIONS

ANY QUESTIONS ??

