MULTIMEDIA UNIVERSITY

PDS0101 Introduction to Digital Systems

Tutorial 7

Tutorial outcomes

By the end of today's tutorial, you should be able to

- distinguish between combinational and sequential circuits
- identify the different latches
- define/describe/show how latch works as a device for storage

Theory based questions

1. What are the differences between combinational and sequential circuits?

2. How many 'states' can a S-R latch transition into?

3. Draw the logic circuit and block diagram for an active-LOW S-R latch – show the alternatives possible in the logic circuit diagram
   - What is an alternative name for the active-LOW S-R latch?
   - Complete the truth table for the active-LOW S-R latch

4. Draw the logic circuit and block diagram for an active-HIGH S-R latch – show the alternatives possible in the logic circuit diagram
   - What is an alternative name for the active-HIGH S-R latch?
   - Complete the truth table for the active-HIGH S-R latch

5. Explain how an active-LOW S-R latch transitions from resting/stable state into set state and then into reset state.

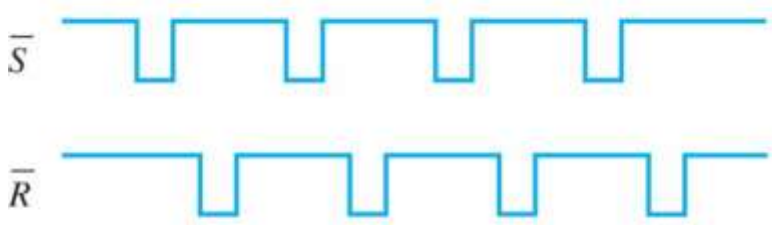
6. What happens when both inputs to the NAND S-R latch are set to HIGH?

7. What happens when both inputs to the negative-AND S-R latch are set to HIGH?

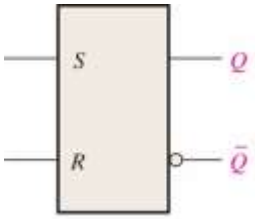
8. Why is it not possible for a gated D-latch to fall into an invalid state?

Applied-knowledge based questions

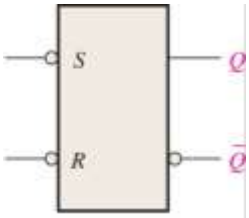
1. The waveforms in the timing diagram are applied to the latches shown below. Draw the resulting output waveform at Q in relation to the inputs assuming that Q starts low.



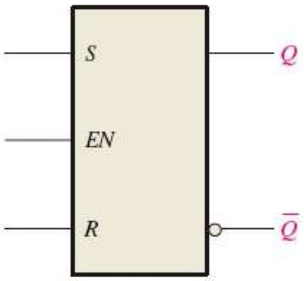
a)



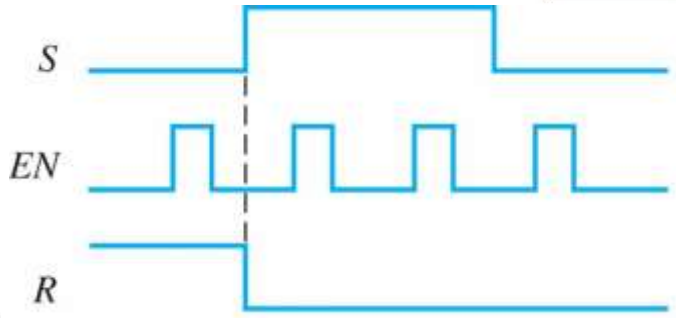
b)



2. Determine the Q and Q' inputs for the inputs of S and R to the following latch given that the Q output is initially LOW



a)



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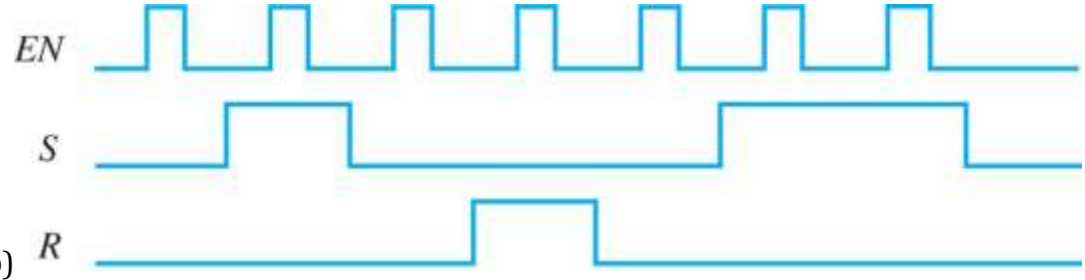
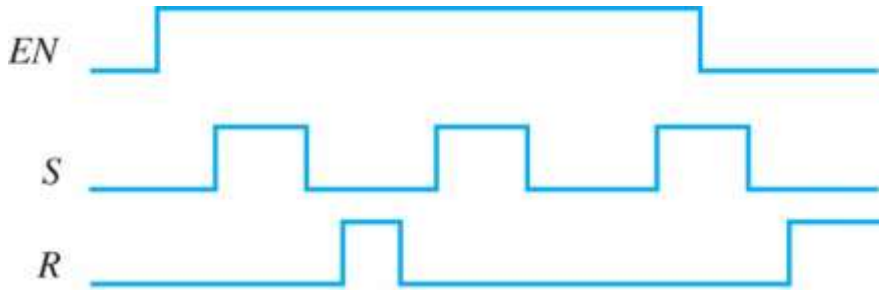
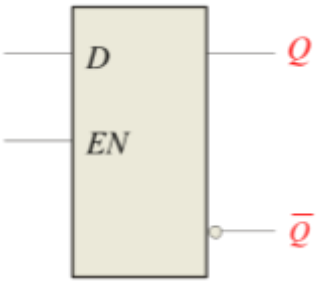
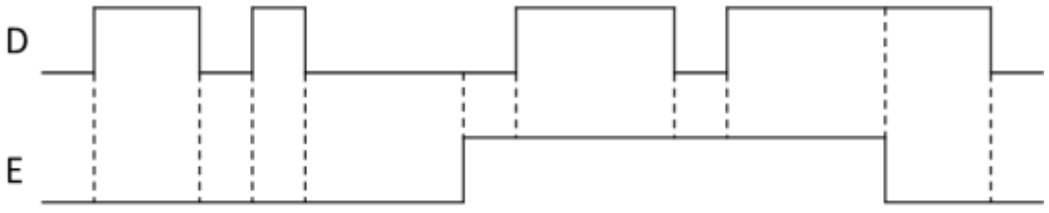




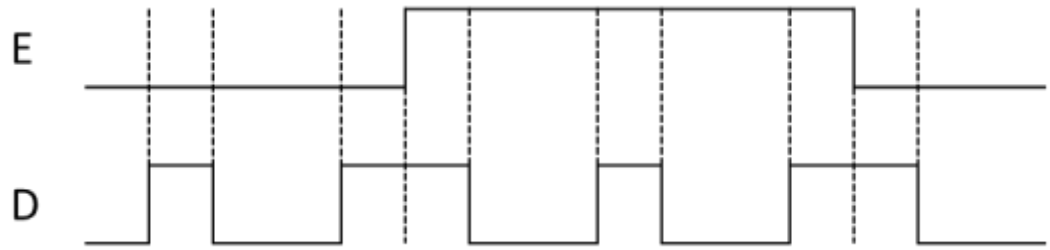
c)

3. Given the following latch, determine the outputs for Q and Q' with the inputs shown if given that the Q output for the latch is initially LOW

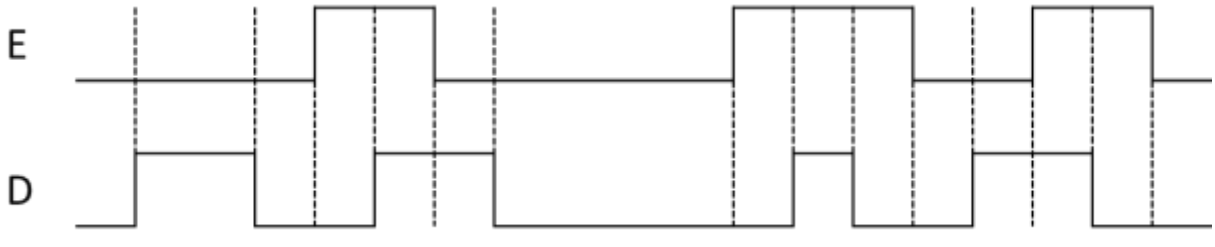




a)



b)



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