MMU
MULTIMEDIA UNIVERSITY

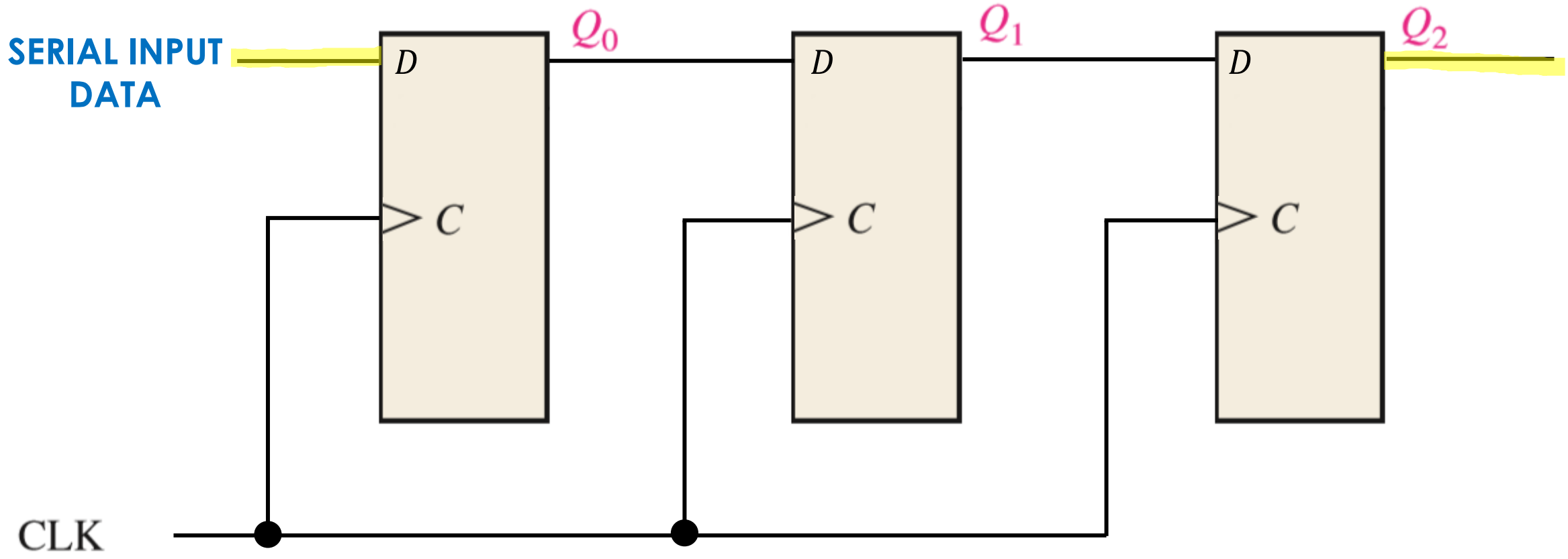
TUTORIAL 10
COUNTER & SHIFT REGISTER

PDS0101: INTRODUCTION TO DIGITAL SYSTEMS
TRI 2, 2022-2023

QUESTIONS 1

Draw the logic circuit diagram for a **3-bit serial in/serial out shift register .**

Which **FFs** do you use? **D FF**



QUESTIONS 2

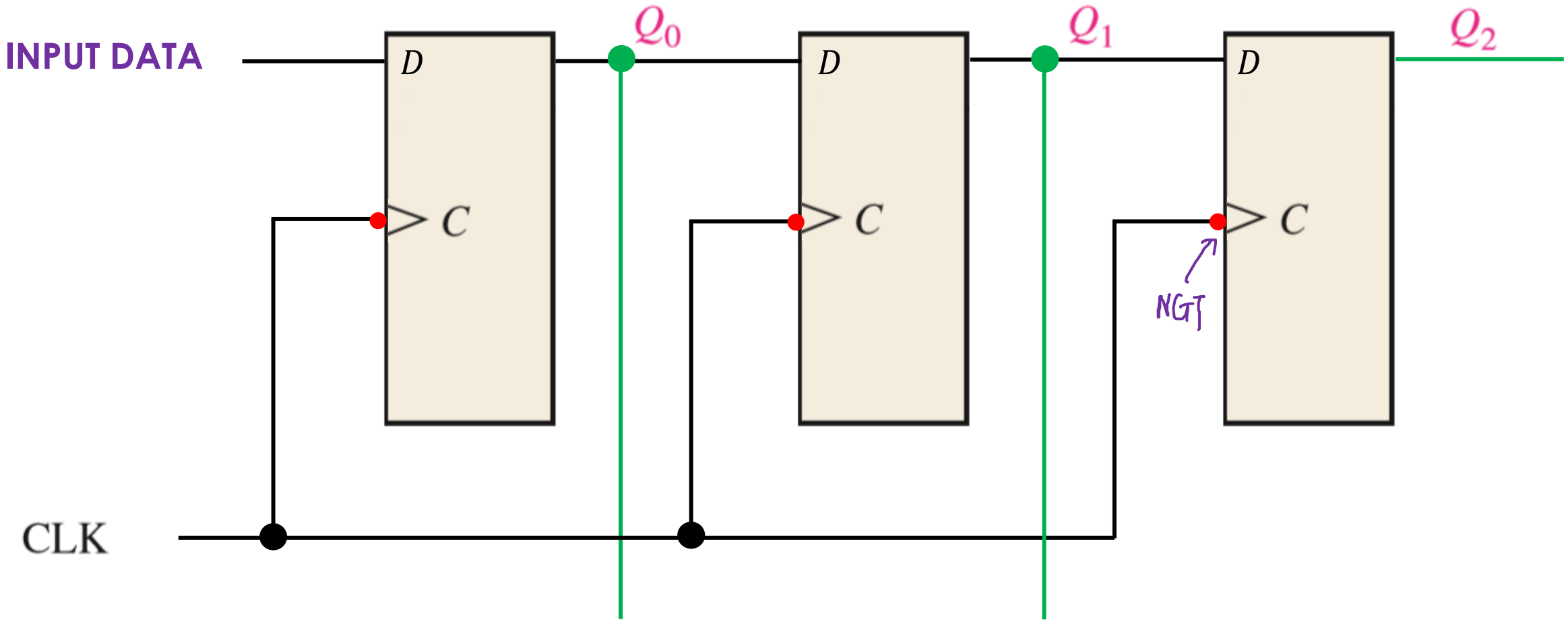
SI PO

Sync

Revise the circuit from (1) to create a **3-bit serial in / parallel out shift register**

NGT

PARALLEL OUT



QUESTIONS 3

Q_0, Q_1, Q_2, Q_3

The sequence **1011** is applied to the input line of a **4-bit serial shift register**. If the **register** is initially **cleared**, what is the **state of the register after 3 clock pulses**?

MSB ↖ 1011 ↙ LSB

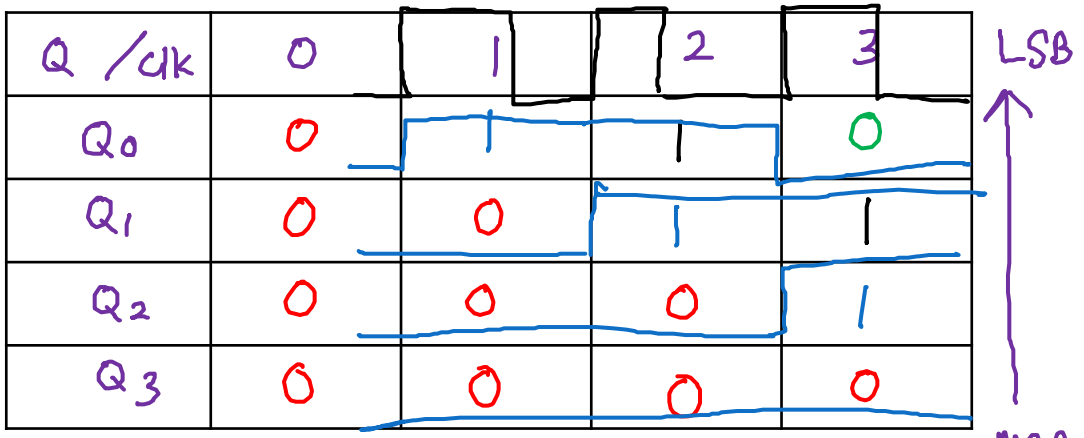
Start insert using LSB

Clk / Q	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	0	1	1	0

LSB ← MSB

$Q_3 Q_2 Q_1 Q_0 = 0110$

Similar with timing diagram



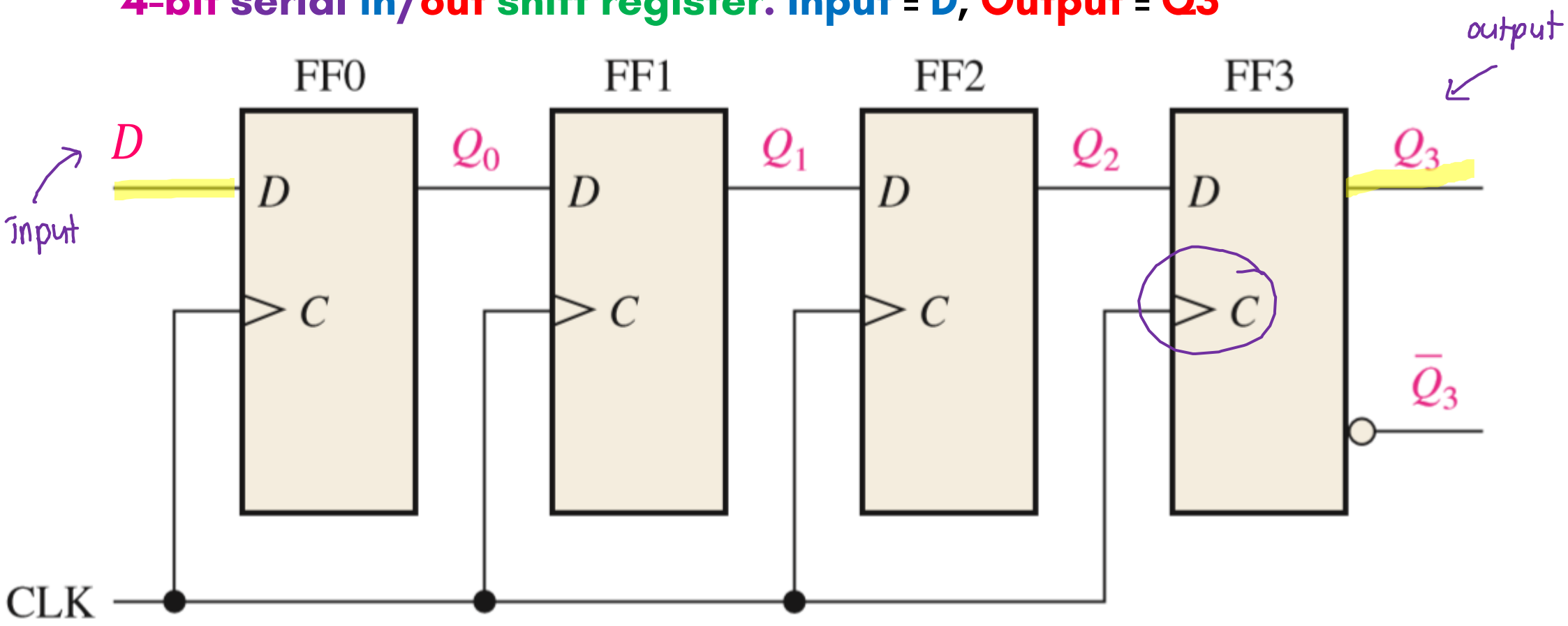
$Q_3 Q_2 Q_1 Q_0 = 0110$

QUESTIONS 4

Identify the **shift register** shown in the diagram below. Then identify which is the **input** and output for the register

PGT

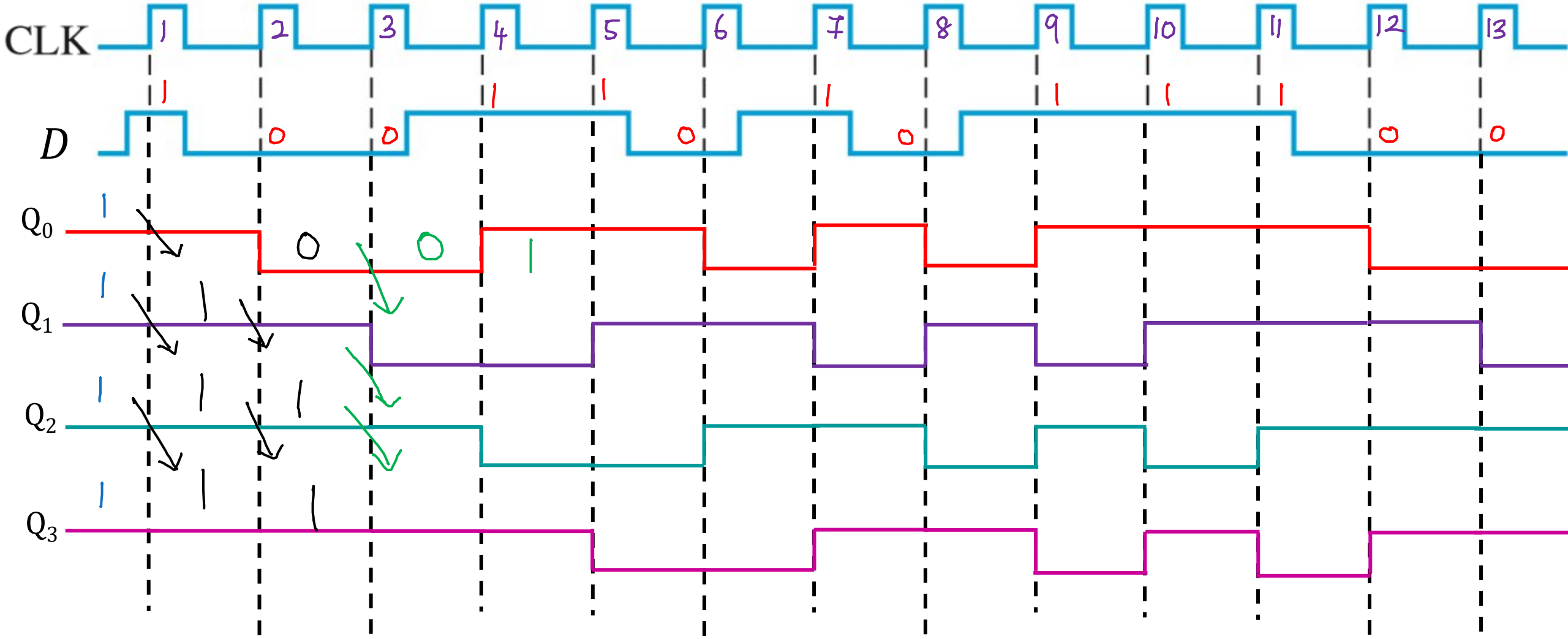
4-bit serial in/out shift register. Input = D, Output = Q3



QUESTIONS 5 (a)

Q_D follow D

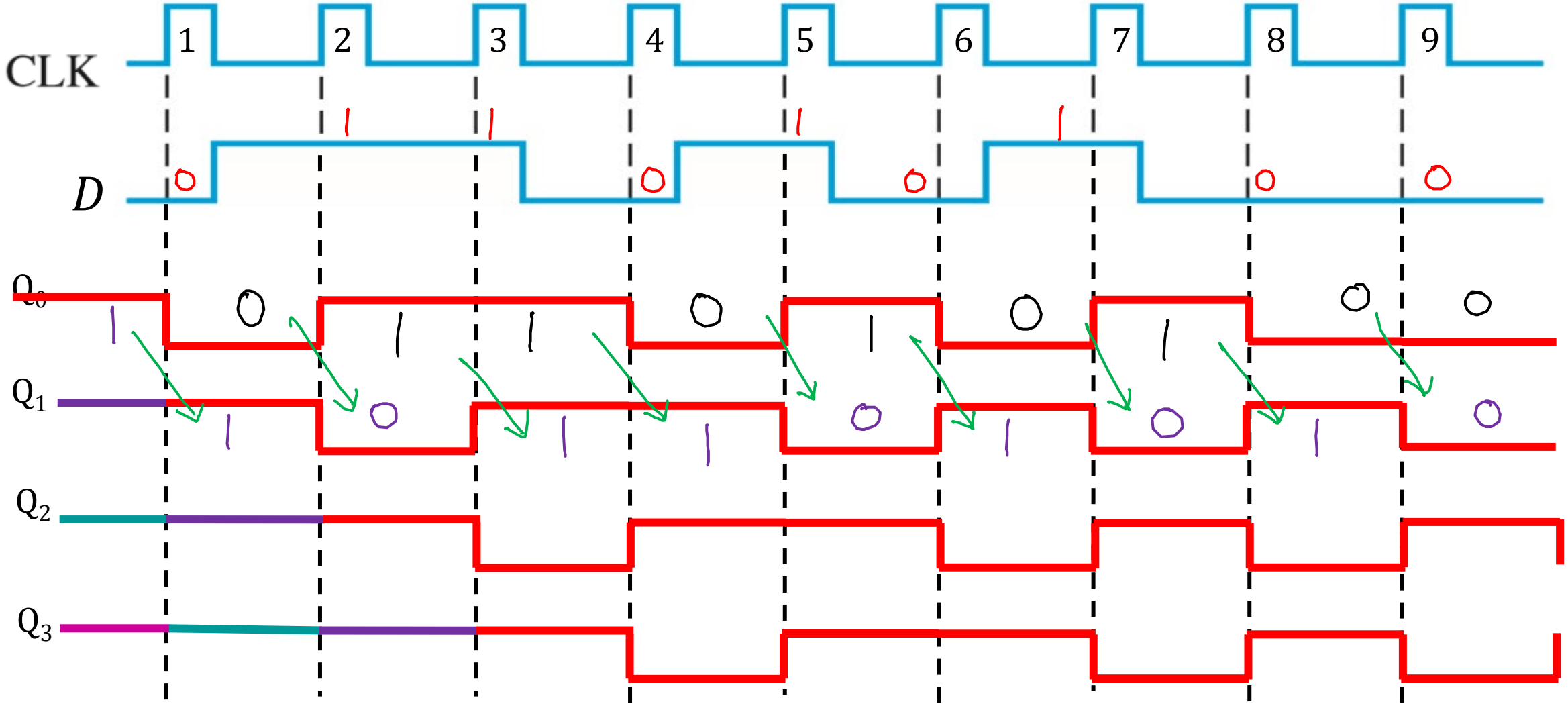
Using the register above in (4), determine the state of each flip-flop and show the Q waveforms in with the data inputs and clock timing diagrams shown PGT below. The register has all 1's in each FF when it begins.



QUESTIONS 5(b)

Q_0 follow D

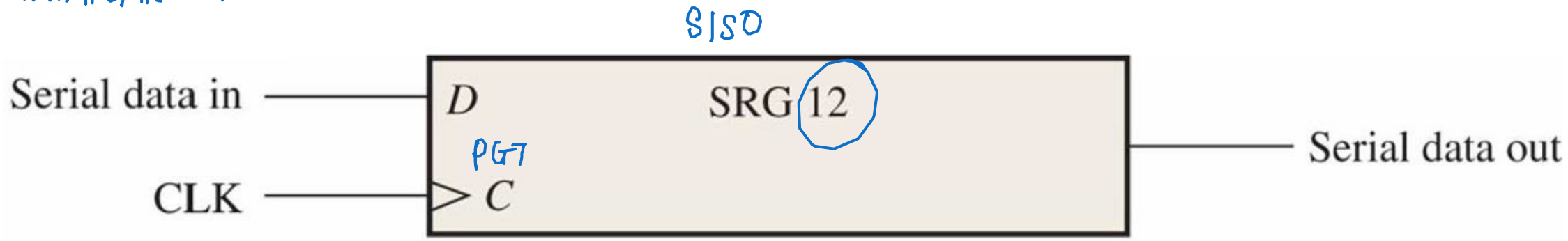
Using the register above in (4), determine the state of each flip-flop and show the Q waveforms in with the data inputs and clock timing diagrams shown below. The register has all 1's in each FF when it begins.

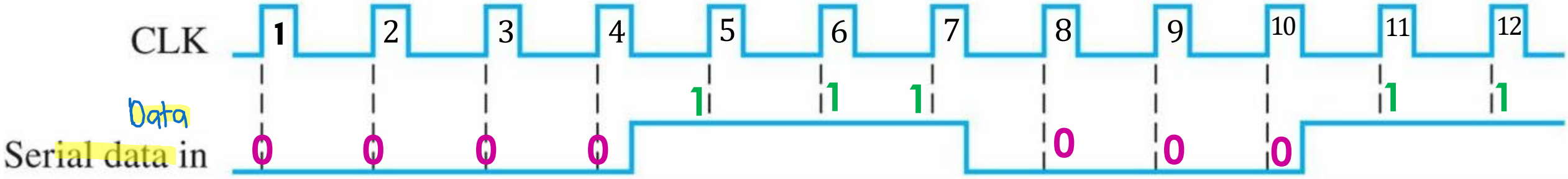


QUESTIONS 6

What is the state of the register below after each clock pulse if it starts in the **101001111000** state?

Initial state



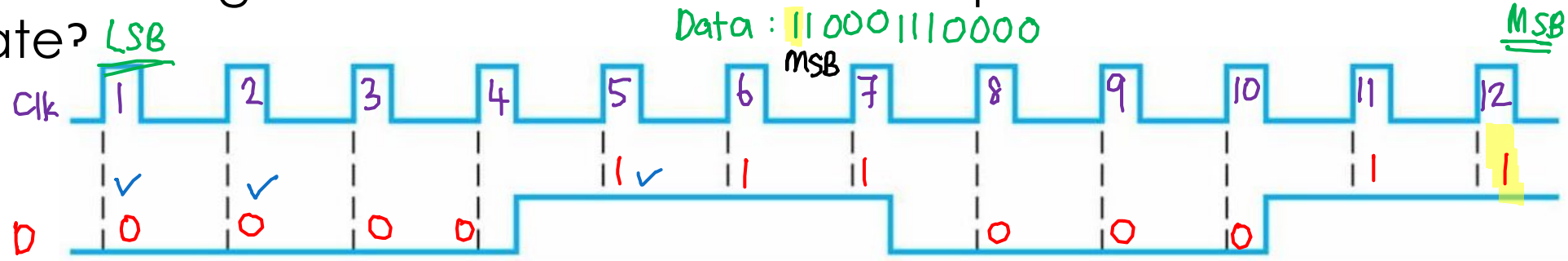


QUESTIONS 6

What is the state of the register below after each clock pulse if it starts in the **101001111000** state?

└ initial state

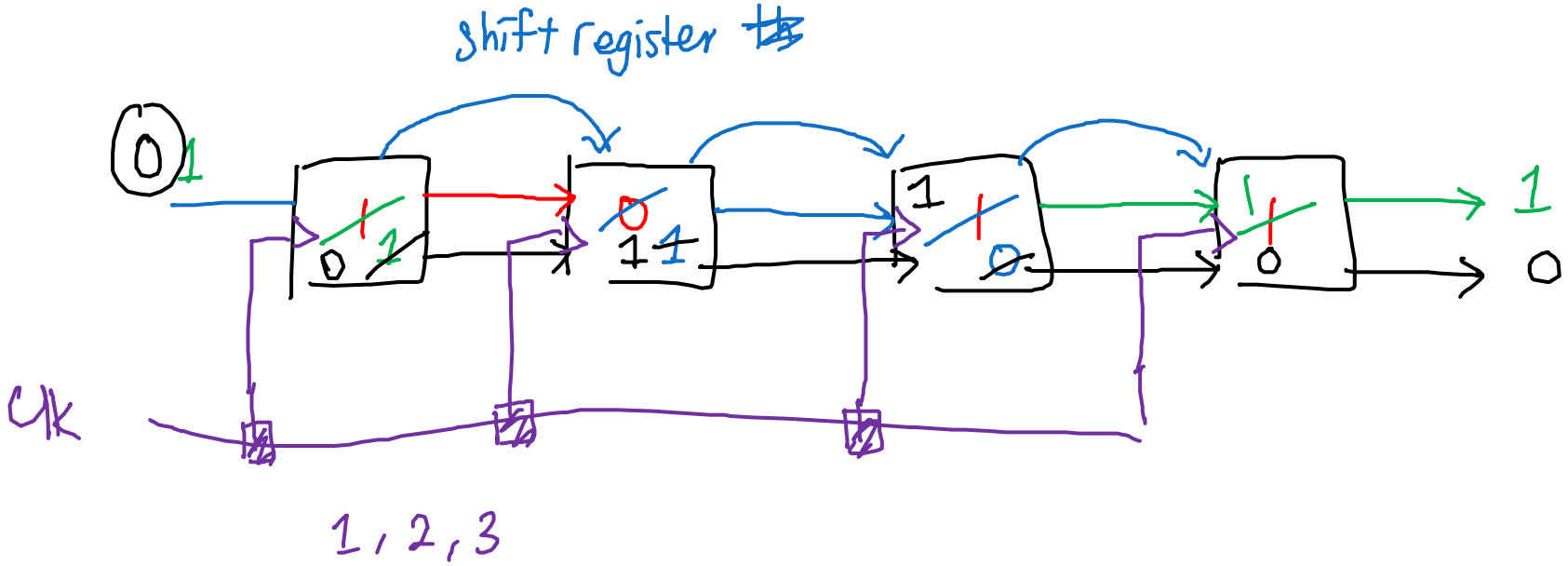
Data : 110001110000



Clk/Q	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}
0	1	0	1	0	0	1	1	1	1	0	0	0
1	0	1	0	1	0	0	1	1	1	1	0	0
2	0	0	1	0	1	0	0	1	1	1	1	0
3	0	0	0	1	0	1	0	0	1	1	1	1
4	0	0	0	0	1	0	1	0	0	1	1	1
5	1	0	0	0	0	1	0	1	0	0	1	1
6	1	1	0	0	0	0	1	0	1	0	0	1
7	1	1	1	0	0	0	0	1	0	1	0	0
8	0	1	1	1	0	0	0	0	1	0	1	0
9	0	0	1	1	1	0	0	0	0	1	0	1
10	0	0	0	1	1	1	0	0	0	0	1	0
11	1	0	0	0	1	1	1	0	0	0	0	1
12	1	1	0	0	0	1	1	1	0	0	0	0

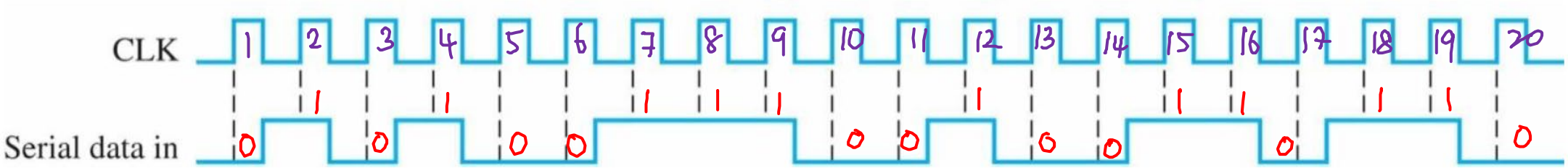
Q/C	0	1	2	3	4	5	6	7	8	9	10	11	f...
Q_0	1	0	0	0									
Q_1	0	1	0										
Q_2	1	0	1										
Q_3	0	1	0										
Q_4	0	0	1										
Q_5	1	0	0										
Q_6	1	1	0										
Q_7	1	1	1										
Q_8	1	1	1										
Q_9	0	1	1										
Q_{10}	0	0	1										
Q_{11}	0	0	0										

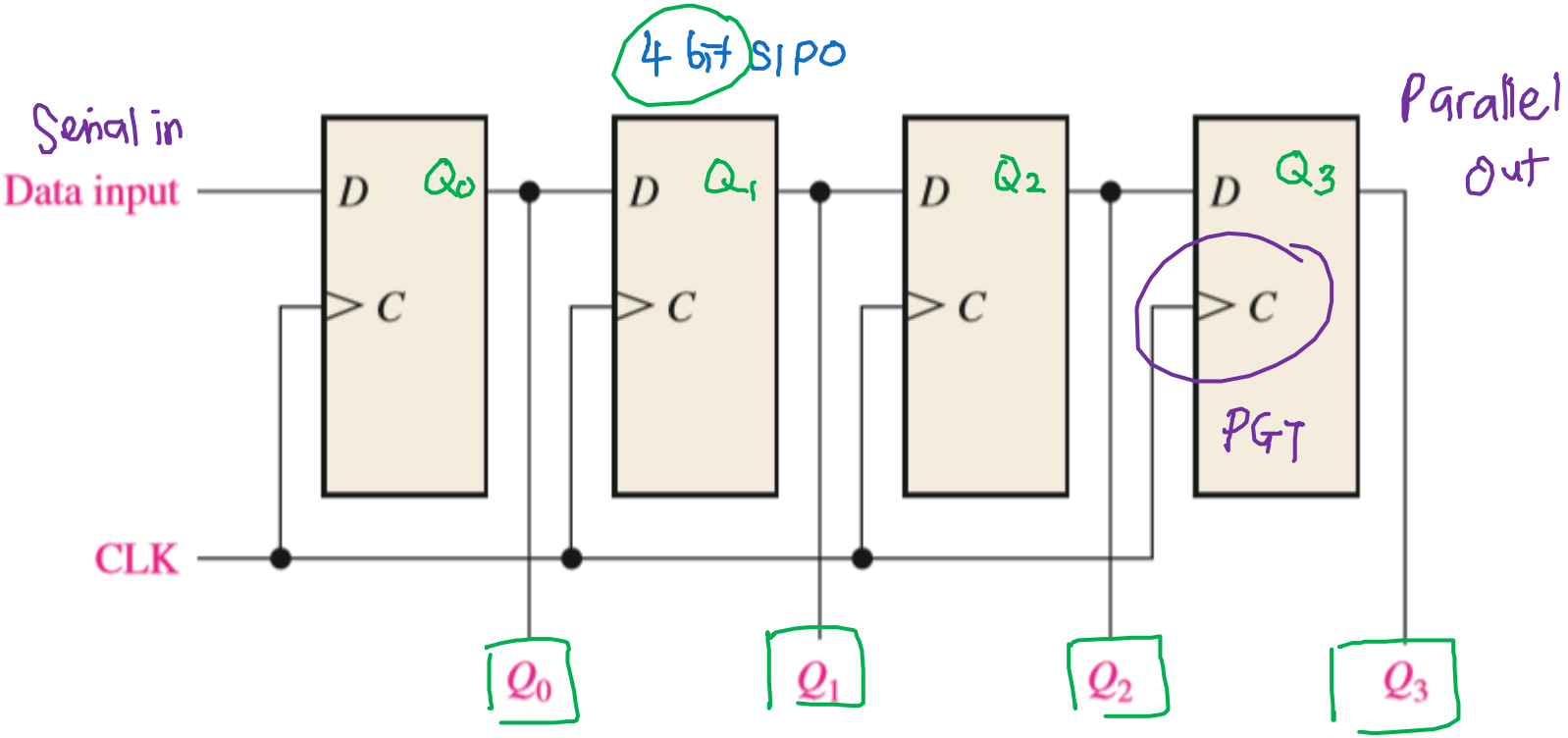
Sync

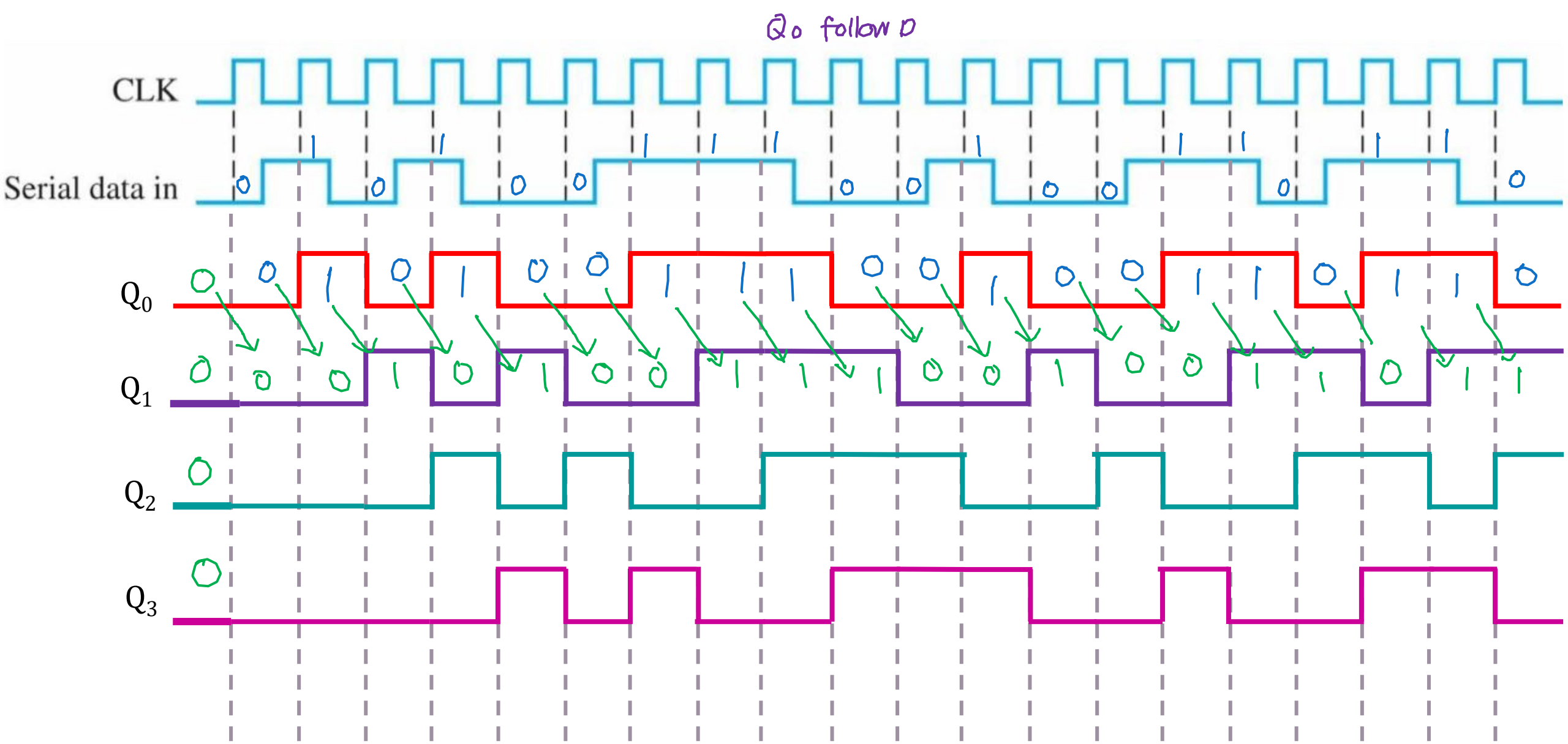


QUESTIONS 7

Identify and show the timing diagram including the **parallel outputs** for the shift register below using the given input waveform (the register is **initially clear**)

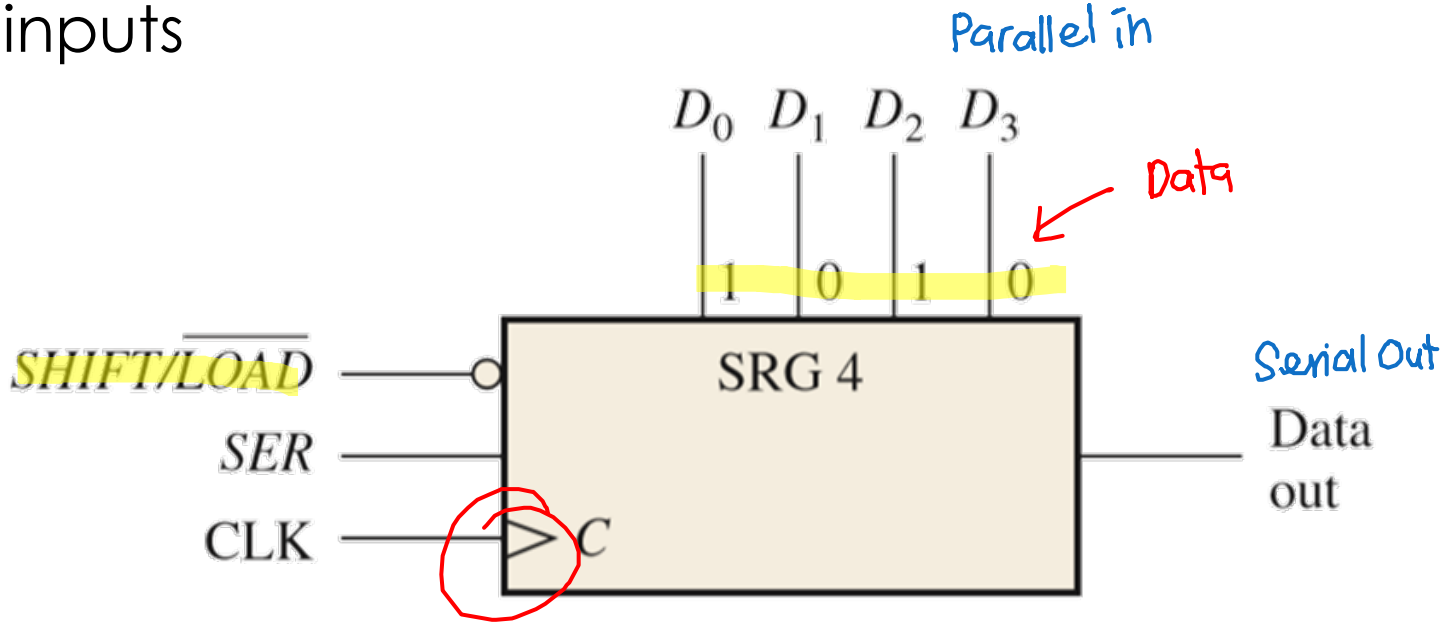


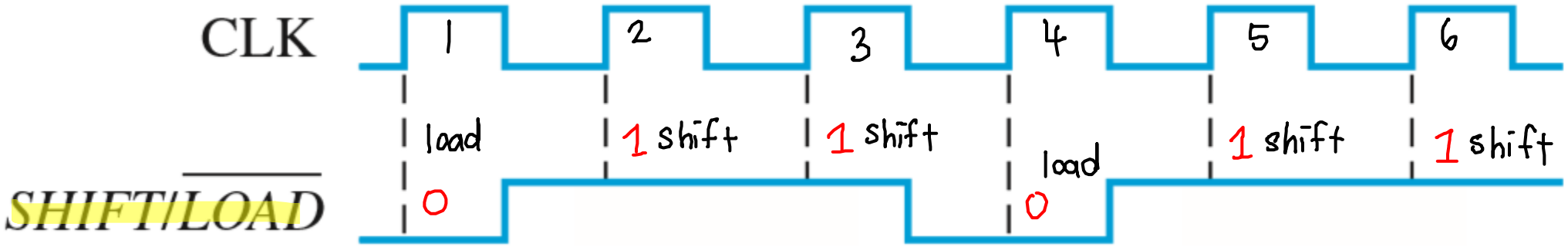



Q0 follow D
CLK
Serial data in
Q0
Q1
Q2
Q3

QUESTIONS 8

The parallel in/serial out register below has the **SHIFT/LOAD** and CLK inputs as shown in the timing diagram below. The parallel data inputs are constant at D0 = 1, D1 = 0, D2 = 1 and D3 = 0. Draw the data-output waveform of the register in relation to the inputs

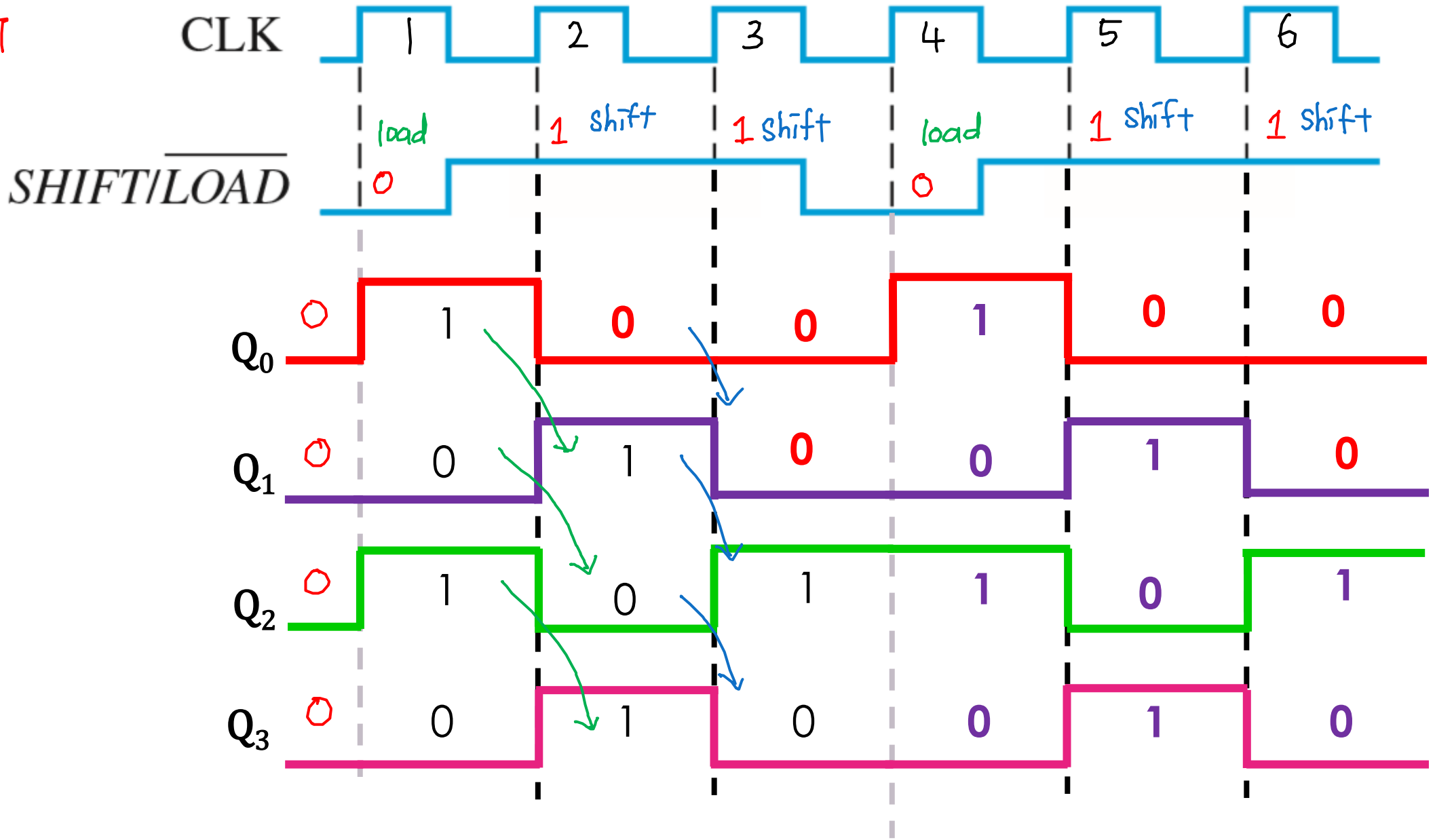




D0 = 1, D1 = 0, D2 = 1 and D3 = 0.

Q start Low/clear

4bit Parallel in Serial out Shift Register



QUESTIONS 9

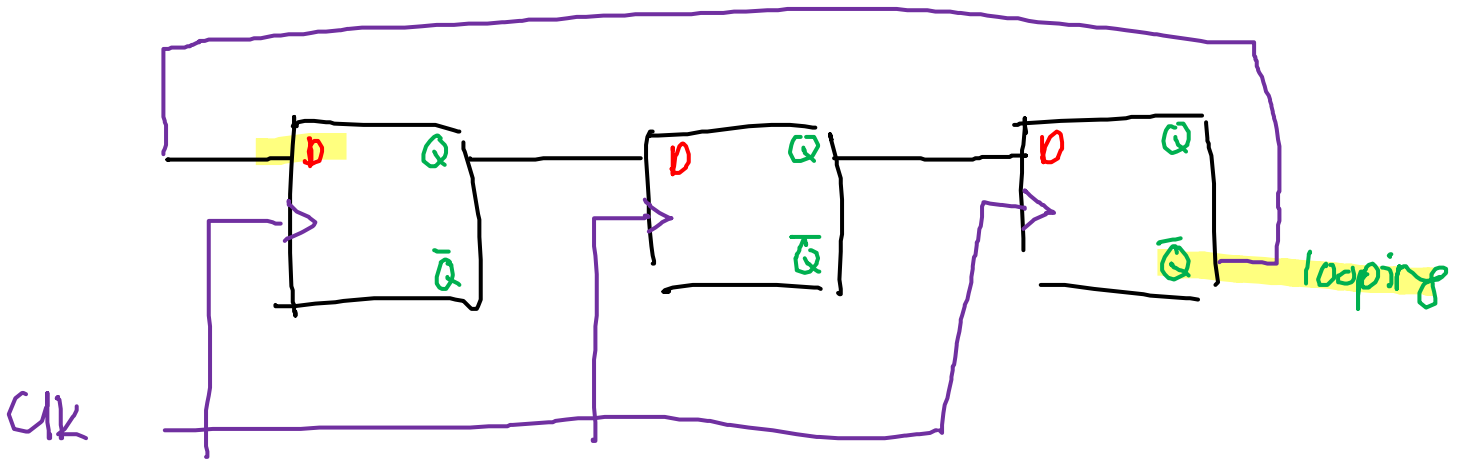
Determine the number of flip-flops required to implement each of the following in a **Johnson counter** configuration 2n

a. modulus-6 **2n=6 therefore number of FF, n=3**
b. modulus-10 **2n=10, n=5**
c. modulus-14 **2n=14, n=7**
d. modulus-16 **2n=16, n=8**

DO NOT MIX THIS UP WITH THE MODULUS IN EARLIER COUNTERS!!

mod 6 JC counter

(Shift Register) → Sync



QUESTIONS 10

18 state

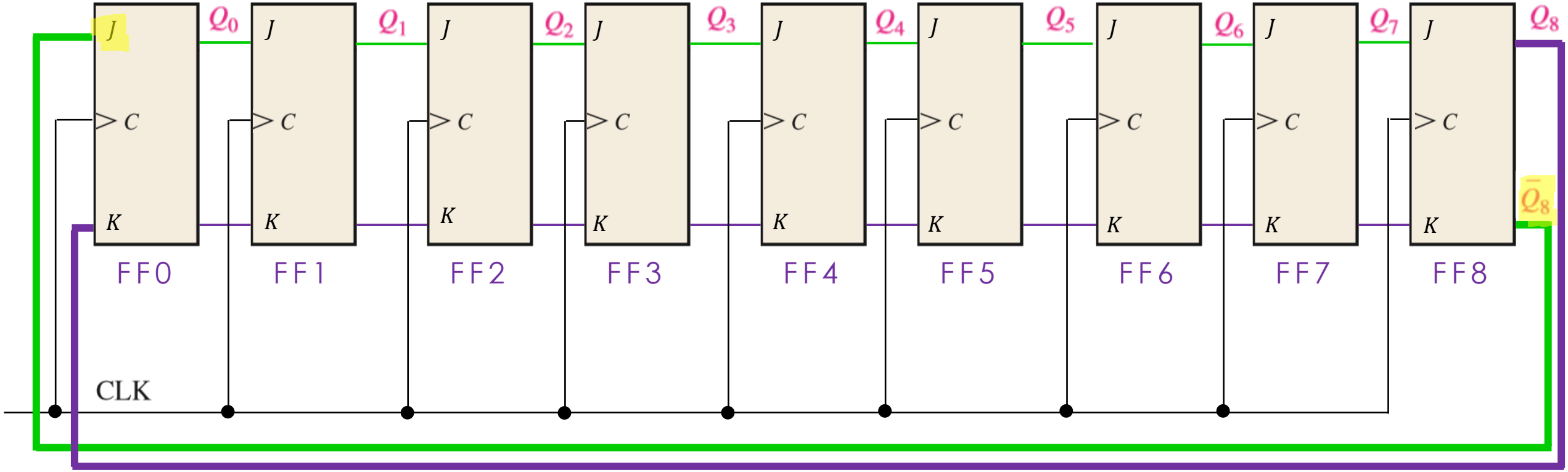
$2n = 18;\ n = 9$

Draw the logic diagram for a modulus-18 Johnson counter using J-K flip-flops and show the timing sequence of its flip-flops in tabular form. How would the sequence change if it were a ring counter instead?

$2n = 18, n=9$ The counter requires 9 FFs. In Johnson, the complement is feedback to the initial FF

JOHNSON COUNTER

(using JK FF)

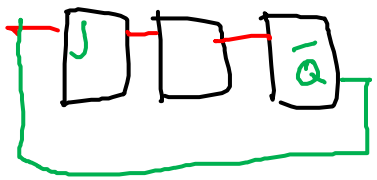


JOHNSON COUNTER

CLK	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0	0
4	1	1	1	1	0	0	0	0	0
5	1	1	1	1	1	0	0	0	0
6	1	1	1	1	1	1	0	0	0
7	1	1	1	1	1	1	1	0	0
8	1	1	1	1	1	1	1	1	0
9	1	1	1	1	1	1	1	1	1
10	0	1	1	1	1	1	1	1	1

Q_8 $\bar{Q}_8$
= 0 = 1

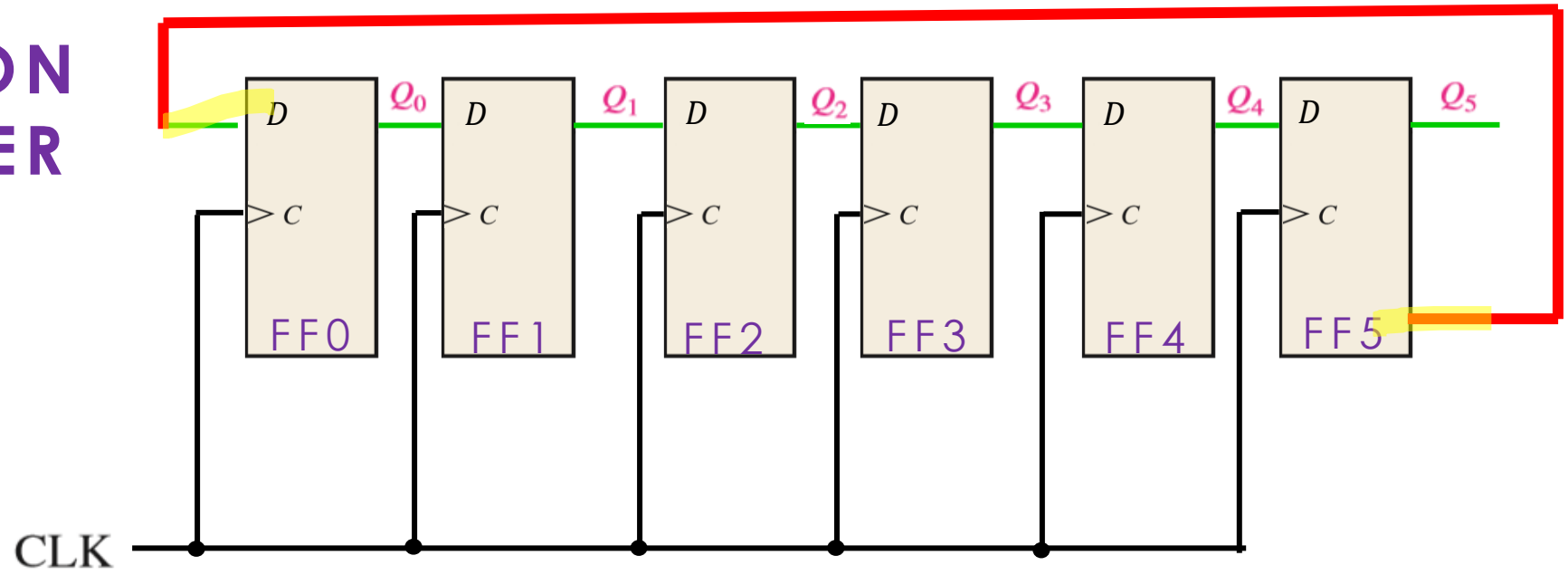
Q_8 $\bar{Q}_8 = 0$
= 1



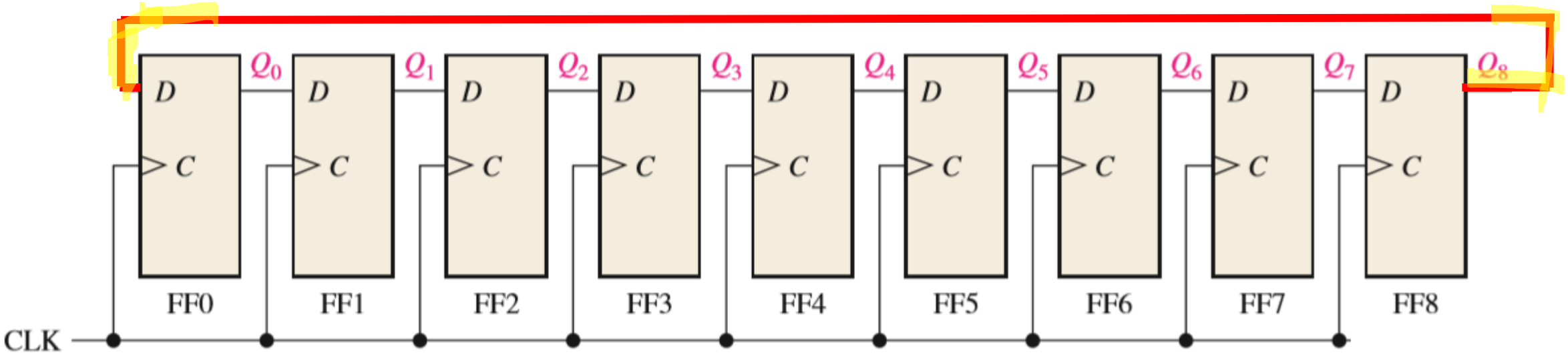
JOHNSON COUNTER

CLK	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
11	0	0	1	1	1	1	1	1	1
12	0	0	0	1	1	1	1	1	1
13	0	0	0	0	1	1	1	1	1
14	0	0	0	0	0	1	1	1	1
15	0	0	0	0	0	0	1	1	1
16	0	0	0	0	0	0	0	1	1
17	0	0	0	0	0	0	0	0	1
18	0	0	0	0	0	0	0	0	0

JOHNSON COUNTER



RING COUNTER



JOHNSON COUNTER

Initial state : 10010

mod-10

Clk/Q	Q_0	Q_1	Q_2	Q_3	Q_4
0	1	0	0	1	0
1	1	1	0	0	1
2	0	1	1	0	0
3	1	0	1	1	0
4	1	1	0	1	1
5	0	1	1	0	1
6	0	0	1	1	0
7	1	0	0	1	1
8	0	1	0	0	1
9	0	0	1	0	0
10	1	0	0	1	0

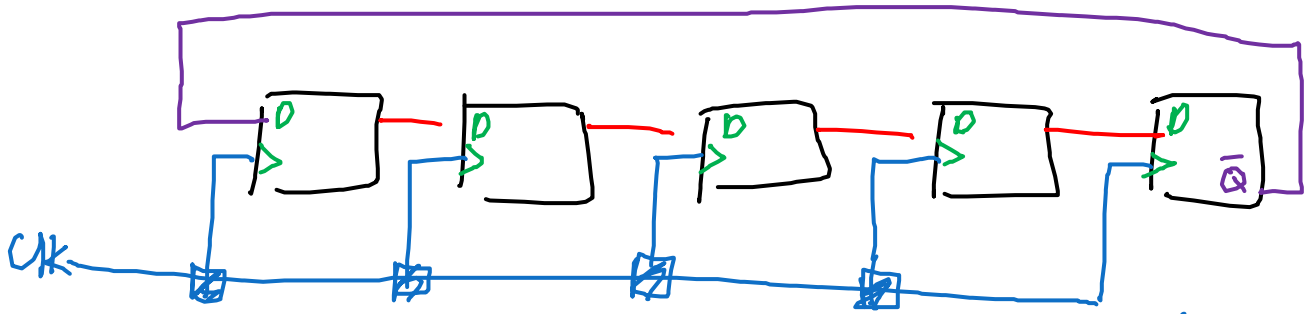
Modulus 10 JC Counter

RING COUNTER

Initial state : 10010

Clk/Q	Q_0	Q_1	Q_2	Q_3	Q_4
0	1	0	0	1	0
1	0	1	0	0	1
2	1	0	1	0	0
3	0	1	0	1	0
4	0	0	1	0	1
5	1	0	0	1	0

JC



RC