MULTIMEDIA UNIVERSITY

PDS0101 Introduction to Digital Systems

Tutorial 6

Tutorial outcomes

By the end of today's tutorial, you should be able to

- describe and design a full and half-adder circuit using truth tables and boolean algebra
- use full-adders to implement multibit parallel binary adders
- implement basic decoders

Theory based questions

1. Perform the following to construct a half-adder logic circuit
   a) Complete the truth table for 1-bit binary addition
   b) Derive the boolean expressions (SOP) for Sum and carry out
   c) Combine the sum and carry out expressions and draw the final logic circuit for a half-adder using only AND, OR and NOT gates
   d) Draw the block diagram for the half-adder

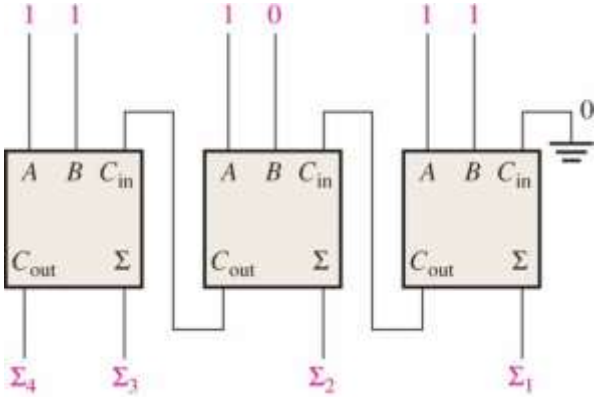
2. Repeat the process above to construct a full-adder logic circuit
   a) Complete the truth table for 1-bit binary addition
   b) Derive the boolean expressions (SOP) for Sum and carry out
   c) Simplify the expressions in (b) using boolean algebra
   d) Draw the block diagram for the full-adder from the simplified expressions in (c)

3. Determine the output value for C_{out} and $\sum$ (Sum) of a full adder, if the inputs are as shown below
   a) A=1, B=0, C_{in}=0
   b) A=0, B=0, C_{in}=1
   c) A=0, B=1, C_{in}=1
   d) A=1, B=1, C_{in}=1

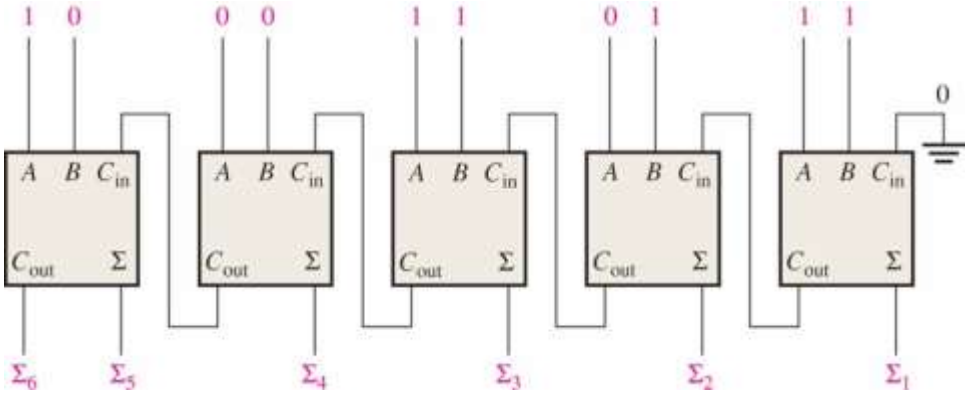
4. Determine the possible full-adder inputs that will produce the following outputs
   a) C_{out} = 0 $\sum$= 1
   b) C_{out} = 0 $\sum$= 0
   c) C_{out} = 1 $\sum$= 1
   d) C_{out} = 1 $\sum$= 0

5. For the parallel adders below, determine the complete sum by analysis of the logical operation of the circuit

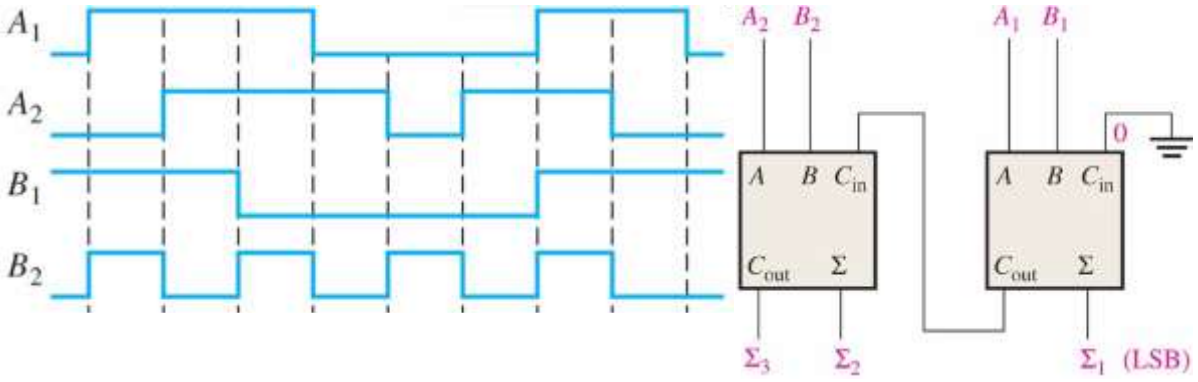
a)



b)

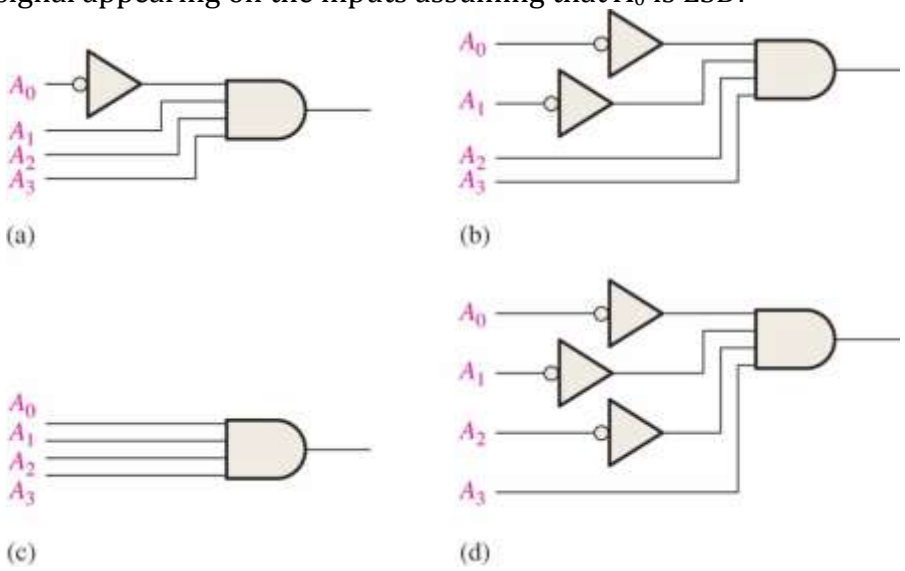


6. The input waveforms in the figure below are applied to the logic circuit shown. Determine the output waveforms in relation to the inputs by completing the timing diagram



7. Design a 3-bit parallel adder by using full adders only

8. When a HIGH output is detected on the output of the following decoder circuits, what is the binary code signal appearing on the inputs assuming that A_0 is LSB?



9. Show the decoding logic for the following codes if an active-HIGH output is required
   a) 1101
   b) 101010
   c) 11011
   d) 1110110

10. Show the decoding logic for the following codes if an active-LOW output is required
    a) 1000
    b) 11100
    c) 111110
    d) 000101

11. Design a decoder that detects the presence of the input binary codes of 1010, 1100, 0001 and 1011. The active-HIGH output is required when the correct input is detected.

12. Design a 2-to-4-Line Decoder (with Enable input) and Active LOW output. Provide the circuit and truth table.

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