MMU
MULTIMEDIA UNIVERSITY

TUTORIAL 6
FUNCTIONS OF COMBINATIONAL LOGIC

PDS0101: INTRODUCTION TO DIGITAL SYSTEMS
TRI 2, 2022-2023

QUESTION 1 : Perform the following to construct a HALF-ADDER logic circuit

a) Complete the **TRUTH TABLE** for **1-bit BINARY ADDITION**

$2^2 = 4$ possible input combination

← input → ← output →

Augend(A)	Addend(B)	Carry Out	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$\begin{array}{r} 0 \\ +\ 0 \\ \hline 0 \end{array} \qquad \begin{array}{r} 0 \\ +\ 1 \\ \hline 1 \end{array}$$

$$\begin{array}{r} 1 \\ +\ 0 \\ \hline 1 \end{array} \qquad \begin{array}{r} 1 \\ +\ 1 \\ \hline 10 \end{array} \rightarrow \text{decimal } 2$$

C_{out} $\quad$ sum

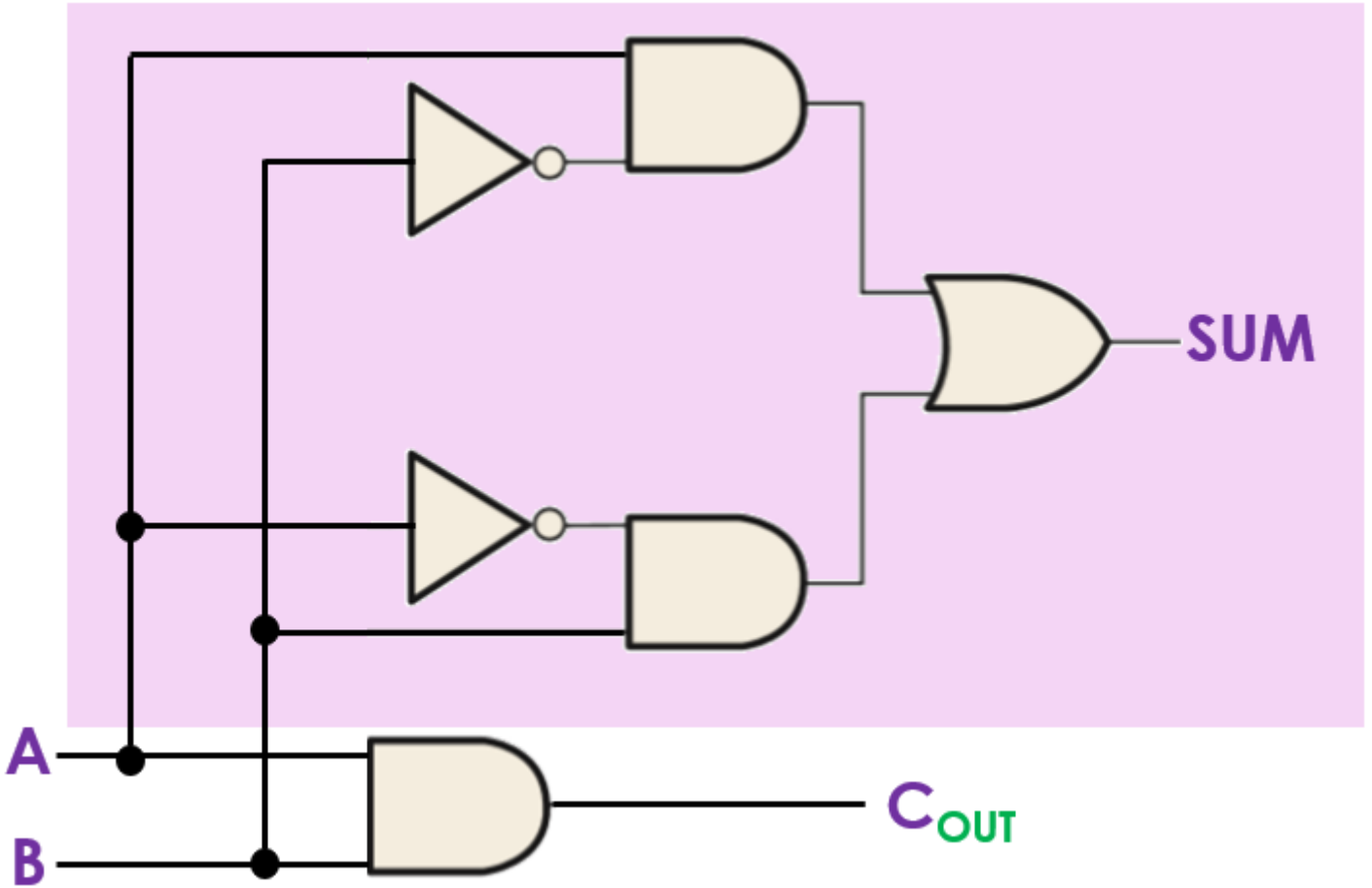
b) Derive the Boolean expressions (SOP) for **SUM** and **CARRY OUT**

$C_{out} = AB$ $\qquad$ $Sum = A \oplus B \;/\; A\bar{B} + \bar{A}B$

QUESTION 1 : Perform the following to construct a HALF-ADDER logic circuit

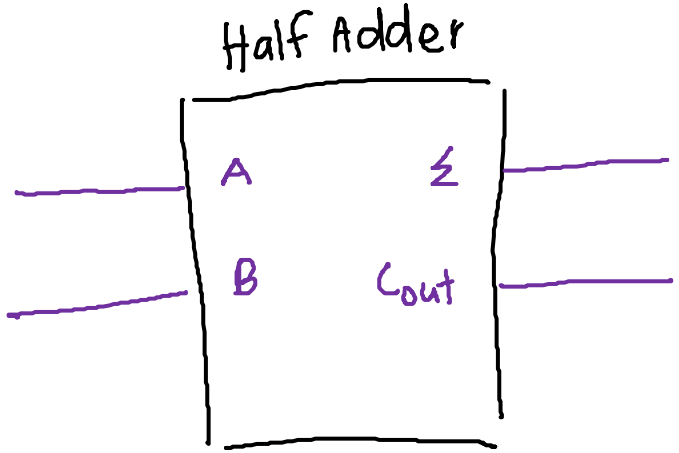
c) Combine the sum and carry out expressions and **draw** the final **logic circuit** for a **half-adder** using only **AND**, **OR** and **NOT** gates

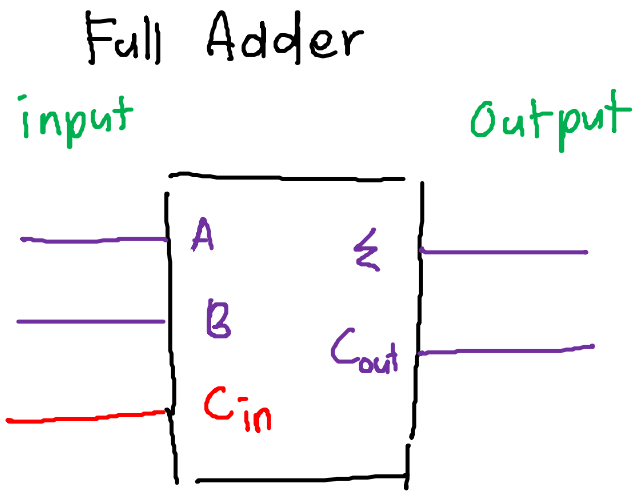
~~A ⊕ B~~ $A\bar{B} + \bar{A}B = Sum$



QUESTION 1 : Perform the following to construct a HALF-ADDER logic circuit

d) Draw the **block diagram** for the **half-adder**





Draw parallel adder for 10011 + 11011 using full adder

(block diagram/logic diagram)

→ 5 bit

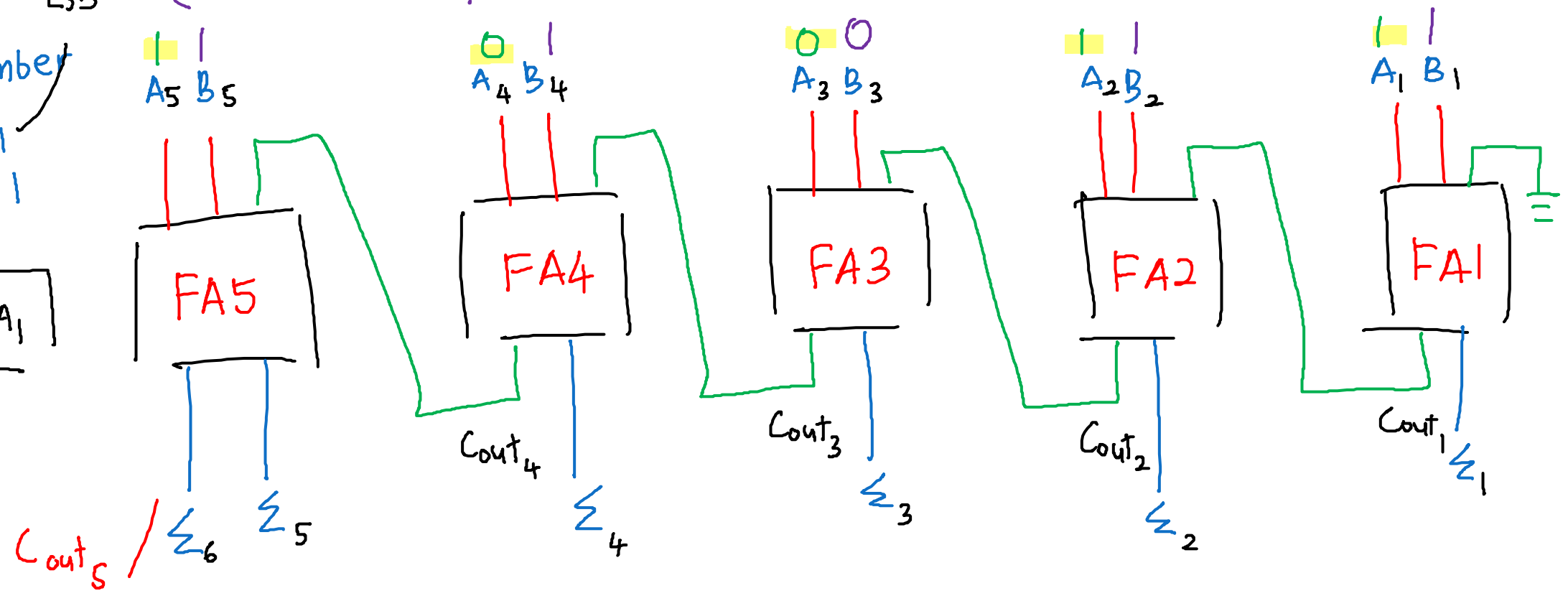
MSB LSB

Binary number

A : 10011

B : 11011

$A_5 A_4 A_3 A_2 A_1$



Draw parallel adder for 10011 + 11011 using full adder

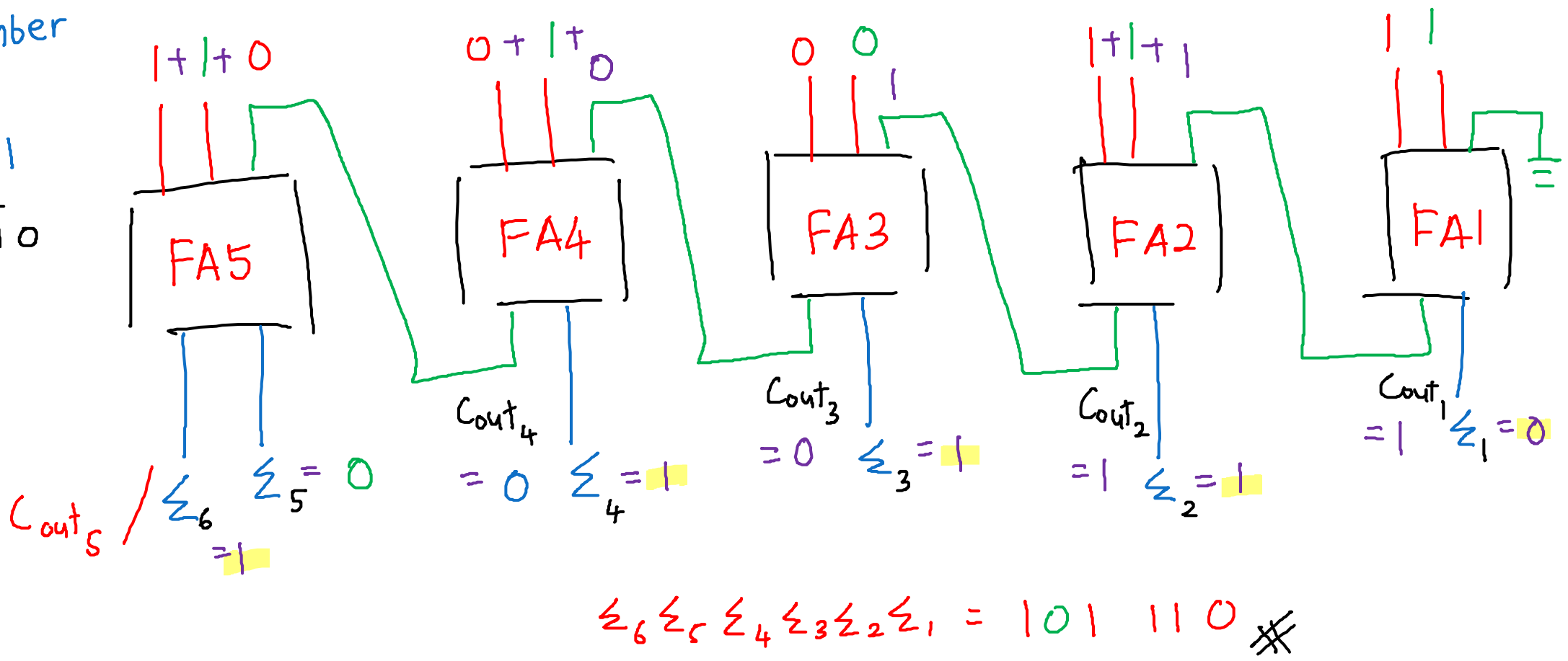
(block diagram/logic diagram)

↳ 5 bit

1 + 1 = 10

Binary number

```
  11
A : 10011
B : 11011
-------
101110
```



$\Sigma_6 \Sigma_5 \Sigma_4 \Sigma_3 \Sigma_2 \Sigma_1 = 101\ 110$ #

Draw parallel adder for 10011 + 11011 using full adder and half adder

(block diagram/logic diagram)

11011 → 5 bit

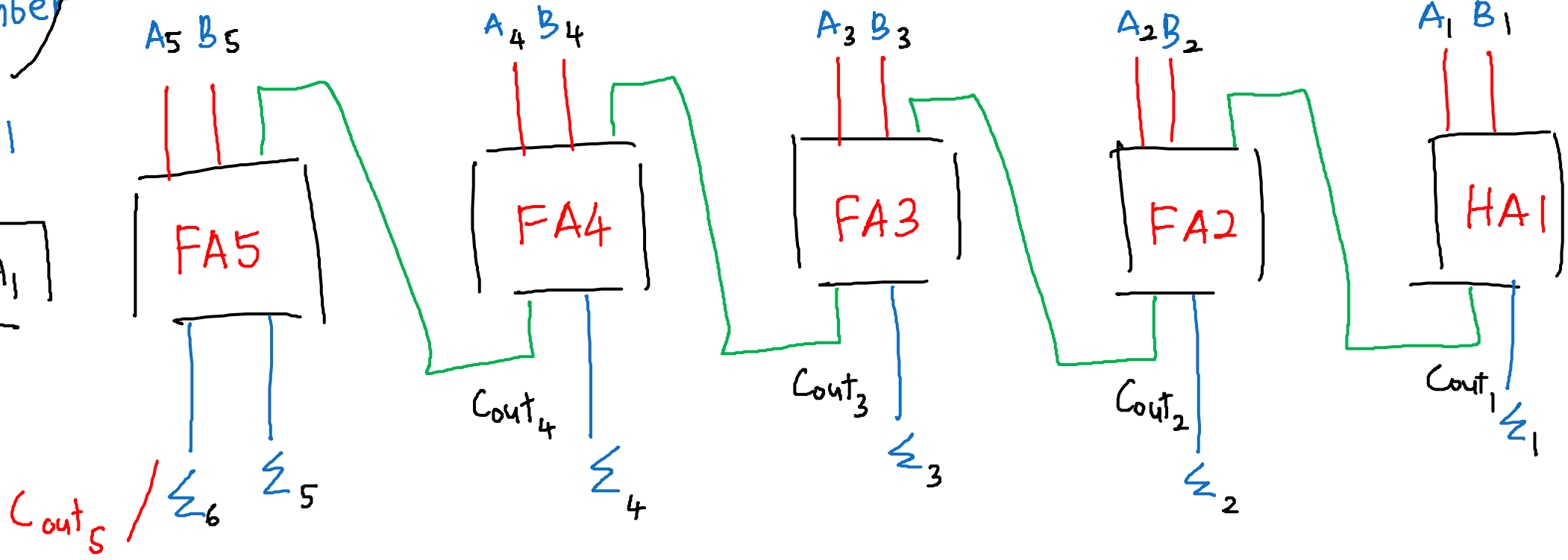
MSB LSB

Binary number

A : 10011

B : 11011

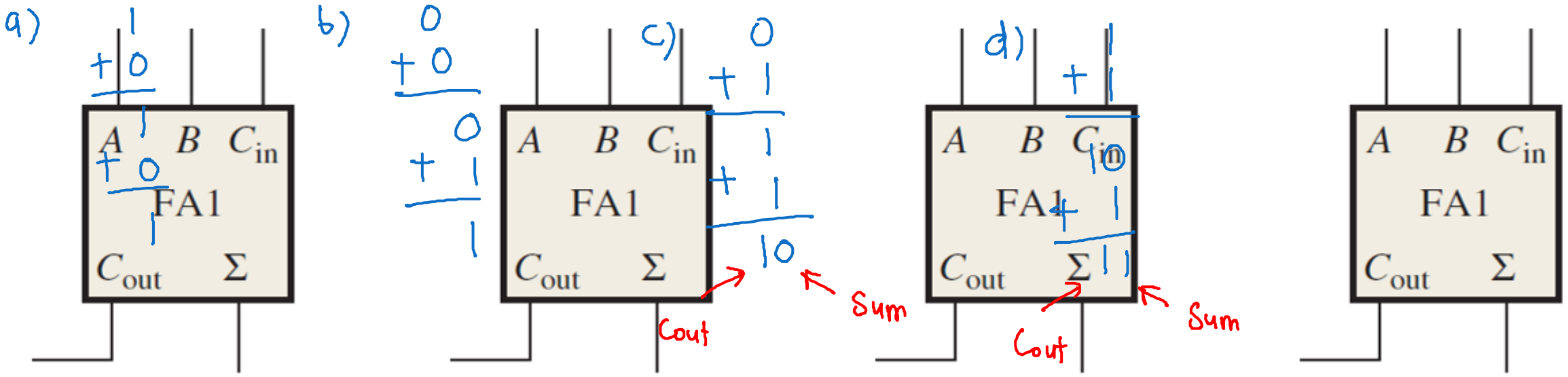
$A_5 A_4 A_3 A_2 A_1$



QUESTION 3

Determine the output value for C_{out} and **Σ (sum)** of a **FULL ADDER**, if the inputs are as shown below

	A	B	C_{in}	C_{out}	Σ (sum)
(a)	1	0	0	0	1
(b)	0	0	1	0	1
(c)	0	1	1	1	0
(d)	1	1	1	1	1



QUESTION 4

Determine the possible **FULL ADDER INPUTS** that will produce the following outputs

← output →

	C_{out}	Σ (sum)	A	B	C_{in}
(a)	0	1	0	1	0
			0	0	1
			1	0	0
(b)	0	0	0	0	0
(c)	1	1	1	1	1
(d)	1	0	1	1	0
			0	1	1
			1	0	1

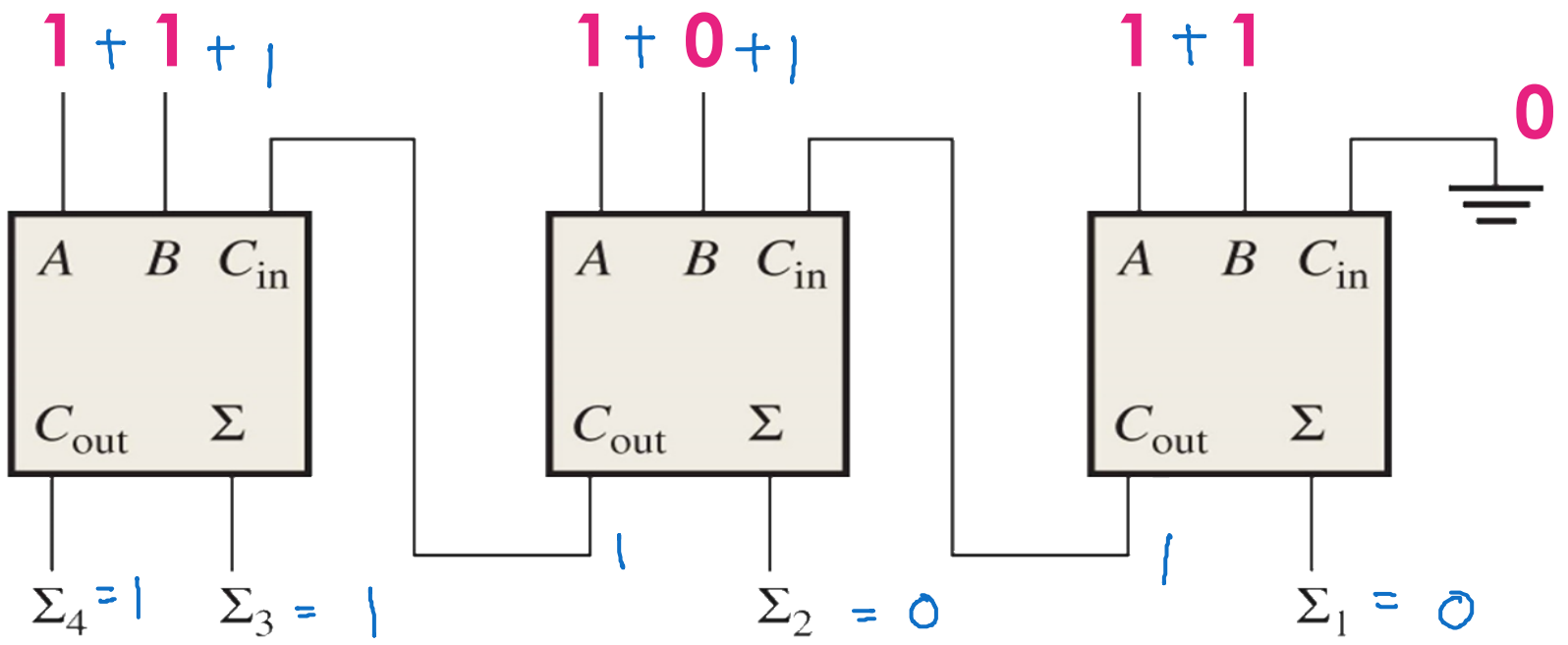
QUESTION 5 (a)

For the **PARALLEL ADDERS** below, determine the complete **SUM BY ANALYSIS** of the logical operation of the circuit

A : 1 1 1 1

B : 1 0 1

1 1 0 0 *



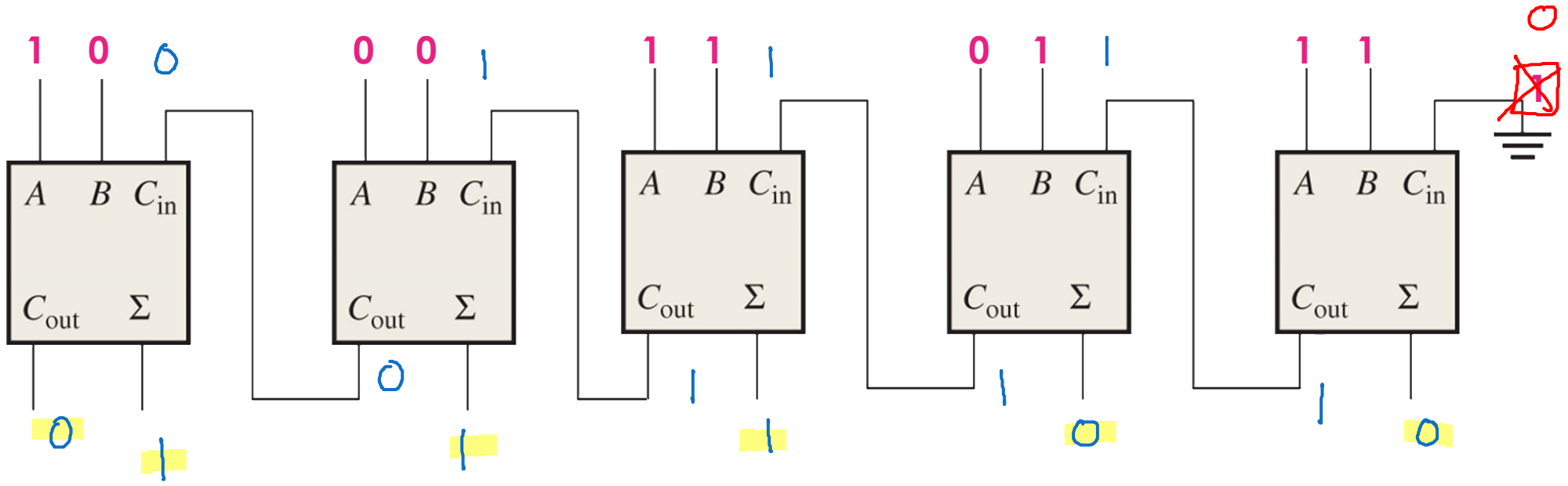
$\Sigma_4\Sigma_3\Sigma_2\Sigma_1 = 1100$ *

QUESTION 5 (b)

For the **PARALLEL ADDERS** below, determine the complete **SUM BY ANALYSIS** of the logical operation of the circuit

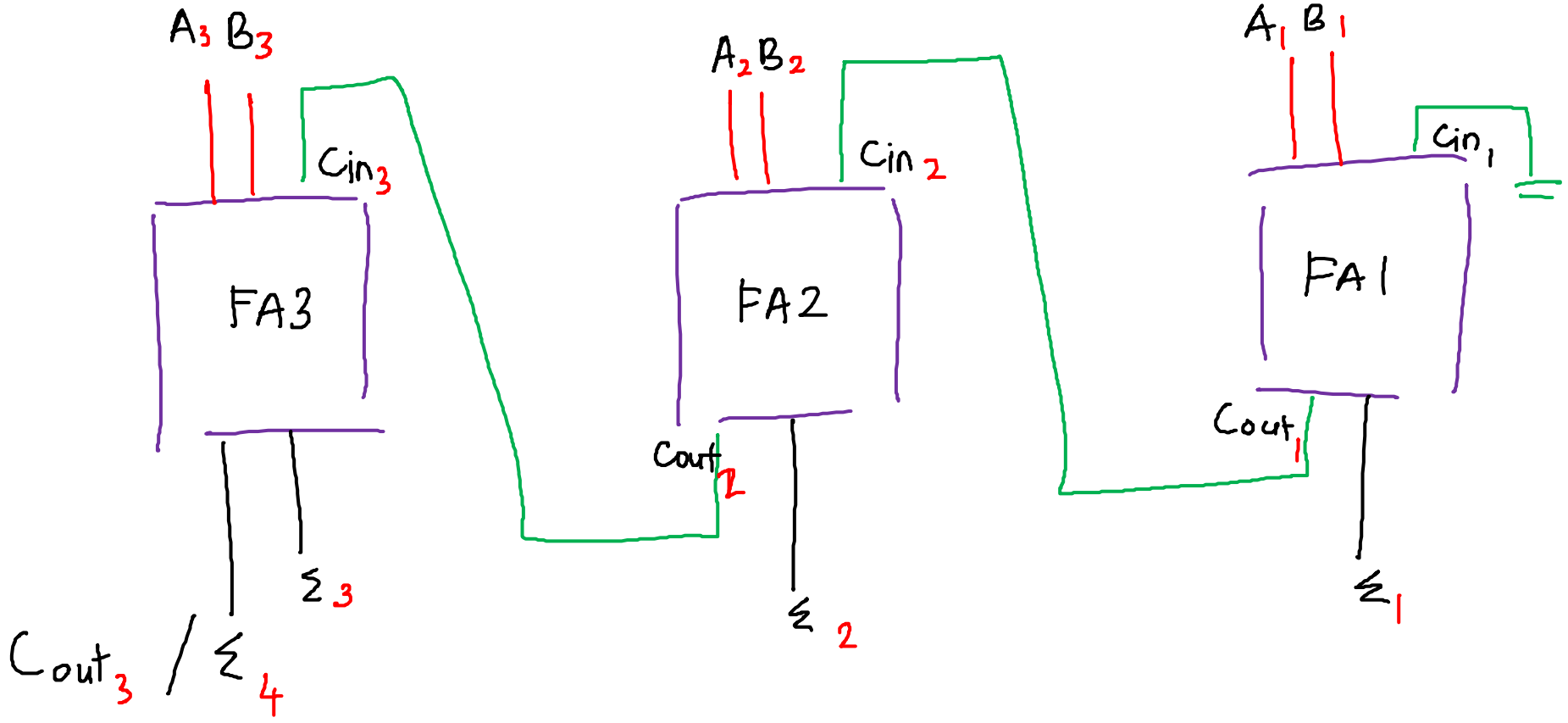
A : 10101

B : 00111



QUESTION 7

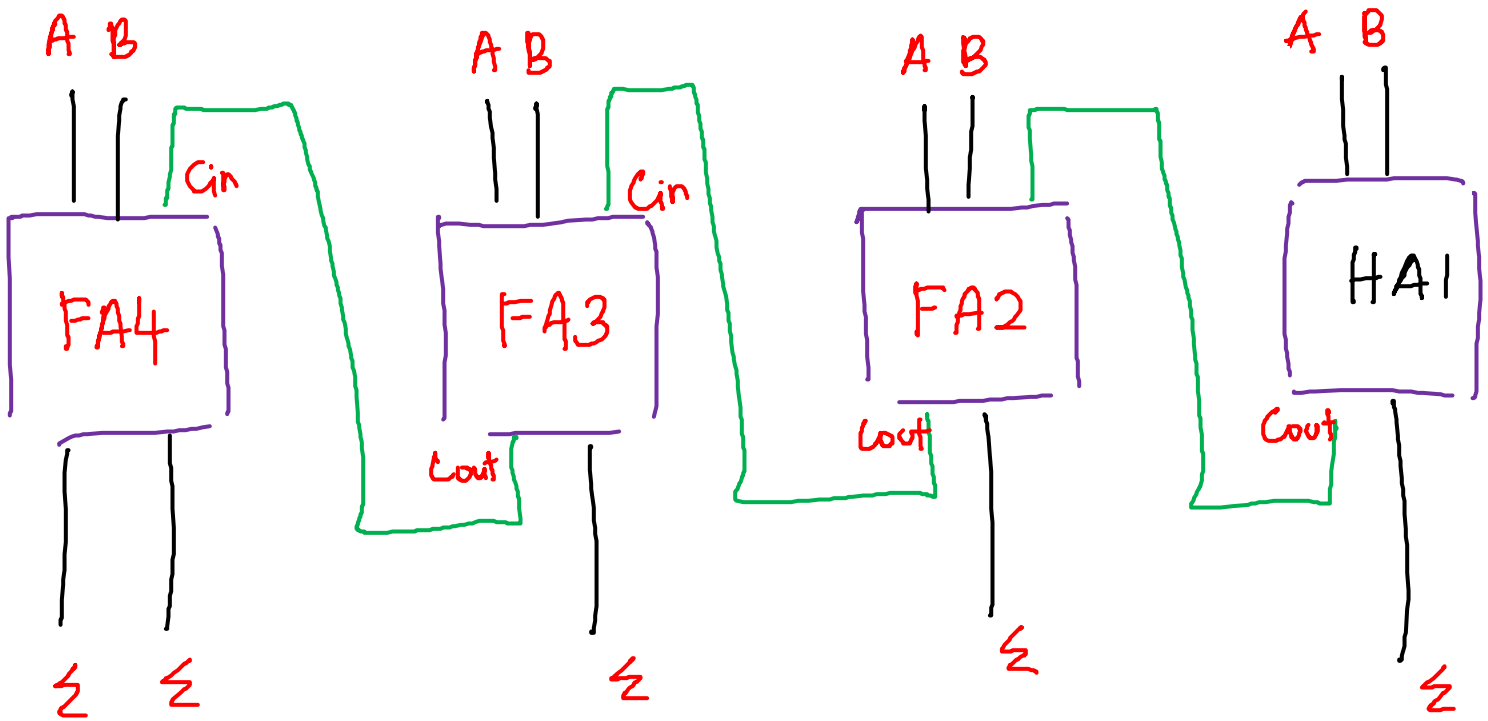
Design a **3-bit** **parallel adder** by using **full adders**



Draw parallel adder for $A_{16} + 14_8$ using full adder and halfadder (LSB)

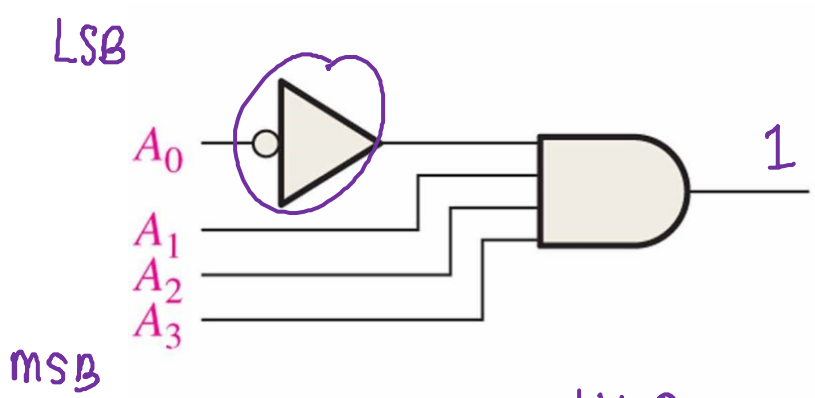
$A_{16} = 1010$

$14_8 = 1100$

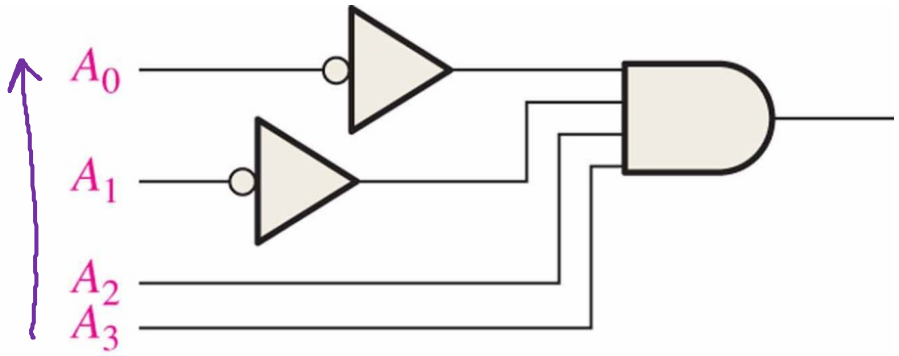


QUESTION 8

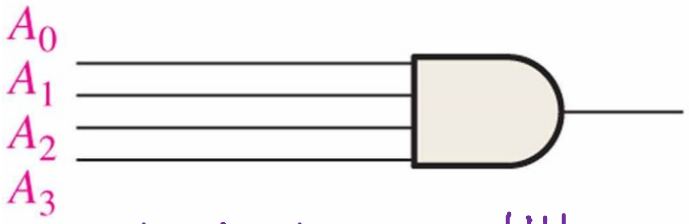
When a **HIGH output** is detected on the output of the following **decoder circuits**, what is the **binary code signal** appearing on the **INPUTS** assuming that A_0 is LSB?



(a) $A_3A_2A_1A_0 = 1110$

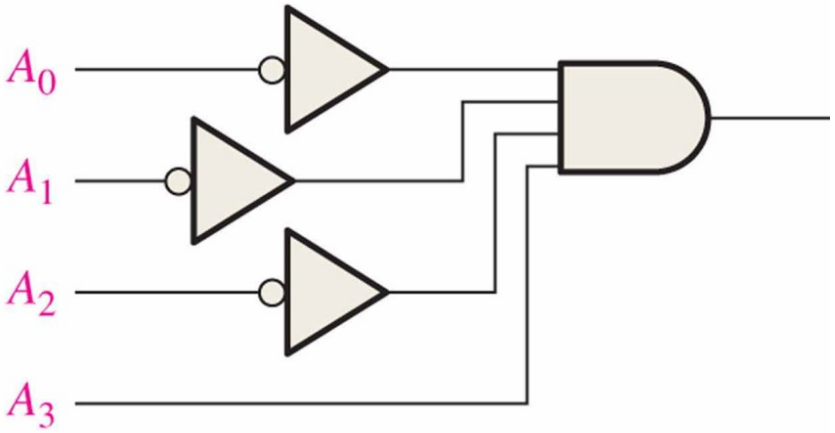


(b) $A_3A_2A_1A_0 = 1100$



$A_3\ A_2\ A_1\ A_0 = 1111$

(c)



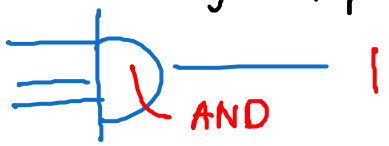
$A_3A_2A_1A_0 = 1000$

(d)

Decoder

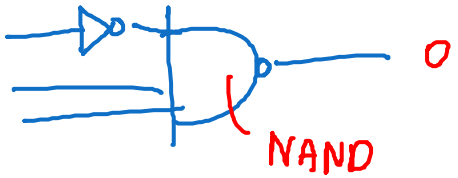
- simple decoder / basic decoder
- decoder that accept multiple combo (SOP)
- line decoder
  - n-to-x
  - 2-to-4 line decoder
  - 3-to-8 line decoder
  - 4 to 16 line decoder

a) Active high output

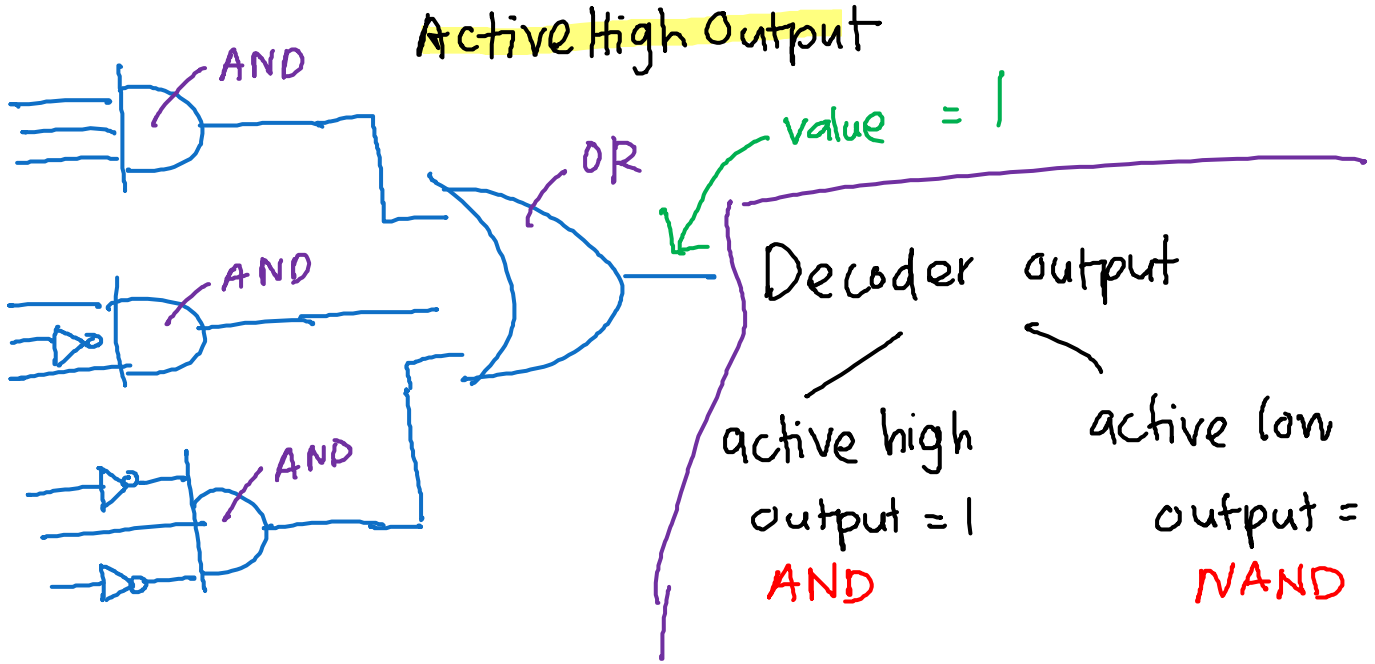


Input = 111

b) Active Low output



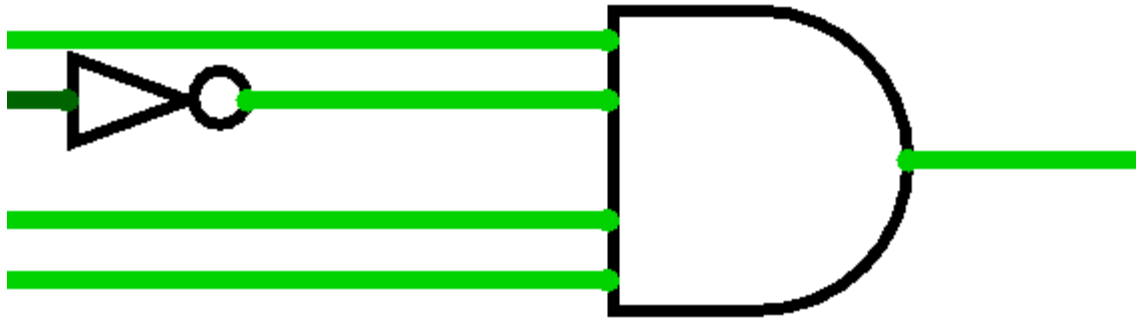
Input = 110



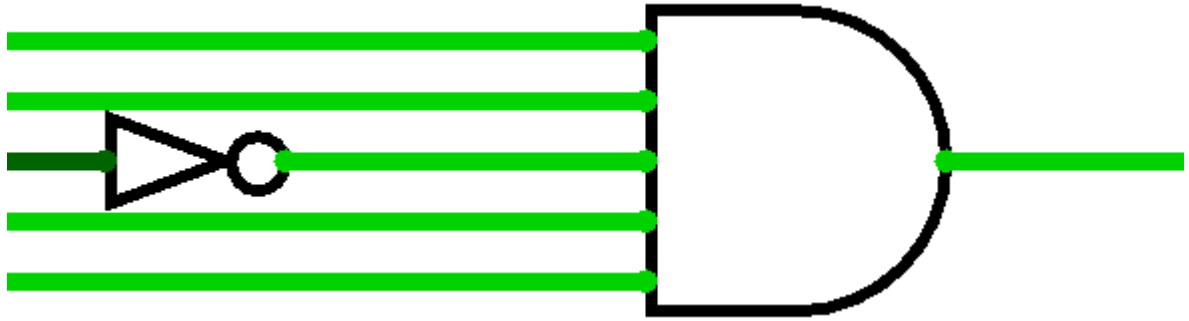
QUESTION 9

Show the **decoding logic** for the following **codes** if an **active-HIGH** output is required

a) 1101



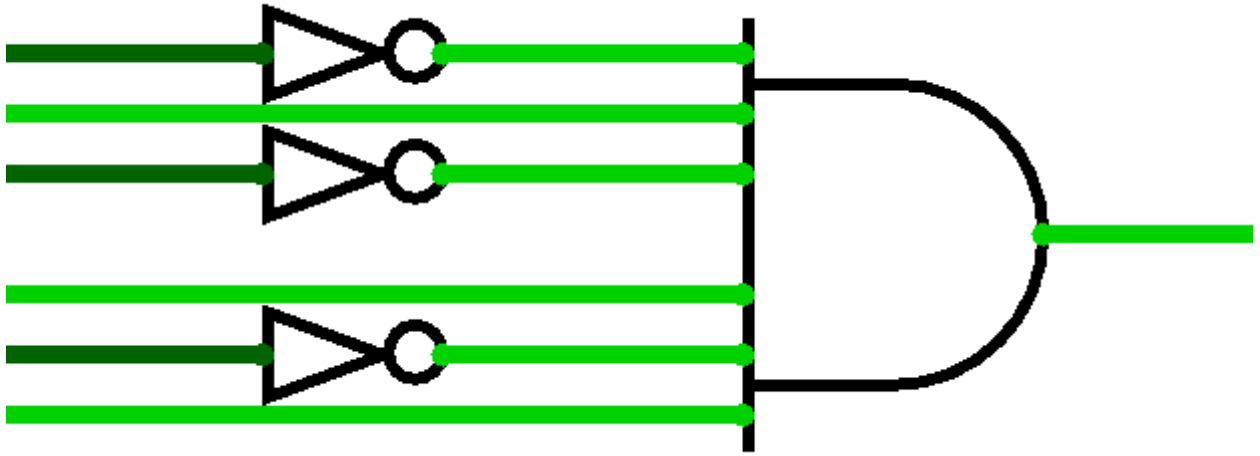
b) 11011



QUESTION 9

Show the **decoding logic** for the following **codes** if an **active-HIGH** output is required

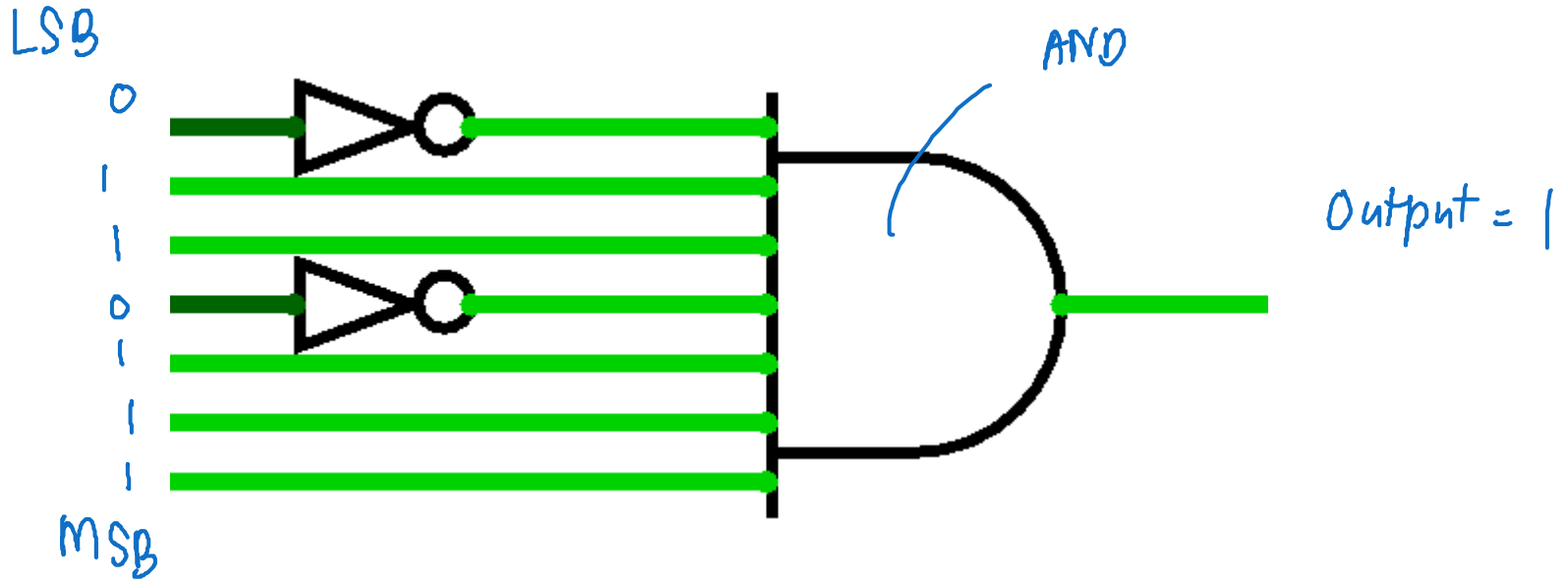
c) 101010



QUESTION 9

Show the **decoding logic** for the following **codes** if an **active-HIGH** output is required

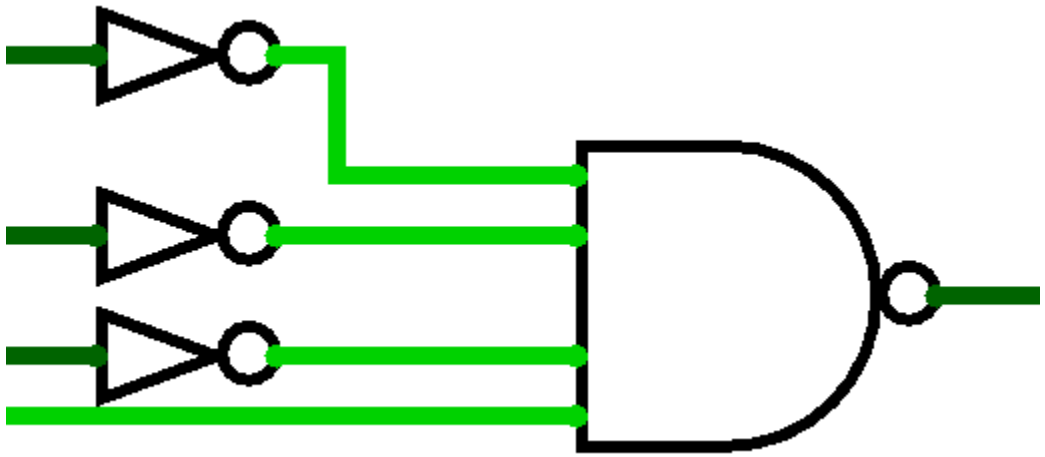
d) 1110110



QUESTION 10

Show the **decoding logic** for the following **codes** if an **active-LOW** output is required

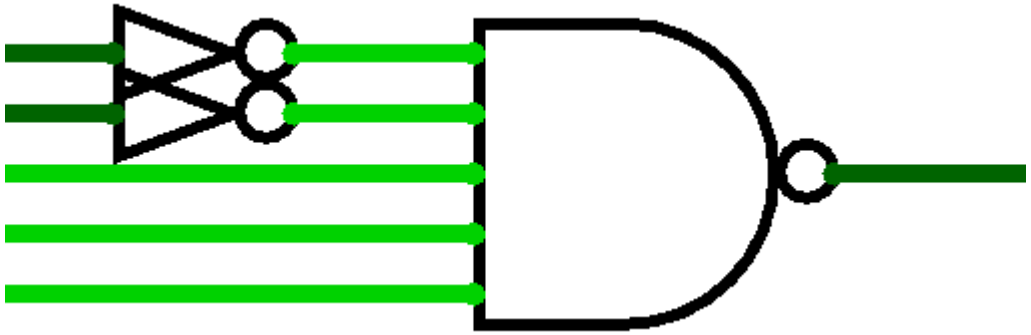
a) 1000



QUESTION 10

Show the **decoding logic** for the following **codes** if an **active-LOW** output is required

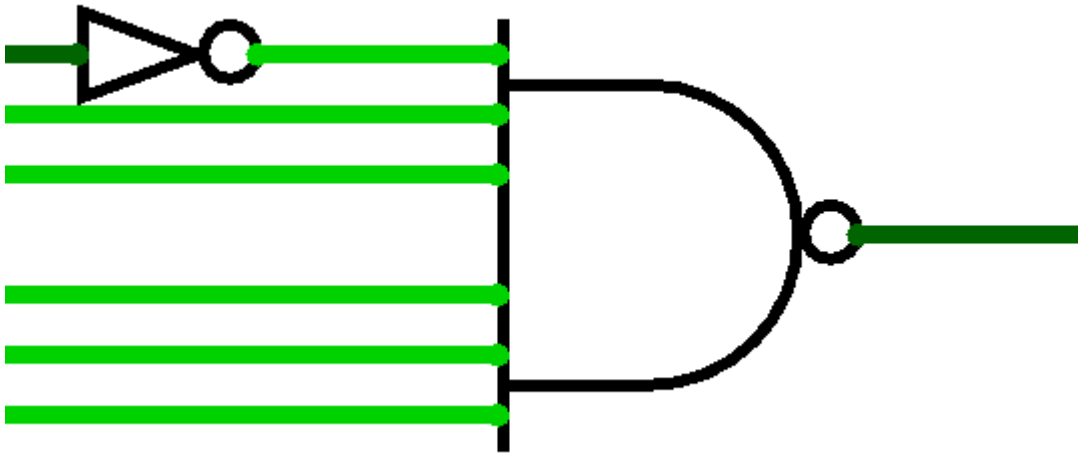
b) 11100



QUESTION 10

Show the **decoding logic** for the following **codes** if an **active-LOW** output is required

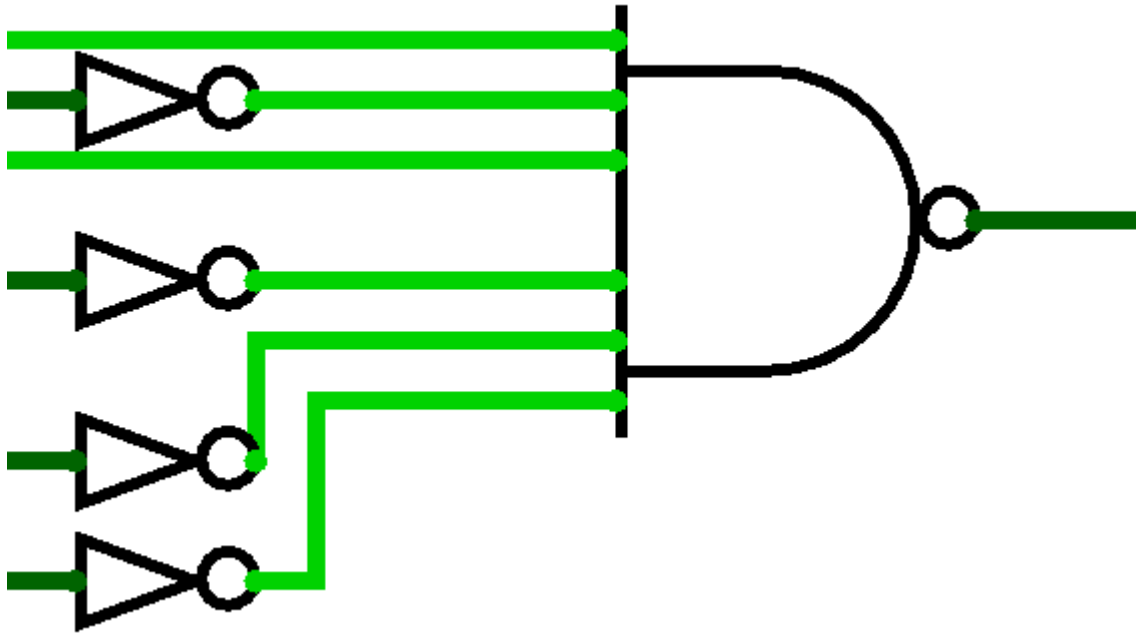
c) 111110



QUESTION 10

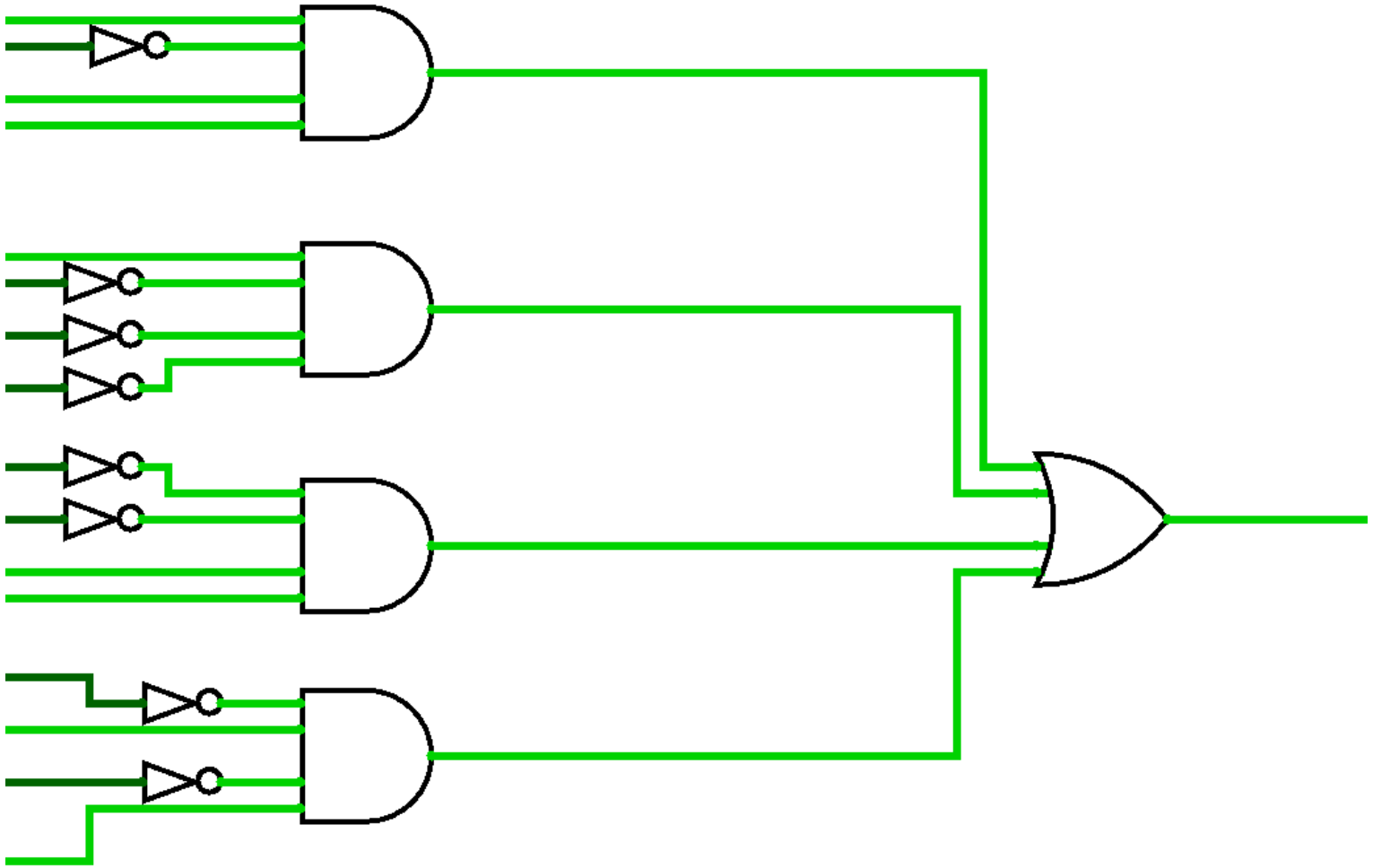
Show the **decoding logic** for the following **codes** if an **active-LOW** output is required

d) 000101



QUESTION 11

Design a decoder that detects the presence of the input binary codes of 1010, 1100, 0001and 1011. The active-HIGH output is required when the correct input is detected.



QUESTION 12

Design a **2-to-4-Line Decoder** (with **Enable input**) and **Active LOW** output.
Provide the circuit and truth table.

input

Combination

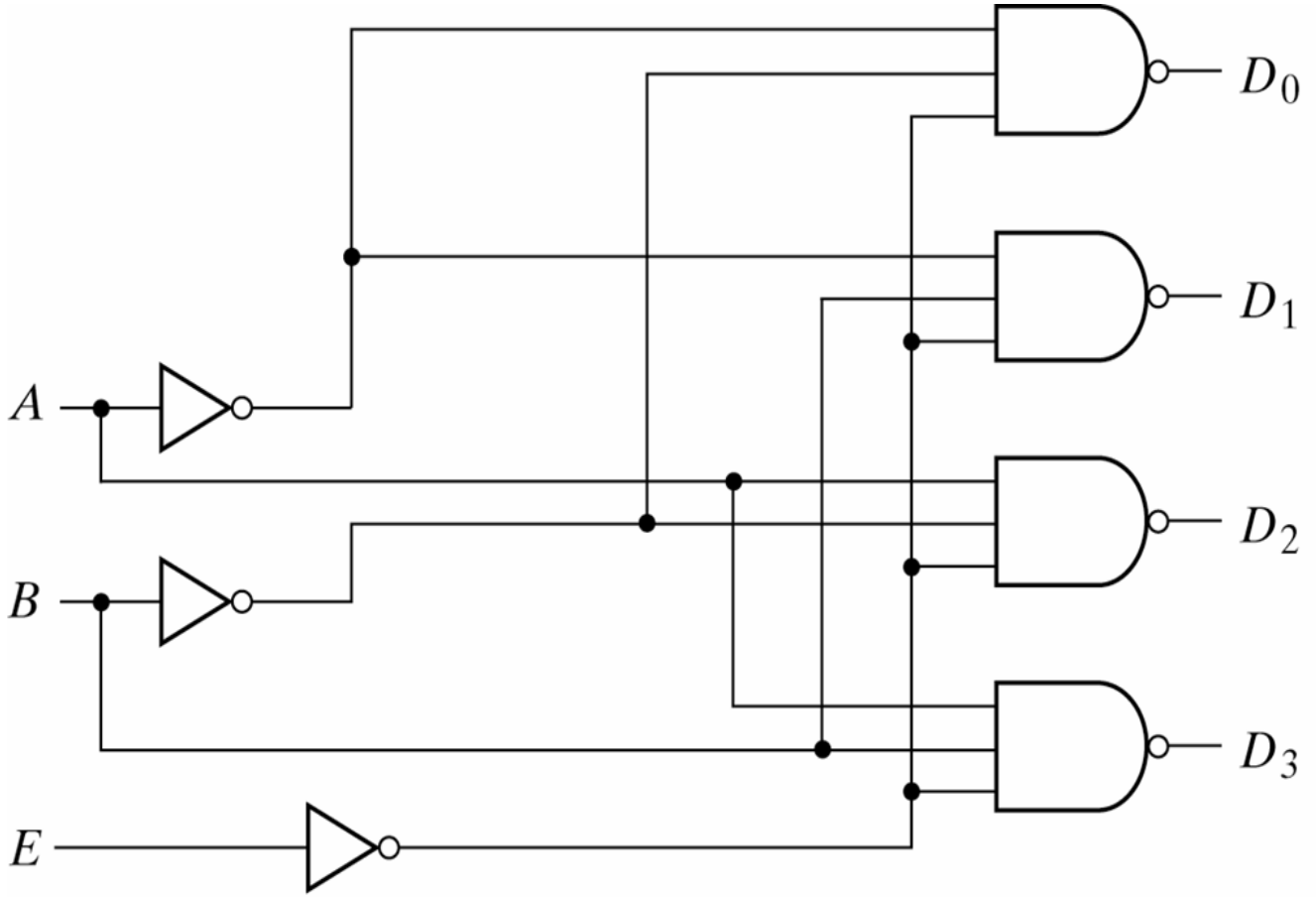
EN = 0 ; active

Output = 0

EN	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

QUESTION 12

Design a **2-to-4-Line Decoder** (with **Enable input**) and **Active LOW** output.
Provide the circuit and truth table.



QUESTION 12

Design a **3-to-8-Line Decoder** (with **Enable input**) and **Active HIGH** output. Provide the circuit and truth table.

EN = 1

Output = 1

EN	A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

END DISCUSSIONS
ANY QUESTIONS ??