TSN1101 Computer Architecture and Organization (Digital Logic Design Lab (A))

LAB A-02 (Week 2) Basic Logic Gates-Verification of Truth Tables

Objectives

- To get familiarity with the operation of the basic logic gates and verify the truth tables experimentally.

Tasks

Questions to be done in the lab and to be submitted in the report:

1. Perform the study of the truth table of the following logic gates and verify the truth table of the gates experimentally.

   2 input NAND gate

   2 input NOR gate

   3 input AND gate

   2 input XOR gate

(Note: For the inputs, 1 should be connected to +5V and 0 should be connected to ground. Outputs can be viewed using LEDs connected through resistors. If the LED is glowing, it will be considered as 1 and if it is not glowing, it will be considered as 0)

2. (i) Prove that NOR gate is equivalent to a negative AND gate by constructing a simple circuit using NOT and AND gates and verify the truth table experimentally.

(ii) Prove that NAND gate is equivalent to a negative OR gate by constructing a simple circuit using NOT and OR gates and verify the truth table experimentally.

Questions to be submitted in the report:

3. Perform NOR operation on decimal inputs 10, 13, and 7. Convert the decimal input to the 4 bits binary form before performing the operations. Draw the timing diagram for the output in relation to the three inputs of the above gates.

4. Perform NAND operation on decimal inputs 6, 9, and 11. Convert the decimal input to the 4 bits binary form before performing the operations. Draw the timing diagram for the output in relation to the three inputs of the above gates.

5. Based on the input and output sequences given below, identify the corresponding logic operation performed on the inputs. Draw the timing diagrams of the output in relation to the inputs.

a. Input sequence A: 1 0 0 1

Input sequence B: 1 1 0 1

Input sequence C: 0 1 1 1

Output sequence: 1 1 1 0

b. Input sequence A: 0 1 0 1

Input sequence B: 0 1 1 0

Output sequence: 0 0 1 1

Report Format :

For each question,

- Problem Statement
- Truth Table
- Construction Diagram (you may snapshot from CircuitVerse)
- Result

Circuit Construction:

- Submit the constructed circuit via CircuitVerse, and label it according to question. Be self-explanatory.

Assessment:

Total marks = 20/10=2%
Construction/Connections of the Circuit and Result during lab session= 4 (Q1) + (Q2) = 10 marks,
Report =5 Questions × 2 marks = 10 marks