MULTIMEDIA UNIVERSITY

PDS0101 Introduction to Digital Systems

Tutorial 3 SAMPLE SOLUTIONS

Tutorial outcomes

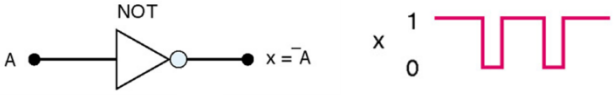
By the end of today's tutorial, you should be able to

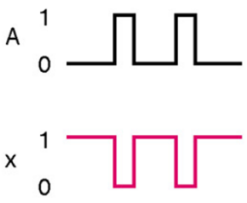
- describe the operations of basic logic gates – AND, OR, NOT, XOR, NAND
- recognize the different logic symbols of each gate
- construct timing diagrams for input and output signals for various logic gates

Theory based questions

Draw the logic symbol and construct the truth tables and timing diagrams for the following gates showing all possible input combinations

1. 1-input inverter

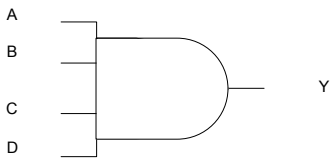


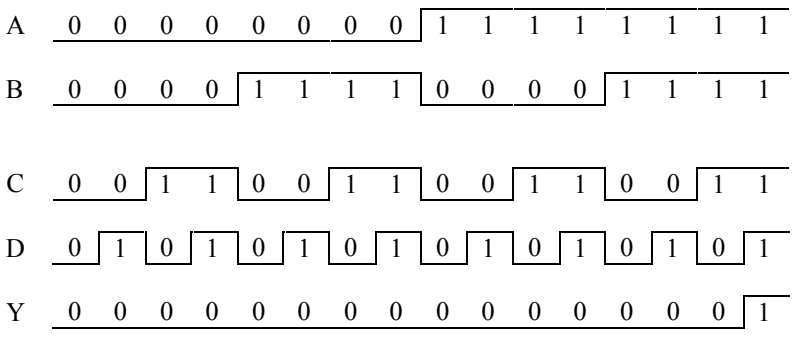


Input	Output	
A	A'	$\bar{A}$
0	1	
1	0	

2. 4-input (quad-input) AND gate

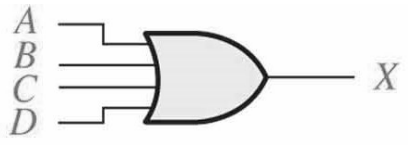
Input				Output
A	B	C	D	Y= ABCD
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

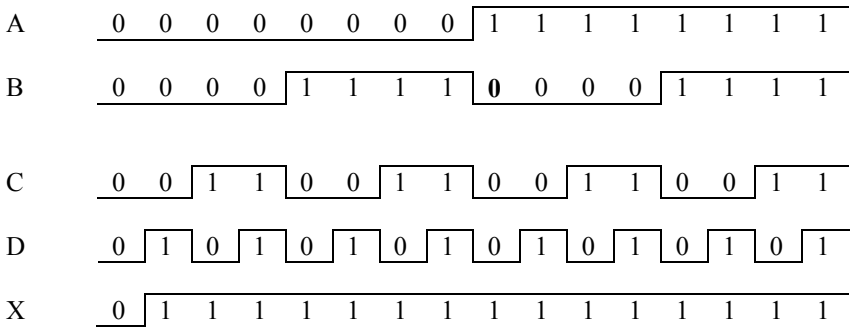




3. 4-input OR gate

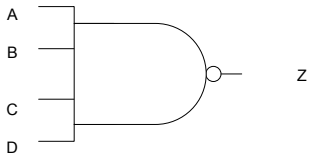
Input				Output
A	B	C	D	X= A+B+C+D
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

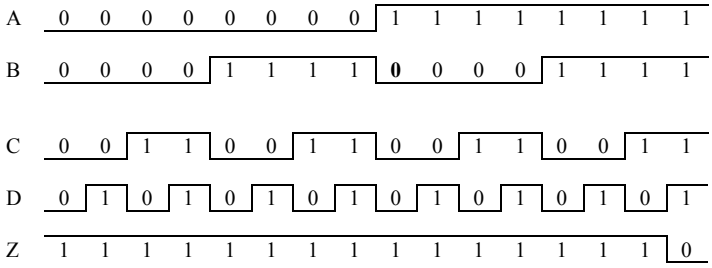




4. 4-input NAND gate

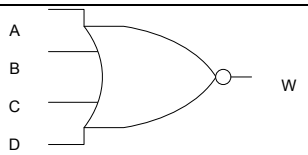
Input				Output
A	B	C	D	Z= (ABCD)' or Z = $\overline{ABCD}$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

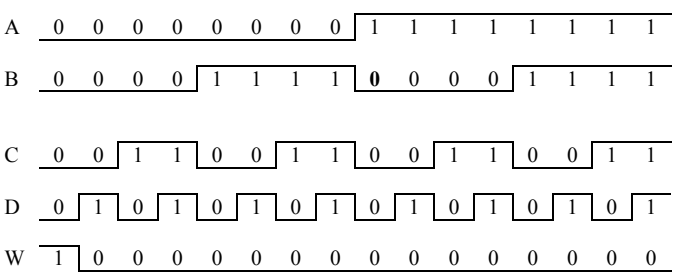




5. 4-input NOR gate

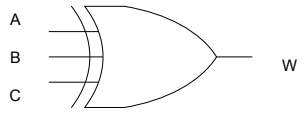
Input				Output	
A	B	C	D	X= A+B+C+D	W = $\overline{A+B+C+D}$ Or W = $\bar{X}$
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	0

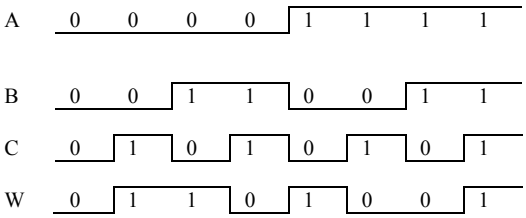




6. 3-input (tri-input) XOR gate

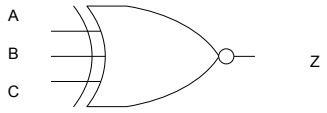
Input			Output
A	B	C	W= A⊕B ⊕C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

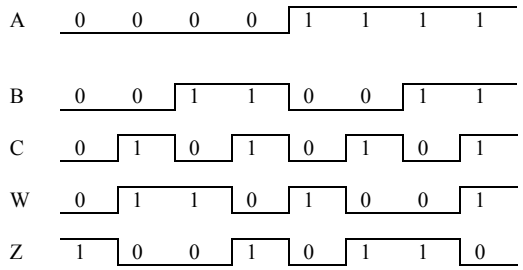




7. 3-input XNOR gate

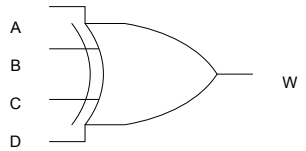
Input			Output	
A	B	C	W= A⊕B ⊕C	$Z = \overline{W}$ or $Z = \overline{A \oplus B \oplus C}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

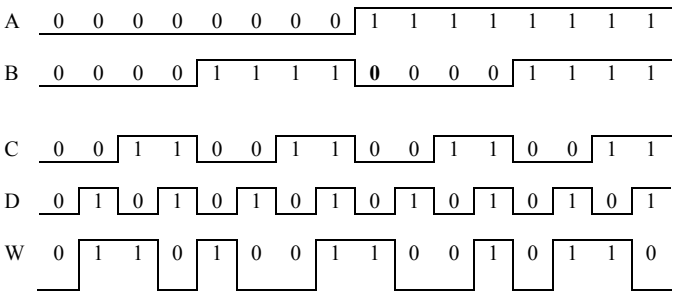




8. 4-input XOR gate

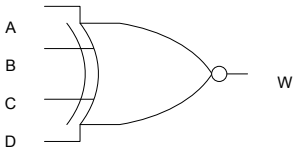
Input				Output
A	B	C	D	W = A ⊕ B ⊕ C ⊕ D
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

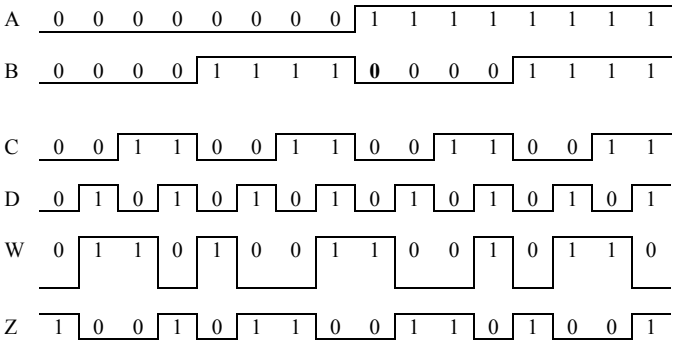




9. 4-input XNOR gate

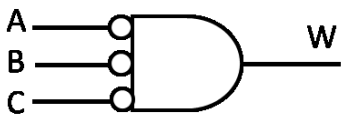
Input				Output	
A	B	C	D	W = $A \oplus B \oplus C \oplus D$	Z = $\overline{A \oplus B \oplus C \oplus D}$
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

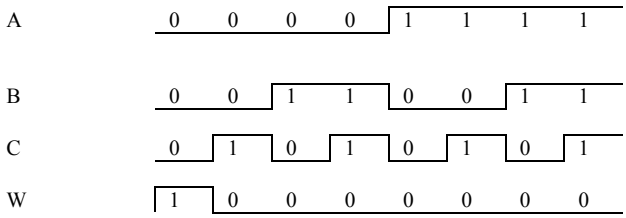




10. 3-input negative-AND gate

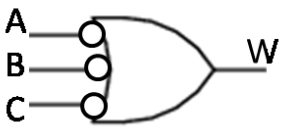
Input			Output
A	B	C	W= A'B'C'
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

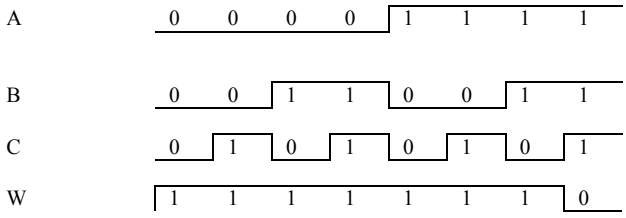




11. 3-input negative-OR gate

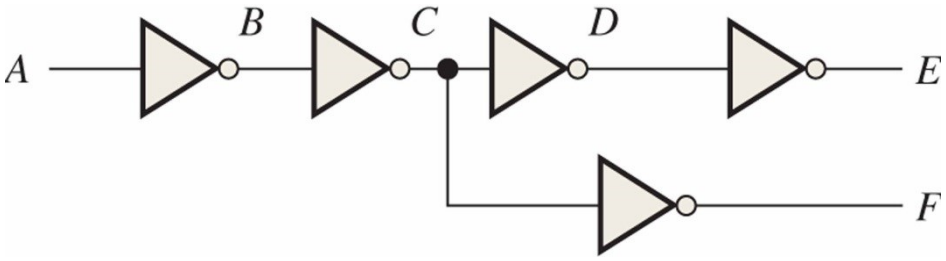
Input			Output
A	B	C	W= A'+B'+C'
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

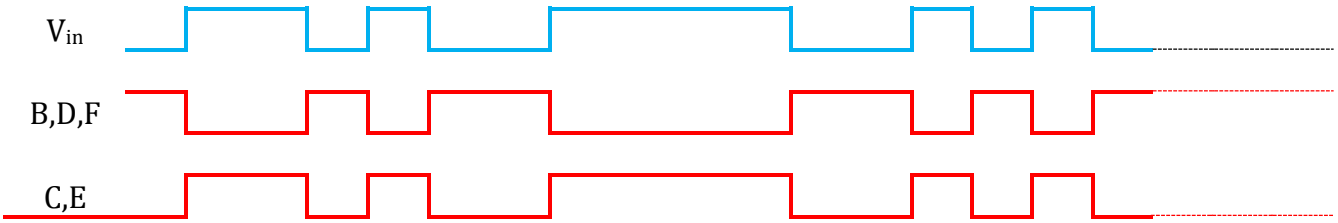




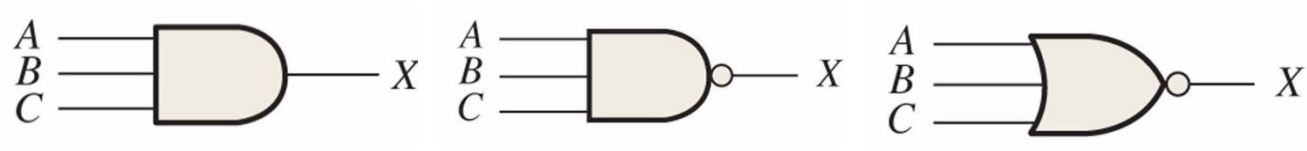
Applied knowledge questions

1. A series of *cascaded* inverters is shown in the figure below. Determine the logic level outputs at B, C, D, E and F if the V_{in} signal at A is given as shown.

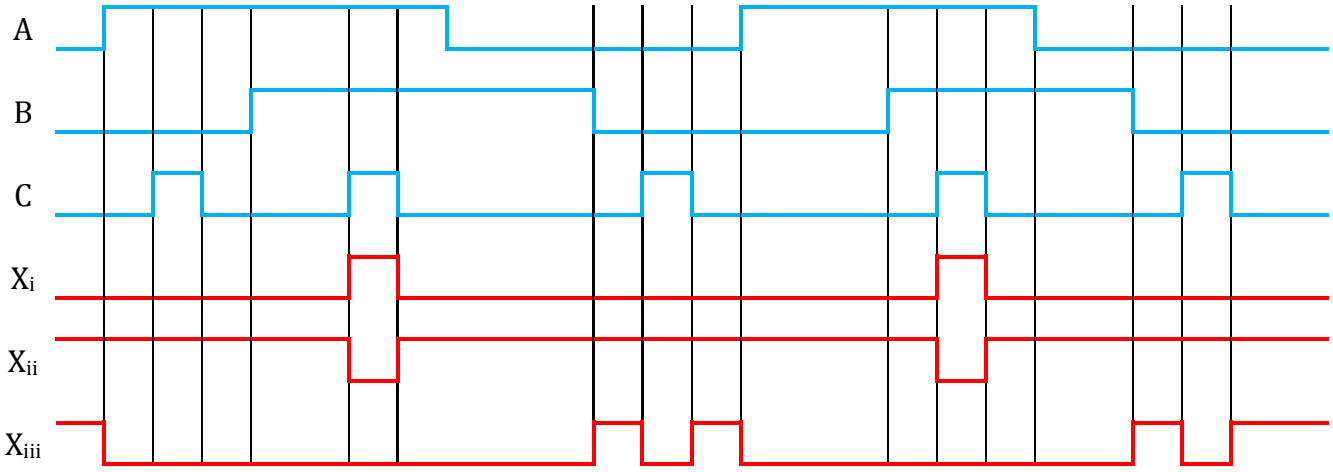




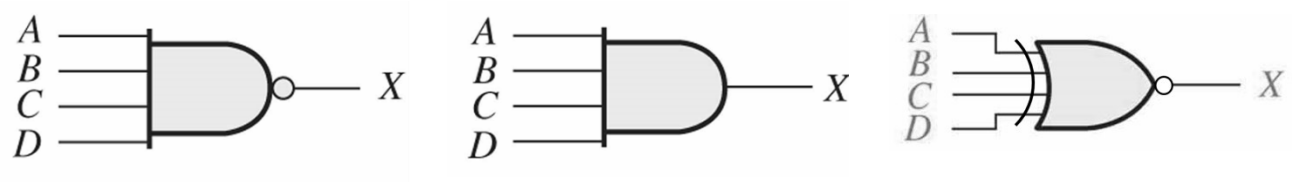
2. Determine the individual outputs of X to the tri-input gates below based on the timing diagrams shown for inputs A, B and C



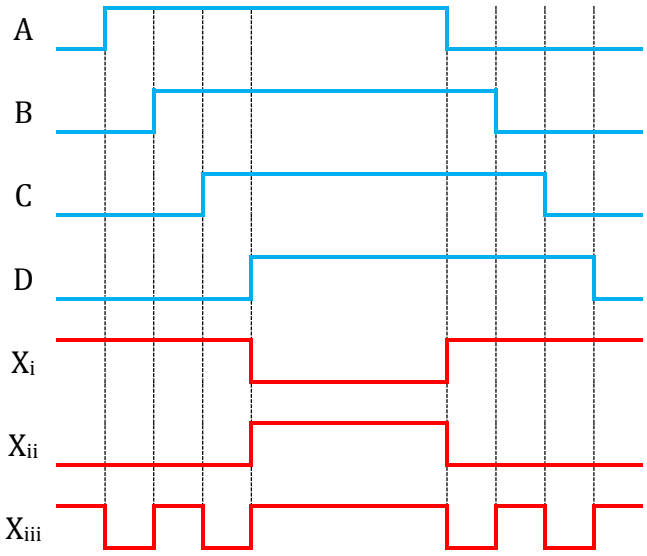
(i) (ii) (iii)



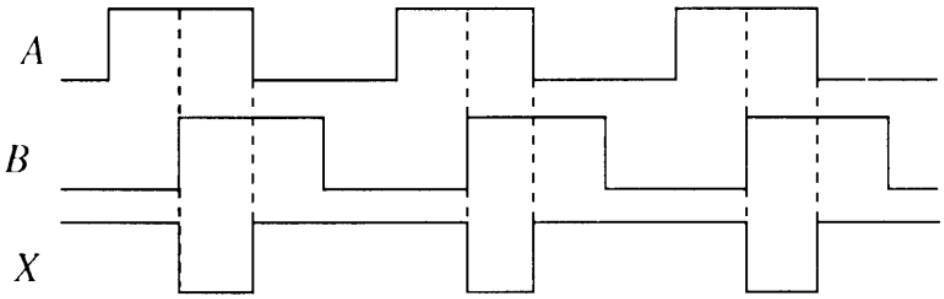
3. Determine the individual outputs of X to the quad-input gates below based on the timing diagrams shown for inputs A, B, C and D



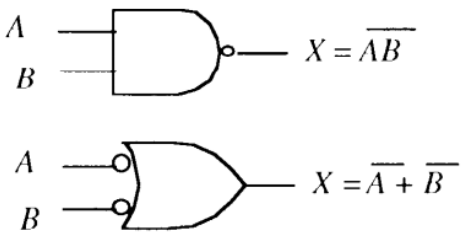
(i) (ii) (iii)



4. Complete the timing diagram for the two gates below based on the inputs A and B shown. What conclusions can you derive from the output of the gates?

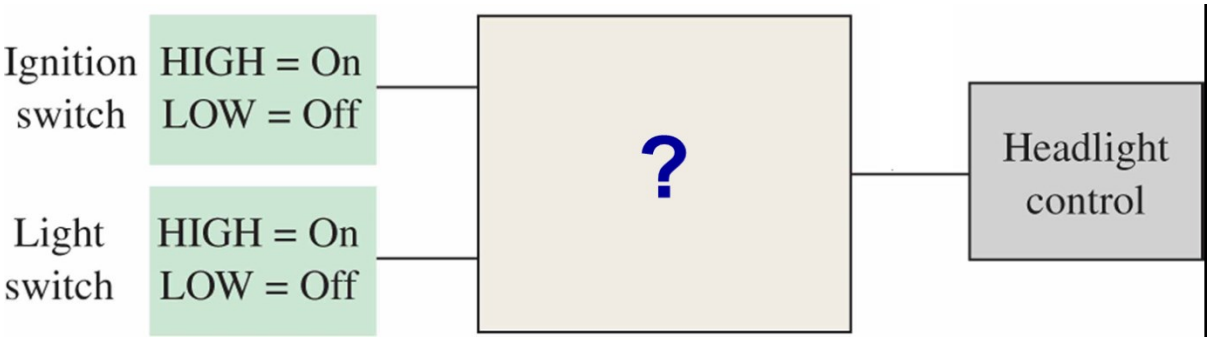


A	B	$\overline{A}$	$\overline{B}$	$\overline{AB}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	0	0



Both gates are equivalent to each other →demorgan's theorem

5. The headlights of a car only turn on (light up) when the car's ignition is turned ON with the key and the headlight switch is turned ON. Assuming that the headlight requires a LOW signal to turn it ON, what gate would be suitable to fit in the blank below to complete the circuit? Explain your answer.



Both inputs need to be high (ON) to activate its output, however the headlight is activated upon a LOW signal, thus necessitating a inverse of the output. Hence the NAND gate is used. (optional negative-OR)