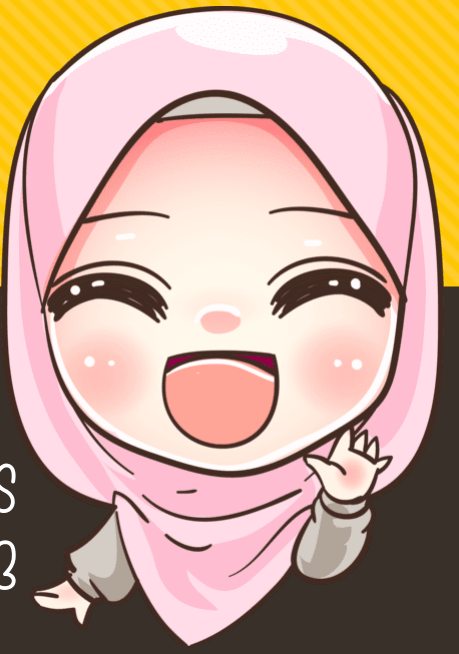
MMU
MULTIMEDIA UNIVERSITY

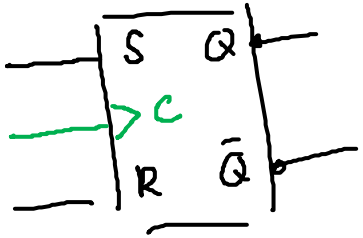
TUTORIAL 8
SEQUENTIAL LOGIC : FLIP FLOP

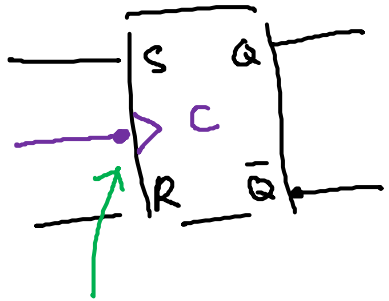


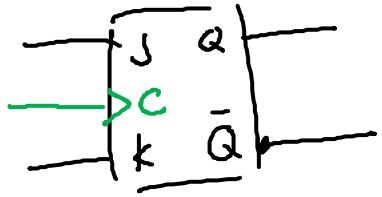
PDS0101: INTRODUCTION TO DIGITAL SYSTEMS
TRI 2, 2022-2023

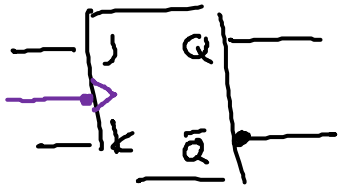
Flip - Flop

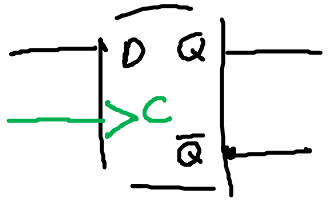
- S-R FF
  - PGT S-R FF
  - NGT S-R FF
- JK FF
  - PGT JK FF
  - NGT JK FF
- D FF
  - PGT D FF
  - NGT D FF

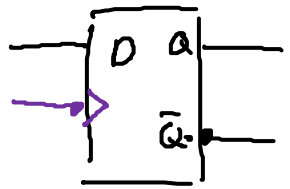












Q start low / reset

Q = 0

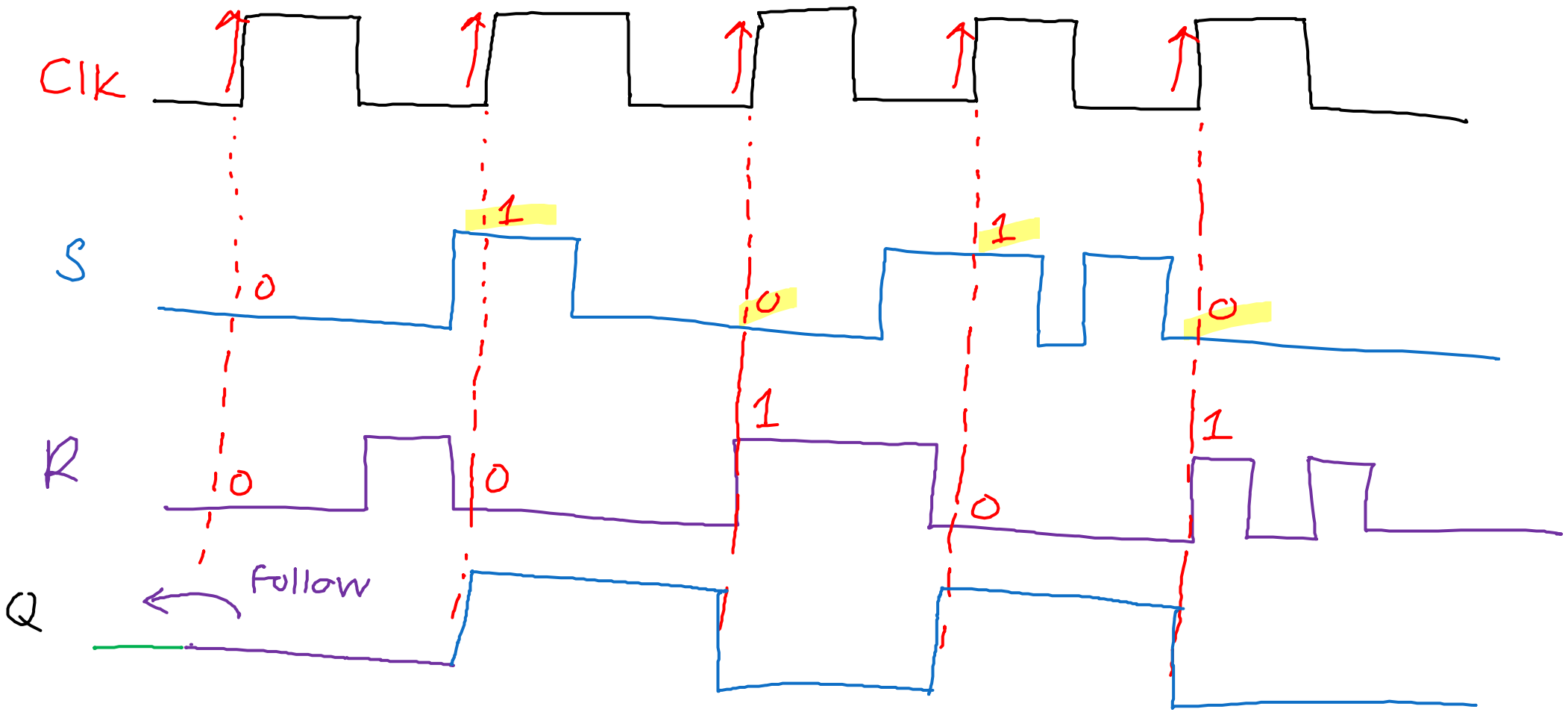
timing diagram

PGT SR FF

Q follow S

S	R	Q
0	1	0
1	0	1

periodic



Truth table

$2^2 = 4$

SR Latch

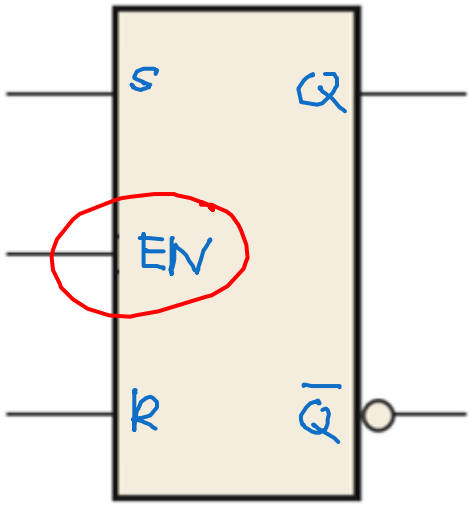
EN	S	R	Output	State
1	0	0	follow	rest
1	0	1	Q = 0	reset
1	1	0	Q = 1	set
1	1	1	follow	invalid

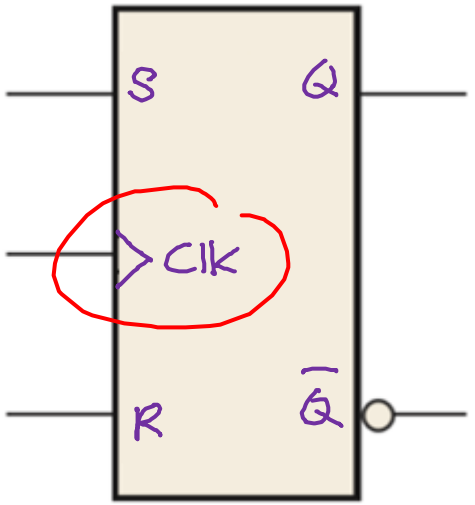
0

PGT SR FF

Clk	S	R	Output	State
↑	0	0	follow	rest
↑	0	1	Q = 0	reset
↑	1	0	Q = 1	set
↑	1	1	follow	invalid

EN = 1





Q follow S

S	R
0	1
1	0

NGT SR FF

clk	S	R	output	state
↓	0	0	follow	rest
↓	0	1	Q = 0	reset
↓	1	0	Q = 1	set
↓	1	1	follow	invalid

Q follow J

J	K
0	1
1	0

NGT JK FF

clk	J	K	output	state
↓	0	0	follow	rest
↓	0	1	Q = 0	reset
↓	1	0	Q = 1	set
↓	1	1	toggle	set/reset

PGT D FF Q follow D

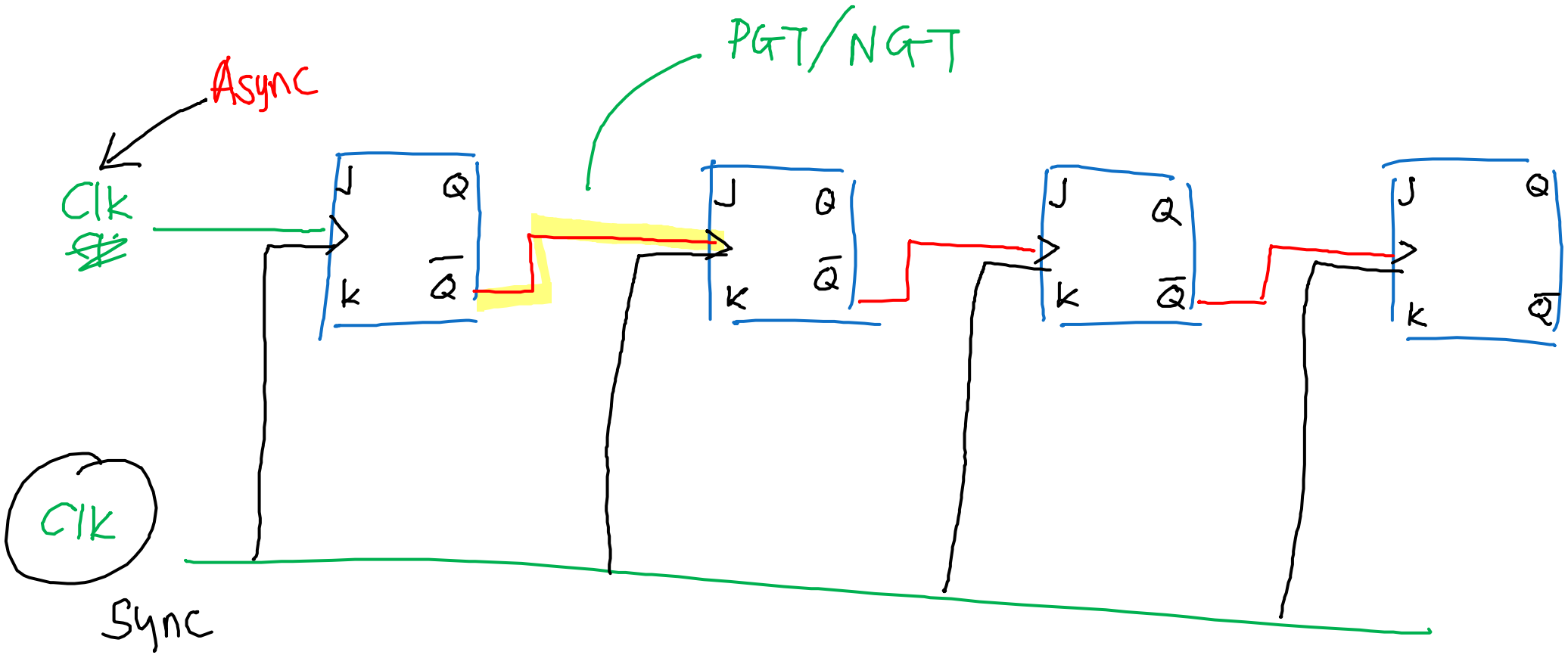
Clk	D		Output	state
↑	0		Q = 0	reset
↑	1		Q = 1	set

Async
Sync

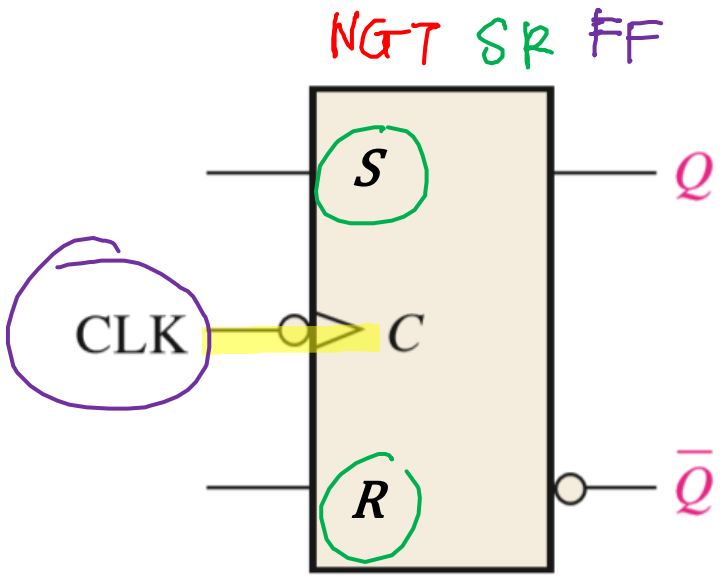
decade ; mod – 12 counter

1010

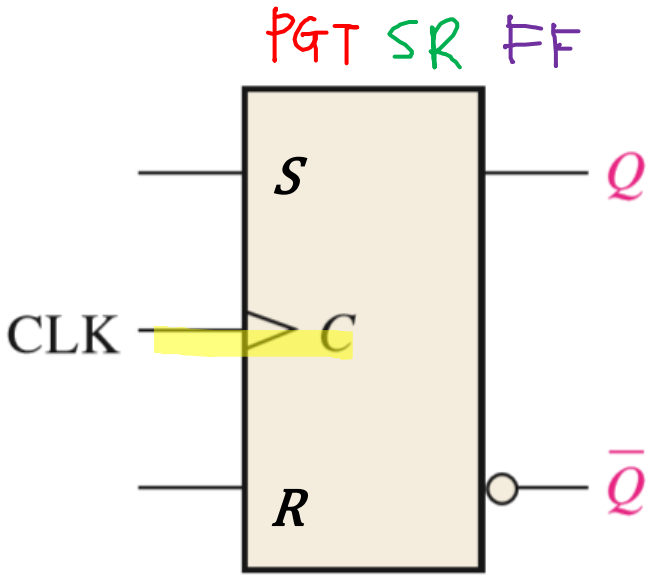
8	4	2	1
1	0	1	0



1. Identify the two **flip-flops** shown below and draw their respective **timing diagrams** for their **Q** outputs based on the inputs shown. The FF are initially **RESET.** Q = 0

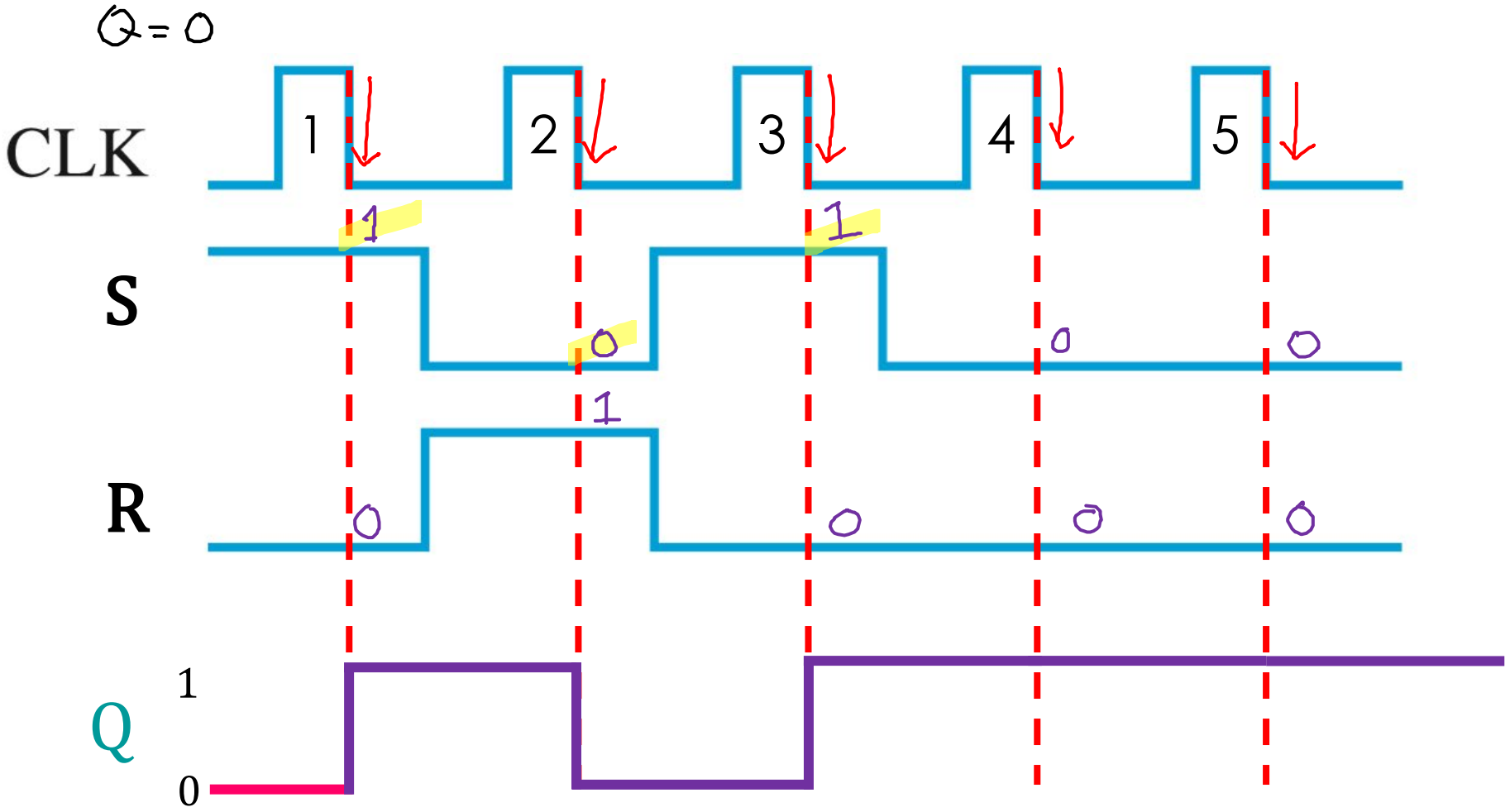


a)Negative Going Edge-triggered(NGT)

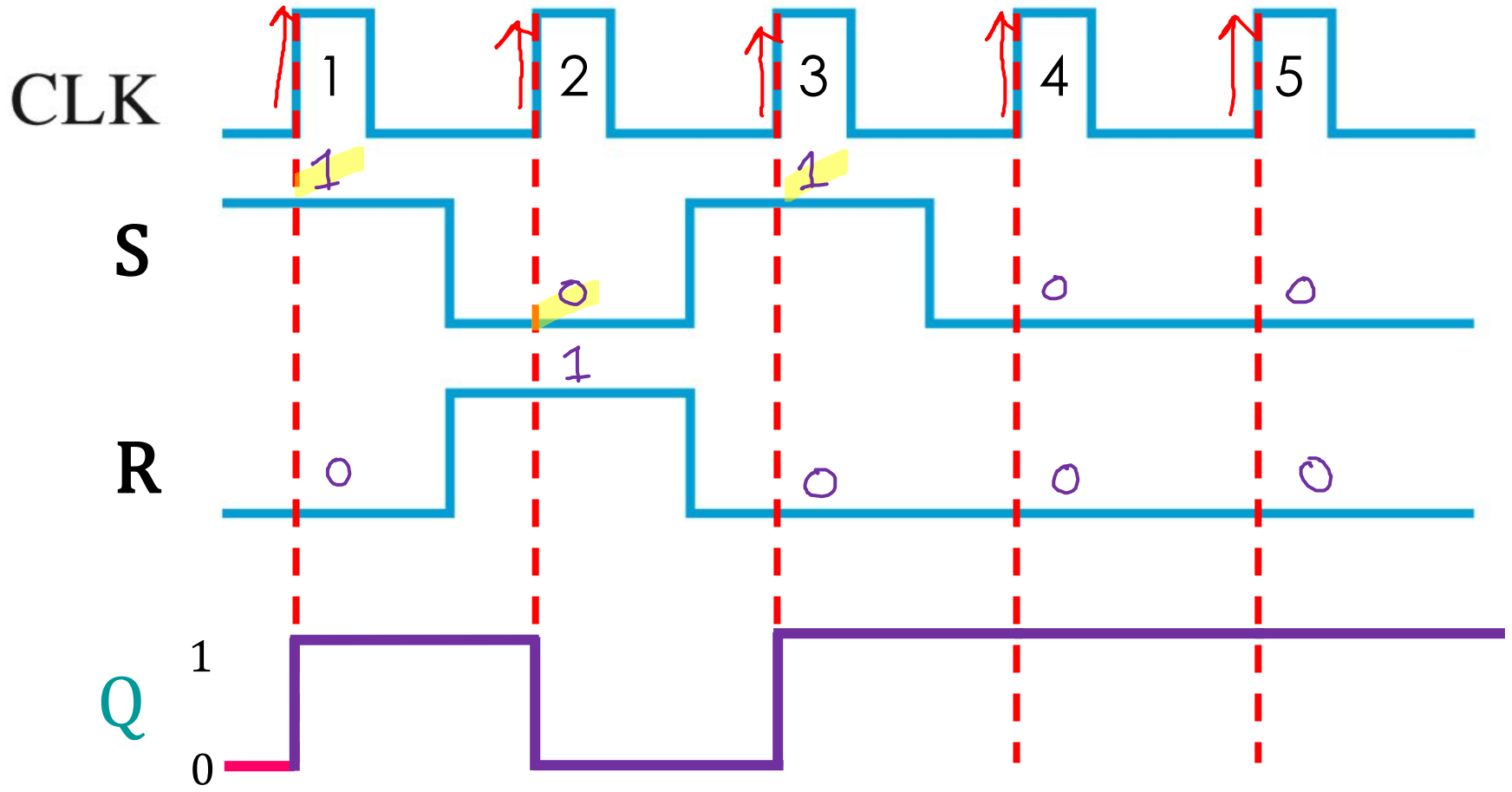


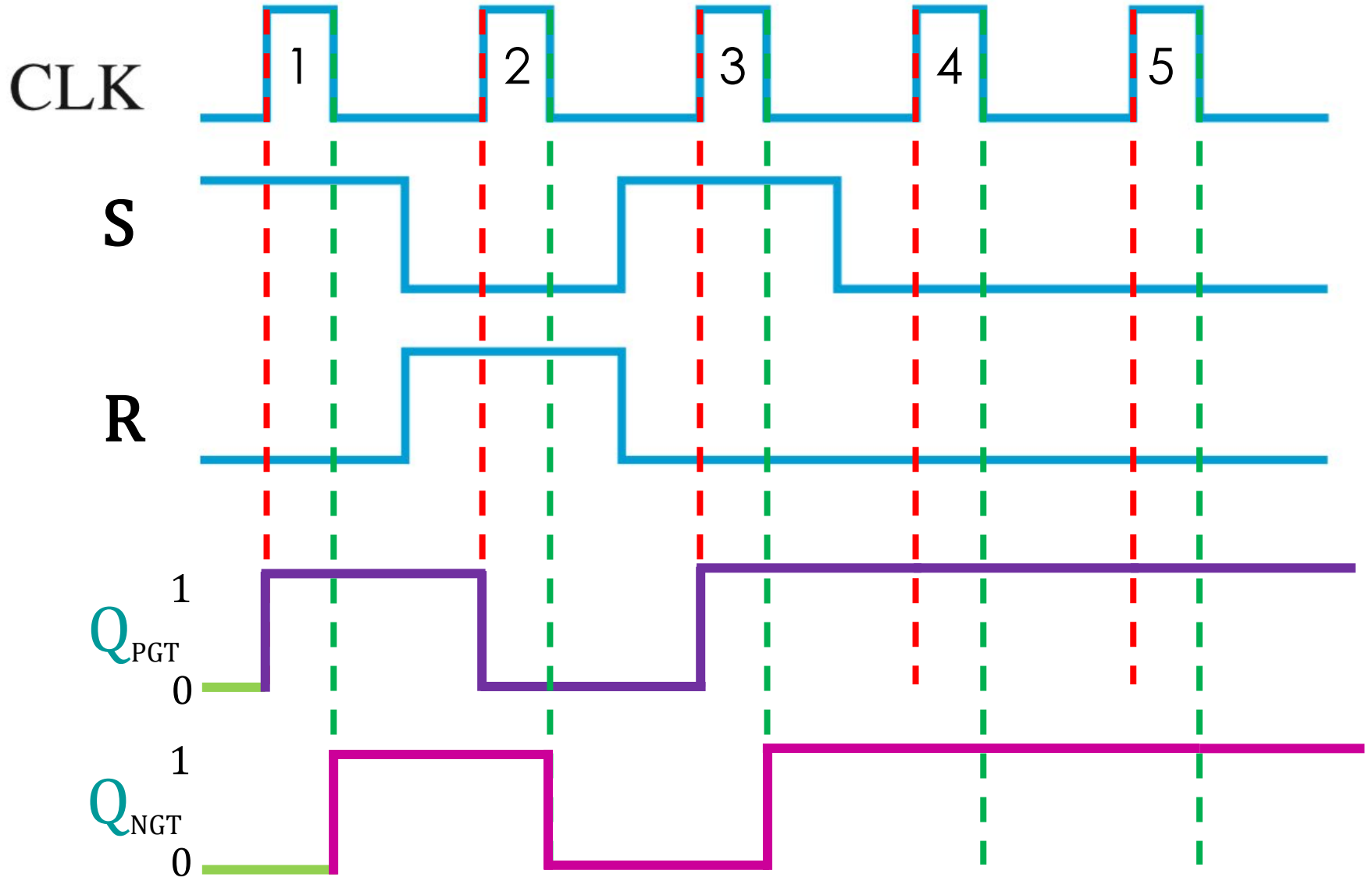
b)Positive Going Edge-triggered(PGT)

The FF are initially **RESET**. **Negative Going Edge-triggered(NGT)**

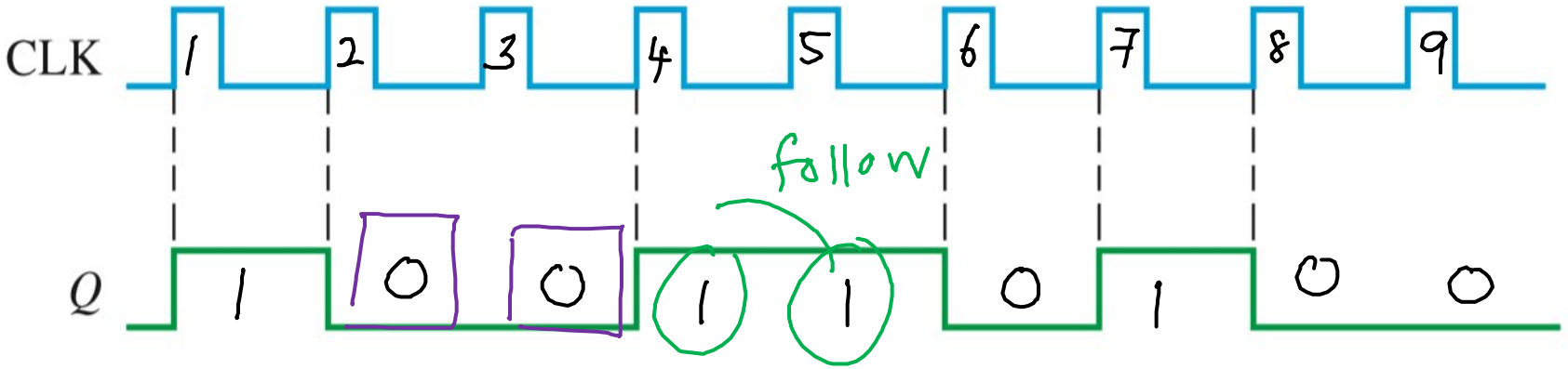


The FF are initially **RESET**. **Positive Going Edge-triggered(PGT)**




CLK
1
2
3
4
5
S
R
1
Q_{PGT}
0
1
Q_{NGT}
0

2. The Q output of a **positive going ET** S-R flip-flop is shown in the timing diagram below. Determine the **correct inputs to S and R** that are required to produce this output.

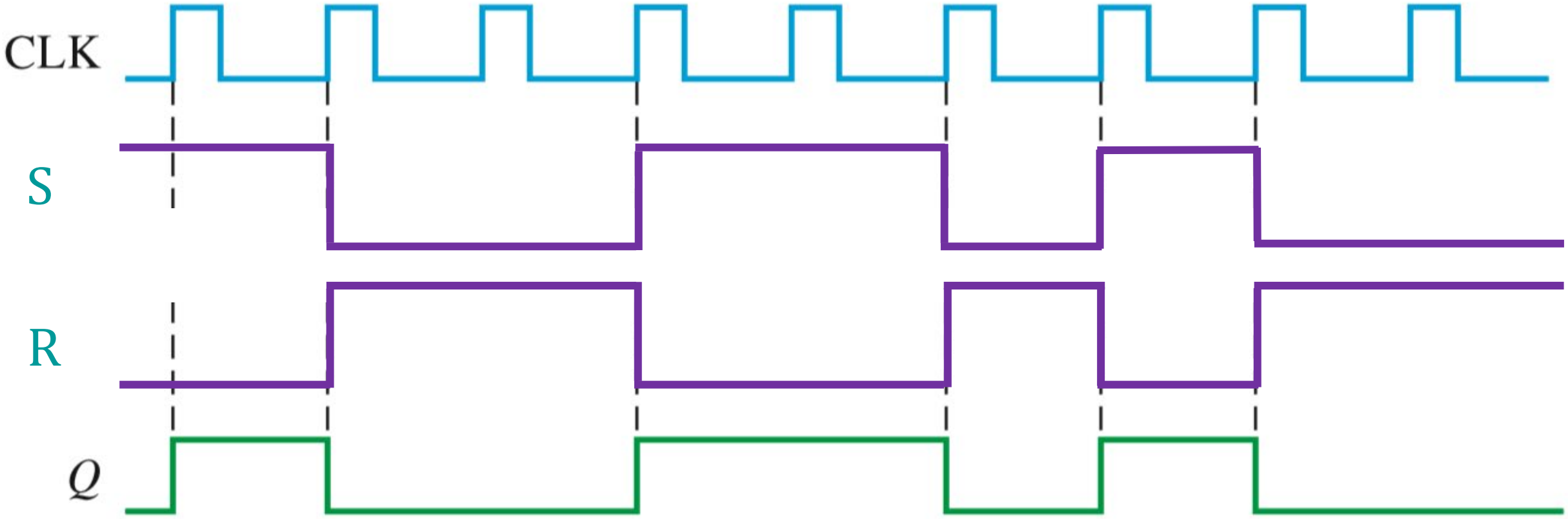


Q follow S

follow

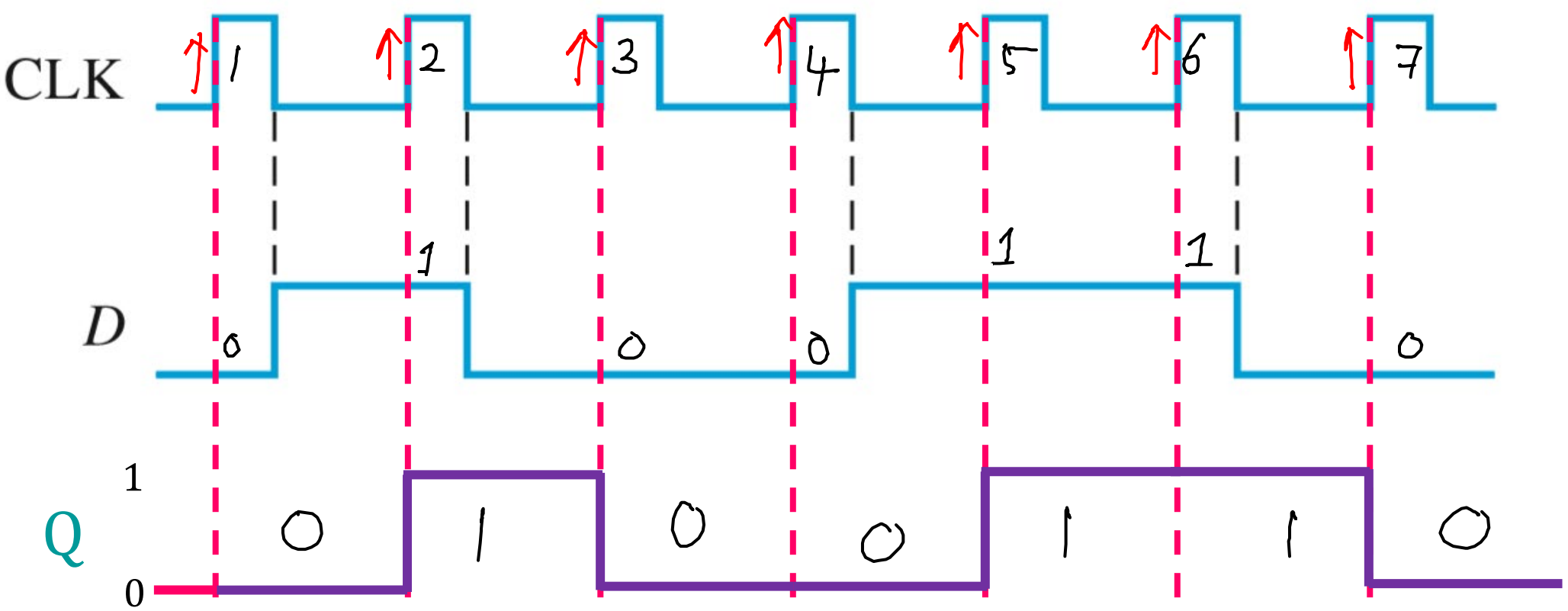
CLK	S	R	Q (OUTPUT)
0			
1	1	0	1
2	0	1	0
3	0 0 1	1 0 1	0
4	1	0	1
5	0 1 1	0 0 1	1
6	0	1	0
7	1	0	1
8	0	1	0
9	0 0 1	0 1 1	0

2. The Q output of a **positive going ET** S-R flip-flop is shown in the timing diagram below. Determine the **correct inputs to S and R** that are required to produce the this output.

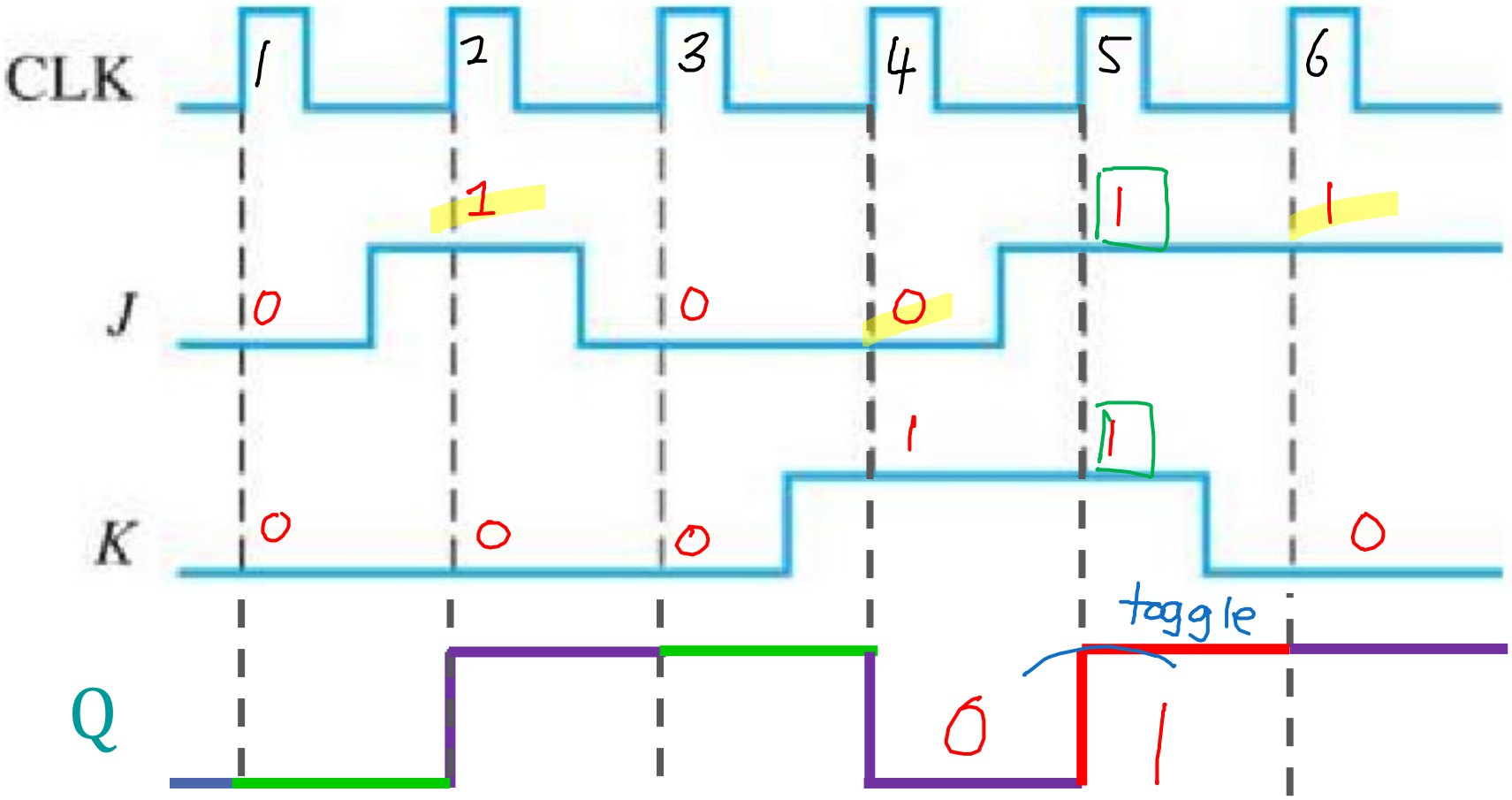


3. Draw the Q output of a **D flip-flop** with the inputs shown in the timing diagram below. You may assume that the FF is **positive going triggered** and **Q** is **initially LOW** Q = 0

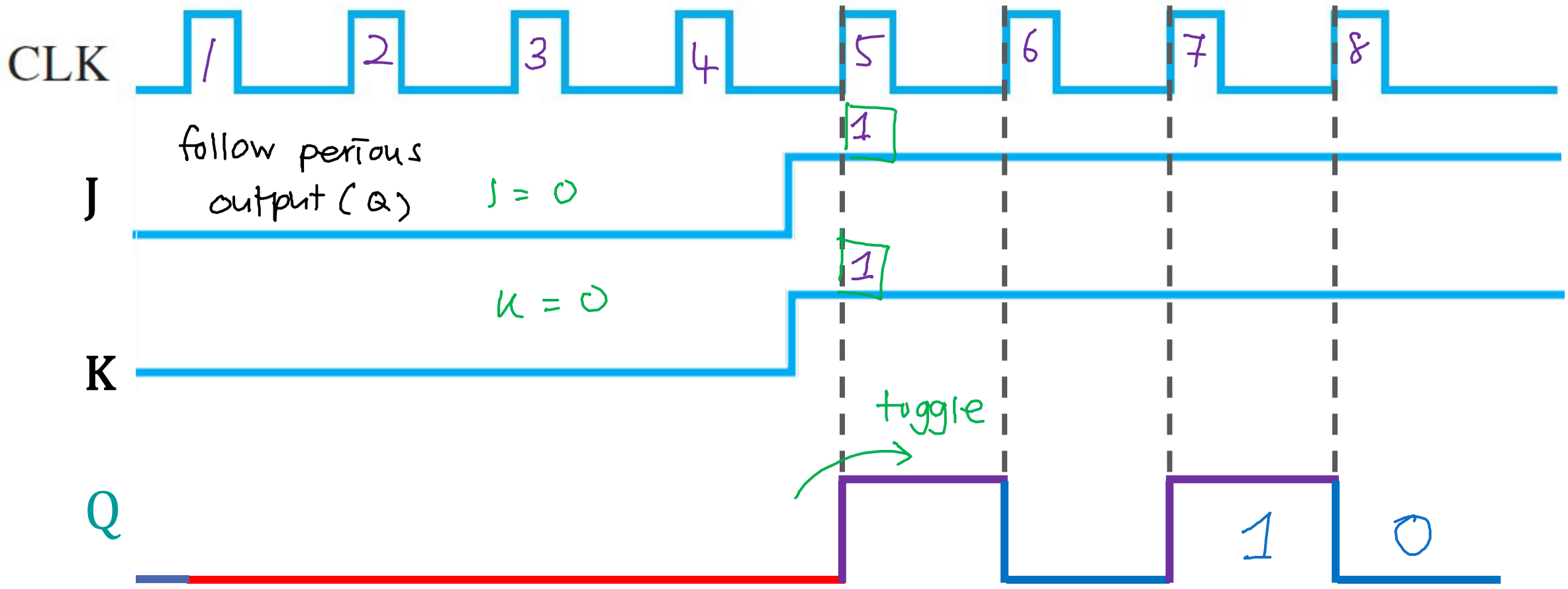
PGT



4. For a **positive** going ET J-K flip-flop with inputs as shown below, determine the Q output relative to the CLK if Q starts out **LOW**

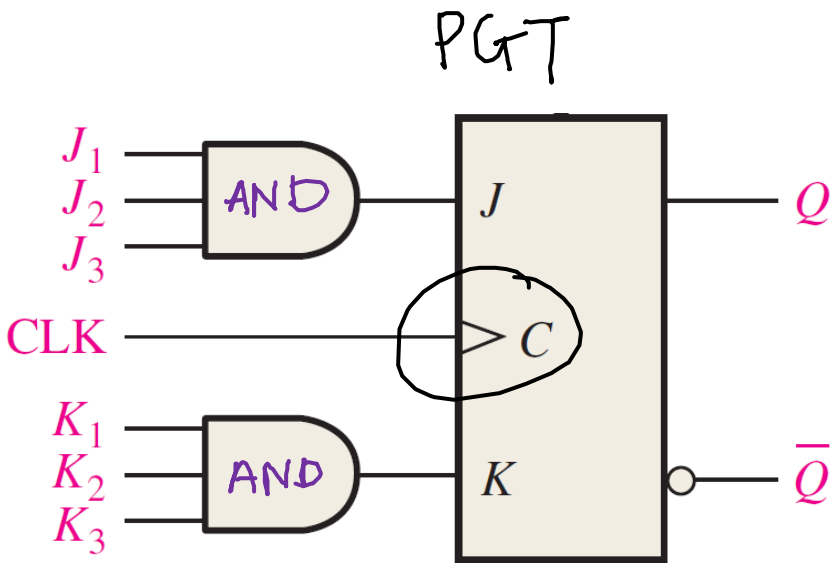


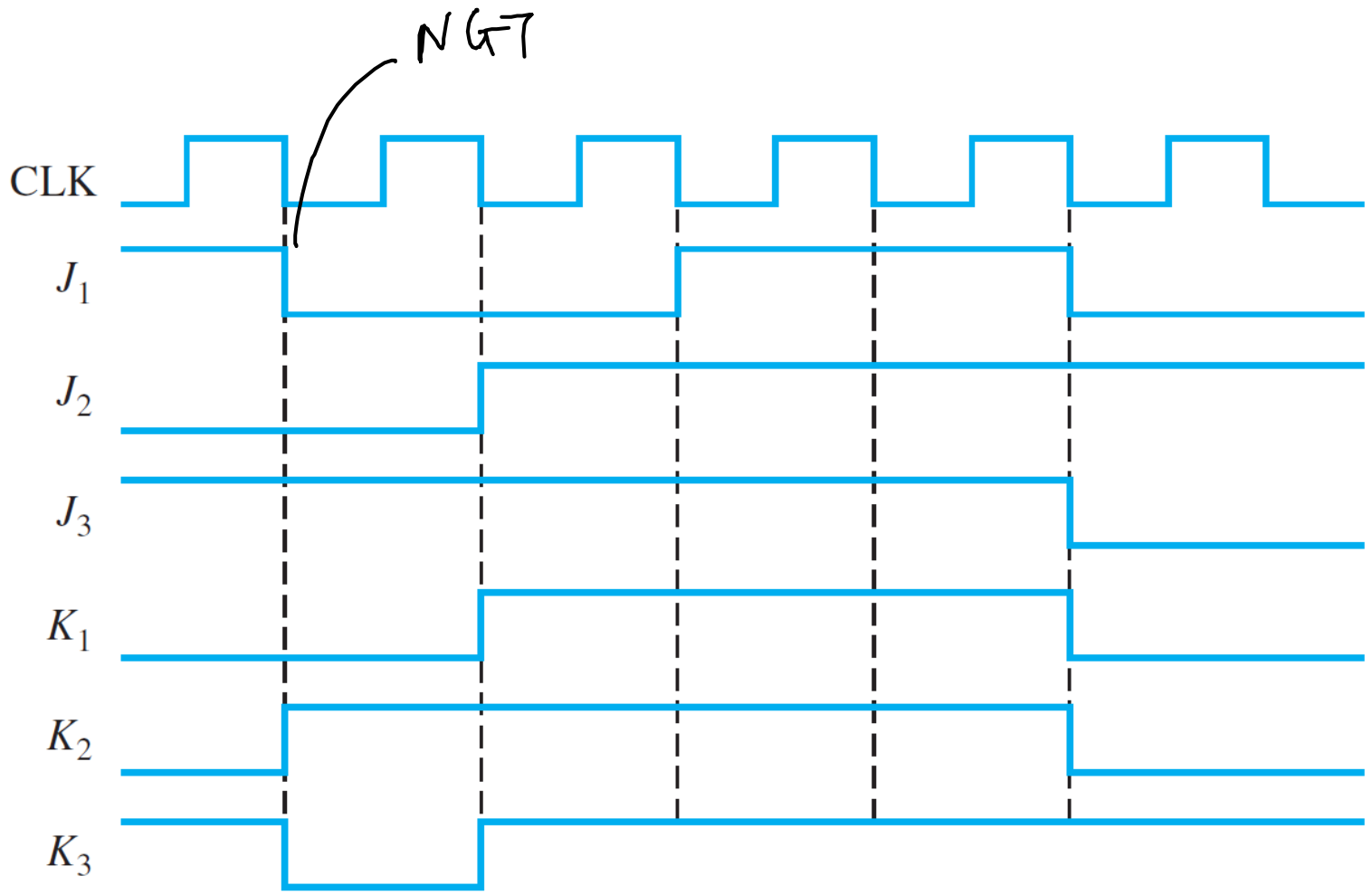
5. For a **positive** going ET J-K flip-flop with inputs as shown below, determine the Q output relative to the CLK if Q starts out **LOW**



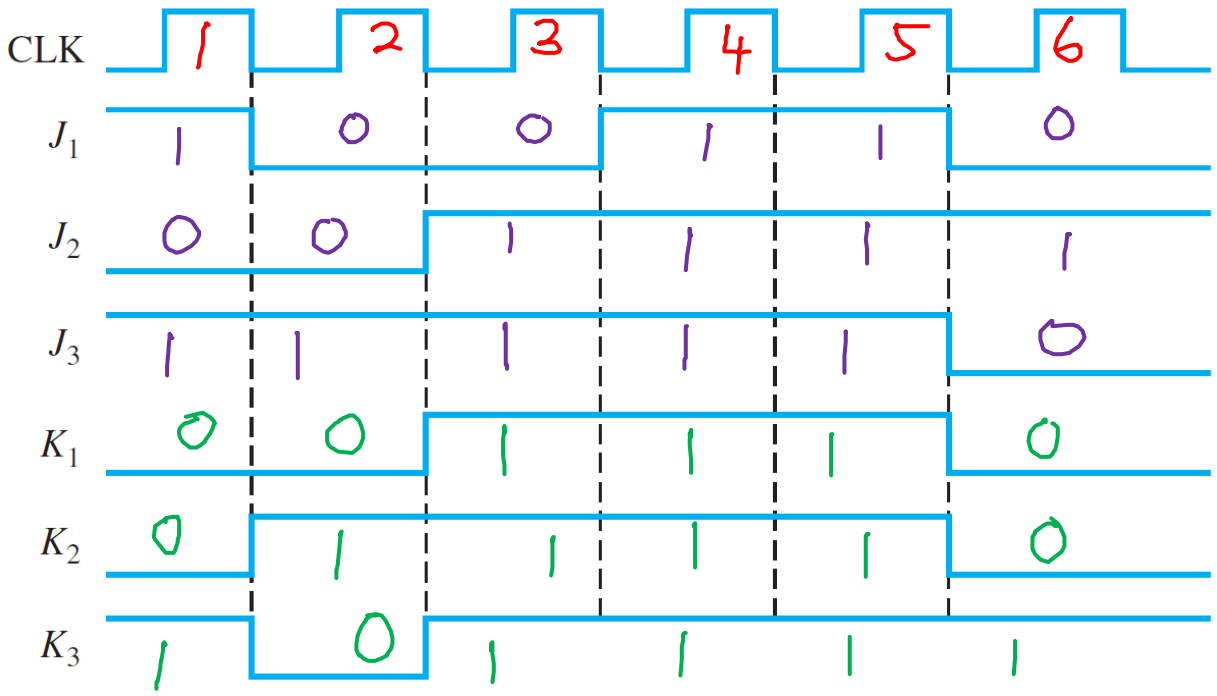
6. For the circuit shown below, determine the output of **Q** (which starts out **LOW**) based on the inputs shown the in the timing diagram

All input ONE ; output ONE



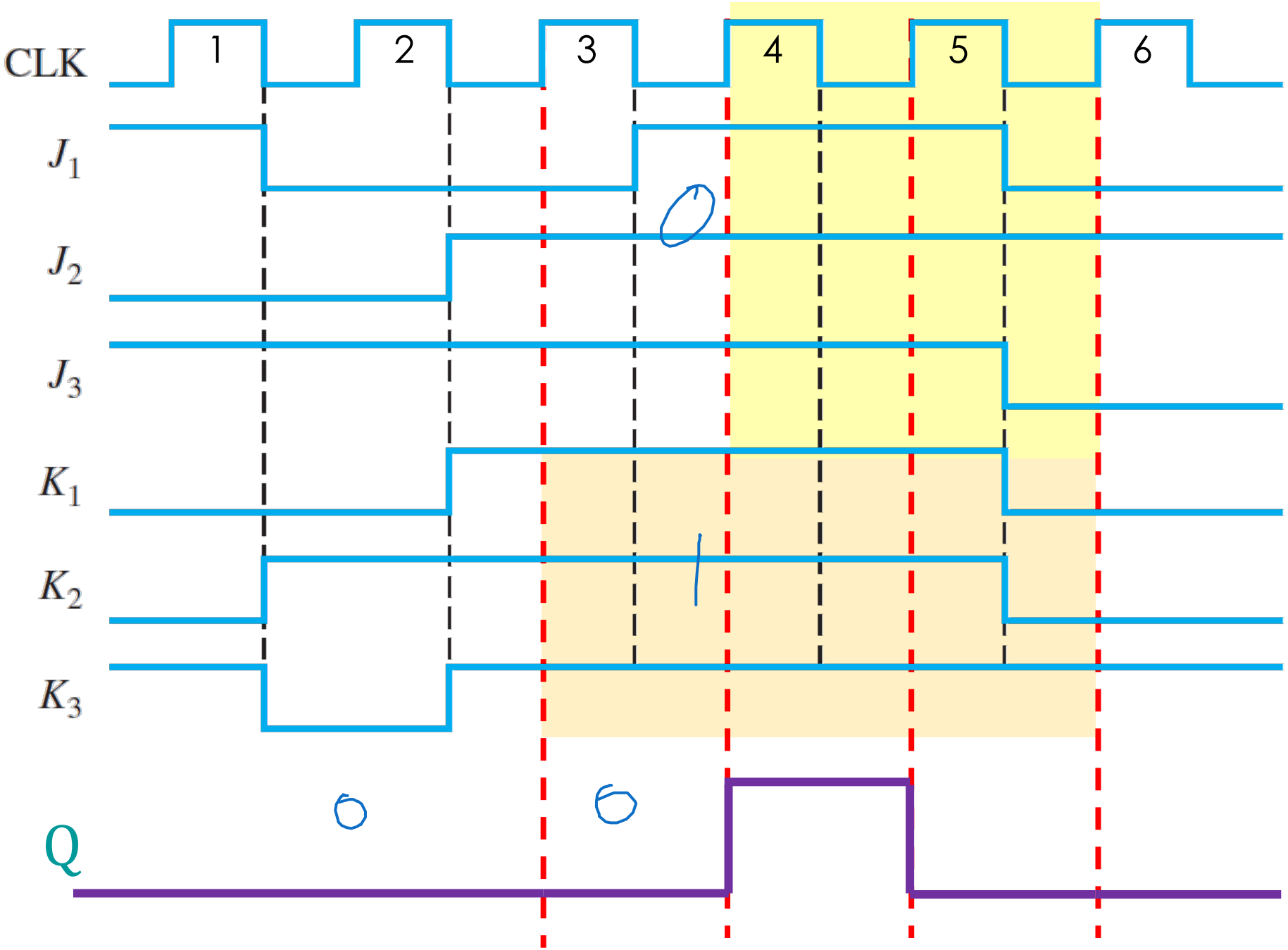


6. For the circuit shown below, determine the output of **Q** (which starts out **LOW**) based on the inputs shown the in the timing diagram

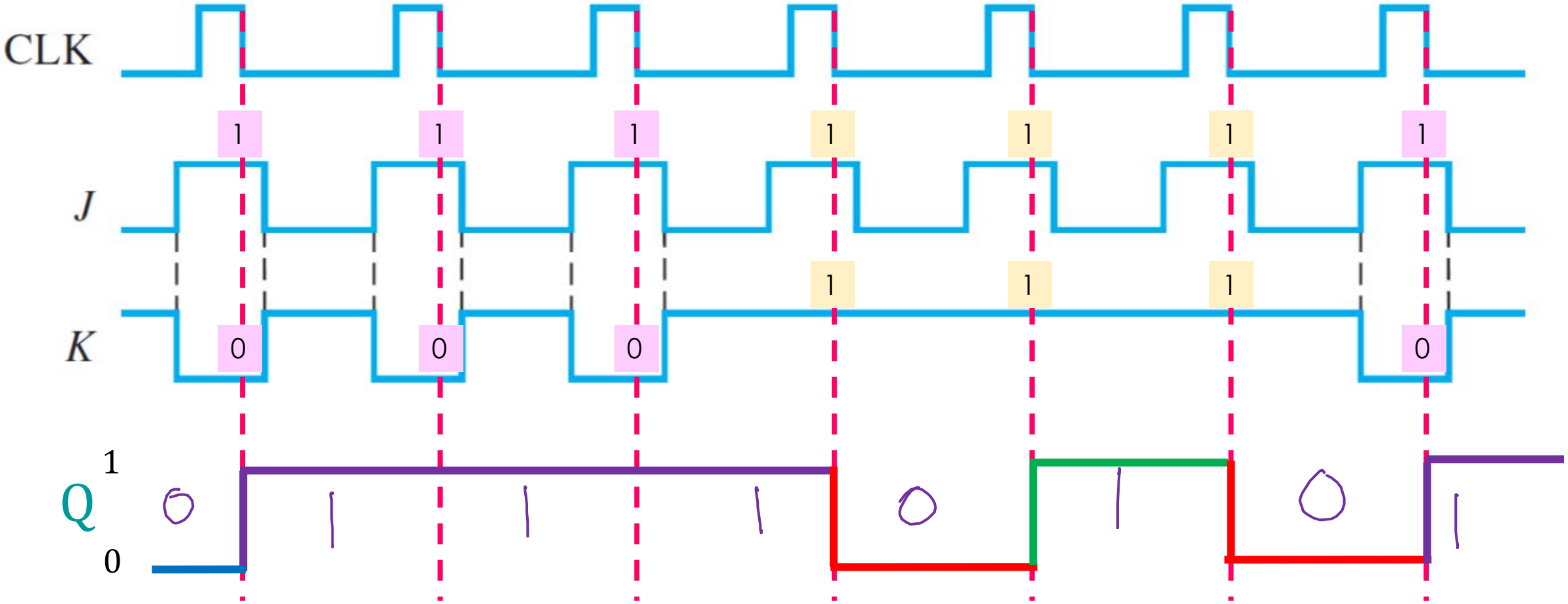


$Q_0 = 0$

CLK	J_1	J_2	J_3	J	K_1	K_2	K_3	K	Q
1	1	0	1	0	0	0	1	0	0
2	0	0	1	0	0	1	0	0	0
3	0	1	1	0	1	1	1	1	0
4	1	1	1	1	1	1	1	1	1
5	1	1	1	1	1	1	1	1	0
6	0	1	0	0	0	0	1	0	0


CLK
1
2
3
4
5
6
J_1
J_2
J_3
K_1
K_2
K_3
Q

7. For a **negative** going ET J-K FF with the inputs shown below, determine the Q output waveform relative to the CLK if **Q is initially RESET** Q = 0



END DISCUSSIONS
ANY QUESTIONS ??