MULTIMEDIA UNIVERSITY

PDS0101 Introduction to Digital Systems

Tutorial 9

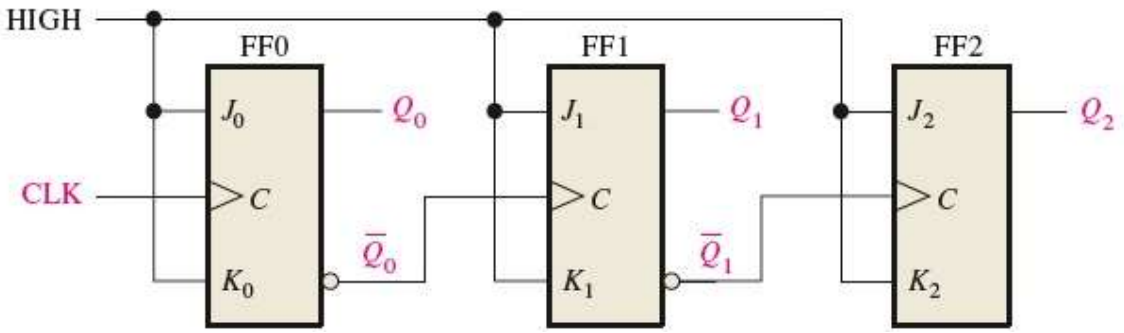
NOTE

Answers shown may be only one of many possibilities available. Please approach your tutor if you have an alternative answer of which you are not sure of. Any errors and omissions in the answers are deeply regretted.

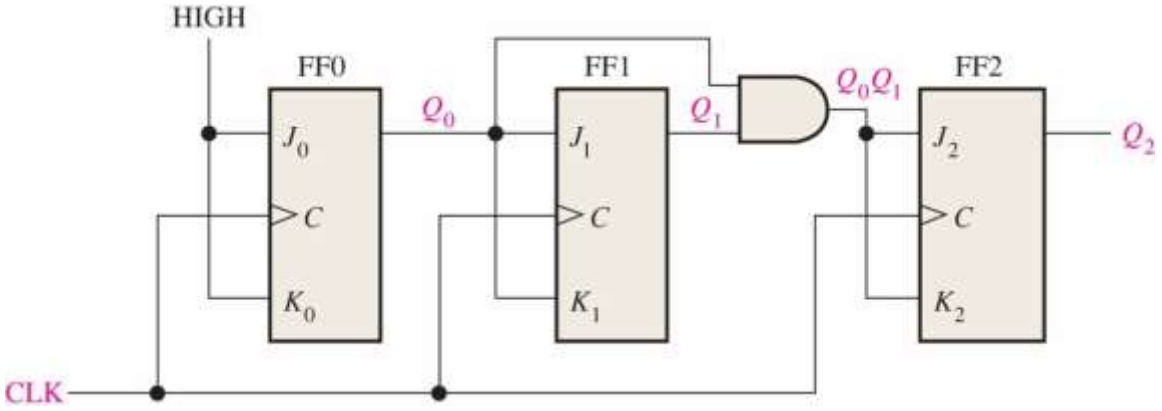
Theory based questions

1. What is the difference between an asynchronous and synchronous counter?
   In a synchronous counter, all FFs are clocked simultaneously and change upon the pulse of the CLK input. The asynchronous counter only has the first FF (usually 'MSB') triggered by the CLK whilst the remaining FFs are triggered by the outputs of the previous FF (hence the ripple effect)

2. Draw the logic circuit diagrams of a 3-bit asynchronous and 3-bit synchronous counter

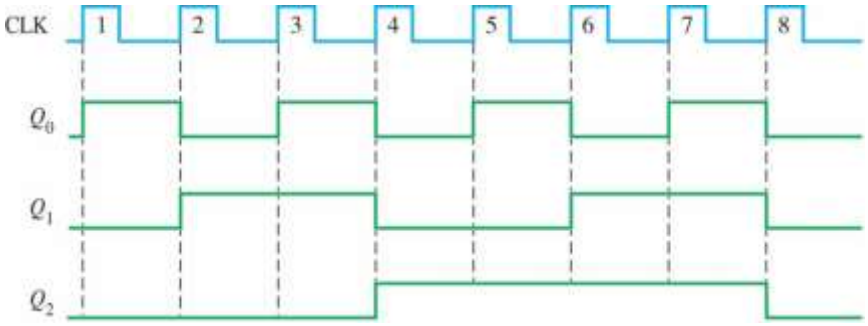


Async



Sync

3. Draw the timing diagrams of the outputs from both counters in (2)



NOTE: both counters have the same timing diagram waveforms

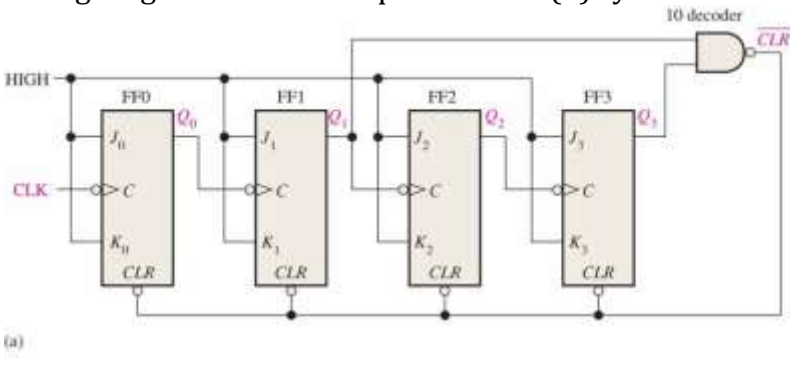
4. How many states would a modulus-15 counter have? What is the minimum number of FFs required to create this counter?

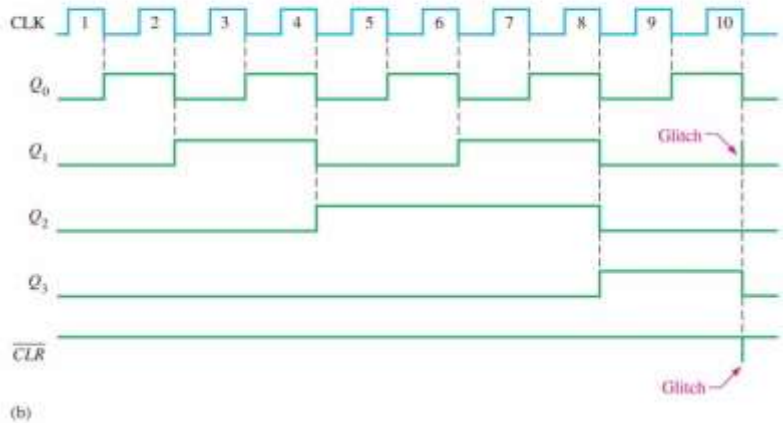
Modulus-15 counter has 15 states. Requires 4 FFs (with 2^4 states) to fully implement

5. Explain the meaning of "*modulus of a counter*" and how it can be used to change regular counters

The modulus of a counter is the number of unique states that the counter will sequence through i.e. The maximum module of any binary counter is 2^n. Counters can also be designed to have a number of states in their sequence that is less than the maximum of 2^n. These counters used a truncated sequence - the counter is forced to recycle before going through all of its possible states. An example of a truncated sequence counter is a decade counter.

6. Draw the logic circuit diagram of a asynchronous decade counter and draw is corresponding timing diagram from its outputs for one (1) cycle.





Applied knowledge based questions

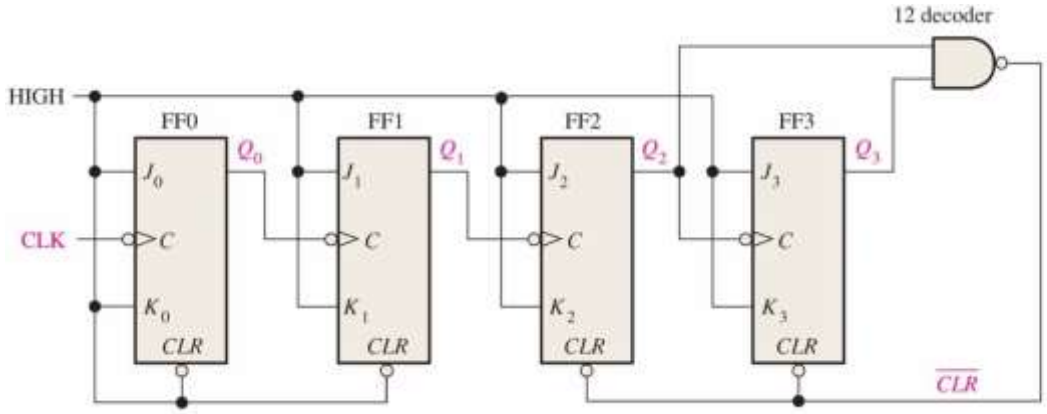
1. Show how an asynchronous counter with a modulus of 12 can be constructed using flip-flops

Mod-12 requires 4 FFs minimum to implement (3FFs only have 8 states which is not enough). The cycle of 4 FFs through all its possible combinations is as follows in the truth table below

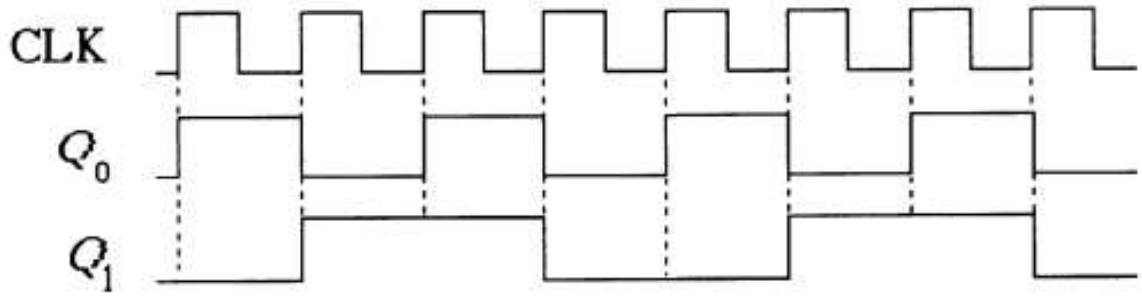
Q3	Q2	Q1	Q0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Counter recycles here

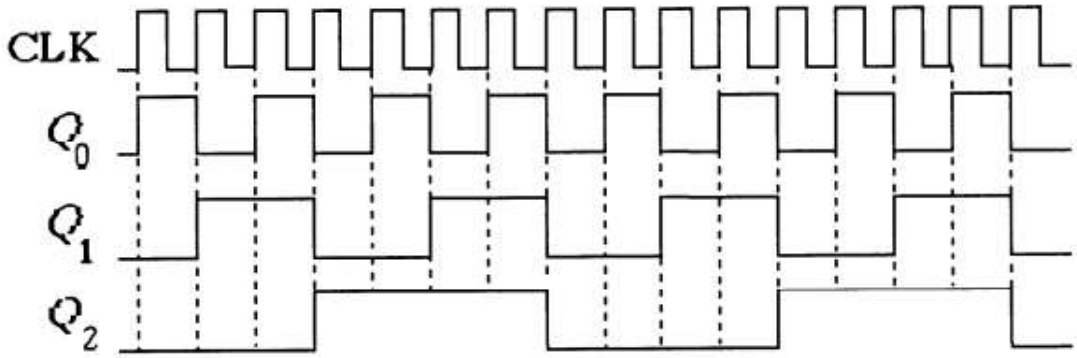
When Q3 and Q2 both are HIGH, the counter recycles, so a decoder can be placed to identify when this condition occurs and CLRs the FF



2. For the ripple counter shown below, show the complete timing diagram for the outputs at Q_0 and Q_1 for eight clock pulses



3. For the counter below, show the complete timing diagram for output waveforms at Q_0, Q_1 and Q_2 for sixteen clock cycles.



4. Design a counter to produce the following cyclic sequence

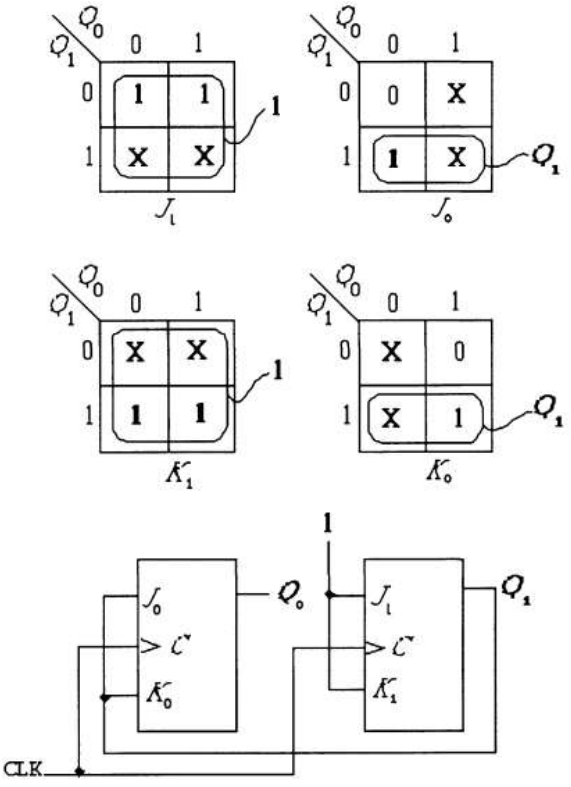
$00 \rightarrow 10 \rightarrow 01 \rightarrow 11$

NEXT-STATE TABLE

Present State		Next State	
Q_1	Q_0	Q_1	Q_0
0	0	1	0
1	0	0	1
0	1	1	1
1	1	0	0

TRANSITION TABLE

Output State Transitions (Present state to next state)		Flip-Flop Inputs			
Q_1	Q_0	J_1	K_1	J_0	K_0
0 to 1	0 to 0	1	X	0	X
1 to 0	0 to 1	X	1	1	X
0 to 1	1 to 1	1	X	X	0
1 to 0	1 to 0	X	1	X	1



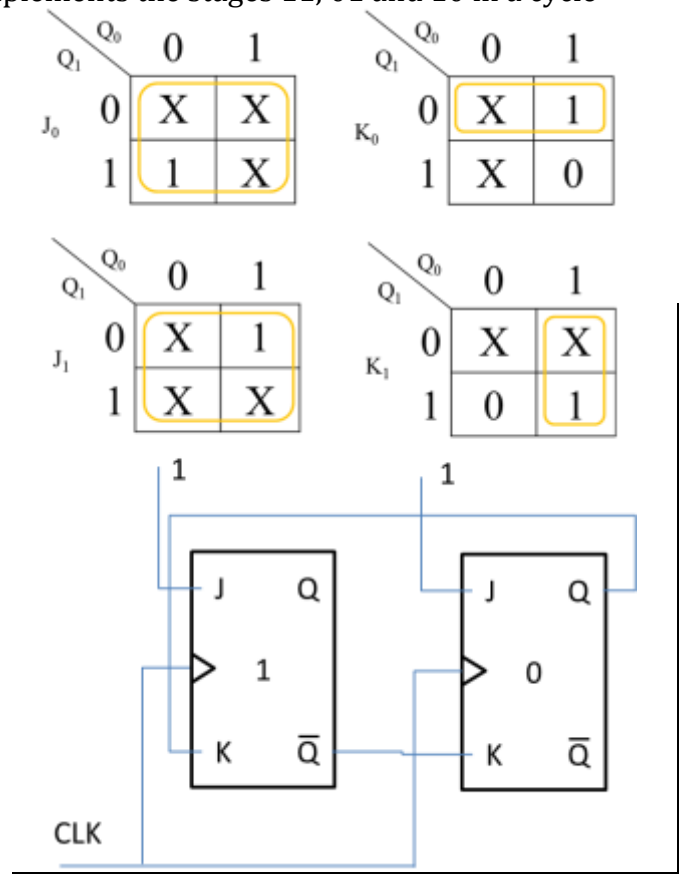
5. Alter the counter from (4) so that it only implements the stages 11, 01 and 10 in a cycle

NEXT STATE TABLE

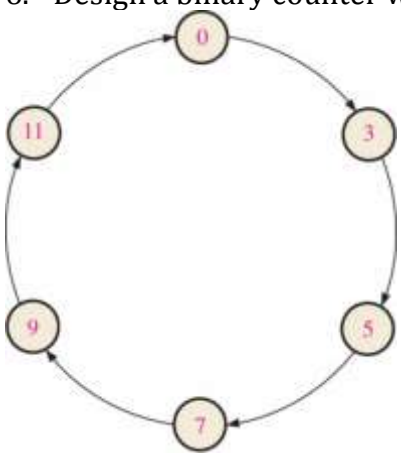
Present		Next	
Q_1	Q_0	Q_1	Q_0
1	1	0	1
0	1	1	0
1	0	1	1
0	0	X	X

TRANSITION TABLE

Present		Next		FF inputs			
Q_1	Q_0	Q_1	Q_0	J_1	K_1	J_0	K_0
1	1	0	1	X	1	X	0
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
0	0	X	X	X	X	X	X

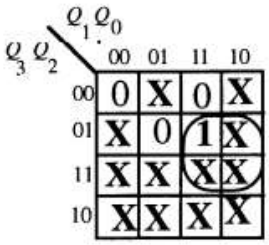


6. Design a binary counter with the sequence shown in the state diagram below

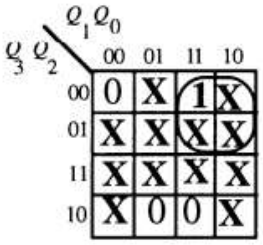


Present State				Next State			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	1	1
0	0	1	1	0	1	0	1
0	1	0	1	0	1	1	1
0	1	1	1	1	0	0	1
1	0	0	1	1	0	1	1
1	0	1	1	0	0	0	0

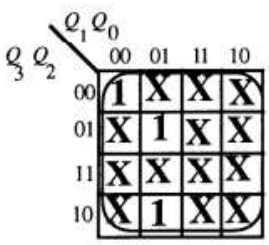
Output State Transitions (Present State to next state)				Y	Flip-flop Inputs			
Q_3	Q_2	Q_1	Q_0		J_3K_3	J_2K_2	J_1K_1	J_0K_0
0 to 0	0 to 0	0 to 1	0 to 1	1	0X	0X	1X	1X
0 to 0	0 to 1	1 to 0	1 to 1	1	0X	1X	X1	X0
0 to 0	1 to 1	0 to 1	1 to 1	1	0X	X0	1X	X0
0 to 1	1 to 0	1 to 0	1 to 1	1	1X	X1	X1	X0
1 to 1	0 to 0	0 to 1	1 to 1	1	X0	0X	1X	X0
1 to 0	0 to 0	1 to 0	1 to 0	1	X1	0X	X1	X1



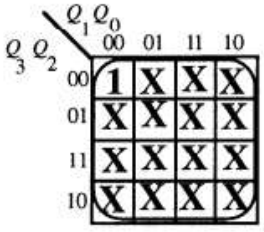
$J_3 = Q_2Q_1$



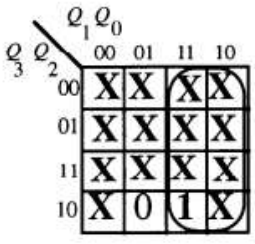
$J_2 = \overline{Q}_3Q_1$



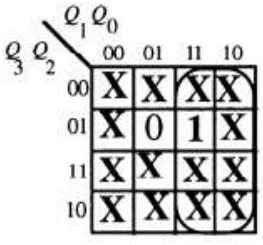
$J_1 = 1$



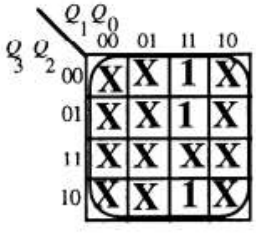
$J_0 = 1$



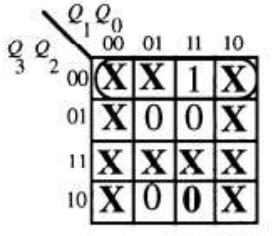
$K_3 = Q_1$



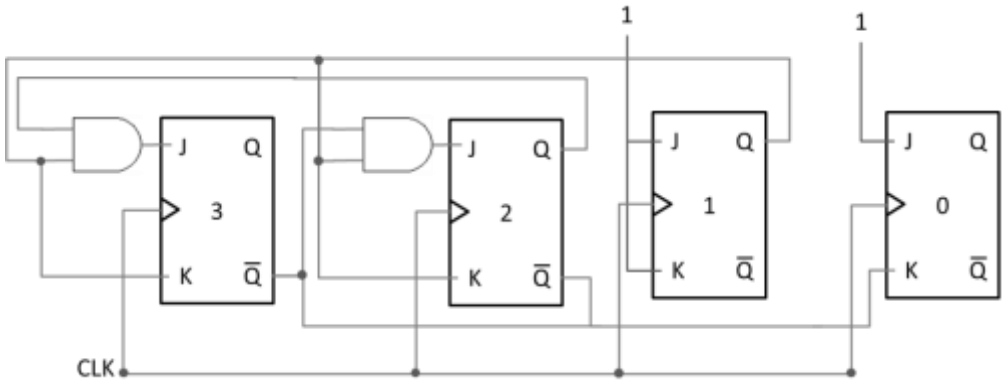
$K_2 = Q_1$



$K_1 = 1$

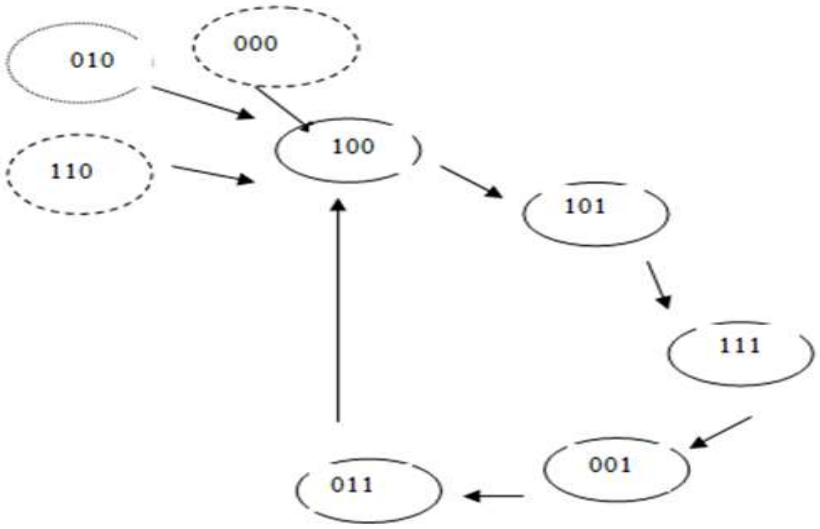


$K_0 = \overline{Q}_3\overline{Q}_2$



7. Design a counter using J-K FFs that follow the cyclic sequence 4,5,7,1,3. Find the minimum number of FFs required to implement the counter and any unwanted FF sequences in the counter go to 4

State transition diagram:



Truth table for 74LS76 IC (JK flip-flop)

$\overline{PRESET}$	$\overline{CLEAR}$	J	K	CLK	Qt	Qt'
1	1	0	0	↓	Q_0	Q_0'
		0	1	↓	0	1
		1	0	↓	1	0
		1	1	↓	TOGGLE	TOGGLE

JK FF Excitation Table:

PRESENT	**NEXT**	**J**	**K**
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

X – DON'T CARE
Q_O – The Q level before transition

JK FF Input Function table

OUTPUT						**INPUT**					
PRESENT STATE			**NEXT STATE**			**C**		**B**		**A**	
C	**B**	**A**	**C**	**B**	**A**	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	1	0	0	1	X	0	X	0	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	0	1	0	0	1	X	X	1	0	X

0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	1	X	0	1	X	X	0
1	1	0	1	0	0	X	0	X	1	0	X
1	1	1	0	0	1	X	1	X	1	X	0

K- Map

	$\overline{A}$	A
$\overline{C}\overline{B}$	1	0
$\overline{C}B$	1	1
CB	X	X
$C\overline{B}$	X	X

$J_C = A' + B$

	$\overline{A}$	A
$\overline{C}\overline{B}$	X	X
$\overline{C}B$	X	X
CB	0	1
$C\overline{B}$	0	0

$K_C = AB$

	$\overline{A}$	A
$\overline{C}\overline{B}$	0	1
$\overline{C}B$	X	X
CB	X	X
$C\overline{B}$	0	1

$J_B = A$

	$\overline{A}$	A
$\overline{C}\overline{B}$	X	X
$\overline{C}B$	1	1
CB	1	1
$C\overline{B}$	X	X

$K_B = 1$

	$\overline{A}$	A
$\overline{C}\overline{B}$	0	X
$\overline{C}B$	0	X
CB	0	X
$C\overline{B}$	1	X

$J_A = CB'$

	$\overline{A}$	A
$\overline{C}\overline{B}$	X	0
$\overline{C}B$	X	1
CB	X	0
$C\overline{B}$	X	0

$K_A = C'B$

DRAW THE CIRCUIT