

# PDS0101 Introduction to Digital Systems

## **Tutorial 9**

#### **Tutorial outcomes**

By the end of today's tutorial, you should be able to

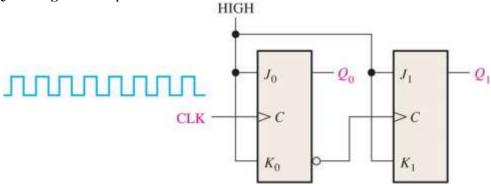
- differentiate between asynchronous and synchronous counters
- analyze counter circuits and determine their output
- determine modulus of a counter
- determine the sequence of a counter
- design a counter with arbitrary number of states

### Theory based questions

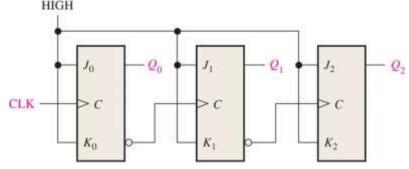
- 1. What is the difference between an asynchronous and synchronous counter?
- 2. Draw the logic circuit diagrams of a 3-bit asynchronous and 3-bit synchronous counter
- 3. Draw the timing diagrams of the outputs from both counters in question (2)
- 4. How many states would a modulus-15 counter have? What is the minimum number of FFs required to create this counter?
- 5. What is an asynchronous decade counter? Describe the characteristics.
- 6. Draw the logic circuit diagram of a asynchronous decade counter and draw is corresponding timing diagram from its outputs for one (1) cycle.

#### Applied knowledge based questions

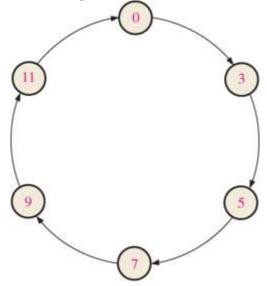
- 1. Show how an asynchronous counter with a modulus of 12 can be constructed using flip-flops
- 2. For the ripple counter shown below, show the complete timing diagram for the outputs at  $Q_0$  and  $Q_1$  for eight clock pulses



3. For the counter below, show the complete timing diagram for output waveforms at  $Q_0$ ,  $Q_1$  and  $Q_2$  for sixteen clock cycles.



- 4. Design a counter to produce the following cyclic sequence 00,10,01,11
- 5. Alter the counter from (4) so that it only implements the stages 11, 01 and 10 in cycle
- 6. Design a binary counter with the sequence shown in the state diagram below



7. Design a counter using J-K FFs that follow the cyclic sequence 4,5,7,1,3. Find the minimum number of FFs required to implement the counter and any unwanted FF sequences in the counter go to 4