MULTIMEDIA UNIVERSITY

PDS0101 Introduction to Digital Systems

Tutorial 6 SAMPLE SOLUTIONS

NOTE

Answers shown may be only one of many possibilities available. Please approach your tutor if you have an alternative answer of which you are not sure of. Any errors and omissions in the answers are deeply regretted.

Theory based questions

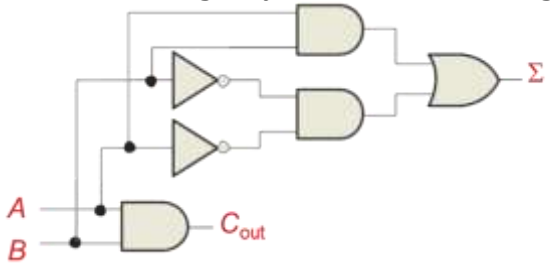
1. Perform the following to construct a half-adder logic circuit
   a) Complete the truth table below for 1-bit binary addition

Augend (A)	Addend (B)	Sum (Σ)	Carry out (C_{out})
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

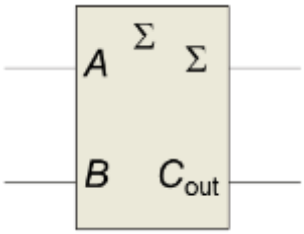
   b) Derive the boolean expressions (SOP) for Sum and carry out

   Sum, Σ = AB' + A'B = A⊕B
   Carry out, C_{out} = AB

   c) Combine the sum and carry out expressions and draw the final logic circuit for a half-adder using only AND, OR and NOT gates



   d) Draw the block diagram for the half-adder



2. Repeat the process above to construct a full-adder logic circuit
   a) Complete the truth table below for 1-bit binary addition

Augend (A)	Addend (B)	Carry in (C_{in})	Sum (Σ)	Carry out (C_{out})
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

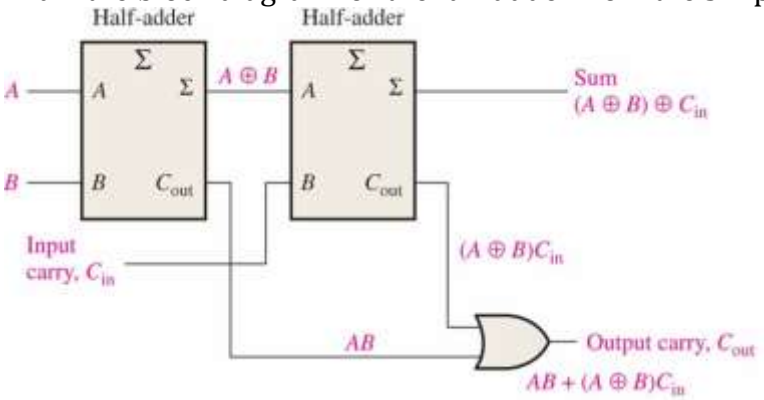
   b) Derive the boolean expressions (SOP) for Sum and carry out

Sum, Σ = $\overline{A}\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\overline{C_{in}} + ABC_{in}$
Carry out, C_{out} = $ABC_{in} + AB\overline{C_{in}} + A\overline{B}C_{in} + \overline{A}BC_{in}$

   c) Simplify the expressions in (b) using boolean algebra

Sum, Σ = $(A \oplus B) \oplus C_{in}$ <see notes>
Carry out, C_{out} = $AB + (A \oplus B)C_{in}$ <see notes>

   d) Draw the block diagram for the full-adder from the simplified expressions in (c)



3. Determine the output value for C_{out} and ∑ (Sum) of a full adder, if the inputs are as shown below
   a) A=1, B=0, Cin=0 — C_{out} = 0 ∑= 1
   b) A=0, B=0, Cin=1 — C_{out} = 0 ∑= 1
   c) A=0, B=1, Cin=1 — C_{out} = 1 ∑= 0
   d) A=1, B=1, Cin=1 — C_{out} = 1 ∑= 1

4. Determine the possible full-adder inputs that will produce the following outputs
   a) C_{out} = 0 ∑= 1 — A=1, B=0, Cin=0 or A=0, B=1, Cin=0 or A=0, B=0, Cin=1
   b) C_{out} = 0 ∑= 0 — A=0, B=0, Cin=0
   c) C_{out} = 1 ∑= 1 — A=1, B=1, Cin=1
   d) C_{out} = 1 ∑= 0 — A=1, B=1, Cin=0 or A=1, B=0, Cin=1 or A=0, B=1, Cin=1

5. For the parallel adders below, determine the complete sum by analysis of the logical operation of the circuit

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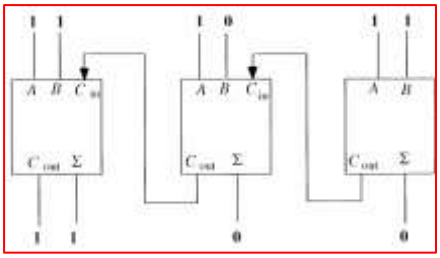
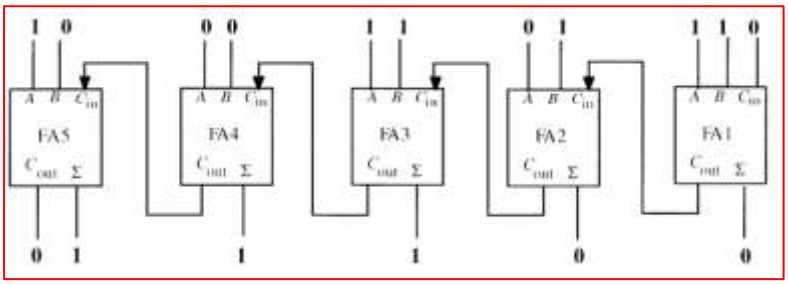
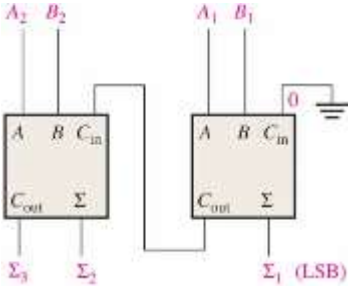
a)



b)

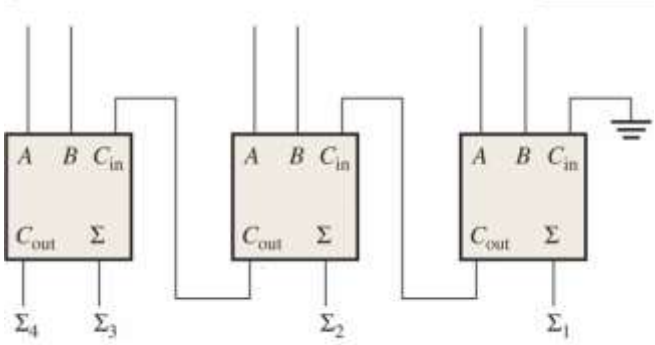


6. The input waveforms in the figure below are applied to the logic circuit shown. Determine the output waveforms in relation to the inputs by completing the timing diagram



please refer to sol 6b

7. Design a 3-bit parallel adder by using full adders only



8. When a HIGH output is detected on the output of the following decoder circuits, what is the binary code signal appearing on the inputs assuming that A_0 is LSB?

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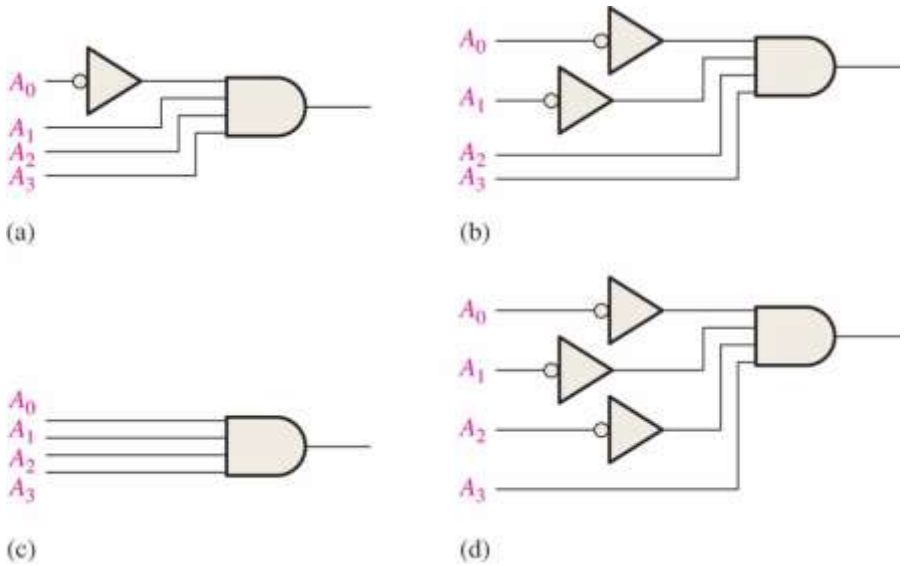
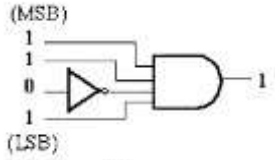
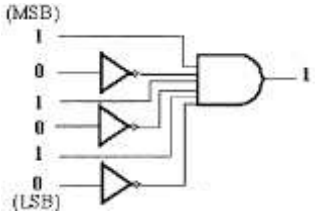
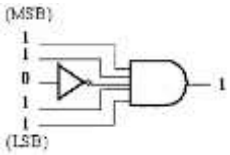
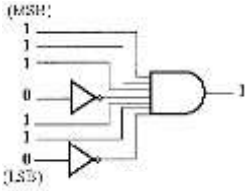


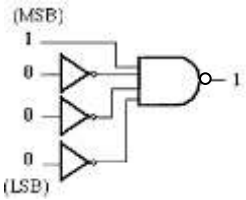
a) 1110 (assuming arrangement of bits is $A_3A_2A_1A_0$)
b) 1100
c) 1111
d) 1000

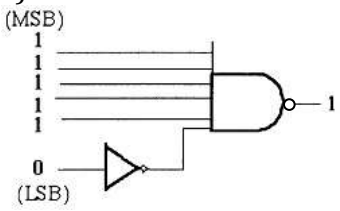
9. Show the decoding logic for the following codes if an active-HIGH output is required
   a) 1101
   

   b) 101010
   

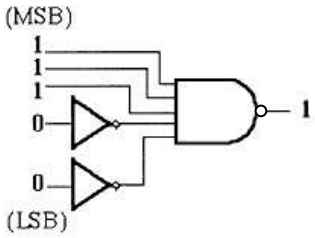
   c) 11011
   

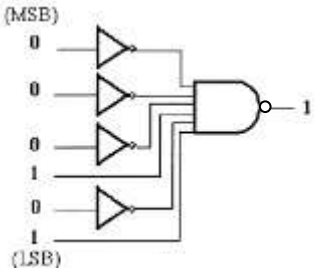
   d) 1110110
   

10. Show the decoding logic for the following codes if an active-LOW output is required
   a) 1000
   

   b) 11100
   c) 111110
   

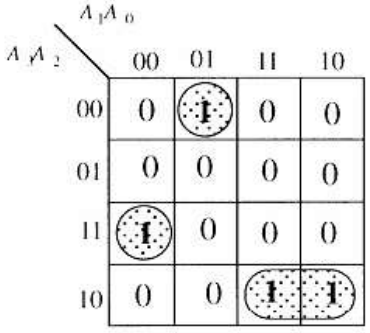
   d) 000101

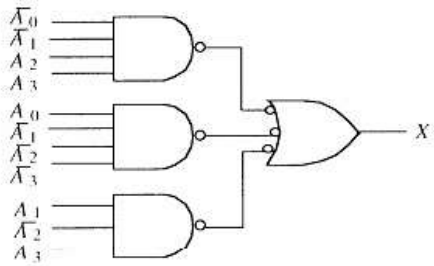




11. Design a decoder that detects the presence of the input binary codes of 1010, 1100, 0001 and 1011. The active-HIGH output is required when the correct input is detected.

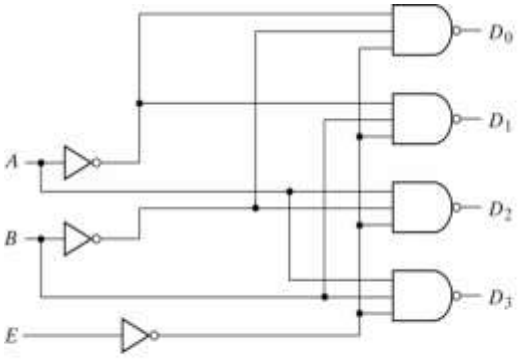
$$X = \overline{A_3}\,\overline{A_2}\,\overline{A_1}A_0 + A_3\overline{A_2}A_1\overline{A_0} + A_3A_2\overline{A_1}\,\overline{A_0} + A_3\overline{A_2}A_1A_0$$





Note that an answer without any boolean simplification is also correct but not optimum(always check question requirements to see if needed)

12. Design a 2-to-4-Line Decoder (with Enable input) and Active LOW output. Provide the circuit and truth table.



(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table