LAB A-05 (Week 5) Construction and Implementation of Combinational Logic Circuits

Objectives

a. To design and implement a priority encoder circuit.
b. To design and implement the higher order decoder using lower order decoder ICs.
c. To design a given arithmetic circuit
d. To design the combinational logic circuit with the given Boolean expression using a suitableMUX/ decoder
e. To design the given code converter circuits.

Tasks

1. Design a **3 input priority encoder circuit**. The inputs are a3a2a1, with a3 having the lowest priority and a1 the highest. The outputs are y2y1, indicating the encoded highest-priority active input, and v, the valid output which indicates that at least one input is active. (Note: Priority input a3 is encoded as 11, a2 as 10 and a1 as 01)
   Perform the following:
   (i) Construct the truth table
   (ii) Simplify the Boolean expressions for ~~y1, y0~~, and v using Karnaugh map techniques.
   (iii) Draw the logic diagram with necessary basic logic gates.
   (iv) Verify your design experimentally

2. Design and construct a **3 to 8 decoder circuit using 2-line-to-4-line decoder** and also other logic gates needed.
   Perform the following:
   - Form the truth table for higher order decoder (3 to 8 decoder)
   - Design higher order decoder using the given lower order decoder.
   - Draw the logic diagram for higher order decoder using two lower order decoders
   - Verify the truth table of 3 to 8 decoder (higher order decoder) by implementing the logic diagram with lower order decoder (2 to 4 decoder) and other necessary logic gate(s).

3. Design a **full subtractor circuit** using
   (i) Two half subtractors.
   (ii) Using only NAND gates
   (iii) Using Only NOR gates.

4. Implement the following Boolean expression
   F(W, X, Y, Z) = ∑ m (1, 2, 4, 6, 7,9,11,14,15)
   (i) Using 8×1 MUX and the needed logic gates
   (ii) Using 16 ×1 MUX and the needed logic gates.
   (iii) Using a suitable decoder and an OR gate.

5. Design code converter circuits for the following problems:
   (i) 3-bit Gray-to- binary code converter
   (ii) 3-bit Binary-to-Gray code converter
   (iii) (8 4 -2 -1) $_{BCD}$ code to (Excess 3) $_{BCD}$ code converter

For the above design problems
- Construct the truth table
- Simplify the Boolean expressions using K-map/Boolean Algebra techniques
- Draw the logic diagram

Report Format

- Objectives
- Question 1 to 5
  - Problem Statement
  - Answer by following the subdivisions given in each question
- Conclusion

Assessment:

Total marks = 20/10=2%

Construction/Connections of the Circuit and Result during lab session = Tutor to pick questions for students to do and submit via CircuitVerse = 10 marks,
Report =5 Questions × 2 marks = 10 marks

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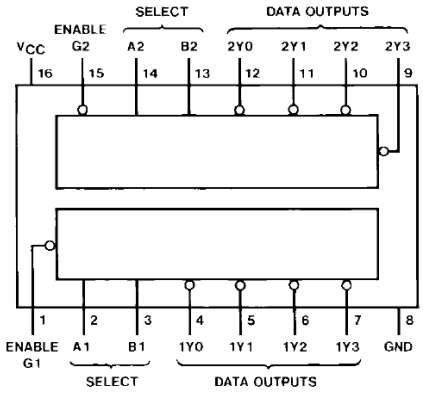

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Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Level
L = LOW Level
X = Don't Care

Note 1: G2 = G2A + G2B

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