References

Ryan Hou

2025-02-20

Table of contents

Preface

Notes on CMOS Integrated Circuits & VLSI.

Resources

Some relevant resources:

- EECS 312 - University of Michigan
- EECS 427 - University of Michigan
- CMOS VLSI Design Web Supplements
  - Contains supplemental materials e.g. lecture slides, figures, solutions, code, etc
- Digital VLSI Chip Design with Cadence and Synopsys CAD Tools
- VLSI Universe

Textbooks:

- J. Rabaey, A. Chandrakasan, and B. Nikolic. Digital Integrated Circuits A Design Perspective, Edition: 2. Alexandria, VA: Prentice Hall, 2003
- CMOS VLSI Design: A Circuits and Systems Perspective 4th Edition

1 Introduction

1.1 Perspective

> Note 1: Definition - Some definition
>
> **Term** is defined as blah blah blah...

This note does ...

1.2 High Level Ideas

2 Circuit Basics

A brief review of the fundamental concepts of electrical circuits that form the foundation for understanding CMOS and VLSI design.

2.1 Important Constants

Constant	Symbol	Value	Units
Elementary Charge	e	1.602×10^{-19}	C
Boltzmann Constant	k_B	1.380×10^{-23}	J/K
Room Temperature	T	300	K
Thermal Voltage at 300K	V_T	25.9	mV
Silicon Bandgap	E_g	1.12	eV
Permittivity of Free Space	ϵ_0	8.854×10^{-12}	F/m
Silicon Relative Permittivity	ϵ_r	11.7	-
Silicon Oxide Relative Permittivity	ϵ_{ox}	3.9	-

2.2 Common Unit Conversions

From	To	Conversion
eV	Joules	1 eV $= 1.602 \times 10^{-19}$ J
Temperature	Thermal Voltage	$V_T = \frac{k_B T}{q}$
Frequency	Time Period	$T = \frac{1}{f}$
Resistance $\times$ Capacitance	Time Constant	$\tau = RC$

2.3 Charge, Voltage, Current, Power

2.3.1 Charge (Q)

Electric charge is measured in Coulombs (C). The fundamental unit of charge is the electron charge:

$$Q_e = -1.602 \times 10^{-19} \text{ C}$$

The movement of charge carriers (typically electrons in circuits) creates current.

2.3.2 Voltage (V)

Voltage is the electric potential difference between two points, measured in Volts (V). Key equations:

$$V = IR \text{ (Ohm's Law)}$$

$$V = \frac{dW}{dQ} \text{ (Work per unit charge)}$$

2.3.3 Current (I)

Current is the rate of charge flow, measured in Amperes (A):

$$I = \frac{dQ}{dt}$$

For sinusoidal signals:

$$I = I_0 \sin(\omega t)$$

2.3.4 Power (P)

Power is the rate of energy transfer, measured in Watts (W):

$$P = VI \text{ (instantaneous)}$$
$$P = I^2R \text{ (resistive loss)}$$
$$P = CV^2f \text{ (dynamic CMOS)}$$
$$P_{avg} = \frac{1}{T}\int_0^T p(t)dt \text{ (average)}$$

2.4 Resistance, Capacitance, Inductance

2.4.1 Resistance (R)

Resistance is the property of a material that opposes the flow of electric current, resulting in the conversion of electrical energy to thermal energy.

Key equations:

$$V = IR \text{ (Ohm's Law)}$$
$$P = I^2R \text{ (power dissipation)}$$
$$R = \rho\frac{L}{A} \text{ (bulk resistance)}$$

where:

- ρ is resistivity
- L is length
- A is cross-sectional area

2.4.2 Capacitance (C)

Capacitance (measured in Farads F) is the ability of a component to store electric charge, measured as the ratio of stored charge to the applied voltage. Key equations:

$$Q = CV \text{ (charge stored)}$$
$$I_C = C\frac{dV}{dt} \text{ (capacitor current)}$$
$$\tau = RC \text{ (time constant)}$$

For parallel plate capacitors:

$$C = \frac{\epsilon_0 \epsilon_r A}{d}$$

where: - A is plate area - d is plate separation - ϵ_0 is permittivity of free space - ϵ_r is relative permittivity

2.4.3 Inductance (L)

Inductance (measured in Henries H) is the property of a circuit element to oppose changes in current flow by storing energy in a magnetic field:

$$V_L = L\frac{dI}{dt}$$
$$\tau_L = \frac{L}{R} \text{ (inductive time constant)}$$
$$E = \frac{1}{2}LI^2 \text{ (stored energy)}$$

2.5 Electric Fields

An electric field is a region of space surrounding a charged particle where another charged particle would experience a force, essentially acting like an invisible "push" or "pull" depending on the charges involved. It is the **force per unit charge** experienced by a small positive test charge placed at that point. Units: V/m or N/C

$$E = \frac{F}{q}$$

-
- electric field is the rate of change of voltage w.r.t. position

- strong electric field -> rapid change in voltage over short distance
- In circuits, voltage sources create electric fields that drive current flow

2.6 KVL & KCL

2.6.1 Kirchhoff's Voltage Law (KVL)

The sum of voltages around any closed loop equals zero:

$$\sum_{k=1}^{n} V_k = 0$$

2.6.2 Kirchhoff's Current Law (KCL)

The sum of currents entering a node equals the sum of currents leaving it:

$$\sum I_{in} = \sum I_{out}$$

$$\sum_{k=1}^{n} I_k = 0 \text{ (node equation)}$$

2.7 Basic Circuit Configurations

2.7.1 Series Connections

In series connections, components share the same current:

$$I_{total} = I_1 = I_2 = ... = I_n$$

For components in series:

- Resistors: $R_{total} = R_1 + R_2 + ... + R_n$
- Capacitors: $\frac{1}{C_{total}} = \frac{1}{C_1} + \frac{1}{C_2} + ... + \frac{1}{C_n}$
- Inductors: $L_{total} = L_1 + L_2 + ... + L_n$
- Voltage Division: $V_i = V_{total} \frac{R_i}{R_{total}}$

2.7.2 Parallel Connections

In parallel connections, components share the same voltage:

$$V_{total} = V_1 = V_2 = ... = V_n$$

For components in parallel:

- Resistors: $\frac{1}{R_{total}} = \frac{1}{R_1} + \frac{1}{R_2} + ... + \frac{1}{R_n}$
- Capacitors: $C_{total} = C_1 + C_2 + ... + C_n$
- Inductors: $\frac{1}{L_{total}} = \frac{1}{L_1} + \frac{1}{L_2} + ... + \frac{1}{L_n}$
- Current Division: $I_i = I_{total} \frac{R_{total}}{R_i}$

2.8 Capacitor

A capacitor stores eletrical energy in an electric field created between two conductive plates separated by an insulator (dialectric)

- When a voltage is applied, electrons build up on one plate (creating negative charge), and the other plate loses electrons (resulting in positive charge)
-

2.9 Additional Topics Relevant to CMOS/VLSI

2.9.1 Small Signal Analysis

Key parameters and equations:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{ (transconductance)}$$

$$r_o = \frac{\partial V_{DS}}{\partial I_D} \text{ (output resistance)}$$

$$A_v = -g_m r_o \text{ (small-signal gain)}$$

2.9.2 RC Networks

Time domain analysis:

$$v(t) = V(1 - e^{-t/RC}) \text{ (charging)}$$
$$v(t) = Ve^{-t/RC} \text{ (discharging)}$$
$$t_p \approx 0.69RC \text{ (propagation delay)}$$

2.9.3 Noise and Signal Integrity

Thermal noise power spectral density:

$$S_v(f) = 4k_BTR \text{ (V}^2\text{/Hz)}$$

Shot noise current spectral density:

$$S_i(f) = 2qI_D \text{ (A}^2\text{/Hz)}$$

Signal-to-Noise Ratio:

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{V_{signal,rms}^2}{V_{noise,rms}^2}$$

2.9.4 Semiconductor Physics Basics

Carrier concentration:

$$n_i^2 = N_C N_V e^{-E_g/k_BT}$$

Built-in potential:

$$V_{bi} = V_T \ln(\frac{N_A N_D}{n_i^2})$$

MOSFET threshold voltage:

$$V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{2\epsilon_s q N_A (2\phi_F)}}{C_{ox}}$$

where:

- V_{FB} is the flatband voltage
- ϕ_F is the Fermi potential
- N_A is acceptor concentration
- C_{ox} is oxide capacitance per unit area

2.10 PN Junctions

The PN junction is fundamental to semiconductor devices and CMOS operation. Key concepts and equations:

2.10.1 Built-in Potential

The built-in potential (V_{bi}) across the junction at equilibrium:

$V_{bi} = V_T \ln(\frac{N_A N_D}{n_i^2})$

where:

- N_A is acceptor concentration in p-region
- N_D is donor concentration in n-region
- n_i is intrinsic carrier concentration
- V_T is thermal voltage ($k_B T/q$)

2.10.2 Depletion Region

The depletion width (W) under bias:

$W = \sqrt{\frac{2\epsilon_s}{q}(\frac{N_A+N_D}{N_A N_D})(V_{bi} - V_A)}$

where:

- V_A is the applied voltage
- ϵ_s is semiconductor permittivity
- q is elementary charge

2.10.3 Current-Voltage Relationship

The ideal diode equation:

$I_D = I_S(e^{V_D/V_T} - 1)$

where:

- I_S is the reverse saturation current
- V_D is the diode voltage
- V_T is thermal voltage

The saturation current:

$I_S = qA(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p)$

where:

- D_p, D_n are diffusion coefficients
- L_p, L_n are diffusion lengths
- A is junction area

2.10.4 Junction Capacitance

The junction capacitance has two components:

Depletion capacitance:

$C_j = \frac{C_{j0}}{\sqrt{1-V_D/V_{bi}}}$

Diffusion capacitance:

$C_d = \tau_T \frac{dI_D}{dV_D} = \tau_T \frac{I_D+I_S}{V_T}$

where:

- C_{j0} is zero-bias junction capacitance
- τ_T is transit time

2.10.5 Temperature Effects

Temperature dependence of key parameters:

$I_S(T) \propto T^3 e^{-E_g/k_B T}$

$V_{bi}(T) = V_{bi}(T_0) - \beta(T - T_0)$

where β is the temperature coefficient.

2.11 Note

> **Note on Temperature Dependencies**
>
> Many parameters in CMOS circuits have significant temperature dependencies. Key relationships include:
>
> - Mobility: $\mu(T) \propto T^{-3/2}$

- Threshold voltage: $V_{th}(T) = V_{th}(T_0) + \alpha(T - T_0)$
- Leakage current: $I_{leak} \propto T^2 e^{-E_g/2k_B T}$

3 High-level Overview

3.1 MOS Transistors

Silicon Lattice

PN Junction

NMOS PMOS

3.2 CMOS Logic

3.2.1 Pass Transistors, Transmission Gates

3.2.2 Tristates

3.2.3 Multiplexers

3.3 Sequential Circuits

3.3.1 Latches

3.3.2 Flip-Flops

3.4 Fabrication & Layout

3.4.1 Fabrication Process

3.4.2 Layout Design Rules

3.4.2.1 Gate Layout

3.4.2.2 Stick Diagrams

3.5 Design Partitioning

3.6 Architecture

3.7 Logic Design

3.8 Circuit Design

3.9 Physical Design

3.10 Design Verification

3.11 Fabrication, Packaging, and Testing

4 CMOS Basics

4.1 MOS Transistor Basics

4.1.1 Silicon Lattice

Silicon (Si)

- semiconductor, forms basic starting material
- A Group IV element -> forms covalent bonds with 4 adjacent atoms
  - with **pure silicon**, all valence electrons are in chemical bonds, thus a **poor conductor**
- Raise conductivity adding **dopants** into the lattice (adding impurities)
- Dopant from Group V (e.g. arsenic As) has 5 valence electrons
  - Replacing one silicon atom leads to the lattice having 4 bonds but 1 valence electron loosely bound (b in fig. below)
  - Free electron can carry current thus raising conductivity
  - This is an **n-type** semiconductor
    - Free **carriers** are **negatively charged electrons**
- Dopant from Group III (e.g. boron B) has 3 valence electrons
  - Similarly, boron atom can borrow electron from neighboring Si which is now short by one electron
    - This creates a **hole** (a missing electron)
    - hole acts as positive carrier
  - This is a **p-type** semiconductor (c in fig. below)
- Note that when current flows, electrons and holes move in **opposite directions**
  - Recall how electrons move opposite to direction of conventional current flow
    - Holes move in same direction as conventional current flow
    - in semiconductors, current can be carried by holes as well because both electrons and holes are primary charge carriers
      - This goes into band structure of semiconductors:

- Electrons occupy two main energy bands: **valence band** (lower energy) and **conduction band** (higher)
- When an electron gains enoug energy (eg through doping) it moves from valence to conduction band, leaving a hole in valence band
- p-type doping creates deficit of electrons in valence band (creating holes)

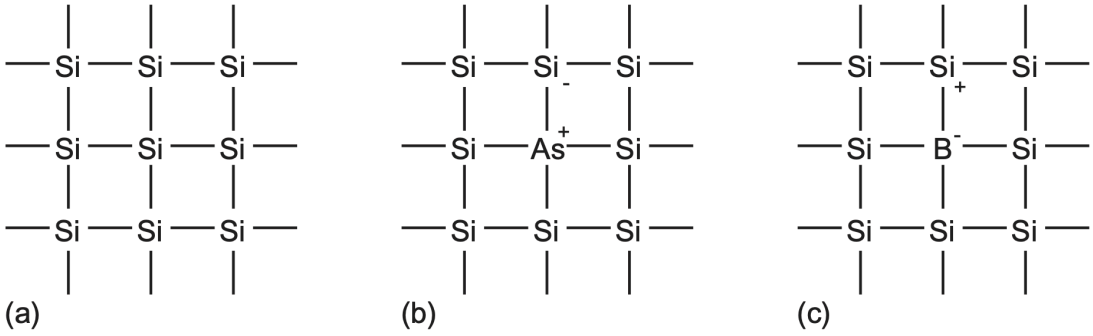


Figure 4.1: Silicon lattice shown as 2D plane for simplicity (but is actually 3D cubic crystal). Source: (Weste and Harris 2010)

4.1.2 PN Junction

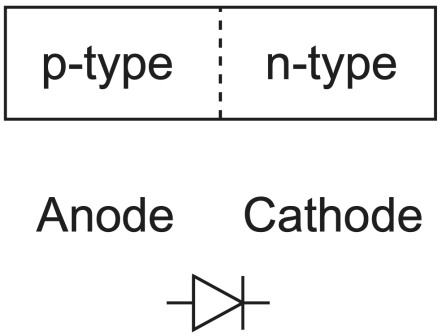


Figure 4.2: PN Junction. Source: (Weste and Harris 2010)

Junction between p-type (anode) and n-type (cathode) is a **diode**

- Voltage on p-type > n-type: diode is **forward biased** and current flows
- Otherwise (p-type $\leq$ n-type): diode is **reverse biased**, very little current flows

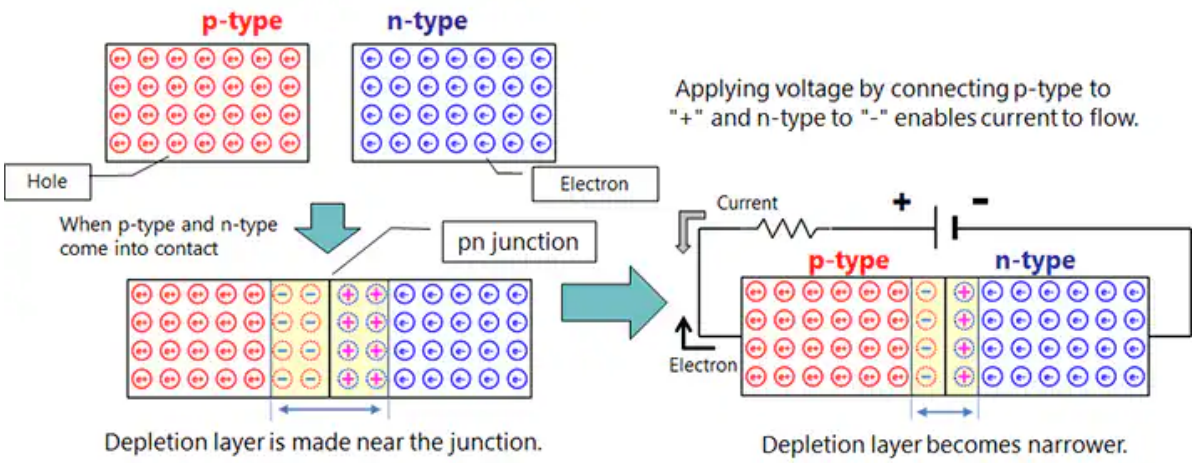


Figure 4.3: Source

- charge transfer (of electrons and holes) across the junction is called **diffusion**
- free electrons in the anode fills up some holes in the cathode
- this forms a **depletion layer**
  - depletion layer is depleted of any free carriers (electrons or holes)
    - in comparison on the n- and p-regions there are still free carriers
  - acts as a barrier to further current flow
- When applying **forward bias** (anode has higher voltage)
  - Positive voltage on p-type pushes holes towards junction
  - Negative voltage on n-type pushes electrons towards junction (where negative ions are repelling)
  - Shrinks depletion region
    - Once voltage is high enough, depletion region becomes so thin that electrons can freely pass (current flow)
- When applying **reverse bias** (anode has lower voltage)
  - Negative voltage on p-type pulls holes away from junction
  - Positive voltage on n-type pulls electrons away from junction
  - Makes depletion region wider
    - Creates stronger barrier to current flow

Analogy: A hill between two valleys. Forward bias reduces height of the hill, making it easy for charges to cross the hill. Reverse bias makes the hill taller, making it more difficult.

Why does the depletion region create a barrier? Why don't more electrons cross into p-type to fill up holes?

- When an electron fills a hole in the p-type
  - leaves behind positive ion on n-type (an atom lost its extra electron)
  - leaves behind a negative ion on the p-type (an atom has an extra electron)
- Thus depletion region becomes filled with positive ions on n-type side and negative ions on p-type side
  - Recall that ions are charged particles - (i.e. has more electrons than protons, or more protons than electrons)
- **Ions create an electric field**
  - (+) ions in the n-side and (-) ions in the p-side create an electric field pointing from n to p
    * electric field opposes the further flow of electrons
    * Think of like building static electricity: more charge separates, the stronger the opposing force becomes

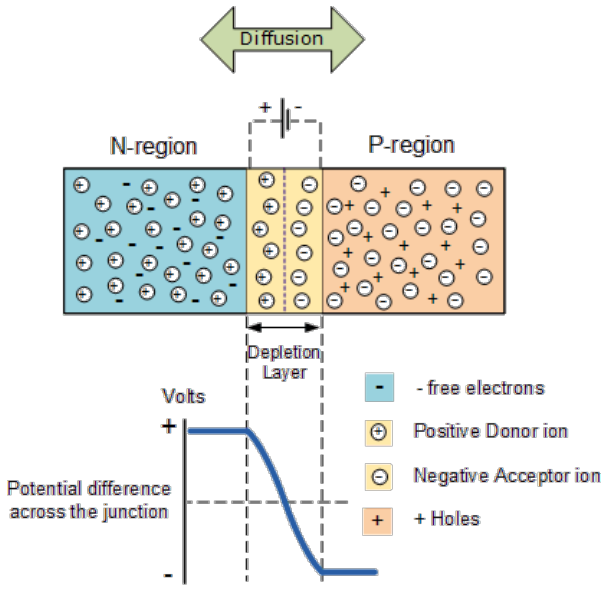


Figure 4.4: Source

4.1.3 Transistor Structure

Terminology clarifications:

- Metal-Oxide Semiconductor (MOS) - refers to the structure used in MOSFETs (ie consisting of the M, O, and S)

- Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) - the actual type of FET that uses MOS structure for a transistor
- Field-Effect Transistors (FET) - superset of MOSFET - transistors that control current using an electric field
  - Voltage-controlled device
  - Sometimes used interchangeably with MOSFET
- Complementary Metal-Oxide Semiconductor (CMOS) - refers to the technology that use both NMOS and PMOS (complementary)
  - Why CMOS?
    - In steady-state, only one type of transistor (N or PMOS) conducts
      - Thus no direct current path from supply to ground, leading to lower static power
      - i.e. power mainly comes from switching (although see further notes on static power)
    - Full rail-to-rail swing (0 to VDD) - good logic level separation
  - E.g. compared to pure NMOS logic, CMOS has lower static power dissipation and full voltage swing (but slower)

FET because transistor operation is controlled by electric fields (thus the *field effect* transistor)

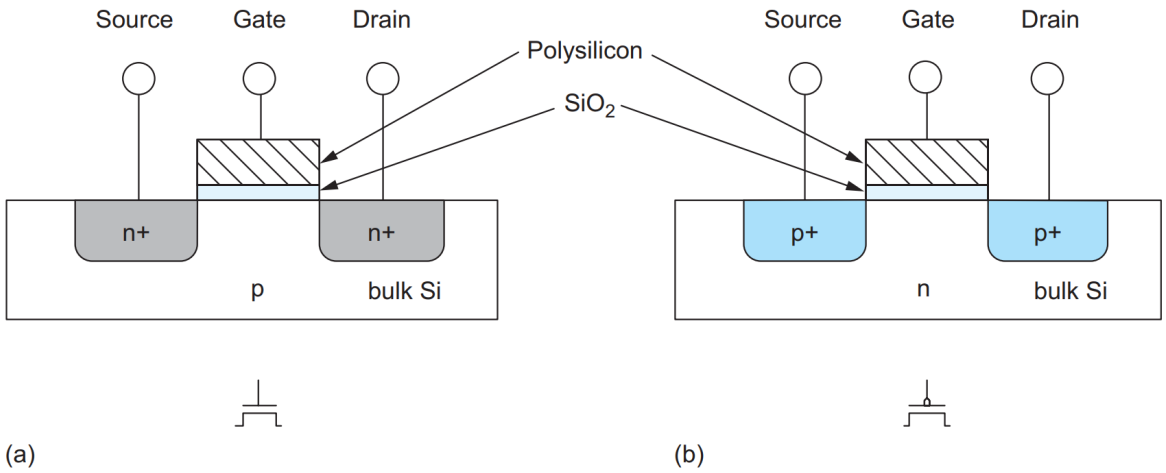


Figure 4.5: Cross-sections of a) nMOS, and b) pMOS. n+/p+ regions are heavily doped. Source: (Weste and Harris 2010)

CMOS technology provides two types of transistors/devices: **n-type transistor (nMOS)**, and **p-type transistor (pMOS)**

MOS Structure:

- **gate** - conducting gate
  - Early transistors: metal gates
  - 1970s and on: **polysilicon** (polycrystalline silicon)
  - metal gates have reemerged in '07
- **silicon dioxide** (SiO_2, glass)
  - Essentially works as the dialectric (insulator) between gate and semiconductor
- **substrate/body/bulk** - the silicon wafer
- NMOS is built with p-type body, with n-type semiconductor adjacent to the gate. These regions are the **source** and the **drain**. The body is typically grounded.
  - PMOS is opposite
- The substrate is either n-type or p-type, with the other flavor of transistor built in a special **well** to form the body of the opposite type
- **gate** is the control input - affecting flow of electrical current between source and drain

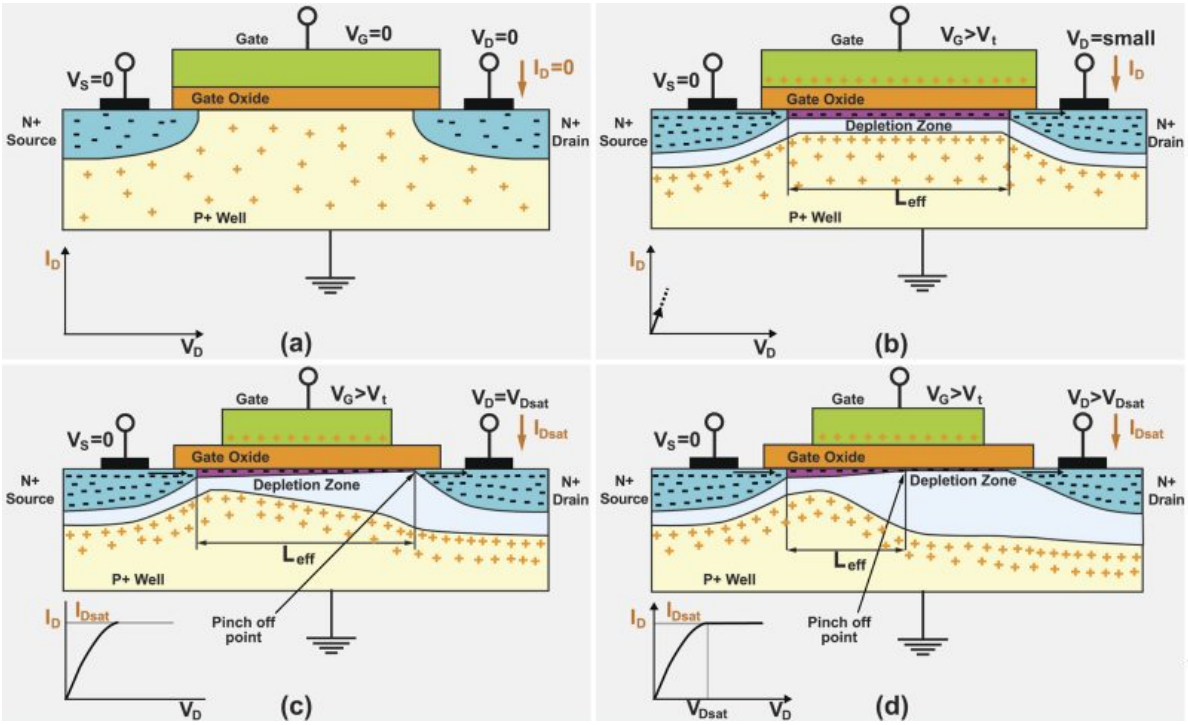


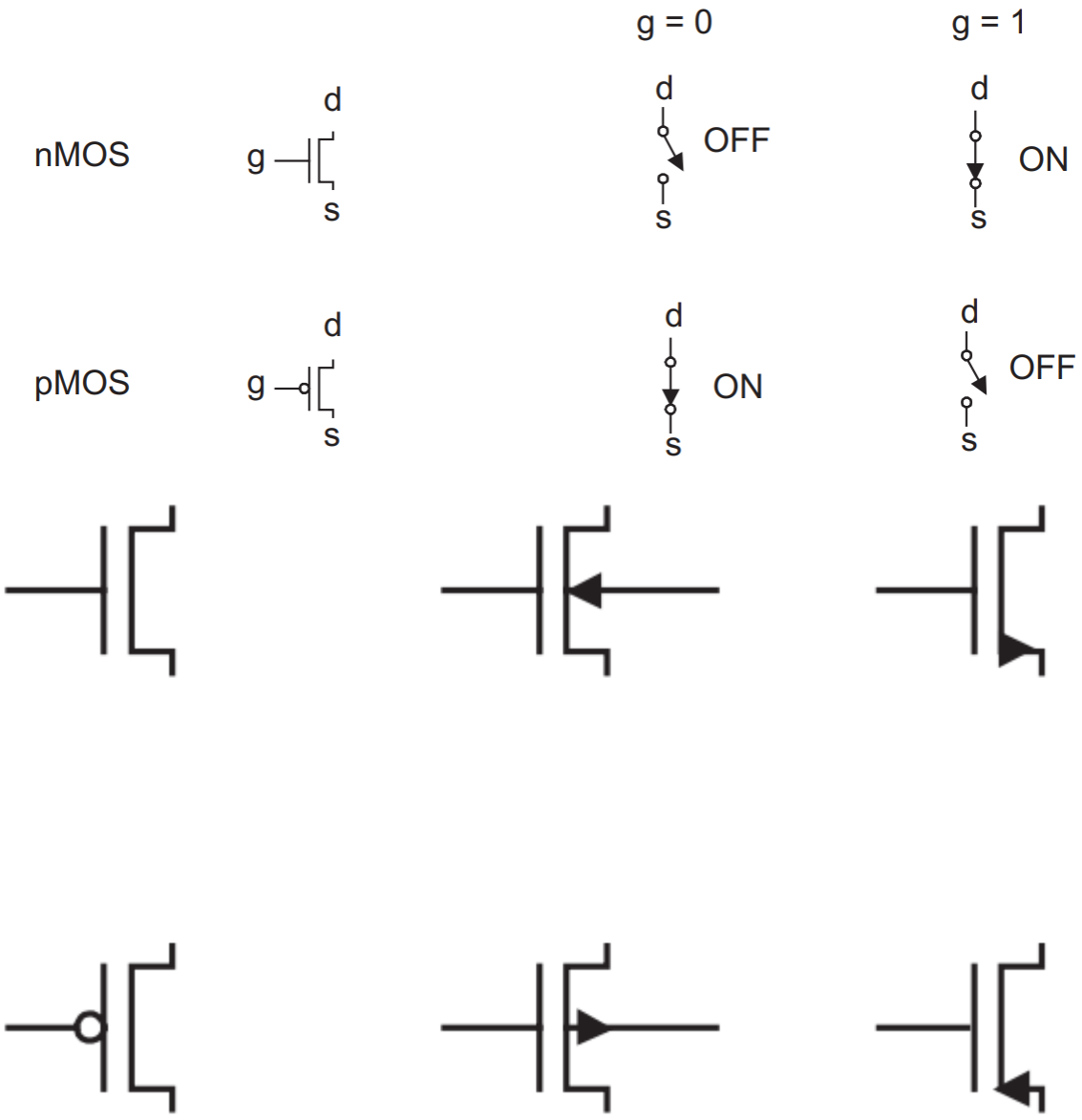
Figure 4.6: NMOS Operations. Source

NMOS:

- body is grounded (pn junction of source and drain to body is reverse-biased)
  - If gate is also grounded, no current can flow through the junctions since they are reverse-biased
    - Thus transistor is OFF
  - As gate voltage is raised, gate creates electric field that attracts free electrons
    - Why does raising gate voltage attract free electrons?
      - MOS structure essentially creates a parallel-plate capacitor (gate as a plate, and silicon beneath SiO_2 as a plate)
      - Gate voltage (potential difference) between the two plates create an electric field
      - Since SiO_2 is an insulator, charge cannot flow through it, thus inducing charge redistribution in the semiconductor
      - Positive gate voltage -> "capacitor" of gate and substrate forms electric field pointing downwards, pulling electrons upwards (positive potential of gate attracts them)
  - Once voltage is raised enough, electrons outnumber holes and creates a **channel**
    - **channel** is the thin region under the gate that becomes inverted to act as an n-type semiconductor
      - allowing conducting path of electron flow between source and drain
      - Thus transistor is ON

PMOS:

- Situation is opposite: body is at positive voltage
  - When gate is at positive voltage, source and drain junctions are reverse-biased -> no current flow
  - At lowered gate voltage, positive charges attracted towards the bottom of the SiO_2
    - Low enough gate voltage inverts the channel creating a conducting path for positive carriers from source to drain
- High voltage (Logic level 1) usually denoted V_{DD} or POWER
  - VDD for Voltage Drain Drain
- Low voltage (Logic level 0) called GROUND (GND) or denoted as V_{SS}
  - VSS for Voltage Source Source
- This allows MOSFETs to be viewed as ON/OFF switches



- The MOS transistor is a **majority-carrier** device - gate voltage controls current in a conducting channel between source and drain
  - NMOS: majority carriers are electrons
  - PMOS: majority carriers are holes
- Note that the source terminal sources the majority carrier which go to the drain
  - i.e. for nmos electrons go from source to drain, for pmos holes go

4.1.4 Very Simplified Model

The following demonstrates a very simplified MOS without the source and drain:

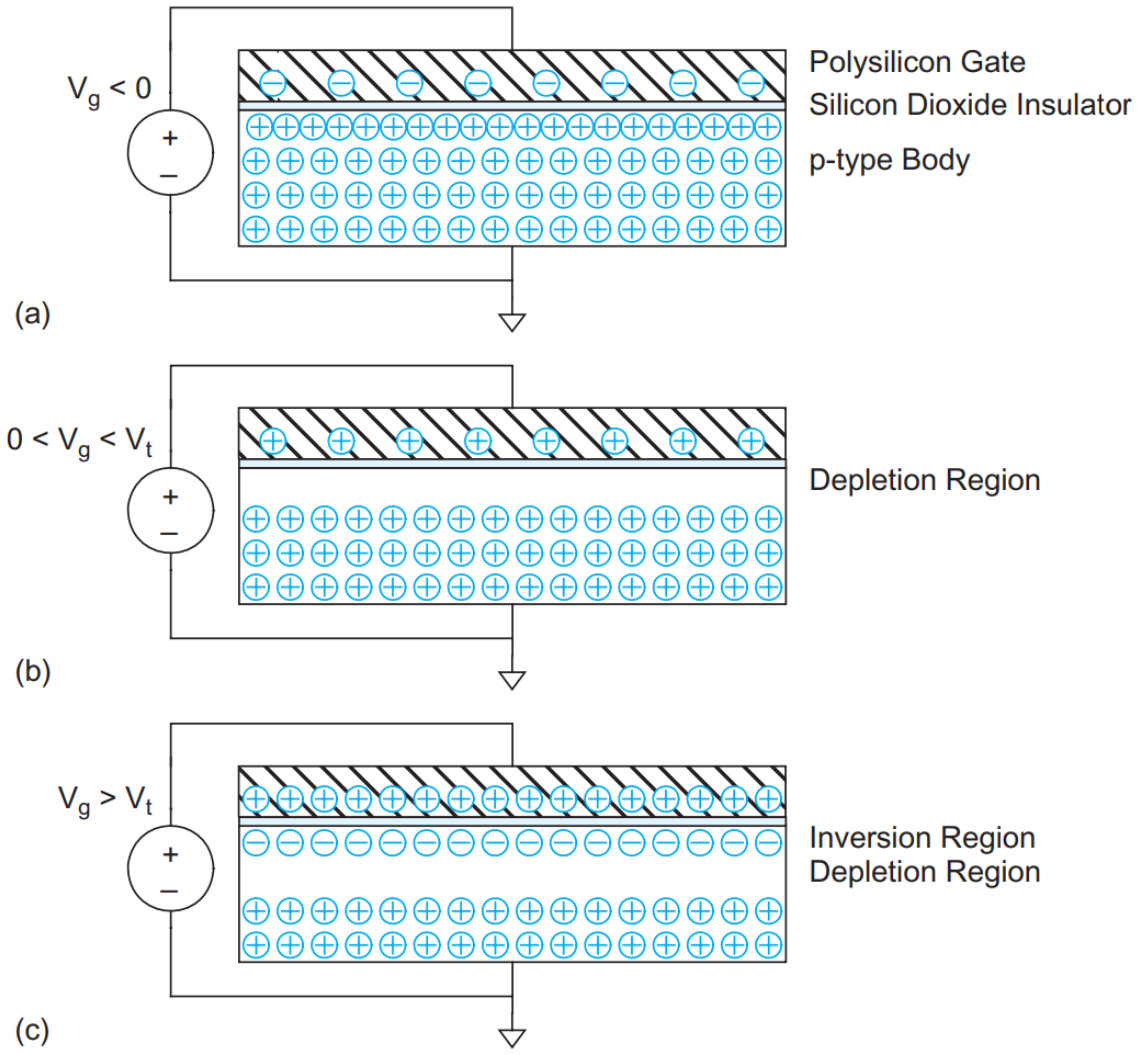


FIGURE 2.2 MOS structure demonstrating (a) accumulation, (b) depletion, and (c) inversion

Figure 4.7: Source:(Weste and Harris 2010)

- a) negative voltage on gate - holes attracted to region beneath the gate
- b) small positive voltage on gate - some positive charge on the gate, repelling the like holes below the gate

  - **depletion** region - region in the body where holes are repelled away

- c) higher positive potential larger than a threshold voltage V_t on gate - attracks a lot of positive charge to the gate, further repelling the holes and some free electrons in the body are attracted to the region beneath the gate
  - **inversion** layer - the conductive layer of electrons in the p-type body

Now let us examine an NMOS:

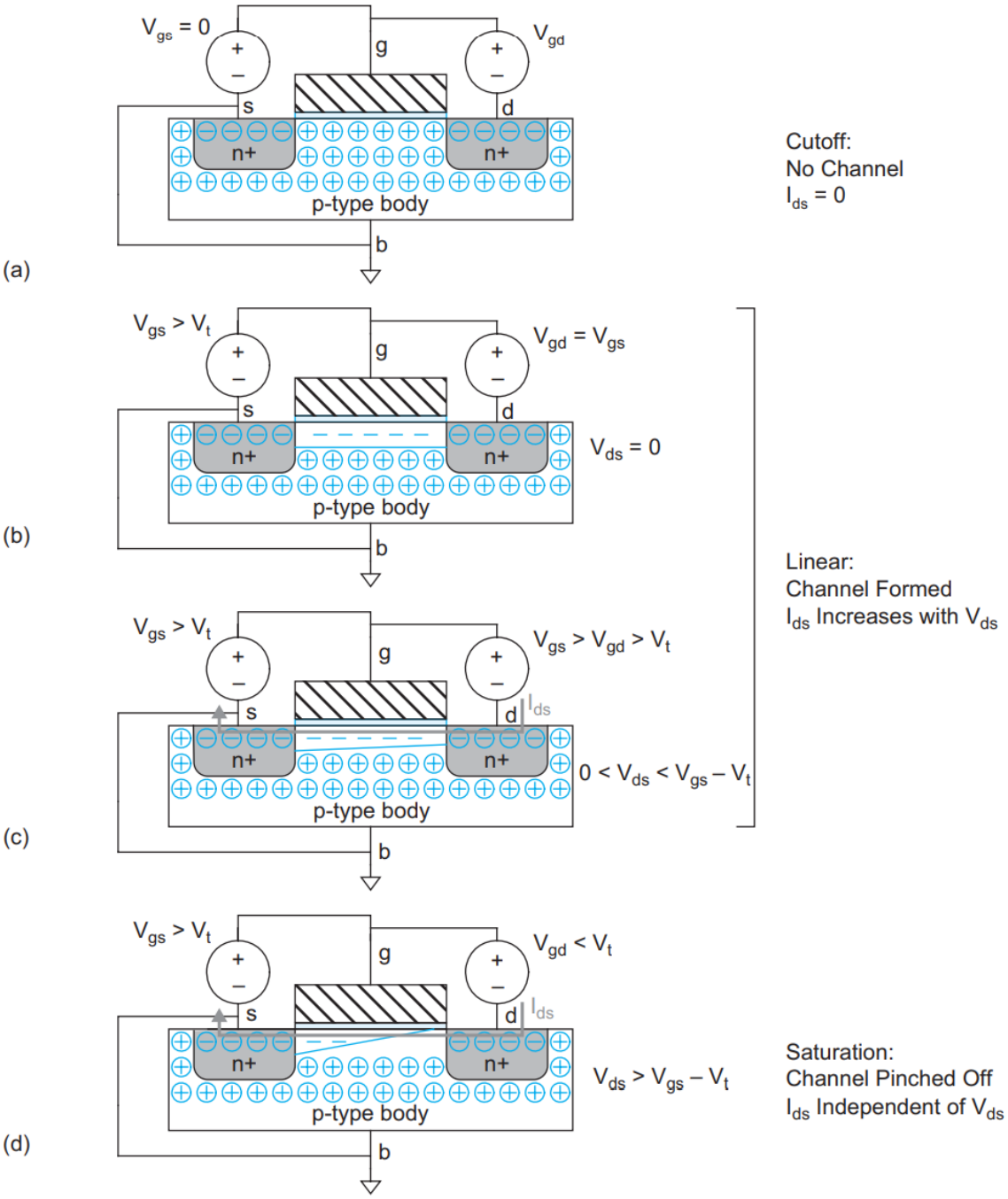


Figure 4.8: NMOS Regions of Operation: a) Cutoff region b, c) Linear region d) Saturation region Source:(Weste and Harris 2010)

Cutoff Region:

- $V_{gs} < V_t$
- Source and drain have free electrons, body has free holes but no free electrons
  - junction between body and source/drain are zero/reverse-biased, so little to no current flow
  - OFF
-

Linear Region:

- aka resistive, triode, nonsaturated, unsaturated, ohmic
- $V_{gs} > V_t$
  - but $0 < V_{ds} < V_{gs} - V_t$
- Inversion region of majority carriers (in this case electrons) - named the **channel** - creates a conductive path betwen source and drain
- ON
- Number of carriers and conductivity increases with gate voltage
- **Potential difference between drain and source**: $V_{ds} = V_{gs} - V_{gd}$
  - if V_{ds} is 0, no eletric field to push current from drain to source
- When small positive V_{ds} - current I_{ds} flows from drain to source
  - The current increases with both V_{ds} and V_{gs}

Saturation Region:

- V_{ds} is so large that $V_{gd} < V_t$
- channel is no longer inverted and is **pinched off**

Analogy: water valve

- Gate is the valve of a water pipe

4.2 Long-Channel I-V Characteristics

4.3 C-V Characteristics

4.4 Nonideal I-V Effects

4.5 DC Transfer Characteristics

4.6 Resources / References

Videos:

- CircuitBread - MOSFET
- CircuitBread - FET Regions of Operation

5 CMOS Fabrication & Process Technology

6 CMOS Capacitance

7 Inverters and More Gates

8 Delay

9 Power

10 Interconnect

11 Robustness

12 Circuit Simulation

13 Combinational Circuit Design

Ref (**cmosvlsi-4th?**)

14 Sequential Circuit Design

15 Datapath Subsystems

16 Array Subsystems

17 Special-Purpose Subsystems

18 Design Methodology and Tools

19 Testing, Debugging, and Verification

20 Summary

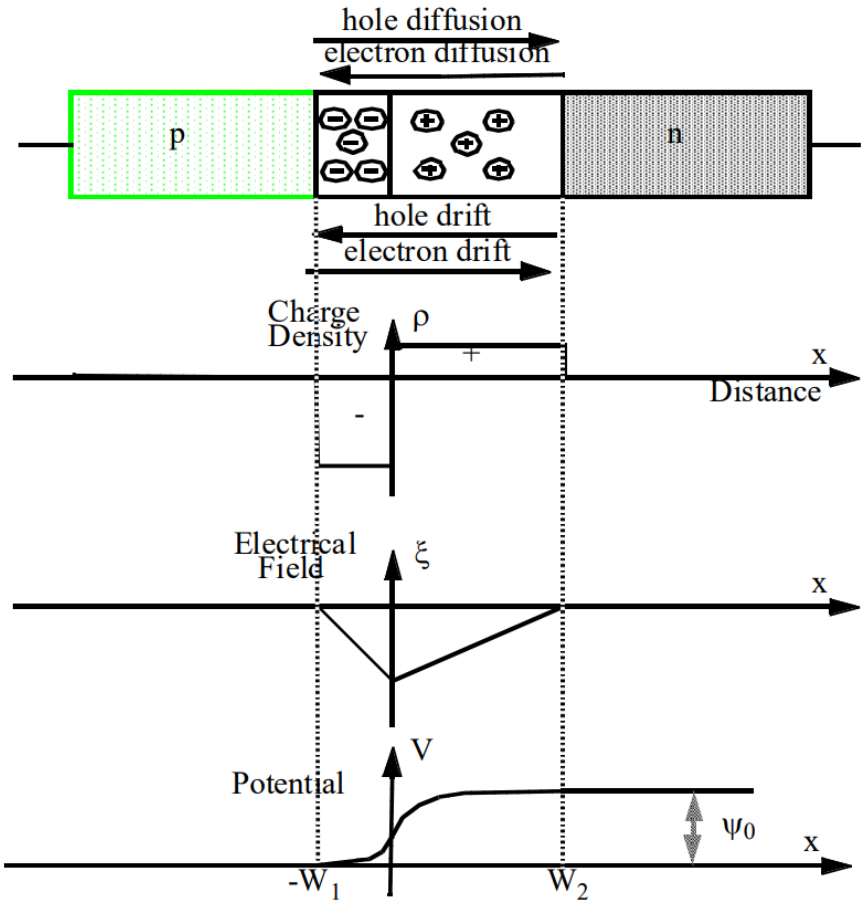
In summary...

20.1 Device: PN Junction and Diodes

For a PN Junction:

- Forward bias (voltage on P-side > N-side) shrinks depletion region - diode allows diffusion current - lowers Vt in a MOS
- Reverse bias (voltage on N-side > P-side) expands depletion region - diode has minimal current - raises Vt in a MOS

Depletion Region

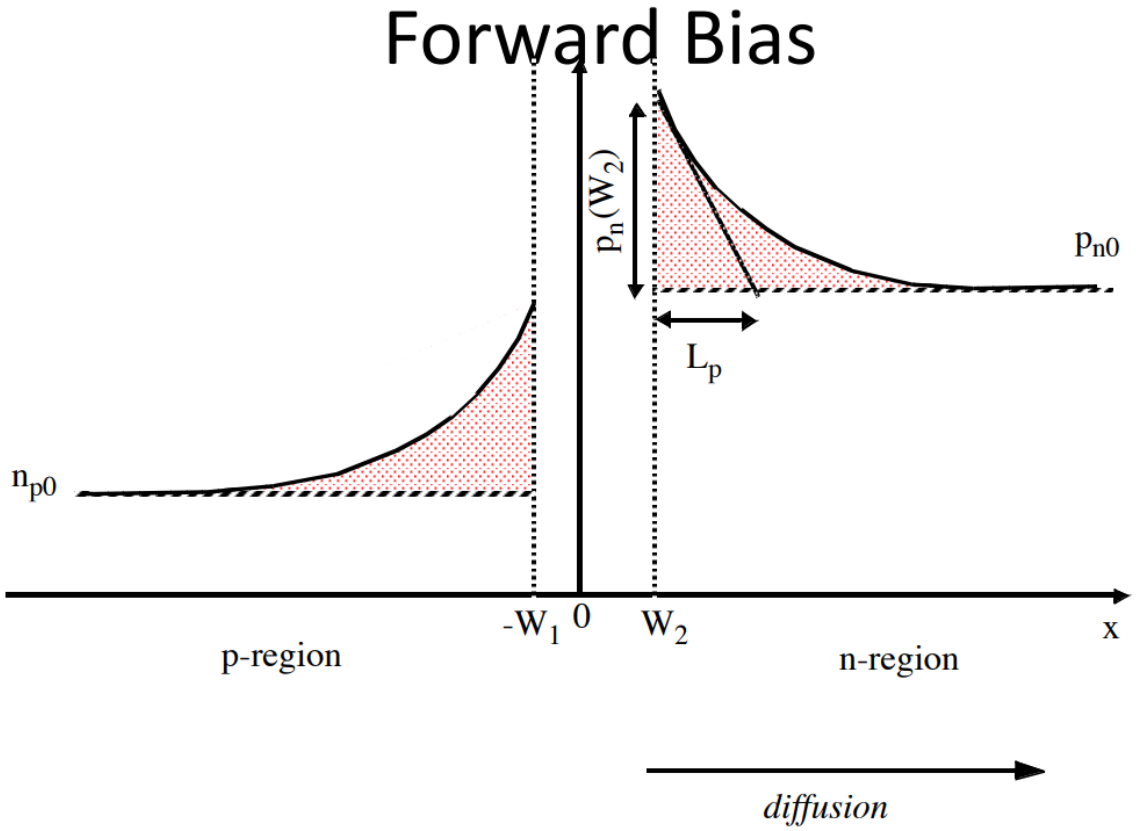


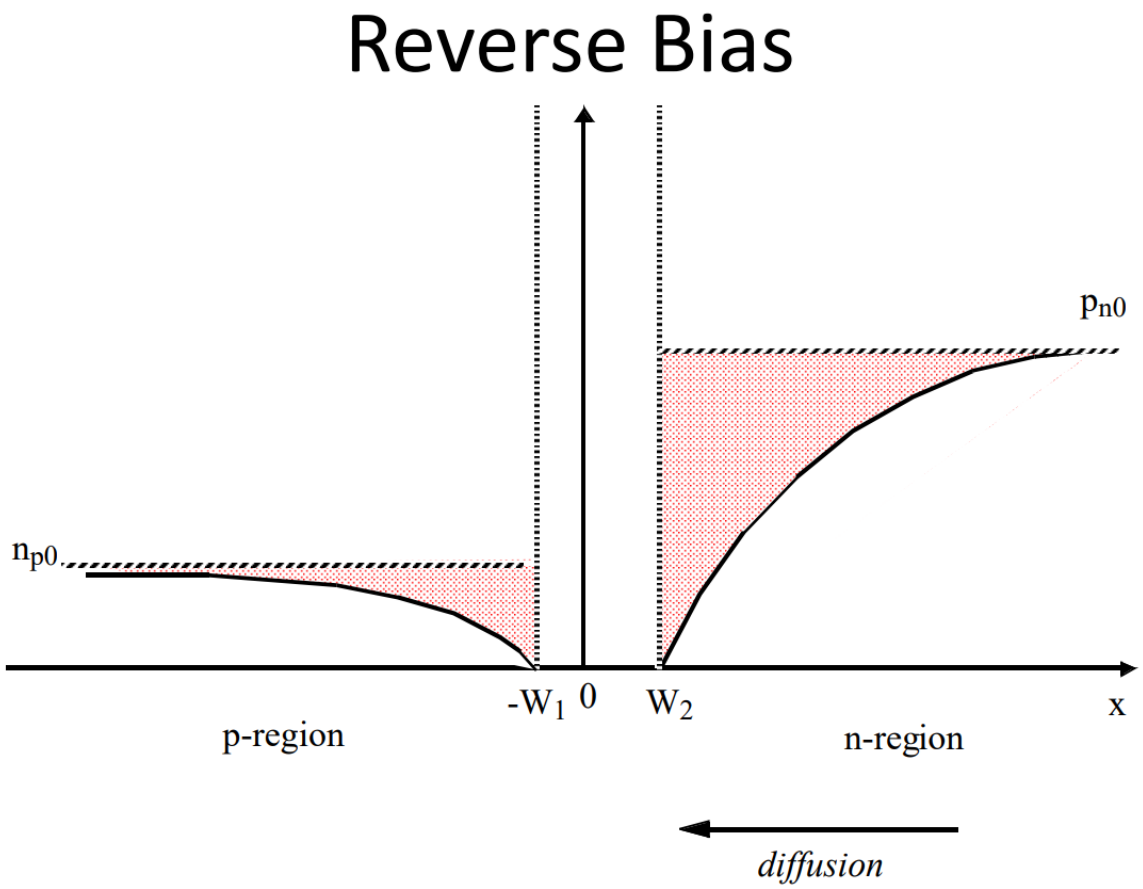
(a) Current flow.

(b) Charge densit

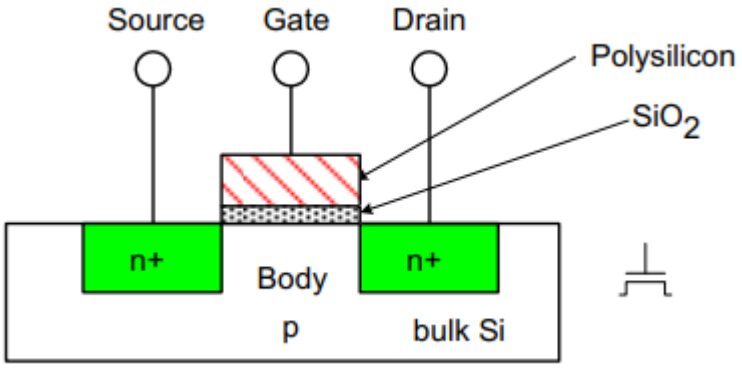
(c) Electric field.

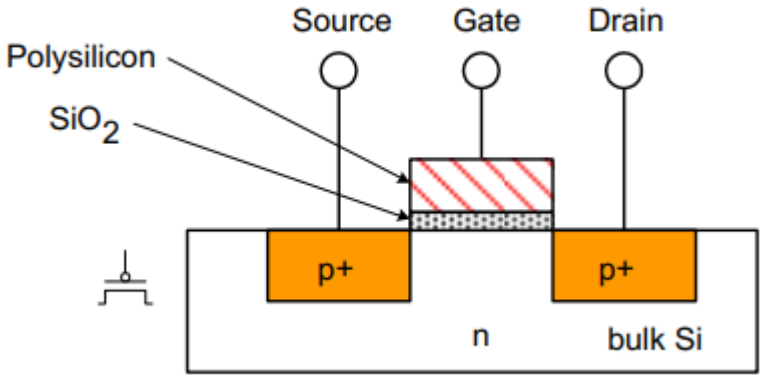
(d) Electrostatic potential.


Forward Bias
$p_n(W_2)$
p_{n0}
L_p
n_{p0}
$-W_1$
0
W_2
x
p-region
n-region
diffusion



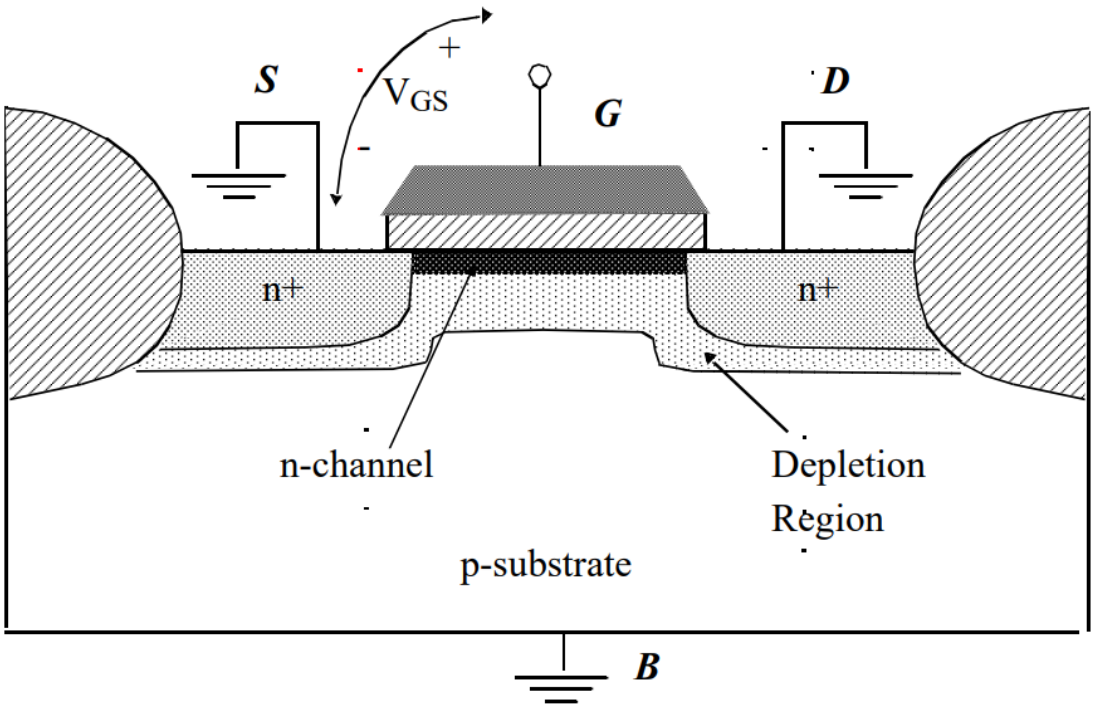
20.2 Device: MOS





Threshold Voltage

Threshold Voltage: Concept



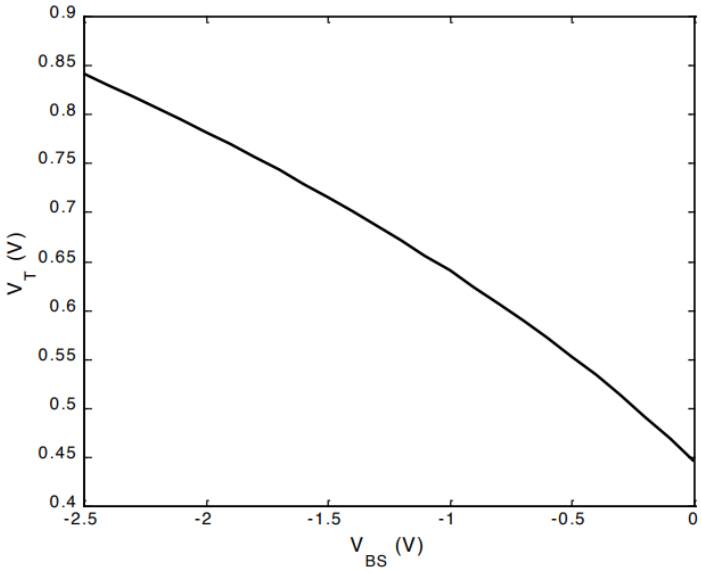
- $V_{GS} < 0$

- Accumulation of holes

- $0 < V_{GS} < V_T$
  - Depletion: repel mobile holes
  - Inversion: accumulation of electrons

- $V_{GS} > V_T$
  - Strong inversion: surface is as strongly n-type as the substrate is p-type

Body Effect



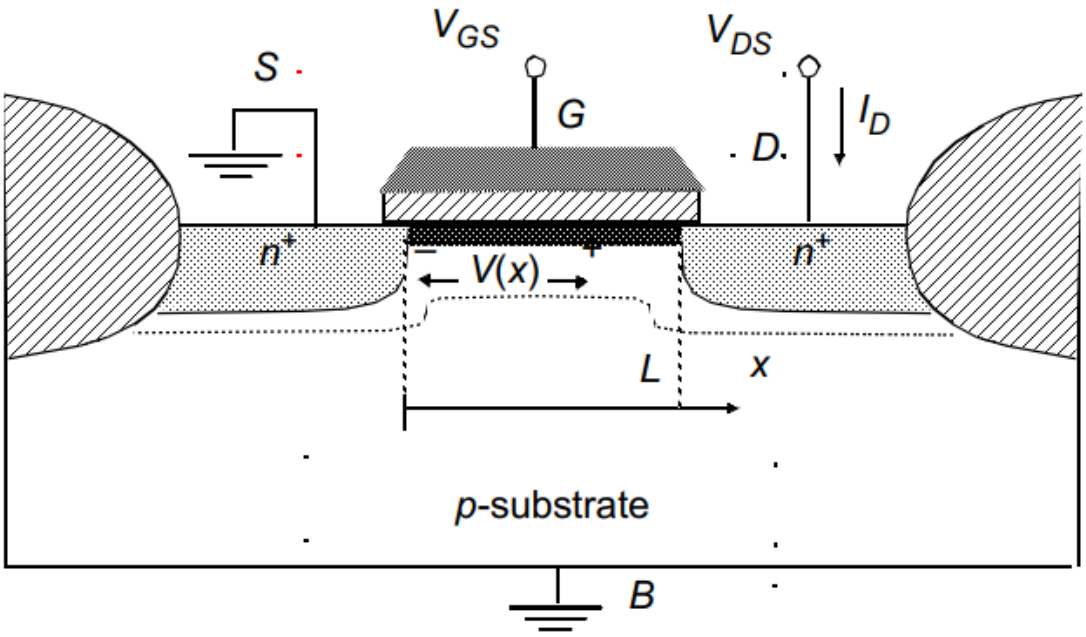
Typical parameters for NMOS:
ϕ_F = -0.3 V
γ = 0.4 $V^{0.5}$

Reverse bias NMOS:
Increase $V_{SB} > 0$, higher V_T

Forward bias NMOS:
Decrease $V_{SB} < 0$, lower V_T
Avoid turning on the PN junction

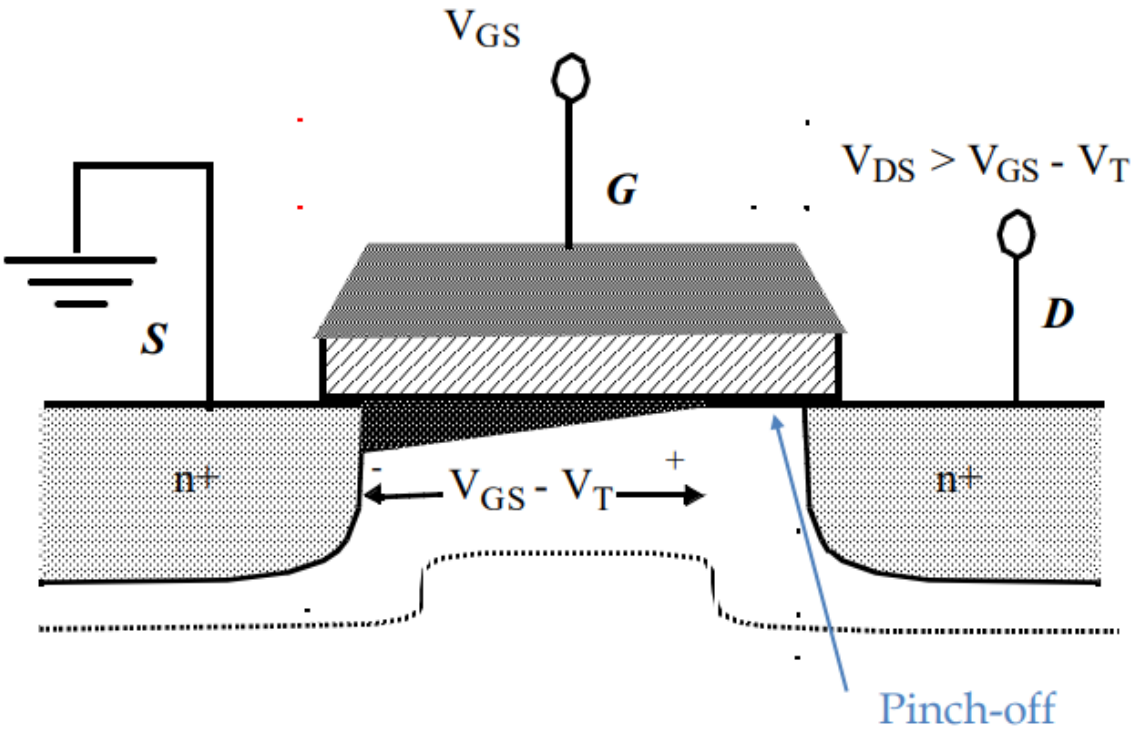
$$V_T = V_{T0} + \gamma(\sqrt{|(-2)\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|})$$

Transistor in Linear



MOS transistor and its bias conditions

Transistor in Saturation



Current-Voltage Relations Long-Channel Device

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

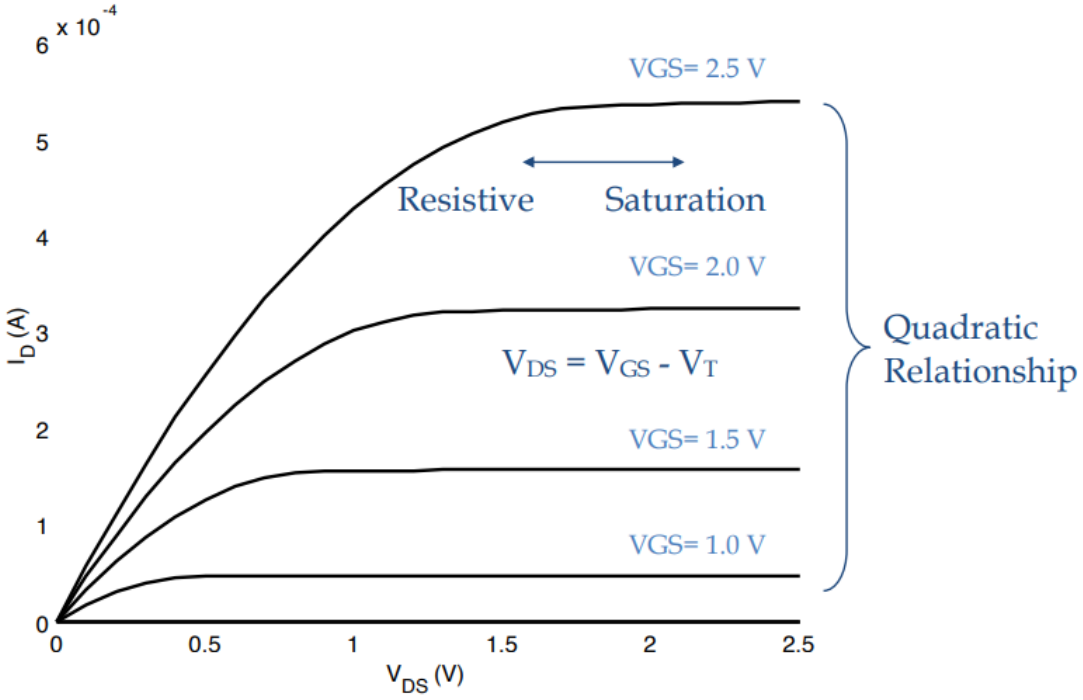
Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

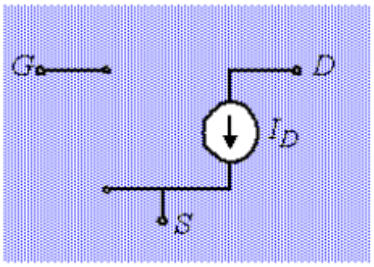
Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Current-Voltage Relations



A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

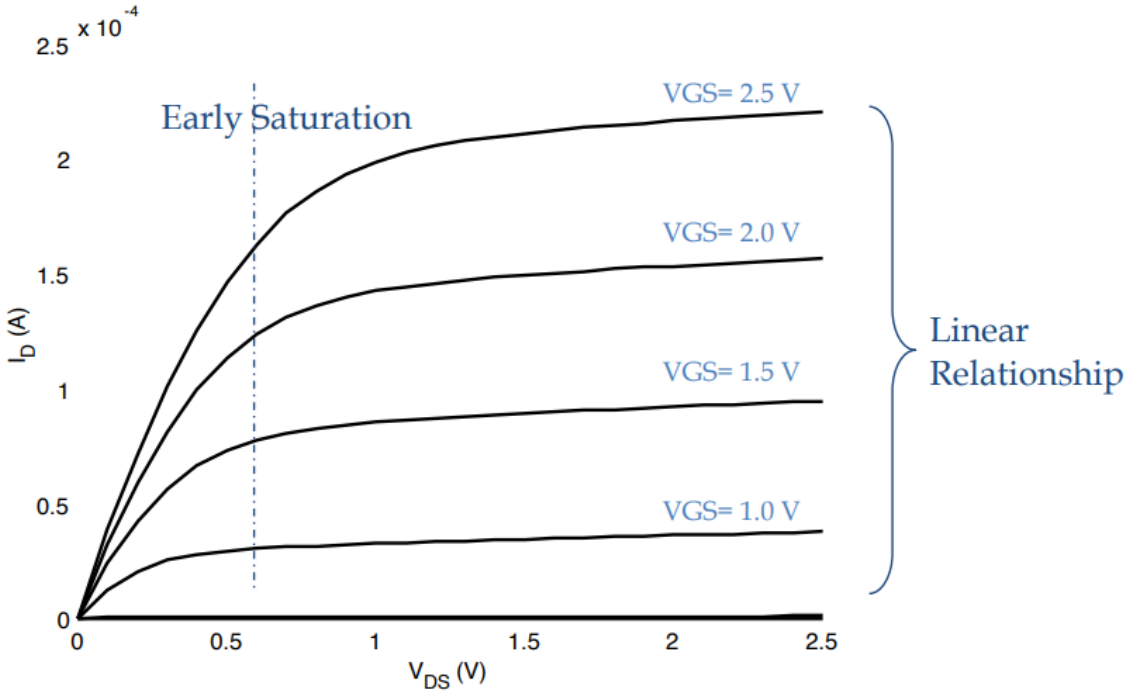
$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

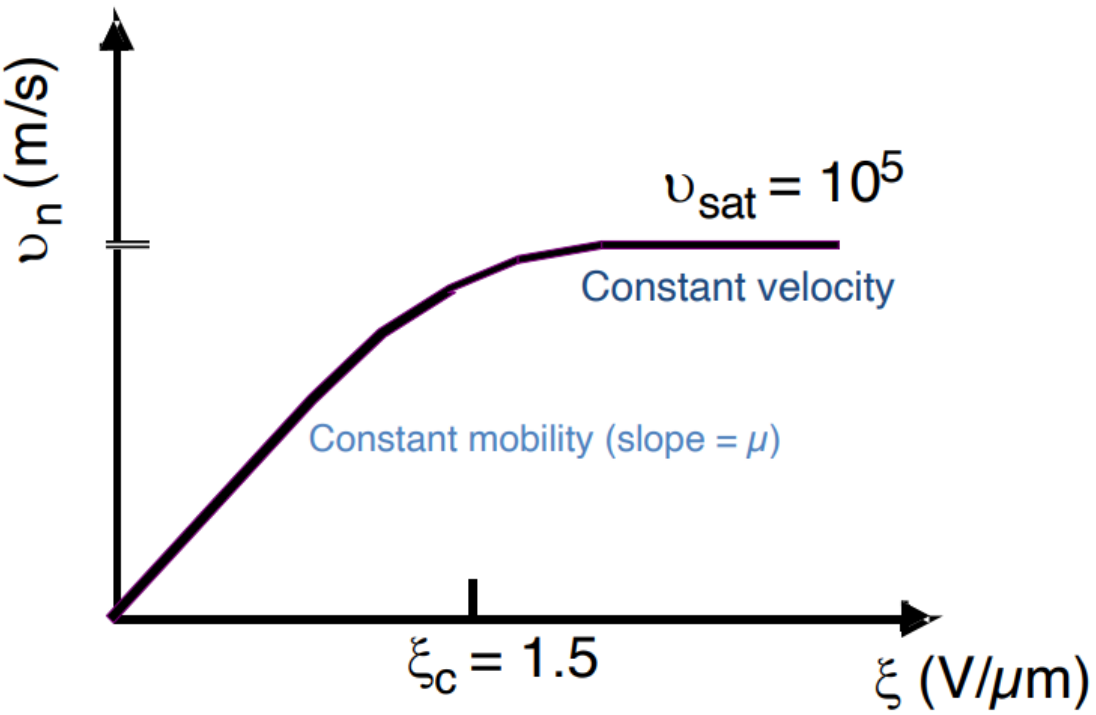
with

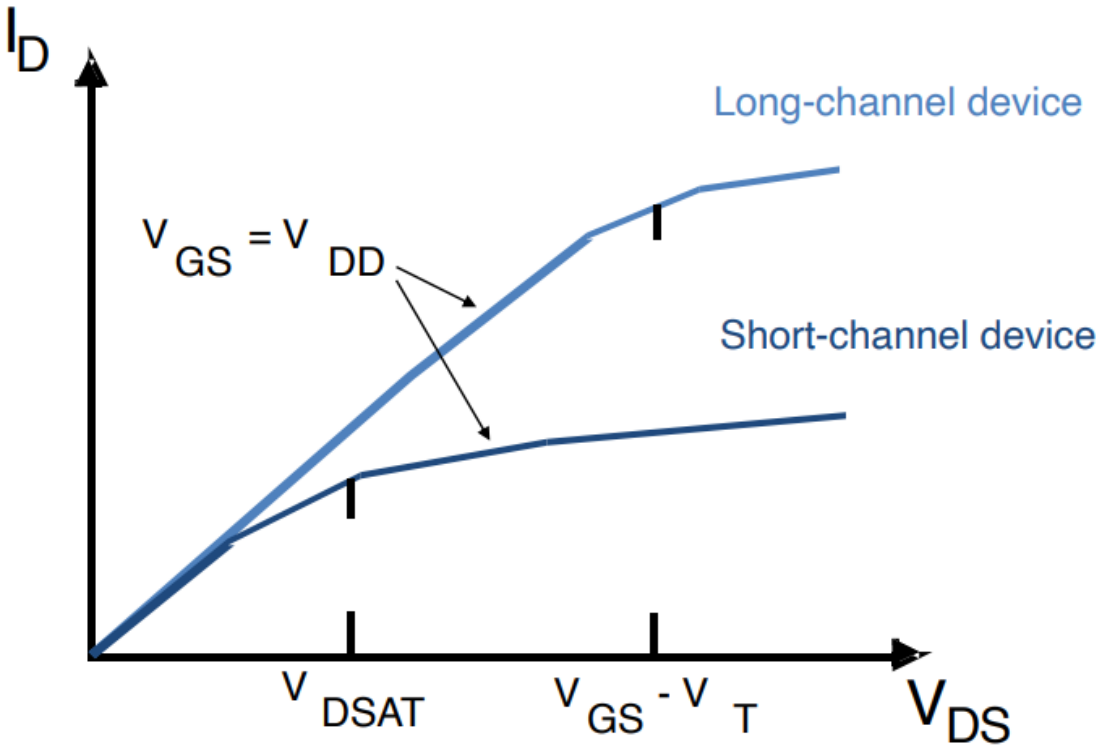
$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

Current-Voltage Relations
The Deep-Submicron Era

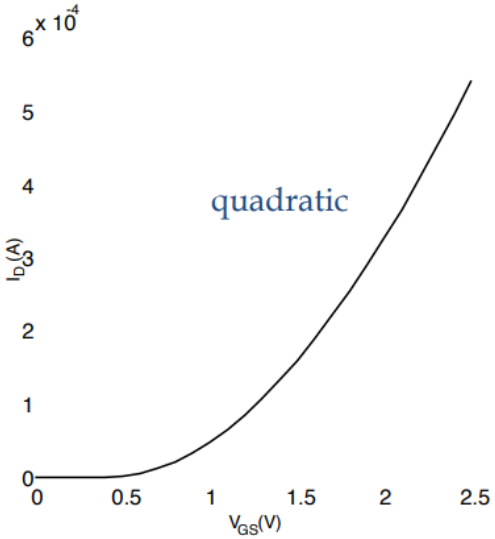


Velocity Saturation

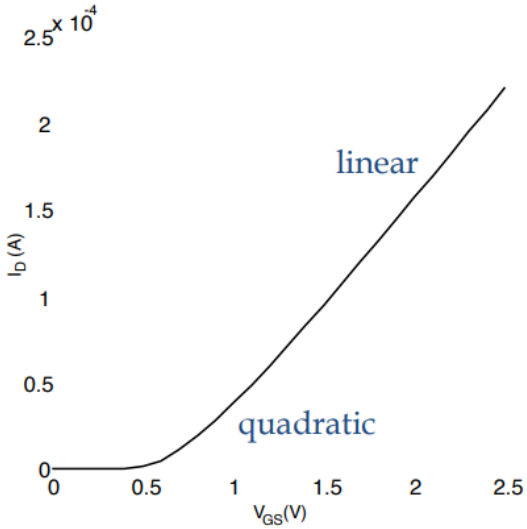



I D
Long-channel device
V GS = V DD
Short-channel device
V DSAT
V GS - V T
V DS

I_D versus V_{GS}

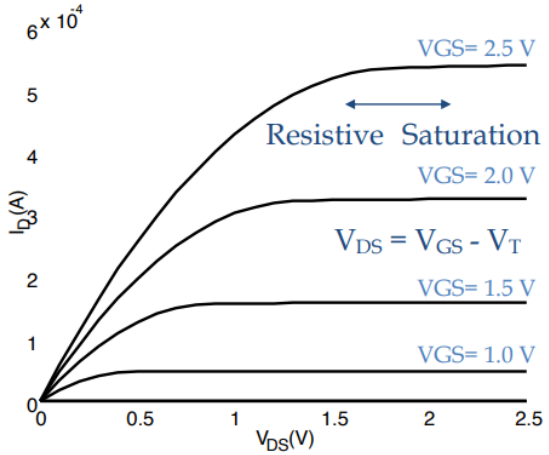


Long Channel

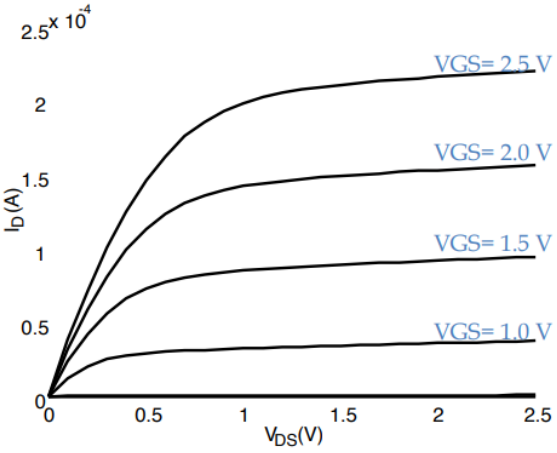


Short Channel

I_D versus V_{DS}

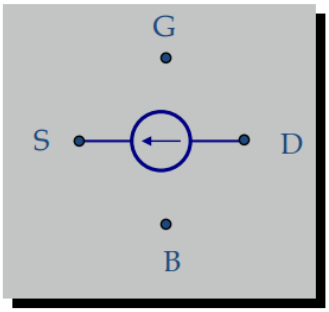


Long Channel



Short Channel

A unified model for manual analysis



$$I_D = 0 \text{ for } V_{GT} \le 0$$

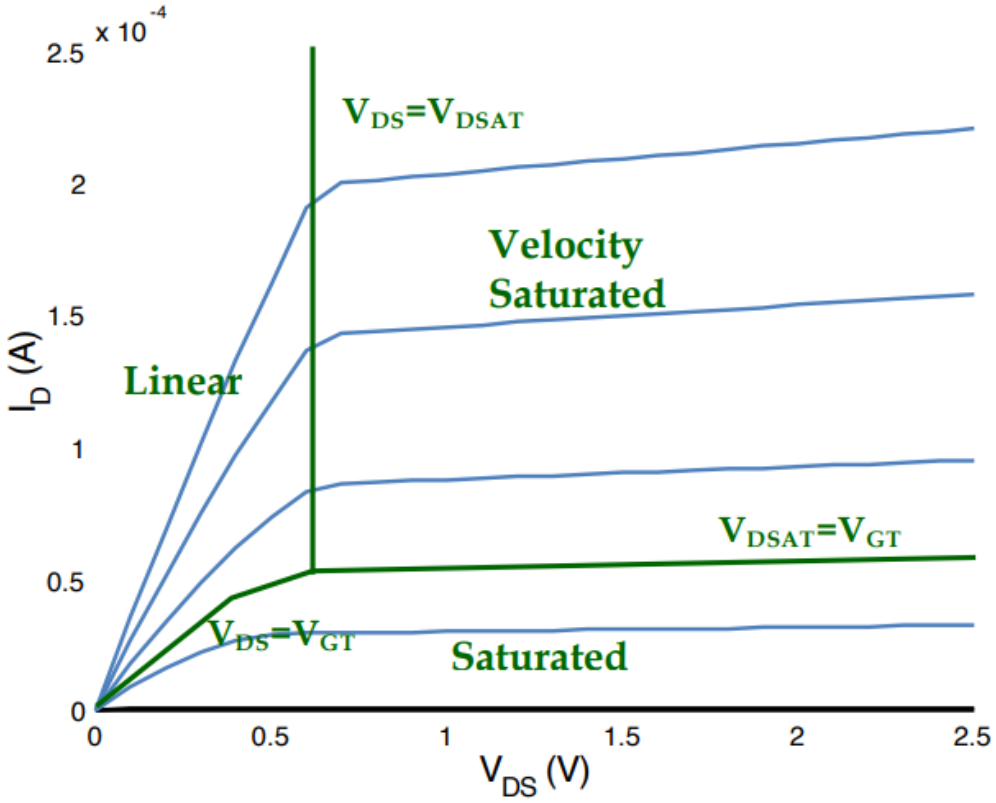
$$I_D = k' \frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

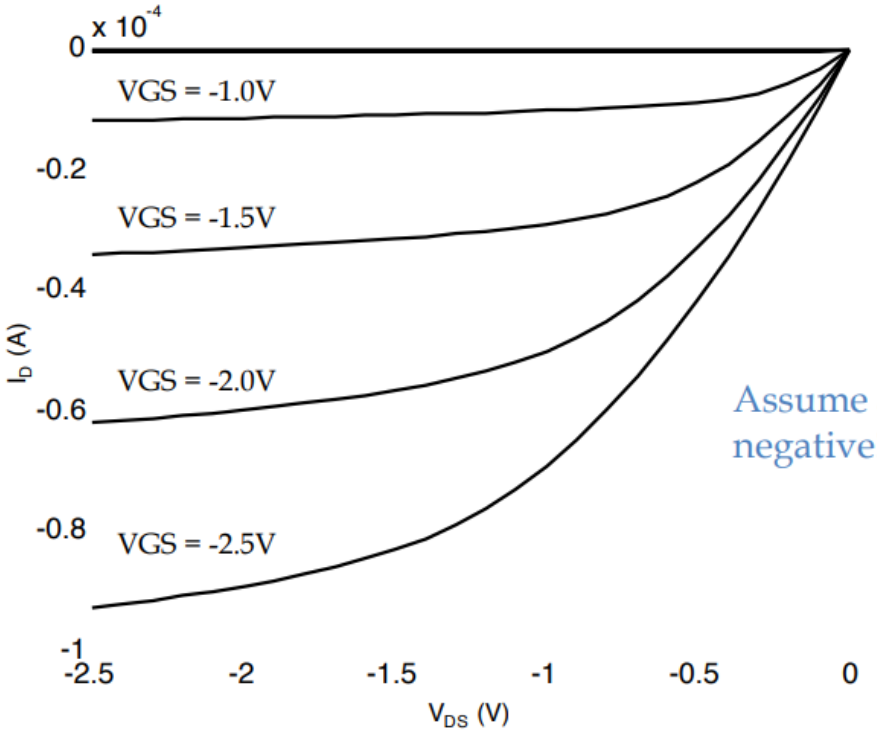
$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

Simple Model versus SPICE

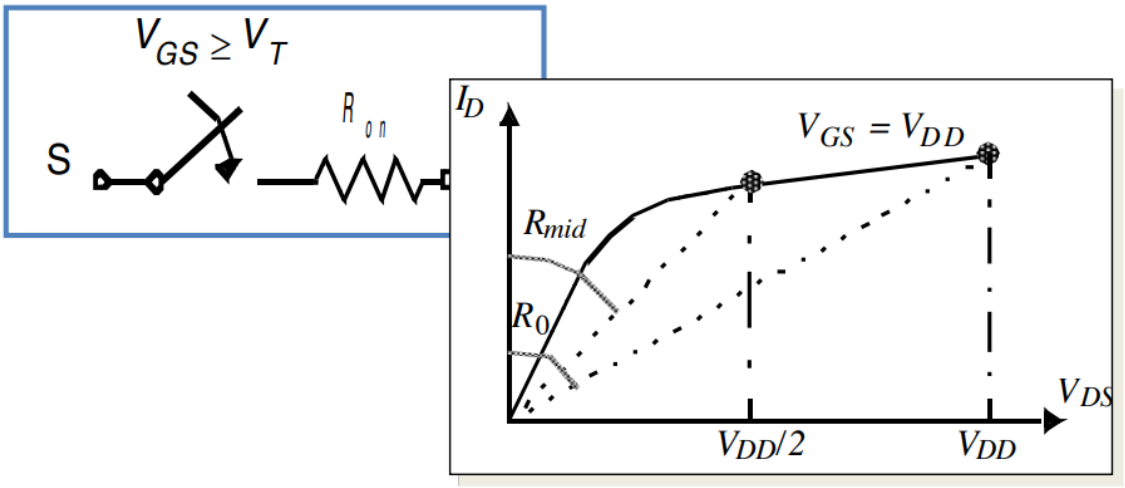


A PMOS Transistor



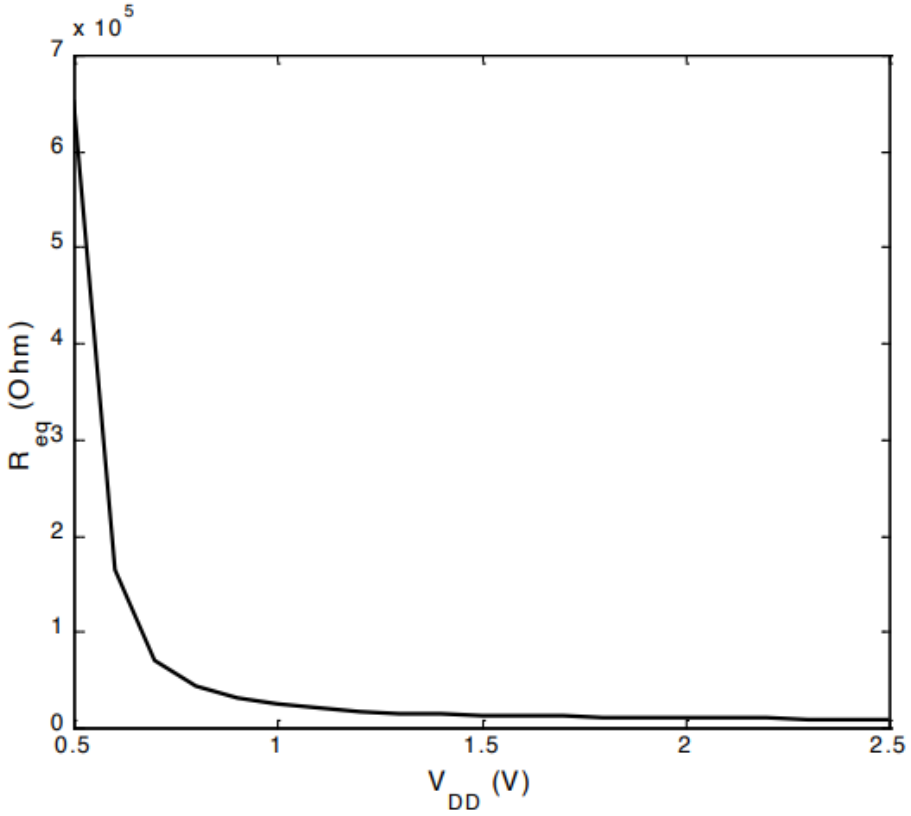
Assume all variables negative!

The Transistor as a Switch

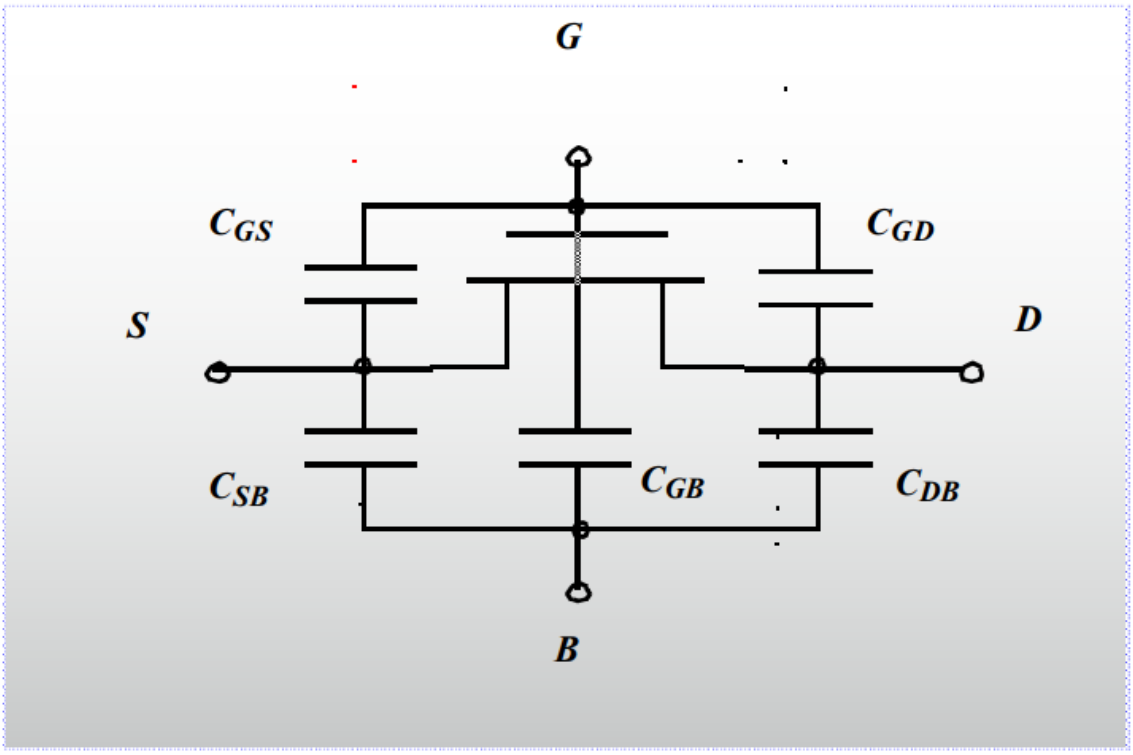


$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

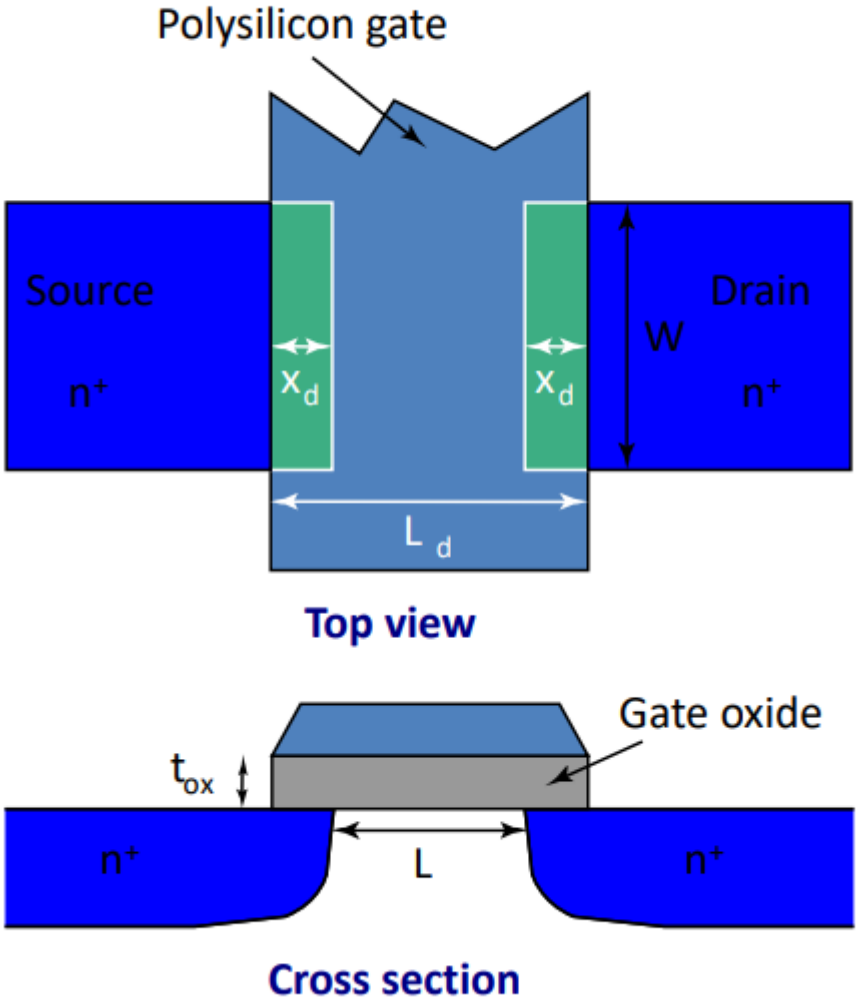
The Transistor as a Switch



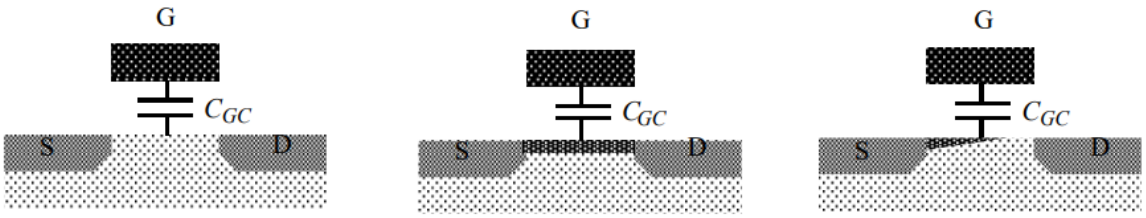
20.2.1 Capacitances and Nonidealities



Gate Overlap Capacitance

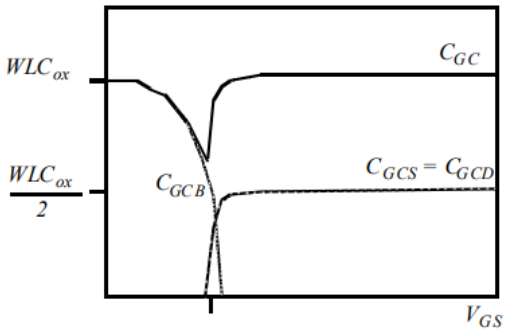


Gate-to-Channel Capacitance

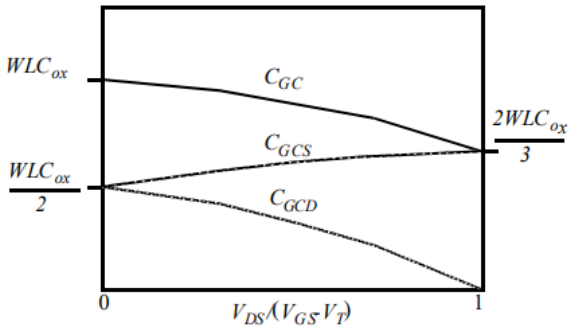


Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Gate Capacitance

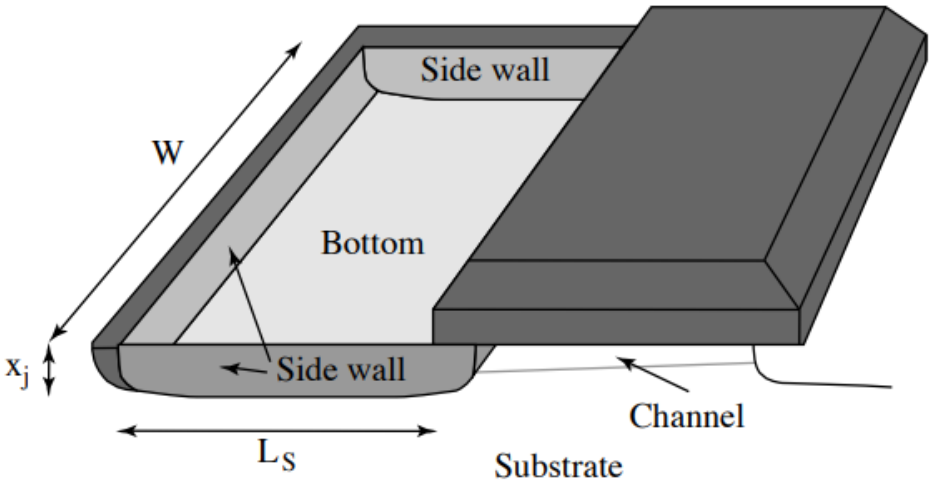


Capacitance as a function of V_{GS} (with $V_{DS} = 0$)



Capacitance as a function of the degree of saturation

Diffusion (Junction) Capacitance

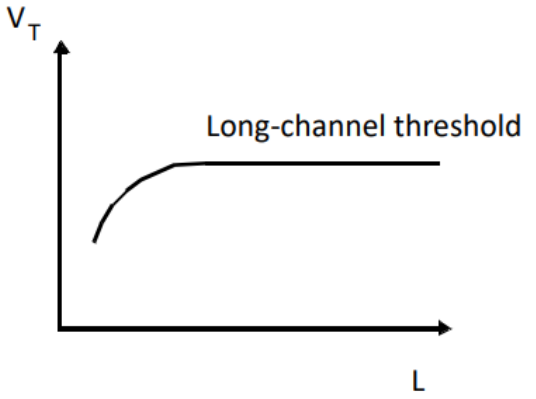


$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

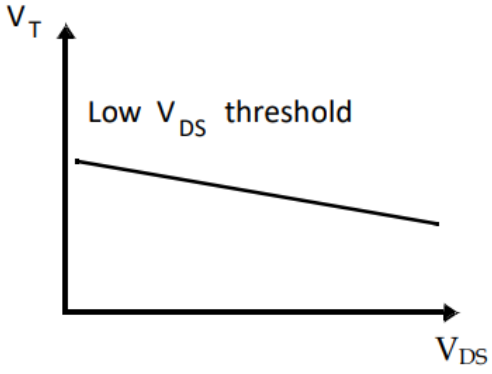
Summary of Capacitances

- Parasitic capacitance of MOS transistor
  - (C_{GS}): overlap, gate-to-channel (linear, saturation/velocity sat)
  - (C_{GD}): overlap, gate-to-channel (linear)
  - (C_{GB}): gate-to-channel (cutoff)
  - (C_{SB}): bottom plate, side wall
  - (C_{DB}): bottom plate, side wall, reverse-bias effect

Threshold Variations

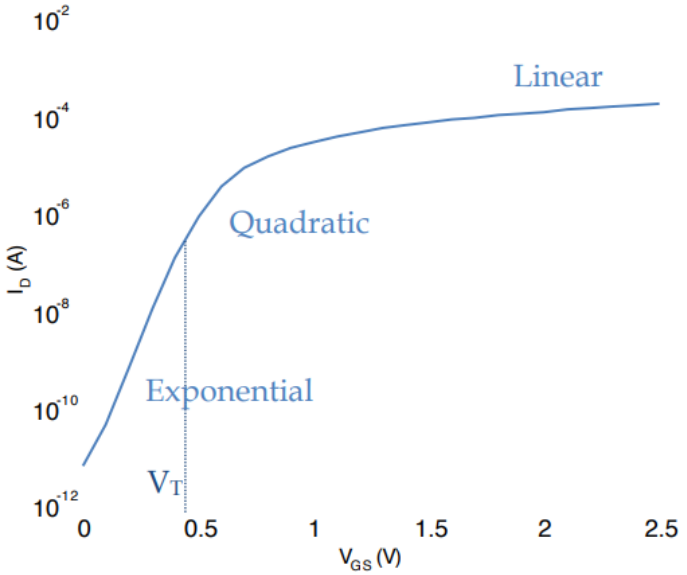


Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)

Sub-Threshold Conduction



$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n \approx 1.5$$

The Slope Factor

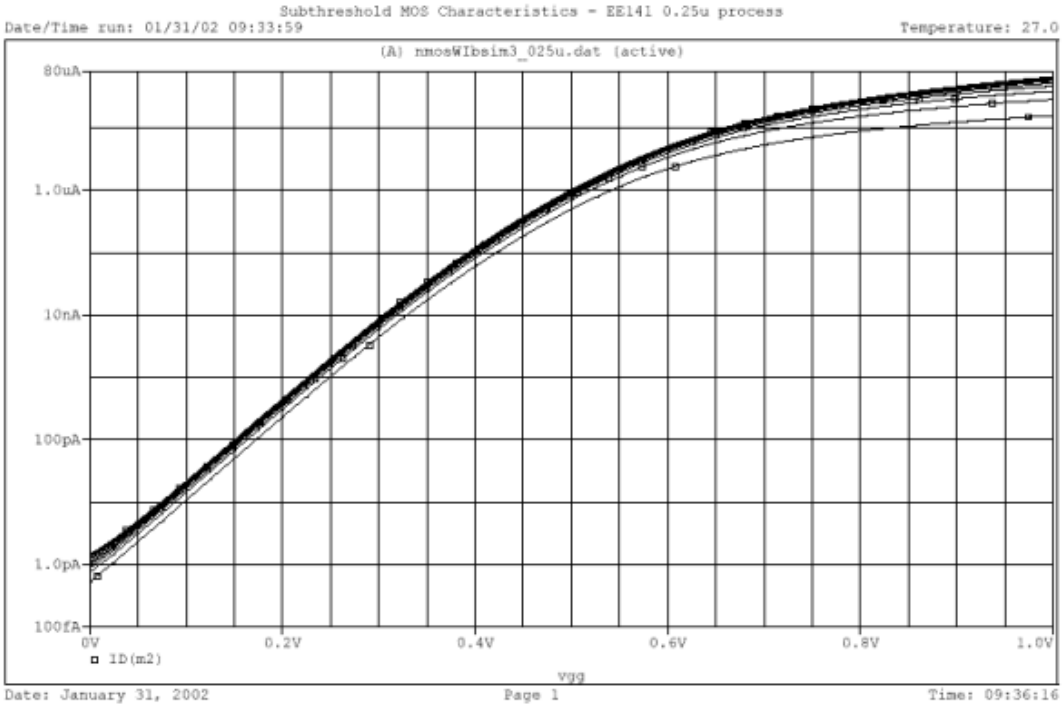
S is ΔV_{GS} for I_{D2}/I_{D1} =10

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Typical values for S:
60 .. 100 mV/decade

Sub-Threshold I_D vs V_{GS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}} \right)$$

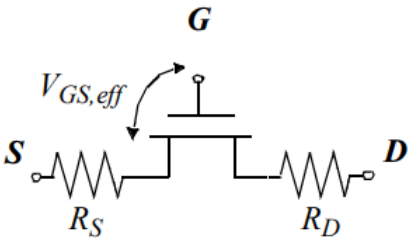


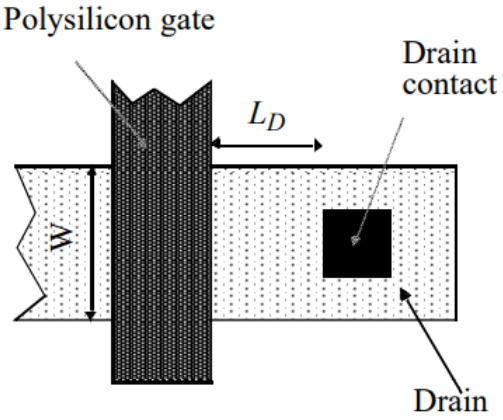
Summary of Sub-threshold Conduction

- Exponential dependence on (V_{GS})
- **Slope factor**
  - Higher slope factor ($\rightarrow$) subthreshold curve bends up, much higher current when (V_{GS} = 0) (more leakage when switched off)
  - Slope factor is a function of process parameter (n) and temperature (T)
- **(V_T) effect**
  - Lower (V_T) ($\rightarrow$) subthreshold curve shifts up, much higher current when (V_{GS} = 0) (more leakage when switched off)

– (V_T) is a function of many parameters, in particular (V_{SB}) (body effect, reverse bias PN junction raises (V_T)) and (V_{DS}) (drain-induced barrier lowering, higher (V_{DS}) lowers (V_T))

Parasitic Resistances



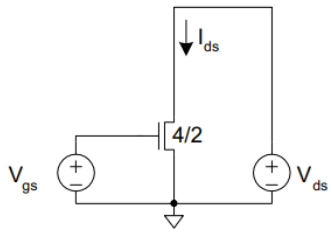


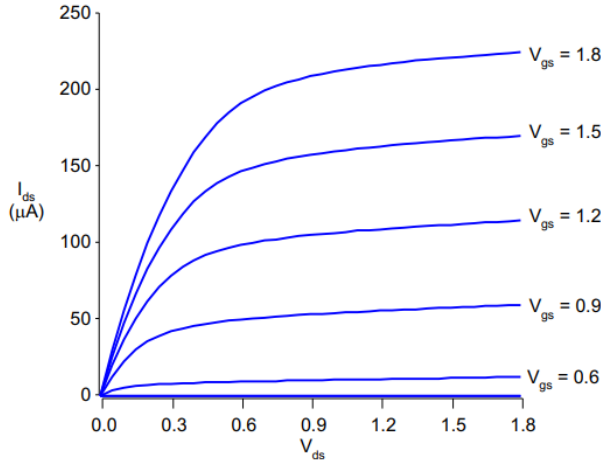
Circuit Simulation

- DC analysis
  - Compute the DC (steady-state, i.e., time->infinity) voltage or current
  - Sweep a range of input values, obtain a collection of output values
- Transient analysis
  - Most frequently used
  - Simulates the operation of the circuit as time progresses
  - Determines propagation delay, rise and fall times, and power dissipation

I-V Characteristics

- NMOS I-V





20.3 Device: MOS Fabrication

20.4 CMOS Inverter: Static Operation

20.5 CMOS Inverter: Dynamic Operation

20.6 CMOS Inverter: Sizing and Energy

20.7 CMOS Inverter: Scaling

20.8 Static CMOS Gates

20.9 Ratioed Logic

20.10 Pass Transistor Logic

20.11 Dynamic Logic

20.12 Interconnects

20.13 Latches and Registers

20.14 Memories

20.15 Memories: Peripherals

20.16 Memories: Flash, SRAM, DRAM

21 Interview & Problems

21.1 Interview

Concepts to know:

21.2 Problems

Common interview problems:

21.2.1 CMOS

21.2.2 Logic Design

21.2.3 Power

Q: Dynamic power dominates but why has static power consumption become increasingly important to deal with?

- Large transistor count - small leakage quickly get big when multiplied by billions of transistors
- Technology scaling - end of Dennard Scaling
  - Dennard Scaling suggested that power density remained constant at smaller transistor sizes - however the scaling has broken down at modern nodes
    - Scaling suggested VDD and VTh scales proportionally with feature size
  - VDD stopped scaling due to reliability
  - VTh stopped scaling as pushing it further down increases leakage
- Increased leakage currents
  - Subthreshold leakage - small threshold voltage leads to faster switching, but increases the leakage current even when transistor is OFF
  - Gate leakage - thin gate oxides in modern nodes lead to tunneling currents through the gate

  - Junction leakage - small junction depths increase leakage at source/drain junctions

Q: How to reduce dynamic power?

Q: How to reduce static power?

Q: What caused the end of Dennard Scaling?

- VDD stopped scaling due to reliability
- VTh stopped scaling as pushing it further down increases leakage

21.2.4 List of Questions - To be categorized...

References

Weste, Neil, and David Harris. 2010. *CMOS VLSI Design: A Circuits and Systems Perspective.* 4th ed. USA: Addison-Wesley Publishing Company.