References

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Invalid Date

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Preface

Notes on CMOS Integrated Circuits & VLSI.

Resources

Some relevant resources:

- EECS 312 - University of Michigan
- EECS 427 - University of Michigan
- CMOS VLSI Design Web Supplements
  - Contains supplemental materials e.g. lecture slides, figures, solutions, code, etc
- Digital VLSI Chip Design with Cadence and Synopsys CAD Tools

Textbooks:

- J. Rabaey, A. Chandrakasan, and B. Nikolic. Digital Integrated Circuits A Design Perspective, Edition: 2. Alexandria, VA: Prentice Hall, 2003
- CMOS VLSI Design: A Circuits and Systems Perspective 4th Edition

1 Introduction

1.1 Perspective

> Note 1: Definition - Some definition
>
> **Term** is defined as blah blah blah...

This note does ...

1.2 High Level Ideas

2 Circuit Basics

A brief review of the fundamental concepts of electrical circuits that form the foundation for understanding CMOS and VLSI design.

2.1 Important Constants

Constant	Symbol	Value	Units
Elementary Charge	e	1.602×10^{-19}	C
Boltzmann Constant	k_B	1.380×10^{-23}	J/K
Room Temperature	T	300	K
Thermal Voltage at 300K	V_T	25.9	mV
Silicon Bandgap	E_g	1.12	eV
Permittivity of Free Space	ϵ_0	8.854×10^{-12}	F/m
Silicon Relative Permittivity	ϵ_r	11.7	-
Silicon Oxide Relative Permittivity	ϵ_{ox}	3.9	-

2.2 Common Unit Conversions

From	To	Conversion
eV	Joules	1 eV $= 1.602 \times 10^{-19}$ J
Temperature	Thermal Voltage	$V_T = \frac{k_B T}{q}$
Frequency	Time Period	$T = \frac{1}{f}$
Resistance $\times$ Capacitance	Time Constant	$\tau = RC$

2.3 Charge, Voltage, Current, Power

2.3.1 Charge (Q)

Electric charge is measured in Coulombs (C). The fundamental unit of charge is the electron charge:

$$Q_e = -1.602 \times 10^{-19} \text{ C}$$

The movement of charge carriers (typically electrons in circuits) creates current.

2.3.2 Voltage (V)

Voltage is the electric potential difference between two points, measured in Volts (V). Key equations:

$$V = IR \text{ (Ohm's Law)}$$

$$V = \frac{dW}{dQ} \text{ (Work per unit charge)}$$

2.3.3 Current (I)

Current is the rate of charge flow, measured in Amperes (A):

$$I = \frac{dQ}{dt}$$

For sinusoidal signals:

$$I = I_0 \sin(\omega t)$$

2.3.4 Power (P)

Power is the rate of energy transfer, measured in Watts (W):

$$P = VI \text{ (instantaneous)}$$
$$P = I^2R \text{ (resistive loss)}$$
$$P = CV^2f \text{ (dynamic CMOS)}$$
$$P_{avg} = \frac{1}{T}\int_0^T p(t)dt \text{ (average)}$$

2.4 Capacitance, Inductance

2.4.1 Capacitance (C)

Capacitance is measured in Farads (F). Key equations:

$$Q = CV \text{ (charge stored)}$$
$$I_C = C\frac{dV}{dt} \text{ (capacitor current)}$$
$$\tau = RC \text{ (time constant)}$$

For parallel plate capacitors:

$$C = \frac{\epsilon_0 \epsilon_r A}{d}$$

where: - A is plate area - d is plate separation - ϵ_0 is permittivity of free space - ϵ_r is relative permittivity

2.4.2 Inductance (L)

Inductance is measured in Henries (H):

$$V_L = L\frac{dI}{dt}$$
$$\tau_L = \frac{L}{R} \text{ (inductive time constant)}$$
$$E = \frac{1}{2}LI^2 \text{ (stored energy)}$$

2.5 KVL & KCL

2.5.1 Kirchhoff's Voltage Law (KVL)

The sum of voltages around any closed loop equals zero:

$$\sum_{k=1}^{n} V_k = 0$$

2.5.2 Kirchhoff's Current Law (KCL)

The sum of currents entering a node equals the sum of currents leaving it:

$$\sum I_{in} = \sum I_{out}$$

$$\sum_{k=1}^{n} I_k = 0 \text{ (node equation)}$$

2.6 Additional Topics Relevant to CMOS/VLSI

2.6.1 Small Signal Analysis

Key parameters and equations:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{ (transconductance)}$$

$$r_o = \frac{\partial V_{DS}}{\partial I_D} \text{ (output resistance)}$$

$$A_v = -g_m r_o \text{ (small-signal gain)}$$

2.6.2 RC Networks

Time domain analysis:

$$v(t) = V(1 - e^{-t/RC}) \text{ (charging)}$$

$$v(t) = Ve^{-t/RC} \text{ (discharging)}$$

$$t_p \approx 0.69RC \text{ (propagation delay)}$$

2.6.3 Noise and Signal Integrity

Thermal noise power spectral density:

$$S_v(f) = 4k_B TR \text{ (V}^2\text{/Hz)}$$

Shot noise current spectral density:

$$S_i(f) = 2qI_D \text{ (A}^2\text{/Hz)}$$

Signal-to-Noise Ratio:

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{V_{signal,rms}^2}{V_{noise,rms}^2}$$

2.6.4 Semiconductor Physics Basics

Carrier concentration:

$$n_i^2 = N_C N_V e^{-E_g/k_B T}$$

Built-in potential:

$$V_{bi} = V_T \ln(\frac{N_A N_D}{n_i^2})$$

MOSFET threshold voltage:

$$V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{2\epsilon_s q N_A (2\phi_F)}}{C_{ox}}$$

where:

- V_{FB} is the flatband voltage
- ϕ_F is the Fermi potential
- N_A is acceptor concentration
- C_{ox} is oxide capacitance per unit area

2.7 PN Junctions

The PN junction is fundamental to semiconductor devices and CMOS operation. Key concepts and equations:

2.7.1 Built-in Potential

The built-in potential (V_{bi}) across the junction at equilibrium:

$V_{bi} = V_T \ln(\frac{N_A N_D}{n_i^2})$

where:

- N_A is acceptor concentration in p-region
- N_D is donor concentration in n-region
- n_i is intrinsic carrier concentration
- V_T is thermal voltage ($k_B T/q$)

2.7.2 Depletion Region

The depletion width (W) under bias:

$W = \sqrt{\frac{2\epsilon_s}{q}(\frac{N_A+N_D}{N_A N_D})(V_{bi} - V_A)}$

where:

- V_A is the applied voltage
- ϵ_s is semiconductor permittivity
- q is elementary charge

2.7.3 Current-Voltage Relationship

The ideal diode equation:

$I_D = I_S(e^{V_D/V_T} - 1)$

where:

- I_S is the reverse saturation current
- V_D is the diode voltage
- V_T is thermal voltage

The saturation current:

$I_S = qA(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p)$

where:

- D_p, D_n are diffusion coefficients
- L_p, L_n are diffusion lengths
- A is junction area

2.7.4 Junction Capacitance

The junction capacitance has two components:

Depletion capacitance:

$C_j = \frac{C_{j0}}{\sqrt{1-V_D/V_{bi}}}$

Diffusion capacitance:

$C_d = \tau_T \frac{dI_D}{dV_D} = \tau_T \frac{I_D+I_S}{V_T}$

where:

- C_{j0} is zero-bias junction capacitance
- τ_T is transit time

2.7.5 Temperature Effects

Temperature dependence of key parameters:

$I_S(T) \propto T^3 e^{-E_g/k_B T}$

$V_{bi}(T) = V_{bi}(T_0) - \beta(T - T_0)$

where β is the temperature coefficient.

2.8 Note

> **Note on Temperature Dependencies**
>
> Many parameters in CMOS circuits have significant temperature dependencies. Key relationships include:
>
> - Mobility: $\mu(T) \propto T^{-3/2}$
> - Threshold voltage: $V_{th}(T) = V_{th}(T_0) + \alpha(T - T_0)$
> - Leakage current: $I_{leak} \propto T^2 e^{-E_g/2k_B T}$

3 High-level Overview

3.1 MOS Transistors

Silicon Lattice

PN Junction

NMOS PMOS

3.2 CMOS Logic

3.2.1 Pass Transistors, Transmission Gates

3.2.2 Tristates

3.2.3 Multiplexers

3.3 Sequential Circuits

3.3.1 Latches

3.3.2 Flip-Flops

3.4 Fabrication & Layout

3.4.1 Fabrication Process

3.4.2 Layout Design Rules

3.4.2.1 Gate Layout

3.4.2.2 Stick Diagrams

3.5 Design Partitioning

3.6 Architecture

3.7 Logic Design

3.8 Circuit Design

3.9 Physical Design

3.10 Design Verification

3.11 Fabrication, Packaging, and Testing

4 CMOS Basics

5 CMOS Fabrication & Process Technology

6 CMOS Capacitance

7 Inverters and More Gates

8 Delay

9 Power

10 Interconnect

11 Robustness

12 Circuit Simulation

13 Combinational Circuit Design

Ref (Weste and Harris 2015)

14 Sequential Circuit Design

15 Datapath Subsystems

16 Array Subsystems

17 Special-Purpose Subsystems

18 Design Methodology and Tools

19 Testing, Debugging, and Verification

20 Summary

In summary...

21 Interview & Problems

21.1 Interview

Concepts to know:

21.2 Problems

Common interview problems:

21.2.1 CMOS

21.2.2 Logic Design

References

Weste, Neil HE, and David Harris. 2015. *CMOS VLSI Design: A Circuits and Systems Perspective*. Pearson Education India.