28.8 A 1.1V 16Gb DDR5 DRAM with Probabilistic-Aggressor Tracking, Refresh-Management Functionality, Per-Row Hammer Tracking, a Multi-Step Precharge, and Core-Bias Modulation for Security and Reliability Enhancement

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DRAM products have been recently adopted in a wide range of high-performance computing applications: such as in cloud computing, in big data systems, and IoT devices. This demand creates larger memory capacity requirements, thereby requiring aggressive DRAM technology node scaling to reduce the cost per bit [1,2]. However, DRAM manufacturers are facing technology scaling challenges due to row hammer and refresh retention time beyond 1a-nm [2]. Row hammer is a failure mechanism, where repeatedly activating a DRAM row disturbs data in adjacent rows. Scaling down severely threatens reliability since a reduction of DRAM cell size leads to a reduction in the intrinsic row hammer tolerance [2,3]. To improve row hammer tolerance, there is a need to probabilistically activate adjacent rows with carefully sampled active addresses and to improve intrinsic row hammer tolerance [2]. In this paper, row-hammer-protection and refresh-management schemes are presented to guarantee DRAM security and reliability despite the aggressive scaling from 1a-nm to sub 10-nm nodes. The probabilistic-aggressor-tracking scheme with a refresh-management function (RFM) and per-row hammer tracking (PRHT) improve DRAM resilience. A multi-step precharge reinforces intrinsic row-hammer tolerance and a core-bias modulation improves retention time: even in the face of cell-transistor degradation due to technology scaling. This comprehensive scheme leads to a reduced probability of failure, due to row hammer attacks, by 93.1% and an improvement in retention time by 17%.

The technology scaling platform, shown in Fig. 28.8.1, is implemented in 1a-nm 16-Gb DDR5 DRAM chip. Row control circuits consist of row hammer (R/H) control circuits based on probabilistic approaches to improve row hammer aggressor tracking ability. This protection scheme is cost-effective since it can be implemented within the peripheral circuit area. Aggressor tracking accuracy is improved using the PRHT scheme, which requires additional bank area and counts the number of active commands for each WL [2]. PRHT consists of a control unit, a read-modify-write (RMW) control block in the column control circuit, and additional R/H cells. A multi-step precharge (PCG) control scheme generates row control signals to implement multiple stages of the WL level during precharge operations to improve the intrinsic row-hammer tolerance. A core-bias modulation scheme is adopted to minimize the temperature variation of the intrinsic row hammer tolerance, which leads to increased refresh-retention time for reliability and reduces refresh power consumption.

The DRAM controller counts the number of activation executions (RAACNT) and reads the threshold (RAAIMT) from the mode-register in the DRAM (see RFM algorithm in Fig. 28.8.2) [3]. When the RAACNT value is larger than RAAIMT, the controller executes RFM so that the DRAM conducts an additional refresh operation with the sampled address from the DRAM R/H control circuit. Refresh (REF) command is utilized for both a normal refresh operation to guarantee cell retention time and a target refresh operation for row-hammer mitigation with the sampled activation address [4]. Based on RFM and REF, the refresh-command-generation block in the R/H control circuit generates a row-hammer refresh command (RH_REF) and normal refresh (NREF) command for cell retention time. Probabilistic-aggressor-tracking (PAT) logic is proposed to sample the active addresses for row hammer mitigation with a higher accuracy than based on probabilistic approaches. To sample the active addresses randomly, a random generation block in the PAT generates a random flag (EN) based on a pseudorandom-binary sequence. When randomly selected activation commands latch ACT_ADD<0:15> in the PRE_LATCH, comparators in the latch sets compare the latched addresses in PRE_LATCH with addresses stored in LATCH<0:6> and the hidden latch. The hidden latch is designed to latch additional active aggressor when all of LATCH<0:6> are occupied, and malicious activation is focused on other addresses. Unlike LATCH<0:6>, a hidden latch does not have a corresponding counter. When an address does not exist in LATCH<0:6> and the hidden latch, all values of COMP<0:7> are set to zero and the R/H controller triggers the PIN signal to store the latched address in PRE_LATCH in one of the latches among LATCH<0:6> with ACT, EN, and COMP<0:7> signals. When the active addresses stored in LATCH<0> to LATCH<6> are sampled in the PRE_Latch again, a paired counter value from COUNTER<0> to COUNTER<6> is also increased. The R/H controller finally selects the row hammer address, RH_ADD, using RH_REF and COUNTER<0:6>, which are counter values. RH_ADD<0:15> is chosen among the stored address from LATCH<0:6> and the hidden latch. The refresh address, REF_ADD<0:15>, is generated with RH_ADD for row hammer mitigation and N_ADD, which is generated with address counters for a normal refresh.

Per-row hammer tracking (PRHT) is presented in Fig. 28.8.3. The R/H cells to store the number of activation executions for each WL are added with additional columns. Internal RD (IRD) and internal write (IWR) execute RMW to check and update the number of activation executions between activation and precharge operations. The IRD and IWR control signals are generated from the RMW control block shown in Fig. 28.8.1. When a WL whose address is 0x3 is activated, the IO sense amplifiers (IOSAs) read the cumulative activation counter number (0xA) from the R/H cell for the WL address and the adder updates the Cell_RD register value to 0xB by adding one to 0xA. If the Cell_RD value is larger than the Max_CNT number, then the Max_CNT number is updated to 0xB and the comparator sends the Update signal to latch sets to store the current active address from address latch0 in address latch1 for row hammer mitigation. The Cell_RD value is written in R/H cell with write driver (WTDRV) with IWR internal command. Two additional refresh commands are needed for row hammer mitigation for each WL. One refresh command is used to reset R/H cell with RSTADD_N1 as zero and next refresh conducts row hammer mitigation for adjacent rows with ADD_N2 and ADD_N0 with addresses stored in address latch 2, which are latched with the refresh for reset.

Charge loss due to a row hammer attack occurs during active and precharge operations. The magnitude of the electric field during a precharge operation can determine the amount of electron charges that are dispersed to neighboring cells. The multi-step precharge circuit, shown in Fig. 28.8.4, improves intrinsic row-hammer tolerance by creating an electric field that helps to maximize the amount of returning electron charges into a victim cell and to minimize electron charges to be dispersed into adjacent cells. In the timing diagram shown in Fig. 28.8.4, V_A is the optimized sub-WL level to minimize charge loss for the victim cell under a row-hammer attack. The mutli-step precharge control circuit shown in Fig. 28.8.4 and 28.8.1 generates MWLT, FXB0, and FXB1 signals to generate the multi-stage sub-WL level in Fig. 28.8.4.

The reduction in cell size leads to a degradation of intrinsic row-hammer tolerance and refresh retention time, which is closely related to a cell transistor reliability and power consumption. Moreover, there is a trade-off between the intrinsic row-hammer tolerance and the refresh retention time within a fixed cell size. The body bias of a cell transistor (V_{BB}) can be used to balance the two parameters by controlling the cell transistor's threshold voltage and leakage. A V_{BB} temperature-modulation circuit is proposed in Fig. 28.8.5 to maximize refresh retention time across 25 – 90°C by making the intrinsic row-hammer tolerance similar across temperature. V_{REFB} and V_{REFBH} are reference voltages generated by the reference generation amplifier. V_{BB} is determined by a feedback loop from a charge pump, which is regulated by a variable resistance controlled by the CTRL_CODE from the TEMP_CTRL block, until detector (DET) cannot detect the difference in input voltage levels. The TEMP_CTRL block sets a variable resistance value based on TEMP_CODE from the temperature sensor and the fuse information based on intrinsic row-hammer tolerance.

Figure 28.8.6 presents measurement results of the proposed schemes. Compared to a DRAM device using conventional aggressor tracking logic [5], the DRAM device with the proposed PAT logic functionally passes fifty row-hammer malicious pattern attacks even with a 66% lower intrinsic row-hammer tolerance, which makes DRAM tolerant even with technology scaling. The probability of failure is reduced when the RFM function enabled, by lowering RAAIMT values. The probability of failure with fifty row hammer malicious patterns is reduced by 90.5% using the PRHT scheme. The intrinsic row-hammer tolerance is improved by 37% with the multi-step precharge scheme compared to a conventional single-step precharge scheme [1]. V_{BB} temperature modulation improves refresh retention time by 17% at 90°C. The 16-Gb DDR5 DRAM is fabricated in a 1a-nm high-k metal-gate DRAM process; the micrograph is presented in Fig. 28.8.7.

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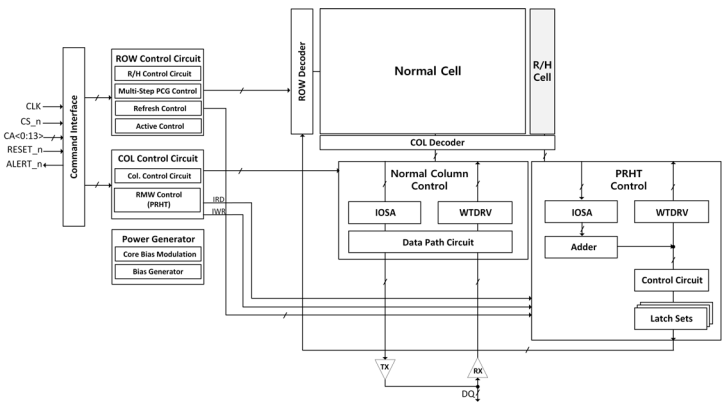

Figure 28.8.1: Block diagram of the technology scaling platform used for evaluating the proposed and conventional schemes.

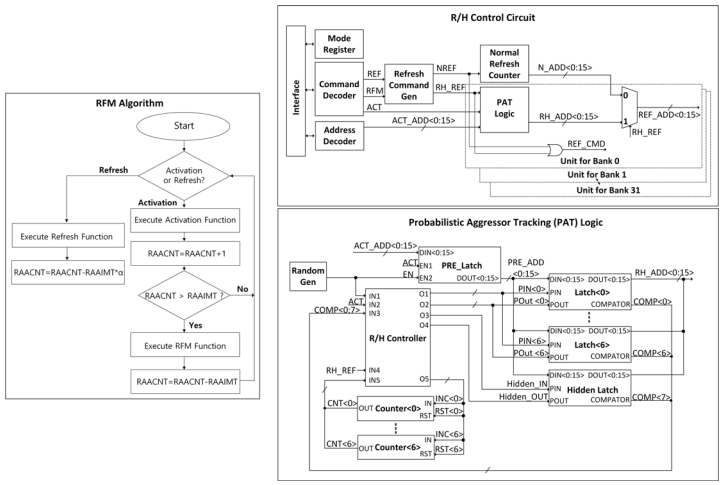

Figure 28.8.2: RFM algorithm with a flow chart to execute RFM function in a memory controller, R/H control circuit for refresh operations, and probabilistic aggressor tracking (PAT) logic for tracking row hammer addresses.

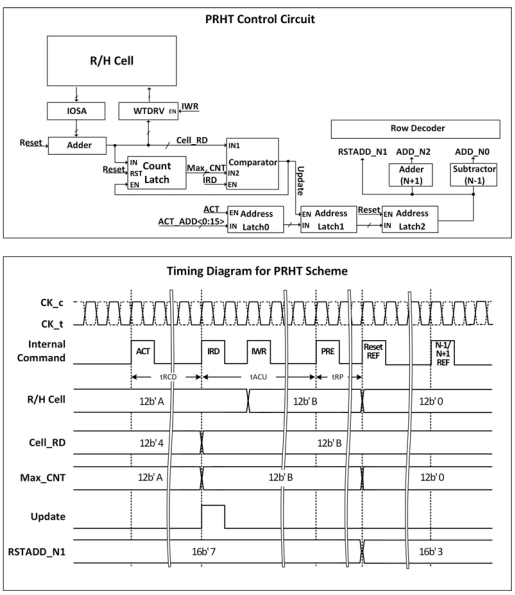

Figure 28.8.3: Control circuit (top) and timing diagram for the PRHT scheme (bottom).

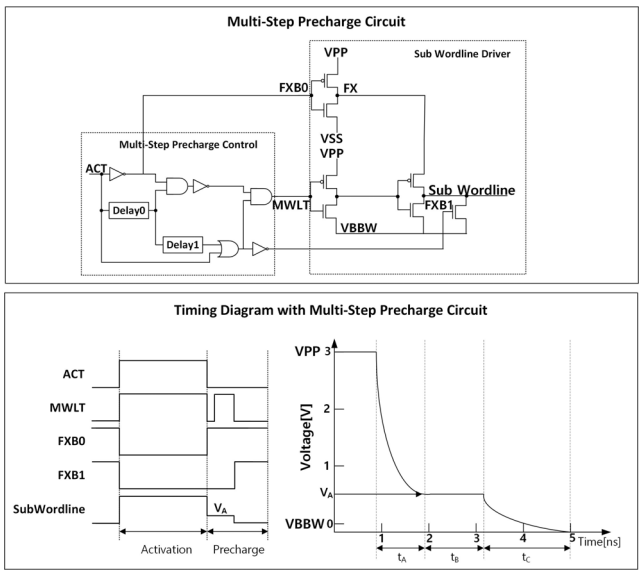

Figure 28.8.4: Circuit (top) and timing diagram (bottom) for multi-step precharge circuit.

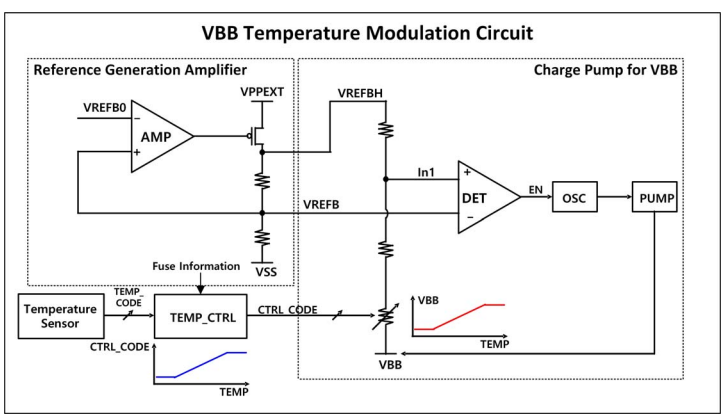

Figure 28.8.5: V_{BB} temperature modulation circuit.

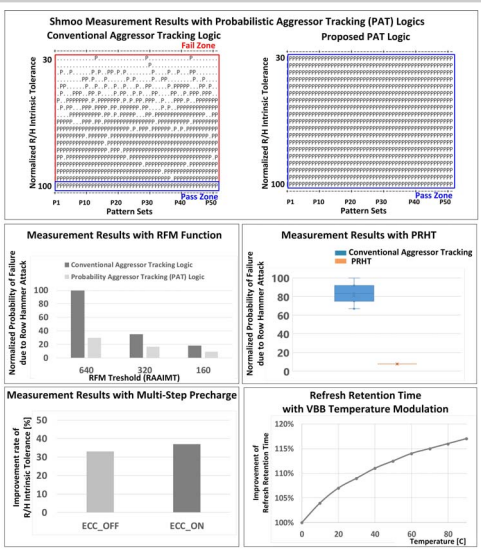

Figure 28.8.6: Measurement results for the proposed schemes: Improvements of row hammer resilience with PAT, RFM, PRHT, and multi-step precharge schemes and refresh retention time with VBB temperature modulation.

Chip summary	
Technology	1anm 5-metal DRAM HKMG process
Data Rate	6.4 Gbps/pin
Burst Length	BC8, BL16 on the fly
Number of IO	X4/X8/X16
Chip Size	7.159mm X 7.444mm

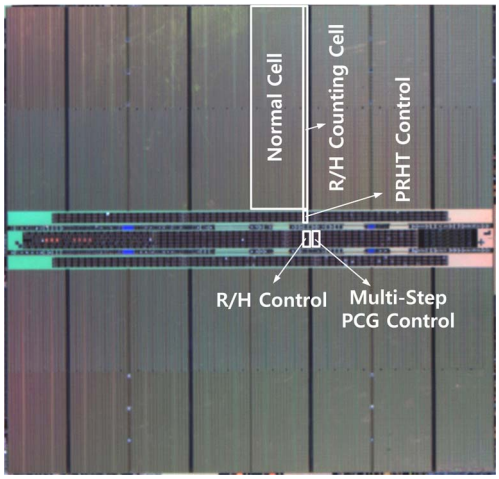

Figure 28.8.7: Chip summary and micrograph.

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