Solution

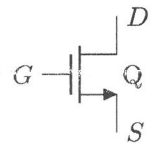
CSU0049 Analog and Digital Computing Elements, Homework 3

Department of Computer Science and Information Engineering

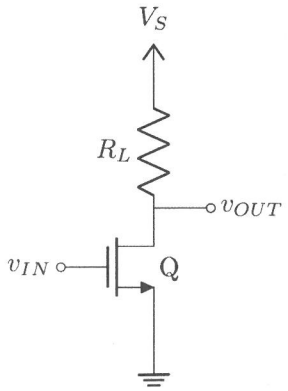
National Taiwan Normal University

October 15, 2024

- 100 regular points plus 50 bonus points (the one labeled *Bonus Task* on the last page). Unless otherwise stated, you should give your answer in English and show clearly how you derived your answer.
- In this course, the MOSFET we study is a specific type in the MOSFET family, called n-channel enhancement-type MOSFET (NMOS for short), with its terminals *gate* (G), *source* (S), and *drain* (D) denoted as follows:

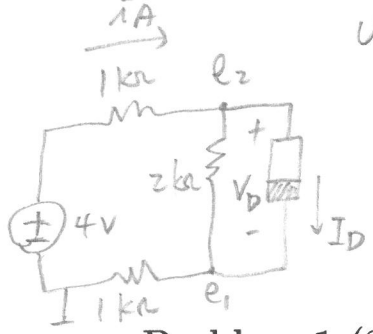


With an arrow to indicate the source terminal, in the rest of this document we do not label each terminal. We use Q to label a MOSFET as a whole. Finally, by *a MOSFET inverter* we suppose the following circuit:



The value of V_T is not needed in this homework assignment.

- The sum-of-products representation, as requested in Problem 5, is a standard way to describe logic expressions, and we will learn it on this Friday.



Using the node analysis,

$$\begin{cases} e_2 - e_1 = V_D \\ \dfrac{4-e_2}{1} = \dfrac{e_1-0}{1} \quad (i_A = i_B, \text{ considering } \boxed{} \text{ as one node.}) \\ \dfrac{e_1-0}{1} = \dfrac{e_2-e_1}{2} + 4V_D^2 \quad (\text{KCL at } e_1) \end{cases}$$

$$\Rightarrow V_D = \frac{-1+\sqrt{33}}{8}\ V \Rightarrow I_D = 4V_D^2\ mA$$

Alternatively, we may first transform the circuit into

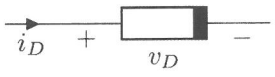
using Thévenin's theorem. Then

$$\frac{2-V_D}{1} = 4V_D^2$$

$$\Rightarrow V_D = \frac{-1+\sqrt{33}}{8}\ V$$

Problem 1 (20 points)

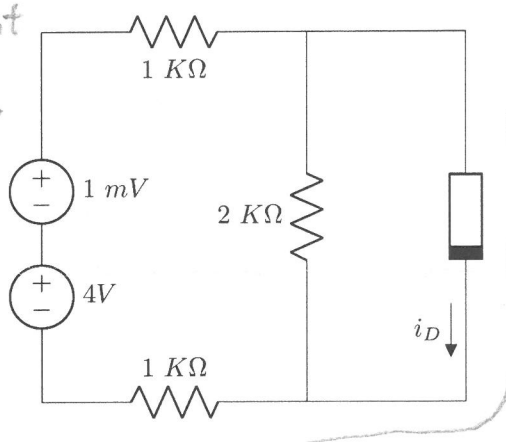
Consider the following nonlinear element:



and its element law:

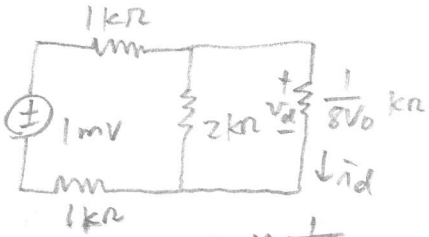
$$i_D = \begin{cases} 4(v_D)^2\ mA & \text{, if } v_D > 0 \\ 0 & \text{, otherwise.} \end{cases}$$

For the following circuit, use the small-signal analysis (i.e., the incremental analysis) to determine the value of i_D. Consider the overall voltage source $v_I = V_I + v_i$, where $V_I = 4\ V$ and $v_i = 1\ mV$.



2° Now, for the current contributed by ± 1 mV, we replace ▭ by its small-signal resistance:

$$r_d = \frac{1}{(4V_D^2)'}\bigg|_{V_D=V_D} = \frac{1}{8V_D}\ k\Omega$$



$$v_d = 1 \times \frac{2 \,//\, \frac{1}{8V_D}}{1 + (2 \,//\, \frac{1}{8V_D}) + 1} = \frac{1}{2+16V_D}\ mV$$

$$\Rightarrow i_D = I_D + i_d = 4V_D^2 + \frac{10^{-3}}{2+16V_D} \cdot 8V_D\ mA$$

$$= \frac{17-\sqrt{33}}{8} + \left(\frac{1}{2} - \frac{\sqrt{33}}{66}\right) \times 10^{-3}\ mA$$

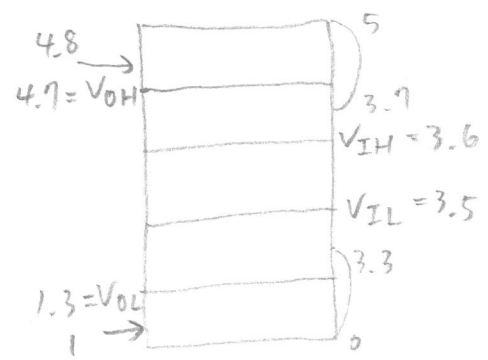
#

Problem 2 (20 points)

Suppose a digital device called D_s operates under a static discipline with the following specification:

$$V_{IH} = 3.6\ V,\ V_{IL} = 3.5\ V,\ V_{OH} = 4.7\ V,\ V_{OL} = 1.3\ V. \qquad (2)$$

The device is built by connecting several sub-modules together, and the connection between sub-modules must satisfy the above specification. The following is one of the candidate sub-modules. For the output side, the sub-module will produce 4.8 volts for logical 1 and 1 volt for logical 0; for the input side, the sub-module can interpret voltage between 3.7 volts and 5 volts as logical 1, and voltage between 0 volt and 3.3 volt as logical 0. Is this sub-module compatible to the specification of the digital device D_s? In other words, can we use it as one of the sub-modules that together build D_s? Explain.



The sub-module is NOT compatible because it violates the specification at the input side. Specifically, it cannot interpret input voltage between 3.6 ~ 3.7 V and between 3.3 ~ 3.5 V. See textbook Example 5.2 for a related problem.

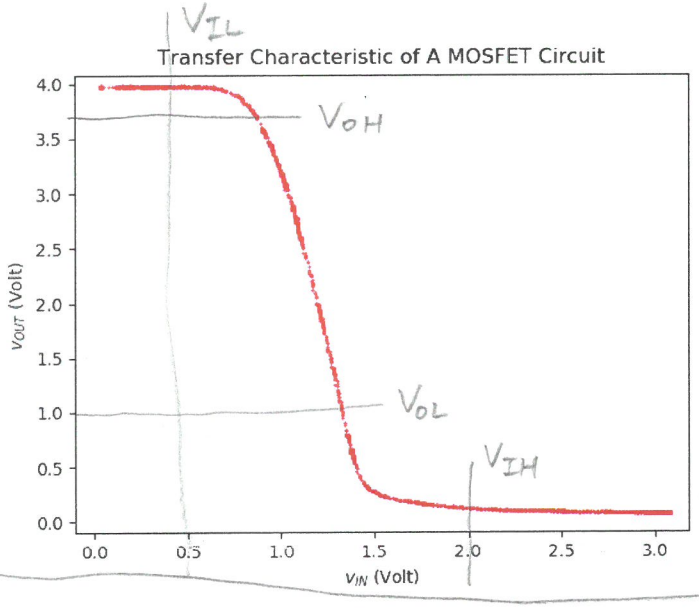
③ Plotting V_{OH}, V_{OL}, V_{IH}, V_{IL} on the figure it shows that the circuit satisfies the given static discipline, because for input $\leq V_{IL}$ the output will be $\geq V_{OH}$ and for input $\geq V_{IH}$ the output will be $\leq V_{OL}$.

Problem 3 (20 points)

While the circuit meets the static discipline here, the discipline itself has a bug: $V_{IL} < V_{OL}$ would provide no noise margin for logical LOW. This teaches us a lesson that if the specification is poor, meeting the specification does not mean the device can function correctly.

The following figure shows a real transfer characteristic of a MOSFET inverter circuit. In view of the following specification, does the circuit satisfy the static discipline? Explain your reasoning for *each* of the four threshold voltages.

Specification: $V_{OH} = 3.7\ V, V_{OL} = 1.0\ V, V_{IH} = 2.0\ V, V_{IL} = 0.5\ V$.



④ input HIGH ⇒ output LOW

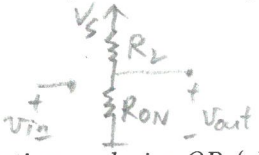
Problem 4 (20 points)

To meet the static discipline, the output logical LOW must have voltage no higher than V_{OL}.

Given a MOSFET inverter, explain why its implementation must satisfy the following inequality:

$$V_S \cdot \frac{R_{ON}}{R_L + R_{ON}} \leq V_{OL},$$

where V_{OL} is the voltage threshold for the static discipline. Assuming that we restrict ourselves to the SR model.



In the MOSFET inverter, the output voltage of logical LOW is $V_S \cdot \frac{R_{ON}}{R_L + R_{ON}}$ according to the voltage divider pattern. Therefore, the implementation must satisfy

$$V_S \cdot \frac{R_{ON}}{R_L + R_{ON}} \leq V_{OL}.$$

QED.

Problem 5 (20 points)

The following truth table defines the logic operation *exclusive-OR* (aka `XOR`), with A, B as the input terminals and C as the output terminal:

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

⑤ $C = \bar{A} \cdot B + A \cdot \bar{B}$

Give the *sum-of-products representation* for the output terminal.

Bonus Task (50 points)

Prepare and submit a two-page note that summarizes what you've learned in the first half of the semester. This is something you can bring to your future career in computer engineering. This could also serve as a note that you can bring with you to the midterm exam. You may write, draw, or use any other formats that you find best.

Suggested Readings

You are encouraged to carefully study textbook Examples 5.1 to 5.5, as well as Section 6.8.1 in the textbook. Those are well-made learning materials.