

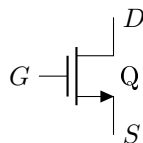
CSU0049 Analog and Digital Computing Elements, Homework 3

Department of Computer Science and Information Engineering

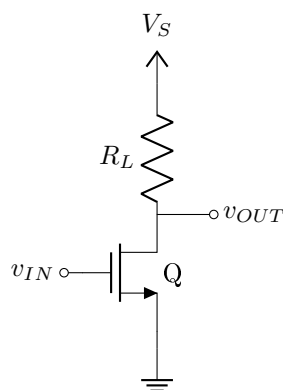
National Taiwan Normal University

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- 100 regular points plus 50 bonus points (the one labeled *Bonus Task* on the last page). Unless otherwise stated, you should give your answer in English and show clearly how you derived your answer.
- In this course, the MOSFET we study is a specific type in the MOSFET family, called n-channel enhancement-type MOSFET (NMOS for short), with its terminals *gate* (G), *source* (S), and *drain* (D) denoted as follows:



With an arrow to indicate the source terminal, in the rest of this document we do not label each terminal. We use Q to label a MOSFET as a whole. Finally, by a *MOSFET inverter* we suppose the following circuit:

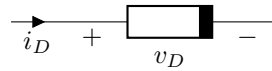


The value of V_T is not needed in this homework assignment.

- The sum-of-products representation, as requested in Problem 5, is a standard way to describe logic expressions, and we will learn it on this Friday.

Problem 1 (20 points)

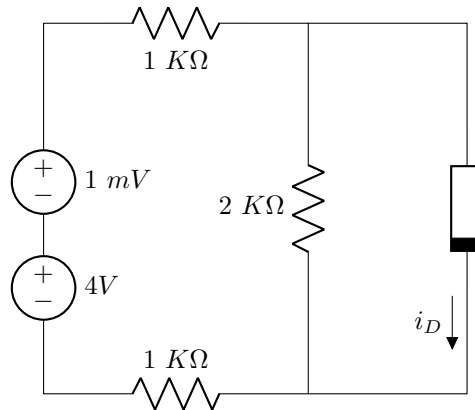
Consider the following nonlinear element:



and its element law:

$$i_D = \begin{cases} 4(v_D)^2 \text{ mA} & , \text{ if } v_D > 0 \\ 0 & , \text{ otherwise.} \end{cases} \quad (1)$$

For the following circuit, use the small-signal analysis (i.e., the incremental analysis) to determine the value of i_D . Consider the overall voltage source $v_I = V_I + v_i$, where $V_I = 4 \text{ V}$ and $v_i = 1 \text{ mV}$.



Problem 2 (20 points)

Suppose a digital device called D_s operates under a static discipline with the following specification:

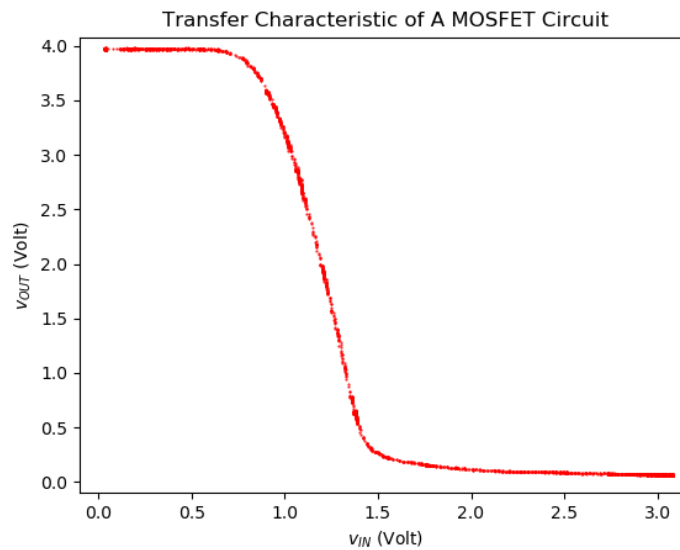
$$V_{IH} = 3.6 \text{ V}, V_{IL} = 3.5 \text{ V}, V_{OH} = 4.7 \text{ V}, V_{OL} = 1.3 \text{ V}. \quad (2)$$

The device is built by connecting several sub-modules together, and the connection between sub-modules must satisfy the above specification. The following is one of the candidate sub-modules. For the output side, the sub-module will produce 4.8 volts for logical 1 and 1 volt for logical 0; for the input side, the sub-module can interpret voltage between 3.7 volts and 5 volts as logical 1, and voltage between 0 volt and 3.3 volt as logical 0. Is this sub-module compatible to the specification of the digital device D_s ? In other words, can we use it as one of the sub-modules that together build D_s ? Explain.

Problem 3 (20 points)

The following figure shows a real transfer characteristic of a MOSFET inverter circuit. In view of the following specification, does the circuit satisfy the static discipline? Explain your reasoning for *each* of the four threshold voltages.

Specification: $V_{OH} = 3.7\text{ V}$, $V_{OL} = 1.0\text{ V}$, $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$.



Problem 4 (20 points)

Given a MOSFET inverter, explain why its implementation must satisfy the following inequality:

$$V_S \cdot \frac{R_{ON}}{R_L + R_{ON}} \leq V_{OL},$$

where V_{OL} is the voltage threshold for the static discipline. Assuming that we restrict ourselves to the SR model.

Problem 5 (20 points)

The following truth table defines the logic operation *exclusive-OR* (aka XOR), with A, B as the input terminals and C as the output terminal:

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Give the *sum-of-products representation* for the output terminal.

Bonus Task (50 points)

Prepare and submit a two-page note that summarizes what you've learned in the first half of the semester. This is something you can bring to your future career in computer engineering. This could also serve as a note that you can bring with you to the midterm exam. You may write, draw, or use any other formats that you find best.

Suggested Readings

You are encouraged to carefully study textbook Examples 5.1 to 5.5, as well as Section 6.8.1 in the textbook. Those are well-made learning materials.