Lab 1 - Introduction

Purpose : This lab is designed to provide an introduction to the Cadence® Orcad Solutions software. We will be using this program to examine logic gates and how they work. In future labs, we will use the software to experiment with the design of logic circuits.

NOTE: We are using a student version of this software so there are some limitations to what we can do. Please keep this in mind.

Deliverables: A printout of your circuit(s) and the timing diagram(s).

Prep Work:

Create a folder named **LAB1** on either the Desktop or your flash drive. This folder is where all the files for this lab will be saved. NOTE: Using a flash drive is HIGHLY recommended.

Download the input.stl file from CANVAS and place it in the folder created above.

Part 1: Getting Started.

1. Log-in to a lab computer using your student ID and password. If you are using your own computer, skip this step.

2. Click on the Windows start menu. Click on all programs.

3. Click on Cadence. Click on **OrCAD 16.6 Lite**. See figure 1.

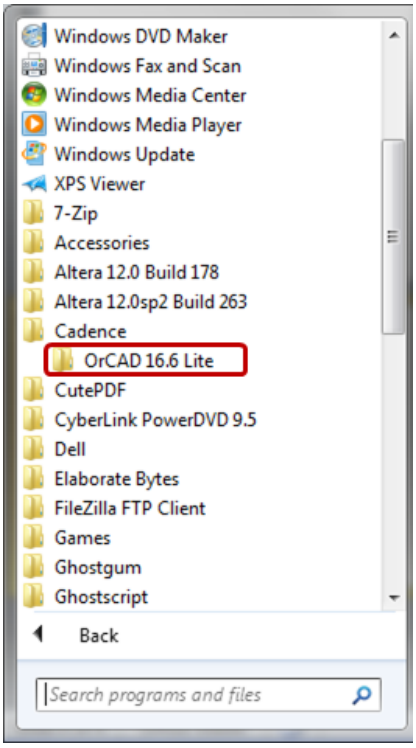

Figure 1: Select OrCAD 16.6 Lite

4. The folder expands and gives you many options. Click on ***OrCAD Capture CIS Lite***. See figure 2.

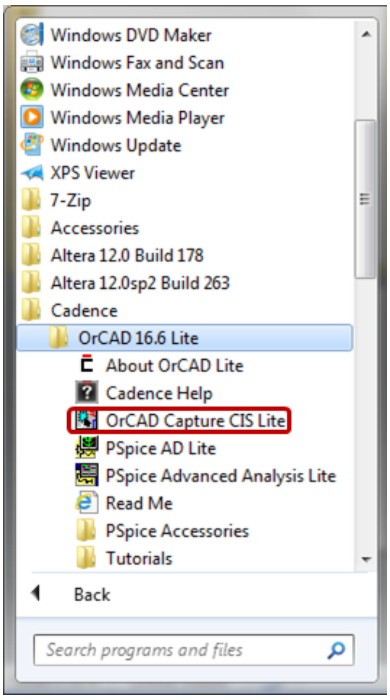

Figure 2: Select OrCAD Capture CIS Lite

5. At this point you may see an error message (see figure 3), if so just hit enter or select yes.

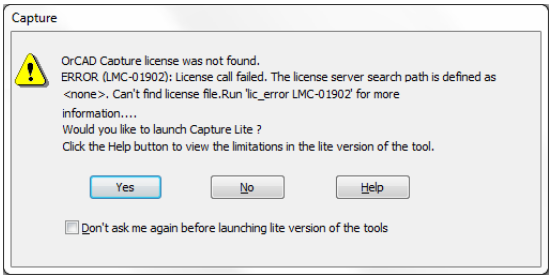

Figure 3: Possible Error Message

6. The OrCAD Capture CIS Lite start page is displayed. This page will be accessible to you via the tab unless you close it. If you choose to close it, all functions are available via the menu options at the top of the screen. Keeping in mind that we will only be using part of this extremely powerful software for this class, feel free to watch the tutorial. It provides much more information than we need for this class, but is available to you if you wish to watch it later. For now let's continue forth and create our first project.

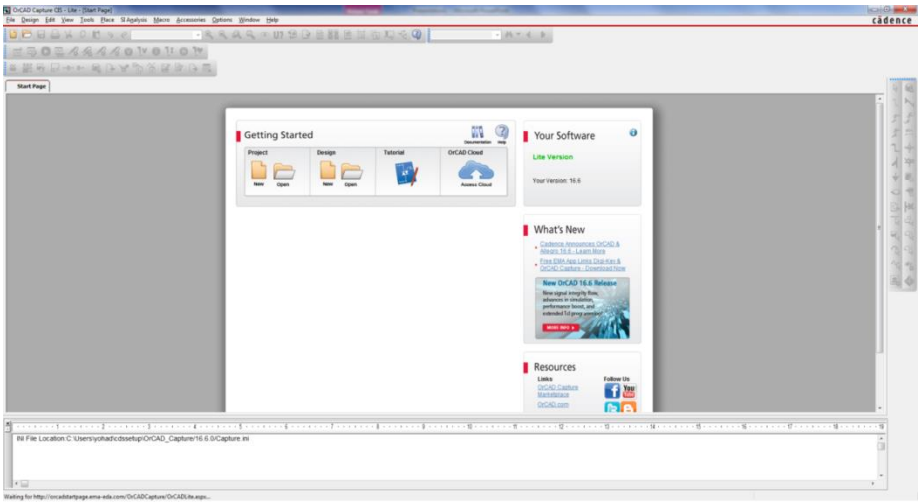

Figure 4: The Start Page

7. To create a new project, you can either click on the **New Project** icon under **Project** or you can select **File -> New -> Project** from the menu bar.

8. A pop-up window appears. Enter your project name in the following format, **LAB1_(lastname)** Make sure **Analog or Mixed A/D** is selected. If it is not, click on it to select it. Otherwise you will not be able to simulate the lab AND will have to start all over. In the location box, browse to the folder created at the start of the lab (Prep Work) and click OK.

Example: LAB1_Yoha

9. Another window pops-up. Make sure the **Create a blank project** is selected and click OK. At this point, a project has been created with a blank schematic ready for input

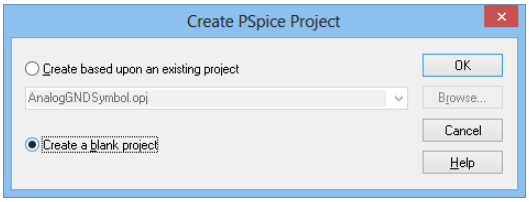

Figure 5: Creating a blank project

10. Click on the tab corresponding to your file name. This tab shows the hierarchy of the files in your project.

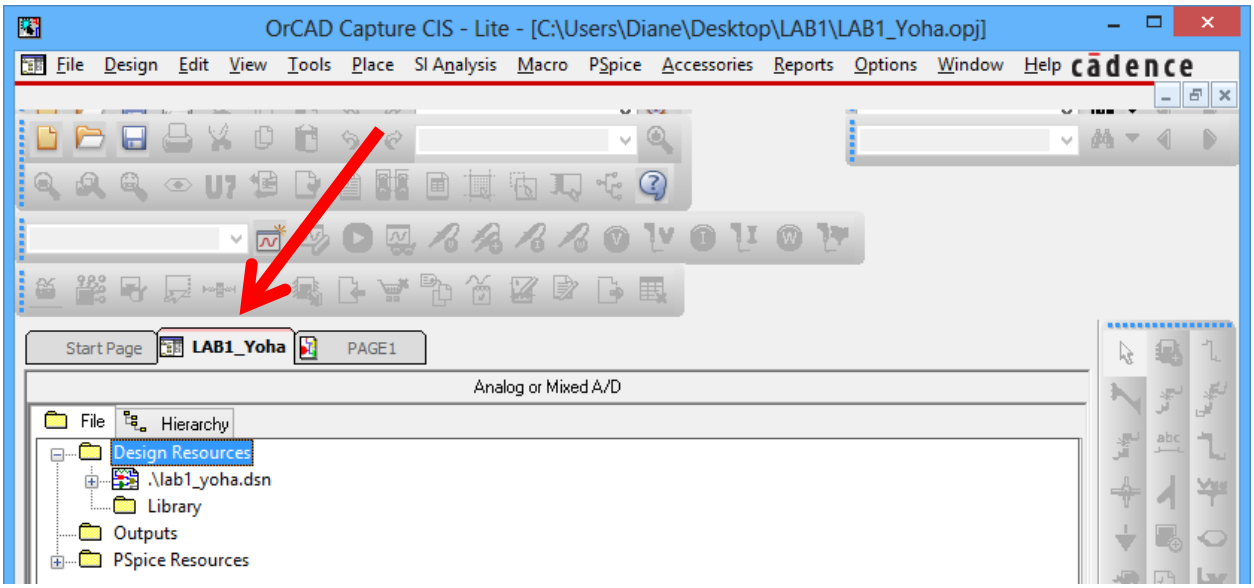

Figure 6: Hierarchy of your project

11. Click on the + to expand all the folders under Design Resouces and click on the + by the filename with the .dsn extension if that section has not been expanded. Keep expanding each successive section under Design Resources until you see PAGE1.

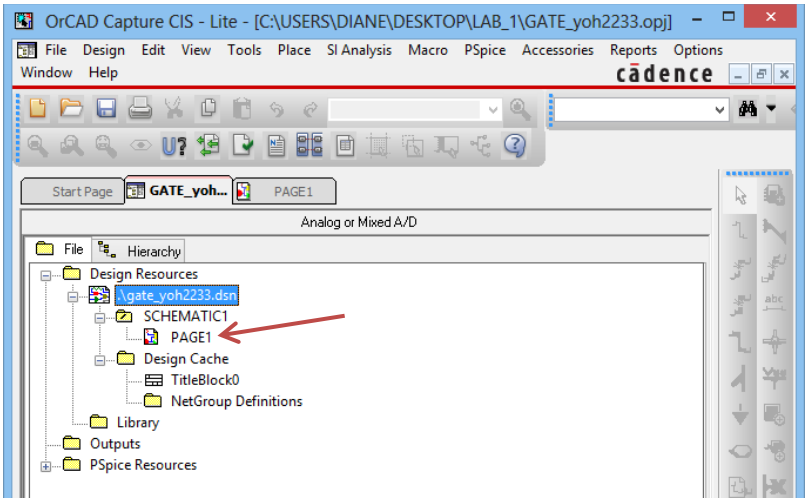

Figure 7: Hierarchy Tab Expanded folders

12. Right click on SCHEMATIC1, click **Rename** and enter the new name – GATES_(lastname). Now rename Page1 the file to the same thing as your project name. Rename PAGE1 to ANDgate_(lastname). Throughout this course, rename all Schematics and subsequent pages to "something logical_lastname."

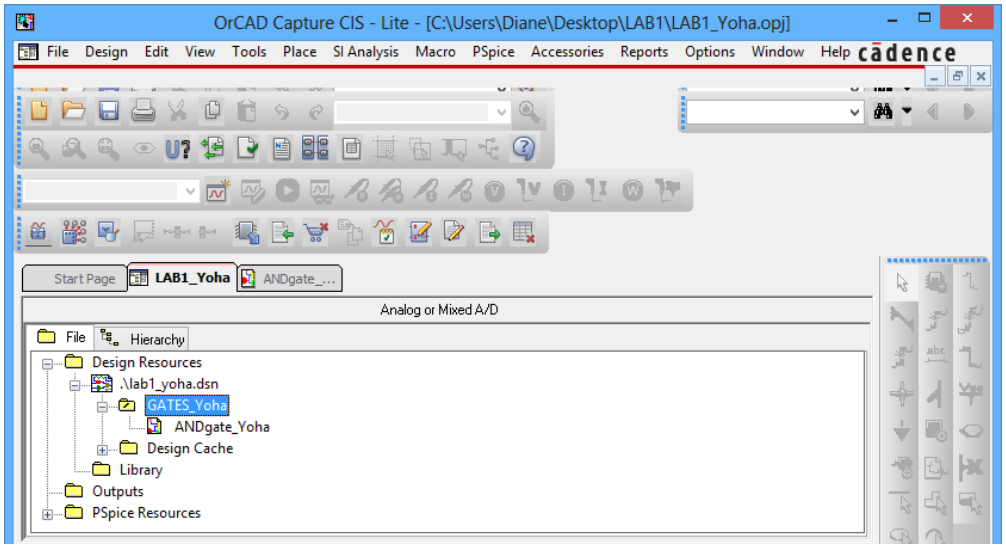

Figure 8: View after files have been renamed

At this point, you have successfully created your project and renamed the files associated with it. If you should accidently close your schematic, you can come back to this tab and reopen your working files. This hierarchy tab proves useful for rapidly opening files for editing.

Part 2: Creating the Logic Diagram.

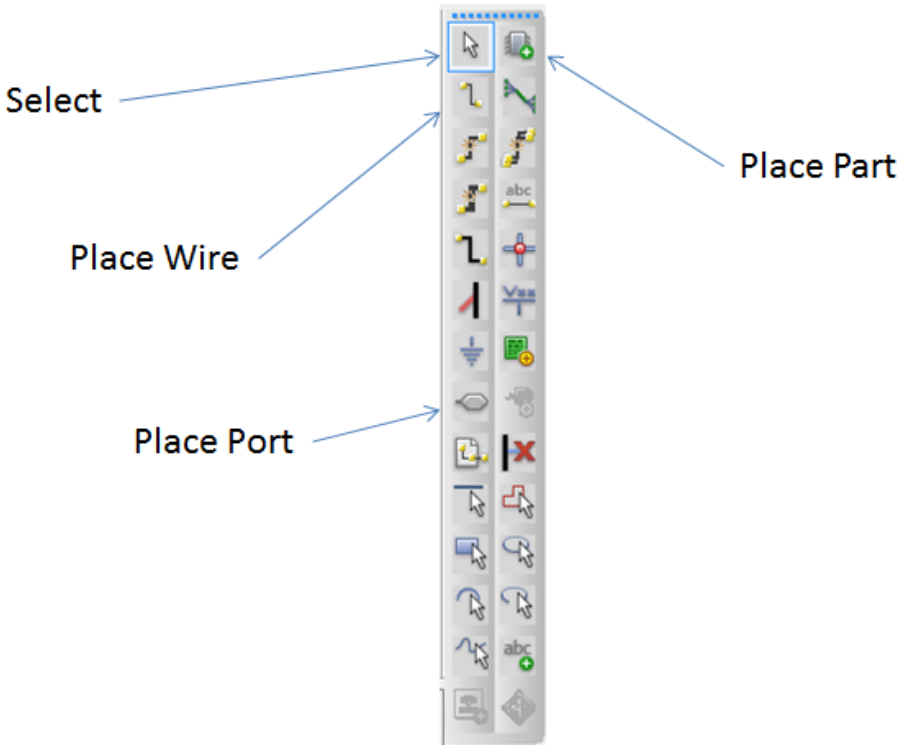

Figure 9: Drawing tools for this lab

1. Placing gates, wires and other necessary elements is fairly simple. You use the drawing tools on the right side of the screen. If this menu is not available, please let me know.

Place Part – this option opens a sub-menu which provides access to all the logic gates we will be using. In future labs, you will create your own parts and they will also be found here.

Select – selects either an object or a group of objects.

Place Wire – the tool used to draw wires to connect parts and parts to ports.

Place Port – This option opens a sub-menu when provides access to all the ports we will be using (inputs/outputs).

2. First let's place a part, in this case a gate. To do so you need to click on the tab corresponding to your drawing/schematic/ diagram (far right tab). Click on the Place Part symbol (shown above) and a new window appears.

If you do not see EVAL listed under the directories you will need to add that library. Do so by clicking on the Add library button (see figure 10). This will bring up the list of available libraries (figure 11) available to add to your project. Select **eval** – NOT EVALAA as this doesn't have the tools we need – and click OK. The Library will appear under Libraries and the Parts List section will be populated with the parts in this library.

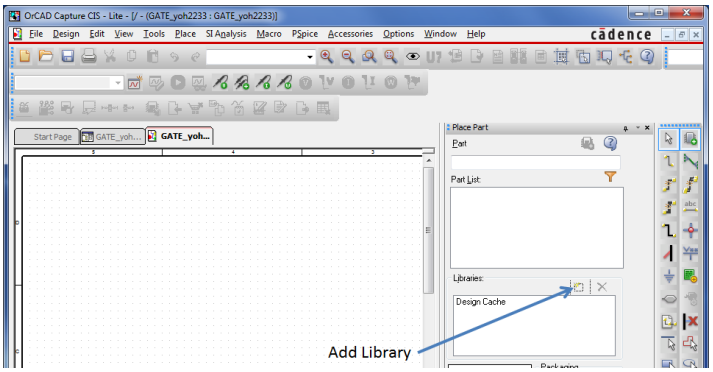

Figure 10: Add Library

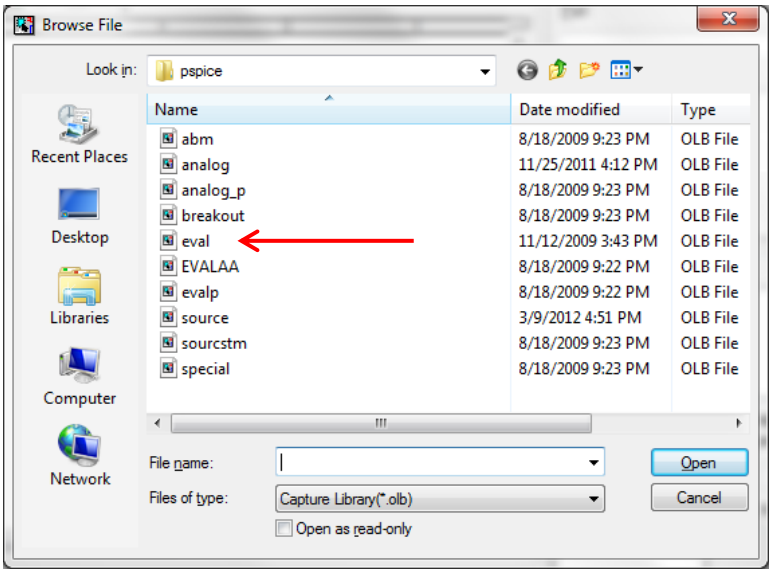

Figure 11: Add Library pop-up

3. The first gate you will add is an AND gate. Select gate 7408 by scrolling through the part list – this is a two input AND gate. Click the place part symbol (small IC chip with a green plus on it) in the Place Part window and place the AND gate in the center of your schematic. Avoid placing it too close to the edges as we need to have room to add other components. As soon as you have placed the gate hit escape. This ends the selection of the gate.

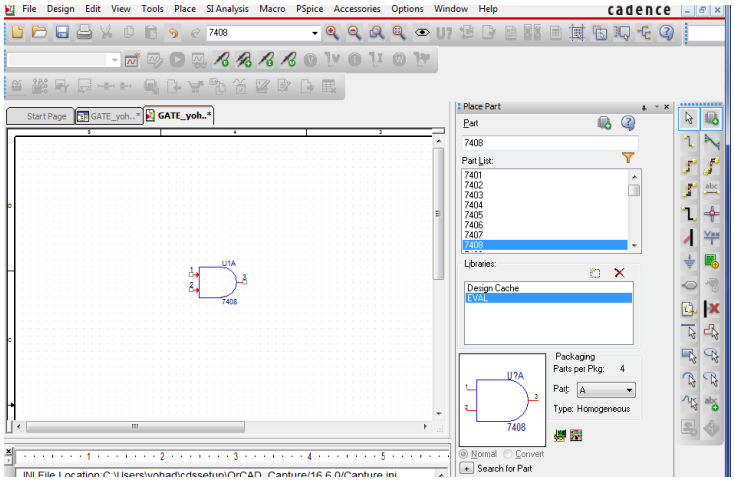

Figure 12: AND gate placed

4. Now we need to add wires and ports to the AND gate. Select Place Wire,  and draw wires connecting to both inputs and the output of the AND gate. It is important that you be sure to connect to the gate or you WILL have problems later. To end drawing a wire, double tap at the end of the wire. You can zoom in to be sure everything is connected.

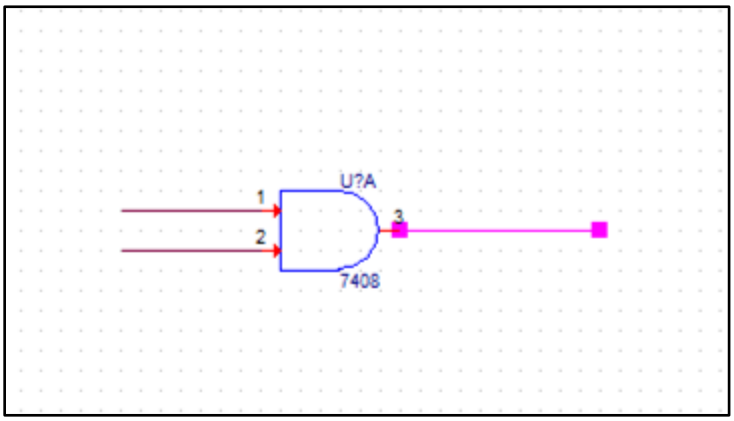

Figure 13: AND Gate with Wires

5. Now add ports to the wires we've just created. Click on Place Hierarchical Port and select **PORTLEFT-L** and connect it to the output of the AND gate. Be sure to hit escape when you are done to avoid having many ports you don't need. Note that a red dots show when you have made connection to the wire. This dot goes away when you have placed the port.

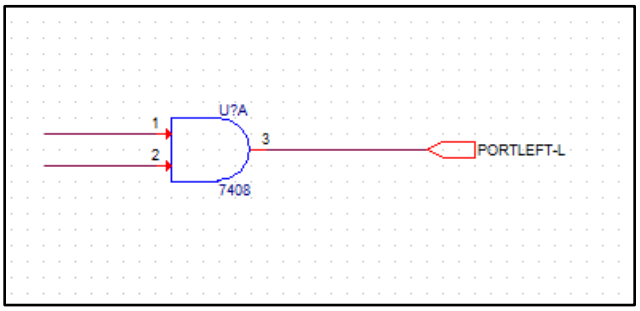

Figure 14: Port added to ouput

6. The next step is to apply a digital stimulation to the inputs. For this we need to add another library to the project. Click on Add Library and select sourcstm and hit OK. Select SOURCSTM and click on DigStim1. Place this on the inputs of the AND gate.

Double click on the top **implementation =** and set value equal to x. Also select **Do Not Display**. Click OK Repeat setting other value equal to y. This is very important. This setting must match a signal in the digital stimulus file. If you do not set this value, the simulation will not know what inputs to apply when you want to simulate your design. This is usually indicated by a double red line in the simulation. More on that later.

Then double click on the top DSTM1 and give it a value of **x**. Give the other input a value of **y**.

NOTE: There can be NO special characters (!, @, etc) or spaces in the naming of any port. The Underscore character may be used, but it is best just to alphanumeric characters.

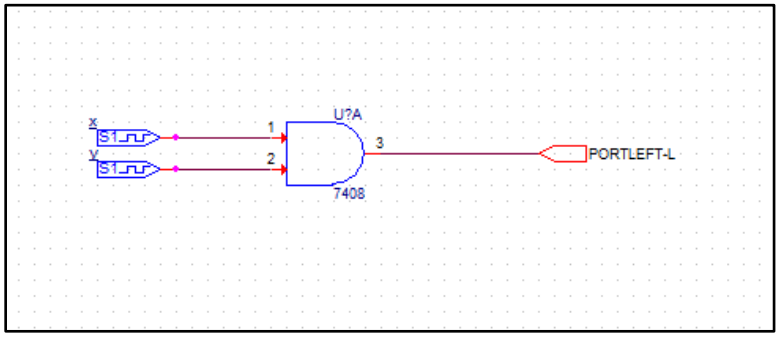

Figure 15: AND with the DigStim1 values renamed as required.

7. Double click on PORTLEFT-L (the name not the symbol) and give it a value of **ANDoutput**. Save your work.

You must rename all the ports to avoid conflicts in the simulation. This becomes more important as the designs become more complex and when you design your own parts.

8. Click on the hierarchical tab (it should be the middle one) and hit save again. The first save (previous step) saves your page, the second saves the project. If you hit save while in this view it will save everything.

9. Click ONCE on the .**dsn** file to highlight it. Go up to Tools on the menu bar and select Annotate. At this time just hit OK, for more complex designs you may have to change some of the options. We will be doing so in later labs. Annotate applies component numbers to your logic gates. Prior to Annotating the file your AND gate was labeled U?A. It should now be named U1A. Anytime you make a change to your design you should re-annotate your file.

10. A warning appears. Hit **yes** and then hit **OK**. Save your project.

Part 3: Simulating your Design

In order to simulate a design, you need to have a simulation profile. The simulation profile contains all the information needed to run your simulation.

1. On the menu bar select **PSpice -> New Simulation Profile**. Enter the name **ANDinput.** Be sure **none** is showing in the dropdown below Inherit From. Click **Create**. If nothing appears on the screen, look down on the taskbar and see if you have a flashing icon, if so click on it.

2. In the run to time box enter 10ms. This is the length of time for your simulation.

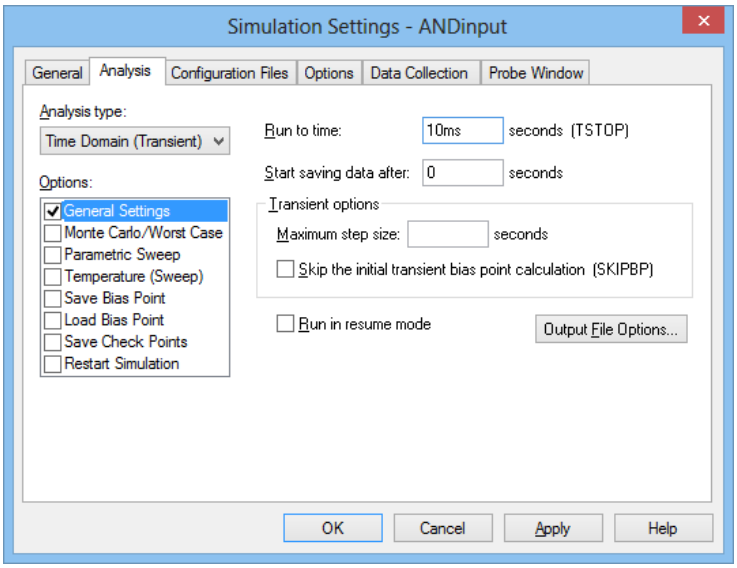

Figure 16: Simulation Settings

3. Select the Configuration Files tab, and browse to the .stl file you saved in your LAB_1 folder (in the prep work section of this lab). Click **Add to Design**. Click **OK**. Save your work. The input.stl file contains the information about the inputs you are applying to your design.

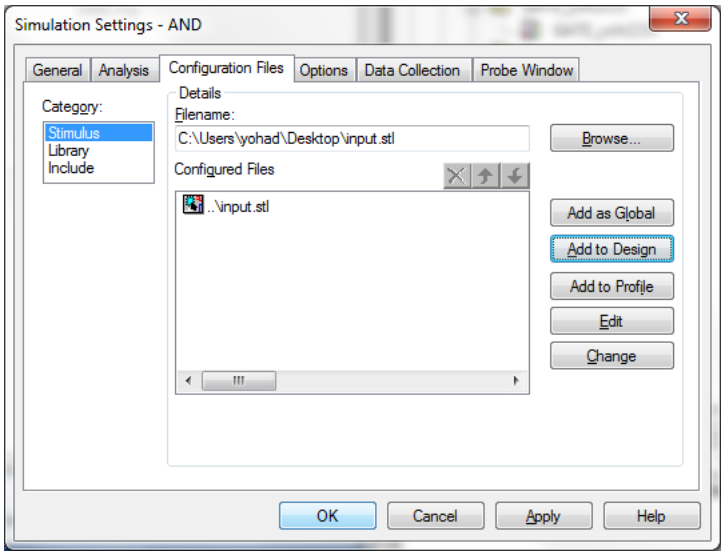

Figure 17: Configuration Tab (Simulation Settings)

4. On the hierarchical project tab, double click on input.stl under PSpice Resources->Stimulus Files. This brings up the Stimulus Editor window which contains all the inputs we need for this project. We are going to edit this file to meet our needs.

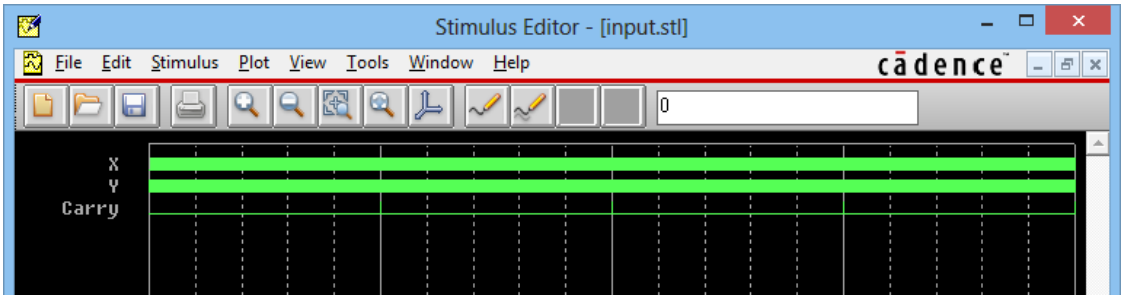

Figure 18: Stimulus Editor

First select CARRY, is should turn red. Select **Edit-> Delete**. This simulation does not require this input.

Now double click on x. Change the frequency to **1K** and hit **OK**. Double click on y and change the frequency to **500** and hit **OK**. Notice the difference between this picture and the previous one.

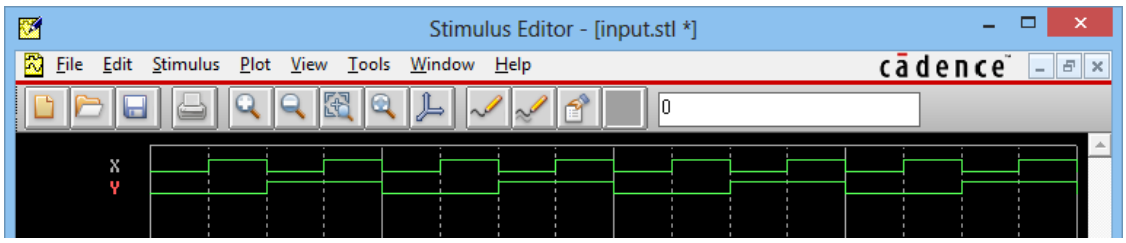

Figure 19: After changes

Click save in the Stimulus Editor and close this window. You can always access it again via the hierarchical tab.

5. We can now run our simulation. Click on PSpice-> Run. You will see that there is no output. Continue on.

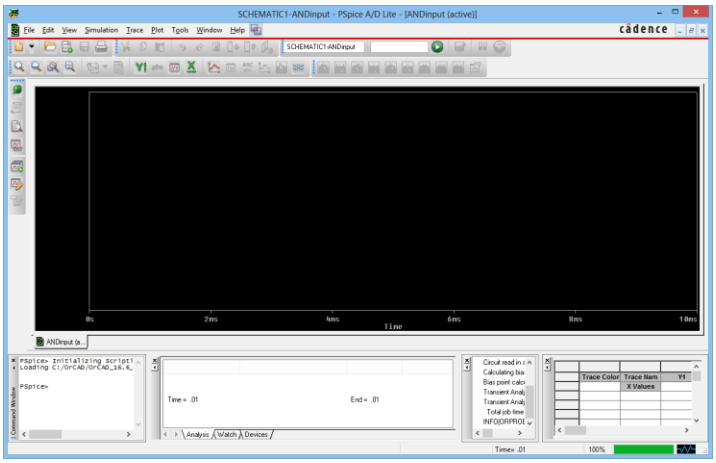

Figure 20: What happens when you forget something important.

6. In order to see the output of a simulation you MUST place markers on your diagram. These markers can go anywhere on your diagram (but must be connected to a wire) and are useful in troubleshooting more complex diagrams. This is a basic schematic so we will just put markers on the inputs and output of the AND gate.

7. Click on the schematic tab. At the top of the page should look something like figure 21. If you look closely, there are four symbols that look very much alike only with different letters. Click on the Probe (Marker) symbol with the V. This is a voltage marker and once placed on your diagram there will be a signal on the output corresponding to this marker. The markers can also be found under PSpice->Markers (figure 22).

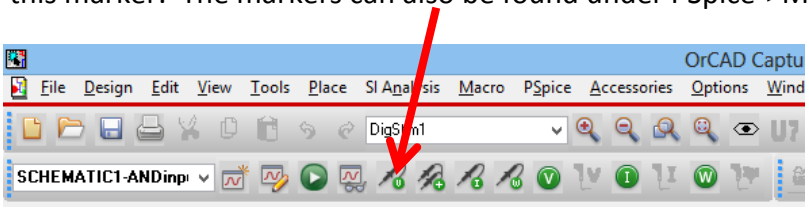

Figure 21: Menu Bar (Page view)

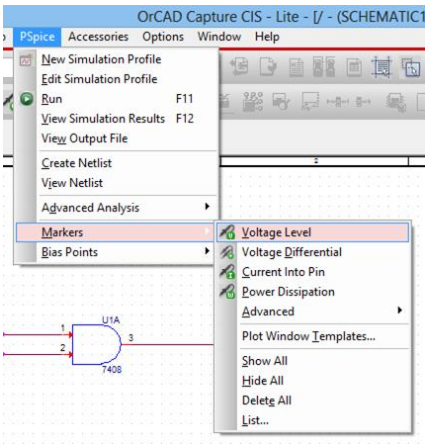

Figure 22: Another way to find the Markers

8. Select the Voltage Markers and place a marker at the two inputs and the output of the AND gate. Then run the simulation again. It is always best to place your markers in some logical order. Placing markers on the inputs and then the outputs makes the result of the simulation easier to read.

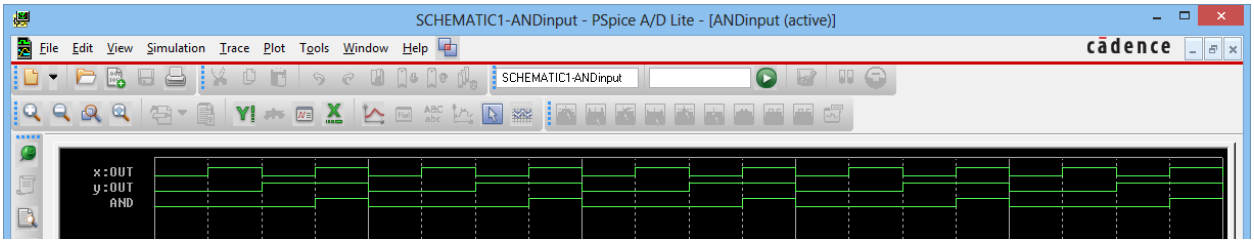

Figure 23: AND gate Simulation

Part 4: Assignment

1. Create a simulation for a two-input OR (part 7432), two-input NOR (7402) , two-input NAND (7400). It is recommended that you simply add these gates to the current page and apply the markers as needed when simulating the gates. NOTE: you may apply the same inputs to the **implementation =** of the port, but the port names must be unique (x1, x2, x3, etc).

2. Right click on your GATES_lastname folder in the hierarchy, select New Page, and name it **part2_lastname**. Create a simulation which applies an inverter (7404) to the output of an AND gate. Do the same thing to the output of an OR gate? Run this simulation.

Part 5: Deliverables

1. A printout of the design(s).

2. A printout of the corresponding simulations results.

3. Upload screenshots of the above printouts to Canvas.

4. A word or pdf document which answers the following questions. Please use complete sentences and don't forget to put your name on the documents. I do NOT need a printout of your document. At this point I don't expect screenshots in your document, but eventually that will be the case. If you wish to start now, that is fine. However, I still want screenshots uploaded to Canvas of any design and the resulting simulations.

Are the results of your simulations what you would expect?

What can you determine about a NAND and a NOR gate when you look at the results of your simulation?