CSCI-1510
Lab 3

Total Points: 100
Due: 3 April 2014

This lab has three (3) parts. The required deliverables are in Part 3. Please read the entire lab before starting.

Part 1: Adders

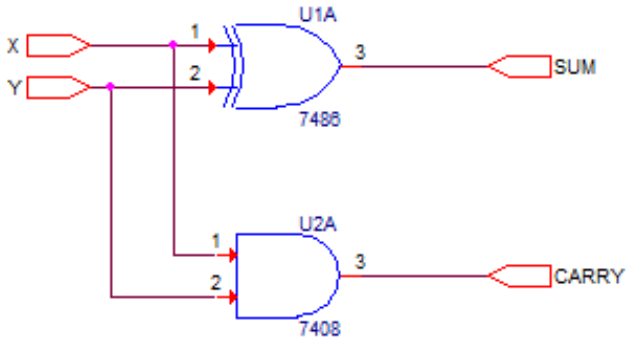
Half-Adder

1. Open a new project called Adders. Rename the Page and the Schematic "Half_Adder." This is an important step, don't skip it.

2. Create your half-adder. Name the upper input "X" and the lower input "Y." The outputs should be named "SUM" and "CARRY." **IMPORTANT: Use XOR 7486**

3. Place the ports. **DO NOT use DSTIM1 as the inputs for x and y.** Use PORTRIGHT-R. This port can be found in the same place as PORTLEFT-L. This is because you will be creating a user-defined part for the half adder later on.

4. SAVE YOUR DESIGN. **Do NOT simulate this design at this point!!!**



Creating a part.

You can generate a part for any circuit design you create. This increases the flexibility of the software and the simplicity of designs.

To generate a part from your design, complete the following steps.

1. In the Project Manager window, select the Half_Adder folder.

2. From the Tools Menu, (top menu bar), select Generate Part.

3. In the Generate Part dialog box which appears, specify the location of the design file that contains the circuit for which the part is to be made – adders.dsn

4. In the Netlist/source file type drop-down box, specify the source type as Capture Schematic/Design.

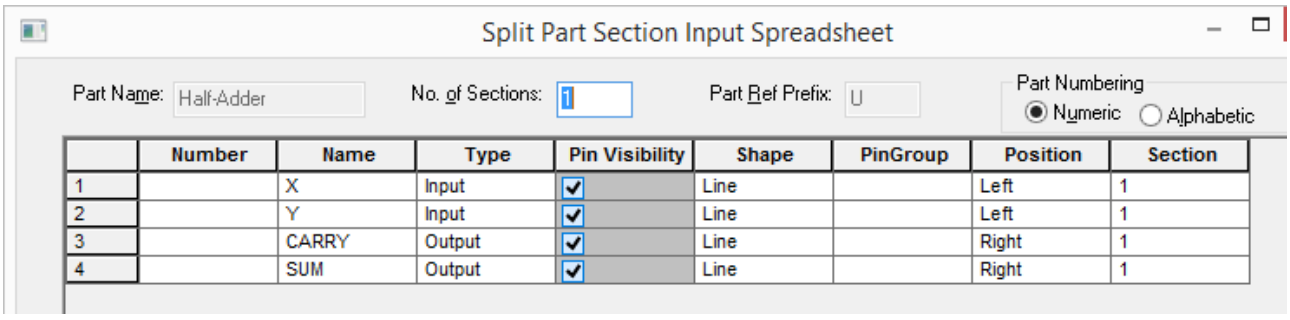
5. In the Part Name text box, specify Half_Adder.

6. The name and location of the library that will contain the created part is ….\adders.olb. If you are using a flash drive, the path should be changed appropriately.

7. Save the source schematic by selecting the Copy Schematic to library check box.

8. Be sure Create new part is selected.

9. To specify the schematic folder that contains the design for which the part is to be made, select Half_Adder from the Source Schematic name drop-down list box. Then click Save. You should see something like this.



	Number	Name	Type	Pin Visibility	Shape	PinGroup	Position	Section
1		X	Input	☑	Line		Left	1
2		Y	Input	☑	Line		Left	1
3		CARRY	Output	☑	Line		Right	1
4		SUM	Output	☑	Line		Right	1

Building a Full-Adder

1. In the Project Manager window, right-click on Adders.dsn and select New Schematic. Name it Full_Adder and click OK.

2. A folder named Full_Adder should appear below the Half-Adder folder.

3. Save the design.

4. Make the full adder circuit design as the root design, or the higher level hierarchical block. Right click on Full_Adder and select Make Root. The Full_Adder folder moves up and a forward slash appears in the folder.

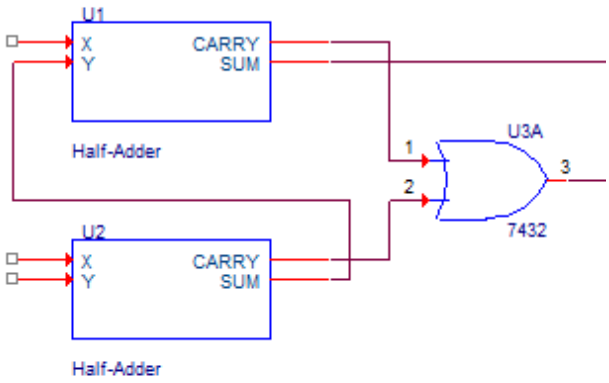
5. Right-click on Full_Adder and select New Page, specify the page name as Full_Adder and click OK. A new page, Full_Adder, gets added below the schematic folder Full_Adder

6. Open the Full_Adder page you just added to open it for editing.

7. In the place part menu, under libraries click on ADDERS. The part you made previously should be here.

8. Use the Half_Adder part you created and make a full adder.

9. Place an OR gate (7432) to the schematic. Then add the wires as shown in the figure below.



10. At this point you are ready to add the stimulus to the design. Add DigStim1, from the Part List, to the inputs on the left of the design. Remember to hit escape when done.

11. Change the **Implementation Value** of the three inputs to Carry, X, and Y, respectively.

12. Select the Place Port  button and add a port (PORTLEFT-L) to the output of the OR gate. Change the port name to CARRY_OUT. Also add a port for the SUM and rename it appropriately.

13. Save the design.

Annotate the design

This is different than the last lab so carefully follow all steps.

1. In the Project Manager window, select the .dsn file.
2. Choose Tools - Annotate.
3. In the Packaging tab of the Annotate dialog box, specify whether you want the complete design or only a part of the design to be updated. Select the Update entire design option.
4. In the Actions section, select the Incremental reference update option.
5. Select the Update Occurrences option.

Note: When you select the Update Occurrences option, you may receive a warning message. Ignore this message because for all complex hierarchical designs, the occurrence mode is the preferred mode. The Use instances option is shown as preferred because the project type is Analog or Mixed A/D.

6. For the rest of the options, accept default values and click OK to save your settings.

The Undo Warning message box appears.

7. Click Yes.

A message box stating that the annotation will be done appears.

8. Click OK.

Your design is annotated and saved. You can view the value of updated cross reference designators on the schematic page.

Please note that each time you make a change to parts/wires/components in a design you will need to re-annotate the design. If you have used a part you created you may need to update occurances. You definitely will if you change the part design and recreate the part.

Test Your Full Adder

1. To test your design, you will have to create a stimulus file with 3 inputs. You will need to ensure that whatever frequencies you select for your inputs, you cover all the possible combinations of the three inputs. Remember with 3 inputs there are $2^n = 8$ possible

combinations. It is strongly suggested that with each input you double the previous frequency to ensure you create all possible combinations of the inputs.

2. Once you have created your stimulus file, simulate your design.

Build a 2 bit adder.

1. Create a part for the Full-Adder. You will need to ensure that you replace the DigiStim inputs on the previous design with ports. **If you do not your design will not work right.**

2. Use your newly created part to create a 2 bit adder.

3. Simulate your design using the provided 2BitAdderTest.stl file.

Part 2: Decoders/Encoders

Create a new project for this part of the lab.

Decoder

1. Design and build a 2 to 4 Decoder.

2. Generate a part for your Decoder.

Encoder

1. Design and build a 4 to 2 Encoder

2. Generate a part for your Encoder.

Circuit

1. Using the parts you generated for the Decoder and the Encoder, create a circuit which encodes a signal. The encoded output should then be fed into your decoder. Simulate this circuit.

Comment:

You should be able to determine if you are getting the correct outputs. If you aren't then your design or stimulus file may need to be modified. There is no reason to lose points for an incorrect design.

<u>Red lines</u> on the simulation result – there is a problem with your input.

<u>Purple lines</u> – in general means you have selected an erroneous part. Try to continue to use the parts we have been using, even if this means you need to cascade gates (i.e. the 3 input and gate).

Part 3. Deliverables

Hardcopy

1. A print out of every schematic.

2. Documentation supporting your design of the Encoder and Decoder (i.e. the truth tables and Boolean Equations). Any other information you feel is needed related to your design decisions may be included here.

Uploaded to CANVAS

Please name your files in such a way that the name is descriptive of what part of the lab they pertain to. Example: Full_Adder_Circuit, Full_Adder_Stimulus, Full_Adder_Results. Files named 1 or part1 will not be accepted for full credit.

1. A screenshot of every schematic

2. Screenshot of the results of the simulations.

3. Screenshot of your simulation files.