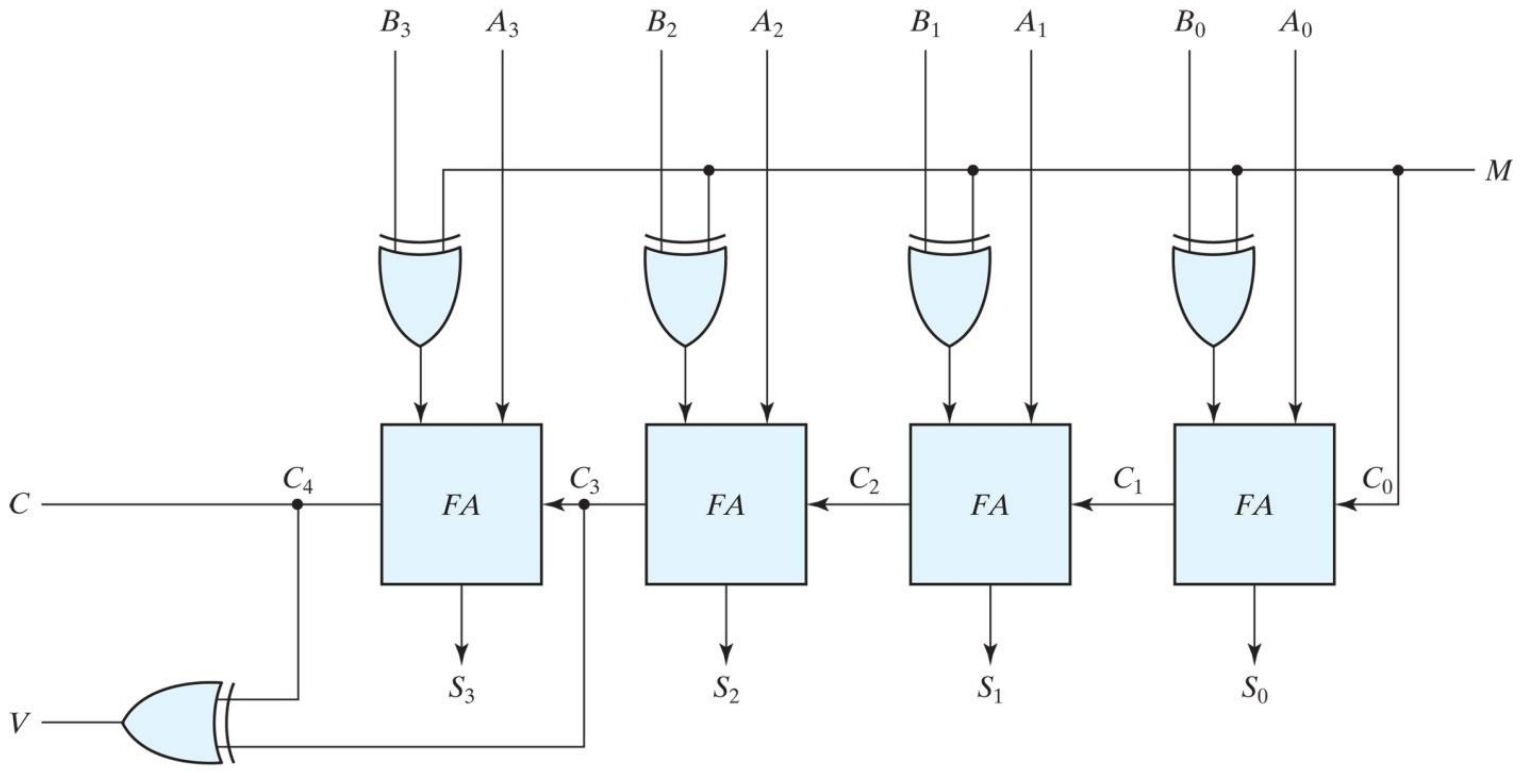
Chapter 4
part 3

If asked to design a circuit

- Where to start
  - Truth table – based on requirements/specs
  - Required outputs – based on a timeline
- Build circuit
- Test circuit
- Does the output match the specifications?
  - Yes – done
  - No - redesign

Review



Decoder

- n to m
- m a max of 2^n
- Only one output active at any given time
- Can have an **Enable** input

Encoder

- Maximum of 2^n inputs and n outputs.
- Output tells you which input line is active

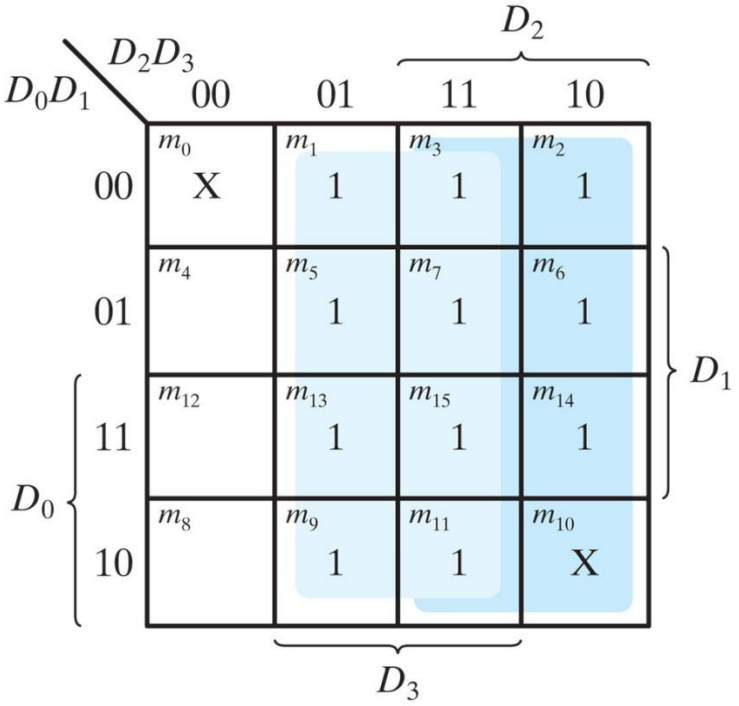
Priority Encoder

- Still Encodes
- If two or more inputs are active at any given time, the highest priority one gets attention.

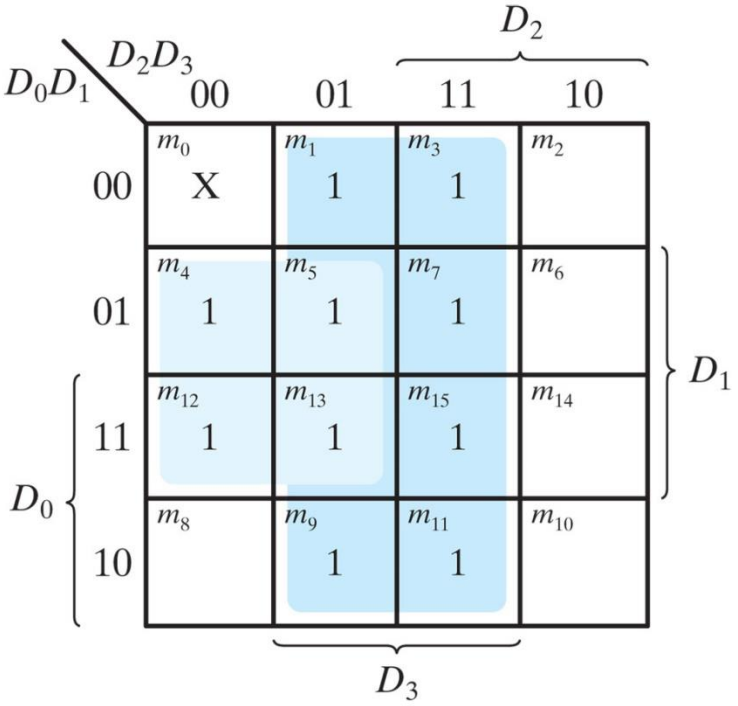
Table 4.8
Truth Table of a Priority Encoder

Inputs				Outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

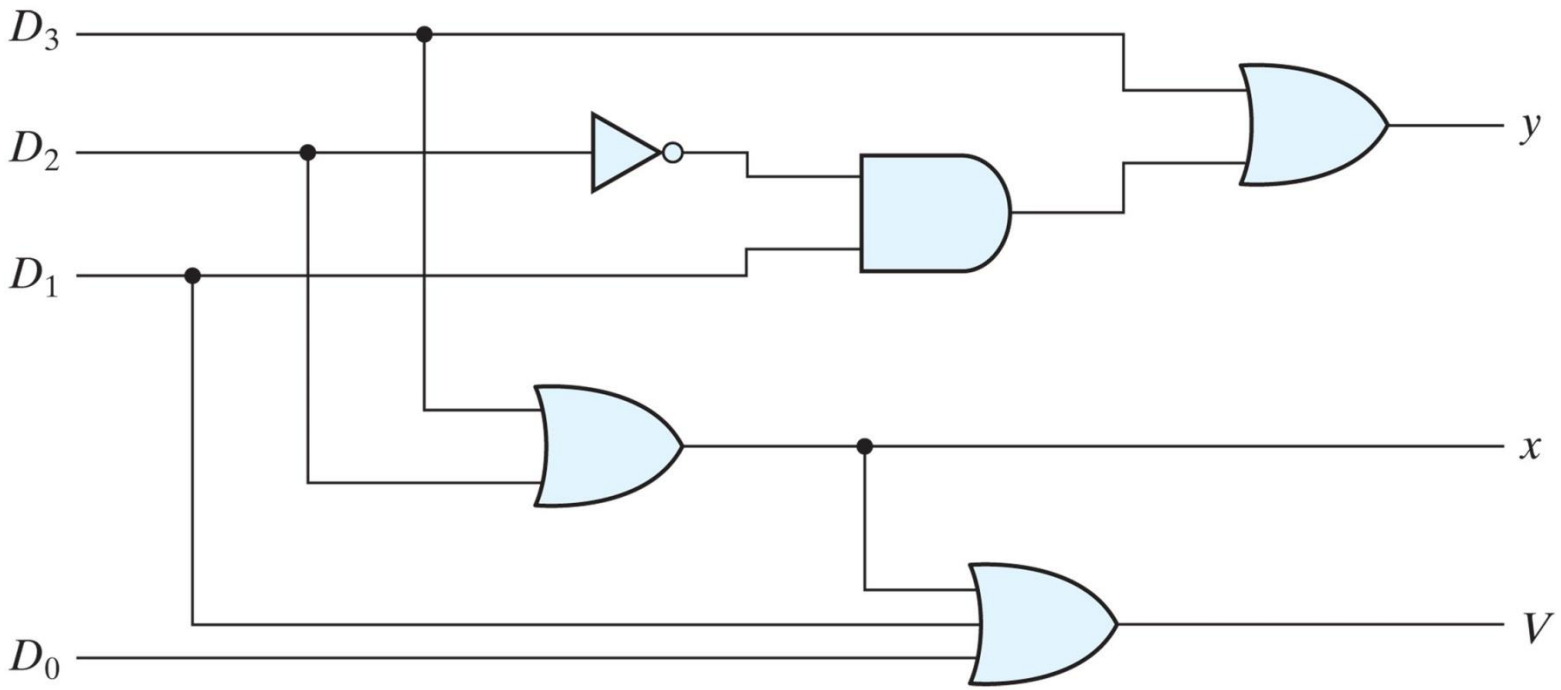
Maps for Priority Encoder



$x = D_2 + D_3$



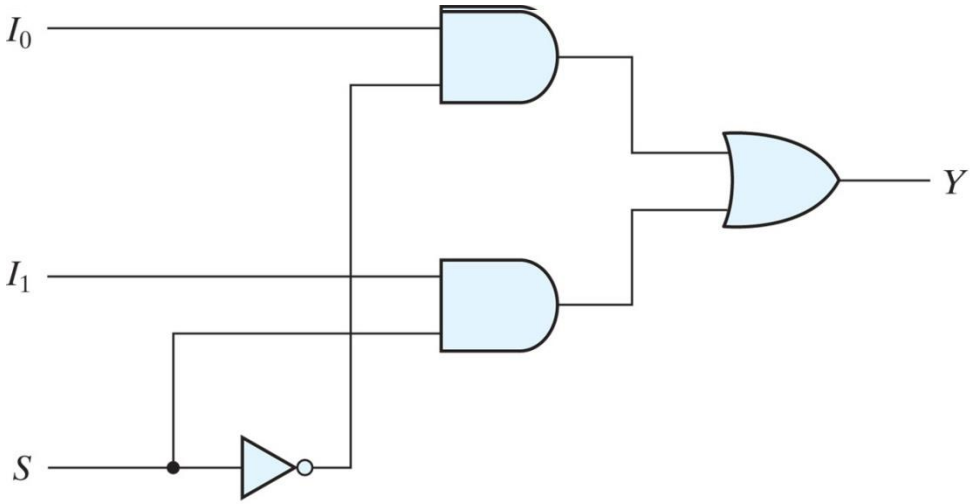
$y = D_3 + D_1D'_2$

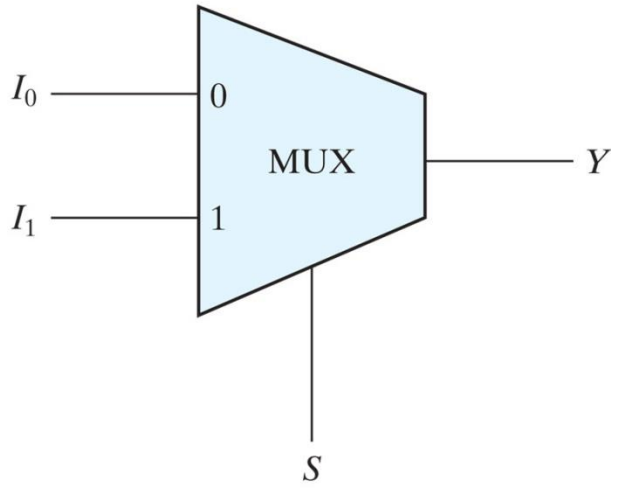

D_3
D_2
D_1
D_0
y
x
V

Multiplexer

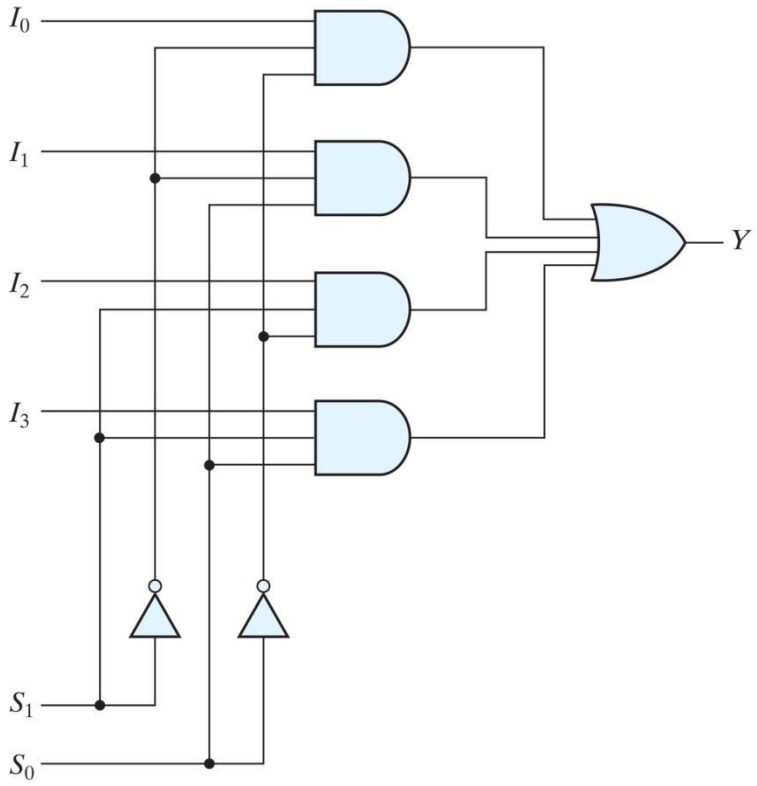
- Selects an input and directs it to the output.
- The selection is made via « selection lines »
  - 2^n input lines (normally)
  - n selection lines
  - 1 output

Basic Circuit and Logic Symbol



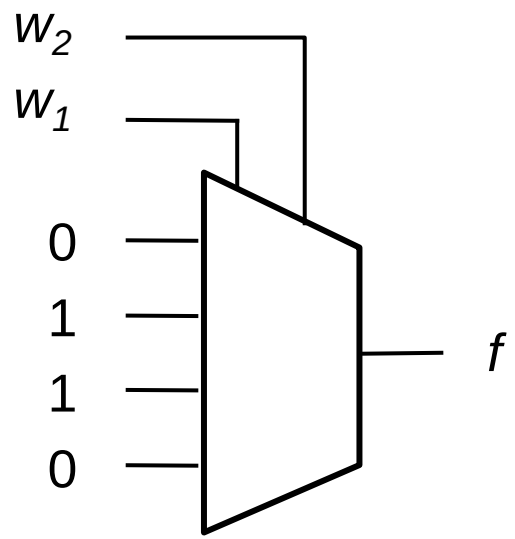


S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



Synthesis of a Logic Function

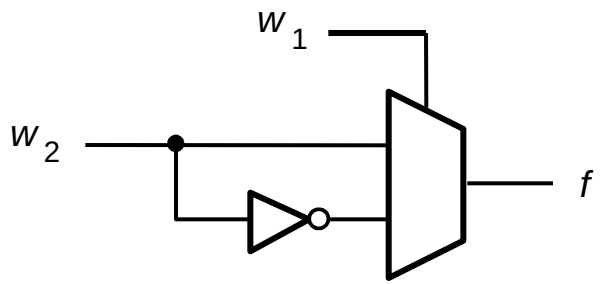
w_1	w_2	f
0	0	0
0	1	1
1	0	1
1	1	0



Synthesis of a Logic Function

w_1	w_2	f
0	0	0
0	1	1
1	0	1
1	1	0

w_1	f
0	w_2
1	$\bar{w}_2$



x	y	z	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

x	y	z	F	
0	0	0	0	$F = z$
0	0	1	1	
0	1	0	1	$F = z'$
0	1	1	0	
1	0	0	0	$F = 0$
1	0	1	0	
1	1	0	1	$F = 1$
1	1	1	1