Lab 2

Prep-work:

1. Create a folder called LAB_2. It can be on your desktop or on your flash drive.

Part 1: Creating a Stimulus File.

1. Read Creating your Stimulus File.pdf (available on Canvas). Don't do any of the steps yet, just read through the document.

2. Create a stimulus file for lab2. Name it **stimfile_lab2.stl**

You will need at least 3 inputs (x, y, z). Start with a clock frequency of 1khz and double it successively for each remaining input. You should end up with signals of 1khz, 2kz, and 4khz.

Note that you will need to add an input to this file for the last portion of the lab.

Part 2: Design

Note that for this lab, each design step requires you to add a schematic to your design. You do this by right-clicking on the .dsn and selecting New Schematic. Remember to rename your schematic to something appropriate for this lab. Ex. Lab2_1. You will have to add a page to the newly created schematic. Right-click on the schematic and make the appropriate selection. You need to rename your new page as well. Before simulating the new schematic/design you will need to make it root. Right click on the schematic and select make root. Don't forget to do this each time you wish to simulate a new design. For the pspice simulation profile to run, the desired schematic MUST be the root.

For each design you should be sure to create the most optimized circuit you can. This means you may have to do some algebraic manipulation.

1. Read Extension of Multiple Inputs (pg 62), if you haven't already.

2. Build a 3-input AND gate using 2-input AND (7408) gates. Be sure to consider gate delay as you design your circuit.

3. Design a majority circuit. This is a circuit which produces a 1 anytime there are more 1's than 0's on the inputs. Your circuit should have 3 inputs.

4. Design a circuit with output f and inputs x1, x0, y1, y0. Let X = x1, x0 be a number where the four possible values of X are 00, 01, 10, 11. Let Y = y1y0 be another number with the same possible values. Your circuit should output a 1 when the two numbers (X and Y) are equal, otherwise 0. (example x1x0 = 00 and y1y0 = 00 then X and Y are equal)

Note you will have to add an input to your .stl file. You may also choose to create a new .stl file. If you do, name it **stimfile_lab2_1.stl**

Part 3. Deliverables

For each design step (2 – 4) above.

Hardcopy.

1. Truth Table , Canonical Product of Sums, Canonical Sum of Products, and any algebraic manipulation done to achieve an optimized solution. Must be legible, but does not have to be typed.

2. Your Design

Screenshots

1. Your design

2. Simulation results and

3. Simulation input (.stl file)