CSCI-1510
Logic Design

Spring 2014

Diane Yoha

About me

- Master's Degree Electrical Engineering (Computer Emphasis)
- Contact me via
  - UCD email : diane.yoha@ucdenver.edu
  - Canvas
- Office hours : TBD

Preferred

Important Documents

- Syllabus
- Honor Code
  - In short, violations will **NOT** be tolerated.
- Academic Calendar

- All of the these are available on Canvas.

Canvas

- Does everyone have access?
- Announcements
  - Check Often – Particularly before class
- Modules
  - Course notes, powerpoints, info, homework, etc.
- Grades
  - Be sure to double check your grades when they are posted.
  - Keep all graded material until the end of the semester

Lab/Classroom Policies

- No Food
- No Drink
- No Music
- Be courteous to your classmates

Homework Policies

- Homework is due at the beginning of class on the due date.
- **Homework will not be accepted late**
- Homework must be legible. E-versions of the homework are acceptable only on a case by case basis and **with prior arrangement.**

Homework Policies

- You must show your work. If you do not show your work, you will **not** receive credit for the problem.
- You may work together on the homework however each student is responsible for his or her own work.

Homework Format

- Homework will have your full name, student ID, section number and assignment number clearly marked in the upper right corner on every page.
  - NOTE: It does not need to be typed.
- Homework shall be stapled together. Not clipped, not folded - STAPLED.

Lab Assignments

- Labs will be turned in BOTH on paper and e-version upload to canvas.
- You will be given a list of deliverables with each lab. Failure to turn-in all deliverables will result in a reduction of your grade.
- Some labs will require a lab report.
  - Format will be provided.

Expected Knowledge at Course Completion

- Able to convert from/to binary and hexadecimal numbers.
- Ability to read/understand basic combinational and sequential logic diagrams.
- Familiarity with computer aided design tools.
- Familiarity with the design and implementation of Algorithmic state machines.

Questions?