ECE 304

Design & Analysis of a 4-input Digital Multiplexor

Abstract:

The purpose of this lab is to design, test, and find propagation delays for the gates in a 4-input digital MUX. To form the MUX we need to build 3 and 4-input NAND gates, as well as use our inverter from lab 1. For the 3-input NAND we size the PMOS 2*(120nm) and NMOS 3*(120nm) in order to satisfy equal resistances for equal pull-up/pull-down strength. The rising edge and falling edge propagation delays were found to be 11.13 ps and 16.33 ps respectively. For the 4-input NAND we size the PMOS 2*(120nm) and NMOS 4*(120nm). The propagation delays for the rising/falling edge here are 14.66 ps and 23.77 respectively. Finally we construct the MUX shown in **Figure 4.** The propagation delays for the rising/falling edge of each input gate is shown in **Table 1.**

Design:

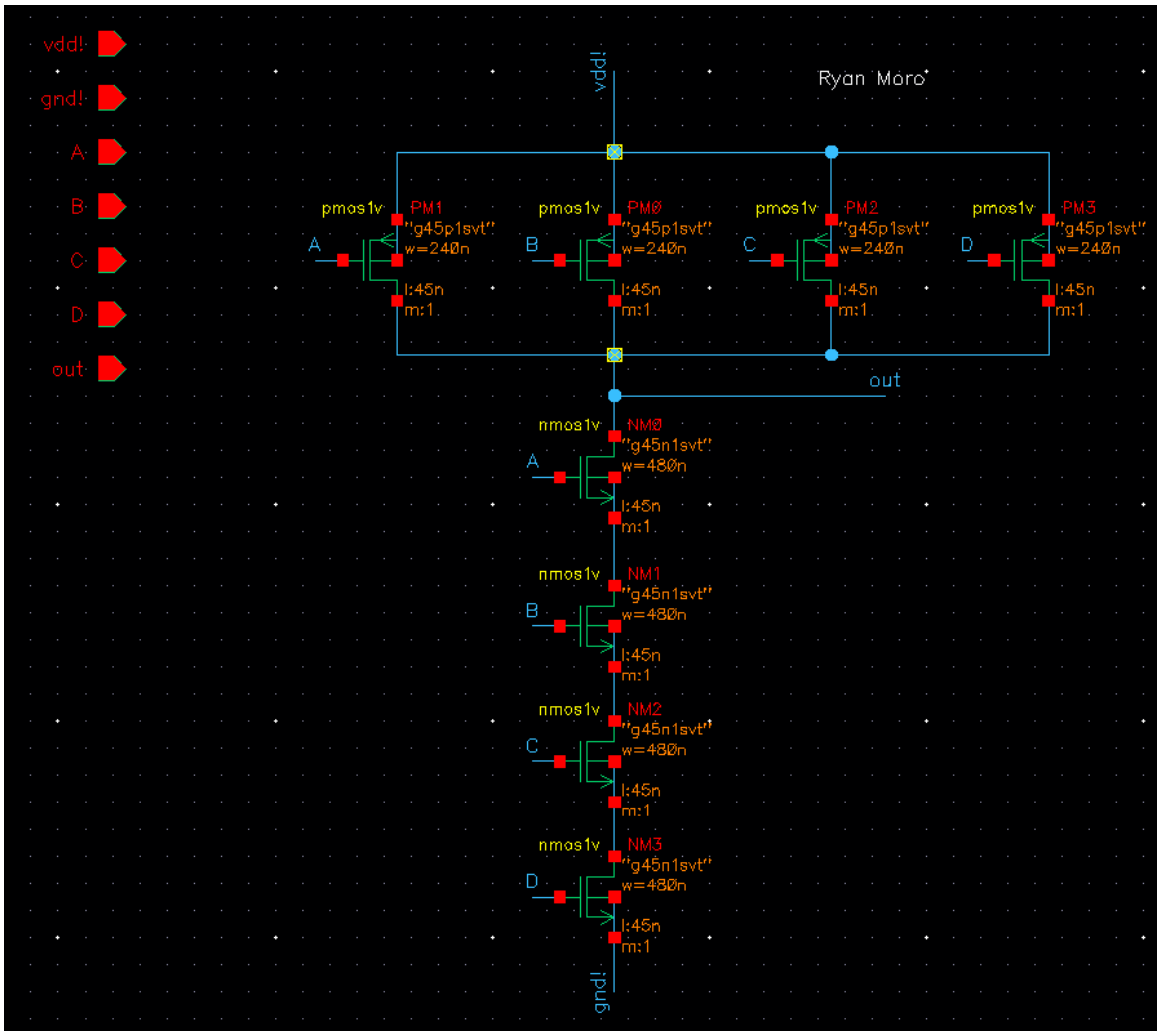


Figure 1 - 4-input NAND schematic

Since $\mu_n = 2\mu_p$, each PMOS has equivalent resistance of 2*R to equalize base current. With 4 active NMOS but only a single PMOS path at a time we size the transistors as shown below to equalize the resistances for the pull-up and pull-down networks. Resistance scales inversely with size so doubling the size reduces the resistance by a half ($I \propto \mu W/L$).

PMOS width = 2*(120nm) = 240nm -> 2R/2, NMOS 4*(120nm) = 480 nm -> 4R/4

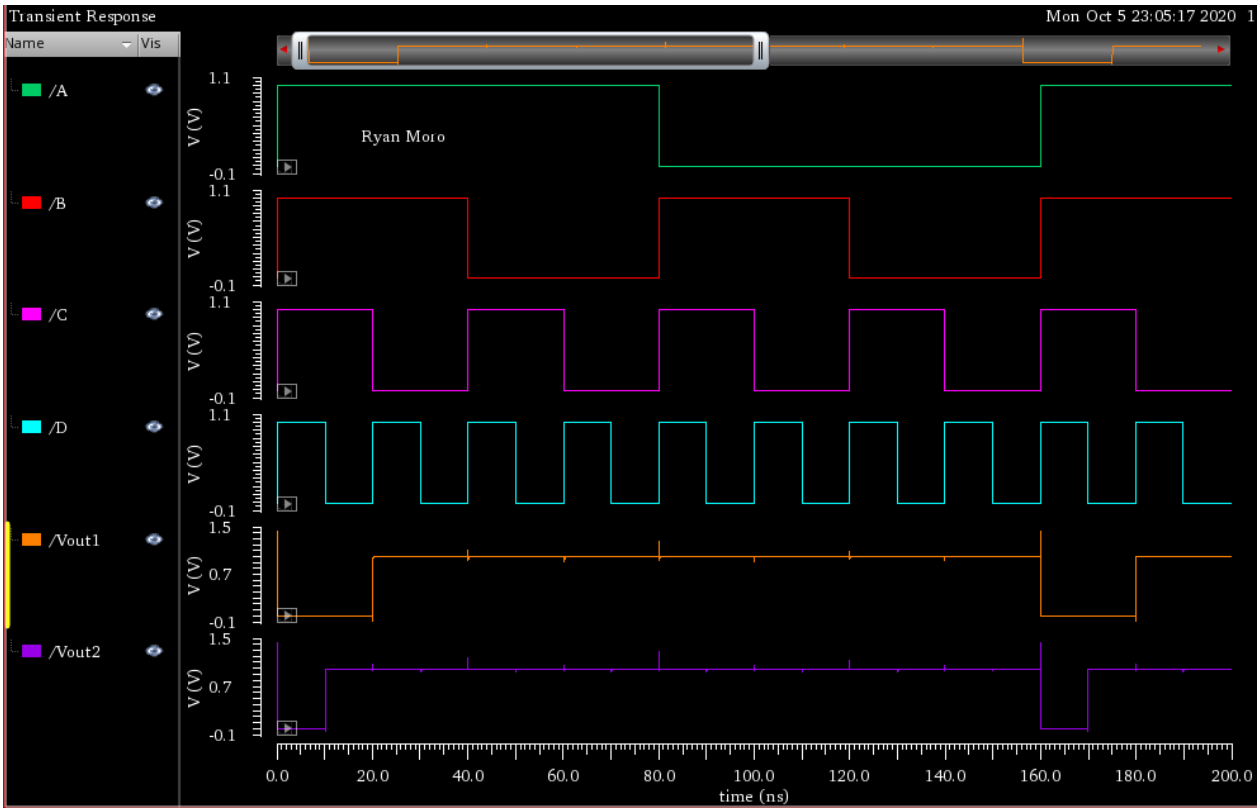


Figure 2 - Testbench plot for NAND gates

Vout1 - 3 input NAND

Vout2 - 4 input NAND

y = 5.0E-1V

/A	/B	/C	/D	/Vout1	/Vout2
500.0fs	500.0fs	500.0fs	500.0fs	18.451496ps	27.415179ps
80.0015ns	40.0015ns	20.0015ns	10.0015ns	20.011627ns	10.016166ns
160.0005ns	80.0005ns	40.0005ns	20.0005ns	160.01683ns	160.02426ns
	120.0015ns	60.0015ns	30.0015ns	180.01163ns	170.01615ns

Figure 3 - Horizontal marker table for Y = 0.5V

Input	Voltage 1	Voltage 2	Rise time	Fall time	Pulse width	Period
A	0	1.0	1p	1p	80n	160n
B	0	1.0	1p	1p	40n	80n
C	0	1.0	1p	1p	20n	40n
D	0	1.0	1p	1p	10n	20n

Figure 3.1 - NAND input vpulse parameters

Propagation delays

NAND3

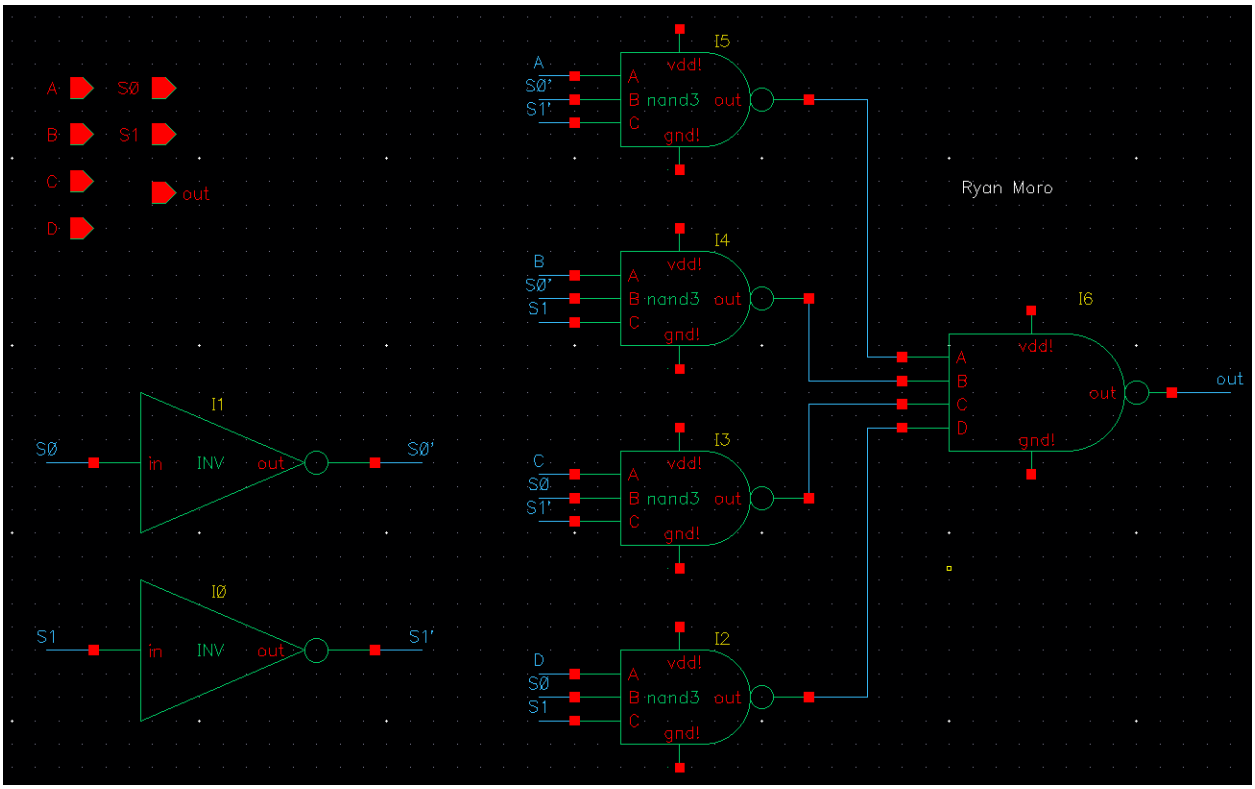
Rising edge: Vout1_2 - D_3 = 20.011627 ns - 20.0005 ns = 11.13 ps

Falling edge: Vout1_3 - A_3 = 160.01683 ns - 160.0005 ns = 16.33 ps

NAND4

Rising edge: Vout2_2 - D_2 = 10.016166 ns - 10.0015 ns = 14.66 ps

Falling edge: Vout2_3 - A_3 = 160.02426 ns - 160.0005 ns = 23.77 ps



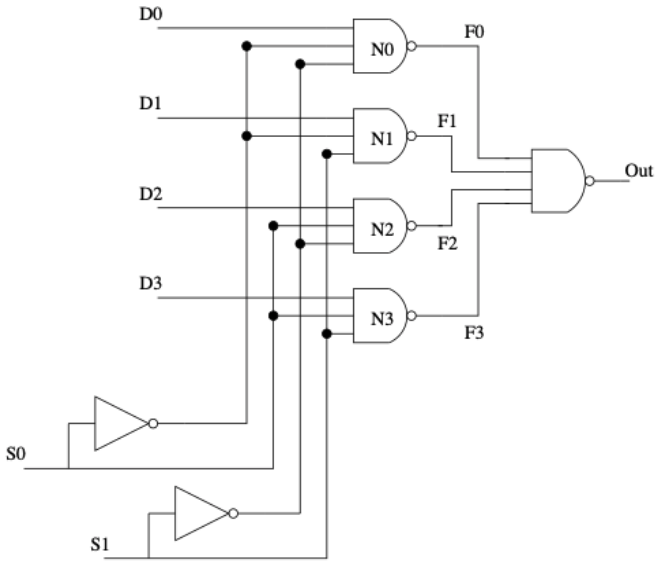


Figure 4 - MUX schematics

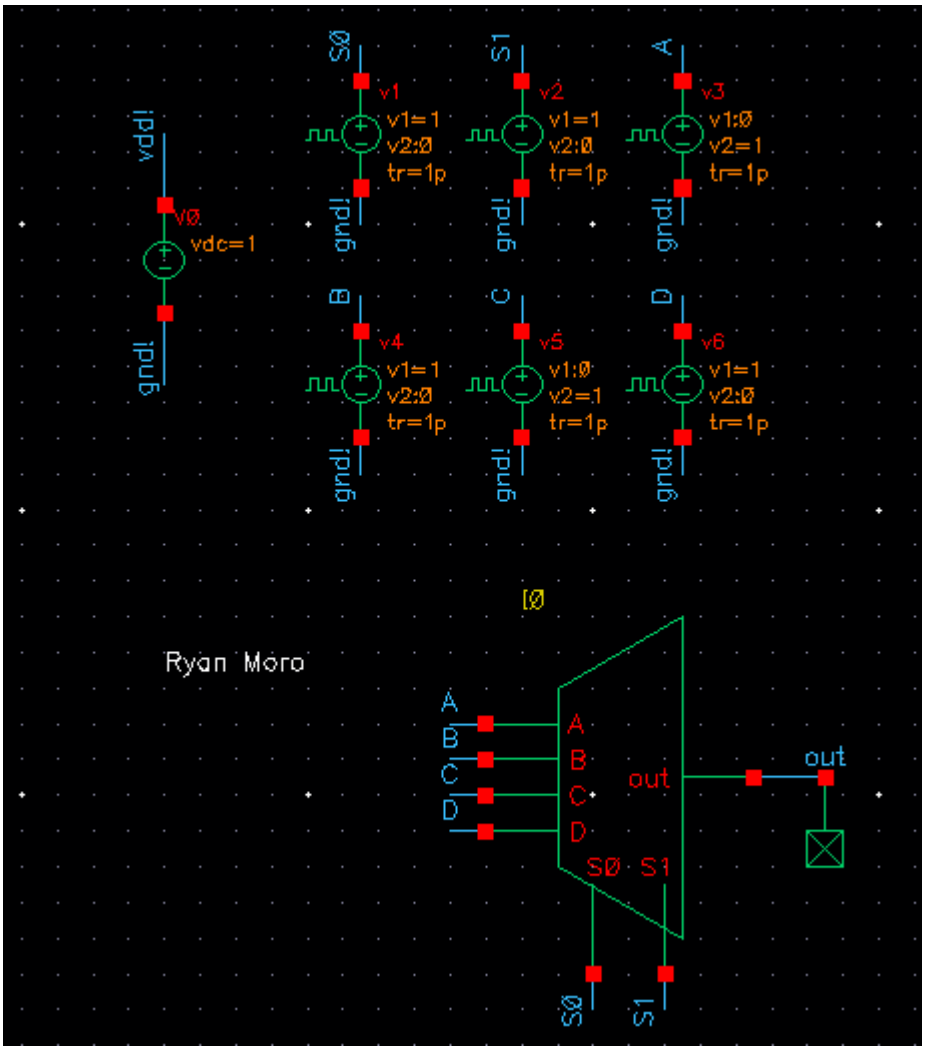


Figure 5 - MUX testbench schematic

Input	Voltage 1	Voltage 2	Delay time	Rise time	Fall time	Pulse width	Period
S0	1.0	0	-5n	1p	1p	40n	80n
S1	1.0	0	-5n	1p	1p	20n	40n
A	0	1.0	0n	1p	1p	10n	80n
B	1.0	0	20n	1p	1p	10n	80n
C	0	1.0	40n	1p	1p	10n	80n
D	1.0	0	60n	1p	1p	10n	80n

Figure 5.1 - MUX simulation input parameters

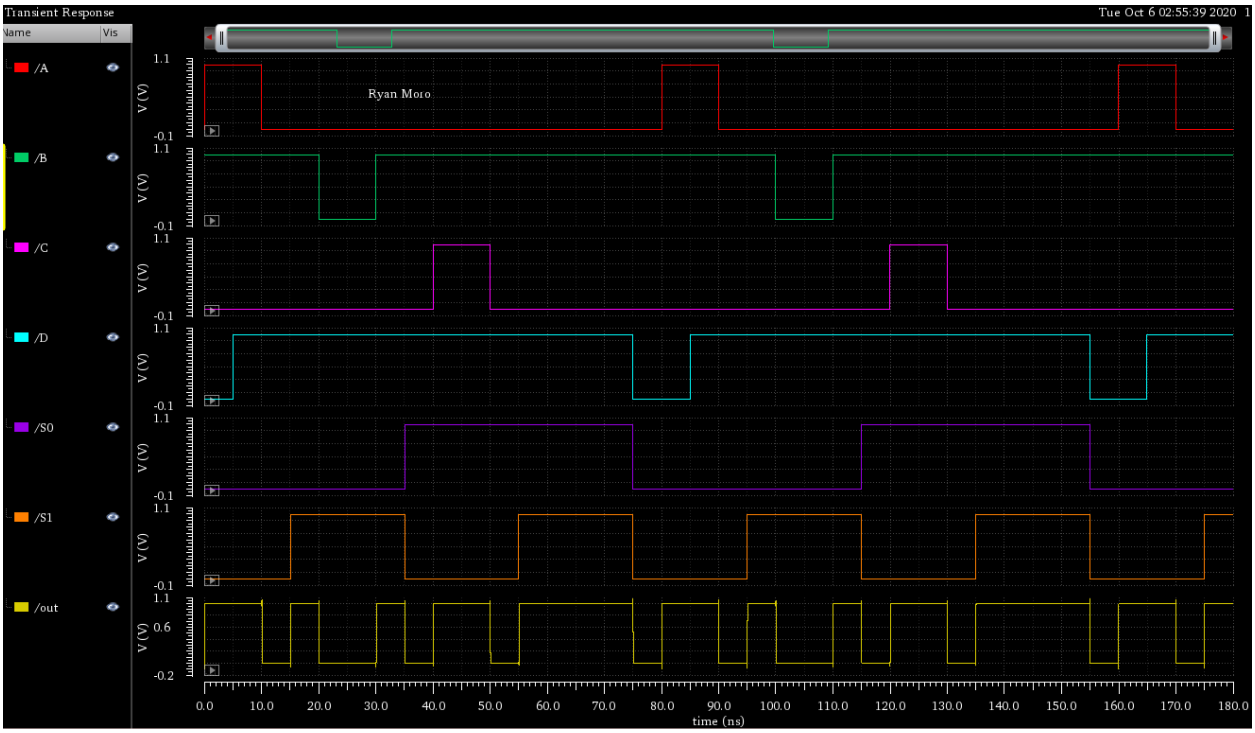


Figure 6 - MUX testbench plot

Mux Behavior

D0	D1	D2	D3	S0	S1	Out
0	X	X	X	0	0	0
1	X	X	X	0	0	1
X	0	X	X	0	1	0
X	1	X	X	0	1	1
X	X	0	X	1	0	0
X	X	1	X	1	0	1
X	X	X	0	1	1	0
X	X	X	1	1	1	1

Table 1 - Propagation delays

D0: Rising edge: 35.17932 ps - 500.0 fs = 34.68 ps
Falling edge: 10.03042 ns - 10.0015 ns = 28.92 ps

D1: Rising edge: 30.03883 ns - 30.0015 ns = 37.33 ps
Falling edge: 20.03418 ns - 20.0005 ns = 33.69 ps

D2: Rising edge: 40.03987 ns - 40.0005 ns = 39.37 ps
Falling edge: 50.03837 ns - 50.0015 ns = 36.87 ps

D3: Rising edge: 5.041911 ns - 5.0015 ns = 40.41 ps
Falling edge: 75.04021 ns - 75.0005 ns = 39.7 ps

y = 5.0E-1V

/A	/B	/C	/D	/S0	/S1	/out
500.0fs	20.0005ns	40.0005ns	5.0015ns	35.0015ns	15.0015ns	35.17932ps
10.0015ns	30.0015ns	50.0015ns	75.0005ns	75.0005ns	35.0005ns	10.03042ns
80.0005ns	100.0005ns	120.0005ns	85.0015ns	115.0015ns	55.0015ns	15.04361ns
90.0015ns	110.0015ns	130.0015ns	155.0005ns	155.0005ns	75.0005ns	20.03418ns
160.0005ns			165.0015ns		95.0015ns	30.03883ns
170.0015ns					115.0005ns	35.03763ns
					135.0015ns	40.03987ns
					155.0005ns	50.03837ns
					175.0015ns	55.04465ns

Figure 7 - Horizontal marker table for original plot.

Propagation delays for rising/falling edges of D0,D1,D2 all appear here.

y = 5.0E-1V

/A	/B	/C	/D	/S0	/S1	/out
500.0fs	20.0005ns	40.0005ns	5.0015ns	35.0015ns	15.0015ns	5.041911ns
10.0015ns	30.0015ns	50.0015ns	75.0005ns	75.0005ns	35.0005ns	75.04021ns
80.0005ns	100.0005ns	120.0005ns	85.0015ns	115.0015ns	55.0015ns	85.04192ns
90.0015ns	110.0015ns	130.0015ns	155.0005ns	155.0005ns	75.0005ns	155.0402ns
160.0005ns			165.0015ns		95.0015ns	165.0419ns

Figure 7 - Horizontal marker table for S0,S1 set to vdd!

Shows propagation delays for rising/falling edge of D3

Questions:

1) Why do we want pull-up and pull-down networks in our gates to have equal strength?

Since the mobility of holes in PMOS is half that of electrons in NMOS we can correct the pull-up/pull-down current to be the same by sizing the transistors so that the resistances of each network are equivalent. The result is that the pull-up response and pull-down response times are the same.

2) Similar as the 2nd question of the prelab, please size the transistors of a n-input complementary logic NAND gate for equal pull-up and pull-down resistance, assuming μn = 2μp.

Pmos width = 240nm

Nmos width = 120nm*n

3) How does the resistance and capacitance of a transistor change as it's width changes?

For a fixed length - R ~ 1/W, C ~ W