ECE (302) Lab #2
(Transistor amplifier)

Abstract

The purpose of this lab is to design and build a transistor amplifier. The amplifier should have a mid-band voltage gain of 12 V/V with an error of ± 5%. It should have a maximum voltage swing of 10 V without any clipping and an input impedance greater than 10 kOhm. The amplifier will be connected to a 1200:8 transformer, which is then connected to a speaker. A dual rail ± 10 V power source will power the amplifier. Due to these design specifications, two different amplifiers were designed, then coupled together. A common collector was chosen to support the high input impedance while a common emitter was chosen to support the medium output voltage needed. The signal source for the circuit produced a 2kHz signal with an output resistance of 50 Ohm. After testing, it was found that the voltage gain was 13.6 V/V and the input resistance was 10.3 kOhm. When changing the frequency of the signal source, it was found that the sound cut off at 27 kHz. Since the amplifier is a mid-band, it would stop all high and low frequencies from passing through. Also, it was found that if the input impedance is raised, the sound from the speaker will decrease.

Objectives

The objective of this lab was to design, test and build a BJT voltage amplifier. The amplifier should have a mid-band voltage gain of 12 V/V with an error of ± 5%, when working at a frequency of 2 kHz. The amplifier should also have an input impedance that is greater than 10 kOhm and a maximum voltage swing of 10 Vpp without any clipping. The midband frequency load of the amplifier has to be 1200 Ohm. This is because the amplifier will be connected to an 8Ohm speaker across a 1200:8 Ohm impedance transformer.

Design

For the design of the transistor amplifier, two different amplifiers, each one full filling different design specifications, were connected together to create the final amplifier. This was then connected to the transformer, then to the speaker. The two amplifiers were also connected to a dual rail ± 10 V power source. An entire block diagram can be seen in Figure 4.

The two different amplifiers were a common collector and a common emitter amplifier. From the specifications, the amplifier needed a high input impedance and a medium output impedance. The amplifier was also designed to have a maximum power transfer. This means the output impedance is equal to the load impedance. A common collector amplifier was chosen to fulfill the high input impedance and a common emitter was chosen to fulfill the medium output impedance specifications. In Figure 3 the circuit of just the amplifiers can be seen. The common collector was connected to the common emitter, which was then connected to the transformer, then the speaker. The common emitter was designed and built first though because the load of the amplifier must be known to design it and due to the design specifications, the load of the CE must be 1.2 kOhm. After the CE was built, the input impedance can be measured, which means the load of the CC will then be known.

Part 1 – Common Emitter

For the first part of the lab, a common emitter amplifier was designed and built. The CE amplifier would be the second stage of the entire amplifier circuit. A common emitter was chosen because it fulfilled the requirements of the circuit. The output impedance (medium) was the best choice for the load and provides the voltage gain specifications.

The design for the CE amplifier can be seen in Figure 1. This amplifier uses an npn transistor. To create a maximum power transfer the value $R_c = R_L$ with R_L being 1.2 kOhm from the specifications. To find the other values, various equations were used:

$$A_v = 13\frac{V}{V} = \frac{R_c||R_L}{r_e + R_e} \quad (1)$$

$$r_e = \frac{V_T}{I_E} \quad (2)$$

$$\alpha_F = \frac{\beta_F}{\beta_F + 1} \quad (3)$$

$$I_c = \frac{10}{R_c} \quad (4)$$

$$I_E = \frac{I_c}{\alpha_F} \quad (5)$$

$$I_{bias} = (\frac{1}{10})I_c \quad (6)$$

$$-10 + I_E R_E + 0.7 = V_B \quad (7)$$

$$10 - V_B = I_{bias}R_{B1} \quad (8)$$

$$-10 - V_B = -I_{bias}R_{B2} \quad (9)$$

Substituting in values of $\beta_F = 100$, it was found through equation 4 and 6 that $I_c = 8.33\ mA$ and $I_{bias} = 0.833\ mA$. From those values and equations 3 and 5, that $I_E = 8.41\ mA$. Which means that $r_e = 2.97\ Ohm$. Using this value, plus equation 1, gave $R_e = 43.18\ Ohm$. For R_{B1} and R_{B2}, equations 7, 8 and 9 were used. The results of these were $R_{B1} = 22\ kOhm$ and $R_{B2} = 1.3\ kOhm$.

Using those equations, all the values are known for the CE amplifier. When building the amplifier, originally, all the capacitors were left out. The transistor was placed, then from the emitter point, a 22 kOhm resistor (R_e) was connected to it, which was then connected to the -10 V rail. From the collector point on the transistor, there was a 1.2 kOhm resistor (R_c) connected, which was then connected to the 10 V rail. Also from the collector, there was the load resistor, 1.2 kOhm, connected in parallel with the R_c resistor. In Figure 1 there is also a 10 nF capacitor in series with the load resistor. This was originally left out to test if the transistor was in saturation. In the final testing and design, the capacitors were put back in. From the base point in the transistor, a 22 kOhm (R_{B1}) was connected to the 10 V rail while a 1.3 kOhm (R_{B2}) was connected in parallel with that to the -10 V rail. The other 10 nF capacitor and 2kHz source and 50 Ohm resistor seen in Figure 1 were included in the testing of the CE amplifier, then removed once the second amplifier in Part 2 was added.

Part 2 – Common Collector

For the second part of the lab, a common emitter amplifier was designed and built for the second stage of the entire amplifier circuit. A common collector was chosen because it will let us meet the input impedance requirements.

The design for the CE amplifier can be seen in Figure 2. This also uses an npn transistor. The maximum voltage swing is achieved when DC voltage on emitter is in the middle between V_- and V_+. We need to choose an R_E so that he current on the CC load doesn't exceed R_E DC current. We already have found V_E to be -10.1 V so we can get R_E, V_B, R_1 and R_2 from the following equations.

$$A_v = \frac{R_E||R_L}{r_e + R_e||R_L} = 1 \tag{1}$$

$$i_{c-peak}|_{CE} = \frac{5}{1.2k\Omega||1.2k\Omega} = 8.33\ mA = I_C \tag{2}$$

$$\alpha_F = \frac{\beta_F}{\beta_F+1} \tag{3}$$

$$I_E = \frac{I_C}{\alpha_F} = \frac{4.17\ mA}{0.99} = 4.21\ mA \tag{4}$$

$$r_e = \frac{V_T}{I} \tag{5}$$

$$I_C = 25 - (8.33 + 8.33) = 8.34\ mA \tag{6}$$

$$I_C|_{DC\ CC} = \frac{8.34\ mA}{2} = 4.17\ mA \tag{7}$$

$$R_E = \frac{0-(-10V)}{4.21\ mA} = 2.4\ k\Omega \tag{8}$$

$$V_B = -10 + I_E R_E + 0.7 = 0.7 \tag{9}$$

$$I_B = \frac{I_C}{10} = 42.1\ mA \tag{10}$$

$$I_B R_{B1} = 10 - V_B = 10 - 0.7 \tag{11}$$

$$I_B R_{B2} - 10 - V_B = -10 - 0.7 \tag{12}$$

$$R_{in} = R_1||R_2||[(\beta_F + 1)(r_e + R_E||R_L)] \tag{13}$$

First we can use equation 2 to find the DC component of the collector. Then we can determine I_C by subtracting the AC and DC components from 25. (Equation 6) Now we are able to find our R_E value with equations 4 and 8. By using KVL through the paths of both R_{B1} *and* R_{B2} we can find their respective resistances to be 22kΩ and 25kΩ. (Equations 11 & 12) Finally we can determine R_{in} (Equation 13) to be 10.02kΩ. We now have all the necessary values to build the CC amplifier.

Part 2 – Common Collector cont'd

Similarly to part 1, all the capacitors were left out to ensure FAM. Here we have the collector directly connected to the +10 V rail and the emitter connected to the -10 V rail through a resistor of value R_E. We then placed R_{B1} and R_{B2} connected to the 10 V and -10 V rails respectively from the base. In the final testing and design, the capacitors were put back in. The other 10 nF capacitor and 2kHz source and 50 Ohm resistor seen in Figure 2 were included in the testing of the CC amplifier, then removed once introduced as a portion of the entire circuit.

Test results

Part 1 – Common Emitter

For the first part of the lab, the common emitter was designed and built. In Figure 1, there are 10 nF capacitors, but those were left out initially to test if the transistor was in bias.

For the final entire design of the CE, the voltage V_c was measured and found to be 4.8mV. This can be seen in 5. The voltage V_B was measured and found to be -8.9 V. Finally, the voltage V_E was measured and found to be -10.1 V.

Part 2 – Common Collector

For the second part of the lab, the common collector was designed and built. Again the circuit was tested without the 10 nF capacitors to make sure it is in forward active mode. Once the capacitors were included in, and the frequency source, the voltage over the input and output was measured. These values would then be used to find the gain. The input was 250 mV, while the output was 256 mV.

The second part to test for the common collector was the input impedance, R_{in}. The amplitude of the inputted frequency source was set to 500 mV. A variable resistor was set in series between the capacitor and the input voltage. The value on the resistor was changed until the Pk-Pk value of the resulting sine wave was 250 mV. The value of R_{in} was 11.3 kOhm when the Pk-Pk value was 253 mV. This wave can be seen in Figure 8.

Part 3 – Entire Circuit Coupled

The last stage of the circuit was coupling the two amplifiers together and measuring the voltage gain, R_{in}, and where the circuit starts to clip. This was all measured with a resistor load of 1.2 kOhm as the load. The gain was found to be 13.6 V as seen in 6. The Pk-Pk value was 6.8 V, which gives the gain as 13.6 V.

The next part that was measured was the voltage to see if clipping would occur before the voltage was 10 V. This was measured over the load resistor. The amplitude of the voltage source was increased from 500mVpp until either the signal wave started to clip, or the Pk-Pk voltage was above 10 V. In the testing, it was found that the amplitude was at 794 mVpp and the Pk-Pk voltage was 10.1 V as seen in Figure 7.

The last part measured was the inputted resistance, R_{in}. This was measured in the same way as in Part 2. The variable resistor was put in series with ground and the inputted frequency source. The inputted amplitude was set to 500 mVpp, and the resistance was changed until the sine wave had a Pk-Pk value of 250 mV. In the testing, the R_{in} value was found to be 10.3 V when the Pk-Pk value was 245 mV.

Part 4 – Coupled circuit with speaker attached

For the last part of this lab, the coupled amplifiers were attached to a transformer, which was then attached to a speaker. When the frequency was increased to 27 kHz, the sound from the speaker cut out completely. The sine wave of this can be seen in 9. When the frequency was set to 2 kHz, but the amplitude voltage was increased to 1 Vpp, the tone of the sound from the speaker changed. The sine wave can be seen in Figure 10.

Simulation results

The schematic of the entire circuit designed in spice is represented in Figure 11. Unfortunately we could not get the correct waveforms from the simulation. An example of one of these is shown by Figure 11.

Discussion

The purpose of this lab was to design a transistor amplifier. This amplifier needed to have a mid-band voltage gain of 12 V/V ± 5% at a design frequency of 2 kHz. It must also have an input impedance greater than 10 kOhm and support a load of 1200 Ohm. The maximum output voltage swing without clipping must be 10 Vpp. To meet these design specifications, the entire amplifier consisted of a common collector and a common emitter amplifier to be coupled together.

For the common emitter amplifier, in theory, the V_c voltage should be 4 mV, which is approximately 0 mV. In the testing of the circuit, this value was found to have a Pk-Pk voltage of 4.8mV. The error can be found by:

$$\%\ error = \frac{x_{theory} - x_{measured}}{x_{theory}} * 100 \quad (1)$$

$$\%\ error = \frac{4\ mV - 4.8\ mV}{4\ mV} * 100 = 20\%$$

This is a rather large error. To lower the voltage, the R_C value could be increased ever so slightly. The next part measured was the V_B value. In theory, this should be -8.93 V. When testing this voltage, it was found to be -8.9 V. Using equation (1), the error would be 0.3%. This value would be exactly what is expected. Finally when measuring the V_E value, theoretically it would be -10 V. During the testing, it was found to be -10.1V. The error for this value is 1%. All these values are near what was expected. Although the V_c value had a large error, 4.8mV is still approximately zero.

For the common collector stage, three different parts were measured. The input, output, and the R_{in} value. When measuring the input value was 250 mV, while the output value was 256 mV. These values were used to find the gain (input/output). Theoretically, the gain, A_v, should be between 0.96 and 0.99. Using the results found, the circuit gain was 0.977. This value fits within the expected theoretical value. For the input resistance, an expected value of 10 kOhm or greater was expected. When doing the testing, the input resistance was found to be 11.3 kOhm. This value is fine, because R_{in} should be equal to or greater than 10 kOhm.

For the last part of the lab, both of the amplifiers were coupled together. The voltage gain, R_{in}, and the clipping point were all measured. Theoretically, the voltage gain should approximately be about 12 ± 5%. When testing, the gain was found to be 13.6. This leads to a 13% error. The final part of testing was to see if the sine wave didn't clip before a 10 V Pk-Pk. Initially, the circuit was clipping at about 3 V. To find the problem, each section of the circuit was retested. The rails were still producing the proper ± 10V that was expected. The biasing on each amplifier was rechecked, and it was found that the common emitter was in saturation instead of forward active mode. The resistor values were changed, which fixed that problem, but the output voltage was still clipping at 3V. Finally the positive and negative lead on the shared capacitor was changed, and this lead to the proper output voltage of 10 V without any clipping. Finally, the input impedance needed to be tested. Theoretically this value should be greater than or equal to10 kOhm. The measured value was 10.3 kOhm which is above the expected value.

Once the transformer and speaker was added to the final circuit, a sound was then produced. When the frequency was increased, the sound from the speaker got more high pitched, then completely cut out. This is because the amplifier designed is a mid-band voltage gain. The gain will reach its optimal value, which in this case is 12 V/V. At this gain, the amplifier will let all the mid range frequencies pass through, which is when there is sound coming from the speakers, but the amplifier won't let low or high frequencies pass through. This is why, at a value of 27kHz, the speaker cut out. If the frequency was lowered enough, the sound would also cut out. The amplifier was also designed to have an input impedance greater than 10 kOhm. This is a variable resistance though, which means it can be raised or lowered. If the input resistance is raised, the sound from the speaker will decrease.

The spice simulation caused some trouble for us as we were unable to get the correct values from the simulation as something must be wrong with the design. I believe this was due to an incorrect implementation of the coupling inductors.

Conclusions

The objective of this lab was to design and build a transistor amplifier. The design specifications of this amplifier was to have a mid-band voltage gain of 12 V/V, at a frequency of 2 kHz. The amplifier must have a maximum output voltage swing, without clipping, of 10 Vpp and an input impedance greater than 10 kOhm. To get these specifications, the amplifier must have a high input impedance and a medium output impedance. The only way to achieve this is to have two different amplifiers coupled together. In this lab, a common collector was chosen as the first stage with the high input impedance and it is coupled with a common emitter amplifier for the medium output impedance. The coupled amplifier used a dual rail power supply and was connected to a 1200:8 transformer, which was then connected to an 8Ohm speaker. The signal source was a 2kHz signal generator with an output resistance of 50 Ohm.

From the results, it was found that the input impedance was 10.3 kOhm. This is greater than the acceptable value of 10 kOhm which is what the input impedance should be. It was also found that the output voltage gain was 13.6 V. This is off the expected value of 12 V by 13 %. There could be many sources of error for this value. The power source not being exactly ± 10 V or each stage of the amplifier could also be off on their values. The positive and negative leads on the capacitors could have been facing the wrong way. The last design specification was having maximum swing voltage of 10 V without any clipping. In the testing, a value of 10.1 V was reached without any clipping, which meets the design specifications.

Although we didn't get the correct results from the spice simulation we still successfully completed the lab. When testing the various properties of the speaker, the inputted frequency was raised and lowered to see what would happen to the sound of the speaker. When the frequency hit 27 kHz, the sound completely cut off. This is because the amplifier was designed to only let mid range frequencies pass through, and stop all low and high frequencies. So if the frequency was lowered enough, the sound would also cut out. It was also found that as the amplitude of the signal source was changed, the tone of the sound changed as well.

Tables and Figures

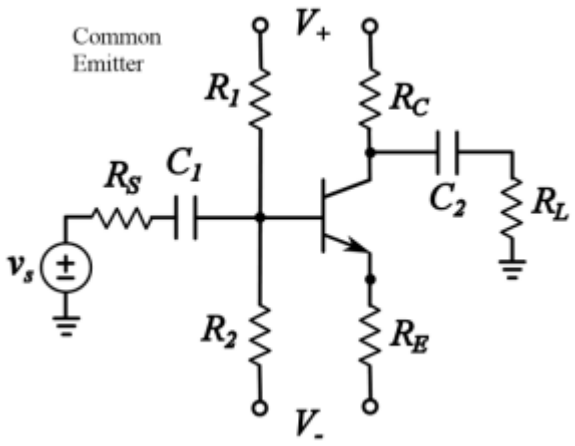

Figure 1 – Common Emitter circuit design

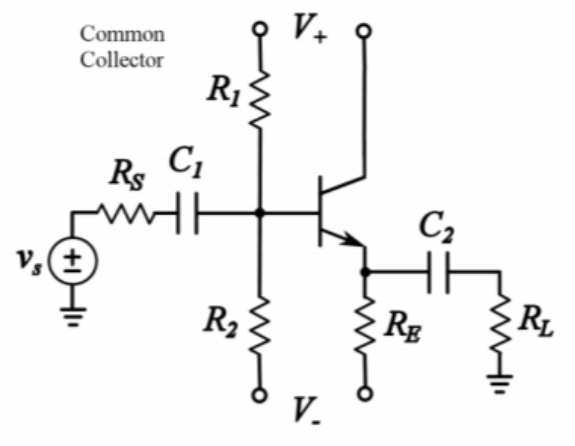

Figure 2 – Common Collector circuit design

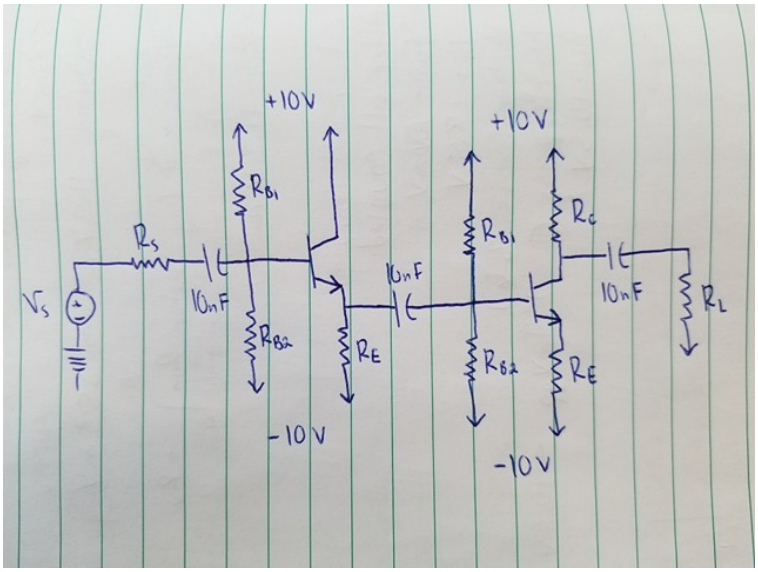

Figure 3 – Common Collector and
Common Emitter circuit

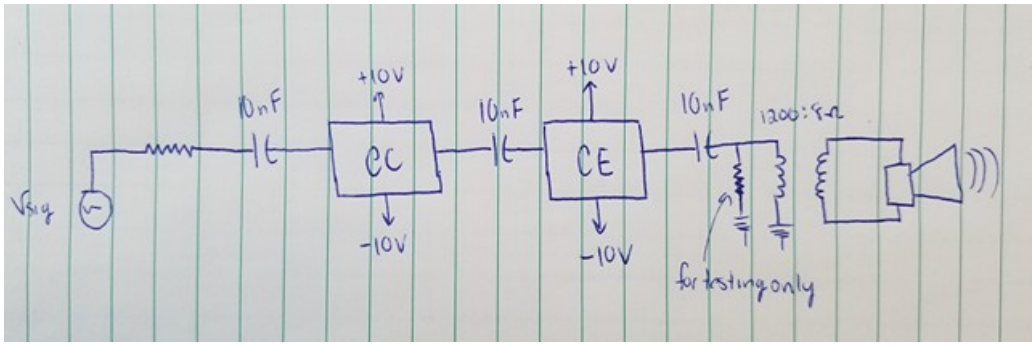

Figure 4 – Block Diagram of Entire Circuit

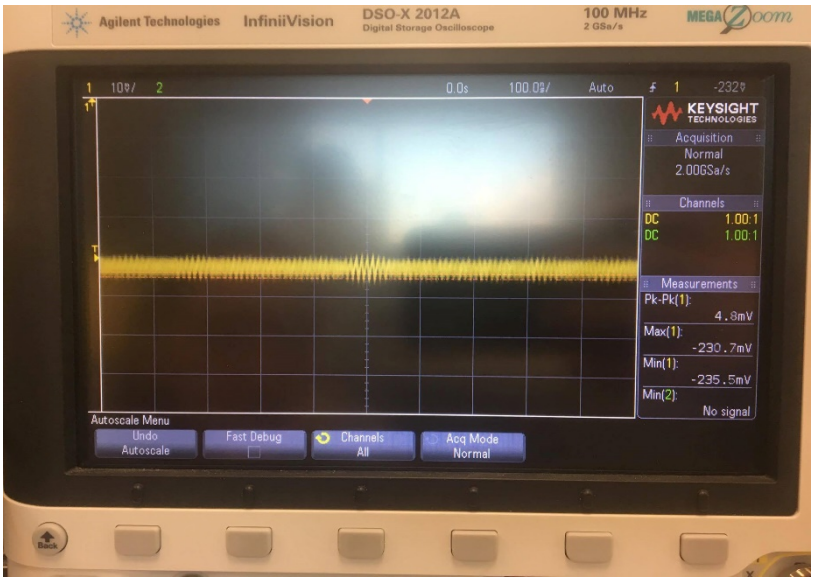

Figure 5 – Sine wave when measuring V_c

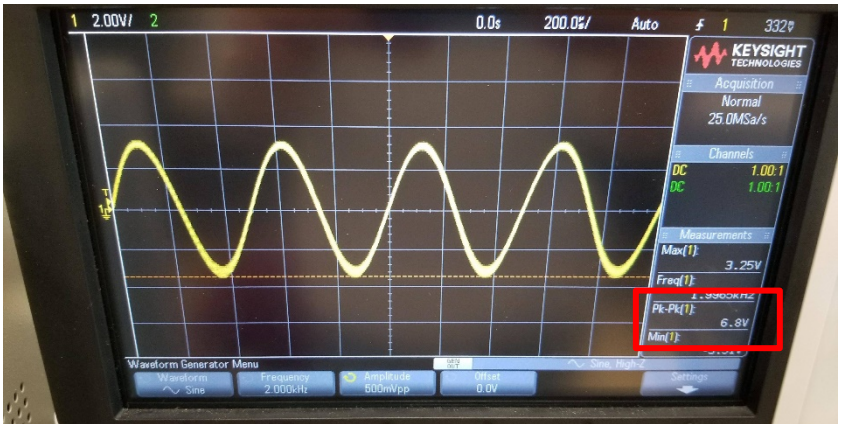

Figure 6 – Voltage Gain of coupled circuit (Pk-Pk = 6.8V)

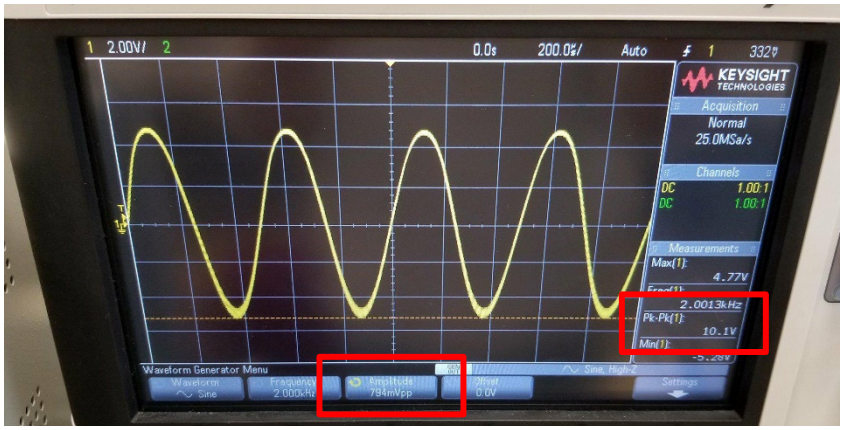

Figure 7 – No clipping after 10V
(Pk-Pk = 10.1V, Amplitude of inputted signal = 794 mVpp)

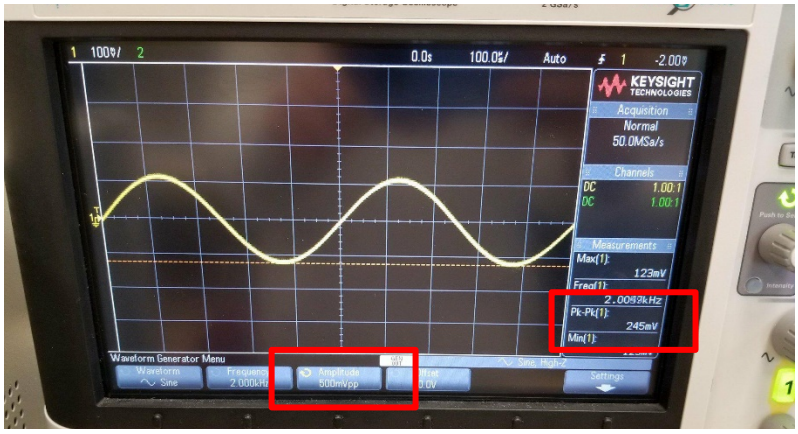

Figure 8 – Sine wave while measuring R_{in} for coupled circuit (Pk-Pk = 245 mV, Amplitude of inputted signal = 500 mVpp)

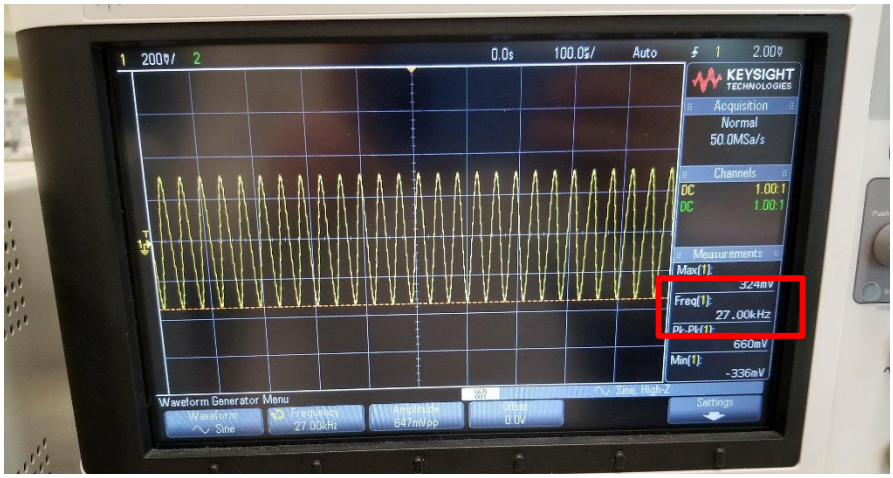

Figure 9 – Sine wave when speaker cut out at high frequency

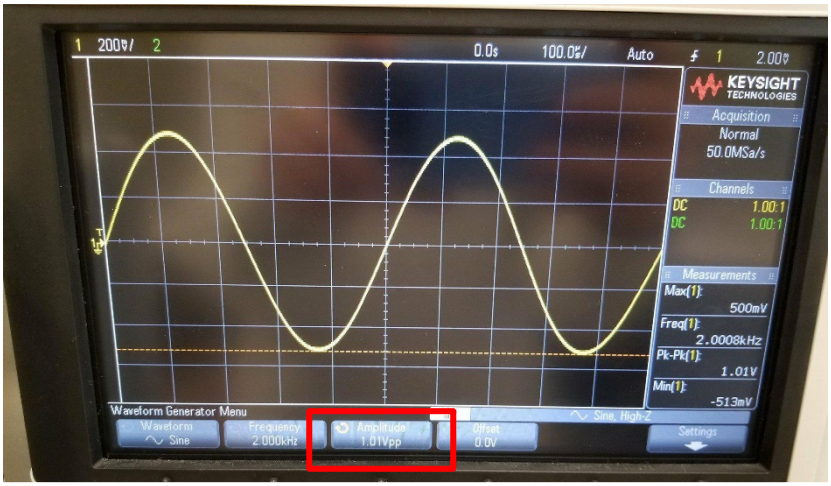

Figure 10 – Sine wave when speaker tone changed

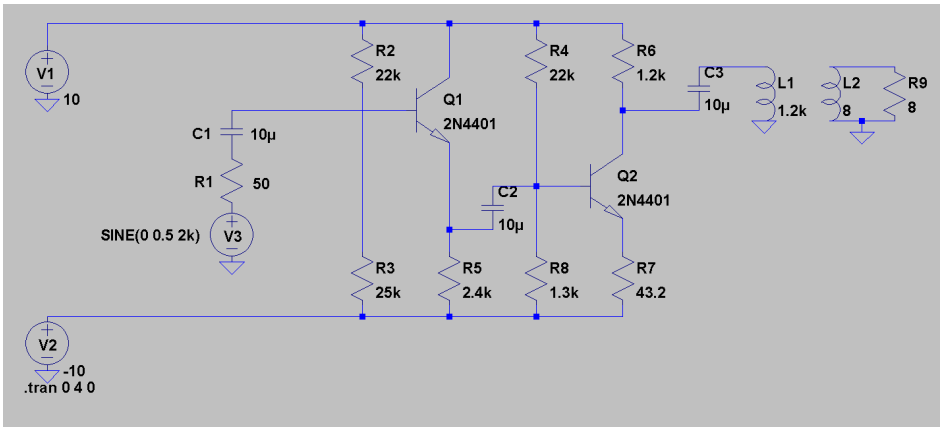

Figure 11 – LTSpice schematic

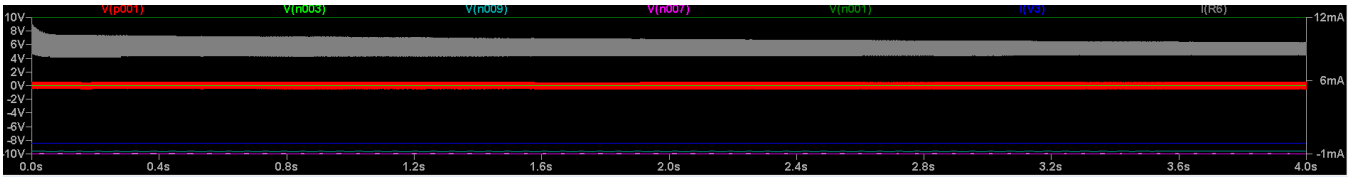

Figure 12