ECE 304

Design and Analysis of a 2-bit Parallel-in-Serial-Out Shift Register

Abstract:

In this lab, we create a single-bit shift register cell and emulate the desired behaviour. Using our previously designed 3-input NAND gate, we disregard one of the inputs by tying it to Vdd (this act of setting it to 1 allows the other 2 inputs to still behave as a 2 input NAND gate). The schematic for the cell is then built by combining the other required components (**Figure 1**) and simulating the testbench for 70n, comparing the plotted results (**Figure 5**) to the expected behaviour (**Figure 3**) to confirm everything is functioning properly. Two of these cells are then combined, using the same select and clock signals, to form a 2 bit shift register that has a data bus containing wires for each bit. This circuit is then applied in a testbench with a piecewise linear voltage source (period of 30.2 ns) and the corresponding output plot (**Figure 8**) analyzed to ensure required behaviour. For each rising clock edge, the output receives a new value (Bit 0 first and then Bit 1). Finally, the Cadence calculator functionality was used to calculate the power consumption of our circuit. Dynamic power consumption creates spikes in the instantaneous power expression waveform due to the circuit capacitors charging and discharging around the clock and input edges. We got the value of average power calculated to be 874.664 nW. In addition, parametric sweeps were used to see the average power response to changes in clock frequency for each different voltage supply (**Figure 13**).

Design:

Part 1: 1-Bit Shift Register Cell

The initial register cell shifts a single bit. The 3-input NAND gates developed previously had one input tied off to Vdd to turn them into 2-inputs and components combined; internal signals are given names in Cadence so the waveforms can be tracked and plotted.

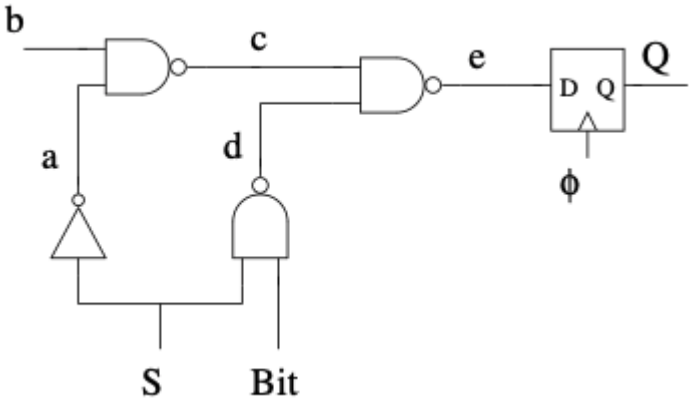

Figure 1 - Shift register cell diagram

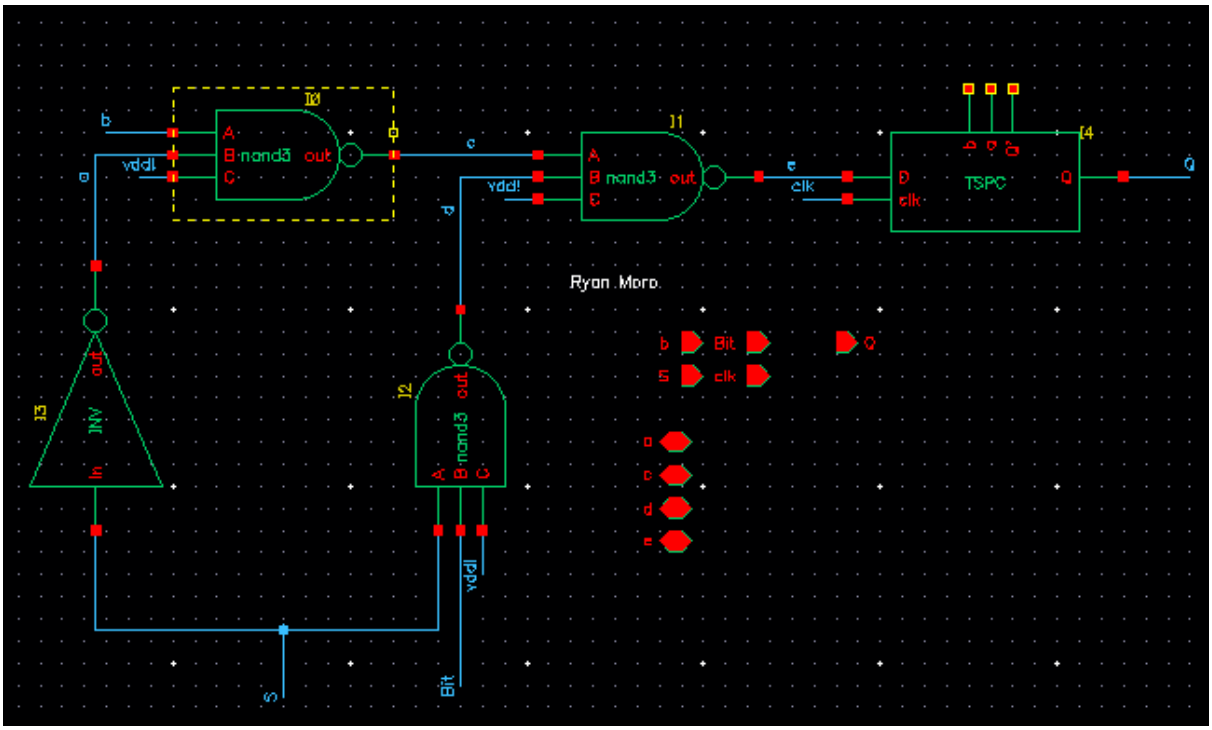

Figure 2 - Shift register cell schematic

One bit shift register cell built using components from previous labs (**Figure 2**). 2-input NAND gates are implemented using our 3-input NANDs with one output tied to Vdd allowing the other 2-inputs to determine the result. Waveform provided by simulating a testbench variant of the circuit for 70 ns to ensure expected output.

Input	Voltage 1	Voltage 2	Delay time	Rise time	Fall time	Pulse width	Period
S	0	1.0	10n	1p	1p	10n	30n
ϕ	0	1.0	19.5n	1p	1p	10n	30n
Bit	0	1.0	35n	1p	1p	35n	70n
b	0	1.0	0	1p	1p	25n	70n

Figure 3 - Shift register cell testbench vpulse parameters

Figure 4 - Shift register cell timing diagram

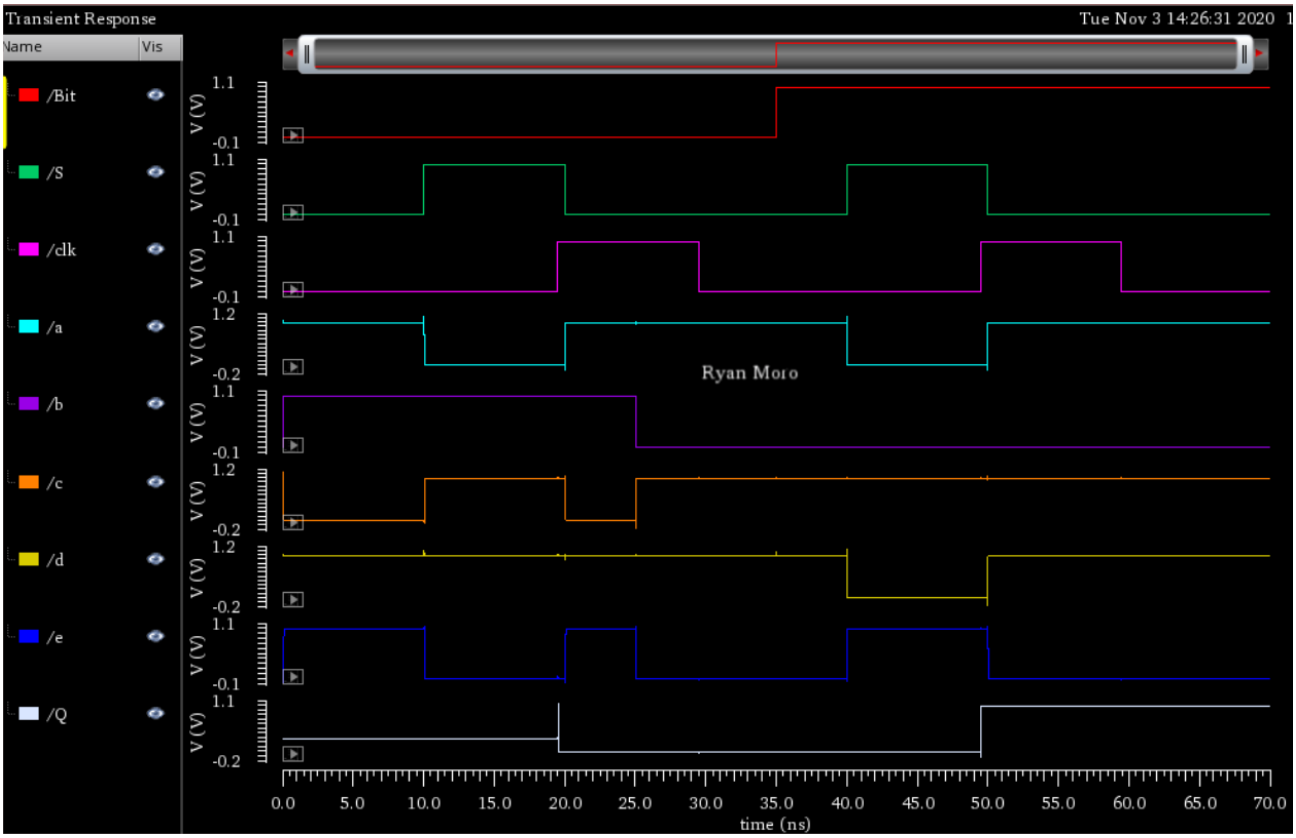

Figure 5 - Shift register cell simulation

	S	a	b	c	d	e
Load data	1	0	X	1	Bit'	Bit
Shift data	0	1	data	b'	1	b

Figure 6 - Shift register cell operation

Part 2: 2-Bit Shift Register

The 2-bit shift register was developed by combining two of the single bit shift cell circuits. Both of these components are synchronized to the same select and clock signals. The clock signal is generated using a piecewise linear voltage source, in which every single time/voltage coordinates of every point on the waveform are specified. Using the provided table parameters (**Figure 9 & 10**), the circuit behaviour is simulated and outputs plotted for 70 ns (**Figure 8 & 11**).

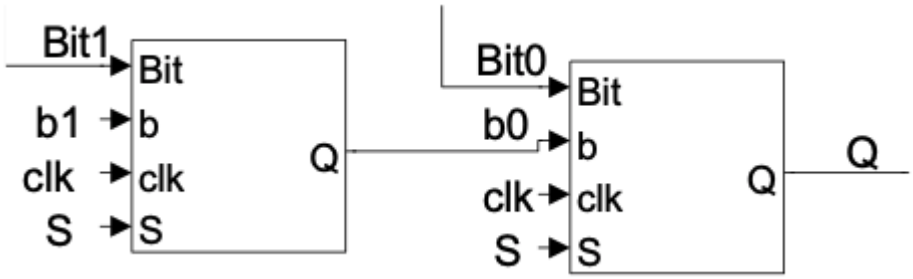

Figure 7 - 2-bit shift register diagram

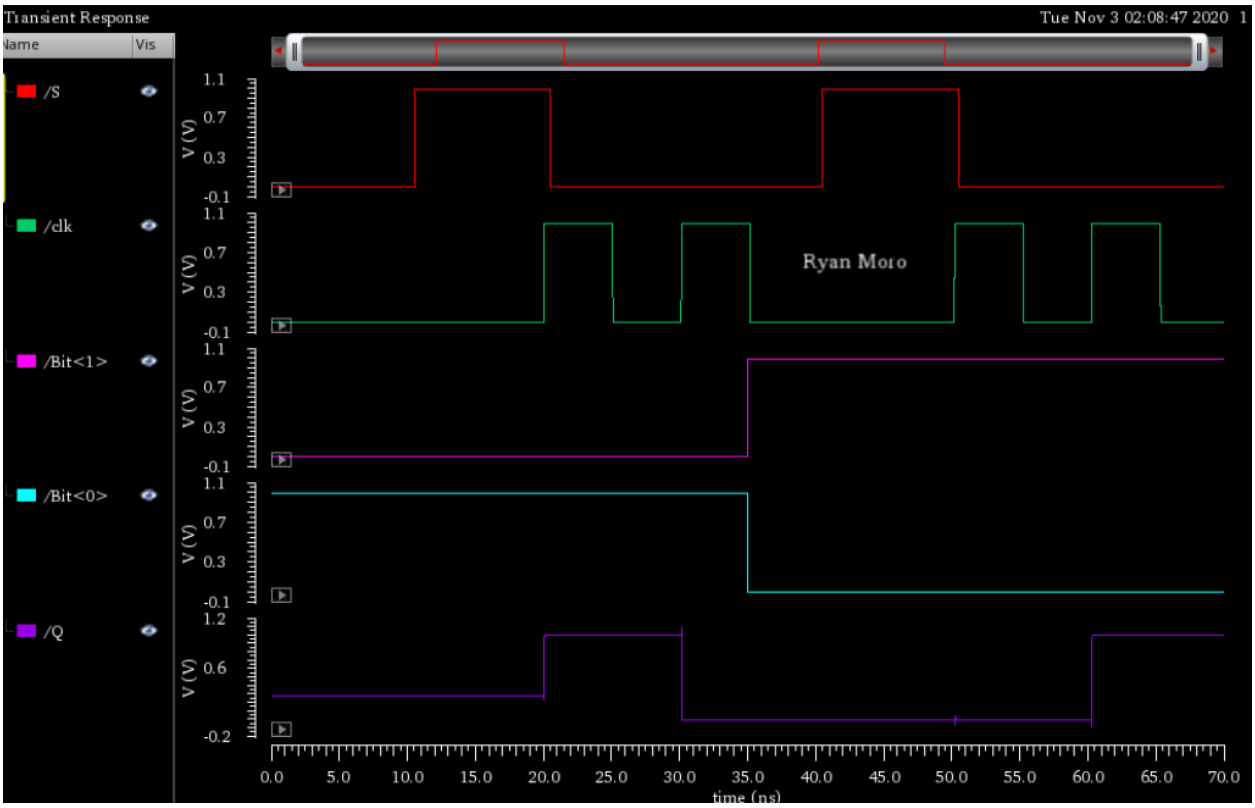

Figure 8 - 2-bit shift register simulation

Input	Voltage 1	Voltage 2	Delay time	Rise time	Fall time	Pulse width	Period
Bit<1>	0	1.0	35n	1p	1p	35n	70n
Bit<0>	1.0	0	35n	1p	1p	35n	70n
S	0	1.0	10.5n	1p	1p	10n	30n

Figure 9 - 2-bit shift register testbench vpulse parameters

Value	Pair 1	Pair 2	Pair 3	Pair 4	Pair 5	Pair 6	Pair 7	Pair 8	Pair 9
Time	0	15n	15.05n	20.05n	20.1n	25.1n	25.15n	30.15n	30.2n
Voltage	0	0	1.0	1.0	0	0	1.0	1.0	0

Figure 10 - 2-bit shift register testbench vpwl parameters

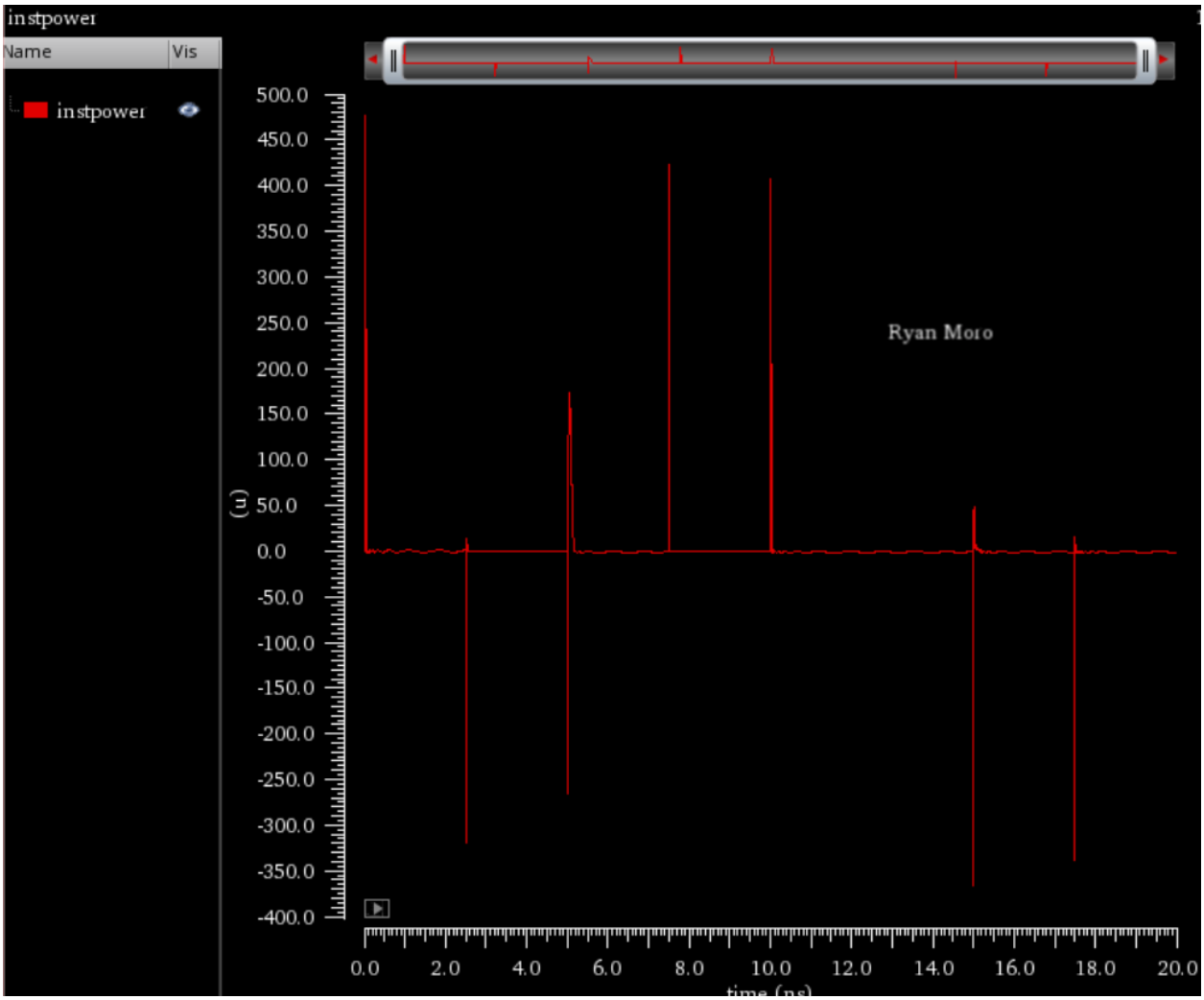

Figure 11 - 2-bit shift register testbench vpwl parameters

The spikes correspond to the clock and input edges due to the capacitances in the circuit being charged/discharged. These values represent the dynamic power consumption. The flat areas between spikes occur when the circuit has returned to a steady state, and the power here is due to static power dissipation (junction leakage, tunnelling, subthreshold conduction). In contrast, the average power consumed by the circuit is a single value calculated from our simulation and component parameters.

Avgpower = 874.664 nW

clkfreq	vsupply				
---	---	1.38889G	1.15		
		1.38889G	1.3		
100M	700m	1.71111G	700m		
100M	850m	1.71111G	850m		
100M	1	1.71111G	1		
100M	1.15	1.71111G	1.15		
100M	1.3	1.71111G	1.3		
422.222M	700m	2.03333G	700m		
422.222M	850m	2.03333G	850m		
422.222M	1	2.03333G	1		
422.222M	1.15	2.03333G	1.15		
422.222M	1.3	2.03333G	1.3		
744.444M	700m	2.35556G	700m		
744.444M	850m	2.35556G	850m		
744.444M	1	2.35556G	1		
744.444M	1.15	2.35556G	1.15		
744.444M	1.3	2.35556G	1.3		
1.06667G	700m	2.67778G	700m		
1.06667G	850m	2.67778G	850m		
1.06667G	1	2.67778G	1		
1.06667G	1.15	2.67778G	1.15		
1.06667G	1.3	2.67778G	1.3		
1.38889G	700m	3G	700m		
1.38889G	850m	3G	850m	3G	1.15
1.38889G	1	3G	1	3G	1.3

Figure 12 - Sweep values for clkfreq and vsupply

These values are used to build the plot below (**Figure 13**) showing the effect on average power consumption. Cadence's parametric analysis is used to get these clock frequency and voltage supply sweep values; their effects can be visualized in the output waveform.

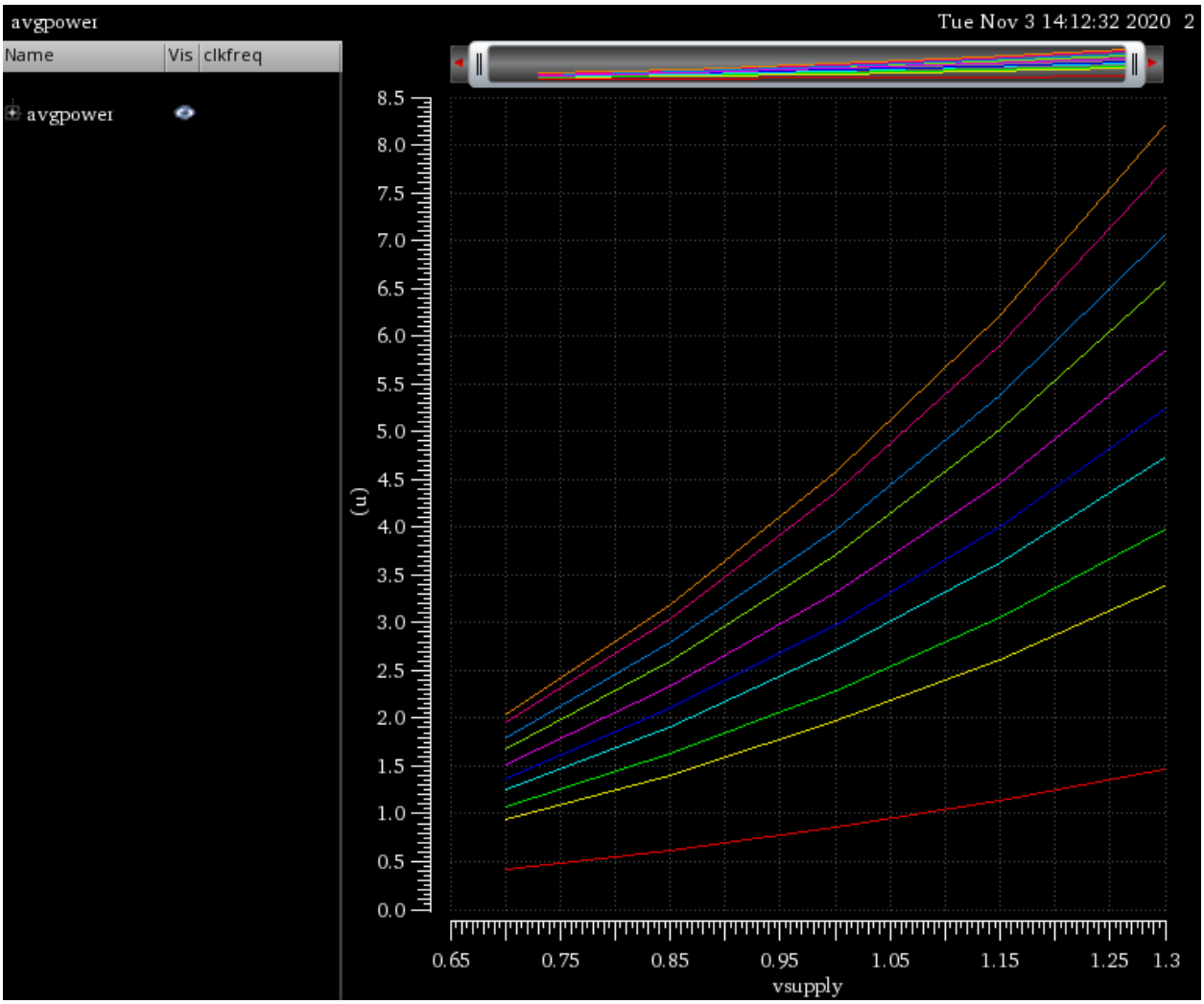

Figure 13 - Parametric sweep of average power with varying clock freq and supply voltage

Questions:

1) What could happen in the shift register if S = 1 did not slightly overlap the first rising clock edge?

S is used to select between modes. When S = 1, data is loaded (parallel in) from Bit. It propagates through the circuit to e, where it waits for a rising clock edge φ.When the rising clock edge comes, S goes to 0, and data is shifted from e to Q, and that data from e is replaced by the data from b.

If there was no overlap, the Bit value may not have propagated through the circuit to e before the rising clock edge potentially resulting in an incorrect bit being shifted out to Q.

2) How does average power change with clock frequency and voltage supply?

Average power scales linearly with clock frequency, and exponentially with voltage supply. A parametric sweep considering both these variables displays both the linear and exponentially increasing average power in **Figure 11**.

3) Using the first value you found for average power, and assuming that the large majority of that power is dynamic power dissipation, estimate the total capacitance that is being charged/discharged in your flip-flop (assuming that activity ratio is equal to 1).

Avgpower = 874.664 nW = P_dynamic = $\alpha * f * C * V_{dd}^2$

α = 1, f_{clk} =1/T =$1/(30 * 10^{-9})$ = 33.3 MHz, C = ? , V_{dd}^2= 1 V

=> C = 26.3 fF