Lab Report 4: Design & Simulation of 1-bit adder

ECEN 454/714
2/19/2024

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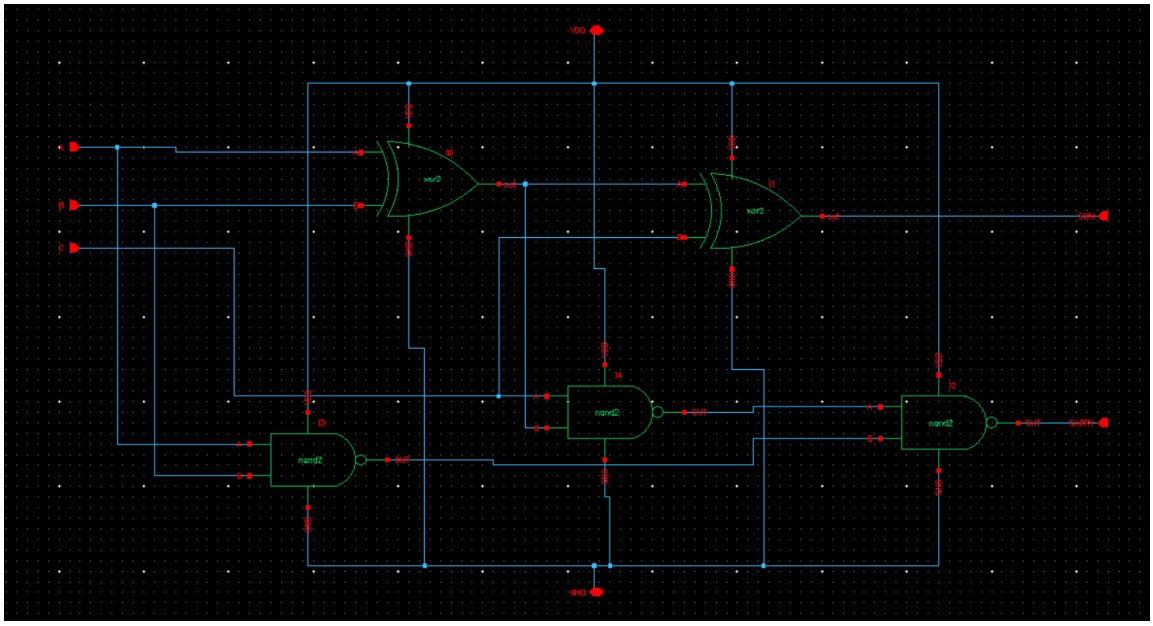
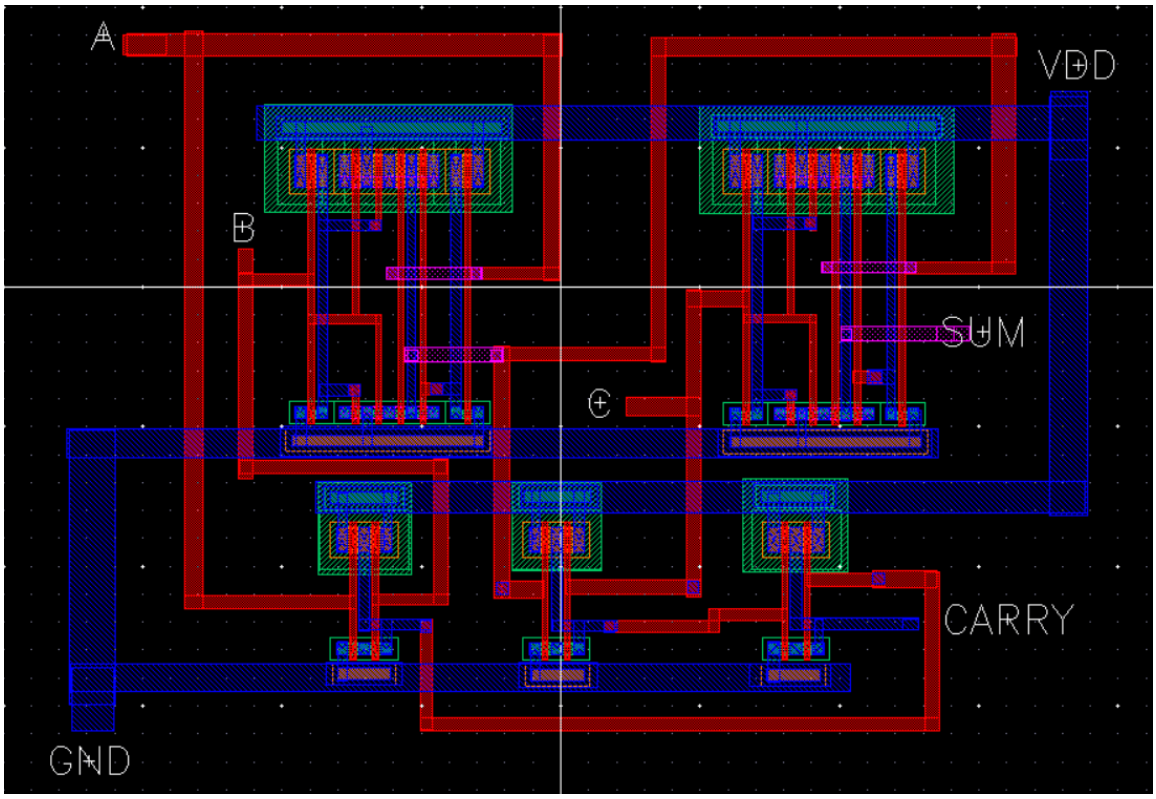
1) Schematic, Layout, DRC, LVS Reports of the 1-bit adder:

a) Schematic:



b) Layout:



c)

```
DRC started.......Sat Feb 24 19:13:44 2024
    completed ....Sat Feb 24 19:13:45 2024
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "1_bit_adder layout"   *********
   Total errors found: 0
```

d)

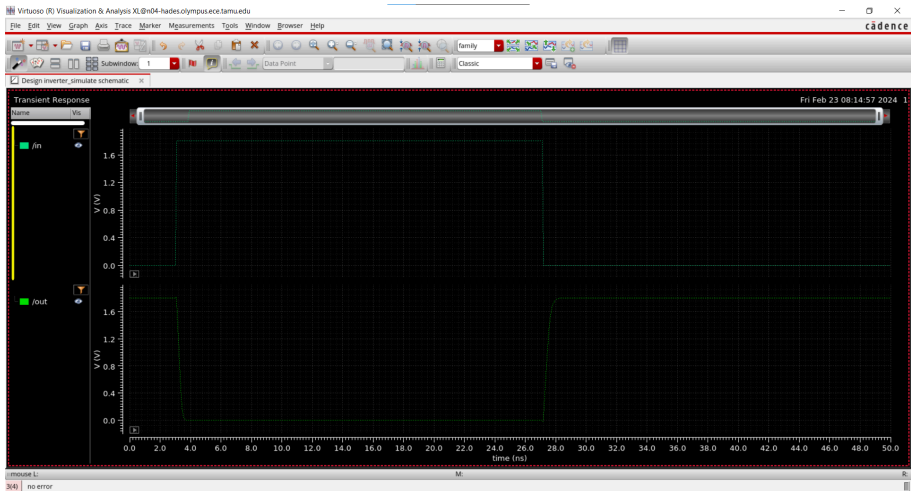
Virtuoso® 6.1.8-64b - Log: /home/ugrads/p/pengryan188/CDS.log@n05-prometheus.olympus.ece.tamu.edu

File Tools Options Help

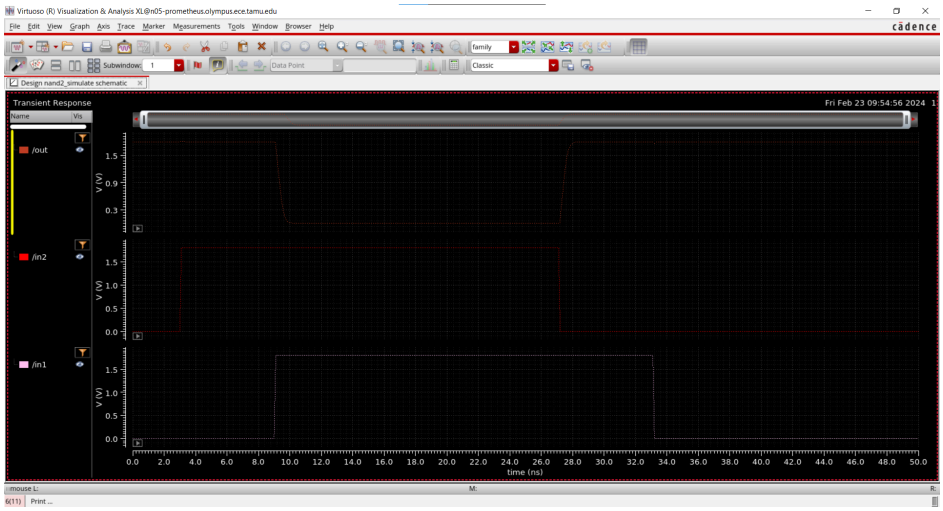
```
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Sat Feb 24 18:47:24 2024
    completed ....Sat Feb 24 18:47:24 2024
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "xor2 layout"   *********
   Total errors found: 0


Extraction started at Sat Feb 24 18:47:37 2024

Validating hierarchy instantiation for:
library: Design
cell:    xor2
view:    layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaEXT.rul.
Inclusion limit is set to 1000.
Switches used: Extract_parasitic_caps.
Running layout Extraction analysis
flat mode
Full checking.
For layer nChannelTran :
    6  shapes encountered.
    6  nmos4 ivpcell NCSU_Analog_Parts devices well formed.
For layer pChannelTran :
    6  shapes encountered.
    6  pmos4 ivpcell NCSU_Analog_Parts devices well formed.
0 cap ivpcell NCSU_Analog_Parts parasitics created.
0 cap ivpcell NCSU_Analog_Parts parasitics created.
0 cap ivpcell NCSU_Analog_Parts parasitics created.
0 cap ivpcell NCSU_Analog_Parts parasitics created.
0 cap ivpcell NCSU_Analog_Parts parasitics created.
0 cap ivpcell NCSU_Analog_Parts parasitics created.
0 pcapacitor ivpcell NCSU_Analog_Parts parasitics created.
0 pcapacitor ivpcell NCSU_Analog_Parts parasitics created.
0 pcapacitor ivpcell NCSU_Analog_Parts parasitics created.
19 pcapacitor ivpcell NCSU_Analog_Parts parasitics created.
7 pcapacitor ivpcell NCSU_Analog_Parts parasitics created.
6 pcapacitor ivpcell NCSU_Analog_Parts parasitics created.
Extraction started.......Sat Feb 24 18:47:37 2024
          completed ....Sat Feb 24 18:47:37 2024
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "xor2 layout"   *********
   Total errors found: 0
```

2) Output waveforms of the INV, NAND2, XOR2, and a 1-bit adder

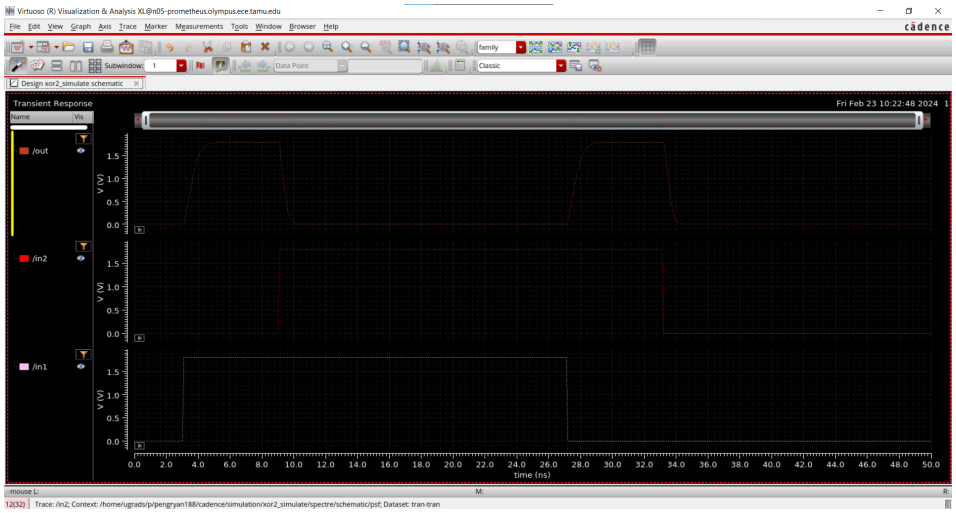
a) INV



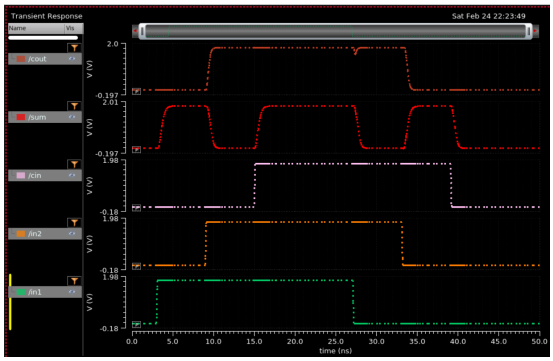
b) NAND2



c) XOR2



d) 1-bit adder



3) Delay table for every layout

	Rising Delay	Falling Delay	Error %
INV	0.241	0.24152	0.216%
NAND2	0.276 ns	0.312	13.04%
XOR2	0.449346 ns	0.419116 ns	7.213%
1-bit Adder	0.612 ns	0.618 ns	0.98%

4) Power Dissipations

For VDC: Average Power = 1.8V * Average Current
For VPulse: Average Power = Average DC Voltage * Average Current

a) INV

V0 (VDC): 1.8V * (-1.949E-6 A) = **-3.5082E-6 W**
V1 (VPulse): (0.8676 V) * (1.862E-9 A) = **1.615E-9 W**

b) NAND2

V0 (VDC): 1.8V * (-2.042E-6 A) = **-3.6756E-6 W**
V1 (VPulse): (0.8676 V) * (-828.6E-12 A) = **-7.189E-10 W**
V2 (VPulse): (0.8676 V) * (425.4E-12 A) = **3.69E-10 W**

c) XOR2

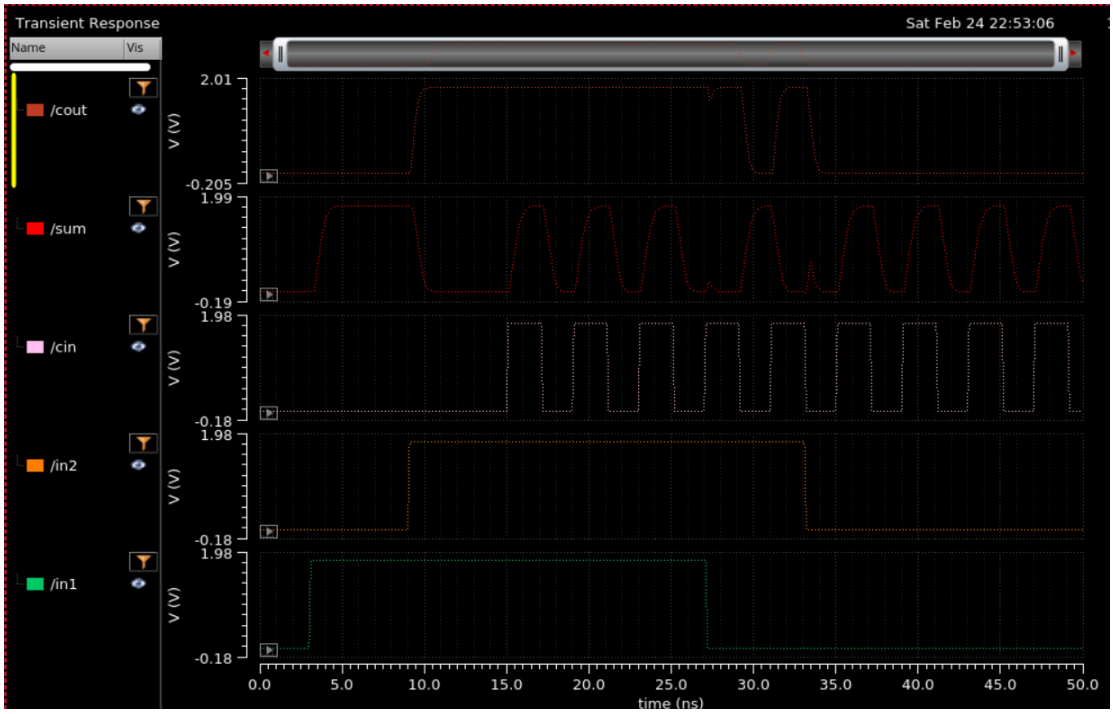
V0 (VDC): 1.8V * (-4.981E-6) = **-8.9658E-6 W**
V1 (VPulse): (0.8676 V) * (3.457E-9 A) = **3E-9 W**
V2 (VPulse): (0.8676 V) * (-7.667E-9 A) = **-6.652E-9 W**

d) 1-bit Adder

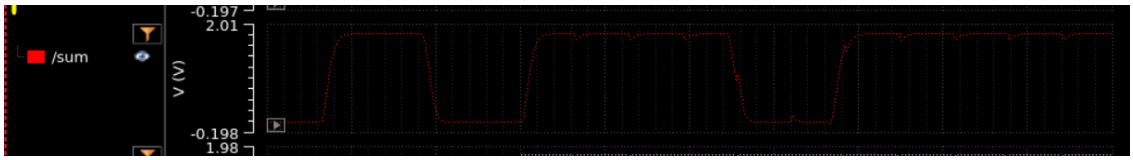
V0 (VDC): 1.8V * (-12.73E-6 A) = **-22.914E-6 W**
V1 (VPulse): (0.8676 V) * (363.8E-12 A) =
V2 (VPulse): (0.8676 V) * (10.75E-9 A) =
V3 (VPulse): (0.8676 V) * (-20.73E-9 A) =

5) Max Frequency

We achieved the maximum frequency where the output was stable at pulse width of 2ns, and period of 4ns.



The next test was at pulse width 3ns, and period of 3ns.

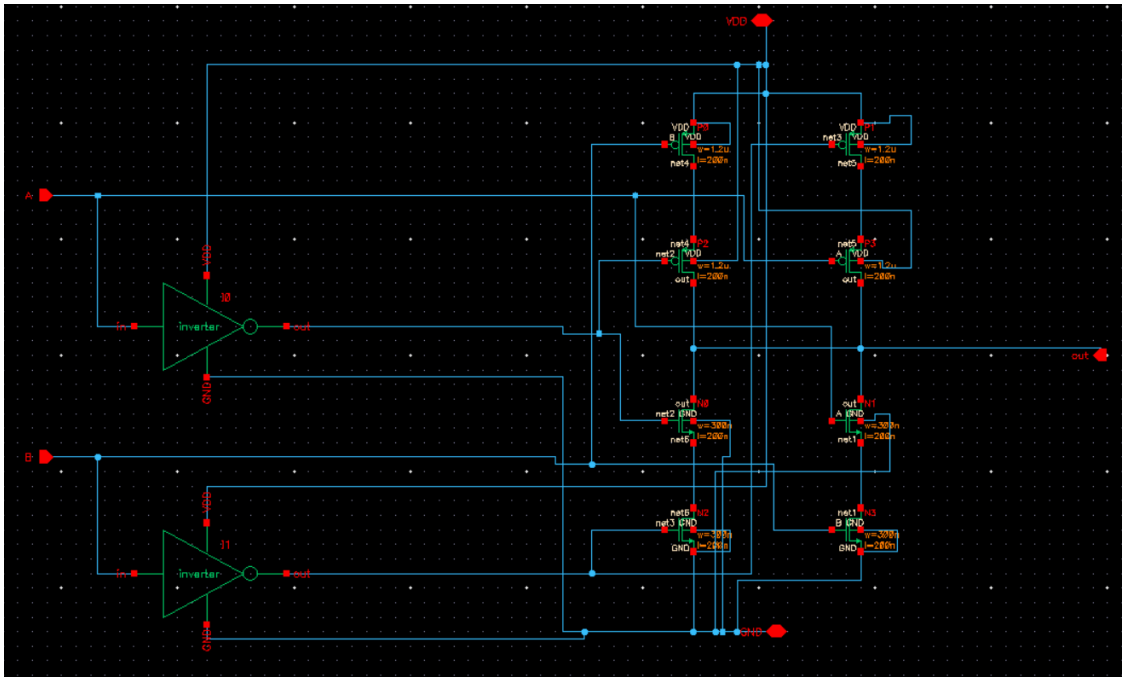


The graph starts to fail to reach zero and stays at about 1.8V as its amplitude throughout the graph

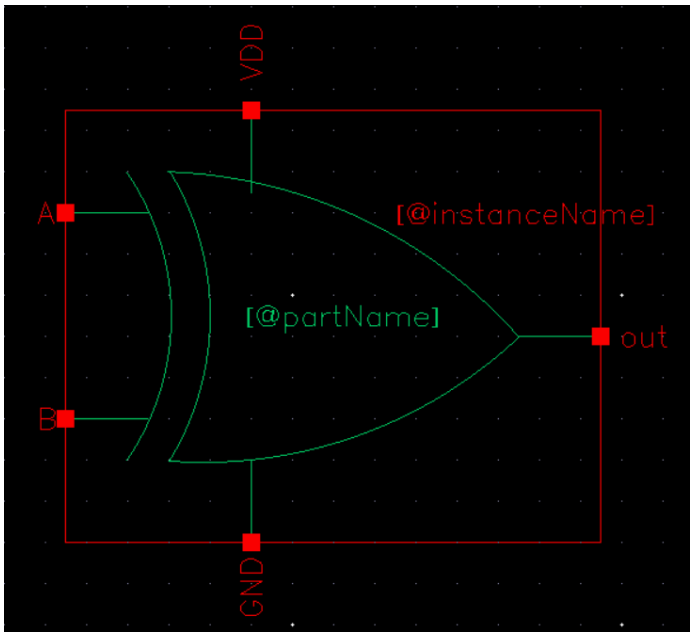
6) Reducing Delay

To reduce the delay, we adjusted the size of the XOR2 gate based on the results in lab 3. The results we got were the width of the PMOS is 1.2um and the width of the NMOS is 300 nm.

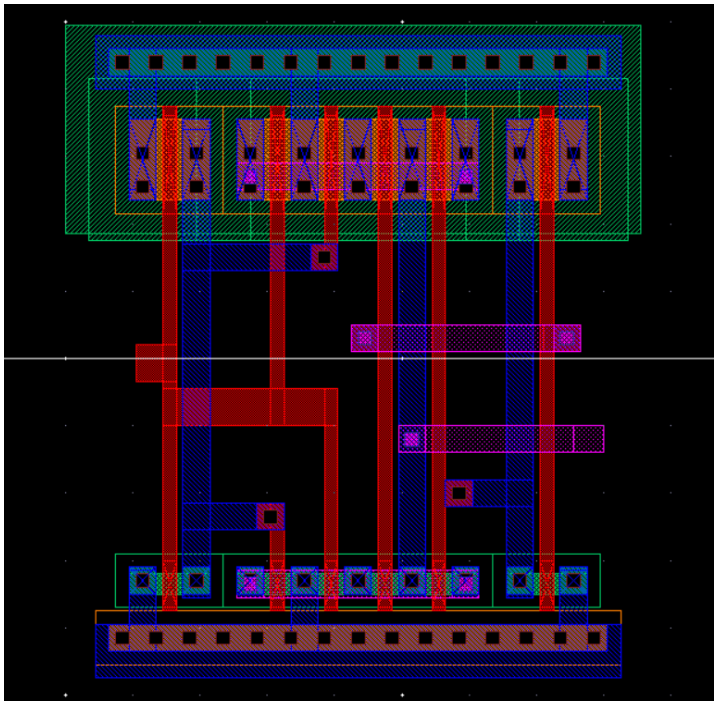
a) XOR2 Schematic



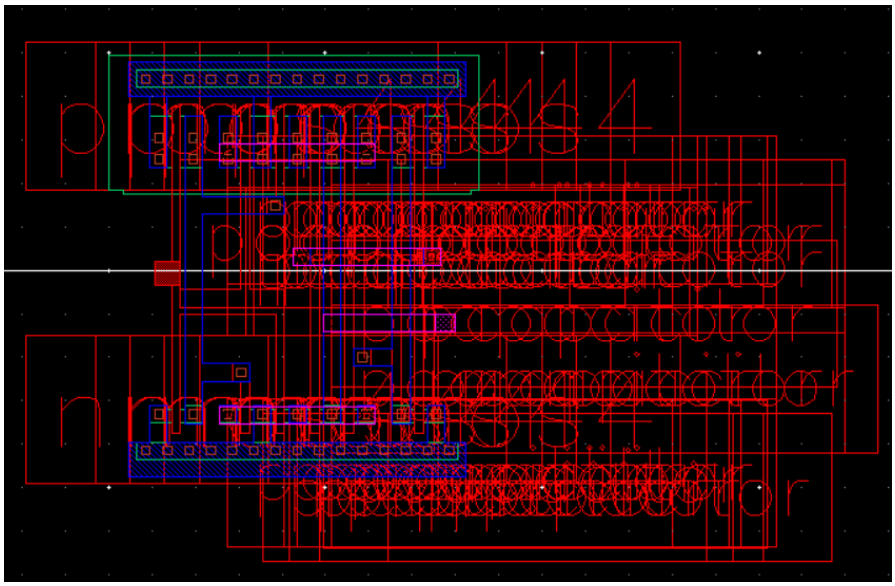
b) XOR2 Symbol



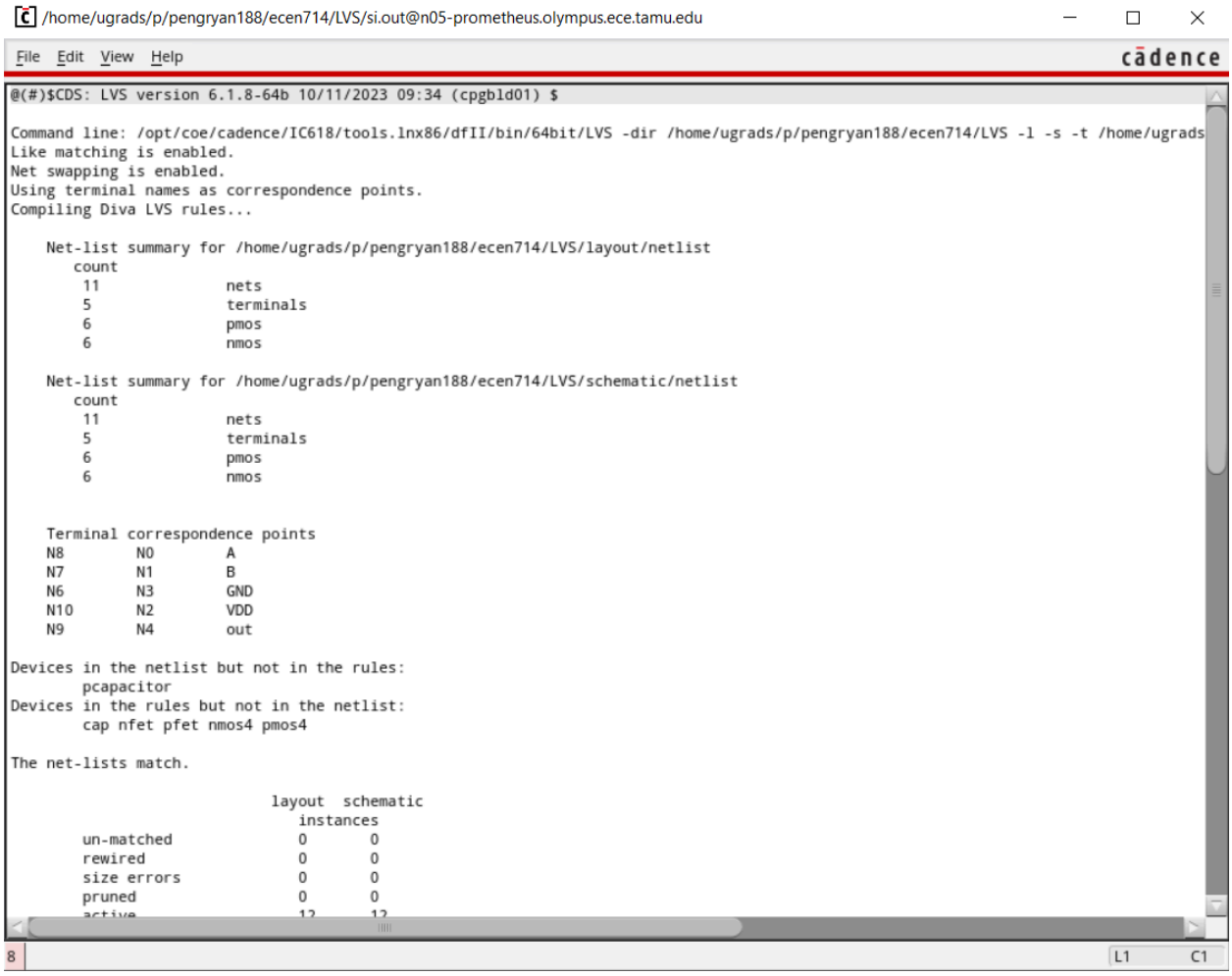
c) XOR2 Layout



d) XOR2 Extraction



e) XOR2 LVS


/home/ugrads/p/pengryan188/ecen714/LVS/si.out@n05-prometheus.olympus.ece.tamu.edu
File Edit View Help
cadence
@(#)$CDS: LVS version 6.1.8-64b 10/11/2023 09:34 (cpgbld01) $
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/p/pengryan188/ecen714/LVS -l -s -t /home/ugrads
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...
Net-list summary for /home/ugrads/p/pengryan188/ecen714/LVS/layout/netlist
count
11 nets
5 terminals
6 pmos
6 nmos
Net-list summary for /home/ugrads/p/pengryan188/ecen714/LVS/schematic/netlist
count
11 nets
5 terminals
6 pmos
6 nmos
Terminal correspondence points
N8 N0 A
N7 N1 B
N6 N3 GND
N10 N2 VDD
N9 N4 out
Devices in the netlist but not in the rules:
pcapacitor
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4
The net-lists match.
layout schematic
instances
un-matched 0 0
rewired 0 0
size errors 0 0
pruned 0 0
active 12 12
8
L1 C1