

Post Lab Report 6: Design & Characterization of a Flip-flop

ECEN 454/714

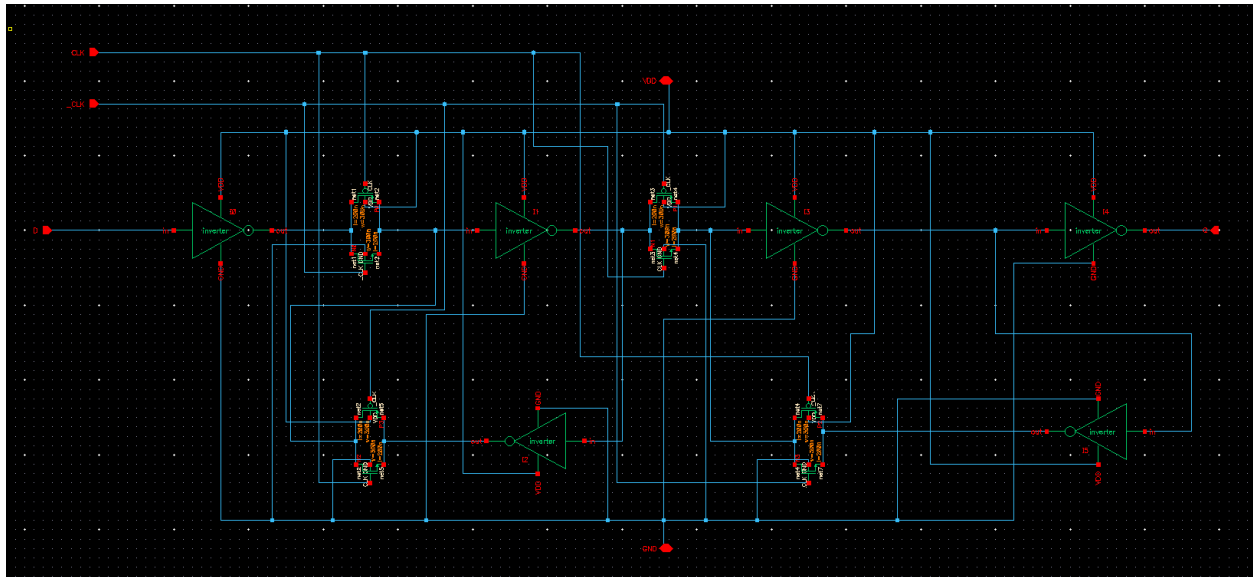
3/18/2024

TA: Saichand Samudrala

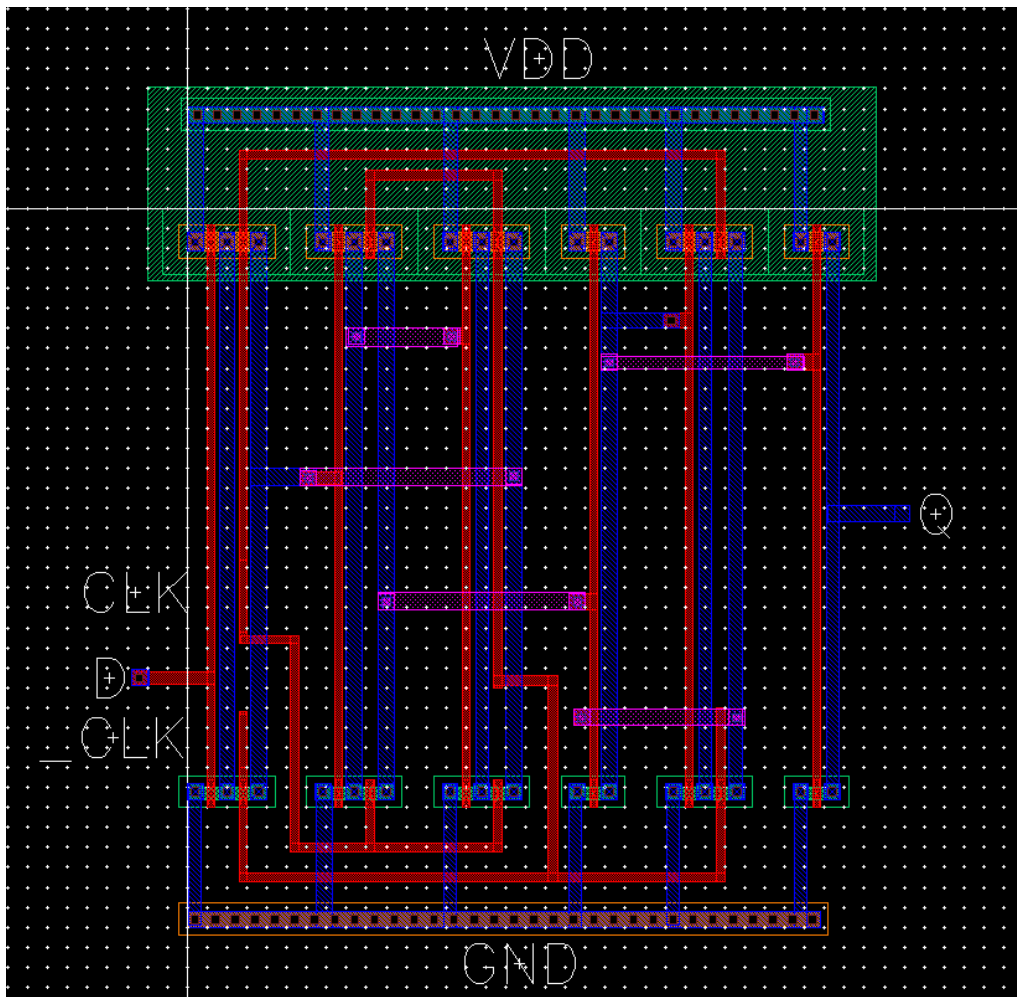
Ryan Peng

631003156

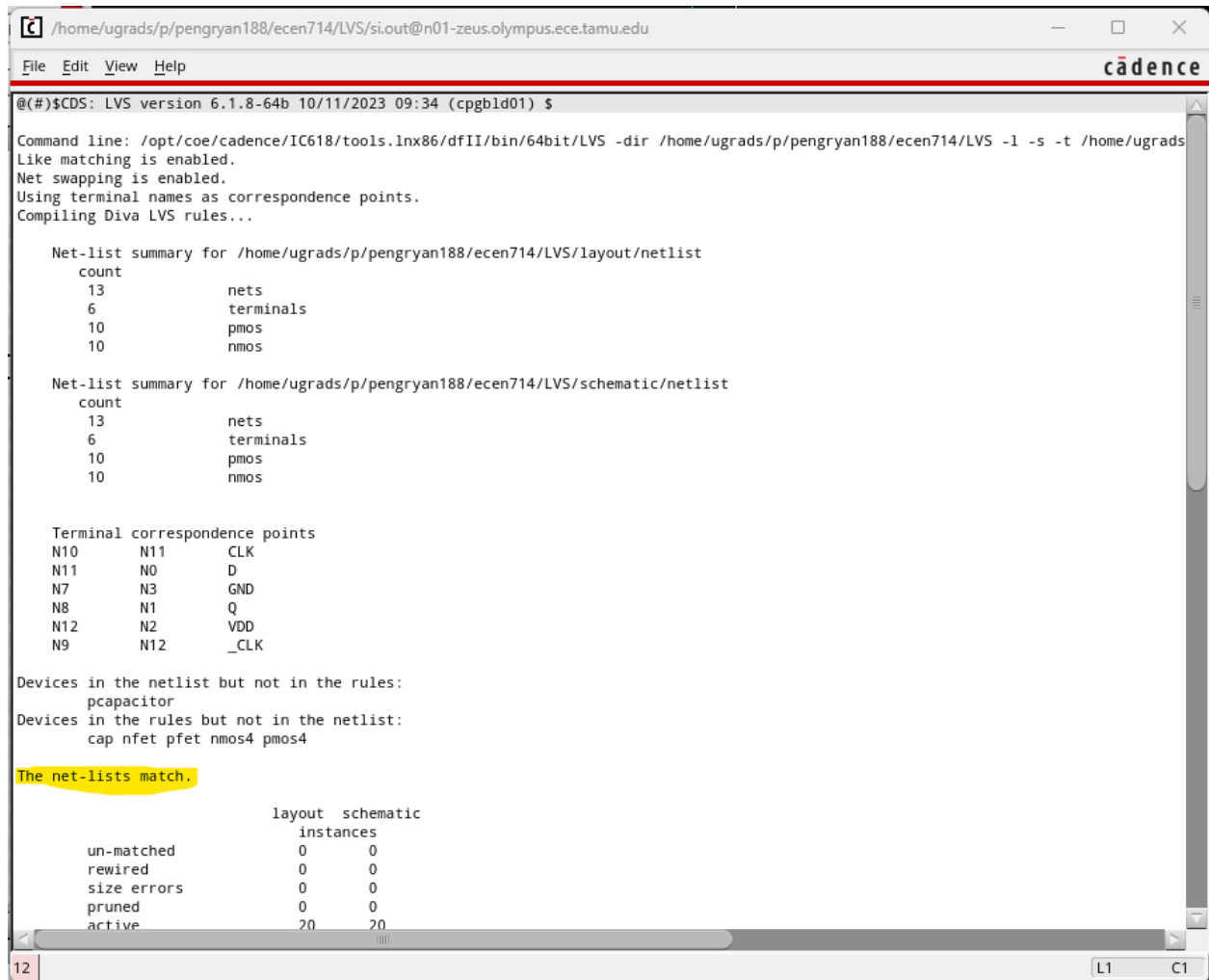
DFF Schematic:



DFF Layout:



DFF LVS Report:



```
@(#)CDS: LVS version 6.1.8-64b 10/11/2023 09:34 (cpgb1d01) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/p/pengryan188/ecen714/LVS -l -s -t /home/ugrads
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/ugrads/p/pengryan188/ecen714/LVS/layout/netlist
count
13      nets
6       terminals
10      pmos
10      nmos

Net-list summary for /home/ugrads/p/pengryan188/ecen714/LVS/schematic/netlist
count
13      nets
6       terminals
10      pmos
10      nmos

Terminal correspondence points
N10     N11     CLK
N11     N0      D
N7      N3      GND
N8      N1      Q
N12     N2      VDD
N9      N12     _CLK

Devices in the netlist but not in the rules:
pcapacitor
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

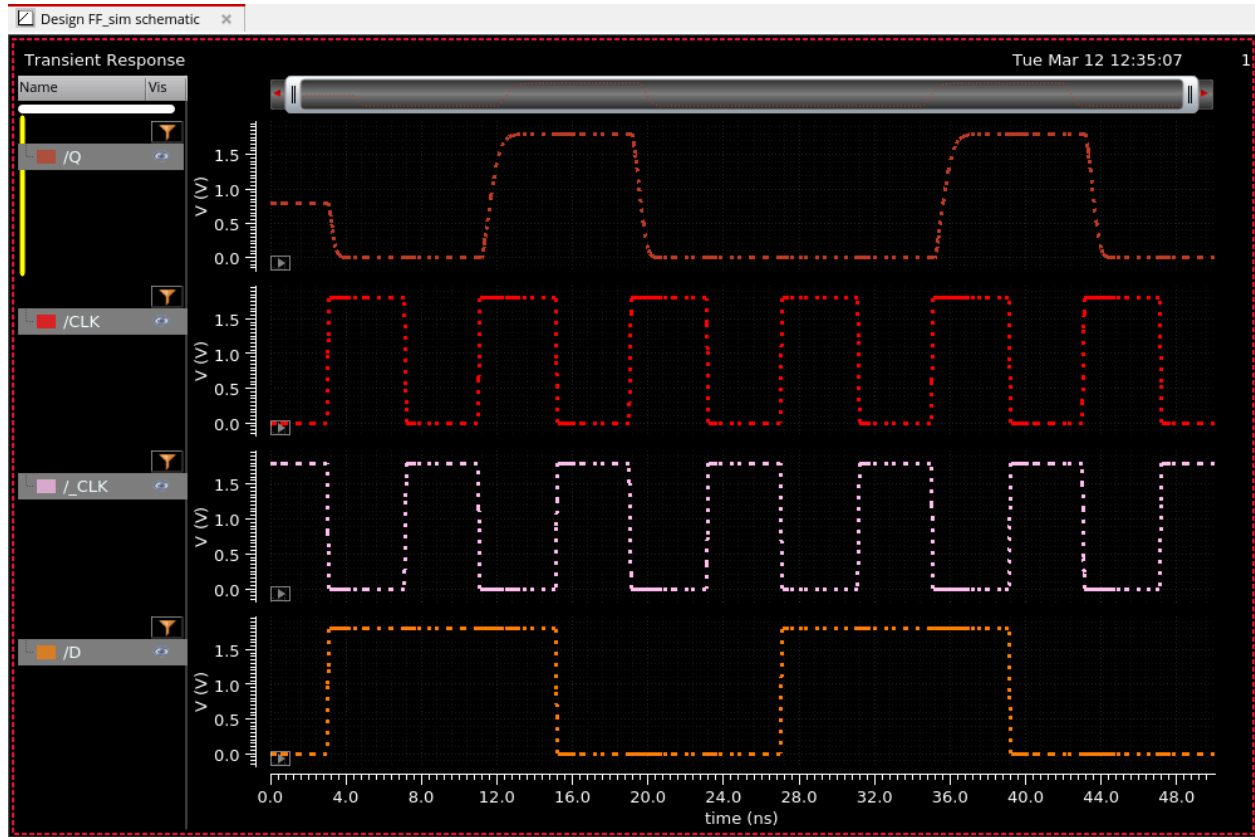
The net-lists match.

              layout  schematic
              instances
un-matched    0      0
rewired       0      0
size errors   0      0
pruned        0      0
active        20     20
```

12

L1 C1

DFF Output waveform

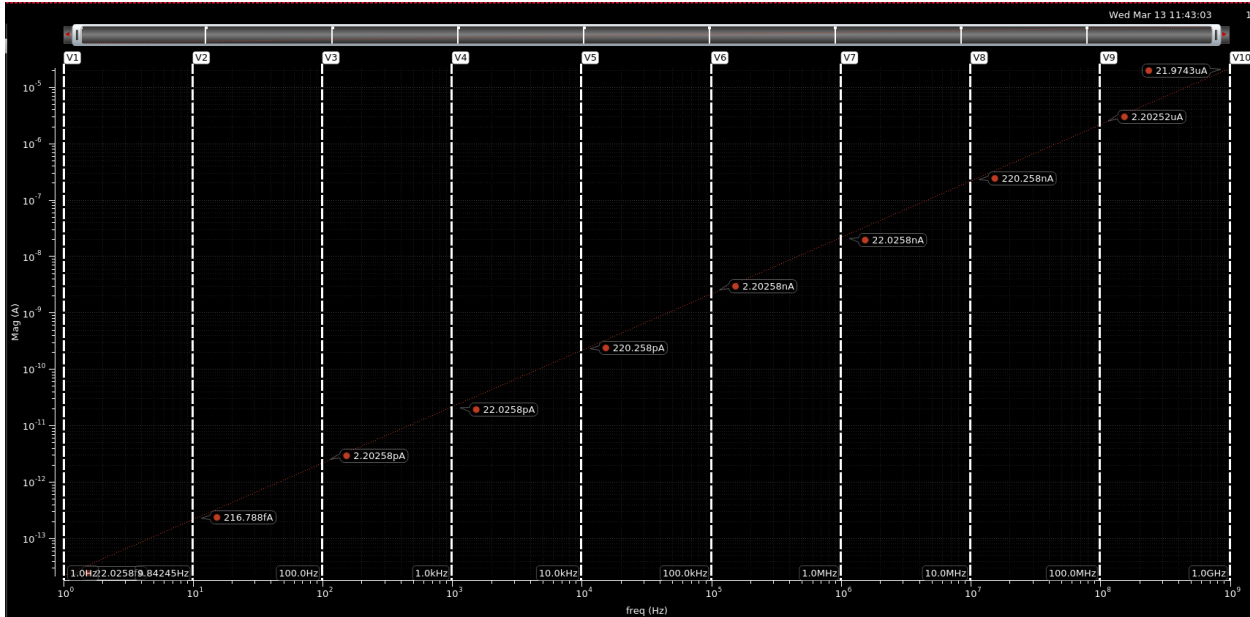


Delay table:

C1	Rising Delay (ns)	Falling Delay (ns)	Error %
100f F	0.6379	0.5943 ns	7.336%
92f F	0.61445	0.5948	3.304%
85f F	0.59231	0.5597	3.261%
78f F	0.56023	0.5235	3.673%
71f F	0.53982	0.49834	4.148%
64f F	0.512	0.48152	5.541%
57f F	0.4747	0.4623	2.682%
50f F	0.4432	0.4123	3.09%
43f F	0.389	0.3711	4.823%
36f F	0.3568	0.3398	1.7%

29f F	0.3158	0.3068	2.934%
22f F	0.2819	0.2698	4.5%
15f F	0.2497	0.244	2.336%
8f F	0.2194	0.2118	3.588%
1f F	0.1836	0.1769	37.874%

Capacitance:

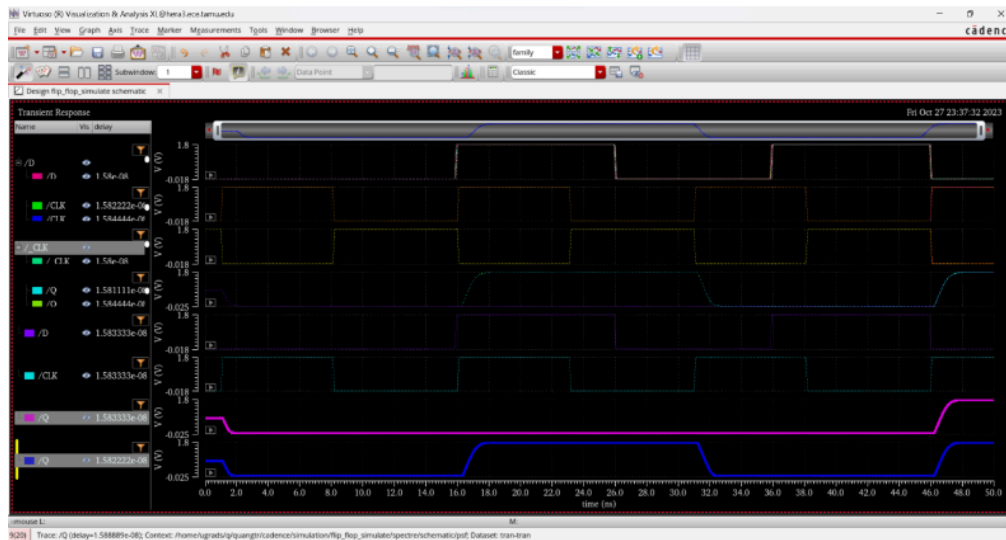


Freq (GHz)	Current (uA)	Input cap
0.1	2.203	3.169
0.2	4.39747	3.499
0.3	6.664	3.535
0.4	8.867	3.528
0.5	11.0557	3.519
0.6	13.258	3.517
0.7	15.29	3.476
0.8	17.631	3.508
0.9	19.811	3.504

1	21.9743	3.497
---	---------	-------

Mean Input Capacitance: 3.475 fF

Setup Time:



Rising delay: 0.1667 ns

Falling delay: 0.0667 ns

Setup time: 0.1667 ns

The time delay for this parametric analysis was ran from 15.8ns to 15.9 ns before a CLK rise time of 16ns. We can see that at time of 15.822ns, the Q output still behaves normally; however, at time of 15.833ns, the Q output failed to rise, so we took the time difference for both rising and falling cases of D input and CLK input at this delay where the longer delay is the setup time.

