Lab Report 5: Design & Simulation of 4-bit adder

ECEN 454/714
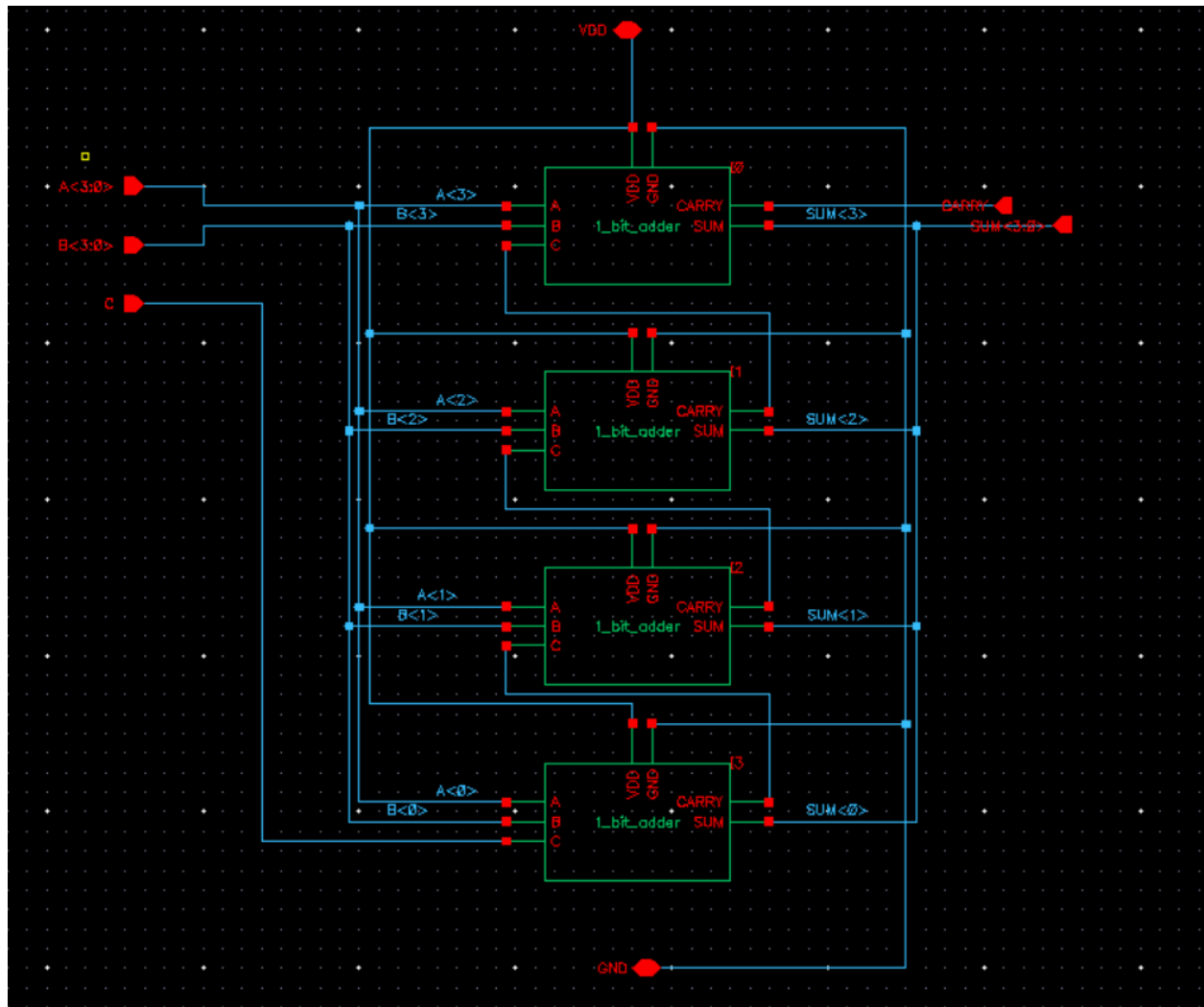3/3/2024

TA: Saichand Samudrala
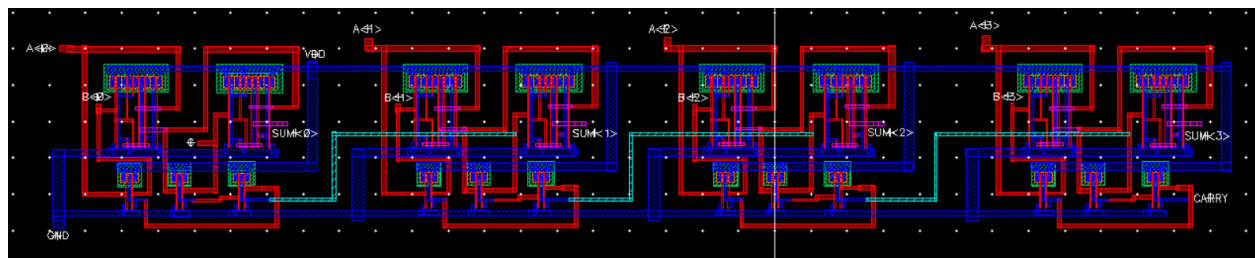
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Schematic of the 4-bit adder:

Layout of the 4-bit adder

LVS Results:

File   Edit   View   Help

cādence

```
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/p/pengryan188/ecen714/LVS/layout/netlist
        count
        91              nets
        16              terminals
        72              pmos
        72              nmos

    Net-list summary for /home/ugrads/p/pengryan188/ecen714/LVS/schematic/netlist
        count
        91              nets
        16              terminals
        72              pmos
        72              nmos


    Terminal correspondence points
    N82       N5         A<0>
    N79       N4         A<1>
    N76       N3         A<2>
    N75       N2         A<3>
    N90       N9         B<0>
    N87       N8         B<1>
    N86       N7         B<2>
    N85       N6         B<3>
    N81       N10        C
    N89       N15        CARRY
    N78       N1         GND
    N84       N14        SUM<0>
    N83       N13        SUM<1>
    N80       N12        SUM<2>
    N77       N11        SUM<3>
    N88       N0         VDD

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.
```
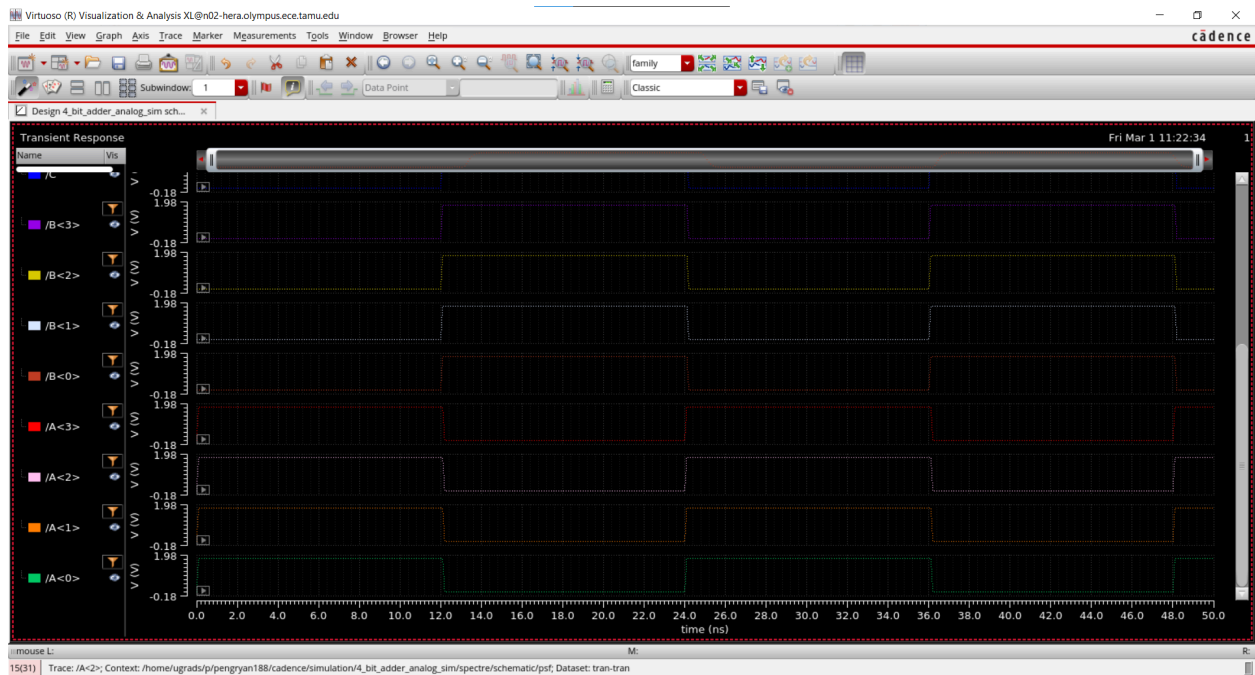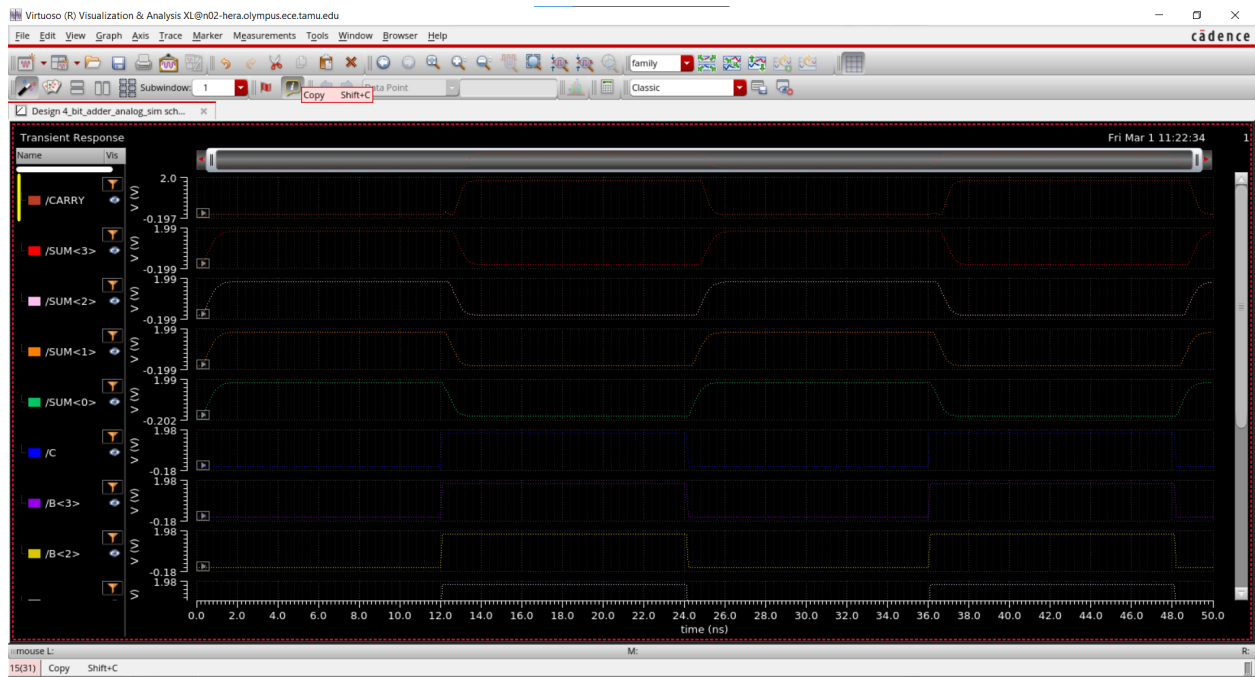
For: A=0000, B=1111, Carry In=1

Waveforms:

Delay Estimate:

	Rising Delay	Falling Delay	Error %
CARRY	1.0075	1.00056	0.68883
SUM<3>	1.0059	1	0.059
SUM<2>	0.80775	0.8013	0.79851
SUM<1>	0.61394	0.6101	0.62547
SUM<0>	0.42417	0.4221	0.48801

Power:

Expression	Value
1 average(i("/V0/P...	-54.46E-6

* 1.8V = -98.028E-5

For A=1010 B=0101 Cin = 0:

Waveforms:

Delay Estimate:

	Rising Delay	Falling Delay	Error %
CARRY	0.9662	0.8743	9.511
SUM<3>	0.9507	0.1552	14
SUM<2>	0.8113	0.7607	6.652
SUM<1>	0.6172	0.6079	1.53
SUM<0>	0.42417	0.4221	0.48801

average(i("/V0/PLUS" ?result "tran"))

Expression	Value
1 average(i("/V0/P...	-53.66E-6

* 1.8V = -96.588E-5

For A=1010 B=0101 Cin = 1
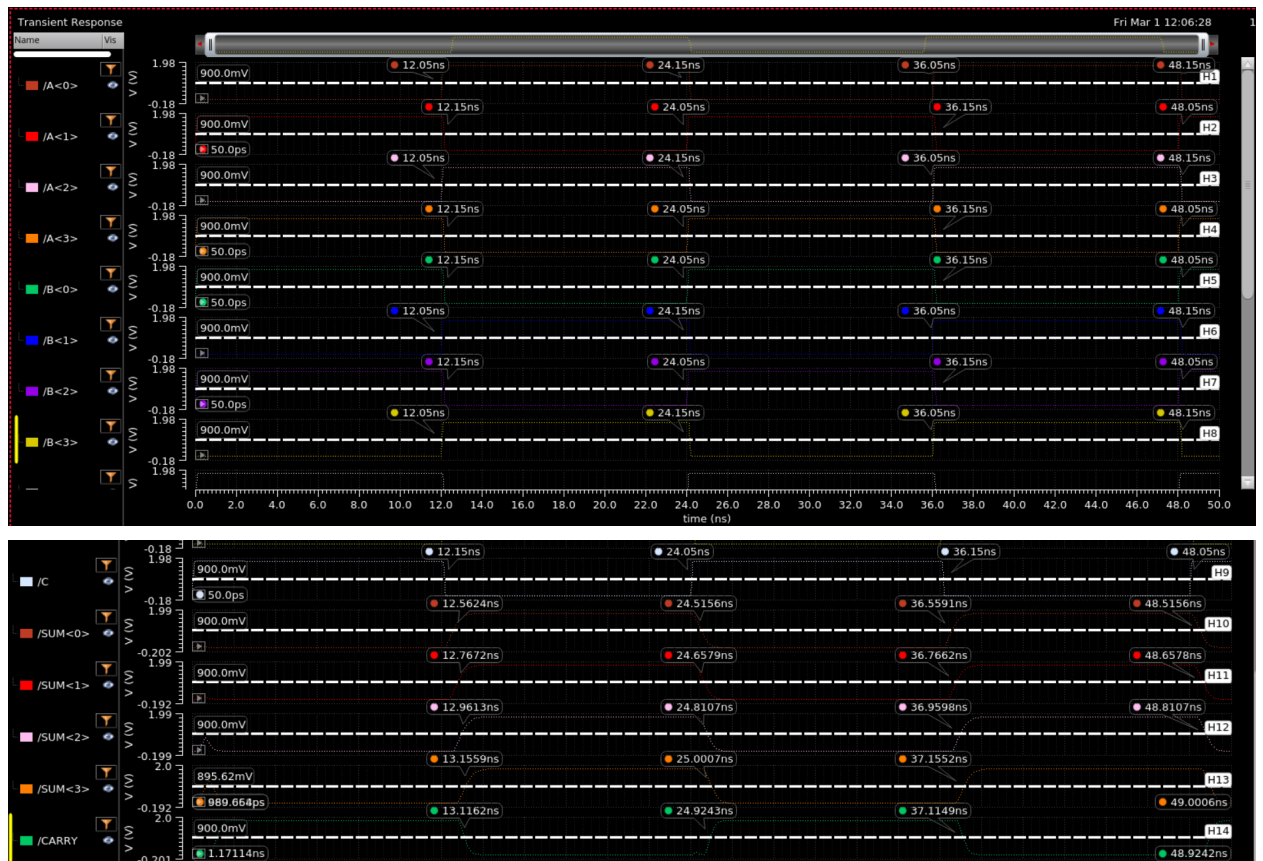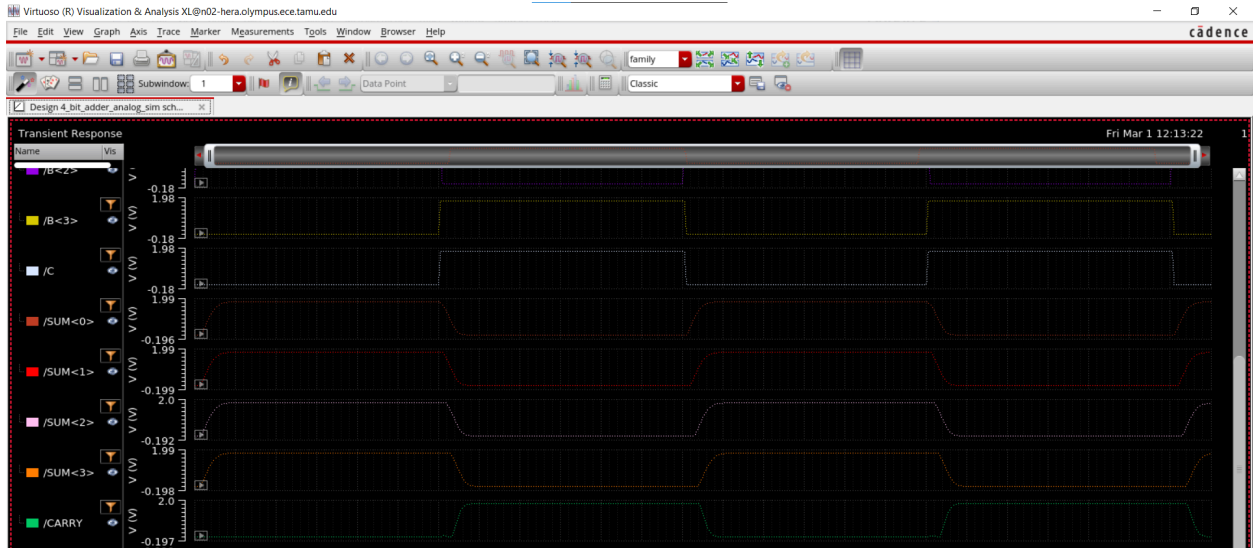
Delay Table:

	Rising Delay	Falling Delay	Error %
CARRY	0.9634	0.8687	10.9
SUM<3>	1.0045	0.9387	7.01
SUM<2>	0.7536	0.8097	7.444
SUM<1>	0.5803	0.6105	5.204
SUM<0>	0.5056	0.5187	2.591

Power:

* 1.8V = -97.974E-5

A=1100, B=1000, Carry In=0
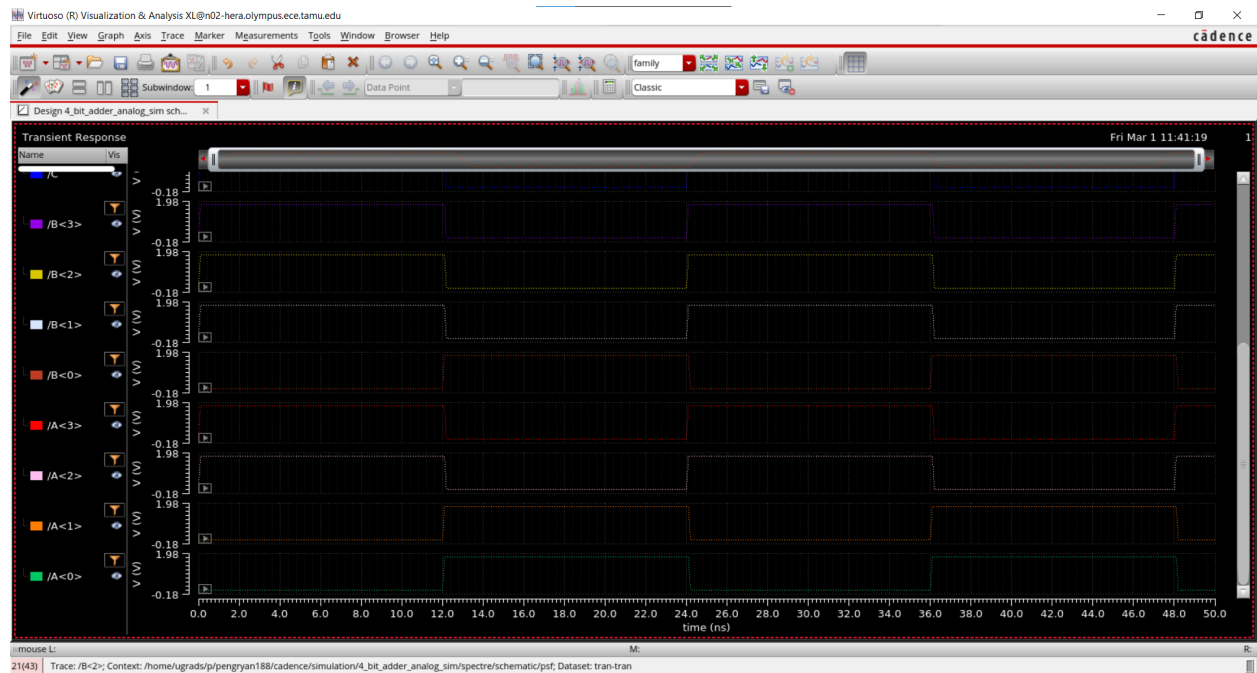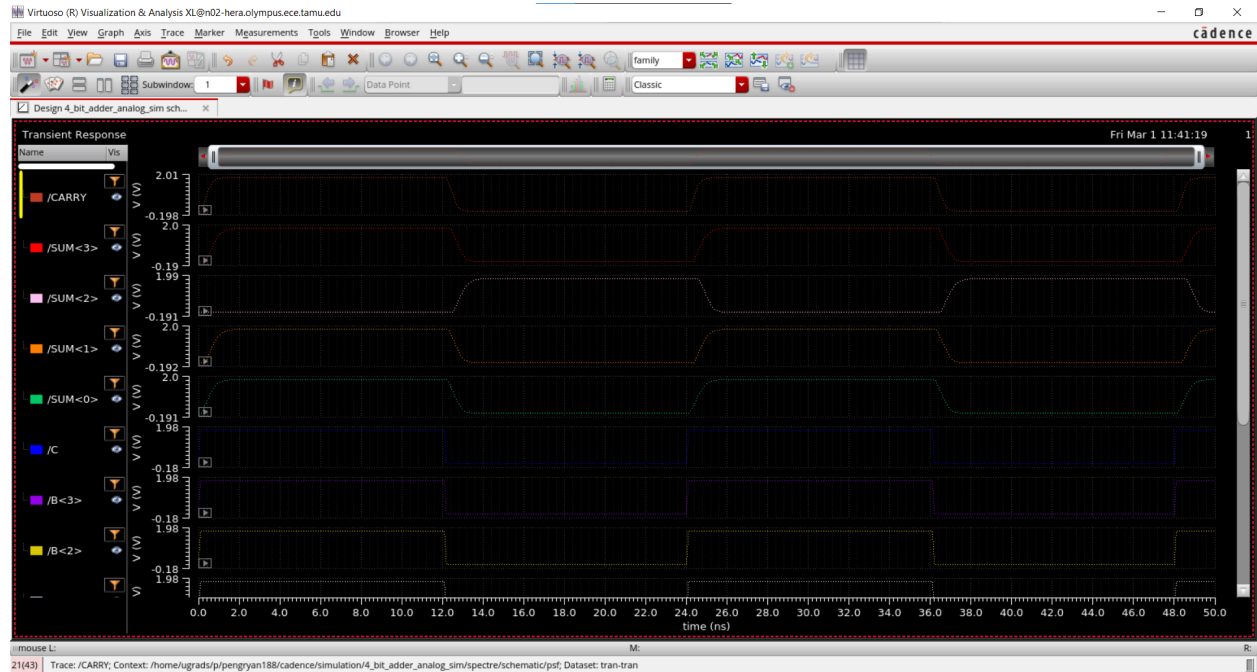
Delay:

	Rising Delay	Falling Delay	Error %
CARRY	0.3597	0.3615	0.5004
SUM<3>	0.635	0.6606	4.031
SUM<2>	0.8502	0.8328	2.089
SUM<1>	0.6297	0.5918	6.404
SUM<0>	0.5716	0.51	12.078

Power:

average(i("/V0/PLUS" ?result "tran"))   ✕

Expression	Value
1 average(i("/V0/P...	-48.53E-6

x 1.8 = -8.6354E-5