Post Lab Report 6: Design & Characterization of a Flip-flop

ECEN 454/714
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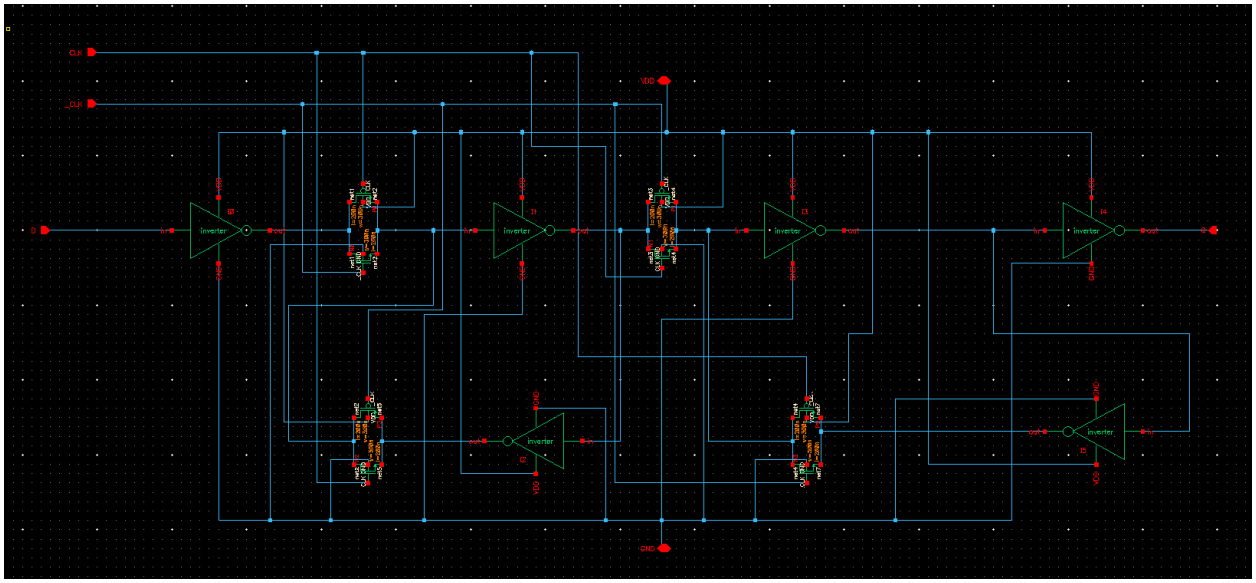
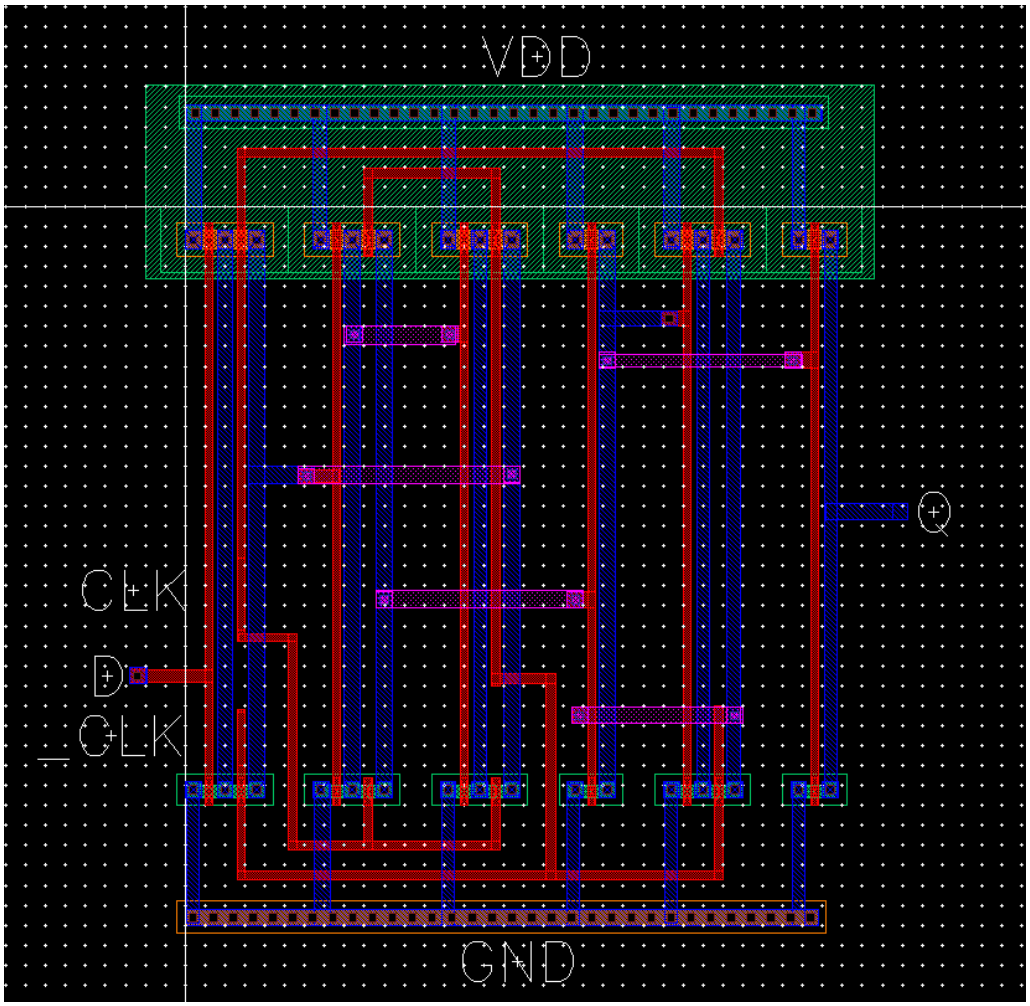
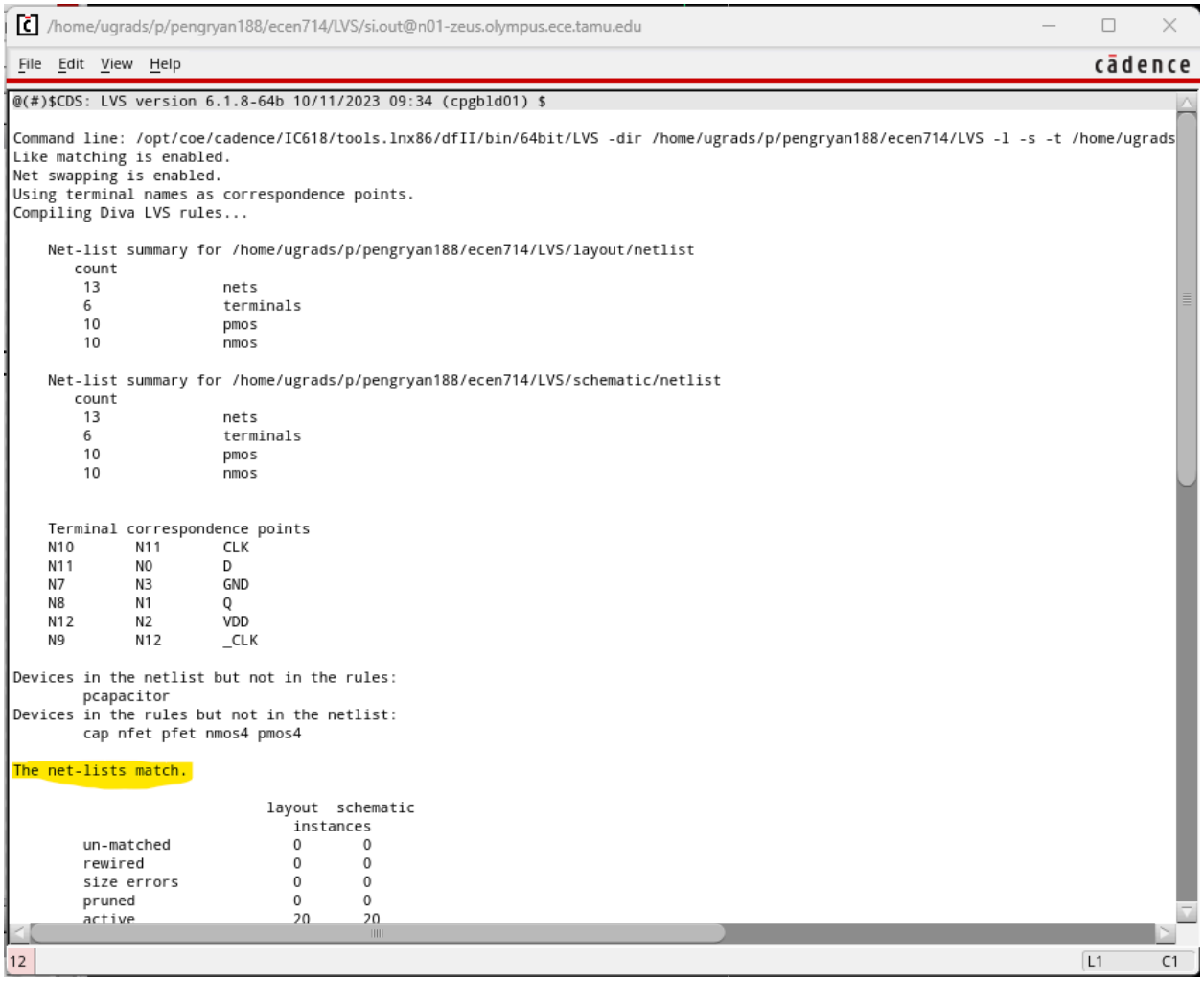
DFF Schematic:



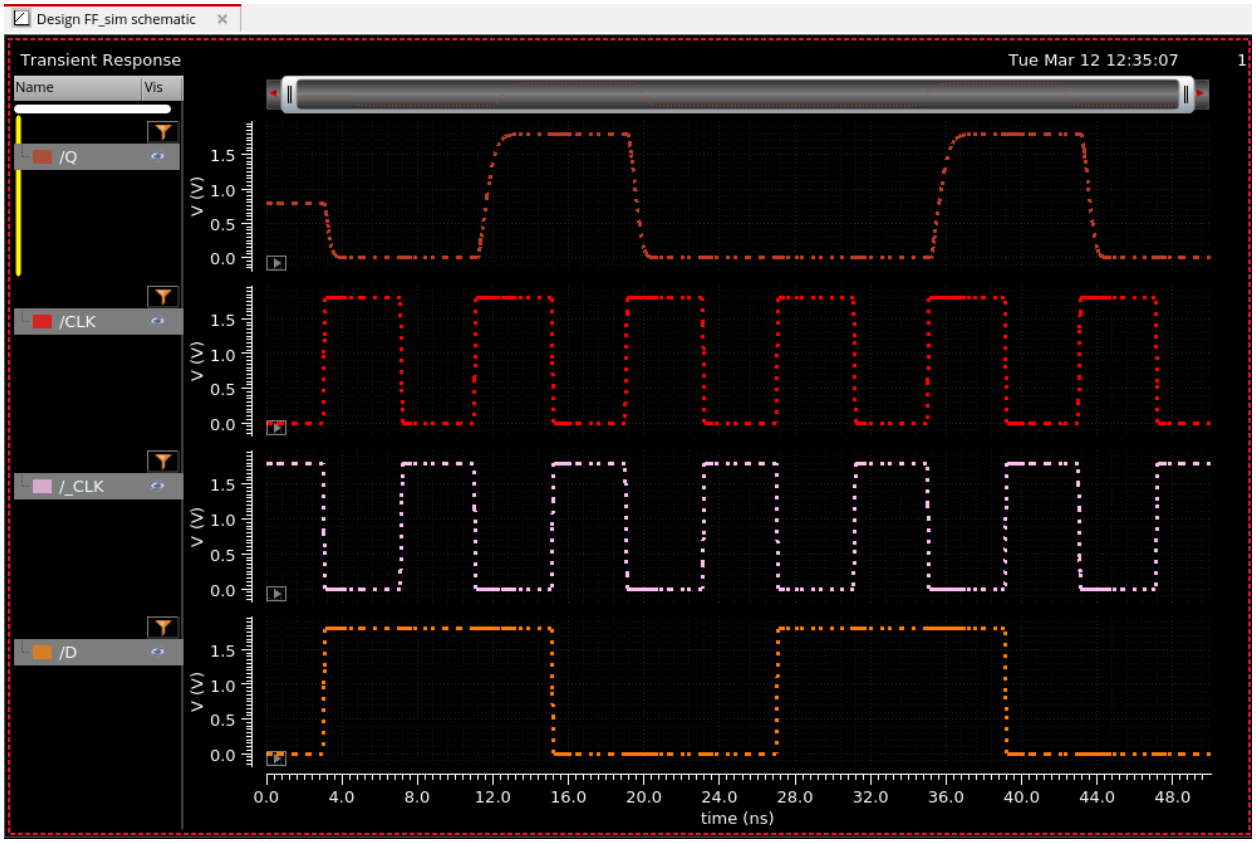
DFF Layout:



DFF LVS Report:



DFF Output waveform

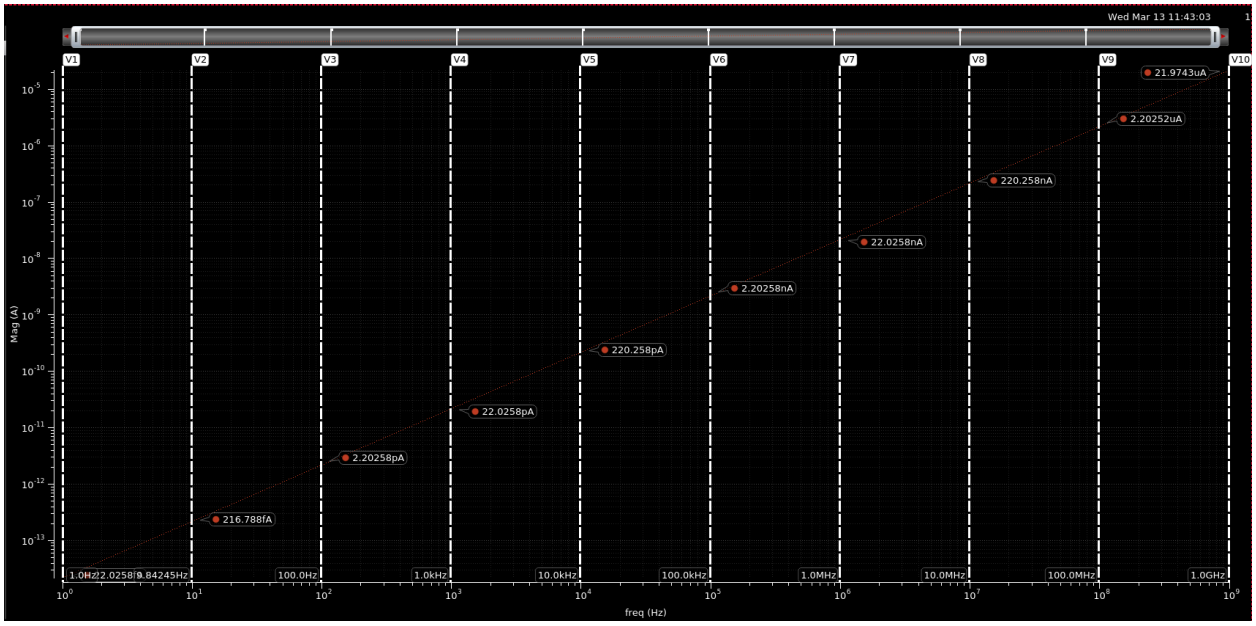


Delay table:

C1	Rising Delay (ns)	Falling Delay (ns)	Error %
100f F	0.6379	0.5943 ns	7.336%
92f F	0.61445	0.5948	3.304%
85f F	0.59231	0.5597	3.261%
78f F	0.56023	0.5235	3.673%
71f F	0.53982	0.49834	4.148%
64f F	0.512	0.48152	5.541%
57f F	0.4747	0.4623	2.682%
50f F	0.4432	0.4123	3.09%
43f F	0.389	0.3711	4.823%
36f F	0.3568	0.3398	1.7%

29f F	0.3158	0.3068	2.934%
22f F	0.2819	0.2698	4.5%
15f F	0.2497	0.244	2.336%
8f F	0.2194	0.2118	3.588%
1f F	0.1836	0.1769	37.874%

Capacitance:

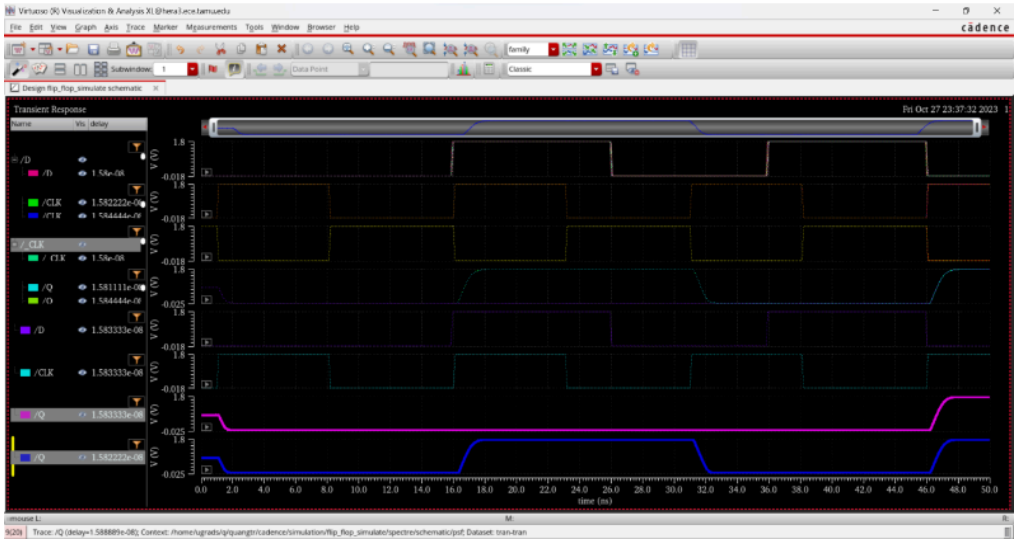


Freq (GHz)	Current (uA)	Input cap
0.1	2.203	3.169
0.2	4.39747	3.499
0.3	6.664	3.535
0.4	8.867	3.528
0.5	11.0557	3.519
0.6	13.258	3.517
0.7	15.29	3.476
0.8	17.631	3.508
0.9	19.811	3.504

1	21.9743	3.497

Mean Input Capacitance: 3.475 fF

Setup Time:



Rising delay: 0.1667 ns
Falling delay: 0.0667 ns
Setup time: 0.1667 ns

The time delay for this parametric analysis was ran from 15.8ns to 15.9 ns before a CLK rise time of 16ns. We can see that at time of 15.822ns, the Q output still behaves normally; however, at time of 1.5833ns, the Q output failed to rise, so we took the time difference for both rising and falling cases of D input and CLK input at this delay where the longer delay is the setup time.