Lab Report 2: Cadence Custom Layout: Design Rules, Extraction, and Verification

ECEN 454/714
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For the NOT/inverter gate, I designed the following schematic, with a down down NMOS network and a pull up PMOS network:

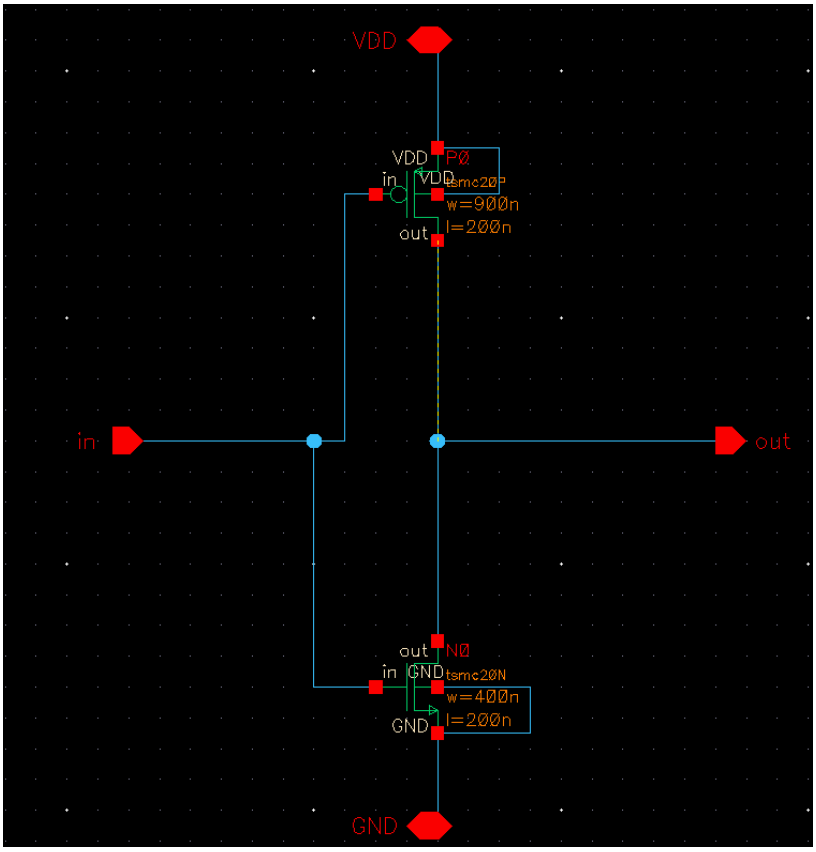


Figure 1: NOT gate schematic view

Then, we created a symbol view for the symbol. I created a custom symbol in the symbol view by deleting the original bounds, and keeping the instance name, part name, and the pinout. I then created a symbol:

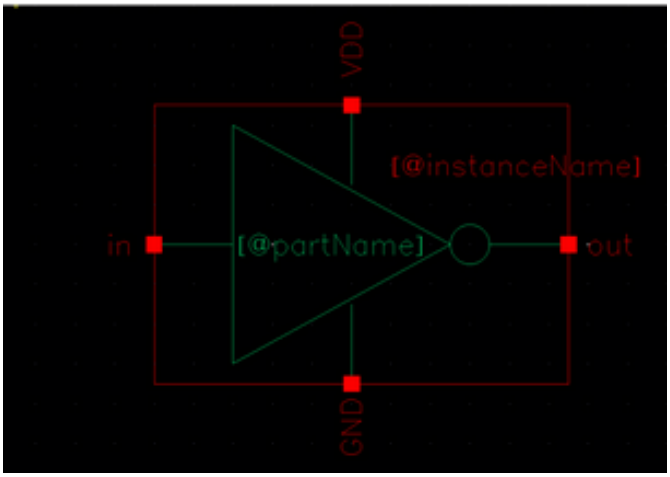


Figure 2: NOT gate symbol view

Afterwards, I made a layout view depicting the layers involved in the design:

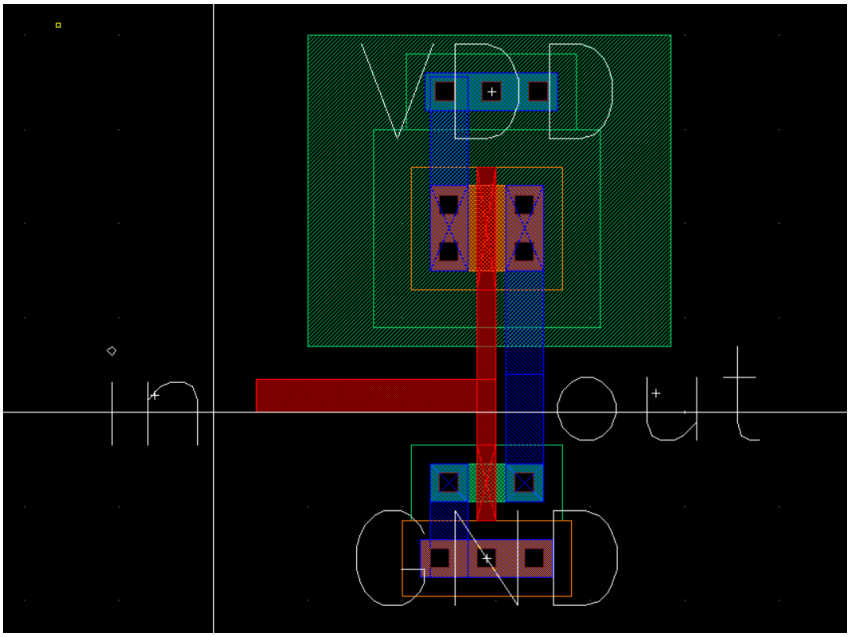


Figure 3: Layout view of a NOT gate

Lastly, I extracted it to the extracted view:

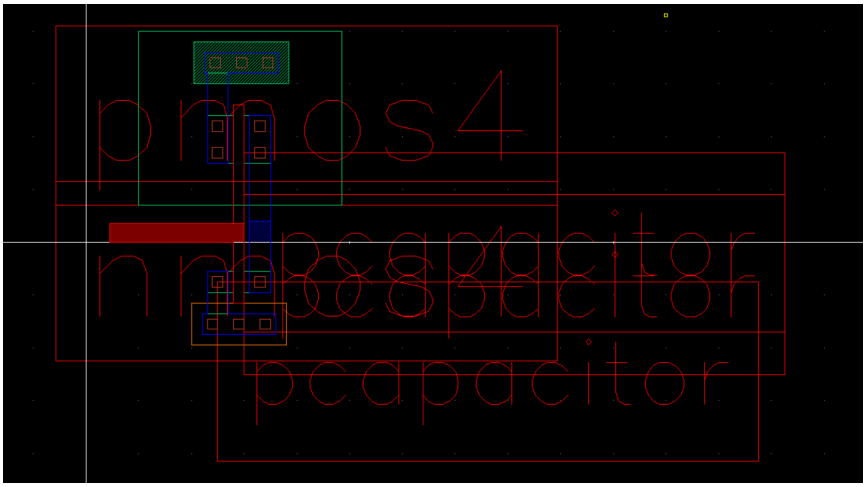


Figure 4: Extracted view of the NOT gate

To verify everything worked properly, we did a LVS report:

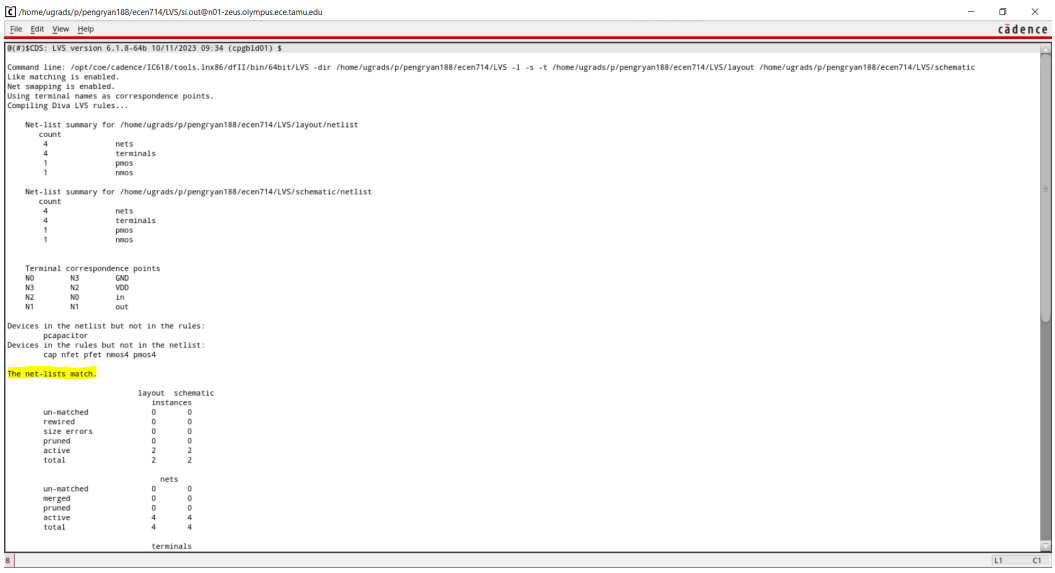


Figure 5: LVS report of the NOT gate

NAND2:

We repeat the process for the NAND2 component:

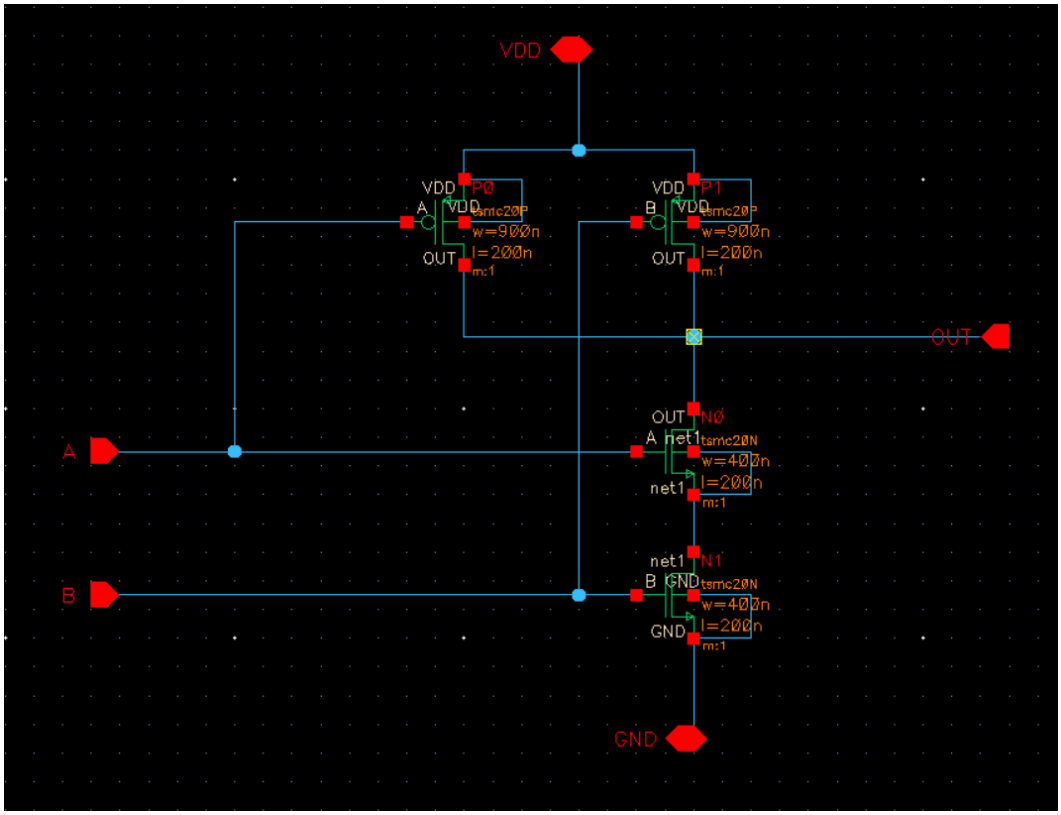


Figure 6: Schematic view of the NAND2 gate

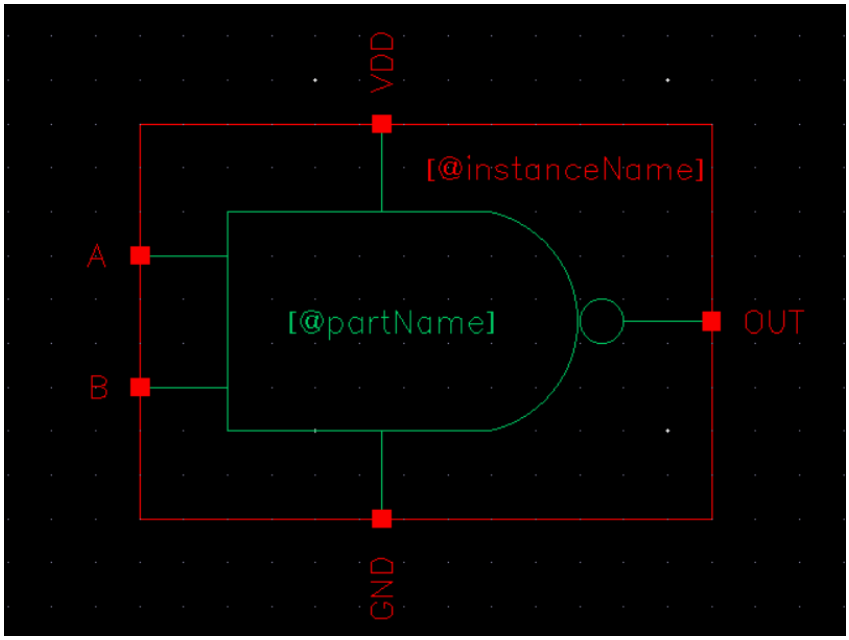


Figure 7: Symbol view of the NAND2 gate

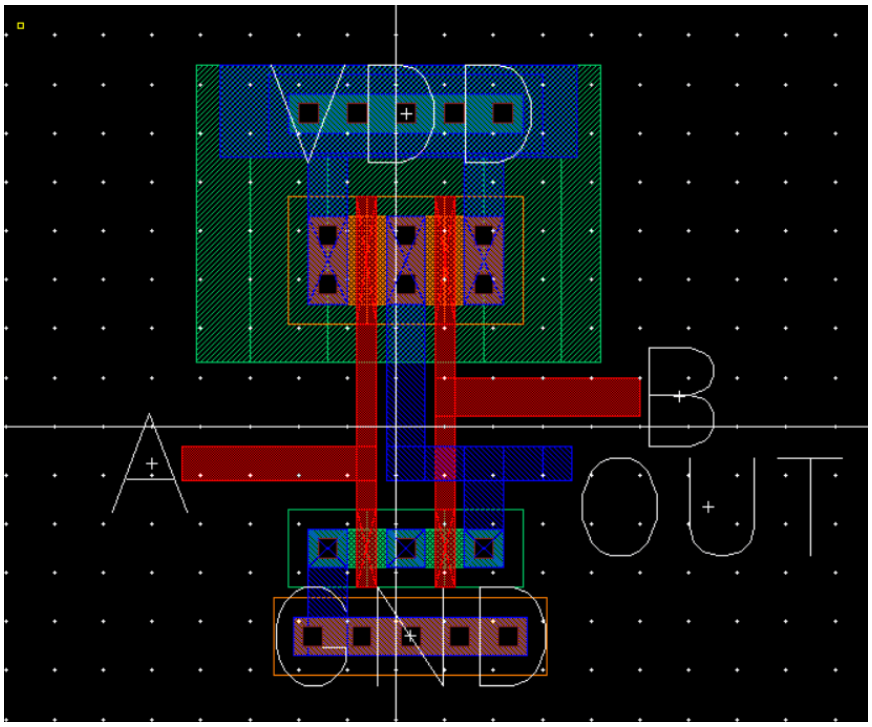


Figure 8: Layout view of the NAND2 gate

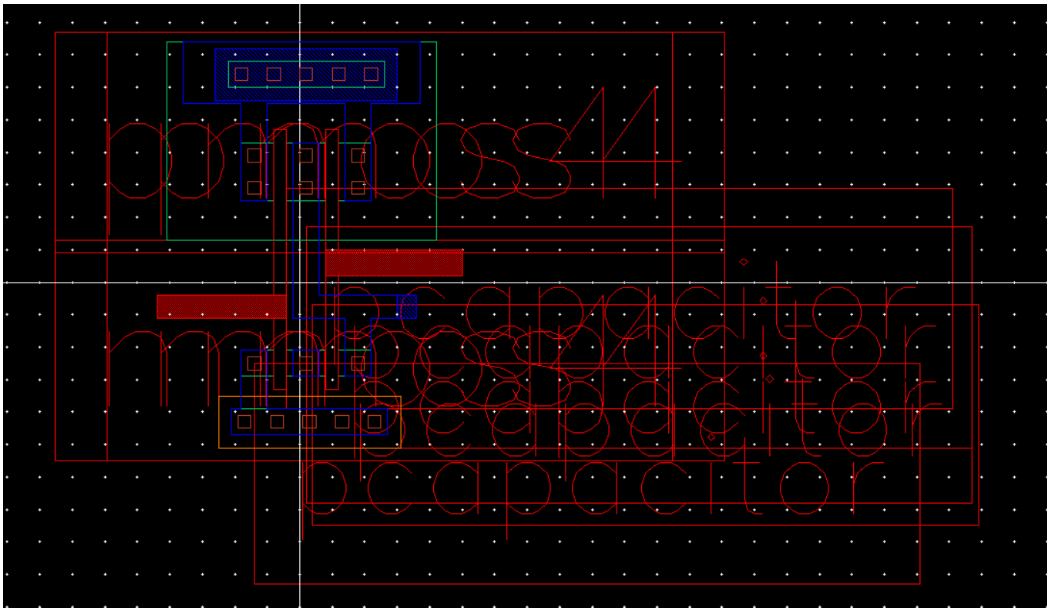
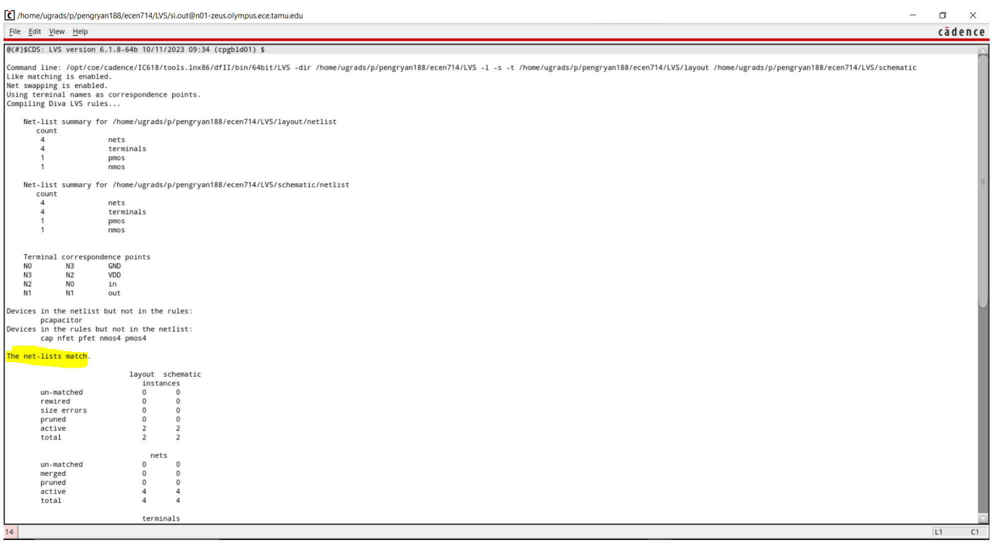


Figure 9: Extracted view of the NAND2 gate



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/home/ugrads/p/pengryan188/ecen714/LVS/si.out@n01-zeus.olympus.ece.tamu.edu
File  Edit  View  Help                                                    cādence
@(#)$CDS: LVS version 6.1.8-64b 10/11/2023 09:34 (cpgbld01) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/p/pengryan188/ecen714/LVS -l -s -t /home/ugrads/p/pengryan188/ecen714/LVS/layout /home/ugrads/p/pengryan188/ecen714/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/p/pengryan188/ecen714/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/ugrads/p/pengryan188/ecen714/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N0        N3        GND
    N3        N2        VDD
    N2        N0        in
    N1        N1        out

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0        0
        rewired                 0        0
        size errors             0        0
        pruned                  0        0
        active                  2        2
        total                   2        2

                                  nets
        un-matched              0        0
        merged                  0        0
        pruned                  0        0
        active                  4        4
        total                   4        4

                                terminals
14
```

Figure 10: LVS Report for the NAND2 gate

XOR2:

Lastly, we repeated the same steps for the XOR2 gate:

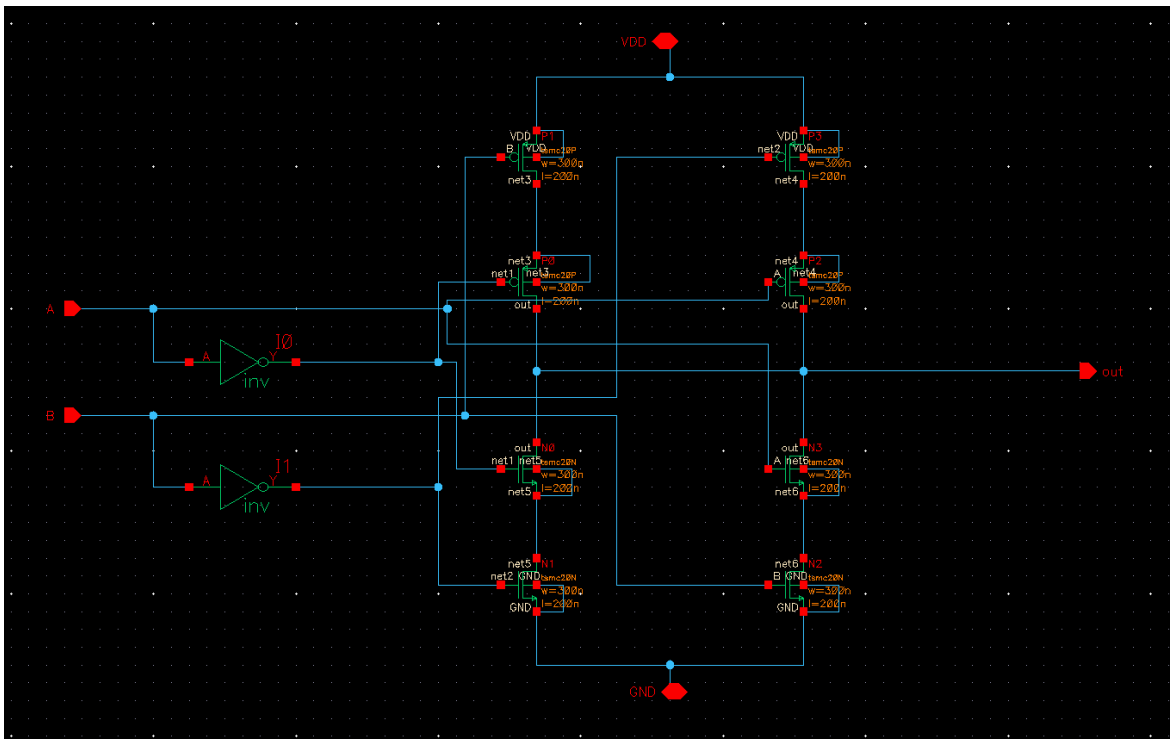

Figure 11: Schematic of the XOR2 gate

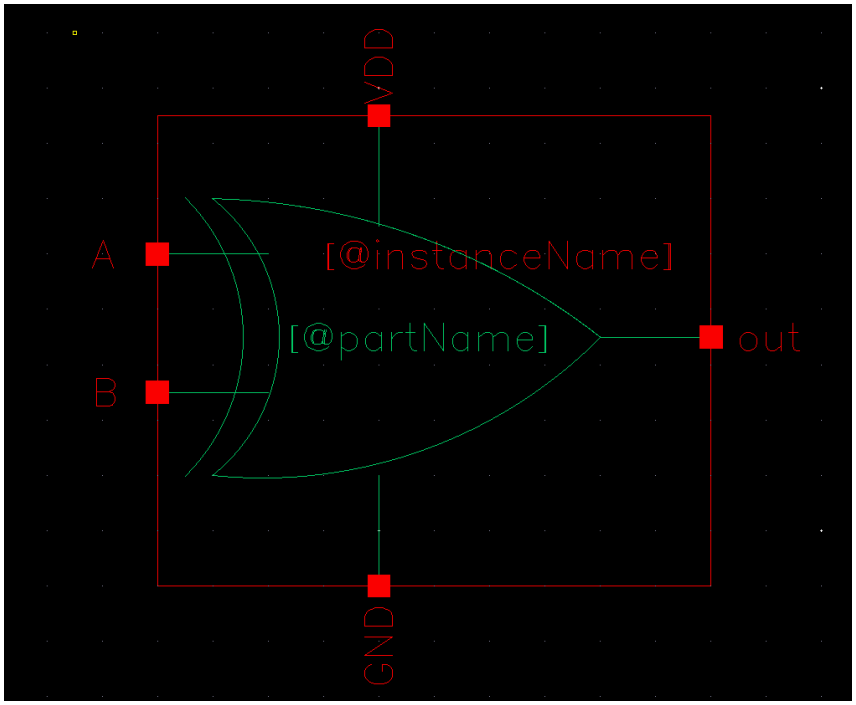

Figure 12: Symbol view of the XOR2 gate

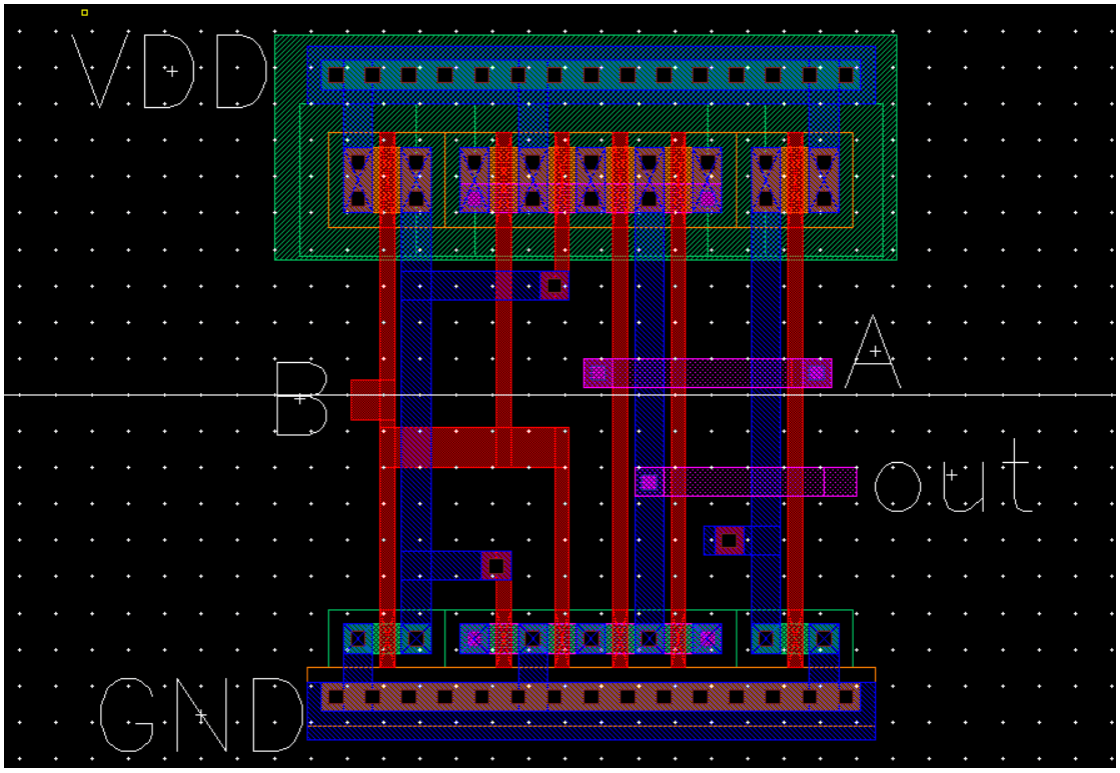

Figure 13: Layout view of the XOR2 gate

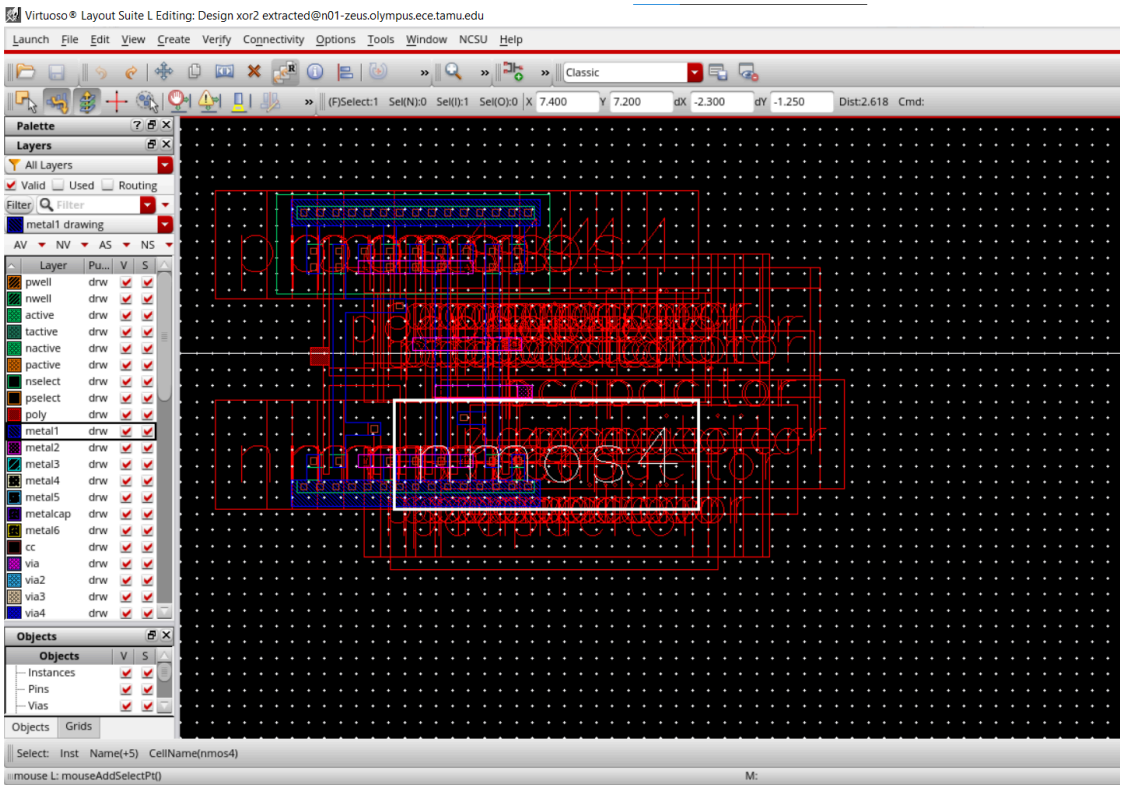

Figure 14: Extracted view of the XOR2 gate

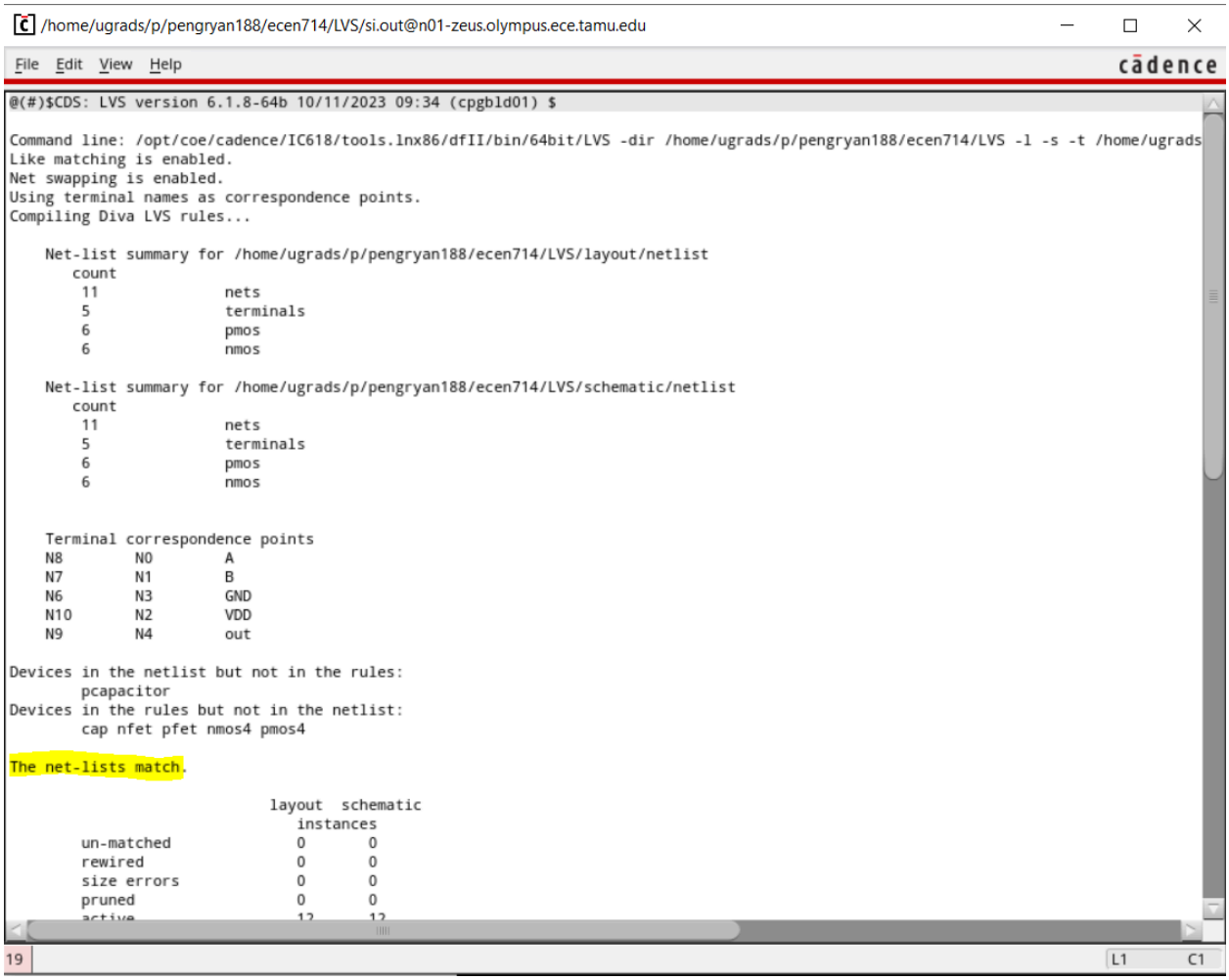

Figure 15: LVS Report for the XOR2 gate