A 14-16 GHz Parallel Sliding-IF Receiver Front-End on 45nm CMOS for 6G Low-Band Applications

Ryan Wans , *Student, Purdue University*

***Abstract*—In this paper, we introduce a sliding-IF receiver architecture implemented in 45nm CMOS for the anticipated 6G low-band (14-16 GHz). Our implementation is complete with amplifiers, mixers, and a VCO that fully enables the sliding-IF architecture. First, an LNA with gain of 21.4 dB and NF of 980 mdB is designed to meet low SNR requirements. Next, passive double-balanced mixers are used to down-convert to the intermediate frequency (IF) band before parallel IQ mixers further down-convert to baseband (BB). Also on-chip is an LC-VCO with injection-locked frequency dividers to generate an LO for the mixers. All together, this receiver achives a gain of -9.2 dB with a NF of 9.7 dB across 14-16 GHz.**

***Index Terms*—6G, CMOS, LNA, sliding-IF, mixer, VCO, receiver, IQ, OFDMA, ILFD, IEEE 802.16.**

I. Introduction

With the onset of increasing demands for wireless networks, 6th generation (6G) technology is expected to rely on even higher frequency bands than its predecessors. This introduces several design challenges that impede the implementation of this standard. Of these are the demand for higher efficiency, lower cost devices that are able to support the stringent requirements of the standards, such as OFDM-based modulation schemes. To meet these needs, much attention has shifted to CMOS technology due to its low cost, low power consumption, and high f_T devices. Furthermore, the ability to down-convert IQ signals is of utmost importance for the latest modulation schemes. To this end, we propose using the sliding-IF archiecture, shown in Figure 1. Aside from the ability to down-convert IQ, it combines the benefits of a two-stage conversion (better linearity and noise) and single-stage conversion (lower power consumption, one LO). This is achieved by sliding the LO, affecting both the IF and BB bands.

II. Sliding IF Receivers

The sliding-IF receiver has been explored all across the millimeter-wave (mm-wave) spectrum, from 2.4 GHz [1], to 5 GHz [2], 28 GHz [3], 40 GHz [4], 220 GHz [5], and even 300 GHz [6]. The boilerplate architecture is shown in Figure 1. Some designs use a VCO to generate the LO for the BB mixers, and then rely on multiplication for the IF mixer [4], [5], [7]. In this design, we choose to rely on LO division with quadrature output instead, similar to [2]. Frequency division offers the advantages of better phase noise, smaller passives, and avoid the harmonic generation of multipliers. Common realizations of mm-wave frequency division include regenerative frequency dividers [8] and injection-locked dividers [9], [10]. Injection-locking implementations such as [9] build off of the usual cross-coupled pair (XCP) architecture while affording the benefit of quadrature output. On the other hand, frequency multipliers such as [11] offer simpler implementation with fundamental rejection but require a lower LO frequency.

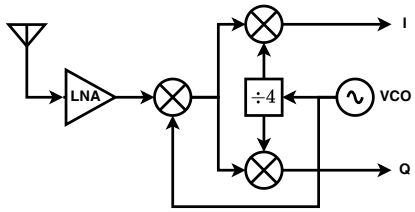

Fig. 1. Sliding-IF receiver block diagram.

At our target frequencies of 14-16 GHz, as in [1] and [2], it is impractical to rely on distributed elements and transmission lines. As a result, we will not have to worry about power dividers and the impedance matching of wires.

For receivers which rely on their own LO generation [4], it is most common to use an LC-VCO implementation such as in [12]. The advantage of this is the ability to slide the IF on-chip and reduce the necessary components off-chip. Passive LC components in the 14-16 GHz range are easily integrated on-chip without consuming too much area.

Among mixer topologies used in current implementations, the doubled-balanced Gilbert cell is the most popular choice [4]–[7], while others rely on passive mixers [2], [3]. Gilbert cell-based topologies offer better conversion gain and higher linearity while passive mixers afford lower noise figure and no LO-induced flicker noise.

III. Proposed Implementation

A. Cascode Low Noise Amplifier

We've chosen to implement a cascode topology with inductive source degeneration and input/output matching as shown in Fig. 2(a). The gate and source inductors of M1 are chosen such that the input impedance, given by

$$Z_{in} = \frac{g_{m1}L_s}{C_{gs1}} + j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs1}},$$

is matched to 50Ω. A bias tee is also implemented off-chip in order to keep M1 in saturation. The sizing of M1 and M2 determine the drain current, which is picked to strike a

Contact: wansr@purdue.edu
For Purdue ECE60420 RFIC Design Fall 2025.

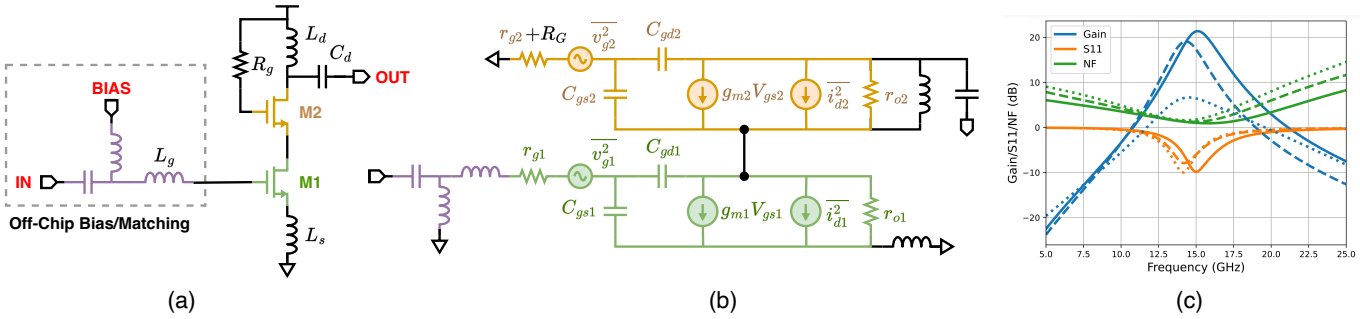

Fig. 2. (a) Schematic of LNA, (b) its equivalent noise model, and (c) simulated gain, S11, and noise figure with postlayout (dashed) and EMX (dotted).

balance between low power consumption, low noise figure, sufficient output swing, and input/output matching. The small signal noise model in Fig. 2(b) elucidates ways to reduce the amplifier noise figure. Increasing the finger count of M1 and M2 effectively reduces gate resistance r_g and since

$$\overline{v_g^2} = 4kTR\Delta f, \quad \overline{i_d^2} = 4kT\gamma g_m \Delta f,$$

it reduces the overall noise. Hence, decreasing transistor sizing or drain current will also reduce g_m and thus noise. One should also care for the parasitic series resistance posed by larger inductors when sizing them, which will add to the noise. Finally, drain inductor L_d is chosen to strike a balance between gain, area, and ease of output matching, which hence determines C_d.

Simulated gain, NF, and S11 are depicted in Fig. 2(c). A suitable gain of 21.4 dB, NF of 980 mdB, and S11 close to -10 dB occur at the center frequency of 15 GHz. Over the target bandwidth of 14-16 GHz, the simulated gain is above 19.7 dB and NF is below 1.2 dB. An I_d of 2.9 mA with sizing ratio of 533 was chosen in our implementation.

B. LC-VCO

In the interest of reasonable power consumption, tunability, and stability, an LC-VCO topology with NMOS and PMOS cross-coupled pairs (XCPs) was chosen as shown in Fig. 3(a). An LC tank is formed using an inductor with MOS varactors tuned by V_{tune}. Increasing V_{tune} causes the effective capacitance to increase, and hence the resonant frequency to decrease. The XCP circuits create a negative g_m, and hence resistance, when looking into the drains (from the LC tank). This effect allows us to tune the XCP g_m to counteract the parasitic parallel resistance caused by the inductor:

$$R_P = \frac{(\omega_0 L)^2}{R_S} = Q_L^2 R_S$$

Thus in order to ensure that the XCP can sufficienyly overcome losses faced by tank, we desire

$$g_m > \alpha \left(Z_0 + \frac{1}{Q_L \omega_0 L} + \frac{w_0 C}{Q_C} \right)$$

where $\alpha > 3$ is a safety factor to ensure startup of the oscillator. This ensures the poles of the transfer function of our oscillator on well within the right half-plane and any noise transient will kick-start it.

There are several benefits to employing both NMOS and PMOS XCPs. Aside from a trivially higher $-g_m$ in the circuits, we also eliminate the need for a tail current source and gain the ability to tune the biasing/swing of the output waveform. Since both XCPs rely on the same drain current, we also increase the efficiency of the VCO; our implementation consumes only 154 μA.

The output from the tank is then DC-decoupled and buffered so as not to load the tank. The transimpedance amplifier (TIA) buffers, depicted in Fig. 3(b), also allow us to further amplifier or tune the output. Our implementation, like many others in modern literature, replaces the feedback resistor with a PMOS with its gate and source tied.

C. Double-Balanced Passive Mixer

The chosen prototypical topology is shown in Fig. 3(c), utilizing just 4 FETs and no power requirement. The only degree of freedom here is the sizing of FET. Hence by tuning this value, we aim to strike a tradeoff between conversion gain, noise figure, P1dB, and port-to-port isolation.

The RF and LO ports are fed at 50% cycle into their respective ports and an IF is generated at the output also at 50% duty cycle. The goal is for each FET to act as an ideal switch, where the alternating LO+ and LO- signals gate the RF+/RF- inputs, creating a mixing product at the output. Accordingly, the bias and amplitude of the LO, as well as power of the RF signal, determine the conversion gain.

$$G_C = \frac{2}{\pi} \cdot \frac{R_L}{R_S + R_L + R_{on}}$$

Given that $G_C \geq 2/\pi \approx 0.637$, the minimum conversion loss will be 3.92 dB. Nonzero R_{on}, parasitics, and mismatch, all contribute to a higher conversion loss. Each output of our receiver will have been mixed twice, and hence a minimum total conversion loss of 7.84 dB is to be expected. IIP3 and P1dB can both be improved by increasing the power of LO.

D. Injection-Locked Frequency Divider

The beauty of the sliding-IF architecture lies in its ability easily tune both mixers of a dual conversion receiver from one LO. We accomplish this by dividing our LO frequency by 4 before down converting again. This is realized via cascaded injection-locked frequency dividers (ILFDs) with a quadrature output as shown in Fig. 3(d). The topology and theory are

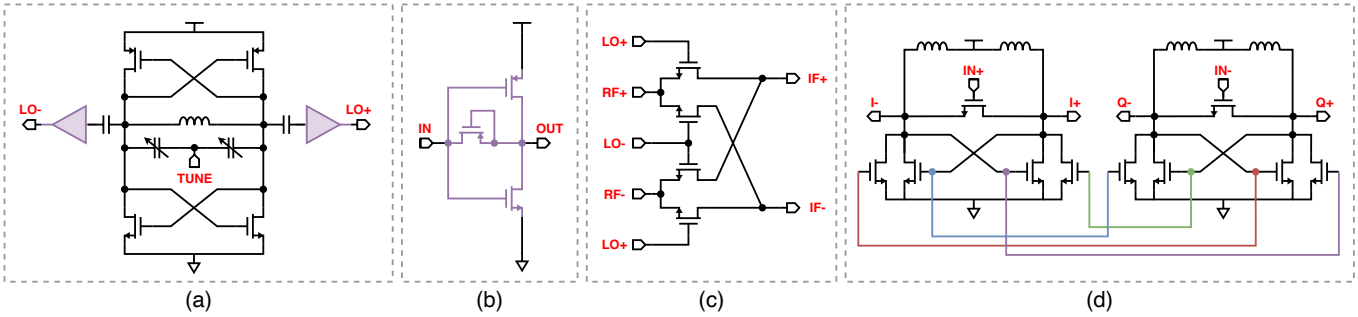

Fig. 3. Schematics of (a) LC-VCO, (b) VCO output buffers, (c) passive double-balanced mixer, and (d) ILFD with quadrature output.

strikingly similar to that of the LC-VCO and passive mixer from before! Each input FET acts as a mixer and since the current in each branch is the second harmonic of the input frequency, there is an innate division by two. Hence,

$$\omega_0 = \omega_{in} - N\omega_0 \iff \omega_0 = \frac{\omega_{in}}{N+1},$$

and for $N = 1$, we're effectively feeding the IF back into the LO of a passive mixer. As derived in [10], we've that

$$\omega_L = \frac{\omega_0}{2Q} \cdot \frac{i_{inj}}{i_T}$$

whence the locking frequency ω_L and range can be optimized by minimizing Q of the tank or maximizing injection current i_{inj}. The output is intrinsically differential, and by coupling two ILFDs as in Fig. 3(d), we achieve 4-phase quadrature output for I/Q down conversion.

IV. Simulation Results & Comparison

The proposed sliding-IF receiver was design and simulated using GPDK 45nm. Afterwards, both post-layout and EMX simulations were conducted for comparison. The LNA and LC-VCO were also individually simulated.

In post-layout, the overall system gain decreased to -11.5 dB, NF increased to 12/16.7 dB, P1dB decreased to -41.4 dB, and power consumption decreased to 45.8 mW. The LC-VCO has phase noise of -101 dBc/Hz, a $V_{tune} = 0$ frequency of 11.5 GHz, and stopped oscillating for $V_{tune} = 1$. The LNA center frequency shifted to 14.2 GHz, had a gain of 19.2 dB, NF of 1.38 dB, S11 of -7.9 dB, and P1dB of -19.2 dB. The pre- and post-layout and EMX simulations for the LNA are shown in Fig. 2(c).

Electromagnetic Extraction (EMX) was then conducted for the full system, the LC-VCO, and the LNA. The overall system exhibited a gain of -39.4 dB, NF of 22.2/23.9 dB, and power consumption of 11.4 mW. PSS analysis did not converge, so P1dB and VCO measurements are missing. The LNA exhibited a center frequency of 14.6 GHz, gain of 6.7 dB, NF of 1.63 dB, S11 of -9.97 dB (at 14.15 GHz), and P1dB of -14.9 dB. These figures are not terribly far off from our pre-layout simulations, indicating strong layout.

The pre-layout system-level results are shown and compared against state-of-the-art sliding-IF receivers in Table I. Our design exhibits significantly lower gain than other results due to passive mixers and lack of IF amplifiers. We suspect this contributed to lower P1dB and NF as well, though our NF is relatively good. Due to the integration of 3 total ILFDs (divisin by 2 twice), we exhibited relatively large power consumption as well. These figures can be improved by implementing active mixers, additional IF amplifiers if needed, and optimizing ILFD operation (perhaps at the loss of locking range). Finally, we exhibited a good LO phase noise result.

V. Conclusion

In this project, we designed and simulated a sliding-IF receiver on 45nm CMOS for the 14-16 GHz band. We integrated a cascode LNA, passive double-balanced mixer, LC-VCO, and ILFDs to achieve this. We presented novel results of using a passive mixer in this archiecture and showed its effect on gain. Finally, we concluded by comparing to other recent results and recommending improvements.

TABLE I
Comparison to State-Of-The-Art Sliding-IF Receivers

Ref.	Tech.	Freq. (GHz)	Gain (dB)	NF (dB)	P1dB (dBm)	Power (mW)	Area (mm^2)	LO Phase Noise (dBc/Hz) @ 10 MHz Offset
[2]	65nm	5.1-5.9	39	1.9/2.4	-28.5	72	0.56	
[3]	22nm FDSOI	28	37.5	3.5	-31	19.5		
[4]	65nm	61.5-66.5	28	9	-26	80	0.5	-115 @ 64 GHz
[6]	130nm SiGe	187-313	15.2	29.5	-17	406	2	
[7]	22nm SOI	137-156	30	9/10.5	-29	197.5	3.10	
This Work	**45nm**	**14-16**	**-9.2***	**9.7/14.2**	**-40**	**188†**	**0.21**	**-127 @ 16 GHz**

*Passive mixers and no IF amplifier, †Includes frequency dividers

REFERENCES

[1] S. Lee, D. Jeong, and B. Kim, "Ultralow-Power 2.4-GHz Receiver With All Passive Sliding-IF Mixer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 5, pp. 2356–2362, May 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8288686/

[2] K. Yang, X. Yi, C. C. Boon, Z. Liang, G. Feng, C. Li, and L. Bei, "A Parallel Sliding-IF Receiver Front-End With Sub-2-dB Noise Figure for 5–6-GHz WLAN Carrier Aggregation," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 2, pp. 392–403, Feb. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9169712/

[3] S. J. Fang, F. Zhang, A. Bellaouar, and S. Embabi, "A 28GHz Sliding-IF Receiver in 22nm FDSOI," in *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*. Cracow, Poland: IEEE, Sep. 2019, pp. 385–388. [Online]. Available: https://ieeexplore.ieee.org/document/8902515/

[4] S. Bozzola, D. Guermandi, F. Vecchi, M. Repossi, M. Pozzoni, A. Mazzanti, and F. Svelto, "A sliding IF receiver for mm-wave WLANs in 65nm CMOS," in *2009 IEEE Custom Integrated Circuits Conference*. San Jose, CA, USA: IEEE, Sep. 2009, pp. 669–672. [Online]. Available: http://ieeexplore.ieee.org/document/5280754/

[5] Z. Li, J. Chen, H. Li, J. Yu, Y. Lu, R. Zhou, Z. Chen, and W. Hong, "A 220-GHz Sliding-IF Quadrature Transmitter and Receiver Chipset for High Data Rate Communication in 0.13-μm SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 7, pp. 1913–1927, Jul. 2023. [Online]. Available: https://ieeexplore.ieee.org/document/10025412/

[6] S. P. Singh, M. Jafari Nokandi, T. Rahkonen, M. E. Leinonen, and A. Pärssinen, "A 300-GHz Band Sliding-IF I/Q Receiver Front-End in 130-nm SiGe Technology," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 5, pp. 284–294, 2025. [Online]. Available: https://ieeexplore.ieee.org/document/11122561/

[7] C. Wang and G. Rebeiz, "A 2-Channel 136-156 GHz Dual Down-Conversion I/Q Receiver with 30 dB Gain and 9.5 dB NF Using CMOS 22nm FDSOI," in *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. Atlanta, GA, USA: IEEE, Jun. 2021, pp. 219–222. [Online]. Available: https://ieeexplore.ieee.org/document/9490408/

[8] A. Q. Safarian and P. Heydari, "Design and Analysis of a Distributed Regenerative Frequency Divider Using a Distributed Mixer."

[9] W.-C. Lai, S.-L. Jang, and C.-L. Li, "Quadrature Injection-Locked Frequency Divider ÷2 for Radio Frequency Interference Reduction," in *2020 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*. Suzhou, China: IEEE, Jul. 2020, pp. 1–3. [Online]. Available: https://ieeexplore.ieee.org/document/9199774/

[10] J. Kim, S. Lee, and D.-H. Choi, "Injection-Locked Frequency Divider Topology and Design Techniques for Wide Locking-Range and High-Order Division," *IEEE Access*, vol. 5, pp. 4410–4417, 2017. [Online]. Available: http://ieeexplore.ieee.org/document/7805197/

[11] A. Meyer, M. L. Leyrer, C. Ziegler, M. Maier, V. Lammert, and V. Issakov, "A 4.4mW Inductorless 2–20 GHz Single-Ended to Differential Frequency Doubler in 45 nm RFSOI CMOS Technology," in *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. San Diego, CA, USA: IEEE, Jun. 2023, pp. 209–212. [Online]. Available: https://ieeexplore.ieee.org/document/10186178/

[12] L. Jia, J.-G. Ma, K. Yeo, and M. Do, "9.3–10.4-GHz-Band Cross-Coupled Complementary Oscillator With Low Phase-Noise Performance," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 4, pp. 1273–1278, Apr. 2004. [Online]. Available: http://ieeexplore.ieee.org/document/1284798/