ECE60420 Final Project
14-16 GHz Sliding-IF Receiver

Ryan Wans
Purdue University
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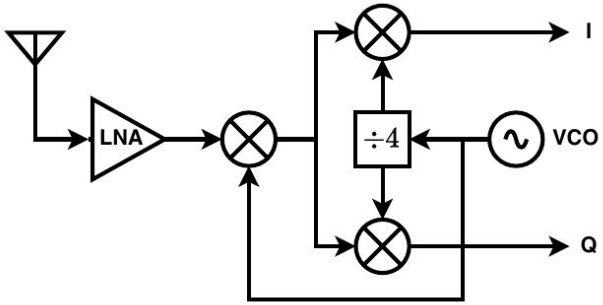
Sliding-IF Receivers

- Dual conversion receiver for I/Q output
- LO controls both mixers via divider
- Growing popularity for modern modulation schemes

- Usually ~20-60nm CMOS or SiGe
- Implementations up to >300 GHz

Prior Approaches:

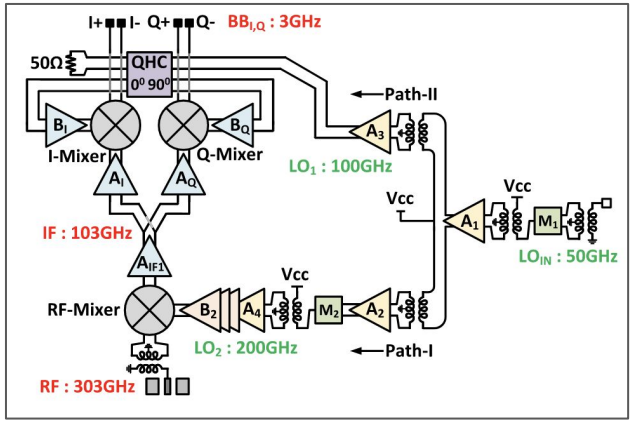
- Cascode LNA, active double-balanced mixers, DFD divider(s), LO off-chip (!)

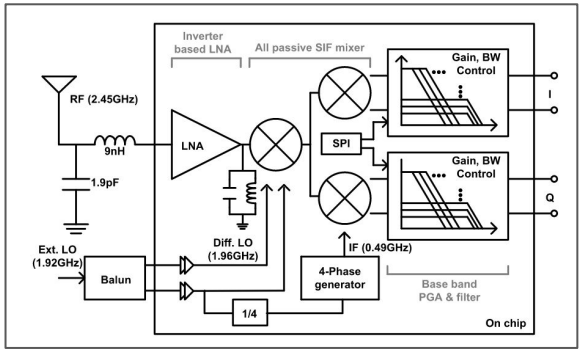


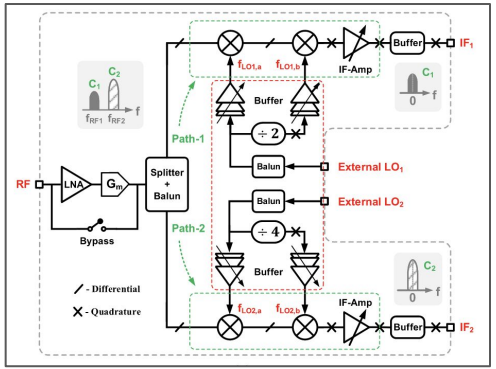
Sliding-IF Receivers

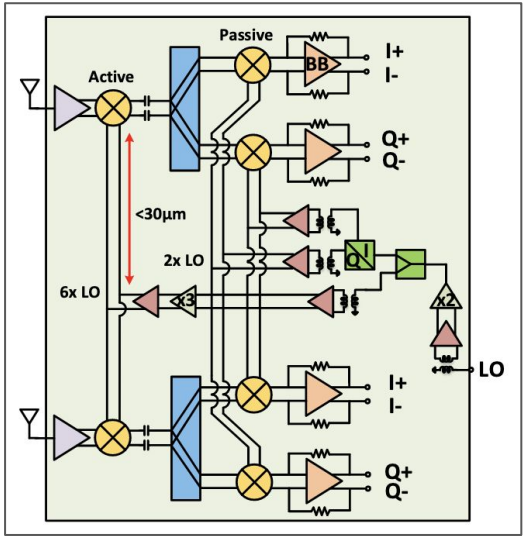
Standard Figures of Merit

- Gain (typ. > 30 dB)
- NF (typ. < 10dB)
- P1dB (typ. < 25 dBm)
- Power (typ. < 100 mW)
- Area (typ. < 1 mm^2)
- LO Phase Noise (typ. < 100 dBc/Hz)









Circuit Analysis & Predictions

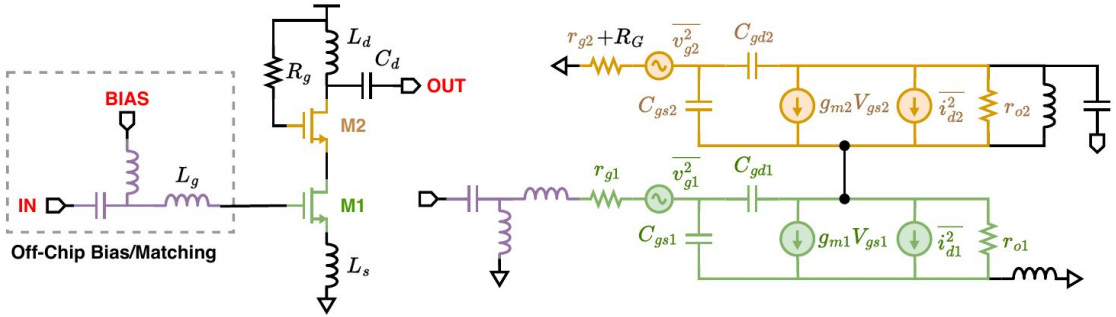
Low Noise Amplifier

Cascode w/ ind. degen.

NF < 1dB and Gain > 20dB

Will have to add shunt C_g

^ GPDK 45nm not super realistic

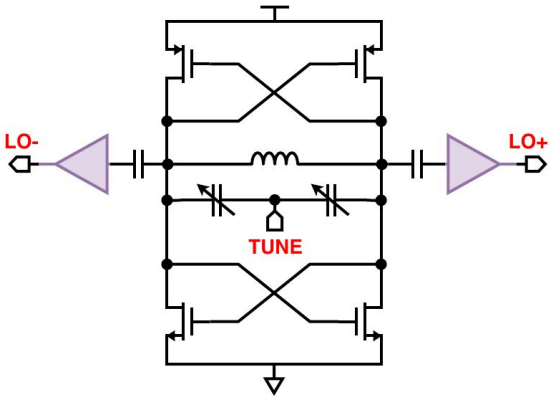


LC-VCO

Want big L for higher Q of tank, want higher C for tuning

NMOS/PMOS XCP for output Z, low I_d, negative g_m

Output buffer to prevent loading, allow biasing/gain



Circuit Analysis & Predictions

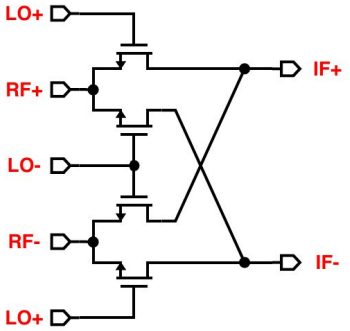
Mixer

Double balanced, passive

High linearity, low noise, low power consumption, low complexity

Low gain: conversion loss >= 3.92 dB

Output sees 2 mixers ⇒ >= 7.84 dB of loss :(



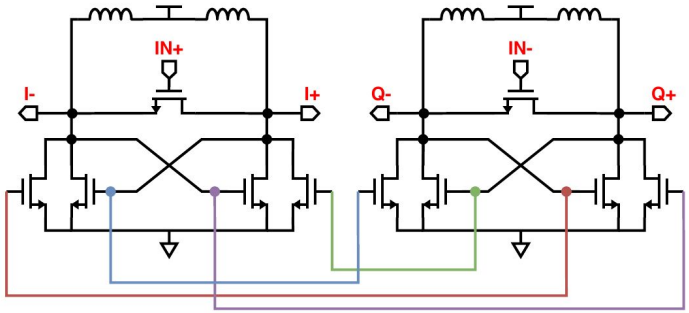
Frequency Divider

Injection-Locked Freq. Div (ILFD)

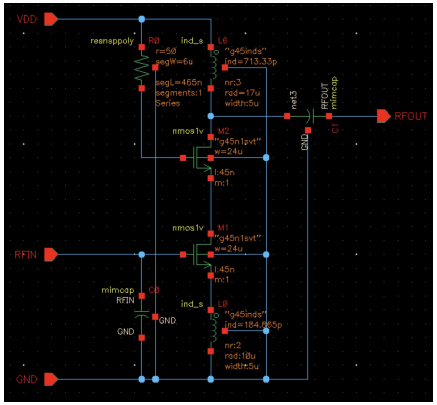
Combined LC-VCO with passive mixer!

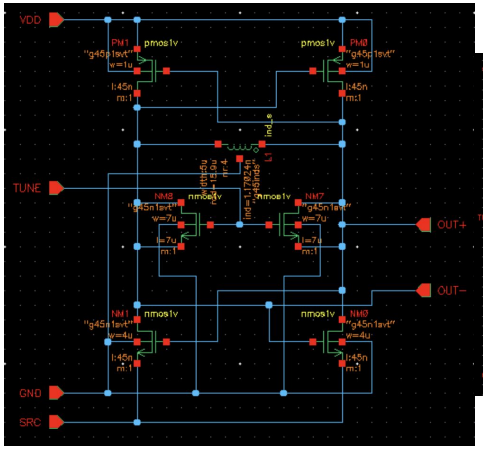
Fold two: allows for 4 -phase quadrature output

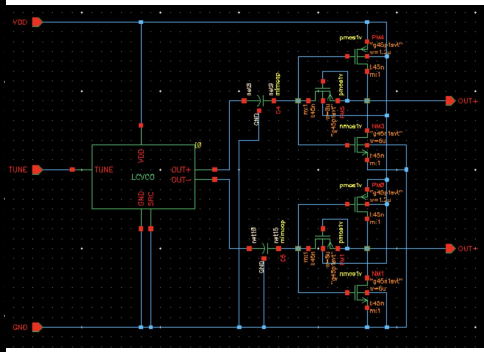
Sizing determines gain, locking range, power cons.



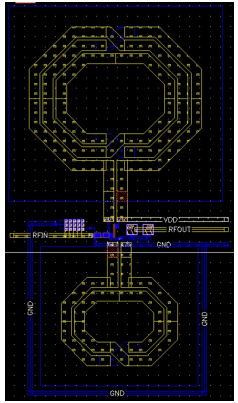
Circuit Design & Layout

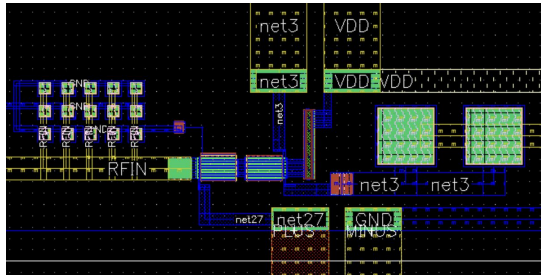




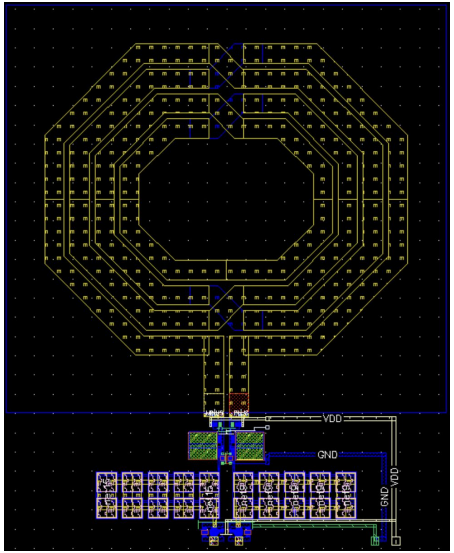


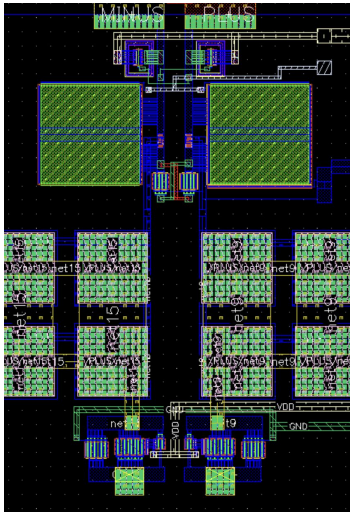
VCO





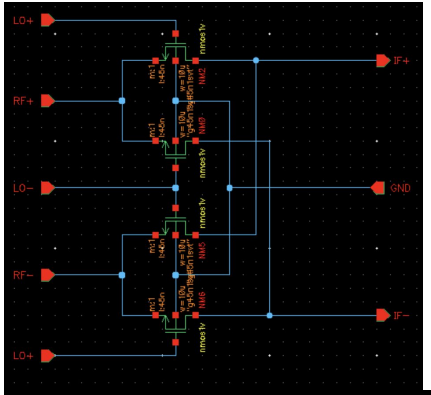
Low Noise Amplifier



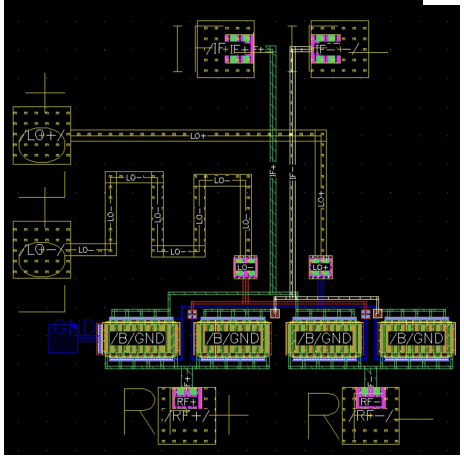


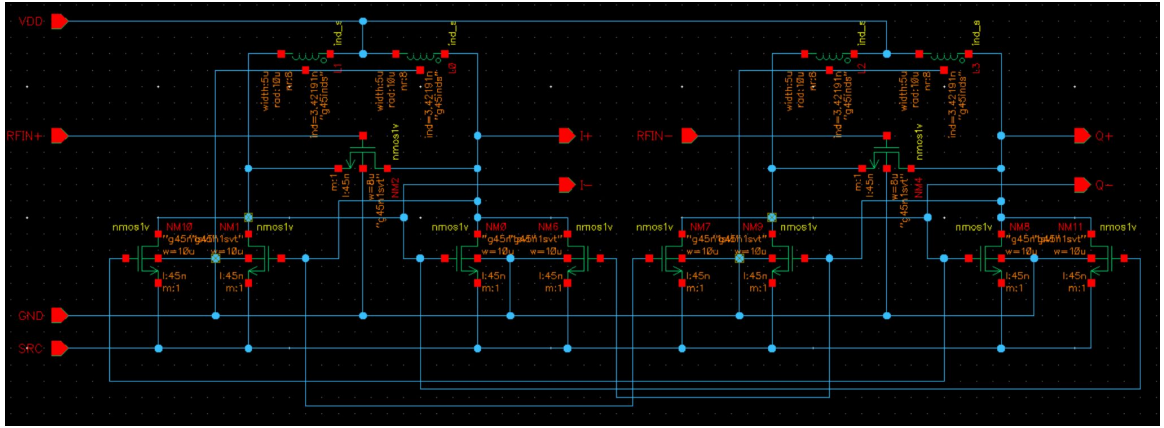
Circuit Design & Layout

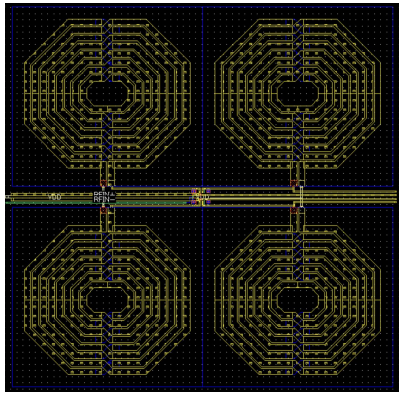
I/Q Div-by-4 ILFD

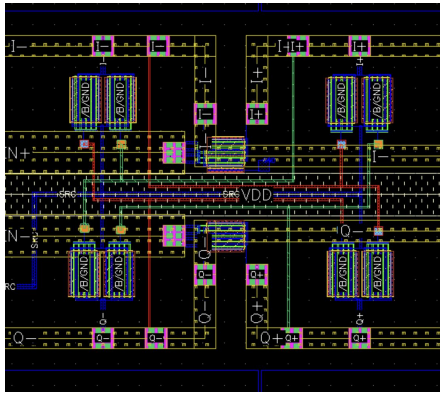


Mixer





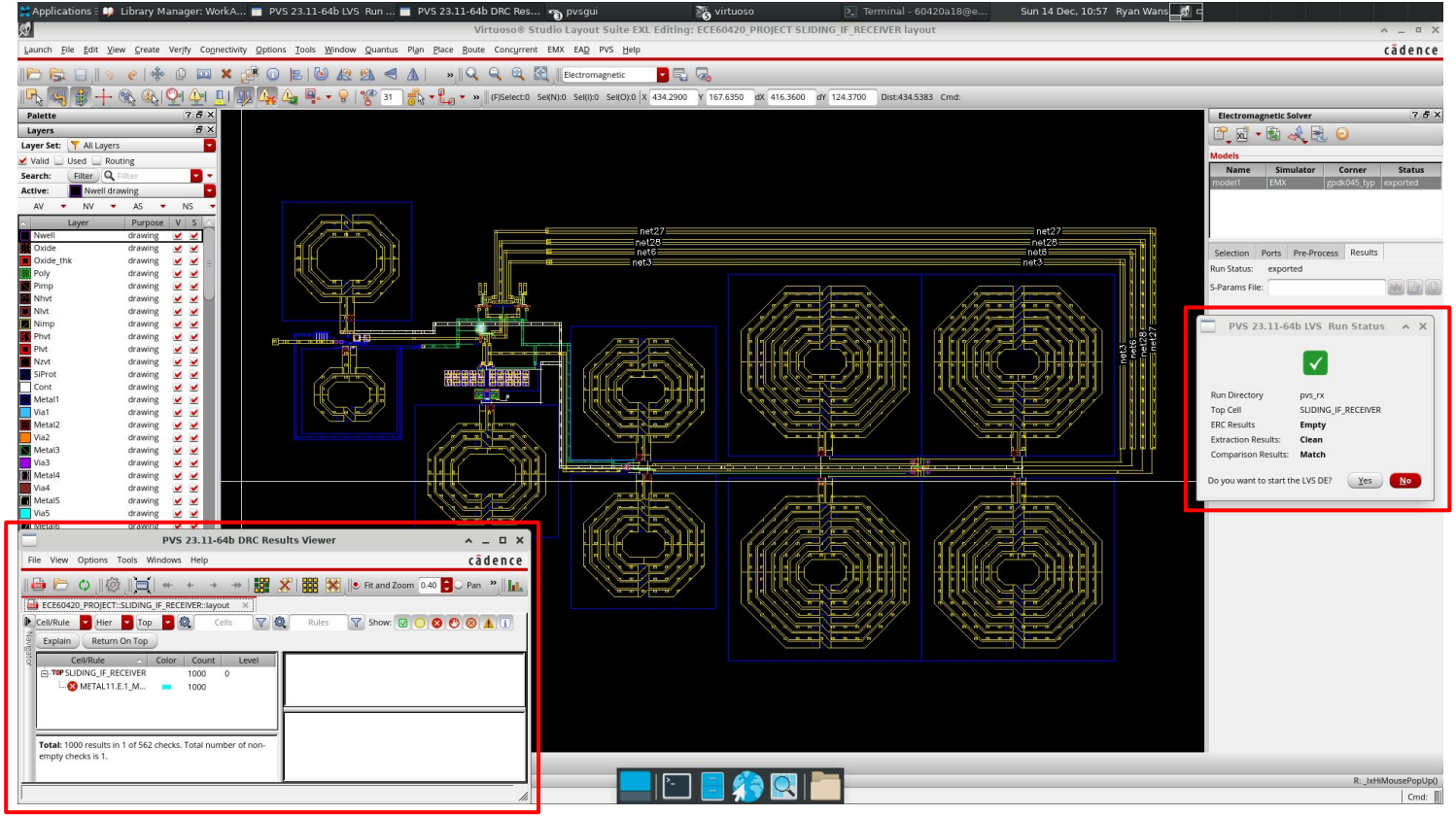




Layout DRC/LVS Results

Minor DRC errors due to poor inductor pcells

Clean :)



Simulation Results (Pre-Layout)

System

- Gain: **-9.2 dB** (no IF amplifiers, passive mixers)
- NF: **9.7/14.2 dB**
- P1dB: **-40 dB**
- Power: **188 mW**
- Input Z: **~50 + j0 Ohms**

VCO

- LO Phase Noise: **-127 dBc/Hz**
- LO Freq. (tune = 0): **12.8 GHz**
- LO Freq. (tune = 1): **10.5 GHz**

LNA

- Center: **15 GHz**
- Gain: **21.4 dB**
- NF: **980 mdB**
- S11: **-10 dB**
- P1dB: **-22 dB**

Simulation Results (Post-Layout)

System

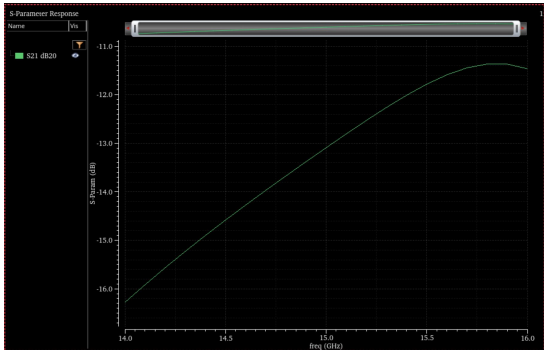
- Gain: **-11.5 dB** (worse)
- NF: **12/16.7 dB** (worse)
- P1dB: **-41.4 dB** (worse)
- Power: **45.8 mW** (better)
- Input Z: **18 + j34 Ohms** (worse)

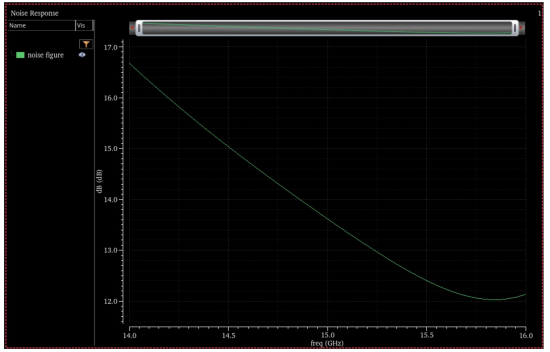
VCO

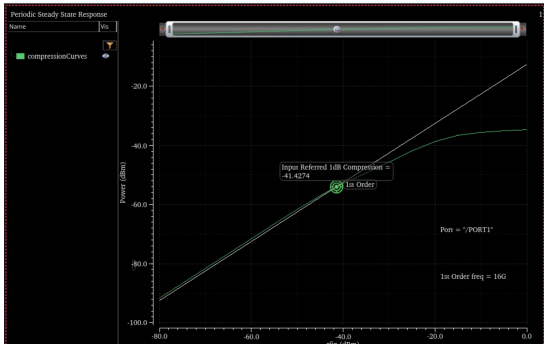
- LO Phase Noise: **-101 dBc/Hz** (worse)
- LO Freq. (tune = 0): **11.5 GHz** (worse)
- LO Freq. (tune = 1): **0 GHz :(** (worse)

LNA

- Center: **14.2 GHz** (worse)
- Gain: **19.2 dB** (worse)
- NF: **1.28 dB** (worse)
- S11: **-7.9 dB** (worse)
- P1dB: **-19.2 dB** (better)







Simulation Results (EMX)

System

- Gain: **-39.4 dB**
- NF: **22.2/23.9 dB**
- P1dB: **pss divergence**
- Power: **11.4 mW**
- Input Z: **26.8 + j31 Ohms**

VCO

- LO Phase Noise: **no start**
- LO Freq. (tune = 0): **no start**
- LO Freq. (tune = 1): **no start**

LNA

- Center: **14.6 GHz**
- Gain: **6.7 dB**
- NF: **1.63 dB**
- S11: **-9.97 dB** (@ 14.15 GHz)
- P1dB: **-14.9 dB**

Conclusion

- Successfully performed sliding-IF down conversion
- Room for improvement with gain, P1dB, and power consumption
- Recommendation: active mixers or IF amplifier, optimize ILFDs

TABLE I
COMPARISON TO STATE-OF-THE-ART SLIDING-IF RECEIVERS

Ref.	Tech.	Freq. (GHz)	Gain (dB)	NF (dB)	P1dB (dBm)	Power (mW)	Area (mm^2)	LO Phase Noise (dBc/Hz) @ 10 MHz Offset
[2]	65nm	5.1-5.9	39	1.9/2.4	-28.5	72	0.56	
[3]	22nm FDSOI	28	37.5	3.5	-31	19.5		
[4]	65nm	61.5-66.5	28	9	-26	80	0.5	-115 @ 64 GHz
[6]	130nm SiGe	187-313	15.2	29.5	-17	406	2	
[7]	22nm SOI	137-156	30	9/10.5	-29	197.5	3.10	
This Work	**45nm**	**14-16**	**-9.2***	**9.7/14.2**	**-40**	**188†**	**0.21**	**-127 @ 16 GHz**

*Passive mixers and no IF amplifier, †Includes frequency dividers