ADC Tutorial

This guide gives instructions for using the pin header on the DE1-SoC board dedicated to analog inputs. The analog inputs (0V-5V or 0V-2.5V depending on configuration) connect to an on board AD7928 ADC which connects to the Cyclone V's FPGA fabric. A driver for the ADC written in System Verilog accompanies this guide. Please refer to the DE1-SoC user manual and the AD7928 datasheet for details not discussed in this document.

Physical and Electrical Interface

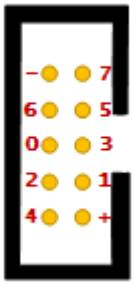

Figure 1: Top down view showing the pinout for DE1-SoC ADC pin header

Figure 1 shows the pinout for the DE1-SoC's ADC pin header. The header has a +5V pin (+), a 0V pin (-), and eight analog channels (0-7). Note that this pinout does not match the DE1-SoC user manual, which is erroneous. Pins 0 and 4 have been swapped in the user manual.

The header for the ADC is a male pin header with a standard 0.1" pitch. It is suggested that these pins be accessed using a compatible female connector; crimp and IDC style connectors with a 0.1" pitch are readily available. Electrically, there are only two special precautions. The first is not to draw too much current from the +5V reference pin. Keep in mind that the +5V reference is not fused. Second, do not to exceed the 0V to +5V input range of the analog inputs. Diodes built into the ADC designed to protect from electrostatic discharge may be damaged by excessive voltages.

FPGA Interface

The FPGA connects to the ADC via four signal lines, a chip select signal from the FPGA, a serial clock signal from the FPGA, a serial data signal from the FPGA, and a serial data signal from the ADC. This guide describes the usage of an accompanying driver and not low level implementation details regarding the four signal lines and their timings.

The ADC driver provides a simple solution for the ADC. Every 67 cycles of the 50MHz clock, the driver produces a sample of data from the ADC. Since each of the eight channels is sampled individually, the driver proceeds in a round robin fashion sampling from each in turn, for a total period of 536 clock cycles. This means that sampling occurs at approximately 91.6

kHz. Data are presented as a packed array of eight numbers, each being twelve bits long. Two options control the behavior of the driver. A RANGE parameter controls the upper limit the ADC can measure, either the reference (+5V) or half that (+2.5V). A CODING parameter controls the encoding, either straight binary, where 0V is zero, or two's complement, where the center value (half of the upper limit) is considered to be zero. A summary of the necessary inputs and outputs to operate the driver is as follows:

- Parameters
  - RANGE – 1'b0: 0V-5V, 1'b1: 0V-2.5V
  - CODING – 1'b0: two's complement, 1'b1: straight binary
- User Inputs
  - clock – 50 MHz clock
  - reset – active high reset signal
- User Outputs
  - data – the values returned by the driver for each channel as a packed array (the System Verilog expression for this type is *wire [7:0][11:0] <name>*)
- Top Level Inputs
  - ADC_CS_N – chip select
  - ADC_DIN – data in
  - ADC_SCLK – serial clock
- Top Level Outputs
  - ADC_DOUT – data out

Users should connect the clock and inputs as well as the data output to their design. The remaining inputs and outputs should connect to top level pins of the same name. Keep in mind that the first dimension of data is the channel number (eight channels) and the second is the bit number (twelve bits). What analog voltage the bits represent is determined by the RANGE and CODING parameters.

Tutorial and code developed by Kyle Gagner working with Jesse Liston and Professor Scott Hauck