**FPGA Board Comparison (Front-End):**

A table comparing the most important performance metrics for the ROACH2 (our current FPGA board type) to the VCU118 is provided below. The VCU118’s FPGA has significantly more resources than the ROACH2 (allowing larger, more computationally intense designs), significantly smaller feature size (simplifying timing-closure), and significantly faster transceivers (allowing higher I/O bandwidth).

One benefit of the ROACH2 over the VCU118 however, is that the ROACH2 was specifically designed by a radio astronomy research and instrumentation organization with radio astronomy applications in mind, whereas the VCU118 is a development board developed by Xilinx whose purpose is to exhibit the full range of the possibilities created by the Virtex Ultrascale+ series chips. Functionally, the one are of the boards where this discrepancy is made obvious is the high-speed transceivers – on the ROACH2 all of the transceivers are connected to expansion bus connectors, whereas many transceivers on the VCU118 are connected to ‘exhibition’ technologies (PCIe, Samtec FireFly) that we do not intend to use on our deployed VCU118s. Despite these ‘wasted’ transceivers, the overall ‘useable’ I/O bandwidth of the VCU118 far exceeds that of the ROACH2.

|  |  |  |
| --- | --- | --- |
| Resource | ROACH2 (Current) | VCU118 |
| FPGA System Logic Cells (K) | 476 | 2586 |
| FPGA DSP Slices | 2016 | 6840 |
| FPGA BRAM (Mb) | 38 | 75.9 |
| Board DDR4 (GB) | 2 | 8 |
| High-Speed Ethernet | 8x10GbE | 3x100GbE |
| FPGA Silicon Feature Size | 40nm | 16nm |
| Expansion Bus | 2xZDOK | 1xFMC, 1xFMC+ |
| Max FPGA transceiver speed (Gbps) | 6.6 | 32.75 |

**ADC Comparison:**

A table comparing performance specifications between our current standard ADC (EV8AQ160) and our prospective standard ADC (AD9213) is provided below. The specifications for the AD9213 are relatively representative of the upcoming generation of high-speed ADCs. As the electronics industry advances, so do ADC technologies – the AD9213 is faster, more precise, and lower-noise than our current deployed technology. One large driver behind the lower Spur-Free Dynamic Range is the improved manufacturer-provided calibration techniques for the suppression of multi-core interleaved spurs that are inherent in pipelined ADC technologies, and have plagued radio astronomy receivers for years.

|  |  |  |
| --- | --- | --- |
| Feature/Spec | E2V EV8AQ160 (Current) | AD AD9213 |
| Max. Sampling Rate (GHz) | 5 | 10.25 |
| Bit-Depth | 8 | 12 |
| Spur-Free Dynamic Range (at max rate) | 56dBc | 68dBc |
| Power Consumption (at max rate) | 4.2W | 5.1W |
| Effective Number of Bits (at max rate, Fin=~1/10Fs) | 7.1 | 8.7 |