**Section II.A.Technical Motivation.Sharing the spectrum**

Despite existing in the center of the federally-defined, 13,000 square-mile “National Radio Quiet Zone”, radio frequency interference (RFI) from a variety of sources (satellites, ground-based RADAR, wireless consumer devices, etc…) is a continual plague upon the data quality at the Green Bank Observatory (GBO) and other radio astronomy observatories around the world. Due to the expanding presence of wireless devices in our lives, and the inevitable pervasiveness of self-driving cars relying on RADAR or similar active-RF methods for guidance, as well as the increasing bandwidth of astronomy receiver systems (and thus the total number of RFI detections per-second), GBO is actively pursuing methods of staying at the forefront of real-time RFI excision techniques.

Due to limitations with existing hardware, we are not able to implement and test/qualify many promising RFI mitigation techniques (ex. Spectral Kurtosis, Machine Learning) – if we were to have access to additional hardware resources, implementing and testing these methods would become possible.

In addition to developments in the number of FPGA resources, there has been great developments in FPGA toolflows and related hardware that fundamentally changes the paradigm of what is possible (see Xilinx SDAccel tool, as well as the Xilinx Alveo and Versal series hardware).

Having access to these new hardware and software platforms outlined in this document will enable the GBO to maintain or increase its position as a world-leader in spectrum-sharing.

**Section II.B.New Hardware**

As mentioned above, the acquisition of new hardware will allow the GBO to make tremendous strides towards becoming truly a world-leader in the next generation of digital backend systems. As these newest generations of technologies become available, many levels of testing and qualification will need to be done to prove the efficacy of new designs – these will be complex problems to define and test, but will inevitably lead to achieving levels of performance (by any useful metric) that are simply not achievable under our current hardware regimes.

The evaluations that we do on different aspects of the cutting-edge hardware will be more widely applicable to other interested observatories (and research institutions) in the national and international community. A small subset of expected investigations is listed below:

1) Custom encoding protocols similar to 8/10b to enable transmission of high bit-rate, high bit-depth ADC outputs to enable lower-overhead (and thus higher-bandwidth) transmission of the digitized signal to the processing units in the server room.

2) Exploration of packet-loss rate (and overall system reliability) on 100GbE networks at high bit-rates, under different topology setups, and with different hardware options

-Exploration of the efficiacy of DWDM and duplex implementations of 100GbE network links – possibly in conjunction with PCIe connections as well

3) Exploration of cooling and RFI-shielding methods and requirements for Xilinx evaluation and production boards

4) Exploration of new ADCs and their calibration methods (as well as spur suppression and channel isolation)

5) Exploration of the logic requirements necessary to implement communication interfaces (100GbE, duplex 100GbE, DWDM 100GbE, PCIe 3x8, PCIe 3x16, PCIE 4x8, FMC, FMC+, etc…) in new Xilinx boards

**Section II.B.Firmware Development**

In light of the variety of new hardware that GBO intends to base future digital backend systems on, a variety of new firmware ‘blocks’ will need to be developed for interfacing with various FPGA-facing peripherals as well as for executing for advanced DSP techniques. In addition, new firmware ‘tools’ may need to be developed to allow our CASPER-based designs to take advantage of the totality of hardware advancements that are provided by Xilinx Ultrascale+ and later technologies. A list of prospective developments is provided below (“Basic EDK” vs. “CASPER EDK” refers to whether the block will need to interface with off-chip peripherals – both categories will be of interest to the wider community):

1) Basic EDK blocks to implement our custom encoding protocols (as listed above) – both for the conversion and for the de-conversion

2) CASPER EDK blocks to interface any custom or Commercial-Off-The-Shelf (COTS) hardware (ADC/GbE/etc…) FMC cards with FPGA boards (custom or COTS)

3) CASPER EDK blocks to interface the Programmable Software (PS) portion of Xilinx MPSoC or RFSoC chips to the Programmable Logic (PL) portion the chips

4) CASPER EDK blocks to interface the FPGA with the various I/O protocols outlined in investigation #5 above

5) Basic EDK blocks to implement the Spectral Kurtosis RFI-excision technique outlined in section II.B.Active RFI Excision  
6) Basic EDK blocks necessary to implement a next-generation Artificial Pulsar for instrument testing (generating, sampling/saving example data-sets)  
7) CASPER EDK blocks to interface DACs with CASPER toolflow

**Section II.B.Protocols/formats for high data rates**

As part of our exploration of future digital backend systems, it is important to evaluate the opportunities and difficulties created by higher BW communication networks and higher bit-per-second data rates coming from the ADCs. To this effect, we propose examining the following topics:

1. Exploring the possibility and overall suitability of Duplexed or DWDM 100GbE links.
2. Exploring the implications of a network topology based on ‘few’ 100GbE links as opposed to ‘many’ 10GbE links.
3. Reliable/fast/low-latency/generalized packet formats for relaying high-speed, high bit-depth ADC samples from a receiver-room based transmitter to a equipment-room based DSP system
4. Evaluation of a PCIe-mounted (gen 3 or 4) FPGA-based card for suitability in larger systems.

**Section II.B.Active RFI excision**

As mentioned in section II.A, the GBO is committed to continuing in its role as a world-leader at spectrum sharing. To that point, a survey of current RFI-excision techniques under development or consideration at the observatory is provided below.

In addition to active techniques for detecting and removing unwanted RFI in real-time, GBO specifically (and the radio astronomy community in general) is in need of a robust and generalized test methodology for validating the ability of any RFI-excision technique to be effective while simultaneously maintaining the scientific quality of the affected data – such a methodology does not exist in the public domain, but would be a great boon to the future of the larger community.

**Impulsive RFI Mitigation:**  
Initially conceived by Cedric Viou at Nancay Observatory as a method for detecting and eliminating interference from ground-based RADAR sources, the GBO digital group has now implemented it in firmware, and has implemented it in multiple backend systems currently being used on-site at Green Bank. Testing is currently underway, but our ability to validate its effectiveness (and to have it become accepted by the wider astronomy community at large) is severely hindered by a lack of formal validation plan like the one outlined above. To the best of our knowledge, GBO currently possesses the only CASPER-implemented real-time RFI-excision enabled backend systems.  
Source: https://arxiv.org/pdf/1703.00473.pdf

**Spectral Kurtosis:**Initially conceived by Gelu Nita at the Center for Solar-Terrestrial Research at New Jersey Institute of Technology as a robust statistical RFI detector, the simple sum/sum-squared algorithm lends itself naturally to implementations in FPGAs. Over the past year, a collaboration between the GBO digital group and West Virginia University (Richard Prestage & Evan Smith) have created a python-based implementation of the “Generalized Spectral Kurtosis Estimator” (source 1). Our current implementation is not real-time, and has been designed specifically on archived (and extensively analyzed) GUPPI-RAW data files – its overall effectiveness has been proven, and while more evaluation is required, we are limited in our ability to do so. Our current data is too small, too old, and too disparately sampled to allow our tests to arrive at a high level of certainty of its effectiveness under varying conditions (especially when initialization/calibration is taken into account). Additionally, none of our existing backend systems have enough overhead in the FPGA chips to allow an HDL implementation to co-exist with the existing firmware – new, larger hardware would enable us to create and test a real-time implementation of this method that could then be shared with the wider community.  
Source 1: <https://arxiv.org/pdf/1005.4371.pdf>

**Machine Learning:**Machine learning is subset of artificial intelligence whos applicability and accesability has increased dramatically in recent years. In response to industry trends, Xilinx has recently taken steps to optimize their hardware (see Zynq Ultrascale+, Alveo, and Versal hardware lines) and software (see Deephi acquisition, Xilinx ML Suite, SDAccel) - to the point where ML algorithms run faster and can be developed much easier than in the recent past. While there has been some discussion about Machine Learning’s possible applications to the astronomical community, there have been few attempts at what could be a relatively ideal and straightforward application of the technology to existing problems of real-time RFI detection/mitigation/classification - GBO intends to explore these as possibilities. In addition, as a by-product of an ongoing decadal analysis of RFI at the GBO site, we have access to 40Million samples of sortable and searchable RFI instances - this will likely be a great starting point for a supervised learning implementation.

**RFI Excision Plan of non-interference (Qualification):**While being able to accurately and precisely detect/remove RFI is an important and difficult problem to solve, it is not necessarily more difficult or important than defining a generic test procedure or methodology for ensuring/testing the general efficacy of specific removal techniques - or their ability to preserve the underlying scientific data of interest. Therefore, GBO proposes to make a concerted effort towards developing a generalized RFI mitigation test/qualification methodology/test procedure.